STM32 COURSE
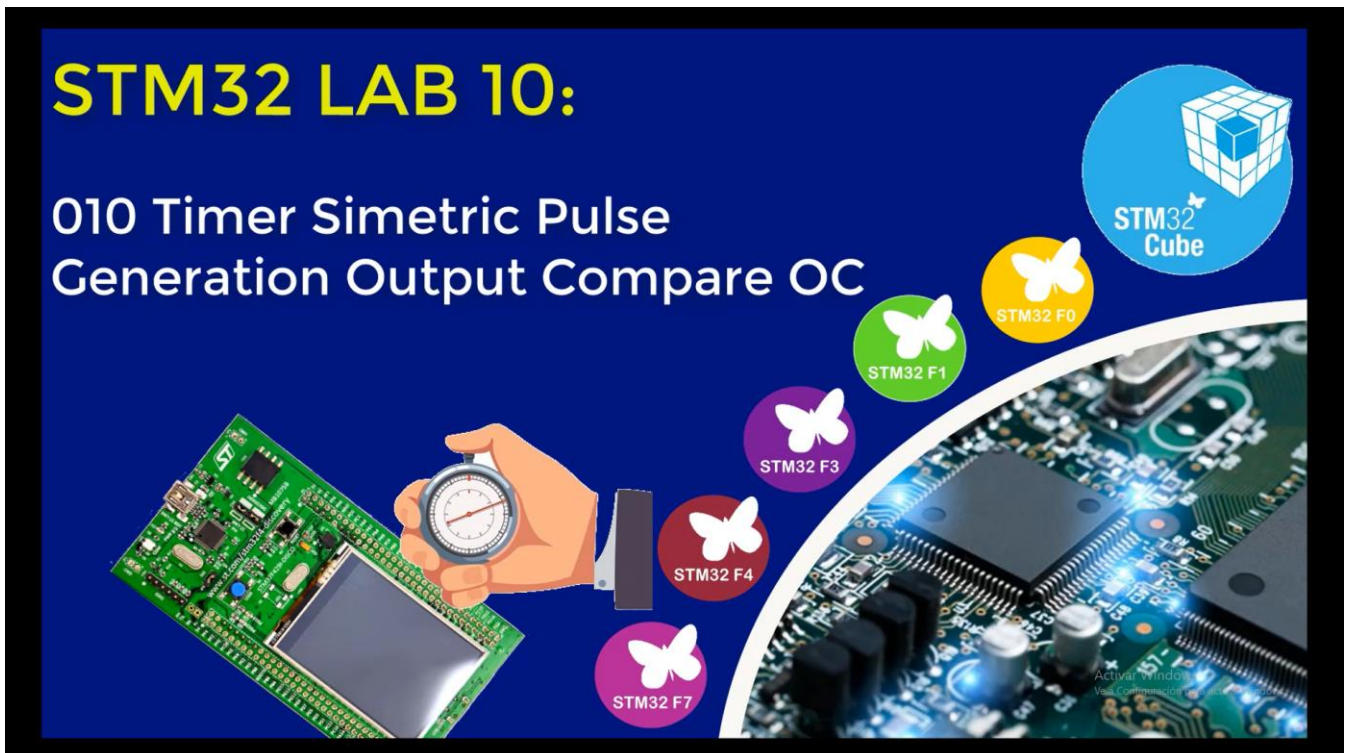
010 Timer Pulse Simetric Generator Output Compare OC
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SECTION 10

010 Timer Pulse Simetric Generator Output Compare OC


What will we learn?

In this video we will generate a pulse train signal using the Output Capture Timer feature, we will do this at a low frequency, the program will start generating the programmed signal at a certain frequency and we will enable the user button input to stop the generation of pulses, the generated pulse train is period symmetric, that is, the same time at the high and low level ttl.

> *"We will use HAL Drivers, which will help us greatly to port and recycle code routines from one processor in one Family to another in another Family."*
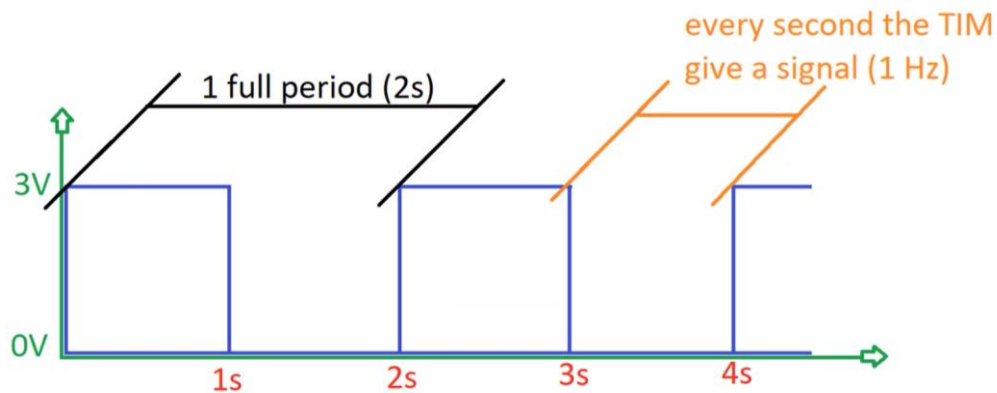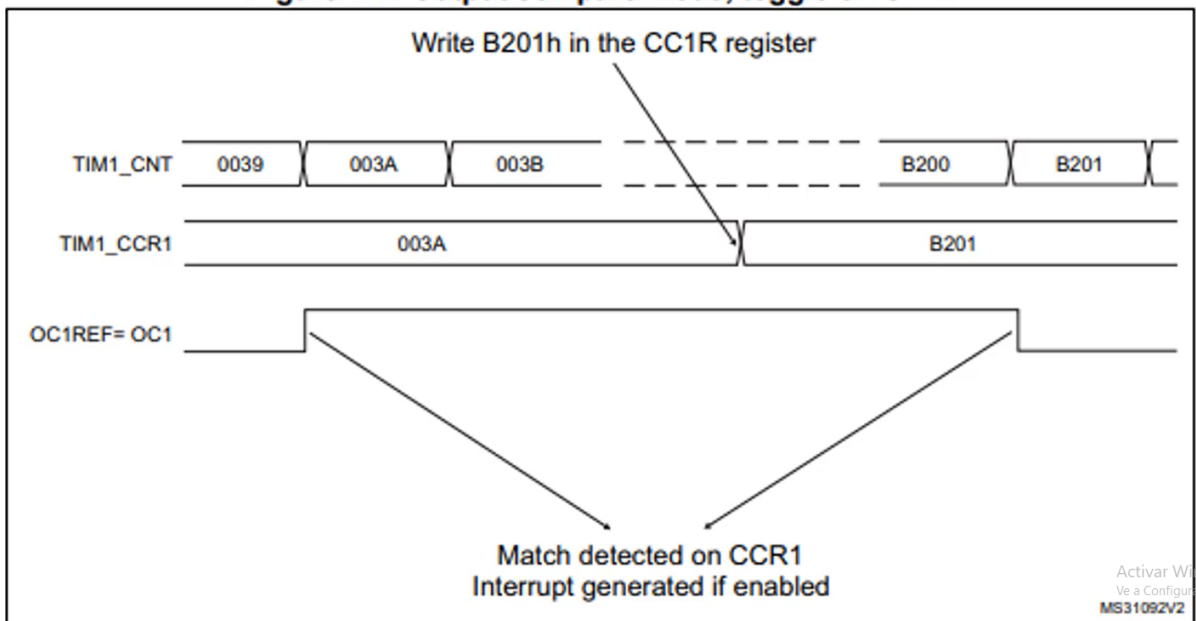
SIGNAL GENERATED

CRITERION

Figure 117. Output compare mode, toggle on OC1.

When the timer counter TIM1-> CNT restarts, that is, it overflows its value, then the output channel (Output Capture Channel) changes state by selecting Toggle, if we generate a Timer signal at 1 Hz we will actually have 1 second in high and 1 second low, this means that a complete period is 2 seconds, which we can say that in reality the frequency generated is actually 0.5 Hz.