Jameco Part Number 1383736

- **Operating Range 2-V to 5.5-V V_{CC}**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54AHC14 . . . J OR W PACKAGE
SN74AHC14 . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y
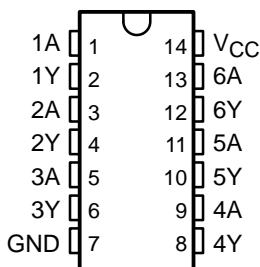
SN74AHC14 . . . RGY PACKAGE
(TOP VIEW)

1A V_{CC}

1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A

GND 4Y
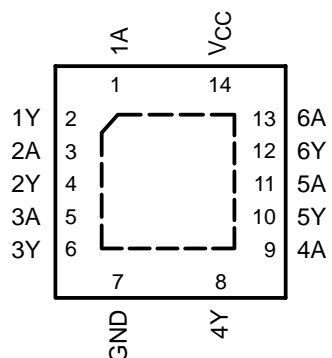
SN54AHC14 . . . FK PACKAGE
(TOP VIEW)

1Y 1A NC V_{CC} 6A

2A	4	18	6Y
NC	5	17	NC
2Y	6	16	5A
NC	7	15	NC
3A	8	14	5Y

3Y GND NC 4Y 4A

NC – No internal connection

description/ordering information

The 'AHC14 devices contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AHC14RGYR	HA14
	PDIP – N	Tube	SN74AHC14N	SN74AHC14N
	SOIC – D	Tube	SN74AHC14D	AHC14
		Tape and reel	SN74AHC14DR	
	SOP – NS	Tape and reel	SN74AHC14NSR	AHC14
	SSOP – DB	Tape and reel	SN74AHC14DBR	HA14
	TSSOP – PW	Tube	SN74AHC14PW	HA14
		Tape and reel	SN74AHC14PWR	
	TVSOP – DGV	Tape and reel	SN74AHC14DGVR	HA14
–55°C to 125°C	CDIP – J	Tube	SNJ54AHC14J	SNJ54AHC14J
	CFP – W	Tube	SNJ54AHC14W	SNJ54AHC14W
	LCCC – FK	Tube	SNJ54AHC14FK	SNJ54AHC14FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
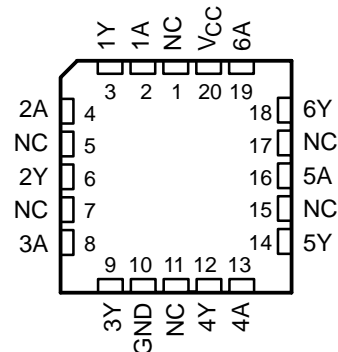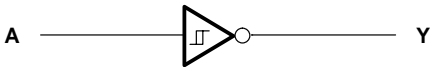
TEXAS INSTRUMENTS

SN54AHC14, SN74AHC14
HEX SCHMITT-TRIGGER INVERTERS

SCLS238I – OCTOBER 1995 – REVISED JULY 2003

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)

A   Y

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
(see Note 2): DB package .... 96°C/W
(see Note 2): DGV package .... 127°C/W
(see Note 2): N package .... 80°C/W
(see Note 2): NS package .... 76°C/W
(see Note 2): PW package .... 113°C/W
(see Note 3): RGY package .... 47°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			SN54AHC14		SN74AHC14		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		−50		−50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		−4		−4	mA
		$V_{CC} = 5$ V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		4		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8		8	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54AHC14		SN74AHC14		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage		3 V	1.2		2.2	1.2	2.2	1.2	2.2	V
		4.5 V	1.75		3.15	1.75	3.15	1.75	3.15	
		5.5 V	2.15		3.85	2.15	3.85	2.15	3.85	
V_{T-} Negative-going input threshold voltage		3 V	0.9		1.9	0.9	1.9	0.9	1.9	V
		4.5 V	1.35		2.75	1.35	2.75	1.35	2.75	
		5.5 V	1.65		3.35	1.65	3.35	1.65	3.35	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		3 V	0.3		1.2	0.3	1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	0.5	1.6	
V_{OH}	$I_{OH} = -50\ \mu A$	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	$I_{OH} = -4\ mA$	3 V	2.58			2.48		2.48		
	$I_{OH} = -8\ mA$	4.5 V	3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50\ \mu A$	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	$I_{OL} = 4\ mA$	3 V			0.36		0.5		0.44	
	$I_{OL} = 8\ mA$	4.5 V			0.36		0.5		0.44	
I_I	$V_I = 5.5$ V or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20		20	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0$ V.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3$ V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$			SN54AHC14		SN74AHC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15$ pF		8.3**	12.8**	1**	15**	1	15	ns
t_{PHL}					8.3**	12.8**	1**	15**	1	15	
t_{PLH}	A	Y	$C_L = 50$ pF		10.8	16.3	1	18.5	1	18.5	ns
t_{PHL}					10.8	16.3	1	18.5	1	18.5	

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5$ V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$			SN54AHC14		SN74AHC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15$ pF		5.5**	8.6**	1**	10**	1	10	ns
t_{PHL}					5.5**	8.6**	1**	10**	1	10	
t_{PLH}	A	Y	$C_L = 50$ pF		7	10.6	1	12	1	12	ns
t_{PHL}					7	10.6	1	12	1	12	

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

TEXAS INSTRUMENTS

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC14			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	9	pF

TEXAS
INSTRUMENTS

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9680201Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9680201QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9680201QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-9682001QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9682001QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN74AHC14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74AHC14DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC14NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC14NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74AHC14PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
SN74AHC14PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC14RGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74AHC14RGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SNJ54AHC08J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AHC08W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54AHC14FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AHC14J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AHC14W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
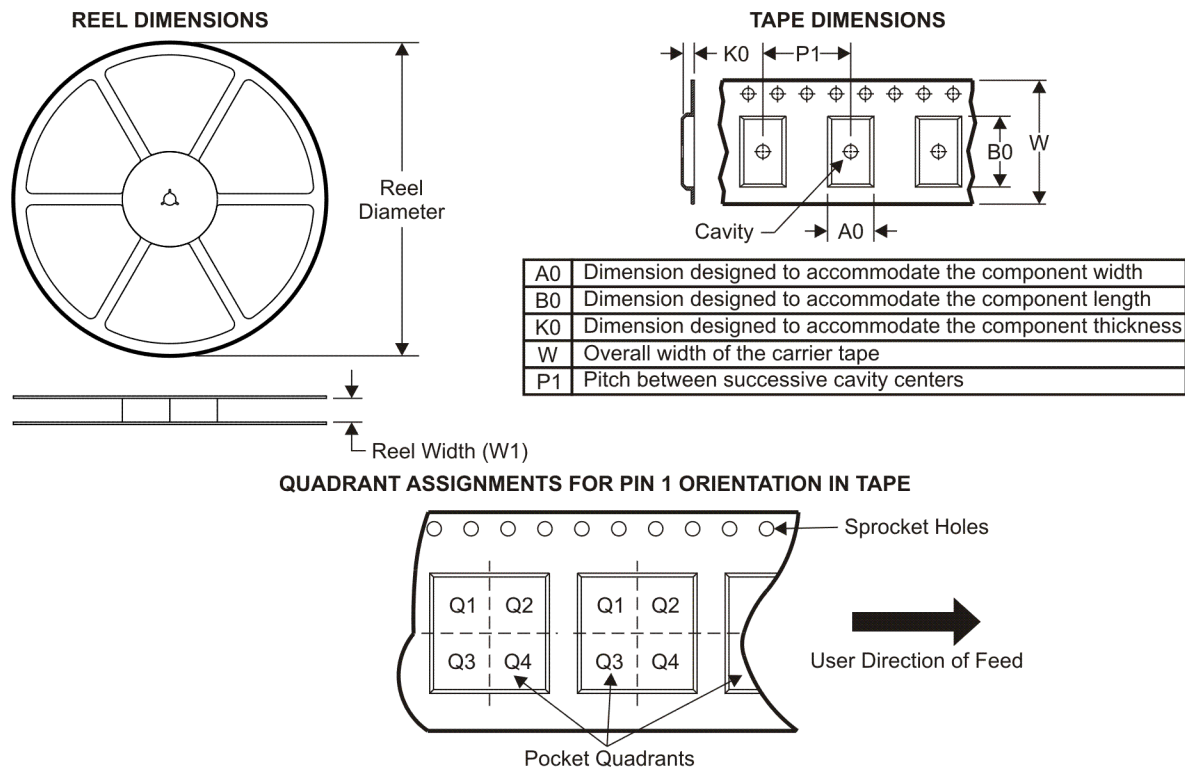**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC14DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC14DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC14NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC14PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74AHC14RGYR	QFN	RGY	14	1000	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
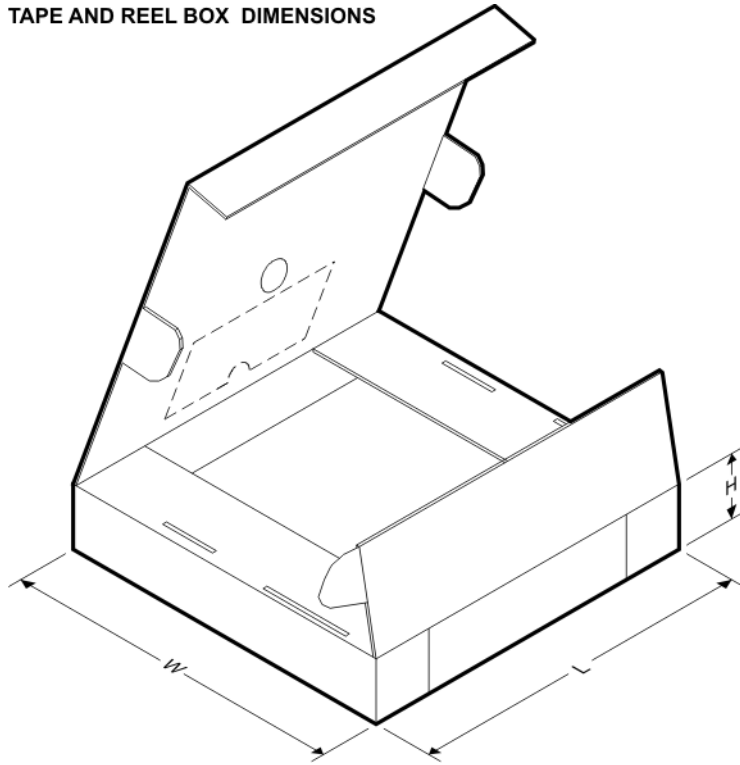
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC14DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74AHC14DGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74AHC14DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74AHC14DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74AHC14NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74AHC14PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74AHC14RGYR	QFN	RGY	14	1000	190.5	212.7	31.8

DB (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

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PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

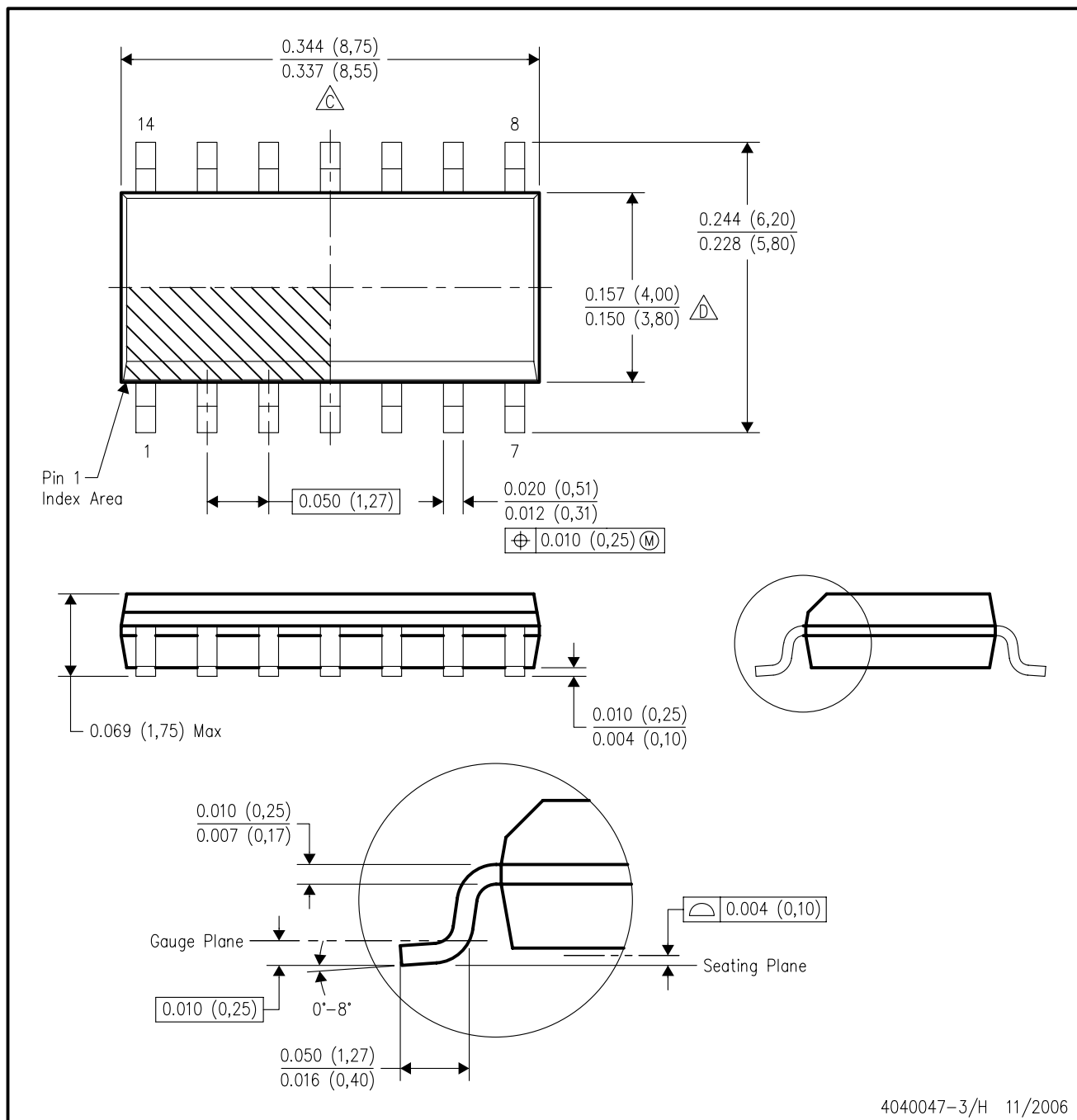| DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97
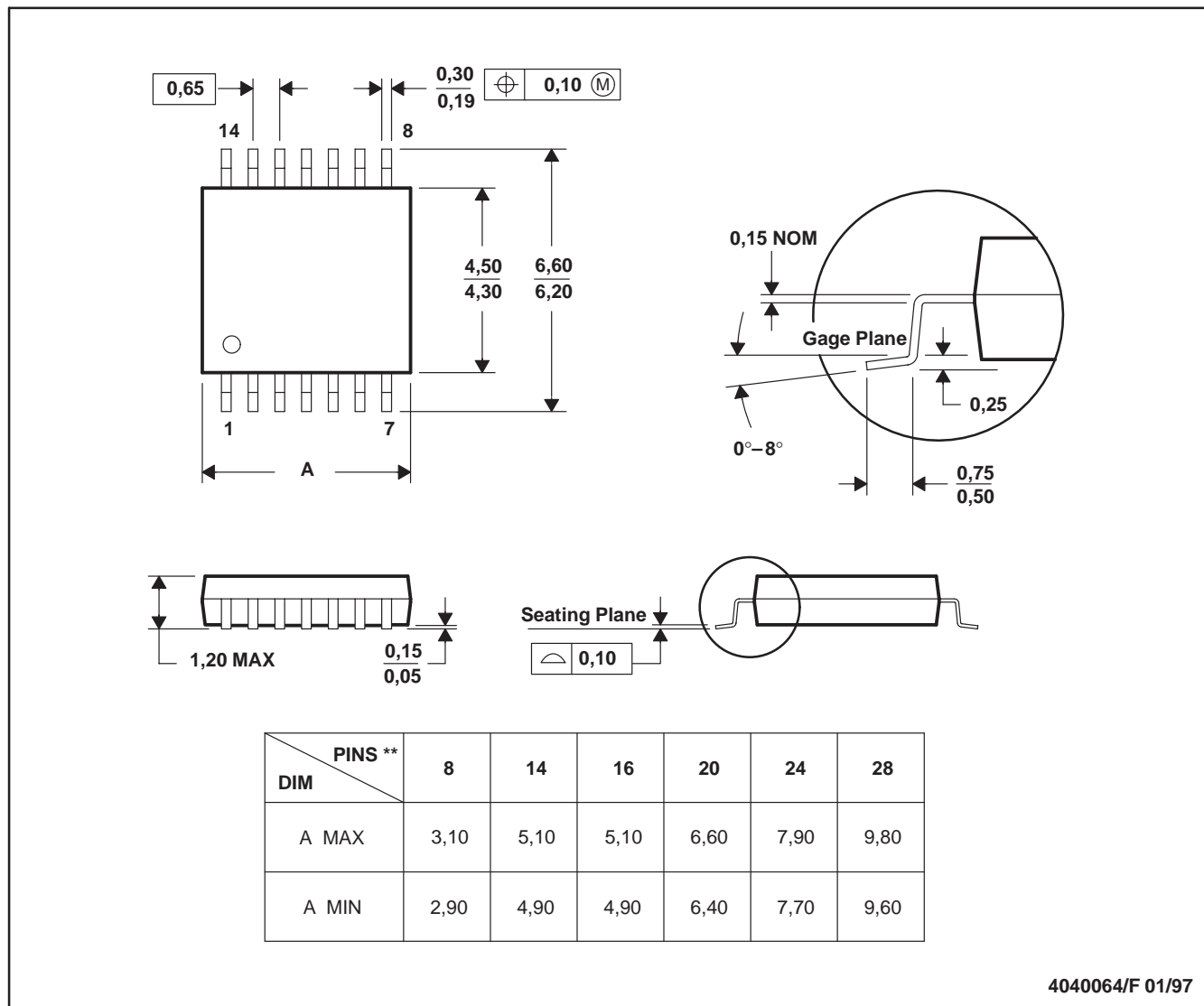
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN
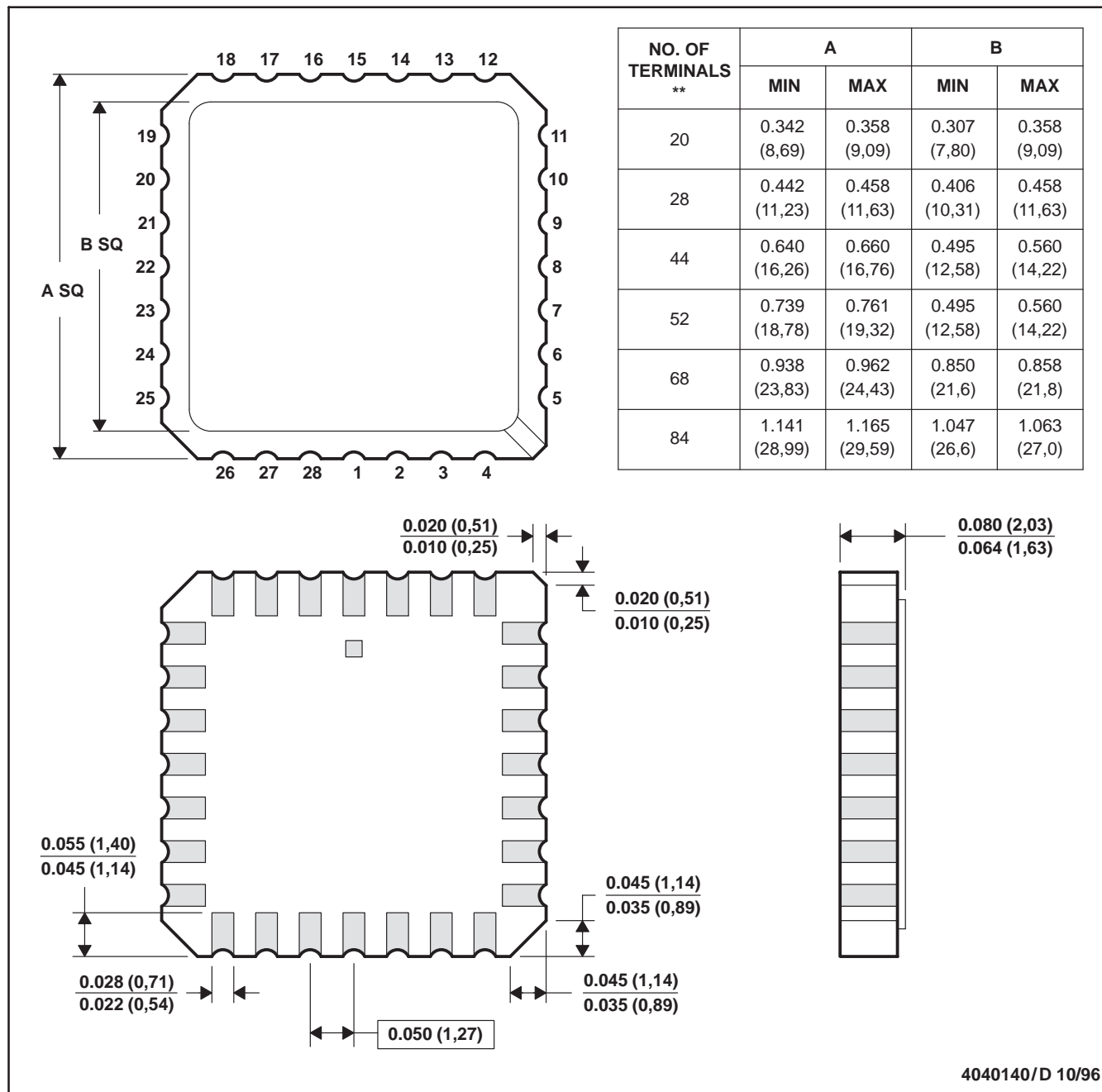
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
           B. This drawing is subject to change without notice.
           C. This package can be hermetically sealed with a metal lid.
           D. The terminals are gold plated.
           E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS

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MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN
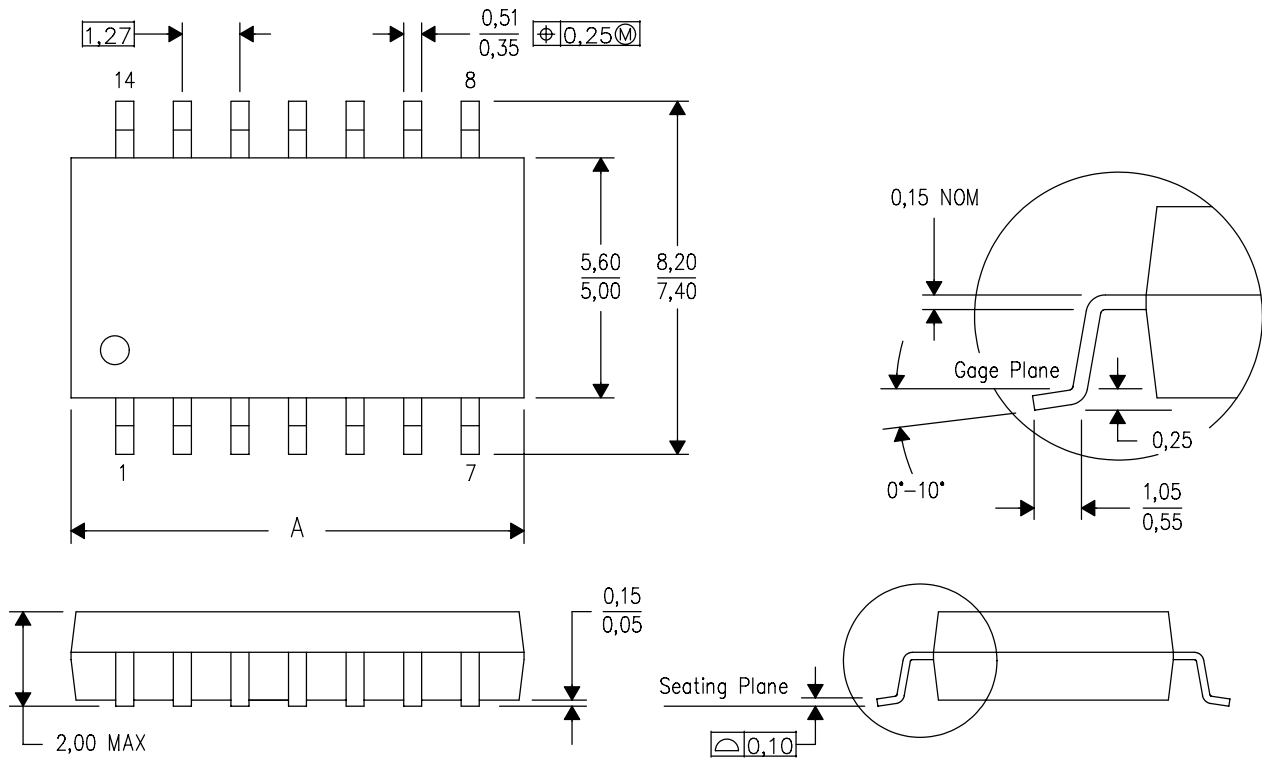
DIM	PINS **	14	16	20	24
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

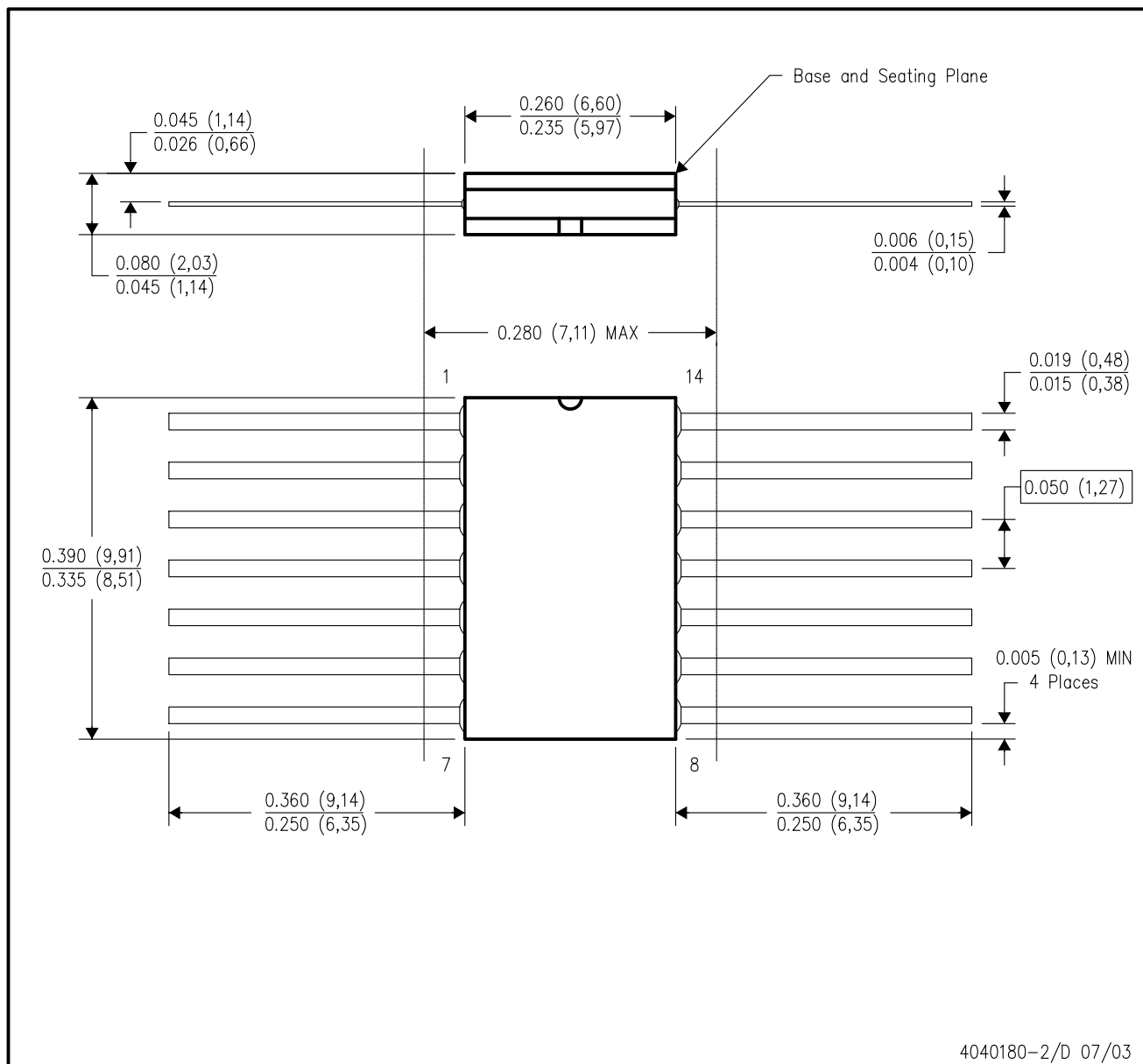| PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
                                14/16/20/56 Pins – MO-194

D (R−PDSO−G14)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)
△C

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/H 11/2006

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
     △C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed .006 (0,15) per end.
     △D   Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
         E.   Reference JEDEC MS−012 variation AB.

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RGY (S−PQFP−N14)   **PLASTIC QUAD FLATPACK**

Pin 1 Index Area
Top and Bottom

⟨E⟩

0,20 Nominal
Lead Frame

Seating Plane

Seating Height

Exposed Thermal Pad

⟨D⟩

Bottom View

4203539−2/G   04/2005
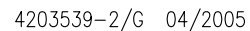
NOTES:
   A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
   B. This drawing is subject to change without notice.
   C. QFN (Quad Flatpack No−Lead) package configuration.
  ⟨D⟩ The package thermal pad must be soldered to the board for thermal and mechanical performance.
  ⟨E⟩ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
     The Pin 1 identifiers are either a molded, marked, or metal feature.
   F. Package complies to JEDEC MO−241 variation BA.

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THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No−Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
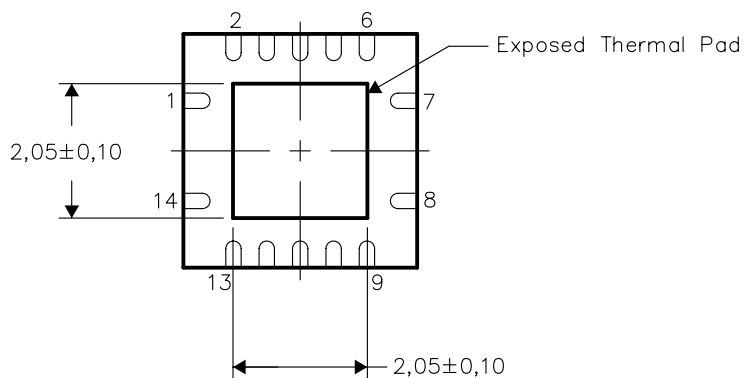
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R−PQFP−N14)

Example Board Layout

4,30

4,30

2,60

1,50

2,05

2,05

Note D

0,50

0.28

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,25

4,25

2,65

1,50

0,82 SG

0,80

0,80 x 14 PL.

0,50

0,23 x 14 PL.

64% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07

0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6x∅0,3

4208122−2/C 09/06

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout. These documents are available at
www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

W (R−GDFP−F14)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.260\ (6,60)}{0.235\ (5,97)}$

$\dfrac{0.080\ (2,03)}{0.045\ (1,14)}$

$\dfrac{0.006\ (0,15)}{0.004\ (0,10)}$

0.280 (7,11) MAX

1   14

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

0.050 (1,27)

$\dfrac{0.390\ (9,91)}{0.335\ (8,51)}$

0.005 (0,13) MIN
4 Places

7   8

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$ $\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

4040180−2/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within MIL STD 1835 GDFP1−F14 and JEDEC MO−092AB

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.