MiniRISC Reference Data



CORE INST	TRUCTION SET			Load Word W R[rd] = M[R[r1] + imm]		
NAME	MNEMONIC	FORMAT	OPERATION	Store Word sw SB $M[R[r1] + imm] = R[r2]$		
ADD	add	R	R[rd] = R[r1] + R[r2]	Jump j J R[rd] = PC + 4; PC = {imm,2'b00}		
SUB	sub	R	R[rd] = R[r1] - R[r2]			
XOR	xor	R	R[rd] = R[r1] ^ R[r2]	Jump jr I if {R[r1] != R[r2]} {PC += register {imm,2'b00}}		
OR	or	R	R[rd] = R[r1] R[r2]	$ \begin{array}{lll} \text{Branch} == & \text{beq} & \text{SB} & \text{if } \{R[r1] == R[r2]\} \left\{\text{PC} += \left\{\text{imm,2'b00}\right\}\right\} $		
AND	and	R	R[rd] = R[r1] & R[r2]	Branch != bne SB if $\{R[r1] != R[r2]\} \{PC += \{imm, 2'b00\}\}$		
Shift Left Logical	sll	R	R[rd] = R[r1] << R[r2]	Branch < blt SB if {R[r1] < R[r2]} {PC += {imm,2'b00}}		
Shift Righ Logical	t srl	R	R[rd] = R[r1] >> R[r2]	Branch \leq bge SB if $\{R[r1] >= R[r2]\} \{PC += \{imm, 2'b00\}\}$		
Shift Left Arith*	sla	R	R[rd] = R[r1] << R[r2]	PSEUDOINSTRUCTION SET		
Shift Righ Arith*	t sra	R	R[rd] = R[r1] >> R[r2]	NAME MNEMONIC		
Set Less Than	slt	R	R[rd] = (R[r1] < R[r2])? 1:0	No nop operation		
ADD Immediate	addi e	1	R[rd] = R[r1] + imm	BASIC INSTRUCTION FORMATS		
XOR Immediate	xori e	I	R[rd] = R[r1] ^ imm	R rd r1 r2 f6 f4 opcode 31 26 25 20 19 14 13 87 4 3 rd		
OR Immediate	ori e	I	R[rd] = R[r1] imm	I rd r1 imm f4 op code 31 26 25 20 19 87 43 (
AND Immediate	andi e	I	R[rd] = R[r1] & imm	SB imm r1 r2 imm f4 opcode 31 26 25 20 19 14 13 87 4 3 opcode 31 26 25 20 19 14 13 87 4 3 opcode 32 opcode 33 opcode 34 opcode		
Shift Left Logical Im	slli nm	I	R[rd] = R[r1] << imm	J rd imm f4 op code 31 2625 87 43 (
Shift Righ Logical Im		1	R[rd] = R[r1] >> imm	MEMORY ALLOCATION		
Shift Left Arith Imm	slai	I	R[rd] = R[r1] << imm	0x0000 0FFF Stack and heap		
Shift Righ Arith Imm		1	R[rd] = R[r1] >> imm	0x0000 0880		
Set Less Than Imm	slti	1	R[rd] = (R[r1] < imm)?1:0	0x0000 0480 0x0000 047F		
Ecall	ecall	I	imm = argumento	0x0000 0080 0x0000 007F 0x0000 0000 Periferics		

OPCODES AND SIGNALS

Instruction Type	Op code	PC Src	Reg Write	ALU Src	Mem Write	Mem ToReg
R	0000	00	1	0	0	1
ı	0001	00	1	1	0	1
L	0010	00	1	1	0	0
Jr	0011	10	0	1	0	0
S	0100	00	0	1	1	1
В	0101	01	0	0	0	0
J	0111	01	0	0	0	0

Instruction	F4	ALUOperation			
Add/Addi	0000	0000			
Xor/Xori	0001	0001			
Or/Ori	0010	0010			
And/Andi	0011	0011			
SII/SIIi	0100	0100			
Srl/Srli	0101	0101			
Sla/Slai	0110	0110			
Sra/Srai	0111	0111			
Sit	1000	1000			
Sub	1001	1001			

PERIPHERALS AVAILABLE

Timers

- Timer 0 and Timer 1;
- Each one has a specific max count;
- The counting is triggered separately for each timer
- An interruption is triggered when counting reaches the end.

GPIO

- Set of 32 pins made available to the user for general purpose;
- Can be configured freely as input or output and used during program execution;
- Triggers an interruption when an input changes its logical value.