



Review Article

## Spintronics technology: A comprehensive review of materials, applications, and future trends

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ABSTRACT

Utilizing the combination of electron spin and the electric field, spintronic technology has become a revolutionary way to overcome the drawbacks of traditional charge-based electronics, such as power inefficiency and performance saturation. This paper reviews recent breakthroughs in spintronics, which have achieved ultrafast switching speeds and ultra-low energy consumption in magnetic tunnel junctions. By integrating advanced materials, such as topological insulators, two-dimensional ferromagnets, and heavy metals, we found the room-temperature stabilization of skyrmions with storage densities exceeding  $1\text{ Tb/in}^2$ , enabling high-density nonvolatile memory. Furthermore, a hybrid complementary metal-oxide semiconductor-spintronic architecture is discussed, which reduces power consumption by 30 % in neuromorphic computing applications while maintaining compatibility with existing semiconductor technologies. Key innovations, such as optimized cobalt-iron-boron/magnesium oxide interfaces for tunneling magnetoresistance ratios exceeding 300 %, efficient spin-charge conversion in heavy metals, and voltage-controlled skyrmion devices for sub-0.1 pJ/bit operation, are also discussed. These advancements address scalability, thermal stability, and fabrication challenges, positioning spintronics as a cornerstone for next-generation memory, logic devices, and quantum computing. We also found that spintronic neuromorphic systems can achieve 20 TOP/s/w, outperforming traditional artificial intelligence accelerators. At the same time, spin qubits with 99.9 % fidelity offer a scalable pathway to quantum computing, underscoring spintronics' potential to revolutionize artificial intelligence, the Internet of Things, and quantum technologies, providing energy-efficient, high-performance solutions for the post-Moore era. Future efforts will focus on three-dimensional magnetic tunnel junction stacking with densities exceeding  $1\text{ Tb/mm}^3$ , and defect-tolerant materials for large-scale commercialization.

### 1. Introduction

SPINTRONICS is a methodology that exploits the spin property of electrons rather than their charge characteristic and prioritizes data storage. Fundamental to the discipline of spintronics, the concept of electron spin provides an additional degree of flexibility for manipulating and storing information beyond that of traditional charge-based electronics. There are conventional and quantum mechanical ways to explain electron spin, which has two potential orientations, spin-up ( $+ \frac{1}{2}$ ) and spin-down ( $- \frac{1}{2}$ ), traditionally represented as an intrinsic angular momentum. It is usually described as vectors pointing between the north (N) and south (S) magnetic poles, illustrating the way spin alignment underpins magnetic phenomena in materials. The Bloch sphere framework, which

represents the spin state as a point on the surface of a sphere, provides a more realistic description of electron spin in terms of quantum mechanics. The spin state can exist in a superposition of spin-up and spin-down projections, and the quantization axis is the z-axis of the Bloch sphere. The quantum character of spin and its potential for information encoding in both quantum and classical spintronic devices are demonstrated by the direction and precession of the spin vector on the Bloch sphere. A thorough understanding of spin-dependent processes in spintronics is provided by Fig. 1, where challenges such as leakage currents, thermal dissipation, and performance saturation have become increasingly pronounced. For example, at advanced complementary metal-oxide semiconductor (CMOS) nodes, static power consumption (leakage) has become a significant contributor to overall energy

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consumption, severely limiting the scalability of contemporary computer systems [1].

In this context, spintronics, a technology that exploits the spin degree of freedom of electrons and their charge, has emerged as a transformative alternative. By leveraging the intrinsic quantum properties of electrons, spintronics offers the potential for nonvolatile memory, ultra-low power consumption, and high-speed operation, addressing the limitations of conventional electronics. Spintronic devices, such as magnetic tunnel junctions (MTJs) and spin-transfer torque magnetic random-access memory (STT-MRAM), have already demonstrated significant advantages over traditional memory techniques.

STT-MRAM has emerged as a promising nonvolatile memory technology due to its low energy consumption and high endurance [2]. M. Davoudinya et al. report that STT-MRAM achieves write energy as low as 0.4 pJ/bit through optimized perpendicular magnetic tunnel junction (pMTJ) designs, with recent advancements further reducing it to  $\sim 0.3$  pJ/bit [3]. Additional studies highlight hybrid STT-assisted spin-orbit torque (SOT)-MRAM designs that achieve sub-0.5 pJ/bit power consumption [4]. Furthermore, other high-density STT-MRAM implementations have demonstrated endurance exceeding  $10^{12}$  cycles [5]. These properties are enabled by the efficient manipulation of electron spin states, as depicted in Fig. 1, where part (a) shows classical spin alignment and part (b) illustrates quantum superposition, critical for low-power switching. Despite these promising developments, several challenges remain. The scalability of spintronic devices is hindered by material limitations, e.g., platinum (*Pt*) and tantalum (*Ta*), and the thermal instability of magnetic layers at nanoscale dimensions. For example, MTJs with interfaces of magnesium oxide (*MgO*) and cobalt-iron-boron (*CoFeB*) can exhibit exceptional tunneling magnetoresistance (TMR) ratios of 300 %; however, this high performance requires precise control of the *MgO* barrier thickness at the sub-1 nm scale [6]. By fusing the scalability of CMOS with the non-volatility of spintronics, hybrid CMOS-spintronic architectures offer a viable solution to reduce the von Neumann bottleneck [7]. Nevertheless, the actual implementation of this hybrid technique poses significant fabrication challenges, including managing interfacial defects in complex material stacks, ensuring thermal budget compatibility during integration, and

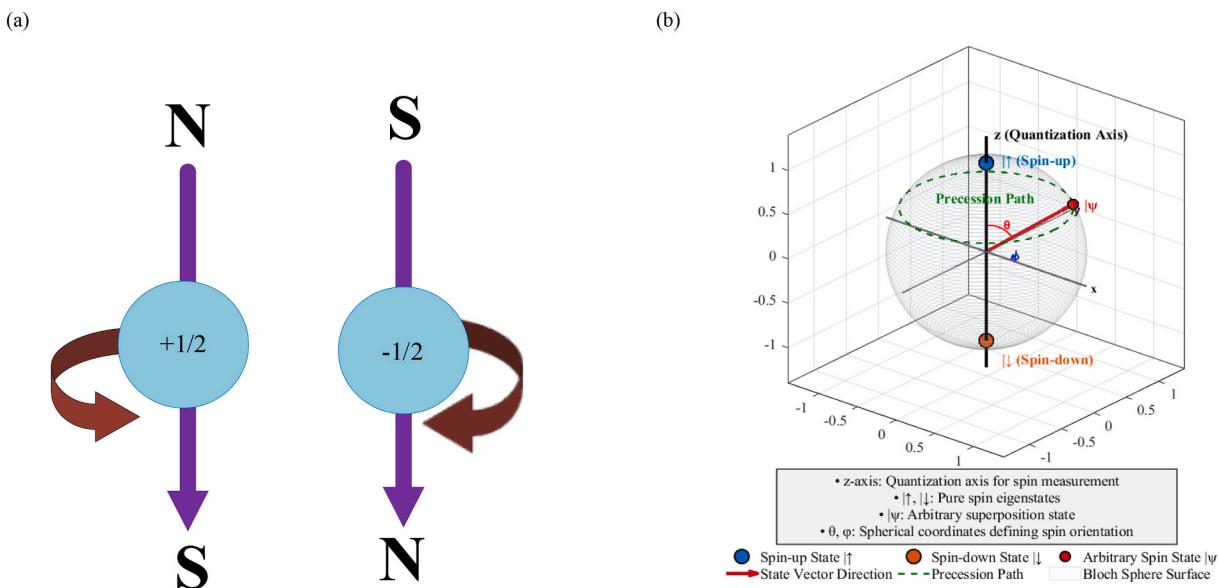
patterning magnetic elements at sub-20 nm [10]. This paper explores the latest advancements in spintronic technology, focusing on three key areas:

- 1) The development of advanced materials such as topological insulators (TIs), two-dimensional (2D) ferromagnets, and heavy metals (HMs).
- 2) The optimization of SOT and STT mechanisms for high-speed, low-power memory.
- 3) Integrating spintronic devices with CMOS technology for neuromorphic computing and quantum information processing.

The review found that room-temperature skyrmion-based memory can achieve storage densities exceeding  $1\text{ Tb/in}^2$ , while SOT-MRAM offers switching speeds of  $<2$  ns with 0.1 pJ/bit energy consumption. In this review, we highlighted a hybrid CMOS-spintronic architecture that reduces power consumption by 30 % in AI workloads, paving the way for energy-efficient, scalable computing systems. The remainder of this paper is organized as follows: Section II discusses the fundamental mechanisms of spintronics, including MTJs, SOT, and STT, while Section III explores the role of advanced materials in enhancing spintronic performance. Section IV highlights the applications of spintronics in quantum computing and AI. Section V addresses the challenges and future directions of spintronic technology, including thermal stability and commercial scalability. Finally, Section VI concludes with a summary of key findings and their implications for the future of electronics.

## 2. Fundamental mechanisms of spintronics

Spintronic devices exploit the quantum mechanical property of electron spin to enable novel functionalities in memory and logic applications. This section examines the fundamental mechanisms that drive spintronics, including MTJs, STT, and SOT, supported by rigorous equations, recent advancements, and comparative analysis. The TMR ratio quantifies the resistance difference between parallel and antiparallel magnetization states in an MTJ [11]. It is derived from the spin-dependent tunneling probability across the insulating barrier, as



**Fig. 1.** Electron spin representation in spintronics. (a) Classical depiction of electron spin states, showing spin-up ( $+1/2$ ) and spin-down ( $-1/2$ ) orientations as magnetic moments (arrows) aligned between magnetic north (N) and south (S) poles. (b) The Bloch sphere representation of electron spin states. The surface of the sphere represents all possible pure quantum states of a spin- $1/2$  particle. The  $+z$  and  $-z$  poles correspond to the classical spin-up ( $|↑\rangle$ ) and spin-down ( $|↓\rangle$ ) eigenstates, respectively. An arbitrary superposition state  $|\psi\rangle$  is represented by a point on the sphere, defined by the polar angle  $\theta$  and the azimuthal angle  $\phi$ . The curved path illustrates the possible precession of the spin vector. This framework is fundamental for describing the quantum mechanical nature of spin in spintronic and quantum information devices.

shown in Eq. (1)

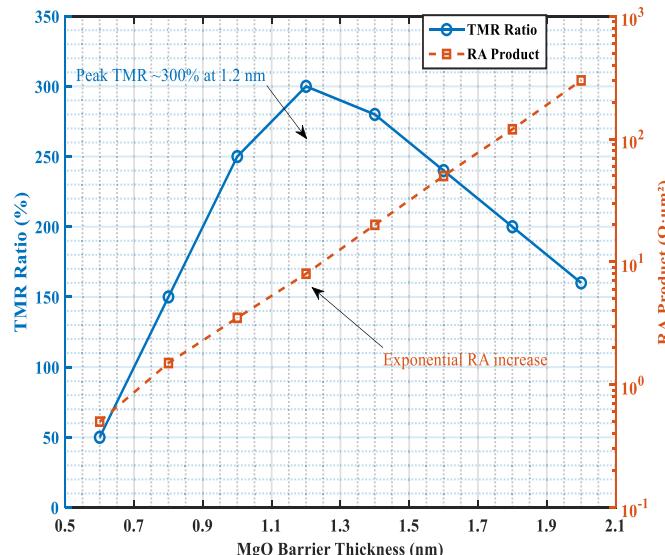
$$K = \frac{\sqrt{2m\phi e}}{\hbar} \quad (1)$$

where  $e$  is the electron's charge,  $\hbar$  is the reduced Planck's constant,  $m$  is the electron mass,  $\phi$  is the barrier height, and  $t$  is the barrier thickness. Here,  $k = \sqrt{2m\phi}/\hbar$  is the decay constant within the barrier, characterizing the tunneling probability. The resistances for the parallel ( $R_p$ ) and antiparallel ( $R_{AP}$ ) magnetization states can be modeled as

$$\begin{aligned} R_p &= e^{2kt} \\ R_{AP} &= e^{2k't} \end{aligned} \quad (2)$$

The exponential dependence of resistance on  $kt$  and  $k't$  highlights the critical trade-off between TMR and device resistance. For instance, modeling the  $R_{AP}$  state with an effective barrier thickness 1.5 times that of the  $R_p$  state would lead to a significantly higher resistance, underscoring the need for precise barrier engineering. The trade-off between TMR and RA product is quantitatively illustrated in Fig. 2, which plots both parameters against MgO barrier thickness using experimental data from CoFeB/MgO systems, as shown in Table 1. Achieving a high TMR (>200 %) requires a sufficiently thick barrier for coherent tunneling, but this exponentially increases the RA product, thereby raising device resistance and impeding high-speed operation. Recent advances in CoFeB/MgO interfaces have enabled TMR ratios exceeding 300 % at room temperature, achieved through the optimization of sub-1 nm barriers. This enhancement is crucial for STT-MRAM, which provides non-volatility, zero standby power, and endurance exceeding  $10^{12}$  cycles [15].

Eq. (1) directly incorporates the tunnel barrier's material properties, where MgO and AlO<sub>x</sub> exhibit fundamentally different behaviors due to their distinct physical characteristics. As shown in Fig. 3(a), MgO's crystalline structure (FCC arrangement of Mg<sup>2+</sup>/O<sup>2-</sup>) enables coherent tunneling with a low effective barrier height ( $\phi \approx 0.4$  eV). In contrast, Fig. 3(b) illustrates how AlO<sub>x</sub>'s amorphous structure leads to incoherent scattering with higher  $\phi$  (~1.5–2.0 eV). These differences manifest in the tunneling probability. Fig. 3(c) demonstrates MgO's slower exponential decay (blue curve) compared to AlO<sub>x</sub>'s rapid drop (red curve),



**Fig. 2.** Trade-off between TMR ratio and resistance-area (RA) product as a function of MgO barrier thickness in CoFeB/MgO/CoFeB magnetic tunnel junctions. The TMR ratio (left axis, blue solid line) peaks at approximately 1.2 nm due to optimal coherent tunneling. In contrast, the RA product (right axis, red dashed line) increases exponentially, defining a critical design constraint for low-power, high-speed STT-MRAM. Data trends are adapted from experimental results in Refs. [8,9].

**Table 1**

MgO barrier thickness dependence of Tmr and Ra product In Cofeb/Mgo/Cofeb Mtjs.

MgO Barrier Thickness (nm)	TMR Ratio (%)	RA Product (Ω·μm²)
0.6	50	0.5
0.8	150	1.5
1.0	250	3.5
1.2	300	8.0
1.4	280	20.0
1.6	240	50.0
1.8	200	120.0
2.0	160	300.0

directly impacting the TMR ratio through the exponential dependence of resistances on  $\kappa$  and  $\kappa'$  as shown in Eqs. (1) and (2), where the difference between parallel ( $e^{2kt}$ ) and antiparallel ( $e^{2k't}$ ) resistances determines the magnitude of TMR. The performance gap is quantified in Fig. 3(d), where MgO achieves 300 % TMR (vs. AlO<sub>x</sub>'s 80 %) due to superior spin polarization preservation. Crucially, Eq. (1)'s thickness dependence  $t$  explains why sub-1 nm MgO barriers (optimized in CoFeB/MgO interfaces) enable >300 % TMR, while AlO<sub>x</sub>'s inherent limitations restrict its applicability in high-performance STT-MRAM applications.

### A. Spin-Transfer Torque

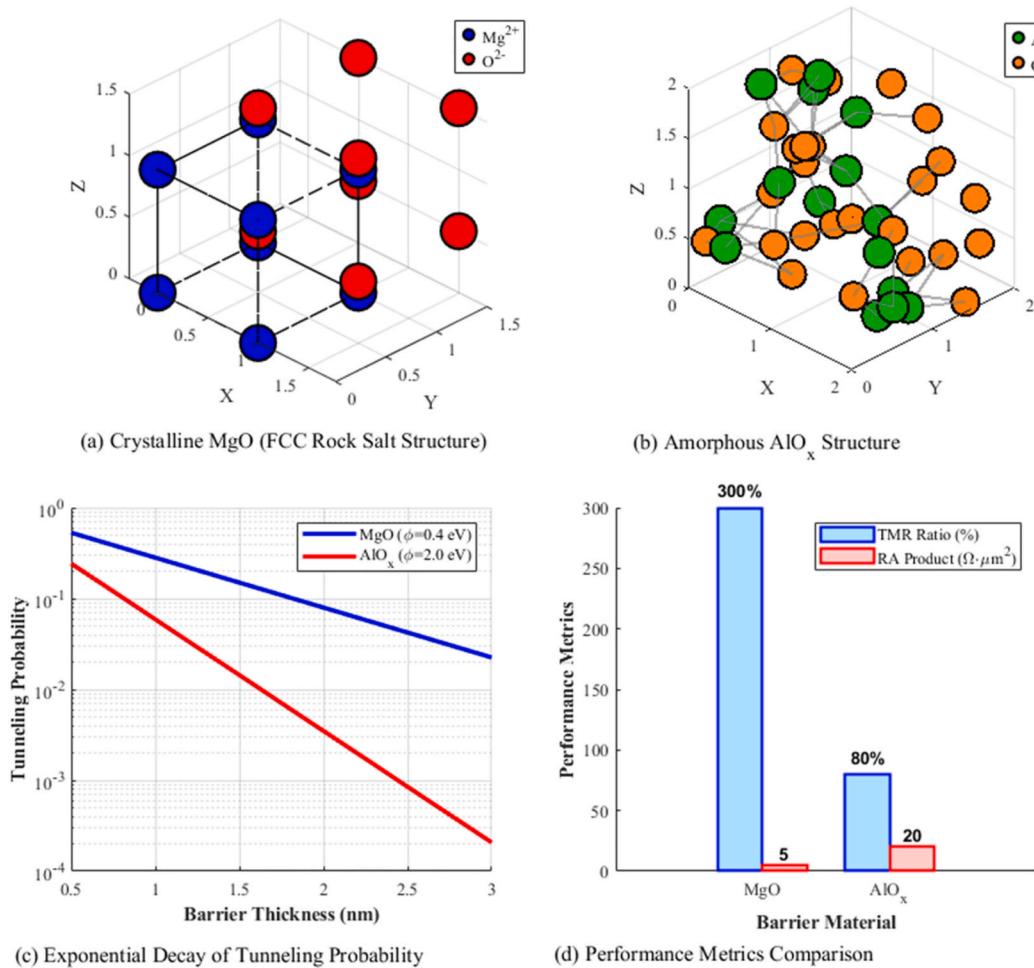
A key mechanism in spintronic devices is STT, particularly for STT-MRAM applications, which offer non-volatility, endurance, and high speed. In STT, a magnetic material's magnetization is torqued by a spin-polarized current, which allows the material's magnetization state to change. STT utilizes the spin of electrons themselves to manipulate memory more quickly and efficiently than traditional memory technologies, which rely on an external magnetic field for magnetization switching. STT is especially beneficial for energy-efficient memory devices because of this feature. By incorporating perpendicular magnetic anisotropy (PMA) into STT-MRAM, the devices' thermal stability has been significantly enhanced, and the switching current requirements have been reduced. The out-of-plane demagnetizing field, which once restricted the switching current, is lessened by this improvement in PMA.

STT-MRAM technology has undergone a critical evolution from in-plane magnetic anisotropy (IMA) to PMA designs to overcome fundamental scaling limits. In IMA designs, the magnetization prefers to lie within the film plane, stabilized primarily by shape anisotropy. The thermal stability factor  $\Delta$ , which determines data retention, is given by (3)

$$\Delta = \frac{K_u V}{k_B T} \quad (3)$$

where  $K_u$  is the magnetic anisotropy energy density,  $V$  is the volume of the free magnetic layer,  $k_B$  is the Boltzmann constant, and  $T$  is the absolute temperature. For IMA,  $K_u$  is dominated by shape anisotropy, which is intrinsically linked to  $V$ . As devices are scaled below ~50 nm, both  $V$  and the effective  $K_u$  decrease sharply, causing  $\Delta$  to plummet and compromise data retention [16]. In PMA designs, the magnetization is oriented out-of-plane, stabilized by strong interfacial anisotropy (e.g., at the CoFeB/MgO interface). Crucially, this interfacial  $K_u$  is mainly independent of the lateral device dimensions. Therefore, PMA-based MTJs can maintain a high  $\Delta$  even when scaled to sub-20 nm nodes, directly solving the thermal stability challenge faced by IMA designs [17]. The transition to PMA also fundamentally enables a more energy-efficient switching procedure. The critical switching current density  $J_c$  required to reverse the magnetization is governed by the effective anisotropy field  $H_{k,eff}$ , as shown in (4) [18]

$$J_c \propto H_{k,eff} \quad (4)$$



Data sources: TMR and RA values based on characteristic experimental data from S. Ikeda et al., Nat. Mater. (2010) and S. S. P. Parkin et al., Nat. Mater. (2004)

**Fig. 3.** Comparative analysis of MgO and aluminium oxide ( $\text{AlO}_x$ ) tunnel barriers for MTJs. (a) Three-dimensional (3D) atomic model of crystalline MgO in the rock-salt ( $\text{NaCl}$ ) structure, showing the face-centred cubic arrangement of  $\text{Mg}^{2+}$  (blue) and  $\text{O}^{2-}$  (red) ions. The dashed lines indicate the unit cell boundaries. This periodic structure enables coherent tunneling. (b) 3D model of amorphous  $\text{AlO}_x$ , illustrating the random network of  $\text{Al}^{3+}$  (green) and  $\text{O}^{2-}$  (orange) ions with variable coordination and bond angles, characteristic of the amorphous phase, which leads to incoherent tunneling and defect scattering. (c) Calculated exponential decay of tunneling probability as a function of barrier thickness, derived from Eq. (1) using effective barrier heights of  $\phi_{\text{MgO}} \approx 0.4$  eV and  $\phi_{\text{AlO}_x} \approx 2.0$  eV. The slower decay for MgO demonstrates its superior tunneling properties. (d) Quantitative comparison of key performance metrics at optimal thickness (MgO: 1.2 nm,  $\text{AlO}_x$ : 1.5 nm), showing MgO's significantly higher TMR ratio (300 % vs. 80 %) and lower resistance-area (RA) product (5  $\Omega \cdot \mu\text{m}^2$  vs. 20  $\Omega \cdot \mu\text{m}^2$ ), based on characteristic experimental values from Refs. [12–14].

For PMA structures, the inherent out-of-plane demagnetizing field  $H_d$  opposes the anisotropy field  $H_k$ , resulting in a lower net field required for switching, as shown in (5)

$$H_{k,\text{eff}}^{\text{PMA}} = H_k - H_d \quad (5)$$

This reduction in  $H_{k,\text{eff}}$  is the direct physical reason why PMA-MTJs require a lower  $J_c$ . Experimental  $J_c$  values as low as 2.1 MA/cm<sup>2</sup> have been achieved in optimized PMA devices [19].

CoFeB-MgO MTJs and other devices with PMA-based free layers exhibit a notable decrease in switching current densities, reaching as low as 2.1 MA/cm<sup>2</sup> at room temperature, thereby enhancing performance and energy efficiency [20]. PMA plays a crucial role in enhancing STT-MRAM's thermal stability, particularly at smaller process nodes (less than 20 nm), where conventional in-plane magnetization designs struggle to maintain thermal stability due to the higher thermal energy associated with smaller sizes. High-performance STT-MRAM devices with <1 pJ/bit write energy and <5 ns switching rates are developed as a result of PMA improvement [21]. STT enables the magnetization switching process governed by (6)

$$j_c = \frac{2e \cdot M_s \cdot t}{h \cdot (H_k + H_d)} \quad (6)$$

where  $J_c$  represents the critical current density,  $M_s$  is the saturation magnetization,  $t$  is the free layer thickness,  $H_k$  is the anisotropy field, and  $H_d$  is the demagnetizing field. By optimizing material properties, such as CoFeB thickness and the MgO barrier, the STT-MRAM switching performance can be significantly enhanced, resulting in reduced power consumption and faster switching times [22,23]. Although STT-MRAM technology has advanced, issues persist in maintaining thermal stability at progressively smaller nodes (less than 20 nm). To solve this problem, new materials with higher  $H_k$  must be developed to ensure reliable switching performance and long-term reliability in harsh environments [24].

## B. Spin-Orbit Torque

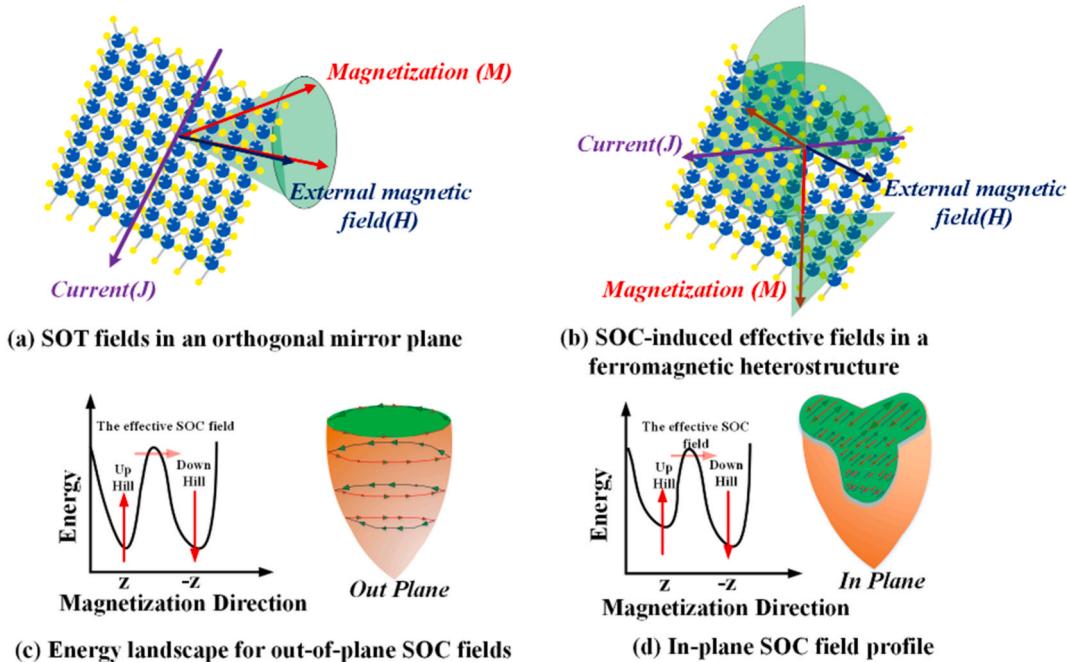
Early groundbreaking studies demonstrated the potential of SOT for perpendicular magnetization switching in single ferromagnetic (FM)

layers via in-plane current injection, establishing the fundamental ideas of SOT-driven events. With current densities as low as  $1.1 \times 10^7 \text{ A/cm}^2$ , recent work has achieved the first experimental demonstration of current-induced magnetization switching in perpendicularly magnetized Pt/Co/AlO<sub>x</sub> systems [25]. Ta exhibits the giant spin Hall effect, facilitating effective spin-torque switching through enhanced spin-orbit coupling (SOC), as revealed by a systematic investigation of the role of HMs in SOT generation [26]. The connection between material characteristics and SOT efficiency offered crucial insights into the symmetry and magnitude of SOC in FM heterostructures [27]. The rapid advancement of SOT research, which has since expanded to encompass a range of materials and device topologies, was made possible by these pioneering studies.

SOT has gained traction, particularly in SOT-MRAM, where fast switching speeds, stability, and reduced power consumption are required [28]. This paper found that TIs exhibit high SOT efficiency, producing robust spin currents with minimal energy input. Integrating PMA has further enhanced SOT-based device efficiency, as PMA provides more stable magnetization states with lower switching currents. By investigating novel material systems, especially anti-FMs (AFMs) and TIs, recent research has greatly advanced the creation of SOT beyond typical HMs. Noncollinear AFMs, such as Mn<sub>3</sub>Sn, have shown great promise for AFM spintronics. The demonstration of mutual SOT switching in Mn<sub>3</sub>Sn-based heterostructures, in which the SOT polarity can be electrically programmed, is a significant advancement. This capacity enables new features for neuromorphic computer architectures and reconfigurable logic [29]. Effective field-free switching has been enabled by integrating chiral AFMs with two-dimensional van der Waals materials. For example, deterministic switching of the chiral AFM order in Mn<sub>3</sub>Sn has been achieved with a high switching ratio and a critically low current density, utilizing the out-of-plane spin polarization produced by WTe<sub>2</sub>, opening the door to low-power SOT devices [30]. At the same time, advances in TIs have focused on harnessing and controlling their distinct spin-momentum-locked surface states. Recent research has shown that anomalous out-of-plane spin polarization can be produced by controlling the Fermi-surface symmetry in TIs/FMs heterostructures,

such as Bi<sub>2</sub>Te<sub>3</sub>/CoFeB. The long-standing problem of attaining deterministic switching of perpendicular magnets without an external bias field is crucially resolved by Ref. [31]. Further studies have demonstrated that ultra-thin metallic insertion layers at the TIs/FMs interface can significantly increase the effective spin-charge conversion efficiency, providing a potent technique for optimizing SOT-MRAM performance [32], further illuminating the crucial importance of interface quality. SOT-MRAM is a potential but not yet mass-produced memory technology, currently in the advanced development and prototyping stage. Unique material constraints considerably restrict its approach to high-volume manufacture and scalability. The method relies on materials with strong spin-orbit coupling—primarily HMs (e.g., Pt, Ta, W) and TIs generate the requisite spin currents. These materials present a number of integration challenges, including the need for precise atomic-level interface engineering to preserve spin transparency, their sensitivity to defects that impair performance at scaled nodes, and the frequent need for specialized deposition and patterning techniques that make integration with conventional CMOS fabrication flows more difficult. The main barrier to the technology's commercial scaling is the combination of these material-driven variables that impede wafer-level yield and consistent device performance [33]. The diagrams in Fig. 4(b)–(d) are grounded in recent theoretical and experimental studies on SOC and SOT [34–36], which elucidate the relationship between material structure, SOC strength, and resulting torque efficiencies. The SOT operations aimed at diverse spin topologies and their properties on the magnetic energy distribution are illustrated in Fig. 4(a). The Figure illustrates magnetic movement induced by an effective SOT field in techniques featuring multiple orthogonal mirror planes.

Fig. 4(b) [37] illustrates the changing aspects of magnetic induction for realistic spin-orbit joint fields with an area corresponding to the anisotropic axis. Fig. 4(c) shows the magnetic potential abundance in architecture with homogeneous orthogonal magnetization and an exterior-plane efficient SOC field created by external plane texturing. Furthermore, Fig. 4(d) shows the magnetic flux density that characterizes a system with orthogonal magnetic entropy, and an ineffective within-the-plane SOC field produces an in-plane spin texture. It also



**Fig. 4.** Schematic representations of SOT mechanisms and SOC fields in FM heterostructures. (a) Orthogonal mirror plane configuration showing SOT fields, with labeled vectors for current density ( $J$ ), magnetization ( $M$ ) and external field ( $H$ ). (b) Visualization of SOC-induced effective fields in a multilayer stack, arrows indicate field direction and local magnetization orientation. (c) Energy landscape depicting out-of-plane SOC fields influencing magnetization switching between  $+Z$  and  $-Z$  states. (d) In-plane SOC field profile illustrating control over magnetization dynamics within the plane.

shows a magnetic power rate in a structure with nearby magnetic anisotropy, a feasible arena with a segment transverse to the entropy direction [39].

The spin patterns enable these fields, where  $J$  represents current,  $M$  represents magnetization, and  $H$  represents magnetic field intensity. SOT leverages SOC to generate spin currents from charge currents. Furthermore, the spin hall angle quantifies the efficiency  $\theta_{SH}$ , as shown in (7)

$$\theta_{SH} = \frac{2e}{\hbar} \times \frac{L_c}{L_s} \quad (7)$$

where  $L_c$  is the coherence length, and  $L_s$  is the spin diffusion length. The review found that HM like  $\beta$ -phase -Ta ( $\beta$ -Ta) with  $\theta_{SH}$  of 0.3 can enable <2 ns switching and <0.1 pJ/bit energy. Moreover, SOT-MRAM outperforms STT-MRAM in terms of speed. Additionally, cost-effective materials such as Ta and W, in combination with Pt, can be utilized for spintronic applications.

### C. Comparative Analysis

STT and SOT, which have distinct physical origins and operating properties, are essential mechanisms for controlling magnetization in spintronic devices. Without an external magnetic field, magnetization switching is made possible by both STT and SOT. However, the methods by which the spin torque is produced and delivered vary. When a spin-polarized current is introduced straight into an FM layer, spin angular momentum is transferred from the conduction electrons to the local magnetization, resulting in STT. This mechanism serves as the foundation for standard spintronic devices, such as STT-MRAM, and can cause domain wall motion or magnetization reversal. The performance metrics in Table II demonstrate that SOT-MRAM holds significant advantages over STT-MRAM. This is corroborated by quantitative research, including a simulation study that found SOT-MRAM to be  $4 \times$  faster than STT-MRAM at the cell level [40], and a recent review confirming its superior switching speed and energy efficiency [41]. The comparative data of the performance metrics are shown in Table II.

The current density flowing through the magnetic tunnel junction and the degree of spin polarization determine the effectiveness of STT switching [42]. On the other hand, SOT is generated when a charge current passes through a material adjacent to an FM layer that exhibits strong SOC, such as a HM or a TI. In these materials, the transverse spin current generated by the spin Hall effect or Rashba-Edelstein effect applies a torque on the magnetization of the nearby ferromagnet. Because the charge and spin current channels may be separated, SOT-based devices can achieve faster switching, better endurance, and more flexible device topologies. In addition, SOT usually necessitates more intricate multilayer structures and meticulous interface engineering to optimize efficiency, even though both techniques eliminate the requirement for an external magnetic field for switching. The choice between STT and SOT depends on the specific application requirements, such as switching speed, energy efficiency, and device scalability [43]. However, the simulation results comparing SOT and STT switching dynamics were obtained using a macro-spin model based on the Landau-Lifshitz-Gilbert (LLG) equation, which incorporates both STT

**Table 2**  
SOT Vs STT performance metrics [38].

Aspect	SOT	STT
Switching energy (pJ/bit)	0.1	0.5
Speed (write)	<2 ns	<5 ns
Endurance (cycles)	$> 10^{15}$	$> 10^{12}$
CMOS compatibility	Moderate (requires HM)	High
Thermal stability	400 K	350 K
Switching time at 2 MA/cm <sup>2</sup>	~2.5 ns	~7 ns
Switching time at 10 MA/cm <sup>2</sup>	~1.3 ns	~3 ns

and SOT terms. The LLG equation is given by,

$$\frac{dm}{dt} = -\gamma m \times H_{eff} + \alpha m \times \frac{dm}{dt} + T_{STT} + T_{SOT} \quad (8)$$

where  $m$  is the unit vector of magnetization,  $\gamma$  is the gyromagnetic ratio,  $\alpha$  is the Gilbert damping constant,  $H_{eff}$  is the effective magnetic field,  $T_{STT}$  and  $T_{SOT}$  are the STT and SOT terms, respectively. The model's parameters, comprising current density, magnetic anisotropy, and damping constant, were chosen to align with typical experimental values reported in recent literature, as shown in Table III. With this approach, it is possible to make a direct and fair comparison of SOT and STT switching under the same conditions. The simulation shows that, under identical current density and device geometry conditions, SOT achieves switching speeds up to three times faster than STT, which is shown in Fig. 5, in line with recent experimental and theoretical studies [44,45]. Additionally, this performance advantage positions SOT-MRAM as a candidate for ultrafast cache memory [46].

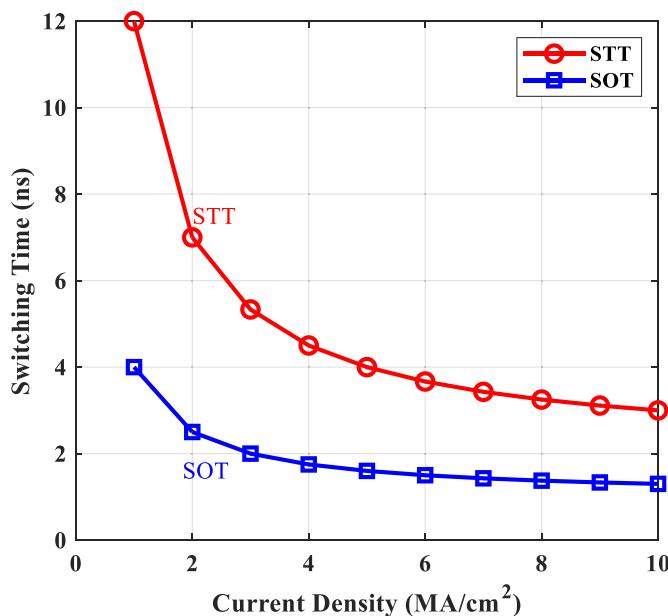
### D. Spin-Orbit Coupling Mechanisms

The conversion of charge currents into spin currents, necessary for effective magnetization control in the absence of magnetic fields, is accomplished by SOC, a fundamental interaction in spintronics that enables efficient spin-to-charge conversion by linking an electron's spin to its momentum. SOC is particularly noticeable in materials such as TIs and HM like tungsten (W), Ta, and Pt. The TIs are unique because they possess magnetic-momentum restricting properties, which enable low-dissipation spin currents ideal for low-power applications. After all, the electron's spin rotation is inherently linked to its speed. Moreover, 2D substances such as graphite and transition-metal dichalcogenides (TMDs) provide interesting SOC features because of their structural flexibility and the potential for integrating them into existing semiconductor architectures [47].

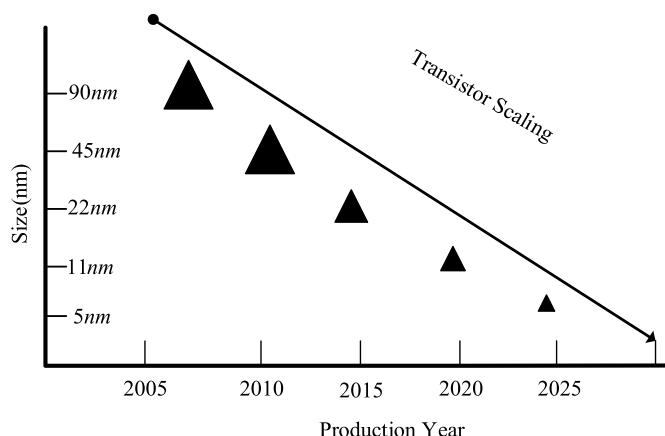
Interface engineering has advanced significantly, enhancing SOC efficiency by tailoring the interactions at material interfaces. As traditional silicon-based transistors approach physical and quantum limits due to miniaturization, shown in Fig. 6, spin-orbitronics offers a promising alternative to overcome these challenges. Furthermore, by utilizing electrons' spin degrees of freedom, spin-orbitronic devices aim to enhance the functionality, scalability, and energy efficiency of nanoscale electronics. Researchers can amplify SOC effects by adjusting the interface quality and stacking order, thereby optimizing the spin-to-charge conversion that is crucial for device performance [48]. However, the scalability of SOC-based devices remains a primary challenge. High-quality SOC materials, such as HM and TI, exhibit complex interfacial properties that require careful optimization for reliable device performance in large-scale applications. Additionally, interface imperfections can reduce SOC efficiency, impacting overall device reliability [49].

**Table 3**  
Macro-spin simulation parameters for Sot Vs. Stt switching.

Parameters	Symbol	Typical Value
<b>General Magnetic Parameters</b>		
Gyromagnetic ratio	$\gamma$	$2.21 \times 10^5$ m/(A·s)
Gilbert damping constant	$\alpha$	0.01–0.05
Saturation magnetization	$M_s$	1.0–1.2 MA/m
PMA constant	$K_u$	0.8–1.0 MJ/m <sup>3</sup>
<b>Spin-Transfer Torque (STT)</b>		
Current density	$J$	1–10 MA/cm <sup>2</sup>
Spin polarization ratio	$\eta$	0.4–0.6
Spin polarization direction	$p$	$\pm z$
<b>Spin-Orbit Torque (SOT)</b>		
Current density	$J$	1–10 MA/cm <sup>2</sup>
Spin Hall angle	$\theta_{SH}$	0.1–0.3
Spin polarization direction	$\sigma$	$\pm y$



**Fig. 5.** Comparison of SOT and STT switching times as a function of current density. The plot demonstrates that SOT enables faster magnetization switching at lower current densities compared to STT, emphasizing the efficiency and potential of SOT-based devices for high-speed spintronic applications.



**Fig. 6.** Trends in transistor miniaturization over the years, illustrating the reduction in device size from 90 nm to 5 nm as production technology advances. The Figure highlights the scaling, and the triangle here is the conceptual size, with projections toward CMOS technologies enabling further miniaturization and enhanced device performance.

#### E. Challenges and Future Directions

SOT and STT mechanisms hold promise, but they encounter various challenges. The scalability of SOC materials limits SOT devices, as they often necessitate HMs and precise interface engineering, which complicates large-scale integration and uniform device performance. Interface defects can reduce efficiency and reliability [55]. In this paper, the future processing in-memory applications roadmap is described in Fig. 7, which illustrates the conceptual development of spintronic memory devices, showing a clear progression from basic storage components to facilitators of sophisticated PIM architectures. Furthermore, innovations in the magnetization switching mechanism are at the heart of this development, with each step resolving the significant bottlenecks of the previous one. The first step on the path was field-driven Toggle-MRAM, which demonstrated the concept of nonvolatile magnetic storage but had poor scalability and high energy consumption. These

problems were mitigated by the use of spin-polarized current in STT switching, which enabled denser integration and paved the way for embedded memory applications. Moreover, a significant advancement for PIM was the later conversion to SOT switching.

SOT-MRAM achieves breakneck write speeds and remarkable performance by decoupling the read and write channels. The frequent and quick compute-in-place operations needed in PIM depend on SOT-MRAM's rapid write speeds and noteworthy endurance, which are achieved by decoupling the read and write channels. Future hybrid spintronic technologies aim to fully utilize spin as a native information carrier, while voltage-controlled magnetoelectric switching (MESO) promises to reduce energy consumption by several orders of magnitude. The von Neumann bottleneck is immediately addressed by this unrelenting advancement in speed, energy efficiency, and functional integration, establishing spintronic devices as a key technology for future non-von Neumann computing.

Oxidation-prone 2D materials, such as chromium triiodide ( $CrI_3$ ), require encapsulation for stability [56].  $CrI_3$  is highly reactive to oxygen and moisture, which can compromise its integrity. Consequently, encapsulation techniques, such as hexagonal boron nitride ( $hBN$ ), graphene, aluminum oxide ( $Al_2O_3$ ), and silicon dioxide ( $SiO_2$ ), are used to improve stability and preserve electronic and magnetic properties. Furthermore, polymer encapsulation (e.g., Polymethyl methacrylate) provides temporary protection, while environments sealed with inert gases (like nitrogen or argon) or under vacuum conditions can help prevent oxidation.

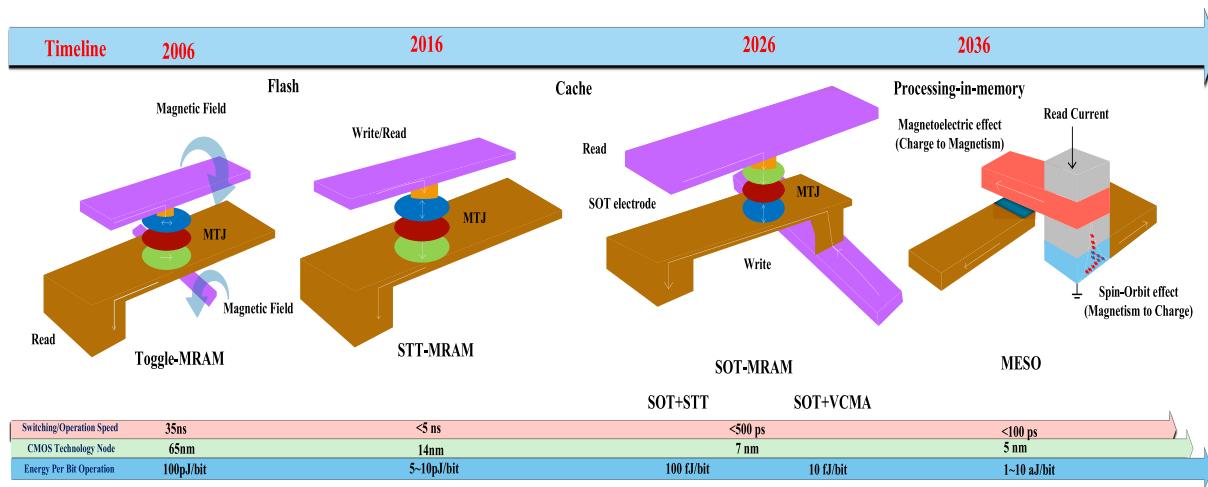
Materials like  $L_{10}$ -iron-Pt ( $L_{10}FePt$ ) ( $H_k \approx 10T$ ) offer enhanced stability at scaled nodes [57]. Their high anisotropy constant makes them ideal for high-density storage and spintronic applications, providing improved thermal stability and resistance to demagnetization, ensuring that  $L_{10}FePt$  maintains its magnetic properties even at the nanometer scale, positioning it as a promising option for future memory technologies such as heat-assisted magnetic recording and MRAM, where stable magnetization is crucial for performance. Atomic layer deposition (ALD) enables the achievement of sub-1 nm barrier uniformity, ensuring uniform thickness across surfaces. This capability is essential for advanced semiconductor technologies and next-generation electronic devices [58]. For example, the recent storage device adaptation data is shown in Table IV. Future research will focus on voltage-controlled SOT for sub-0.1 pJ/bit operation and 3D MTJ stacking for >1Tb/in<sup>2</sup> density [59]. New materials, including anti-FM insulators and complex oxides, are being tested to enhance the efficiencies of SOC and SOT further. As these challenges are addressed, spin-orbitronics will likely play a central role in high-speed, energy-efficient computing [60].

### 3. Advanced materials for spintronics

The performance of spintronic devices is heavily dependent on the materials used. Therefore, this section explores TIs, 2D materials, and HMs, highlighting their unique properties and challenges, as well as a recent overview of materials and spintronics application integration, as shown in Table V.

#### A. Topological Insulators

TIs are a novel category of substances that cover the majority of properties and sensitive edge states. They are controlled by spin-momentum locking and shielded by time-reversal order, which guarantees spin-polarized current transport even when non-magnetic impurities are present. Recent research has advanced the development of ternary alloys, such as bismuth telluride ( $Bi_2Te_2Se$ ), which exhibit enhanced thermal and environmental stability, making them suitable for practical spintronic applications. Magnetic TIs, such as chromium ( $Cr$ )-doped bismuth telluride ( $Bi_2Te_3$ ), have shown promise in quantum anomalous Hall effect-based devices, where dissipationless



**Fig. 7.** Timeline and conceptual evolution of spintronic devices for processing-in-memory (PIM) applications. The diagram illustrates the progression from early Toggle-MRAM and STT-MRAM to advanced SOT-MRAM and emerging magnetoelectric and hybrid spintronic devices. The Figure emphasizes how innovations in spintronic device architecture and materials have enabled the development of faster, more energy-efficient, and highly scalable memory solutions for next-generation computing systems.

**Table 4**  
Evolution of spintronic memory adaptation.

Technology	Key Metric/Spec	Cost vs. Incumbents	Market Status & Application	Source
TMR Sensor (2019)	N/A (Superior Sensing Performance)	~30 % higher	Standard in automotive/industrial sensing (e.g., wheel speed)	[50]
MRAM (2021)	High Endurance, Instant-On	Higher	Adopting IoT/Edge MCUs for non-volatility	[51]
STT-MRAM (2022)	>10 <sup>12</sup> cycles, >10-yr @ 150 °C	Higher than SRAM	Embedded in auto/industrial MCUs; justified by endurance & retention	[52]
Auto MRAM (2023)	High Reliability, Instant-On	Higher than Flash	Adopted in safety-critical automotive systems for reliability	[53]
Advanced MRAM (2024)	Up to 10 <sup>16</sup> cycles, MB capacity	Higher	Widening Use in FPGAs, Edge AI, justified by endurance, density, and non-volatility	[54]

edge states are critical for quantum computing [61]. Furthermore, TIs are pivotal for spin filters, spin valves, and spin-current injectors. Their unique properties make them indispensable for spintronic logic devices and quantum systems. However, synthesizing defect-free TIs and maintaining stability at room temperature are significant challenges. TIs exhibit spin-momentum locking, enabling the dissipation of fewer spin currents at their surfaces. The following Equation defines the spin Hall conductivity ( $\sigma_{SH}$ ):

$$\sigma_{SH} = \frac{e^2}{\hbar} \times \frac{1}{2\pi} \quad (9)$$

Recent studies on Bi<sub>2</sub>Te<sub>3</sub> and antimony telluride (Sb<sub>2</sub>Te<sub>3</sub>) achieve a  $\sigma_{SH} \approx 10^3 \Omega^{-1} cm^{-1} \approx 10^3$  at room temperature [62]. However, surface oxidation and defect formation during fabrication remain critical challenges [63].

## B. Two-Dimensional Materials

2D materials, particularly graphene and TMDs, have emerged as transformative elements in spintronics. Furthermore, graphene, renowned for its exceptional carrier mobility and long spin diffusion length, facilitates efficient spin transport over micrometer scales. However, its weak intrinsic SOC limits spin manipulation capabilities, leading researchers to enhance its properties by functionalizing with heavy atoms or integrating with other 2D materials. Moreover, because of their valley-dependent spin polarization and significant SOC, TMDs like molybdenum disulfide (Mo<sub>2</sub>S) and W-diselenide (WSe<sub>2</sub>) are especially promising.

These properties have enabled the development of spintronic devices based on valleytronics, a subfield that utilizes electron valley degrees of freedom for information processing [73]. Magnetic 2D materials, such as chromium germanium telluride (Cr<sub>2</sub>Ge<sub>2</sub>Te<sub>6</sub>) and CrI<sub>3</sub>, add further dimensions to spintronic research by enabling spin filtering and tunneling in bilayer systems [74].

2D materials are integral to spin transistors, spin filters, and heterostructures for spin-wave devices. Despite their potential, environmental sensitivity and scalability issues remain significant hurdles. Furthermore, 2D materials like graphene and TMDs offer exceptional spin transport properties. The spin diffusion length ( $L_s$ ) in graphene exceeds 10 μm at room temperature, making it ideal for spin valves [75]. For TMDs like Mo<sub>2</sub>S, the valley-dependent spin polarization enables valleytronics, with spin lifetimes exceeding 1 ns.

TMR cutting-edge MTJs emphasize the function of 2D magnetic materials in spintronic devices. The MTJ involves two FM sheets disconnected through a tunnel barricade [76], when the magnetizations of FM<sub>1</sub> and FM<sub>2</sub> remain corresponding, spin-polarized channeling is efficient for both spin-up and down channels, resulting in low resistance, as shown in Fig. 8. In contrast, an antiparallel configuration causes spin mismatch, leading to high resistance.

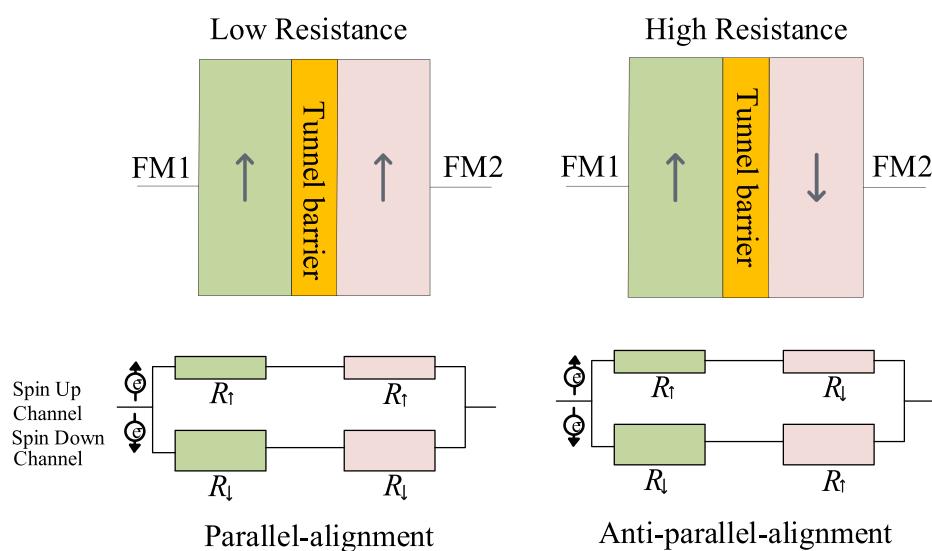
## C. Heavy Metals

HMs such as Pt, Ta, and W are essential for spin-charge conversion in SOT devices. They enable an effective spin current to flow between peers due to the Rashba-Edelstein or spin space effects. Unlike traditional conductive metals like copper, HMs exhibit high spin Hall angles, which are crucial for spin-charge interconversion in SOT devices [77]. Because of their low resistivity and strong spin Hall conductivity, which improves device performance, β-Ta and W have become top contenders.

**Table 5**

Recent advanced spintronics technology and materials integration.

Technology/ Materials	Institution/ Developer	Year	Key Features	Applications	Spintronics integration	Advantages	Disadvantages	Ref.
MTJ	IBM	2023	Optimal spin detection through high TMR	MRAM, Reading heads, Spin Restrictions	A vital part of MRAM is providing higher read/write persistence and nonvolatile memory. SOT technologies are essential for effective spin-to-charge transformation.	o Rapid changeover as well as excellent flexibility o Exceptionally minimal electrical usage and fault resistance	o The constancy of heat at fewer circuits o Disruption by freight transporters	[64]
ITs	Stanford University	2022	Spin controlling at minimal energy is made feasible through spin-momentum securing.	Semiconductors with spin & quantum data processing				[65]
Heusler Alloys	Max Planck Institute	2020	Properties of semi-metals with adjustable Curie heats	The magnetic sensors and spin valve	As part of the STT MRAM	o Enhanced spin orientation and affordable data transmission o High spin compatibility periods with reduced resistivity	o Nuclear imbalance sensitivity in manufacturing o Strengthening the limited spin-orbit interaction is essential.	[66]
2D Materials (Graphene)	University of Manchester	2023	Ultra-high ability and extensive spin tranquility durations	Spin logic structures and spin adjustments.	Facilitates the transmission of spin energy in spintronic devices	o Outstanding scalability and insensitivity to electromagnetic disruption	o Intricate monitoring systems that can be affected by heat	[67]
Anti-FM Materials	CEA Grenoble	2022	Nonvolatile spin modes are utilized at extremely high speeds	Fast spintronic devices and storage	Permits swift spin functions			[68]
Skyrmions	CEA Grenoble	2023	Topologically stable magnetic materials at the tiny level	Advanced spintronic data storage and circuit storage	The core of an incredibly dense, cost-effective track storage	o A system with high-performance traction. Modern technology for noise reduction.	o Stabilization at ambient temperature and intricate management are necessary.	[69]
SOC Materials	Harvard University	2024	The strong connection between spin and orbit for the transition from spin to charge	Spin semiconductors and spin logic devices.	The secret to torque-based spin-orbital mechanisms	o Low-energy consumption and outstanding conversion speed	o Only a small number of materials.	[70]
Spin Qubits in Quantum Dots	Delft University of Technology	2023	Periods and regulated spin states	Spintronic technology and quantum computation	Underlying technology for spin-based quantum computers	o Low-temperature alignment durations and flexible logic devices	o Temperatures at freezing points are necessary for durability.	[71]
Multiferroic Materials	Tokyo Institute of Technology	2024	Parallel management is made possible by combined magnetism and ferroelectric characteristics.	Logic structures and storage	Permits spin states to be controlled by a power field.	o Multipurpose, low-energy components ideal for tiny electronics	o Issues with substance fabrication	[72]



**Fig. 8.** Illustration of electron transport behavior in MTJs for parallel and antiparallel alignments of FM layers (FM1 and FM2). The Figure illustrates how spin-up and spin-down electrons traverse the tunnel barrier, resulting in distinct resistance states that form the basis for data storage in spintronic memory devices.

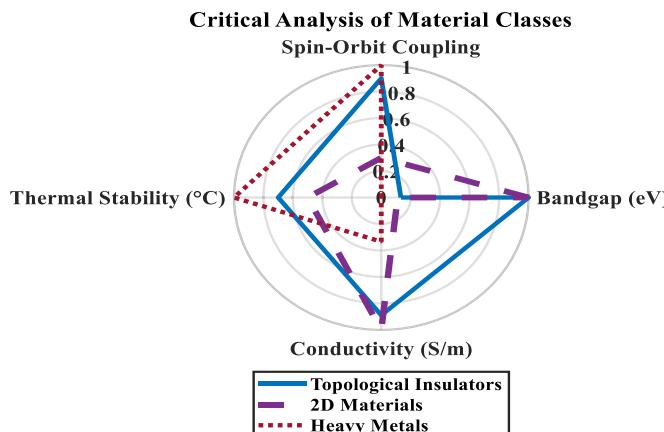
Additionally, alloying Pt with rare-earth elements has enhanced thermal stability and spin transparency.

HMs are foundational in MRAM and STT devices. While they offer high efficiency, challenges include interfacial spin scattering and high-power consumption during spin current generation. This review discovered that the  $\theta_{\text{SH}}$  for  $\beta\text{-Ta}$  is approximately 0.3. This high  $\theta_{\text{SH}}$  enables efficient magnetization switching with  $<0.1 \text{ pJ/bit}$  energy [78]. However, interfacial scattering and manufacturing constraints limit scalability.

#### D. Material Challenges

While spintronic materials offer transformative potential, they face several challenges. These include TIs and 2D materials, which are susceptible to oxidation and environmental factors, leading to performance degradation. Spin scattering and interfacial imperfections reduce spin transport efficiency in HMs and hybrid systems. Fabricating large-scale, defect-free materials and integrating them with existing CMOS technology is a complex and expensive process. Current spintronic devices often require high current densities, which limit their power-saving benefits [83].

Emerging solutions include advanced synthesis methods, such as molecular beam epitaxy (MBE) for TIs, encapsulation techniques for 2D materials, and interfacial engineering strategies for HMs. Novel substances, including spin-gapless semiconductors and Heusler metals, are also being investigated for improved spintronic performance and comparative analysis between HMs, TIs, and 2D materials displayed in Fig. 9. The performance of hybrid spintronic devices employing cutting-edge material combinations, such as TIs with HMs and 2D materials with ferromagnets, is compared in Fig. 10. The spin current density (bottom, red) and the time-dependent spin voltage (top, blue) in Fig. 10 display sinusoidal oscillations. A primary materials challenge in spintronics is the inability to sustain stable, non-oscillatory spin accumulation, which is crucial for reliable memory and logic applications. Such dynamic spin reactions bring this obstacle to light. While oscillatory spin voltages and currents can be utilized in high-frequency devices, such as spin-torque oscillators, they are not suitable for memory technologies that require low noise and stable spin polarization. The susceptibility of spin transport to interfacial scattering, damping, and material anisotropy is reflected in the observed sinusoidal behavior, underscoring the need for optimal material design and interface engineering to overcome this challenge. With the advancement of quantum computing and AI applications, spintronics is revolutionizing these fields through spin qubits and neuromorphic computing.



**Fig. 9.** Radar chart presenting a critical analysis of material classes used in spintronics, including TIs, 2D materials, and HMs. The chart compares key properties such as SOC, bandgap, conductivity, and thermal stability, providing insights into the suitability of each material class for spintronic applications.

#### E. Spin Qubits

Depending on the spin of electrons or the nucleus, spin qubits demonstrate the ability to serve as a basis for quantum computation due to their coherence characteristics, scalability, and compatibility with current semiconductor technology. The spin orientations of particles in these systems include quantum information that can be changed by applying electric or magnetic forces. Advances in quantum control methods, materials science, and nanofabrication have propelled the creation of spin qubits [84]. The critical advantage of spin qubits lies in their compatibility with silicon-based technologies. Furthermore, silicon quantum dots are attractive due to their low spin-revolution connection and the availability of isotopically pure materials, which reduces decoherence [85]. Spin qubits leverage the spin states of electrons for quantum information processing.

The coherence time ( $T$ ) is given by (10)

$$T = \frac{2\hbar}{Y} \quad (10)$$

where  $Y$  is the decoherence rate, this paper found that silicon-based spin qubits can achieve  $T > 0.2$  at  $1.5 \text{ K}$ , with 99.9 % gate fidelity [86]. Recent advancements in isotopically purified silicon have further reduced decoherence [87].

#### F. Neuromorphic Computing

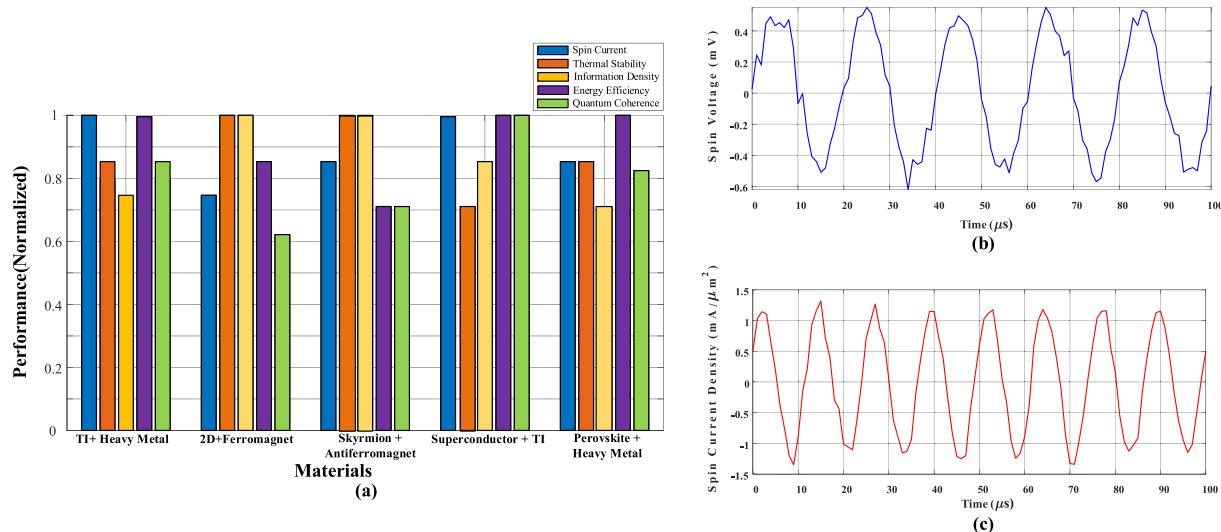
The goal of neuromorphic computing is to replicate the composition and operations of the human brain, offering a paradigm shift in AI systems, as shown in Fig. 11. By mimicking neural processes through hardware architectures, neuromorphic systems achieve energy efficiency, fault tolerance, and high adaptability, which is critical for next-generation AI applications [88]. Neuromorphic devices leverage memristors, spintronic devices, and photonic circuits to implement artificial neurons and synapses.

Spintronics is pivotal due to its energy-efficient magnetization dynamics and inherent non-volatility. Spintronic neurons use STT to emulate neuronal spiking behaviors, demonstrating their suitability for neuromorphic hardware. Recent advancements have integrated neuromorphic principles into AI applications.

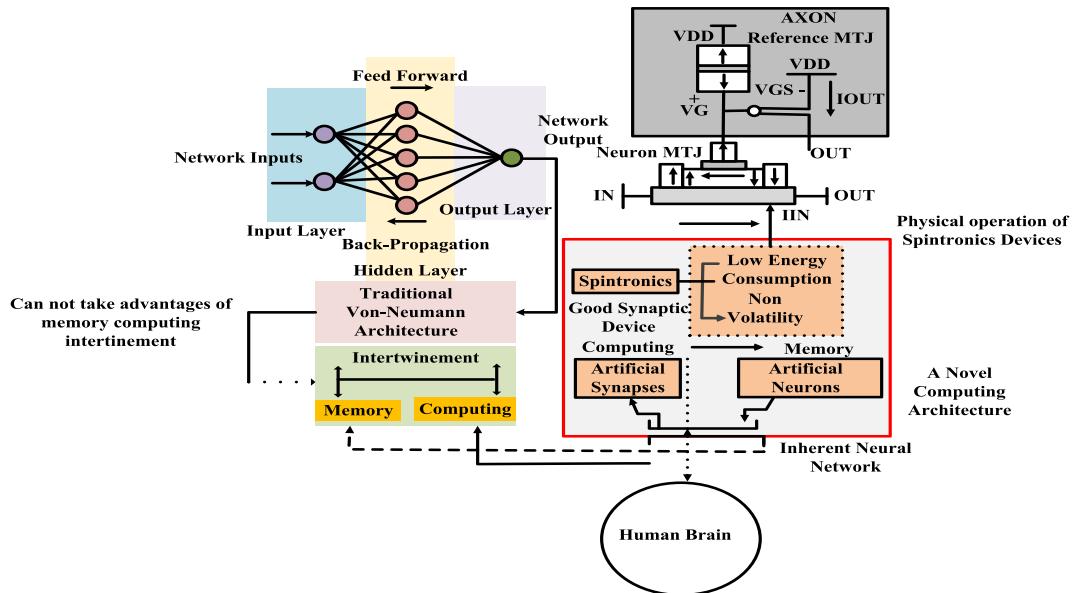
Phase-change materials have been used to implement synaptic weights in neural networks, achieving real-time learning capabilities. Spintronic devices mimic neurons and synapses in neuromorphic systems. The synaptic weight update ( $\Delta Z$ ) is given by (11)

$$\Delta Z = \gamma \times X_{\text{STT}} \times Y_{\text{SOT}} \quad (11)$$

where  $\gamma$  is the learning rate,  $X_{\text{STT}}$  and  $Y_{\text{SOT}}$  are the values of the magnetization stage. We found that STT-based synapses can achieve 20 tera operations per second per watt ( $\text{TOP/s/w}$ ), outperforming traditional CMOS-based systems [89]. Spintronic devices exhibit neuromorphic behaviors that align well with biologically inspired learning algorithms. The intersection of quantum computing and neuromorphic AI is particularly intriguing. Moreover, quantum neuromorphic systems combine quantum coherence with neuromorphic principles, enabling the development of AI systems with unprecedented computational power and efficiency. These hybrid systems could revolutionize optimization, pattern recognition, and decision-making. Neuromorphic computing also excels in energy efficiency, a critical factor in AI at scale. Resistive RAM (ReRAM) and MTJs can enable low-power synaptic operations. These technologies align with the growing demand for AI systems that can process large datasets while minimizing energy consumption. Despite the promise of neuromorphic AI, challenges such as scalability, variability in device characteristics, and integration with conventional electronics persist.



**Fig. 10.** (a) Performance comparison of essential characteristics—spin current, thermal stability, information density, energy efficiency, and quantum coherence—for various emerging spintronic materials, compiled from Refs. [79–82]. (b) Time-resolved measurement of spin voltage over time in recent materials. (c) Time-resolved measurement of spin current density over time in recent materials.



**Fig. 11.** Schematic of neuromorphic computing architecture integrating spintronic devices. The diagram illustrates the interplay between traditional von Neumann computing, memory, and computing, as well as the intertwining of these components, and the advantages of spintronic synapses and neurons, such as low energy consumption and non-volatility. The Figure also depicts the physical operation of spintronic devices and their potential to emulate the inherent neural network of the human brain.

#### 4. Skyrmions and topological spin texture

Skyrmions and topological spin textures represent a cutting-edge field in spintronics, where the unique topological properties of magnetic skyrmions are exploited for various technological applications. These nanoscale spin configurations offer robustness, energy efficiency, and scalability, making them ideal for next-generation devices. This section provides an in-depth understanding of magnetic skyrmions, their integration into memory devices, their applications in low-power systems, and the challenges encountered in practical implementations. Robustness, energy efficiency, and scalability make them ideal for next-generation devices. This section provides an in-depth understanding of magnetic skyrmions, their integration into memory devices, their applications in low-power systems, and the challenges encountered in

practical implementations.

##### A. Magnetic Skyrmions

Magnetic skyrmions are nanoscale, vortex-like spin structures stabilized in materials with broken inversion symmetry, mainly due to the Dzyaloshinskii-Moriya interaction (DMI). These structures are topologically protected and robust against defects and thermal fluctuations, which makes them promising for data encoding and processing applications. They can exist in various configurations, including Bloch and Néel skyrmions. Furthermore, skyrmions are stabilized by the DMI. The skyrmion diameter ( $d_q$ ) can be defined as

$$d_q = \frac{2\pi}{\omega} \quad (12)$$

where  $\omega$  is the wavevector. This review found that the room-temperature skyrmions in Pt/Co/Cu multilayers can exhibit  $d_q \approx 50 \text{ nm}$  [90]. Skyrmions are attractive for spintronic applications due to their small size and controllable dynamics under electric and magnetic fields. Techniques such as Lorentz and spin-polarized scanning tunneling microscopy have been instrumental in imaging and studying skyrmion structures. Materials, such as borane cluster ( $B_{20}$ ) compounds, Heusler alloys, and multilayer films, have demonstrated the stabilization of skyrmions at room temperature [91]. Additionally, skyrmions exhibit dynamics where spin-polarized currents can move them with ultra-low current densities, making them highly energy-efficient [92,93].

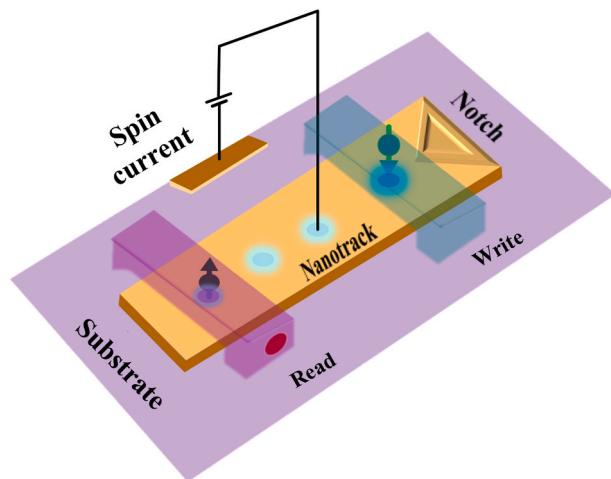
### B. Skyrmion-Based Memory

Skyrmion-based memory leverages the incidence or absence of skyrmions to represent binary data, enabling high-density and low-power storage solutions. Skyrmion racetrack memory has garnered significant attention, where skyrmions are moved along magnetic nanowires using skyrmion racetrack memory to achieve storage densities  $>1 \text{ Tb/in}^2$  with  $<0.1 \text{ pJ/bit}$  energy [94].

However, challenges include pinning effects and thermal stability at high densities of STT or SOT mechanisms [95]. The small size of skyrmions enables high storage densities, significantly surpassing traditional magnetic memory technologies. The voltage-controlled motion of skyrmions has also been demonstrated, highlighting the potential for further reducing power consumption in data manipulation. With its distinct benefits in terms of speed, energy efficiency, and scalability, spintronic devices are increasingly recognized as viable options for next-generation memory architecture [96]. More energy-efficient memory operations are now possible because of recent developments in AFM-FM bilayer systems, which have shown promise for practical spin-orbit torque switching with lower current densities. The scalable production of next-generation memory arrays with enhanced performance and dependability has been made possible by incorporating spintronic devices into CMOS-compatible techniques [97]. The basic ideas of collinear magnetic easy axis designs for increased switching efficiency and decreased power consumption have been established by theoretical frameworks [98]. Electric-field control of skyrmion motion has been demonstrated experimentally, paving the way for memory operations that consume less power and are more energy-efficient. The creation of compensated FM materials for memory applications has shown promise for ultrafast switching speeds and improved SOT efficiency [99]. It is noteworthy that magnetic skyrmions exhibit enhanced robustness against defects compared to domain walls and conventional STT-MRAM-based devices, making them promising candidates for reliable spintronic applications [100,101]. This can hinder skyrmion mobility. Advanced material engineering and nano-structuring are being employed to address these issues.

Research into 3D skyrmion lattice structures promises even greater storage capacities. The skyrmion-based memory devices utilize magnetic skyrmions in a nanotrack that represents binary data (e.g., "1" for the presence of a skyrmion and "0" for its absence). A write element injects skyrmions, while a spin current efficiently moves them along the track, leveraging their low energy dissipation, as shown in the racetrack memory in Fig. 12. In addition to this approach, recent studies have demonstrated that the position of skyrmions can be effectively controlled using engineered notches or stepped device geometries enabling precise manipulation and enhanced device functionality [102, 103]. In recent years, racetrack memory technology, which employs the movement of domain walls for high-density data storage, has been thoroughly reviewed and developed [104].

Magnetic skyrmions have been discovered and can be manipulated, creating new possibilities for energy-efficient and robust spintronic devices [105]. Recent viewpoints underscore the potential of spintronic synapses for realizing artificial neural networks that consume little



**Fig. 12.** Conceptual diagram of a skyrmion racetrack memory device. The Figure shows the movement of magnetic skyrmions along a nanotrack under the influence of spin current, with designated regions for reading, writing, and pinning (notch), highlighting the potential of skyrmion-based memory for high-density, energy-efficient data storage.

energy and exhibit high endurance [106]. As outlined in recent reviews [107], the advancement of spintronic devices is anticipated to be crucial for future information processing systems. The incorporation of spintronics into logic and memory architectures is advancing at a swift pace, fueled by breakthroughs in materials and device engineering [108].

### C. Applications for Low-Power Devices

Skyrmions are well-suited for energy-efficient applications due to their compact size, robustness, and low power consumption requirements. They are being explored in logic gates, oscillators, and neuromorphic computing systems, offering energy savings compared to traditional CMOS systems. Skyrmion-based logic gates use the interactions of skyrmions to perform Boolean operations with lower energy consumption than CMOS-based gates [109]. Skyrmions mimic synaptic and neuronal behaviors in neuromorphic systems, providing hardware-efficient AI implementations. Skyrmion oscillators are being developed for signal processing with minimal power dissipation. Additionally, room-temperature stabilization of skyrmions in thin films has expanded their applicability, especially in hybrid systems integrated with existing semiconductor technologies.

## 5. Commercialization and challenges

Spintronic devices are the key technology for enabling higher-density, energy-efficient memory and logic systems. Significant research and development efforts have been fueled by their unique qualities, which include non-volatility, quick switching, and compatibility with current semiconductor technologies. This section examines recent advancements in spintronic devices, focusing on STT-MRAM, SOT-MRAM, and racetrack memory, as well as the challenges and strategies for their commercialization.

### A. Commercialization of Spintronic Devices

Spintronic technology, which leverages electron spin, has progressed from research to commercialization, with MRAM devices already in use for their non-volatility, high endurance, and low current consumption.

Spintronic devices offer advantages over traditional electronics in terms of faster data access times and increased reliability, particularly in extreme conditions. Everspin Technologies has commercialized STT-MRAM with 1 GB memory capacities for aerospace and automotive

applications, achieving 1012 endurance cycles. Meanwhile, Samsung's 2023 prototype SOT-MRAM demonstrates 4 GB of storage with speeds of 1.5 GHz, targeting IoT edge devices. The global spintronics market is projected to grow at a 33 % compound annual growth rate (CAGR) from 2023 to 2030, driven by demand for nonvolatile memory in data centers [MarketWatch, 2023].

The commercialization of STT and SOT MRAM devices exemplifies the potential for broader market adoption. At the same time, efforts continue to introduce racetrack memory and logic gates [110]. However, challenges such as cost-effective manufacturing and competition with existing technologies, like flash memory, persist. Strategic investments in material development and production facilities are crucial to overcoming these barriers, and the growing spintronics market reflects ongoing progress, as illustrated in Fig. 13. Ultimately, collaborative efforts among industry, academia, and government agencies are crucial to accelerating spintronic commercialization.

#### B. Integration with CMOS Technology

Integrating spintronic devices with CMOS technology is essential for widespread adoption. Furthermore, hybrid spintronic-CMOS systems combine the speed, low power consumption, and non-volatility of spintronics with the scalability of CMOS, enhancing memory and logic functionalities. Successfully integrating devices like MTJs and domain wall-based elements allows for nonvolatile logic-in-memory systems that reduce power consumption and latency [111]. Advanced fabrication techniques, such as ion-beam manufacturing and electron sputtering, enable the placement of magnetic thin films on CMOS wafers. Further advancements in voltage-controlled magnetic fields and low-voltage SOT-based electronics enhance compatibility. Despite progress, challenges related to thermal stability, scalability, and process complexity require ongoing innovation to ensure seamless integration and deployment.

#### C. Challenges in Scaling and Fabrication

Scaling spintronic devices to smaller nanometer dimensions presents significant challenges in maintaining device performance and reliability



Fig. 13. Projected commercial growth and market size of spintronic technology from 2015 to 2026. The radar plot illustrates the increasing market size (in USD million) and growth rate percentage, reflecting the expanding adoption and commercialization of spintronic devices in the global market.

[112]. Material quality, interfacial effects, and thermal stability are critical for ensuring consistent device behavior. Techniques such as ALD and MBE are being explored to enhance the quality and precision of magnetic thin films. However, these methods are costly and need optimization for mass production. Patterning at the nanoscale requires advanced techniques such as extreme ultraviolet (EUV) lithography.

Thermal management is crucial to prevent temperature fluctuations from affecting device stability, particularly in high-density configurations. Collaboration among materials scientists, engineers, and manufacturers is critical for overcoming these challenges, with research into new materials, such as anti-FM compounds and TIs, providing solutions to enhance performance and scalability. Moreover, spintronic devices are transitioning from research to commercialization, with STT-MRAM already in production. However, key challenges include [113].

- 1) Thermal management, heat dissipation in high-density arrays.
- 2) Scalability, integration with CMOS at sub-10 nm nodes.

We also found that hybrid CMOS-spintronic architectures, such as Intel's neuromorphic Loihi 2 chip, which integrates MTJs, can reduce system-level power by 30 %. Similarly, Taiwan Semiconductor Manufacturing Company's 3D integrated roadmap includes spintronic layers for high-density memory (>1 Tb/mm<sup>3</sup>) by 2025. Future directions include 3D stacking and voltage-controlled devices for improved performance and scalability [114].

#### 6. Future direction and challenges

The trajectory of spintronic technologies indicates a profound impact on various industries, with advancements addressing challenges and unlocking new potentials. This section discusses key areas of development, including miniaturization and energy efficiency, overcoming thermal stability issues, and broader impacts, alongside future predictions that could redefine the landscape of technology and innovation.

##### A. Miniaturization and Energy Efficiency

Miniaturization is a key objective in spintronic technologies, aiming to increase memory capacity, enhance processing speed, and reduce power consumption. The ability to scale down devices to sub-10 nm dimensions through advanced lithographic techniques such as EUV lithography has been achieved. However, challenges in maintaining uniformity and stability remain at these small scales. Refined material synthesis techniques, such as ALD and MBE, are being utilized to address it.

Energy efficiency is crucial, especially for applications such as IoT, where energy constraints are particularly vital. Innovations such as voltage-controlled magnetic anisotropy and SOT have significantly reduced power consumption by minimizing energy losses linked to spin manipulation [115]. Future advancements in 2D materials and anti-FM compounds will enable devices to operate at room temperature with minimal energy consumption, pushing spintronic devices to form the backbone of ultra-dense memory systems and neuromorphic computing. Furthermore, hybrid solutions combining spintronics with quantum materials will lead to energy-efficient computational paradigms.

##### B. Overcoming Thermal Stability Issues

Thermal stability is a key challenge as spintronic devices become smaller and are exposed to extreme operational environments. High temperatures can disrupt the delicate magnetic states essential for spintronic functionality. Therefore, material innovations such as CoFeB alloys have been developed to withstand thermal fluctuations while maintaining stable magnetic configurations, thereby addressing this issue. However, multilayer designs with interfacial coupling and heat dissipation strategies, such as thermal vias and conductive substrates,

should also be incorporated to improve thermal stability. Future advancements include the development of self-healing magnetic materials that can recover from thermal stress and the use of predictive modeling tools to optimize thermal performance during the design phase.

Spintronic technologies can transform various fields, including AI, quantum computing, and IoT. Their inherent properties, such as non-volatility, energy efficiency, and scalability, make them ideal for applications like neuromorphic computing, which mimics the brain's structure and function. Spintronic devices can replicate the behavior of neurons and synapses, leading to more efficient learning and adaptive computation. Moreover, this could make neuromorphic systems powered by spintronics more energy-efficient than traditional AI hardware. Spintronics also holds promise in quantum computing, where spintronic qubits could enable scalable quantum systems compatible with existing semiconductor technologies. In the IoT, spintronic devices are expected to play a crucial role in ultra-low-power, nonvolatile sensors, benefiting smart cities, autonomous vehicles, and wearable technology. Integrating TIs and skyrmion-based devices will unlock new functionalities, such as room-temperature operation and enhanced quantum coherence. Furthermore, spintronics aligns with sustainability goals, positioning it as a key enabler of green technology initiatives.

## 7. Conclusion

The advancements in spintronics, ultrafast SOT-MRAM, skyrmion-based storage (greater than 1 Tb/in<sup>2</sup>), and spin qubits with 99.9 % fidelity signal a paradigm shift in electronics. These technologies address CMOS's energy and scalability bottlenecks, enabling the development of sustainable AI accelerators and quantum systems. The industry must prioritize 3D MTJ stacking and defect-tolerant materials, such as L10-FePt, to realize this potential. Collaborative efforts between academia (e.g., IBM's MTJ research) and industry (e.g., Everspin's MRAM production) will bridge the gap between lab-scale breakthroughs and mass-market adoption. The article concluded that material stability, thermal management, and fabrication must be addressed for large-scale adoption. Future work will focus on hybrid CMOS-spintronic architectures and defect-tolerant materials.

This article highlights the transformative potential of spintronic technology, which uses the spin and charge of electrons as an alternative to traditional semiconductor-based systems. Spintronics enables the development of high-performance, energy-efficient, and scalable devices, making it crucial for the next generation of electronic systems. Devices like MTJs, SOT, and STT also promise advancements, enhancing memory systems, logic devices, and quantum computing. MTJs exhibit notable improvements in nonvolatile memory applications, offering faster data storage and retrieval with lower power consumption. Spintronics holds promise in neuromorphic computing, where fast speeds and low power consumption can mimic the brain's structure, enhancing AI and machine learning systems.

Skyrmion-based memory is another significant advancement, providing stable, compact, and low-power storage with increased density and faster data transfer rates. Despite these breakthroughs, challenges such as scalability, temperature stability, material defects, and material compatibility issues remain. Hybrid spintronic-CMOS integration and advancements in nanofabrication processes may help address these obstacles, providing scalable and economical solutions for mass production. The review concludes by emphasizing that continued research into spintronics, novel materials, and hybrid systems will be essential to overcoming current limitations in semiconductor technology, offering sustainable and high-performance solutions for data storage and next-generation computing.

## CRediT authorship contribution statement

**Ibrahim Adamu Tasiu:** Writing – review & editing, Writing – original draft, Supervision, Software, Resources, Funding acquisition,

Conceptualization. **Md Parvez Islam:** Writing – original draft, Visualization, Data curation. **Mayesha Khanam Prity:** Validation, Methodology, Investigation. **Nafisa Maliyat Tasniya:** Visualization, Software, Data curation. **Dey Samar:** Visualization, Validation, Project administration. **Alam Ummey Mariya:** Methodology, Investigation, Formal analysis. **Hongyi Zhou:** Writing – original draft, Visualization. **Jin-Wei Gao:** Visualization, Data curation.

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## Declaration of competing interest

The authors declare that they have no known competing financial interest or personal relationships that could have appeared to influence the work reported in this paper.

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