

Lincoln AI Computing Survey (LAICS) and Trends

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Abstract—In the past year, generative AI (GenAI) models have received a tremendous amount of attention, which in turn has increased attention to computing systems for training and inference for GenAI. Hence, an update to this survey is due. This paper is an update of the survey of AI accelerators and processors from past seven years, which is called the Lincoln AI Computing Survey – LAICS (pronounced “lace”). This multi-year survey collects and summarizes the current commercial accelerators that have been publicly announced with peak performance and peak power consumption numbers. In the same tradition of past papers of this survey, the performance and power values are plotted on a scatter graph, and a number of dimensions and observations from the trends on this plot are again discussed and analyzed. Market segments are highlighted on the scatter plot, and zoomed plots of each segment are also included. A brief description of each of the new accelerators that have been added in the survey this year is included, and this update features a new categorization of computing architectures that implement each of the accelerators.

Index Terms—Machine learning, GPU, TPU, tensor, dataflow, CGRA, accelerator, embedded inference, computational performance

I. INTRODUCTION

In the past 10 years, artificial intelligence and machine learning (AI/ML) has garnered much attention, both in the technical press and in the general media. Starting with deep neural networks (DNNs), then convolutional neural networks (CNNs), and recently generative AI (GenAI), the advances and ensuing exuberance has been energized, in part, by ever-increasing parallel computing capabilities. Much of this capability so far has been delivered to the data center marketplace by Nvidia GPUs, but the sheer size of the AI accelerator market, both in data centers and various embedded “edge” applications, has attracted vast amounts of venture funding for startups and internal development funding in established companies. Further, it has brought to light a wave of innovation in computational architectures, processor-memory interactions, and numerical methods which have been, in many cases, decades in the making.

Perhaps most notable is the emergence of very large GenAI foundation models, which has driven the recent computa-

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tional demand for both training and inference. Before these GenAI models, AI accelerators focused on matrix-matrix fused multiply-add operations, while GenAI models have been emphasizing more matrix-vector fused multiply-add operations and high memory bandwidth to compensate for somewhat lower arithmetic intensity [1]. For training these very large models many more accelerators are being used simultaneously in a synchronous parallel manner interconnected with very high bandwidth networks: Infiniband, NV-Link, and Converged/Ultra Ethernet. However, this survey continues to focus on the accelerators themselves across a wide range of deployed applications – from sub-watt to multi-kilowatts – and on single instances of deployment rather than multiple networked instances. Many new AI accelerators have come to market since the last published iteration of this survey in September 2023, and more insight into the programmability and functionality have been published so another edition of this survey is surely due.

As in past years, this paper continues to focus on accelerators and processors that are geared toward deep neural networks (DNNs), convolutional neural networks (CNNs), and generative AI as they are quite computationally intense. This survey focuses on accelerators and processors for inference for a variety of reasons including that defense and national security AI/ML edge applications rely heavily on inference, though plenty of accelerators in the survey are capable of both inference and training, both computationally and with numerical precisions. And we will consider all of the numerical precision types that an accelerator supports, but for most of them, their best inference performance (both computationally and in accuracy) is in int8 and/or fp16/bf16 (IEEE 16-bit floating point or Google’s 16-bit brain float) precisions.

For much of the background of this study, please refer to the previous IEEE-HPEC papers that our team has published [2]–[6]. The background material in these papers include explanations of the AI ecosystem architecture, the history of the emergence of AI accelerators and accelerators in general, a more detailed explanation of the survey scatter plots, and a discussions of broader observations and trends during each of those years.

II. RELATED WORK

With the amount of research articles and technical press attention that AI accelerators have been given recently, it

should not be surprising that quite a number of surveys have been published recently. There are many surveys [7]–[18] and other papers that cover various aspects of AI accelerators. For instance, the first paper in this multi-year survey included the peak performance of FPGAs for certain AI models; however, several of the aforementioned surveys cover FPGAs in depth so they are no longer included in this survey. Similarly, early surveys often covered research accelerators that were designed, and sometimes produced and tested, to research various features, design choices, and technologies. However, as more commercial accelerators came to market, these research accelerators became less relevant in discussions about what accelerator to use for a project or to deploy in a data center. Hence, research accelerators are no longer included in this survey.

This multi-year survey effort and this paper continues to focus on gathering a comprehensive list of AI accelerators with their computational capability, power efficiency, and ultimately the computational effectiveness of utilizing accelerators in embedded and data center applications. Along with this focus, this paper mainly compares neural network accelerators that are useful for government and industrial sensor and data processing applications. A few accelerators and processors that were included in previous years’ papers have been left out of this year’s survey. They have been dropped because they have been surpassed by new accelerators from the same company, they are no longer offered, or they are no longer relevant to the topic.

III. SURVEY OF PROCESSORS

This paper is an update to IEEE-HPEC papers from the past seven years [2]–[6]. This survey continues to cast a wide net to include accelerators and processors for a variety of applications including defense and national security AI/ML edge applications. The survey collects information on all of the numerical precision types that an accelerator supports, but for most of them, their best inference performance is in int8 or fp16/bf16, so that is what usually is plotted. This survey gathers peak performance and power information from publicly available materials including research papers, technical trade press, and company benchmarks. We have been gathering peak performance and power because it is the most effective for grouping them into application/deployment categories.

All of the AI accelerators for which a marker is plotted is listed in Table I, which summarizes some of the important metadata of the accelerators, cards, and systems, including the labels used in Figure 1. The key metrics of this public data are plotted in Figure 1, which graphs recent processor capabilities (as of Summer 2025) mapping peak performance vs. peak power consumption. As in past years, the x-axis indicates peak power, and the y-axis indicate peak giga-operations per second (GOps/s), both on a logarithmic scale. The computational precision of the processing capability is depicted by the marker used. The form factor, for which peak power is reported, is depicted by color: blue corresponds to a single chip; orange corresponds to a card; and green corresponds to entire

systems (embedded system, single node desktop and server systems). Finally, the hollow markers are peak performance for inference-only accelerators, while the solid markers are performance for accelerators that are designed to perform both training and inference. The same reasonable categorization of accelerators follows their intended application type. The five categories are shown as ellipses on the graph, which roughly correspond to performance and power consumption: Very Low Power for wake word detection, speech processing, very small sensors, etc.; Embedded for cameras, small UAVs, robots, etc.; Autonomous for driver assist services, autonomous driving, and autonomous robots; Data Center Chips and Cards; and Data Center Systems. A zoomed in scatter plot for each of these categories is shown in the subfigures of Figure 2.

TABLE I: List of accelerator metadata, accelerator category, and labels for plots.

Company	Product	Label	Country	Technology	Form Factor	References
AIStorm	AIStorm	AIStorm	USA	analog	Chip	[19]
Alibaba	HanGuang 800	Alibaba	China	tensor	Card	[20]
Amazon	Inferentia	AWSI1	USA	tensor	Card	[21]
Amazon	Inferentia2	AWSI2	USA	tensor	Card	[21]
Amazon	Trainium	AWSt1	USA	tensor	Card	[21]
AMD	MI210	AMD-MI210	USA	GPU	Card	[22]
AMD	MI250	AMD-MI250	USA	GPU	Card	[22]
AMD	MI300X	AMD-MI300X	USA	GPU	Card	[22]
AMD	MI325X	AMD-MI325X	USA	GPU	Card	[23]
AMD	MI350X	AMD-MI350X	USA	GPU	Card	[24]
AMD	MI355X	AMD-MI355X	USA	GPU	Card	[24]
ARM	Ethos N77	Ethos	UK	tensor	Chip	[25]
Aspinity	AML100	AML100	USA	analog	Chip	[26], [27]
Aspinity	AML200	AML200	USA	analog	Chip	[27], [28]
Axlera	Axlera Test Core	Axlera	Netherlands	manycore	Chip	[29]
Baidu	Baidu Kunlun 200	Baidu-K1	China	manycore	Chip	[30]–[32]
Baidu	Baidu Kunlun II	Baidu-K2	China	manycore	Chip	[33]
Biren Technology	br100	br100	China	GPU	Card	[34]–[36]
Biren Technology	br104	br104	China	GPU	Card	[34]–[36]
Blaize	El Cano	Blaze	USA	manycore	Card	[37]
Cambricon	MLU290-M5	Cambricon-M5	China	GPU	Card	[38], [39]
Cambricon	MLU370-X8	Cambricon-X8	China	GPU	Card	[38], [40]
Canaan	Kendrite K210	Kendryte	Singapore	CPU	Chip	[41]
Cerebras	CS-1	CS-1	USA	manycore	System	[42]
Cerebras	CS-2	CS-2	USA	manycore	System	[43]
Cerebras	CS-3	CS-3	USA	manycore	System	[44]
HyperX Logic	HyperX	HyperX	USA	manycore	Chip	[45]
d-Matrix	Corsair	d-Matrix	USA	manycore	Card	[46]
Enflame	Cloudblazer T10	Enflame	China	CPU	Card	[47]
FuriosaAI	RNGD	FuriosaRNGD	S. Korea	tensor	Card	[48], [49]
Google	TPU Edge	TPUedge	USA	tensor	System	[50]
Google	TPU1	TPU1	USA	tensor	Chip	[51], [52]
Google	TPU2	TPU2	USA	tensor	Chip	[51], [52]
Google	TPU3	TPU3	USA	tensor	Chip	[51]–[53]
Google	TPU4i	TPU4i	USA	tensor	Chip	[53]
Google	TPU4	TPU4	USA	tensor	Chip	[54]
Google	TPU5e	TPU5e	USA	tensor	Chip	[55]
Google	TPU5p	TPU5p	USA	tensor	Chip	[55]
Google	TPU6e	TPU6e	USA	tensor	Chip	[55]
Google	TPU7	TPU7	USA	tensor	Chip	[55]
GraphCore	C2	GraphCore	UK	manycore	Card	[56], [57]
GraphCore	C2	GraphCoreNode	UK	manycore	System	[58]
GraphCore	Colossus Mk2	GraphCore2	UK	manycore	Card	[59]
GraphCore	Bow-2000	GraphCoreBow	UK	manycore	Card	[60]
GreenWaves	GAP8	GAP8	France	manycore	Chip	[61], [62]
GreenWaves	GAP9	GAP9	France	manycore	Chip	[61], [62]
Groq	Groq Node	GroqNode	USA	tensor	System	[63]
Groq	Tensor Streaming Proc.	Groq	USA	tensor	Card	[56], [64]
Gyrfalcon	Gyrfalcon	Gyrfalcon	USA	manycore	Chip	[65]
Gyrfalcon	Gyrfalcon	GyrfalconServer	USA	manycore	System	[66]
Hailo	Hailo-8	Hailo-8	Israel	manycore	Chip	[67]
Hailo	Hailo-15H	Hailo-15	Israel	manycore	Chip	[68]
Horizon Robotics	Journey2	Journey2	China	tensor	Chip	[69]
Huawei HiSilicon	Ascend 310	Ascend-310	China	manycore	Card	[70]
Huawei HiSilicon	Ascend 910A	Ascend-910A	China	manycore	Card	[71], [72]
Huawei HiSilicon	Ascend 910B	Ascend-910B	China	manycore	Card	[71], [72]
Huawei HiSilicon	Ascend 910C	Ascend-910C	China	manycore	Card	[71], [72]
IBM	NorthPole	NorthPole	USA	manycore	Chip	[73]–[75]
IBM	Spyre AIU	Spyre	USA	manycore	Card	[76], [77]
Intel	Arria 10 1150	Arria	USA	FPGA	Chip	[78], [79]
Intel	Mobileye EyeQ5	EyeQ5	Israel	manycore	Chip	[37]
Intel	Flex140	Flex140	USA	GPU	Card	[80]
Intel	Flex170	Flex170	USA	GPU	Card	[80]
Intel Habana	Gaudi	Gaudi	Israel	tensor	Card	[81], [82]

Company	Product	Label	Country	Technology	Form Factor	References
Intel Habana	Goya HL-1000	Goya	Israel	tensor	Card	[81]–[83]
Intel Habana	Gaudi2	Gaudi2	Israel	tensor	Card	[84], [85]
Intel Habana	Gaudi3	Gaudi3	Israel	tensor	Card	[84]
Kulraj	Coolidge	Kalray	France	manycore	Chip	[86], [87]
Kneron	KL720	KL720	USA	tensor	Chip	[88]
Maxim	Max 78000	Maxim	USA	tensor	Chip	[89]–[91]
MemoryX	MX3	MX3	USA	manycore	Chip	[92]
Meta/Facebook	MTIA	MTIA	USA	manycore	Card	[93], [94]
Meta/Facebook	MTIA2i	MTIA2i	USA	manycore	Card	[95], [96]
Moore Threads	MTT S50	MTT-S50	China	GPU	Chip	[97]
Moore Threads	MTT S2000	MTT-S2000	China	GPU	Chip	[97]
Mythic	M1076	Mythic76	USA	analog	Chip	[98]–[100]
Mythic	M1108	Mythic108	USA	analog	Chip	[98]–[100]
Neuchips	Raptor	NeuChipsRaptor	Taiwan	tensor	Card	[101]
NovaMind	NovaTensor	NovaMind	USA	tensor	Chip	[102], [103]
NVIDIA	Ampere A10	A10	USA	GPU	Card	[104]
NVIDIA	Ampere A100	A100	USA	GPU	Card	[105]
NVIDIA	Ampere A800	A800	USA	GPU	Card	[106]
NVIDIA	Ampere A30	A30	USA	GPU	Card	[104]
NVIDIA	Ampere A40	A40	USA	GPU	Card	[104]
NVIDIA	Broadwell	B100	USA	GPU	Card	[107]
NVIDIA	Broadwell	B200	USA	GPU	Card	[107]
NVIDIA	DGX-A100	DGX-A100	USA	GPU	System	[108]
NVIDIA	DGX-H100	DGX-H100	USA	GPU	System	[109]
NVIDIA	HGX-B200	HGX-B200	USA	GPU	System	[110]
NVIDIA	Hopper H100 PCIe	H100	USA	GPU	Card	[111]
NVIDIA	Hopper H100 SXM	H100SXM	USA	GPU	Card	[112]
NVIDIA	Hopper H100 NVL	H100NVL	USA	GPU	Card	[111]
NVIDIA	H800 SXM	H800SXM	USA	GPU	Card	[113]
NVIDIA	H800 SXM PCIe	H800	USA	GPU	Card	[113]
NVIDIA	Hopper H200 SMX	H200SXM	USA	GPU	Card	[114]
NVIDIA	Hopper H200 NVL	H200NVL	USA	GPU	Card	[114]
NVIDIA	H20	H20	USA	GPU	Card	[113]
NVIDIA	Jetson AGX Xavier	XavierAGX	USA	GPU	System	[115]
NVIDIA	Jetson NX Orin	OrinNX	USA	GPU	System	[116], [117]
NVIDIA	Jetson AGX Orin	OrinAGX	USA	GPU	System	[116], [117]
NVIDIA	Jetson Xavier NX	XavierNX	USA	GPU	System	[115]
NVIDIA	DRIVE AGX L2	AGX-L2	USA	GPU	System	[118]
NVIDIA	DRIVE AGX L5	AGX-L5	USA	GPU	System	[118]
NVIDIA	L4	L4	USA	GPU	Card	[111]
NVIDIA	L40	L40	USA	GPU	Card	[119]
NVIDIA	L40S	L40S	USA	GPU	Card	[120]
NVIDIA	T4	T4	USA	GPU	Card	[121]
NVIDIA	Volta V100	V100	USA	GPU	Card	[122], [123]
Perceive	Ergo	Perceive	USA	tensor	Chip	[124]
Preferred Networks	MN-Core1	MN-C1	Japan	manycore	Card	[125]–[127]
Preferred Networks	MN-Core2	MN-C2	Japan	manycore	Card	[125], [128]
Quadratic	q1-64	Quadratic	USA	manycore	Chip	[129]
Qualcomm	Cloud AI 100	Qcomm	USA	GPU	Card	[130], [131]
Qualcomm	QRB5165	RBS	USA	GPU	System	[132]
Qualcomm	QRB5165N	RB6	USA	GPU	System	[133]
Rebellions	ATOM Max	ATOM-Max	S. Korea	tensor	Card	[134]–[136]
SiMa.ai	SiMa.ai	SiMa.ai	USA	tensor	Chip	[137]
Syntiant	NDP101	Syntiant1	USA	manycore	Chip	[138], [139]
Syntiant	NDP250	Syntiant3	USA	manycore	Chip	[140]
Tachyum	Prodigy	Tachyum	USA	manycore	Chip	[141]
Tenstorrent	Greyskull	Greyskull	USA	manycore	Card	[142]
Tenstorrent	Wormhole n300	Wormhole	USA	manycore	Card	[143], [144]
Tenstorrent	Blackhole	Blackhole	USA	manycore	Card	[145], [146]
Tesla	Full Self-Driving Comp.	TeslaFSD	USA	tensor	System	[147], [148]
Tesla	Dojo D1	DojoD1	USA	manycore	Chip	[149], [150]
Texas Instruments	TDA4VM	TexInSt	USA	manycore	Chip	[151]–[153]
Toshiba	2015	Toshiba	Japan	manycore	System	[154]

For most of the accelerators, their descriptions and commentaries have not changed since last year so please refer to the previous papers of this survey project for descriptions and commentaries. Several new releases and a few departures are included in this update, and they are chronicled next.

- Amazon AWS has published much more information about their Inferentia and Trainium chips, which have been design by their in-house Annapurna Labs Division. These accelerators are multi-core tensor accelerators [22], and we can expect newer generations of these chips in coming years.
- During the past two years, AMD released the MI300 series of GPUs to compete head-to-head with Nvidia's data center GPUs, namely the MI300X, MI325X, MI350X, and MI355X. Each provided ample competition to the Nvidia counterparts [24], with FP6 and FP4 support and enhanced matrix engines.
- Nvidia continues to release a variety of data center GPUs in order to keep their lead in supplying GPUs for both training and inference. In the past two years, Nvidia released the L4 and L40S for cloud graphics and low-power

inference, several variants of the Hopper GPUs (H100 NVL, H200 SMX, and H200 NVL), and two variants of the Broadwell GPU (B100 and B200). The Hopper and Broadwell GPUs are true transformer/generative AI accelerators with larger matrix engines (TensorCores) along with FP6 and FP4 support. To address export restrictions, Nvidia also released detuned versions of their A100, H100, and H200 GPUs with the A800, H800, and H20 GPUs, respectively.

- Intel has been consolidating their AI accelerator efforts. Intel's Habana subsidiary released their Gaudi2 and Gaudi3 tensor accelerators, which have gained some good traction. Given that traction, Intel has cancelled their GPU training offerings (Xe-HPC, codename Ponte Vecchio and future Rialto Bridge GPU), while still offering the Flex line of data center inference GPUs. On the software side, Intel has integrated CPU, GPU, and FPGA programming into their OneAPI software stack.
- Alphabet Google has continued to refine and improve the performance of their cloud data center TPUs with the releases of their TPU5e, TPU5p, TPU6e, and TPU7 [55]. Each improves performance over the previous generation for their own and their clients' workloads.
- Cerebras has released their third generation Wafer Scale Engine (WSE) accelerator, CS-3, with impressive performance both as a single node and networked multi-node training [44].
- Tesla Motors released details about their Dojo1 data center training chip and system, disclosing an impressive design for very large scale training [149], [150].
- Meta/Facebook has also released many more details about the first and second generation Meta Training and Inference Accelerator (MTIA and MTIA2i), which are both focused on inference. They are both comprised of an 8-by-8 network meshed set of processing elements, and each processing element includes two RISC-V cores for computation. One of the two RISC-V cores includes a 64-element RISC-V vector extension [94], [95].
- Speaking of RISC-V cores, Tenstorrent has released their second and third iteration of their RISC-V based accelerators, the Wormhole and Blackhole. The Wormhole accelerator is comprised of 80 Tensix processor, each of which is comprised of five RISC-V cores, for a total of 400 RISC-V cores. The Blackhole processor expands this to 140 Tensix processors, each also with five RISC-V cores, for a total of 700 RISC-V cores. Blackhole also includes 16 higher performance RISC-V cores for on-device hosting and running Linux and another 52 smaller RISC-V cores for memory management, communications, and system management [145].
- Based on take-aways of the DARPA Synapse neuromorphic computing project from a decade ago, which included the development of the IBM TrueNorth accelerator [155]–[157], IBM has been developing and released the NorthPole inference accelerator [73]–[75]. It features 256 cores that can execute 8-bit, 4-bit, and 2-bit digital

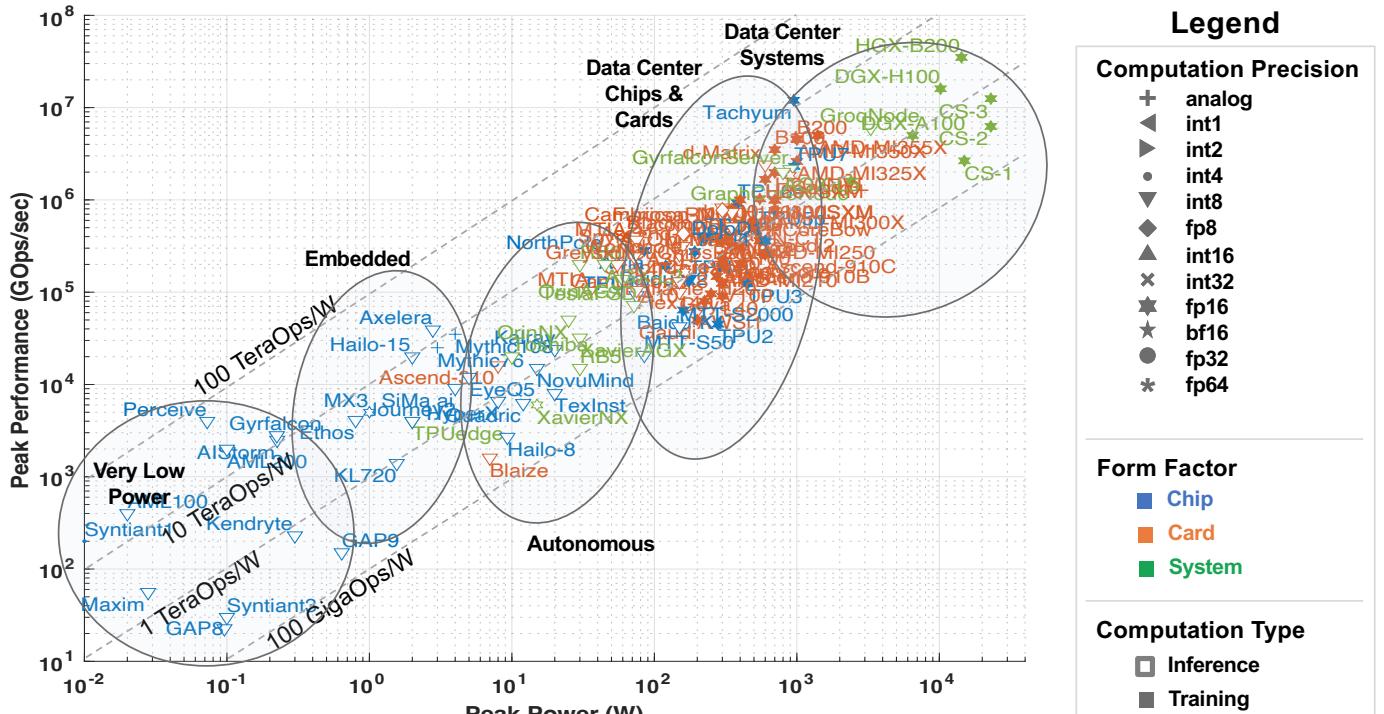


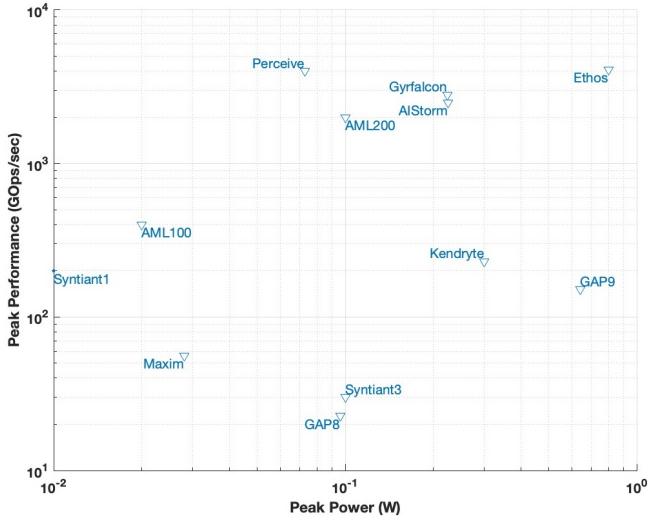
Fig. 1: Peak performance vs. power scatter plot of publicly announced AI accelerators and processors.

arithmetic. It also has four on-chip networks to minimize communication hotspots. IBM has also announced that they will be releasing their AI Acceleration Unit (AIU) in 2026 as a PCIe card called Spyre [76], [77].

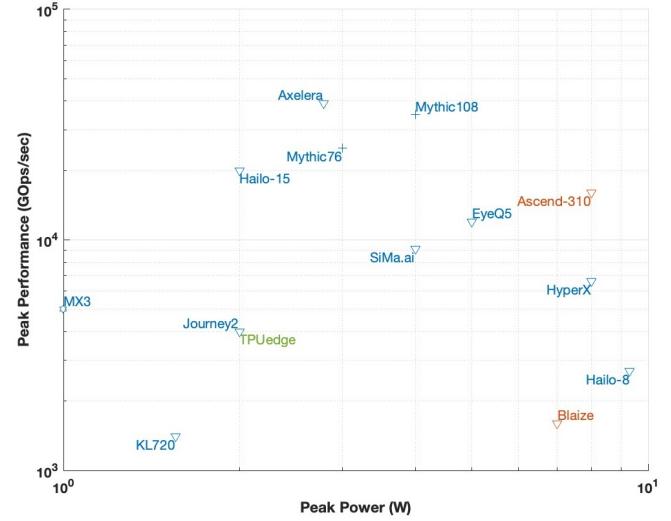
- arithmetic. It also has four on-chip networks to minimize communication hotspots. IBM has also announced that they will be releasing their AI Acceleration Unit (AIU) in 2026 as a PCIe card called Spyre [76], [77].
 - Japanese company Preferred Networks has released its second generation MN-Core2 chip, of which eight are integrated on each PCIe card [125], [128]. The accelerator is aimed at training in that it supports FP16, FP32, and FP64. Future versions will have an inference-focused version and a training-focused version.
 - China's Huawei released two new versions of the Ascend 910: the 910B and 910C [71], [72]. The original 910 has been labeled the 910A. These new Ascend accelerators have the same core design of the 910A, but they are now fabbed indigenously by SMIC (rather than TSMC in Taiwan due to American export restrictions).
 - China's Cambricon, known mainly for its Kiren smartphone GPUs, has also recently released data center GPUs including the MLU290-M5 and MLU370-X8 [38].
 - Moore Threads, another Chinese GPU company, has emerged with a series of GPUs that can be used for business computers, gaming, and AI inference [97].
 - HyperX Logic (formerly Coherent Logix) previous generation HX40416 accelerator features 416 processing elements in a mesh topology, and each PE can execute 4 multiply-accumulate operations per clock cycle [45]. HyperX Logic has been focused on space applications along with audio and video production with its programmable dataflow architecture, and has added AI inference applications to its application portfolio in recent years.

- The d-Matrix Corsair accelerator features arithmetic in SRAM memory cores and RISC-V control CPUs [46]. Each Corsair chiplet has 256 64-by-64 SRAM-arithmetic cell array cores, and there are four chiplets per Corsair package. A Corsair PCIe card has two Corsair packages, which totals 2048 cell array cores. This accelerator is aimed at small-batch, low-latency data center inference.
 - The FuriosaAI RNGD implements tensor contractions as a computational primitive for AI inference [49]. Each Tensor Unit has 64 slices, and each slice has a tensor engine, vector engine and transpose engine. The accelerator is coupled to HBM memory for high bandwidth memory access for executing inference on very large models.
 - Taiwan startup Neuchips introduced their Raptor N3000 AI accelerator chip, which is featured in their first product, the Evo accelerator PCIe card. The Raptor chip includes 10 matrix engines, two vector engines, and an embedding engine [158].
 - South Korean startup Rebellions released their ATOM Max accelerator for data center inference [135], [136].
 - Finally, Syntiant has expanded its very-low power analog accelerator offerings with their NDP250 chip and at audio processing and wake word detection [140].

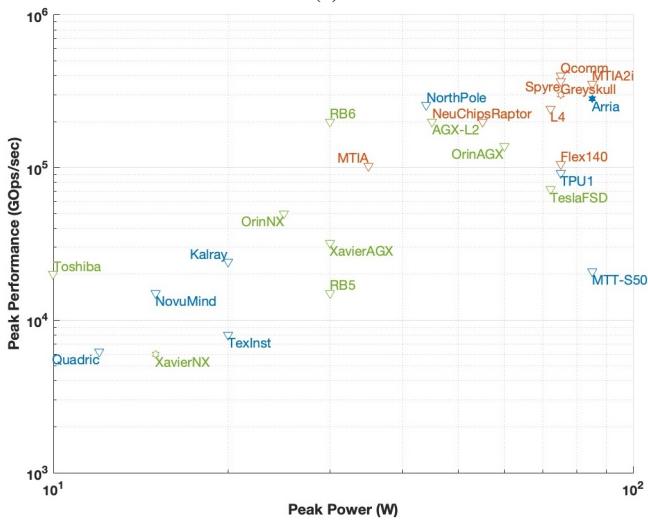
Attrition among AI startups and corporate efforts continue to be part of normal business patterns. These accelerators have been removed from the survey because their accelerator(s) are no longer commercially available. Cornami has been removed because the company has moved their focus to embedded computing solutions for homomorphic encryption. AIotive has been removed because their accelerator product line is an



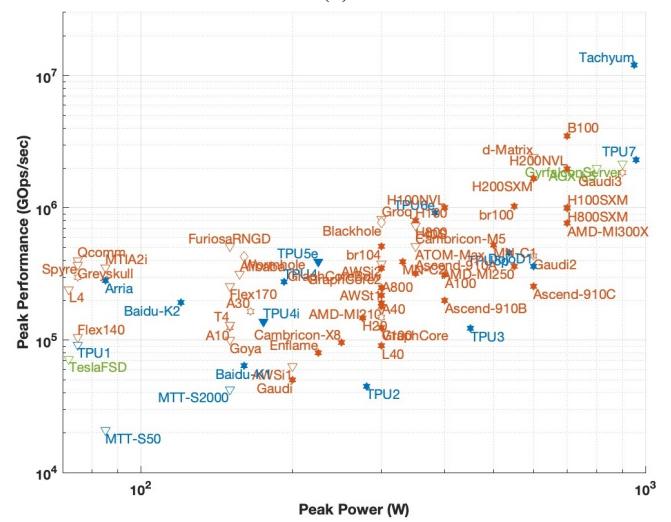
(a)



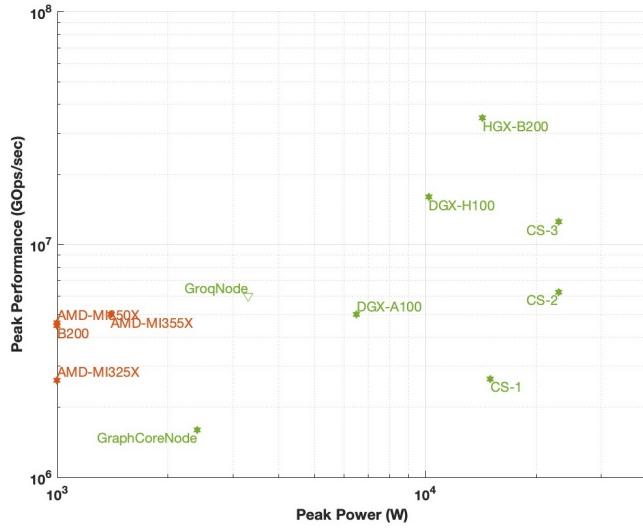
(b)



(c)



(d)



(e)

Fig. 2: Zoomed regions of peak performance vs. peak power scatter plot: **(a)** very low power, **(b)** embedded, **(c)** autonomous, **(d)** data center chips and cards, **(e)** data center systems.

RTL specification rather than a chip product. Three companies have been acquired or are closing down. The staff of Untether AI has been acquired by AMD, and the company is in the process of winding down [159], while Esperanto is also winding down with almost all of their employees having found other opportunities [160]. Further, AlphaICs does not appear to be in business anymore, so their entry has been removed. Finally, after delivering the impressive Aurora supercomputer at Argonne National Laboratory, Intel cancelled its Xe-HPC (codenamed Ponte Vecchio) and plans for other high end computational GPUs.

We are also anxiously awaiting more details about several accelerators that have been announced, including peak performance and peak power numbers. Among the major American GPU vendors, Nvidia has released the names of the next two generations of GPUs, the Ruben and Feynman GPUs, while AMD has announced the expected release their MI430X and MI450X in the first half of 2026. Similarly, Baidu has announced its third generation P800 Kunlun accelerator [161], while there is discussion that Huawei will be releasing Ascend 920 and 920C accelerators soon [113]. HyperX Logic has released a new space-focused accelerator called Midnight, for which we are hoping to see performance and power numbers. Horizon Robotics, which specializes in automotive inference accelerators has released Journey 5 and Journey 6 accelerators, but peak performance and power numbers are not yet available. Tesla has announced their Full Self-Driving Computer V2 (Gen5), but no details have been published yet. Finally, Q.ANT has released an optical accelerator, which is able to compute entire inference chains in the optical domain. This first version demonstrates the capability and opportunity of computing in the optical domain; their roadmap expects to meet and exceed the computational performance and energy efficiency of CMOS-based accelerators within the next few years.

IV. OBSERVATIONS AND TRENDS

In the past two years since the last iteration of this survey, more details have been published in conference papers, journal papers, and technical press articles that have made it possible to more accurately generalize the main categories of architectures that are being used for AI processors/accelerators. These are summarized in Figure 3, and the categories span from highly flexible CPUs on the left to statically deployed FPGAs and ASICs on the left.

While CPUs are very flexible and can execute all applications, they are not optimized to execute the highly parallel computations of inference and training. CPU vector engines are better suited for inference and training than CPUs, but they generally do not have memory coalescing features to pack strided memory accesses into dense vector accesses, which affects their parallel computational efficiency.

At the other end of the categories are FPGAs and ASICs. We do not see ASICs much because of the requirement for most AI applications to support multiple different AI models with the same compute hardware. Similarly, FPGAs are used in embedded applications when AI models have been chosen

for deployment, and some FPGAs even have tensor accelerator blocks included in the available computational blocks.

The bulk of high performance and efficient accelerators are parallel thread accelerators (GPUs), tensor array accelerators, and microcore mesh accelerators because they are designed specifically for high main memory bandwidth, highly parallel computation and highly parallel and complex data movement that are required for highly efficient and highly performing inference and training. Among these, parallel thread accelerators are the most flexibly of these parallel compute engines. They have memory coalescing capability along with parallel compute cores (Symmetric Multiprocessors – SMs - in Nvidia parlance) that are dynamically scheduled with compute kernels. Code redesign and recompilation of kernels is fairly quick. Tensor array accelerators microcore mesh accelerators are more statically scheduled in that one preloads the model parameters and code into the accelerator before executing inference or training on them. To change the model parameters or code, the new one needs to be loaded into the accelerator anew, which involves some latency. Kernel code redesign and recompilation involves both compilation and mapping of the model code and parameters onto the compute elements, which involves an optimization of code and resources thereby taking more time than just compiling the numerical kernel code. But this often results in more efficient execution and higher performance than parallel thread accelerators.

There are several more observations and comments for us to appreciate on Figure 1.

- Int8 continues to be the default numerical precision for embedded, autonomous and data center inference applications, and fp16/bf16 has become the default numerical precision for training. However, some favorable outcomes have come from training in fp8 and even fp4, particularly for generative AI models, which save both computational and data movement energy.
- In our re-evaluation and re-categorization of each of the accelerators in this survey, we were pleasantly surprised by the variety of architectural choices being made to experiment, find, and exploit competitive advantages for using their accelerator in certain applications and for certain models. This was predicted in Nowatzki, et al. [162], and it is encouraging to see it play out in commercial competition.
- In the data center domain, Nvidia continues to dominate the media coverage and sales for AI acceleration. However, AMD, Groq and Cerebras have become significant competitors to Nvidia, while many other commercial offerings are also gaining footholds. And it should be noted that the Groq accelerator is currently being manufactured using a 12-nm process and often outperforming accelerators at smaller circuit feature sizes, which supports the findings in [163]. (Groq has announced a second generation accelerator that will be fabbed at a smaller circuit feature size.) And both Groq and Cerebras accelerators are not GPU architectures.



	CPU Core	CPU Core Vector Engine	Parallel Thread Accelerator (GPUs)	Tensor Array Accelerator (TPU, Groq, TensorCore)	Microcore Mesh Accelerator (Cerebras, TensorCore)	Computational Block Accelerator (FPGA)	Custom Dataflow Accelerator (ASIC)
Technology label	CPU	Vector	GPU	Tensor	Manycore	FPGA	ASIC
ALUs per core	1-4	8-32	32-64	8x8 to 256x256	1 to 4	Various	App. specific
Cores per processor	4-64	4-64	8-128	1 to 4	100s to 1M	Various	App. specific
Parallel performance	Low	Medium Low	Medium High	High	High	High	Very High
Comp. efficiency (Ops/W)	Low	Medium Low	Medium	High	High	High	Very High
Comp. flexibility	Very High	Medium Low	Medium	Medium Low	Medium	Low	Very Low
Computation scheduling	Dynamic by instruction	Dynamic by instruction	Dynamic by kernel	Static by kernel	Static by kernel	Fixed	Fixed
Code redesign	Seconds	Seconds	Seconds/Minutes	Minutes	Minutes/Hours	Hours	Months

Increasing application specificity -> greater parallel performance -> narrower application/computational kernel enablement

Fig. 3: Range of AI accelerator computer architecture categories. Going from left to right, greater optimization of data movement between computations means data travels less distances between computations, and more computations executed in parallel. However, it also means less flexibility in operation types and programmability. CPU = Central Processing Unit; AVX = Advanced Vector eXtensions; SVE = Scalable Vector Extensions; GPU = Graphics Processing Unit; TPU = Tensor Processing Unit; CGRA = Course Grained Reconfigurable Architecture FPGA = Field Programmable Gate Array; ASIC = Application Specific Integrated Circuit

A. Non-CMOS Technologies

As part of this survey, we continue to track other technologies that could be used to implement AI accelerators. Among them are memristors, neuromorphic architectures, cryogenic computing, and optical computing. In all of these domains, research and development continues to show opportunity and hope to become competitive with current commercial offerings. The one new development that is worth noting is in the optical computing area. While we still wait for the release of a commercial accelerator from LightMatter, Lightelligence, and LightOn (we are assured that they are coming!), Q.ant has released a commercial optical accelerator, as we mentioned Section III. This is an exciting development, and we will be watching how they and other optical computing vendors compete among computational accelerators.

V. SUMMARY

This paper updates the Lincoln AI Computing Survey (LAICS) of AI accelerators that span from extremely low power through embedded and autonomous applications to data center class accelerators for inference and training. We presented the new full scatter plot along with zoomed in scatter plots for each of the major deployment/market segments, and we discussed the new additions for the year. We also included a categorization of AI computing hardware based on much new material that has been published for these AI accelerators.

VI. DATA AVAILABILITY

The data spreadsheets and references that have been collected for this study and its papers are posted at <https://github.com/areuther/ai-accelerators> after they have cleared the release review process.

ACKNOWLEDGEMENT

We express our gratitude to LaToya Anderson, Masahiro Arakawa, Bill Arcand, Bill Bergeron, David Bestor, Bob Bond, Alex Bonn, Chansup Byun, Vitaliy Gleyzer, Jeff Gottschalk, Michael Houle, Matthew Hubbell, Hayden Jananthan, David Martinez, Lauren Milechin, Sanjeev Mohindra, Paul Monticciolo, Julie Mullen, Andrew Prout, Stephan Rejto, Antonio Rosa, Charles Yee, and Marc Zissman for their support of this work. We are also grateful to Mark Gouker, Bob Atkins, and Livia Racz for the discussions that eventually were captured in the accelerator categorizations.

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