



# **DesignWare**

## **Building Block IP**

### **Documentation Overview**



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# DesignWare Building Block IP Documentation Overview

DesignWare Building Block IP comprise a technology-independent, microarchitecture-level library that is tightly integrated into the Synopsys synthesis environment. This product was formally known as the DesignWare Foundation Library. A more complete introduction is available in [DesignWare Building Block IP Introduction](#).

The following sections list the entire documentation set and datasheets that supports this library:

- [“DesignWare Building Block IP Document List”](#) on page 3
- [“List of DesignWare Building Block IP”](#) on page 5
- [“Obsoleted IP for New Designs”](#) on page 13

Note: This information is now found in the Release Notes.

## 1.1 DesignWare Building Block IP Document List

**Table 1-1 DesignWare Building Block IP Documentation**

<a href="#">DesignWare Building Block IP Release Notes</a> manuals/dwbb_relnotes.pdf	Contains usage issues for DesignWare Building Block IP Library components (F-2011.09) for Design Compiler DWBB_201012.5.
<a href="#">DesignWare IP Family Reference Guide</a> manuals/dw_digital_ip_quickref.pdf	Provides general information for most DesignWare Synthesizable and Verification IP.
<a href="#">DesignWare Building Block Quick Reference</a> manuals/dwbb_quickref.pdf	Provides a brief pin and parameter descriptions for all the DesignWare Building Block IP in a single document.
<a href="#">DesignWare Building Block IP QuickStart</a> datasheets/dwbb_quickstart.pdf	Provides a quick look-up list of things you need to know to get started with the library of DesignWare Building Block IP.
<a href="#">Basic Library Components Overview</a> datasheets/dwbb_basiclib.pdf	Describes the Basic Library components, which provide basic implementations of common arithmetic functions that can be referenced by HDL operators in your VHDL or Verilog source code.
<a href="#">DesignWare Building Block IP User Guide</a> manuals/dwbb_userguide.pdf	Explains the use of DesignWare Building Block IP.
<a href="#">DesignWare Building Block IP Application Notes</a> manuals/dwbb_appnotes.pdf	A complete compilation of Application Notes that support the DesignWare Building Block IP.

**Table 1-1 DesignWare Building Block IP Documentation (Continued)**

<a href="#">DesignWare Building Block IP Developer Guide manuals/dwdg.pdf</a>	This manual is for silicon suppliers, systems companies, and third party macro and model development houses who want to develop technology-specific designs or proprietary DesignWare components.
<a href="#">Designware GTECH Library Databook manuals/dw_gtech.pdf</a>	Provides detailed datasheets for the GTECH Library components.

## 1.2 DesignWare minPower Components Documentation

NOTE: DesignWare minPower Components documentation is available on the Synopsys website, and requires access authentication.

**Table 1-2 DesignWare minPower Components Documentation**

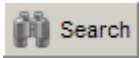
<a href="https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_overview.pdf">DesignWare minPower Components Documentation Overview</a> https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_overview.pdf	Lists the minPower Components documentation, which provide Low Power implementations of common arithmetic functions.
<a href="https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_relnotes.pdf">DesignWare minPower Components DC Release Notes</a> https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_relnotes.pdf	Contains usage issues for DesignWare minPower Components (F-2011.09) for Design Compiler DWBB_201012.5.
<a href="https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_userguide.pdf">DesignWare minPower Components User Guide</a> https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_userguide.pdf	Explains the use of DesignWare minPower Components.
<a href="https://www.synopsys.com/dw/doc.php/doc/dwmp/datasheets/minpower_overview.pdf">DesignWare minPower Components Overview</a> https://www.synopsys.com/dw/doc.php/doc/dwmp/datasheets/minpower_overview.pdf	A listing and brief description of the DesignWare minPower Components. Use this document to access minPower Component datasheets.

### 1.3 Synopsys Common Licensing (SCL)

You can find general SCL information on the following page:

<http://www.synopsys.com/keys>

### 1.4 Searching PDF Files



You can search for a text string within a single PDF document or entire document set using the Search feature of Adobe Reader (formerly Acrobat Reader).

You can search equally well through an individual PDF file located on a web server or on your local file system; however, in order to search through a collection of PDF files, those files must reside on your local file system.

In addition, many collections of PDF files provided by Synopsys are preconfigured with a search index file called INDEX.PDX, which enables even faster search operations. If an INDEX.PDX file is available, the Adobe Reader locates the file automatically for use in the next search operation.

### 1.5 For More Information About Adobe Reader

For more information about using Adobe Reader, refer to the online guide:

Help > Adobe Reader Help

You can also get useful information and download the most recent version of the Reader from the Adobe website:

<http://www.adobe.com>

### 1.6 Additional Information

For additional Synopsys documentation, refer to the following location:

<http://www.synopsys.com/products/designware/docs>

For up-to-date information about the latest verification models and synthesizable IP available from Synopsys, visit the IP Directory:

<http://www.synopsys.com/products/designware/ipdir>

#### 1.6.1 List of DesignWare Building Block IP

The following table provides links to each datasheet. New IP (2010.12 and later) are indicated with a **New** label; updates to existing IP with the **Updated** label. IP that are obsolete for new designs are listed on [page 13](#).

**Table 1-3 List of DesignWare Building Block IP**

IP	Description
<b>Application Specific: Control Logic</b> ( <a href="#">Overview</a> )	
<a href="#">DW_arb_2t</a>	Two-Tier Arbiter with Dynamic/Fair-Among-Equal Scheme
<a href="#">DW_arb_dp</a>	Arbiter with Dynamic Priority Scheme

**Table 1-3 List of DesignWare Building Block IP (Continued)**

IP	Description
<a href="#">DW_arb_fcfs</a>	Arbiter with First-Come-First-Served Priority Scheme
<a href="#">DW_arb_rr</a>	Arbiter with Round Robin Priority Scheme
<a href="#">DW_arb_sp</a>	Arbiter with Static Priority Scheme
<b>Datapath: Arithmetic Components</b> ( <a href="#">Overview</a> )	
<a href="#">DW01_absval</a>	Absolute Value
<a href="#">DW01_add</a>	Adder
<a href="#">DW01_addsub</a>	Adder-Subtractor
<a href="#">DW_addsub_dx</a>	Duplex Adder/Subtractor with Saturation and Rounding
<a href="#">DW01_ash</a>	Arithmetic Shifter
<a href="#">DW_bin2gray</a>	Binary to Gray Converter
<a href="#">DW01_bsh</a>	Barrel Shifter
<a href="#">DW01_cmp2</a>	2-Function Comparator
<a href="#">DW01_cmp6</a>	6-Function Comparator
<a href="#">DW_cmp_dx</a>	Duplex Comparator
<a href="#">DW_cntr_gray</a>	Gray Code Counter
<a href="#">DW01_csa</a>	Carry Save Adder
<a href="#">DW01_dec</a>	Decrementer
<a href="#">DW_div</a>	Combinational Divider
<a href="#">DW_div_pipe</a>	Stallable Pipelined Divider
<a href="#">DW_exp2</a>	Base 2 Exponential ( $2^a$ ) ( <a href="#">datasheet updated</a> )
<a href="#">DW_gray2bin</a>	Gray to Binary Converter
<a href="#">DW01_inc</a>	Incrementer
<a href="#">DW01_incdec</a>	Incrementer-Decrementer
<a href="#">DW_inc_gray</a>	Gray Incrementer
<a href="#">DW_inv_sqrt</a>	Reciprocal of Square-Root ( <a href="#">datasheet updated</a> )
<a href="#">DW_lbsh</a>	Barrel Shifter with Preferred Left Direction
<a href="#">DW_ln</a>	Natural Logarithm ( $\ln(a)$ )
<a href="#">DW_log2</a>	Base 2 Logarithm ( $\log_2(a)$ ) ( <a href="#">datasheet updated</a> )
<a href="#">DW02_mac</a>	Multiplier-Accumulator
<a href="#">DW_minmax</a>	Minimum/Maximum Value

**Table 1-3 List of DesignWare Building Block IP (Continued)**

IP	Description
DW02_mult	Multiplier
DW02_multp	Partial Product Multiplier
DW02_mult_2_stage	Two-Stage Pipelined Multiplier
DW02_mult_3_stage	Three-Stage Pipelined Multiplier
DW02_mult_4_stage	Four-Stage Pipelined Multiplier
DW02_mult_5_stage	Five-Stage Pipelined Multiplier
DW02_mult_6_stage	Six-Stage Pipelined Multiplier
DW_mult_dx	Duplex Multiplier
DW_mult_pipe	Stallable Pipelined Multiplier
DW_norm	Normalization for Fractional Input
DW_norm_rnd	Normalization and Rounding
DW_piped_mac	Pipelined Multiplier-Accumulator
DW02_prod_sum	Generalized Sum of Products
DW02_prod_sum1	Multiplier-Adder
DW_prod_sum_pipe	Stallable Pipelined Generalized Sum of Products
DW_rash	Arithmetic Shifter with Preferred Right Direction
DW_rbsh	Barrel Shifter with Preferred Right Direction
DW01_satrnd	Arithmetic Saturation and Rounding Logic
DW_shifter	Combined Arithmetic and Barrel Shifter
DW_sla	Arithmetic Shifter with Preferred Left Direction (VHDL style)
DW_sra	Arithmetic Shifter with Preferred Right Direction (VHDL style)
DW_square	Integer Squarer
DW_squarep	Partial Product Integer Squarer
DW_sqrt	Combinational Square Root (datasheet updated)
DW_sqrt_pipe	Stallable Pipelined Square Root
DW01_sub	Subtractor
DW02_sum	Vector Adder
DW02_tree	Wallace Tree Compressor

**Table 1-3 List of DesignWare Building Block IP (Continued)**

IP	Description
<b>Datapath: Floating Point (<a href="#">Overview</a>)</b>	
<a href="#">DW_fp_add</a>	Floating Point Adder
<a href="#">DW_fp_addsub</a>	Floating Point Adder/Subtractor
<a href="#">DW_fp_cmp</a>	Floating Point Comparator
<a href="#">DW_fp_div</a>	Floating Point Divider
<a href="#">DW_fp_div_seq</a>	Floating Point Sequential Divider
<a href="#">DW_fp_dp2</a>	2-Term Floating Point Dot-product
<a href="#">DW_fp_dp3</a>	3-Term Floating Point Dot-product
<a href="#">DW_fp_dp4</a>	4-Term Floating Point Dot-product
<a href="#">DW_fp_exp</a>	Floating Point Exponential ( $e^a$ )
<a href="#">DW_fp_exp2</a>	Floating Point Base-2 Exponential ( $2^a$ ) ( <a href="#">datasheet updated</a> )
<a href="#">DW_fpflt2i</a>	Floating Point to Integer Converter
<a href="#">DW_fpi2flt</a>	Integer to Floating Point Converter
<a href="#">DW_fp_invsqrt</a>	Floating Point Reciprocal of Square Root ( <a href="#">datasheet updated</a> )
<a href="#">DW_fp_ln</a>	Floating Point Natural Logarithm ( $\ln(a)$ )
<a href="#">DW_fp_log2</a>	Floating Point Base 2 Logarithm ( $\log_2(a)$ ) ( <a href="#">datasheet updated</a> )
<a href="#">DW_fp_mac</a>	Floating Point Multiply-and-Add
<a href="#">DW_fp_mult</a>	Floating Point Multiplier
<a href="#">DW_fp_recip</a>	Floating Point Reciprocal ( $1/a$ ) ( <a href="#">datasheet updated</a> )
<a href="#">DW_fp_sincos</a>	Floating Point Sine and Cosine ( <a href="#">datasheet updated</a> )
<a href="#">DW_fp_sqrt</a>	Floating Point Square Root ( <a href="#">datasheet updated</a> )
<a href="#">DW_fp_square</a>	Floating Point Square
<a href="#">DW_fp_sub</a>	Floating Point Subtractor
<a href="#">DW_fp_sum3</a>	3-input Floating Point Adder
<a href="#">DW_fp_sum4</a>	4-input Floating Point Adder
<b>Datapath: Sequential (<a href="#">Overview</a>)</b>	
<a href="#">DW_div_seq</a>	Sequential Divider
<a href="#">DW_fp_div_seq</a>	Floating Point Sequential Divider
<a href="#">DW_mult_seq</a>	Sequential Multiplier
<a href="#">DW_sqrt_seq</a>	Sequential Square Root



**Table 1-3 List of DesignWare Building Block IP (Continued)**

IP	Description
<b>Datapath: Trigonometric</b> ( <a href="#">Overview</a> )	
<a href="#">DW_sincos</a>	Combinational Sine - Cosine ( <a href="#">datasheet updated</a> )
<b>Data Integrity</b> ( <a href="#">Overview</a> )	
<a href="#">DW_crc_p</a>	Universal Parallel (Combinational) CRC Generator/Checker
<a href="#">DW_crc_s</a>	Universal Synchronous (Clocked) CRC Generator/Checker
<a href="#">DW_ecc</a>	Error Checking and Correction
<a href="#">DW04_par_gen</a>	Parity Generator and Checker
<b>Data Integrity: Coding</b> ( <a href="#">Overview</a> )	
<a href="#">DW_8b10b_dec</a>	8b10b Decoder
<a href="#">DW_8b10b_enc</a>	8b10b Encoder
<a href="#">DW_8b10b_unbal</a>	8b10b Coding Balance Predictor
<b>Digital Signal Processing (DSP)</b>	
<a href="#">DW_fir</a>	High-Speed Digital FIR Filter
<a href="#">DW_fir_seq</a>	Sequential Digital FIR Filter Processor
<a href="#">DW_iir_dc</a>	High-Speed Digital IIR Filter with Dynamic Coefficients
<a href="#">DW_iir_sc</a>	High-Speed Digital IIR Filter with Static Coefficients
<a href="#">DW_dct_2d</a>	Two Dimensional Discrete Cosine Transform
<a href="#">DW_decode_en</a>	Binary Decoder with Enable
<a href="#">DW_thermdec</a>	Binary Thermometer Decoder and Enable
<b>Interface: Clock Domain Crossing</b> ( <a href="#">Overview</a> )	
<a href="#">DW_data_qsync_hl</a>	Quasi-Synchronous Data Interface for H-to-L Frequency Clocks
<a href="#">DW_data_qsync_lh</a>	Quasi-Synchronous Data Interface for L-to-H Frequency Clocks
<a href="#">DW_data_sync</a>	Data Bus Synchronizer with Acknowledge
<a href="#">DW_data_sync_na</a>	Data Bus Synchronizer without Acknowledge
<a href="#">DW_data_sync_1c</a>	Single Clock Filtered Data Bus Synchronizer
<a href="#">DW_fifo_2c_df</a>	Dual independent clock FIFO
<a href="#">DW_fifo_s2_sf</a>	Synchronous (Dual-Clock) FIFO with Static Flags
<a href="#">DW_fifoctrl_2c_df</a>	Family of FIFO Controllers with Dynamic Flags
<a href="#">DW_fifoctrl_s2_sf</a>	Synchronous (Dual-Clock) FIFO Controller with Static Flags
<a href="#">DW_gray_sync</a>	Gray Coded Synchronizer

**Table 1-3 List of DesignWare Building Block IP (Continued)**

IP	Description
<a href="#">DW_pulse_sync</a>	Dual Clock Pulse Synchronizer
<a href="#">DW_pulseack_sync</a>	Pulse Synchronizer with Acknowledge
<a href="#">DW_reset_sync</a>	Reset Sequence Synchronizer
<a href="#">DW_stream_sync</a>	Data Stream Synchronizer
<a href="#">DW_sync</a>	Single Clock Data Bus Synchronizer
<b>Logic: Combinational Components</b> ( <a href="#">Overview</a> )	
<a href="#">DW01_binenc</a>	Binary Encoder
<a href="#">DW01_bsh</a>	Barrel Shifter
<a href="#">DW01_decode</a>	Decoder
<a href="#">DW_lod</a>	Leading One's Detector
<a href="#">DW_lsd</a>	Leading Signs Detector
<a href="#">DW_lza</a>	Leading Zero's Anticipator
<a href="#">DW_lzd</a>	Leading Zero's Detector
<a href="#">DW01_mux_any</a>	Universal Multiplexer
<a href="#">DW_pricod</a>	Priority Coder
<a href="#">DW01_prienc</a>	Priority Encoder
<b>Logic: Sequential Components</b> ( <a href="#">Overview</a> )	
<a href="#">DW03_bictr_dcnto</a>	Up/Down Binary Counter with Dynamic Count-to Flag
<a href="#">DW03_bictr_scnto</a>	Up/Down Binary Counter with Static Count-to Flag
<a href="#">DW03_bictr_decode</a>	Up/Down Binary Counter with Output Decode
<a href="#">DW_dppll_sd</a>	Digital Phase Locked Loop
<a href="#">DW03_lfsr_dcnto</a>	LFSR Counter with Dynamic Count-to Flag
<a href="#">DW03_lfsr_scnto</a>	LFSR Counter with Static Count-to Flag
<a href="#">DW03_lfsr_load</a>	LFSR Counter with Loadable Input
<a href="#">DW03_lfsr_updn</a>	LFSR Up/Down Counter
<a href="#">DW03_updn_ctr</a>	Up/Down Counter

**Table 1-3 List of DesignWare Building Block IP (Continued)**

IP	Description
<b>Memory: FIFO (<a href="#">Overview</a>)</b>	
<a href="#">DW_asymdata_inbuf</a>	Asymmetric Data Input Buffer
<a href="#">DW_asymdata_outbuf</a>	Asymmetric Data Output Buffer
<a href="#">DW_asymfifo_s1_df</a>	Asymmetric I/O Synchronous (Single Clock) FIFO with Dynamic Flags
<a href="#">DW_asymfifo_s1_sf</a>	Asymmetric I/O Synchronous (Single Clock) FIFO with Static Flags
<a href="#">DW_asymfifo_s2_sf</a>	Asymmetric Synchronous (Dual-Clock) FIFO with Static Flags
<a href="#">DW_fifo_2c_df</a>	Dual independent clock FIFO
<a href="#">DW_fifo_s1_df</a>	Synchronous (Single Clock) FIFO with Dynamic Flags
<a href="#">DW_fifo_s1_sf</a>	Synchronous (Single Clock) FIFO with Static Flags
<a href="#">DW_fifo_s2_sf</a>	Synchronous (Dual-Clock) FIFO with Static Flags
<b>Memory: FIFO Controllers</b>	
<a href="#">DW_asymfifocntl_s1_df</a>	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Dynamic Flags
<a href="#">DW_asymfifocntl_s1_sf</a>	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Static Flags
<a href="#">DW_asymfifocntl_s2_sf</a>	Asymmetric Synchronous (Dual-Clock) FIFO Controller with Static Flags
<a href="#">DW_asymfifocntl_2c_df</a>	Asymmetric Dual-Clock FIFO Controller with Dynamic Flags
<a href="#">DW_fifocntl_2c_df</a>	Family of FIFO Controllers with Dynamic Flags
<a href="#">DW_fifocntl_s1_df</a>	Synchronous (Single Clock) FIFO Controller with Dynamic Flags
<a href="#">DW_fifocntl_s1_sf</a>	Synchronous (Single-Clock) FIFO Controller with Static Flags
<a href="#">DW_fifocntl_s2_sf</a>	Synchronous (Dual-Clock) FIFO Controller with Static Flags
<b>Memory: Registers (<a href="#">Overview</a>)</b>	
<a href="#">DW03_pipe_reg</a>	Pipeline Register
<a href="#">DW_pl_reg</a>	Pipeline Register
<a href="#">DW03_reg_s_pl</a>	Register with Synchronous Enable Reset
<a href="#">DW03_shftreg</a>	Shift Register
<a href="#">DW04_shad_reg</a>	Shadow and Multi-bit Register

**Table 1-3 List of DesignWare Building Block IP (Continued)**

IP	Description
<b>Memory: SRAMs</b>	
<a href="#">DW_ram_r_w_s_dff</a>	Synchronous Write-Port, Asynchronous Read-Port RAM (Flip-Flop-Based)
<a href="#">DW_ram_r_w_s_lat</a>	Synchronous Write-Port, Asynchronous Read-Port RAM (Latch-Based)
<a href="#">DW_ram_2r_w_s_dff</a>	Synchronous Write-Port, Async Dual Read-Port RAM (Flip-Flop-Based)
<a href="#">DW_ram_2r_w_s_lat</a>	Synchronous Write-Port, Async Dual Read-Port RAM (Latch-Based)
<a href="#">DW_ram_rw_s_dff</a>	Synchronous Single-Port, Read/Write RAM (Flip-Flop-Based)
<a href="#">DW_ram_rw_s_lat</a>	Synchronous Single-Port, Read/Write RAM (Latch-Based)
<a href="#">DW_ram_r_w_a_dff</a>	Asynchronous Dual-Port RAM (Flip-Flop-Based)
<a href="#">DW_ram_r_w_a_lat</a>	Asynchronous Dual-Port RAM (Latch-Based)
<a href="#">DW_ram_2r_w_a_dff</a>	Write-Port, Dual-Read-Port RAM (Flip-Flop-Based)
<a href="#">DW_ram_2r_w_a_lat</a>	Write-Port, Dual-Read-Port RAM (Latch-Based)
<a href="#">DW_ram_rw_a_dff</a>	Asynchronous Single-Port RAM (Flip-Flop-Based)
<a href="#">DW_ram_rw_a_lat</a>	Asynchronous Single-Port RAM (Latch-Based)
<b>Memory: Stacks</b>	
<a href="#">DW_stack</a>	Synchronous (Single-Clock) Stack
<a href="#">DW_stackctl</a>	Synchronous (Single Clock) Stack Controller
<b>Test: JTAG (<a href="#">Overview</a>)</b>	
<a href="#">DW_tap</a>	TAP Controller
<a href="#">DW_tap_uc</a>	TAP Controller with USERCODE Support
<a href="#">DW_bc_1</a>	Boundary Scan Cell Type BC_1
<a href="#">DW_bc_2</a>	Boundary Scan Cell Type BC_2
<a href="#">DW_bc_3</a>	Boundary Scan Cell Type BC_3
<a href="#">DW_bc_4</a>	Boundary Scan Cell Type BC_4
<a href="#">DW_bc_5</a>	Boundary Scan Cell Type BC_5
<a href="#">DW_bc_7</a>	Boundary Scan Cell Type BC_7
<a href="#">DW_bc_8</a>	Boundary Scan Cell Type BC_8
<a href="#">DW_bc_9</a>	Boundary Scan Cell Type BC_9
<a href="#">DW_bc_10</a>	Boundary Scan Cell Type BC_10

**Table 1-3 List of DesignWare Building Block IP (Continued)**

IP	Description
<b>Datapath Functions (<a href="#">Overview</a>)</b>	
<a href="#">DWF_dp_absval</a>	Returns the absolute value (magnitude) of an argument
<a href="#">DWF_dp_blend</a>	Implements an alpha blender or linear interpolator
<a href="#">DWF_dp_count_ones</a>	Performs ones count in argument
<a href="#">DWF_dp_rnd</a>	Performs arithmetic rounding
<a href="#">DWF_dp_rndsat</a>	Performs arithmetic rounding and saturation
<a href="#">DWF_dp_sat</a>	Performs arithmetic saturation
<a href="#">DWF_dp_sign_select</a>	Performs sign selection / conditional two's complement
<a href="#">DWF_dp_simd_add</a>	Implements SIMD adder
<a href="#">DWF_dp_simd_addc</a>	Implements SIMD adder with carry
<a href="#">DWF_dp_simd_mult</a>	Implements SIMD multiplier

## 1.6.2 Obsoleted IP for New Designs

For information on DesignWare Building Block IP that is in the process of being obsoleted, refer to “[Obsoleted IP for New Designs](#)” in the *[DesignWare Building Block IP Release Notes](#)*.