DesignWare

Building Block IP

Documentation Overview

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DesignWare Building Block IP Documentation Overview

DesignWare Building Block IP comprise a technology-independent, microarchitecture-level library that is tightly integrated into the Synopsys synthesis environment. This product was formally known as the DesignWare Foundation Library. A more complete introduction is available in *DesignWare Building Block IP Introduction*.

The following sections list the entire documentation set and datasheets that supports this library:

- "DesignWare Building Block IP Document List" on page 3
- "List of DesignWare Building Block IP" on page 5
- "Obsoleted IP for New Designs" on page 13
  Note: This information is now found in the Release Notes.

1.1 DesignWare Building Block IP Document List

Table 1-1 DesignWare Building Block IP Documentation

DesignWare Building Block IP Release Notes manuals/dwbb_relnotes.pdf	Contains usage issues for DesignWare Building Block IP Library components (F-2011.09) for Design Compiler DWBB_201012.5.
DesignWare IP Family Reference Guide manuals/dw_digital_ip_quickref.pdf	Provides general information for most DesignWare Synthesizable and Verification IP.
DesignWare Building Block Quick Reference manuals/dwbb_quickref.pdf	Provides a brief pin and parameter descriptions for all the DesignWare Building Block IP in a single document.
DesignWare Building Block IP QuickStart datasheets/dwbb_quickstart.pdf	Provides a quick look-up list of things you need to know to get started with the library of DesignWare Building Block IP.
Basic Library Components Overview datasheets/dwbb_basiclib.pdf	Describes the Basic Library components, which provide basic implementations of common arithmetic functions that can be referenced by HDL operators in your VHDL or Verilog source code.
DesignWare Building Block IP User Guide manuals/dwbb_userguide.pdf	Explains the use of DesignWare Building Block IP.
DesignWare Building Block IP Application Notes manuals/dwbb_appnotes.pdf	A complete compilation of Application Notes that support the DesignWare Building Block IP.

Table 1-1 DesignWare Building Block IP Documentation (Continued)

DesignWare Building Block IP Developer Guide manuals/dwdg.pdf	This manual is for silicon suppliers, systems companies, and third party macro and model development houses who want to develop technology-specific designs or proprietary DesignWare components.
Designware GTECH Library Databook manuals/dw_gtech.pdf	Provides detailed datasheets for the GTECH Library components.

1.2 DesignWare minPower Components Documentation

NOTE: DesignWare minPower Components documentation is available on the Synopsys website, and requires access authentication.

Table 1-2 DesignWare minPower Components Documentation

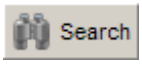
DesignWare minPower Components Documentation Overview https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_overview.pdf	Lists the minPower Components documentation, which provide Low Power implementations of common arithmetic functions.
DesignWare minPower Components DC Release Notes https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_relnotes.pdf	Contains usage issues for DesignWare minPower Components (F-2011.09) for Design Compiler DWBB_201012.5.
DesignWare minPower Components User Guide https://www.synopsys.com/dw/doc.php/doc/dwmp/manuals/minpower_userguide.pdf	Explains the use of DesignWare minPower Components.
DesignWare minPower Components Overview https://www.synopsys.com/dw/doc.php/doc/dwmp/datasheets/minpower_overview.pdf	A listing and brief description of the DesignWare minPower Components. Use this document to access minPower Component datasheets.

1.3 Synopsys Common Licensing (SCL)

You can find general SCL information on the following page:

http://www.synopsys.com/keys

1.4 Searching PDF Files



You can search for a text string within a single PDF document or entire document set using the Search feature of Adobe Reader (formerly Acrobat Reader).

You can search equally well through an individual PDF file located on a web server or on your local file system; however, in order to search through a collection of PDF files, those files must reside on your local file system.

In addition, many collections of PDF files provided by Synopsys are preconfigured with a search index file called INDEX.PDX, which enables even faster search operations. If an INDEX.PDX file is available, the Adobe Reader locates the file automatically for use in the next search operation.

1.5 For More Information About Adobe Reader

For more information about using Adobe Reader, refer to the online guide:

Help > Adobe Reader Help

You can also get useful information and download the most recent version of the Reader from the Adobe website:

http://www.adobe.com

1.6 Additional Information

For additional Synopsys documentation, refer to the following location:

http://www.synopsys.com/products/designware/docs

For up-to-date information about the latest verification models and synthesizable IP available from Synopsys, visit the IP Directory:

http://www.synopsys.com/products/designware/ipdir

1.6.1 List of DesignWare Building Block IP

The following table provides links to each datasheet. New IP (2010.12 and later) are indicated with a New label; updates to existing IP with the Updated label. IP that are obsolete for new designs are listed on page 13.

Table 1-3 List of DesignWare Building Block IP

IP	Description
Application Specific: Control Logic (Overview)	
DW_arb_2t	Two-Tier Arbiter with Dynamic/Fair-Among-Equal Scheme
DW_arb_dp	Arbiter with Dynamic Priority Scheme

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Description
DW_arb_fcfs	Arbiter with First-Come-First-Served Priority Scheme
DW_arb_rr	Arbiter with Round Robin Priority Scheme
DW_arb_sp	Arbiter with Static Priority Scheme
Datapath: Arithmetic Components (Overview)	
DW01_absval	Absolute Value
DW01_add	Adder
DW01_addsub	Adder-Subtractor
DW_addsub_dx	Duplex Adder/Subtractor with Saturation and Rounding
DW01_ash	Arithmetic Shifter
DW_bin2gray	Binary to Gray Converter
DW01_bsh	Barrel Shifter
DW01_cmp2	2-Function Comparator
DW01_cmp6	6-Function Comparator
DW_cmp_dx	Duplex Comparator
DW_cntr_gray	Gray Code Counter
DW01_csa	Carry Save Adder
DW01_dec	Decrementer
DW_div	Combinational Divider
DW_div_pipe	Stallable Pipelined Divider
DW_exp2	Base 2 Exponential (2a) (datasheet updated)
DW_gray2bin	Gray to Binary Converter
DW01_inc	Incrementer
DW01_incdec	Incrementer-Decrementer
DW_inc_gray	Gray Incrementer
DW_inv_sqrt	Reciprocal of Square-Root (datasheet updated)
DW_lbsh	Barrel Shifter with Preferred Left Direction
DW_ln	Natural Logarithm (ln(a))
DW_log2	Base 2 Logarithm ($\log_2$(a)) (datasheet updated)
DW02_mac	Multiplier-Accumulator
DW_minmax	Minimum/Maximum Value

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Description
DW02_mult	Multiplier
DW02_multp	Partial Product Multiplier
DW02_mult_2_stage	Two-Stage Pipelined Multiplier
DW02_mult_3_stage	Three-Stage Pipelined Multiplier
DW02_mult_4_stage	Four-Stage Pipelined Multiplier
DW02_mult_5_stage	Five-Stage Pipelined Multiplier
DW02_mult_6_stage	Six-Stage Pipelined Multiplier
DW_mult_dx	Duplex Multiplier
DW_mult_pipe	Stallable Pipelined Multiplier
DW_norm	Normalization for Fractional Input
DW_norm_rnd	Normalization and Rounding
DW_piped_mac	Pipelined Multiplier-Accumulator
DW02_prod_sum	Generalized Sum of Products
DW02_prod_sum1	Multiplier-Adder
DW_prod_sum_pipe	Stallable Pipelined Generalized Sum of Products
DW_rash	Arithmetic Shifter with Preferred Right Direction
DW_rbsh	Barrel Shifter with Preferred Right Direction
DW01_satrnd	Arithmetic Saturation and Rounding Logic
DW_shifter	Combined Arithmetic and Barrel Shifter
DW_sla	Arithmetic Shifter with Preferred Left Direction (VHDL style)
DW_sra	Arithmetic Shifter with Preferred Right Direction (VHDL style)
DW_square	Integer Squarer
DW_squarep	Partial Product Integer Squarer
DW_sqrt	Combinational Square Root (datasheet updated)
DW_sqrt_pipe	Stallable Pipelined Square Root
DW01_sub	Subtractor
DW02_sum	Vector Adder
DW02_tree	Wallace Tree Compressor

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Description
Datapath: Floating Point (Overview)	
DW_fp_add	Floating Point Adder
DW_fp_addsub	Floating Point Adder/Subtractor
DW_fp_cmp	Floating Point Comparator
DW_fp_div	Floating Point Divider
DW_fp_div_seq	Floating Point Sequential Divider
DW_fp_dp2	2-Term Floating Point Dot-product
DW_fp_dp3	3-Term Floating Point Dot-product
DW_fp_dp4	4-Term Floating Point Dot-product
DW_fp_exp	Floating Point Exponential (e^a)
DW_fp_exp2	Floating Point Base-2 Exponential (2^a) (datasheet updated)
DW_fp_flt2i	Floating Point to Integer Converter
DW_fp_i2flt	Integer to Floating Point Converter
DW_fp_invsqrt	Floating Point Reciprocal of Square Root (datasheet updated)
DW_fp_ln	Floating Point Natural Logarithm (ln(a))
DW_fp_log2	Floating Point Base 2 Logarithm ($\log_2(a)$) (datasheet updated)
DW_fp_mac	Floating Point Multiply-and-Add
DW_fp_mult	Floating Point Multiplier
DW_fp_recip	Floating Point Reciprocal (1/a) (datasheet updated)
DW_fp_sincos	Floating Point Sine and Cosine (datasheet updated)
DW_fp_sqrt	Floating Point Square Root (datasheet updated)
DW_fp_square	Floating Point Square
DW_fp_sub	Floating Point Subtractor
DW_fp_sum3	3-input Floating Point Adder
DW_fp_sum4	4-input Floating Point Adder
Datapath: Sequential (Overview)	
DW_div_seq	Sequential Divider
DW_fp_div_seq	Floating Point Sequential Divider
DW_mult_seq	Sequential Multiplier
DW_sqrt_seq	Sequential Square Root

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Description
Datapath: Trigonometric (Overview)	
DW_sincos	Combinational Sine - Cosine (datasheet updated)
Data Integrity (Overview)	
DW_crc_p	Universal Parallel (Combinational) CRC Generator/Checker
DW_crc_s	Universal Synchronous (Clocked) CRC Generator/Checker
DW_ecc	Error Checking and Correction
DW04_par_gen	Parity Generator and Checker
Data Integrity: Coding (Overview)	
DW_8b10b_dec	8b10b Decoder
DW_8b10b_enc	8b10b Encoder
DW_8b10b_unbal	8b10b Coding Balance Predictor
Digital Signal Processing (DSP)	
DW_fir	High-Speed Digital FIR Filter
DW_fir_seq	Sequential Digital FIR Filter Processor
DW_iir_dc	High-Speed Digital IIR Filter with Dynamic Coefficients
DW_iir_sc	High-Speed Digital IIR Filter with Static Coefficients
DW_dct_2d	Two Dimensional Discreet Cosine Transform
DW_decode_en	Binary Decoder with Enable
DW_thermdec	Binary Thermometer Decoder and Enable
Interface: Clock Domain Crossing (Overview)	
DW_data_qsync_hl	Quasi-Synchronous Data Interface for H-to-L Frequency Clocks
DW_data_qsync_lh	Quasi-Synchronous Data Interface for L-to-H Frequency Clocks
DW_data_sync	Data Bus Synchronizer with Acknowledge
DW_data_sync_na	Data Bus Synchronizer without Acknowledge
DW_data_sync_1c	Single Clock Filtered Data Bus Synchronizer
DW_fifo_2c_df	Dual independent clock FIFO
DW_fifo_s2_sf	Synchronous (Dual-Clock) FIFO with Static Flags
DW_fifoctl_2c_df	Family of FIFO Controllers with Dynamic Flags
DW_fifoctl_s2_sf	Synchronous (Dual-Clock) FIFO Controller with Static Flags
DW_gray_sync	Gray Coded Synchronizer

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Description
DW_pulse_sync	Dual Clock Pulse Synchronizer
DW_pulseack_sync	Pulse Synchronizer with Acknowledge
DW_reset_sync	Reset Sequence Synchronizer
DW_stream_sync	Data Stream Synchronizer
DW_sync	Single Clock Data Bus Synchronizer
Logic: Combinational Components (Overview)	
DW01_binenc	Binary Encoder
DW01_bsh	Barrel Shifter
DW01_decode	Decoder
DW_lod	Leading One's Detector
DW_lsd	Leading Signs Detector
DW_lza	Leading Zero's Anticipator
DW_lzd	Leading Zero's Detector
DW01_mux_any	Universal Multiplexer
DW_pricod	Priority Coder
DW01_prienc	Priority Encoder
Logic: Sequential Components (Overview)	
DW03_bictr_dcnto	Up/Down Binary Counter with Dynamic Count-to Flag
DW03_bictr_scnto	Up/Down Binary Counter with Static Count-to Flag
DW03_bictr_decode	Up/Down Binary Counter with Output Decode
DW_dpll_sd	Digital Phase Locked Loop
DW03_lfsr_dcnto	LFSR Counter with Dynamic Count-to Flag
DW03_lfsr_scnto	LFSR Counter with Static Count-to Flag
DW03_lfsr_load	LFSR Counter with Loadable Input
DW03_lfsr_updn	LFSR Up/Down Counter
DW03_updn_ctr	Up/Down Counter

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Description
Memory: FIFO (Overview)	
DW_asymdata_inbuf	Asymmetric Data Input Buffer
DW_asymdata_outbuf	Asymmetric Data Output Buffer
DW_asymfifo_s1_df	Asymmetric I/O Synchronous (Single Clock) FIFO with Dynamic Flags
DW_asymfifo_s1_sf	Asymmetric I/O Synchronous (Single Clock) FIFO with Static Flags
DW_asymfifo_s2_sf	Asymmetric Synchronous (Dual-Clock) FIFO with Static Flags
DW_fifo_2c_df	Dual independent clock FIFO
DW_fifo_s1_df	Synchronous (Single Clock) FIFO with Dynamic Flags
DW_fifo_s1_sf	Synchronous (Single Clock) FIFO with Static Flags
DW_fifo_s2_sf	Synchronous (Dual-Clock) FIFO with Static Flags
Memory: FIFO Controllers	
DW_asymfifoctl_s1_df	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Dynamic Flags
DW_asymfifoctl_s1_sf	Asymmetric I/O Synchronous (Single Clock) FIFO Controller with Static Flags
DW_asymfifoctl_s2_sf	Asymmetric Synchronous (Dual-Clock) FIFO Controller with Static Flags
DW_asymfifoctl_2c_df	Asymmetric Dual-Clock FIFO Controller with Dynamic Flags
DW_fifoctl_2c_df	Family of FIFO Controllers with Dynamic Flags
DW_fifoctl_s1_df	Synchronous (Single Clock) FIFO Controller with Dynamic Flags
DW_fifoctl_s1_sf	Synchronous (Single-Clock) FIFO Controller with Static Flags
DW_fifoctl_s2_sf	Synchronous (Dual-Clock) FIFO Controller with Static Flags
Memory: Registers (Overview)	
DW03_pipe_reg	Pipeline Register
DW_pl_reg	Pipeline Register
DW03_reg_s_pl	Register with Synchronous Enable Reset
DW03_shftreg	Shift Register
DW04_shad_reg	Shadow and Multi-bit Register

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Description
Memory: SRAMs	
DW_ram_r_w_s_dff	Synchronous Write-Port, Asynchronous Read-Port RAM (Flip-Flop-Based)
DW_ram_r_w_s_lat	Synchronous Write-Port, Asynchronous Read-Port RAM (Latch-Based)
DW_ram_2r_w_s_dff	Synchronous Write-Port, Async Dual Read-Port RAM (Flip-Flop-Based)
DW_ram_2r_w_s_lat	Synchronous Write-Port, Async Dual Read-Port RAM (Latch-Based)
DW_ram_rw_s_dff	Synchronous Single-Port, Read/Write RAM (Flip-Flop-Based)
DW_ram_rw_s_lat	Synchronous Single-Port, Read/Write RAM (Latch-Based)
DW_ram_r_w_a_dff	Asynchronous Dual-Port RAM (Flip-Flop-Based)
DW_ram_r_w_a_lat	Asynchronous Dual-Port RAM (Latch-Based)
DW_ram_2r_w_a_dff	Write-Port, Dual-Read-Port RAM (Flip-Flop-Based)
DW_ram_2r_w_a_lat	Write-Port, Dual-Read-Port RAM (Latch-Based)
DW_ram_rw_a_dff	Asynchronous Single-Port RAM (Flip-Flop-Based)
DW_ram_rw_a_lat	Asynchronous Single-Port RAM (Latch-Based)
Memory: Stacks	
DW_stack	Synchronous (Single-Clock) Stack
DW_stackctl	Synchronous (Single Clock) Stack Controller
Test: JTAG (Overview)	
DW_tap	TAP Controller
DW_tap_uc	TAP Controller with USERCODE Support
DW_bc_1	Boundary Scan Cell Type BC_1
DW_bc_2	Boundary Scan Cell Type BC_2
DW_bc_3	Boundary Scan Cell Type BC_3
DW_bc_4	Boundary Scan Cell Type BC_4
DW_bc_5	Boundary Scan Cell Type BC_5
DW_bc_7	Boundary Scan Cell Type BC_7
DW_bc_8	Boundary Scan Cell Type BC_8
DW_bc_9	Boundary Scan Cell Type BC_9
DW_bc_10	Boundary Scan Cell Type BC_10

Table 1-3 List of DesignWare Building Block IP (Continued)

IP	Description
Datapath Functions (Overview)	
DWF_dp_absval	Returns the absolute value (magnitude) of an argument
DWF_dp_blend	Implements an alpha blender or linear interpolator
DWF_dp_count_ones	Performs ones count in argument
DWF_dp_rnd	Performs arithmetic rounding
DWF_dp_rndsat	Performs arithmetic rounding and saturation
DWF_dp_sat	Performs arithmetic saturation
DWF_dp_sign_select	Performs sign selection / conditional two's complement
DWF_dp_simd_add	Implements SIMD adder
DWF_dp_simd_addc	Implements SIMD adder with carry
DWF_dp_simd_mult	Implements SIMD multiplier

1.6.2 Obsoleted IP for New Designs

For information on DesignWare Building Block IP that is in the process of being obsoleted, refer to "Obsoleted IP for New Designs" in the *DesignWare Building Block IP Release Notes*.