```verilog
 1   `timescale 1ns / 1ps
 2   //////////////////////////////////////////////////////////////////////////////////
 3   // Company:
 4   // Engineer:
 5   //
 6   // Create Date: 03/18/2016 03:28:31 PM
 7   // Design Name:
 8   // Module Name: Round_Sgf_Dec
 9   // Project Name:
10   // Target Devices:
11   // Tool Versions:
12   // Description:
13   //
14   // Dep encies:
15   //
16   // Revision:
17   // Revision 0.01 - File Created
18   // Additional Comments:
19   //
20   //////////////////////////////////////////////////////////////////////////////////
21
22
23   module Round_Sgf_Dec(
24       input wire clk,
25       input wire [1:0] Data_i,
26       input wire [1:0] Round_Type_i,
27       input wire Sign_Result_i,
28       output reg Round_Flag_o
29       );
30
31       always @*
32           case ({Sign_Result_i,Round_Type_i,Data_i})
33           //Round type=00; Towards zero / No round
34           //Round type=01; Towards - infinity
35           //Round type=10; Towards + infinity
36
37
38           //Op=0;Round type=00
39
40           /*5'b00000: Round_Flag_o <=0;
41           5'b00001: Round_Flag_o <=0;
42           5'b00010: Round_Flag_o <=0;
43           5'b00011: Round_Flag_o <=0;*/
44
45           //Op=1;Round type=00
46
47           /*5'b10000: Round_Flag_o <=0;
48           5'b10001: Round_Flag_o <=0;
49           5'b10010: Round_Flag_o <=0;
50           5'b10011: Round_Flag_o <=0;   */
51
52           //Op=0;Round type=01
53
```

```verilog
54          /*5'b00100: Round_Flag_o <=0;
55          5'b00101: Round_Flag_o <=0;
56          5'b00110: Round_Flag_o <=0;
57          5'b00111: Round_Flag_o <=0;   */

59          //Op=1;Round type=01

61          //5'b10100: Round_Flag_o <=0;
62          5'b10101: Round_Flag_o <=1;
63          5'b10110: Round_Flag_o <=1;
64          5'b10111: Round_Flag_o <=1;

66          //Op=0;Round type=10

68          //5'b01000: Round_Flag_o <=0;
69          5'b01001: Round_Flag_o <=1;
70          5'b01010: Round_Flag_o <=1;
71          5'b01011: Round_Flag_o <=1;


74          //Op=1;Round type=10

76          /*5'b11000: Round_Flag_o <=0;
77          5'b11001: Round_Flag_o <=0;
78          5'b11010: Round_Flag_o <=0;
79          5'b11011: Round_Flag_o <=0;   */

81          default: Round_Flag_o <=0;

83          endcase

85      endmodule
86
```