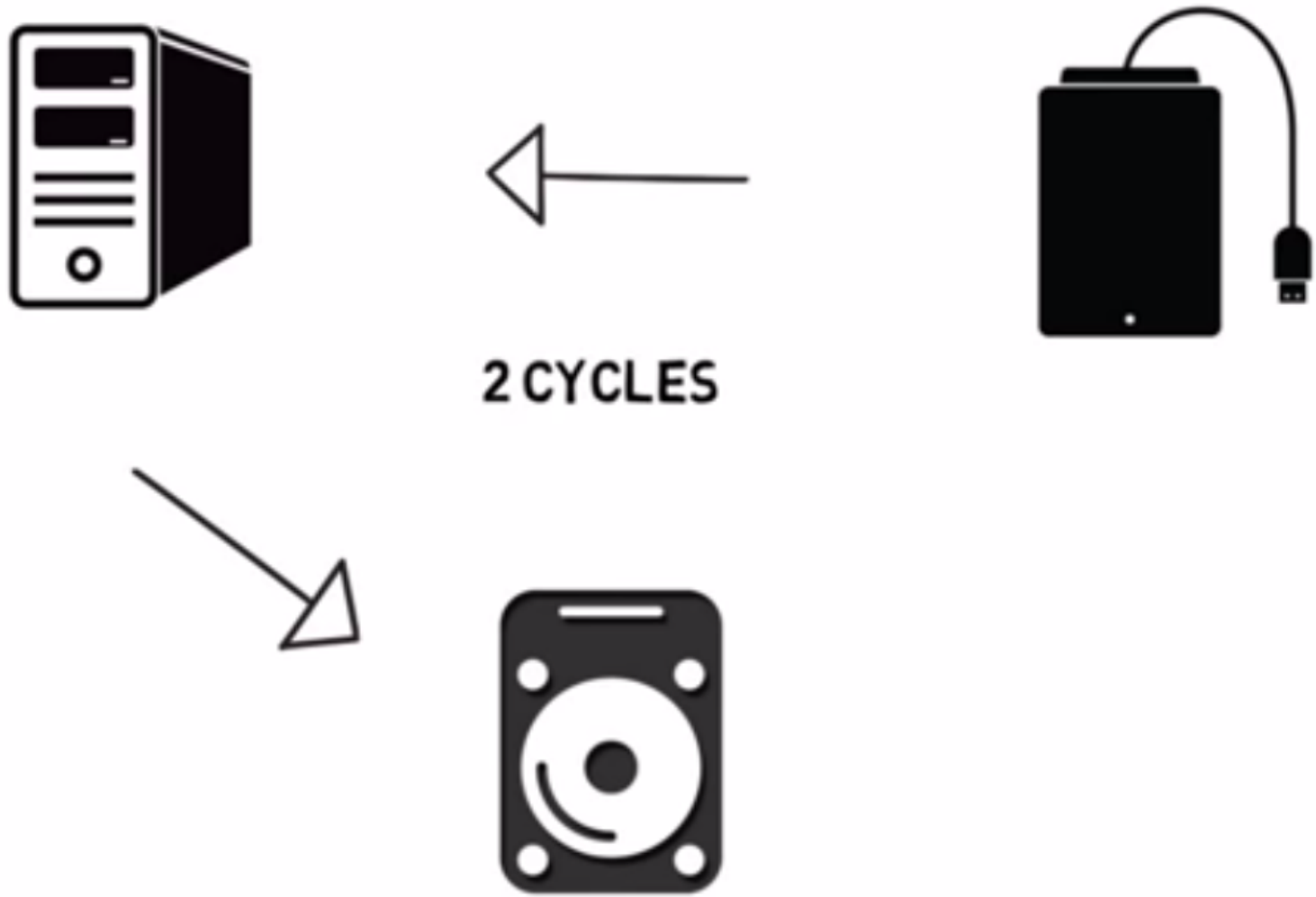
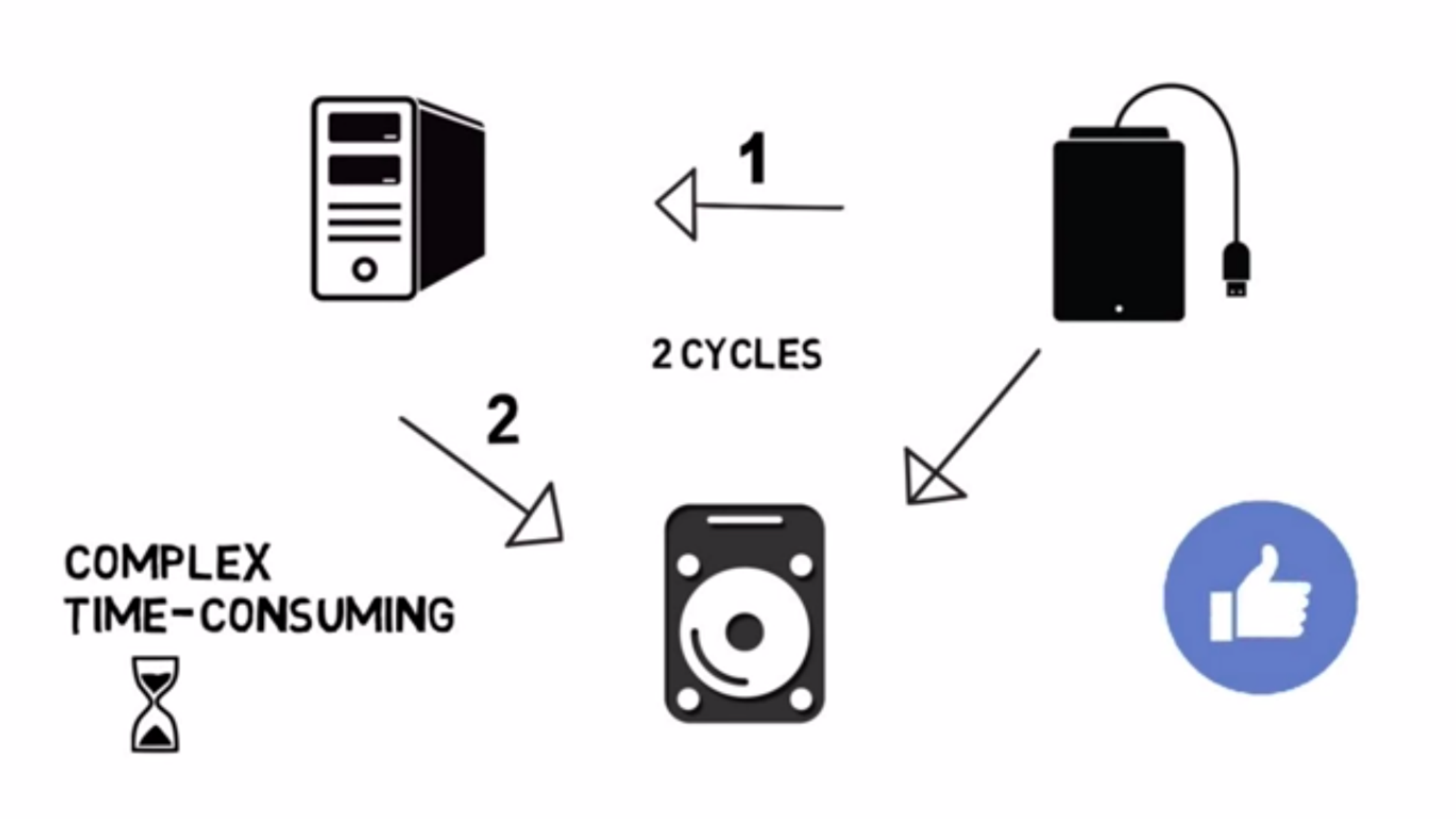
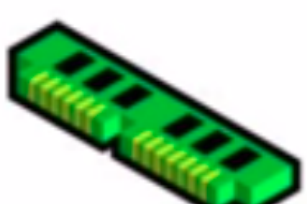

2 CYCLES


1
2 CYCLES
2
COMPLEX
TIME-CONSUMING

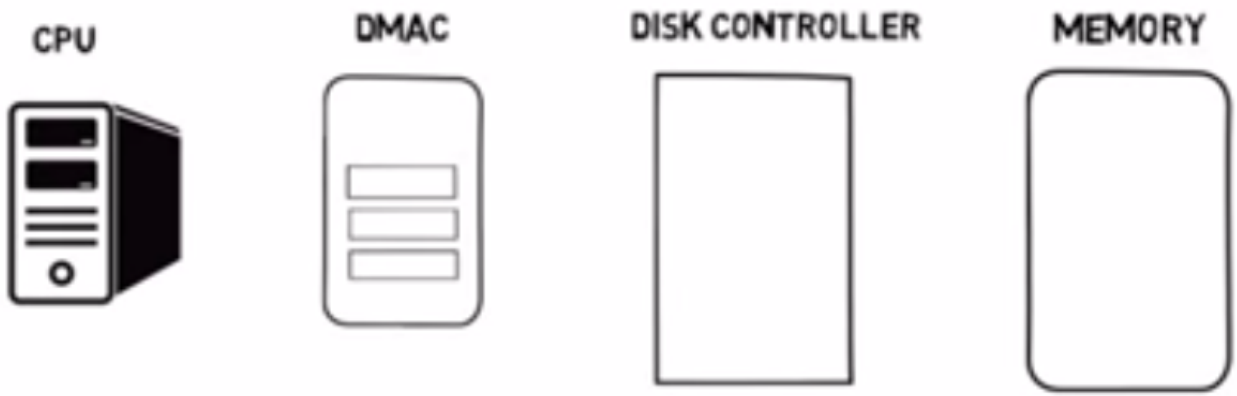
DMA

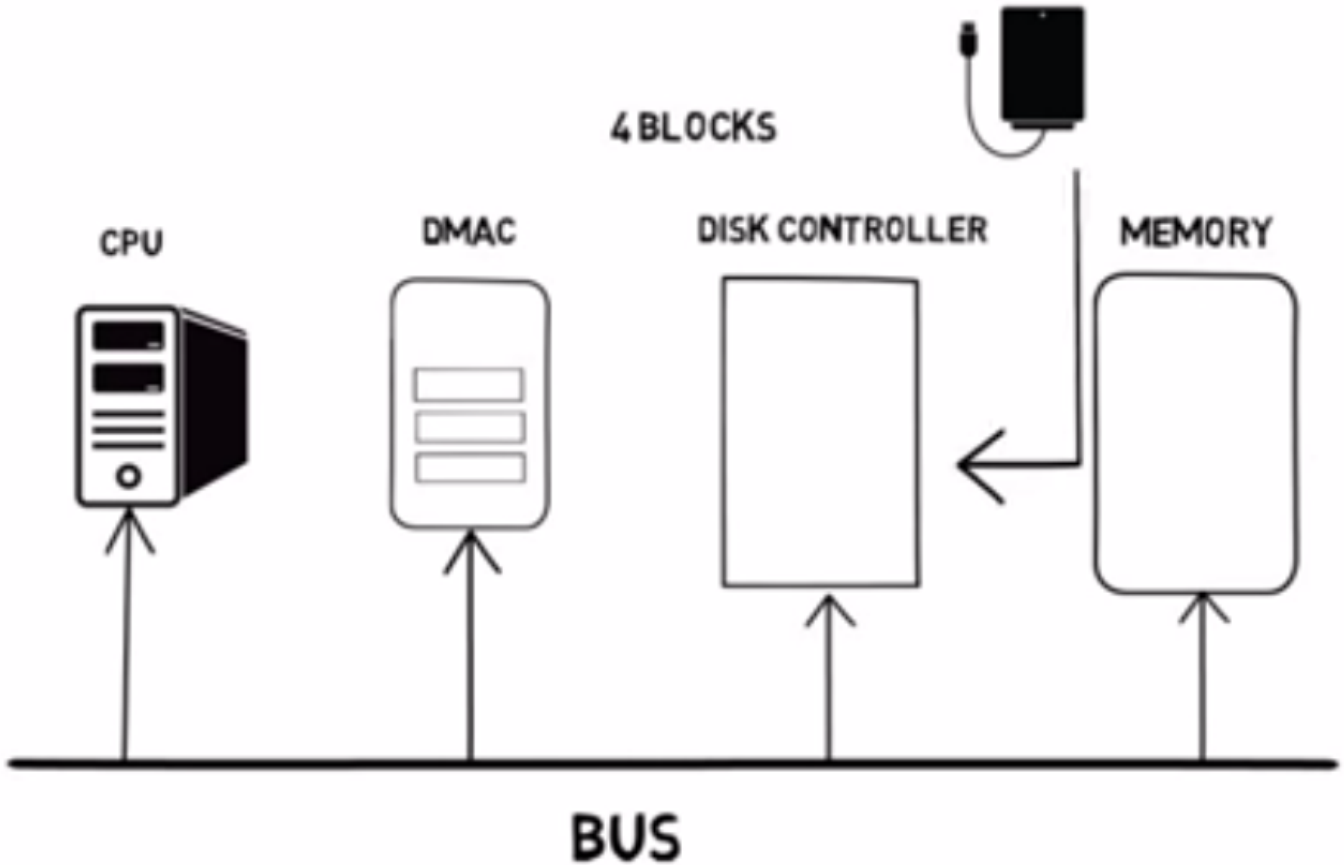
DMA CONTROLLER

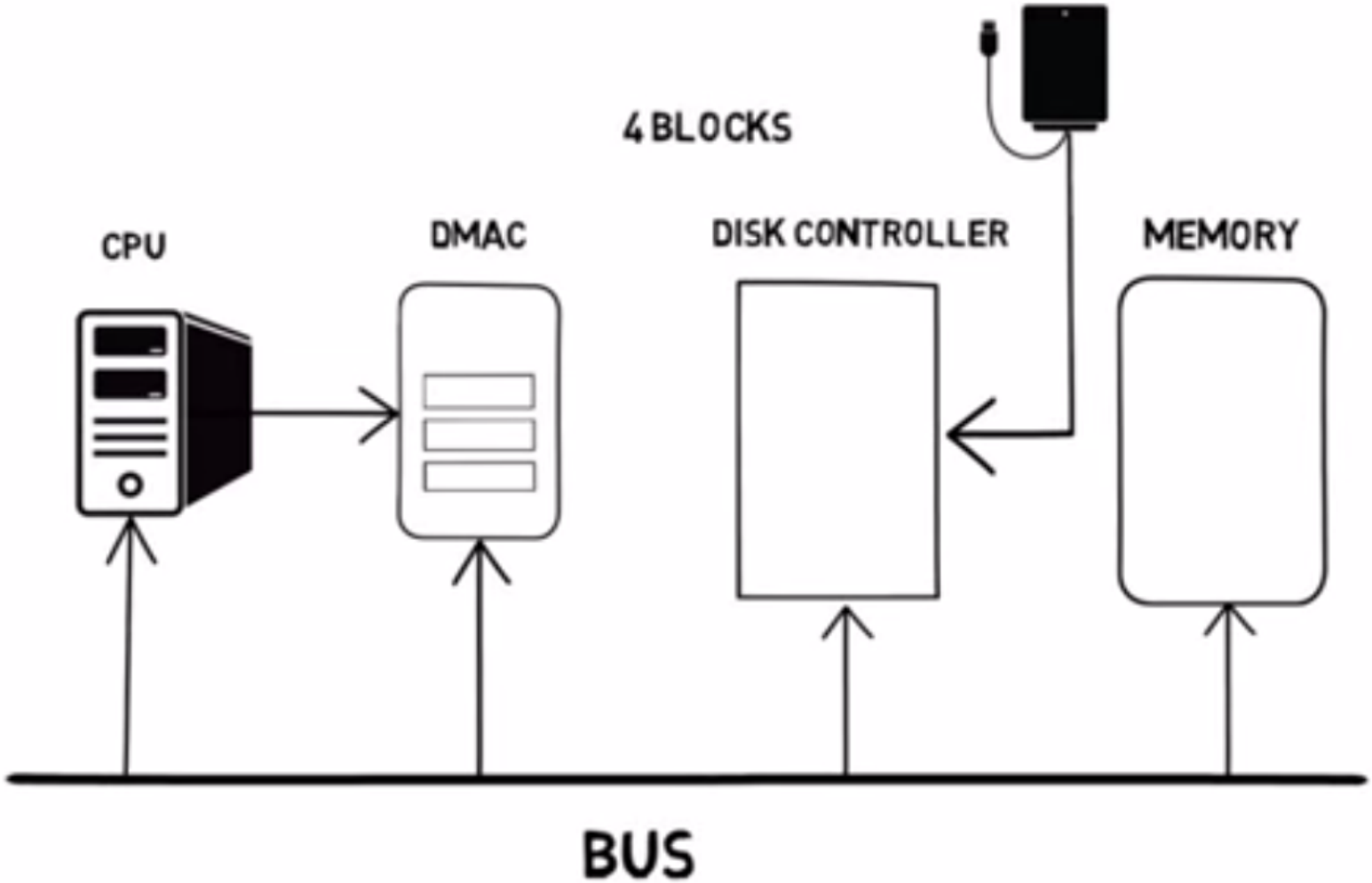
(DMAC)

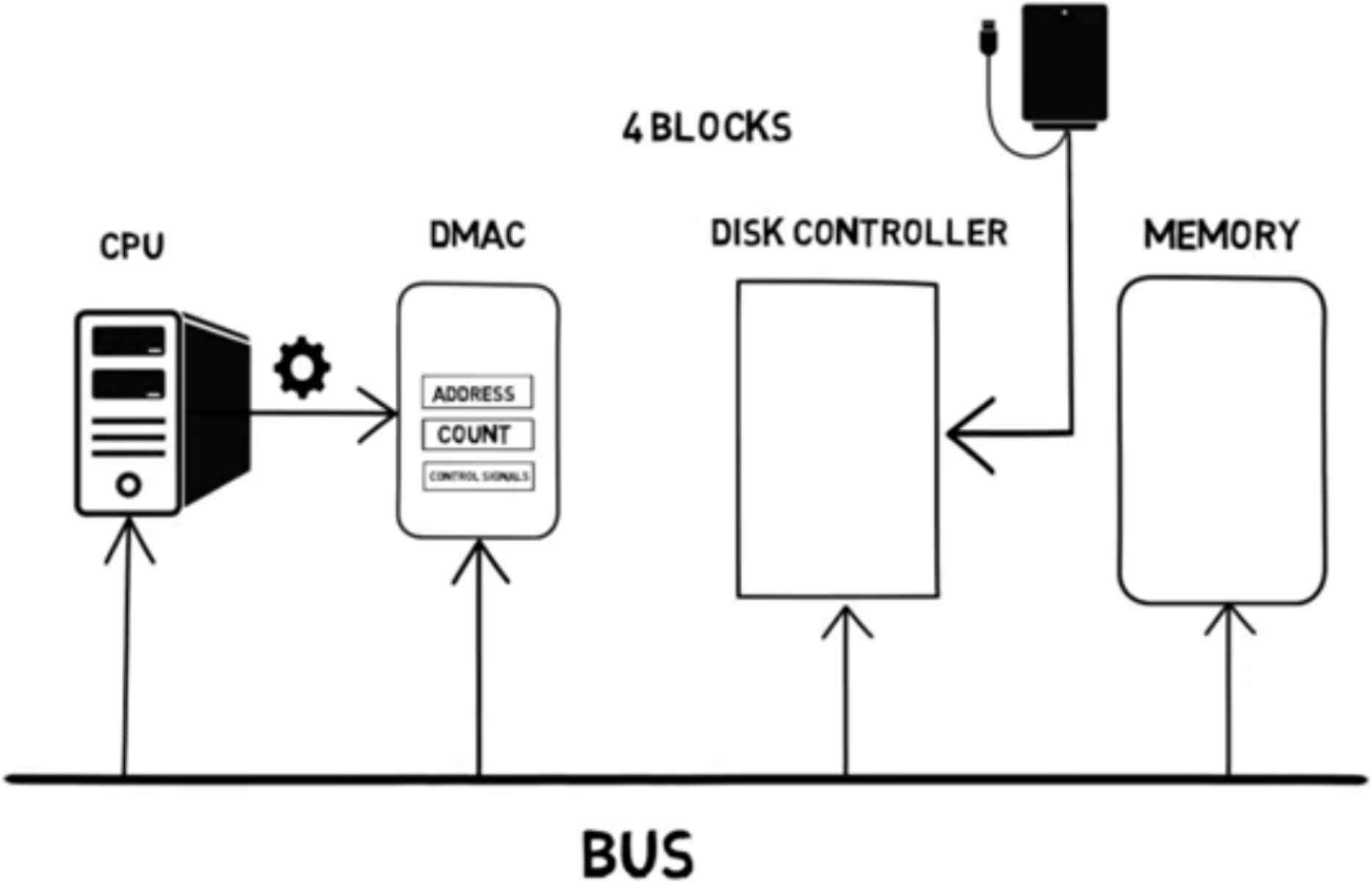


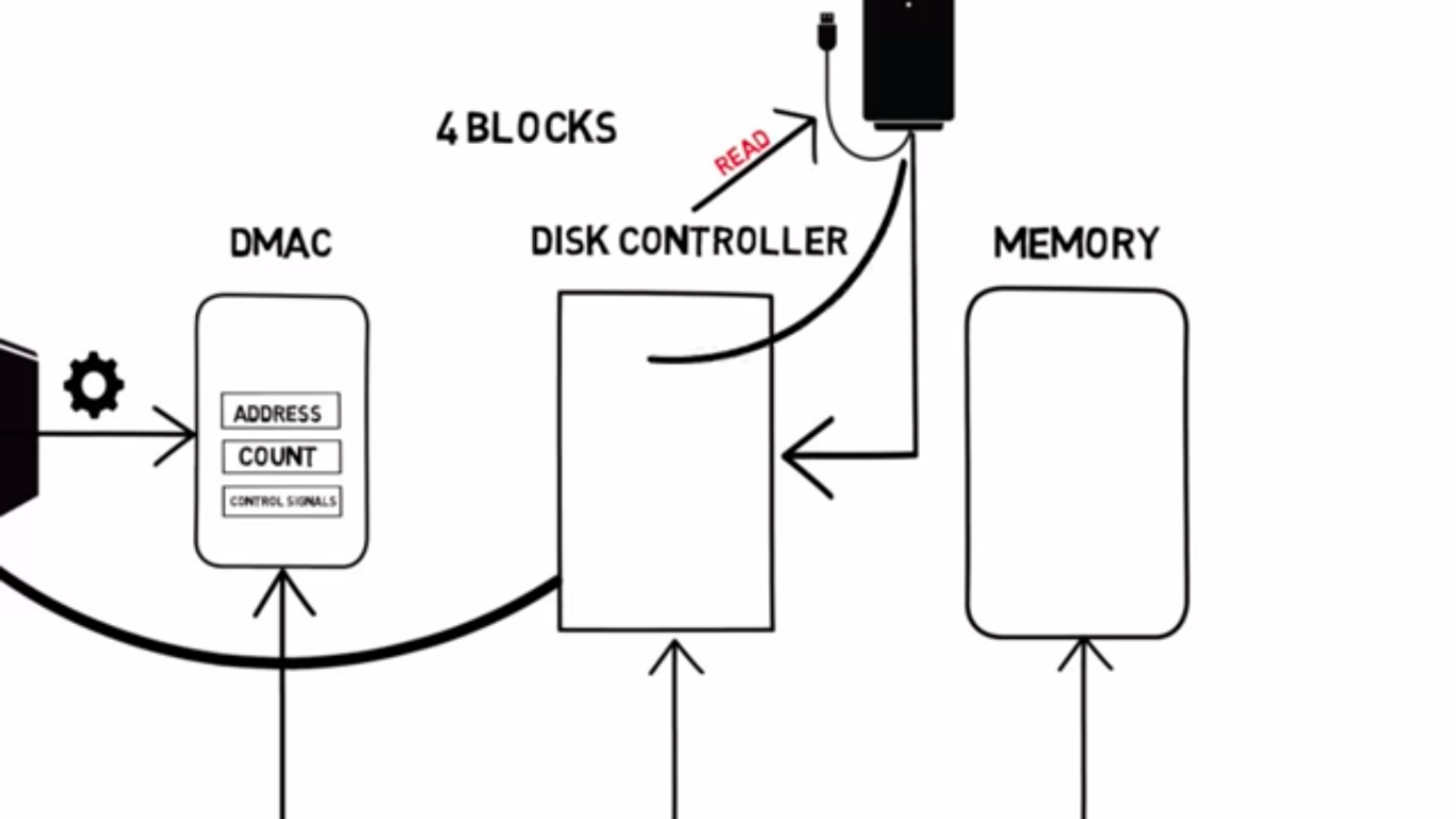
4 BLOCKS

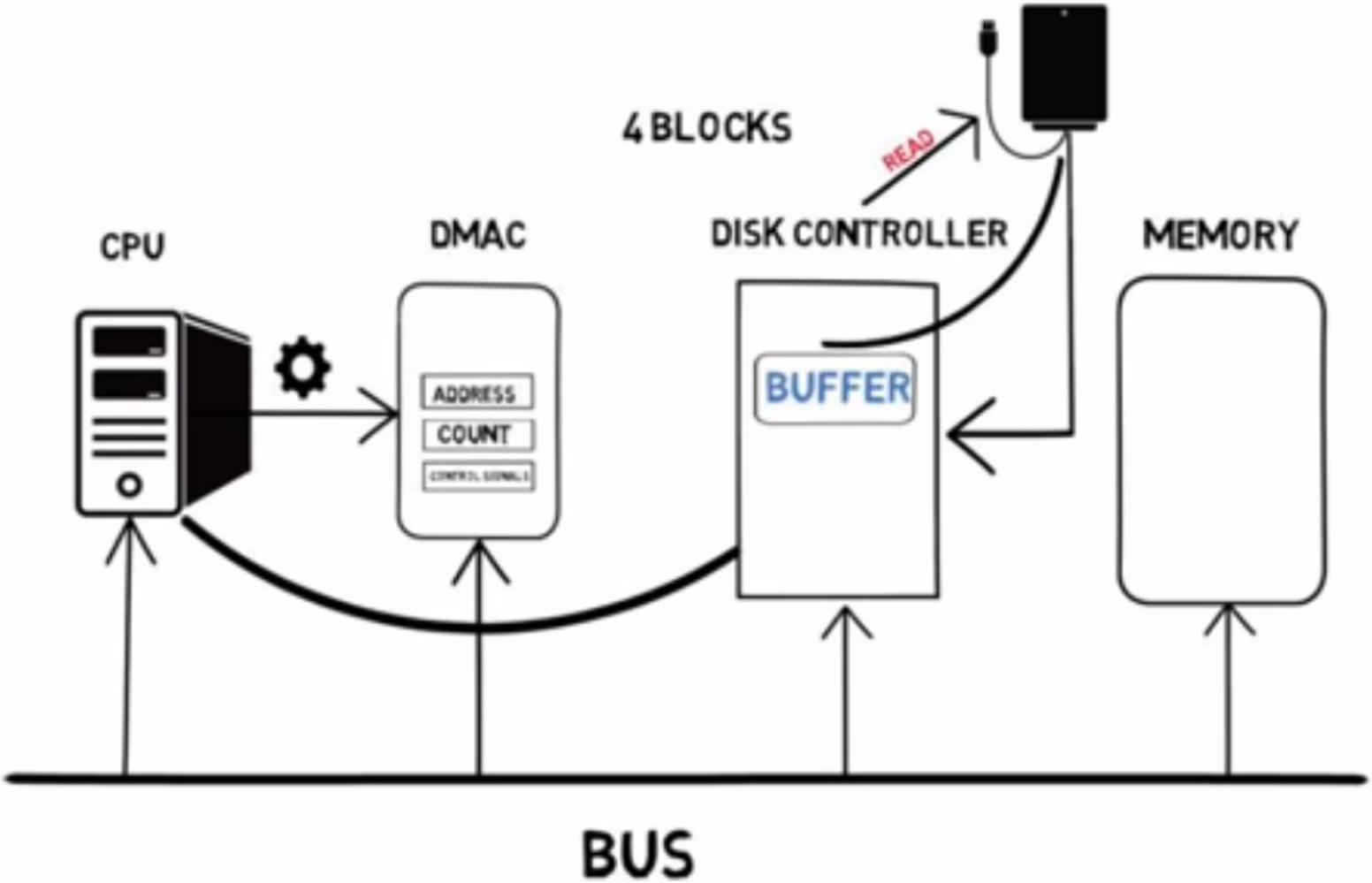


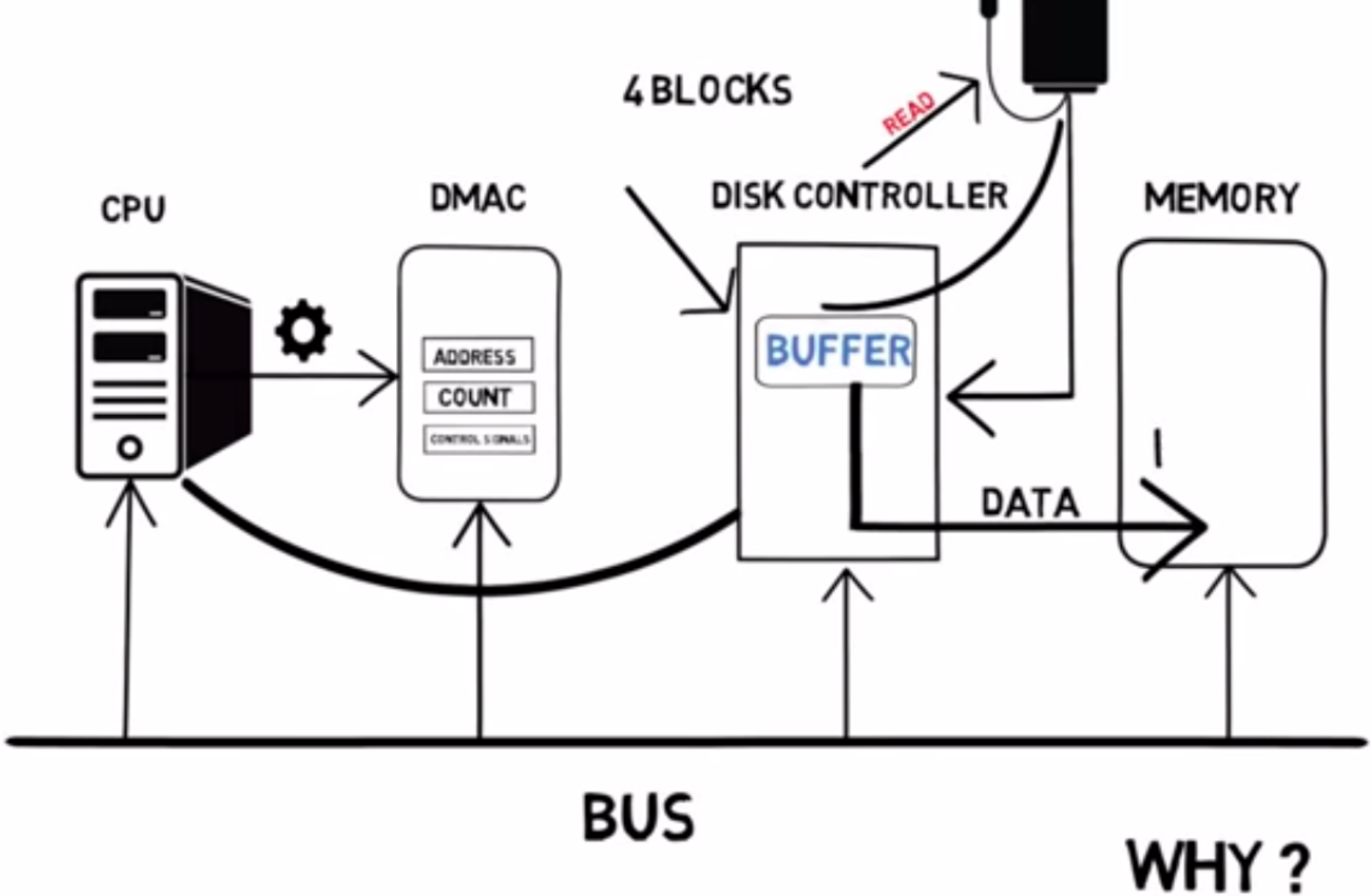

4 BLOCKS
CPU
DMAC
DISK CONTROLLER
MEMORY
BUS

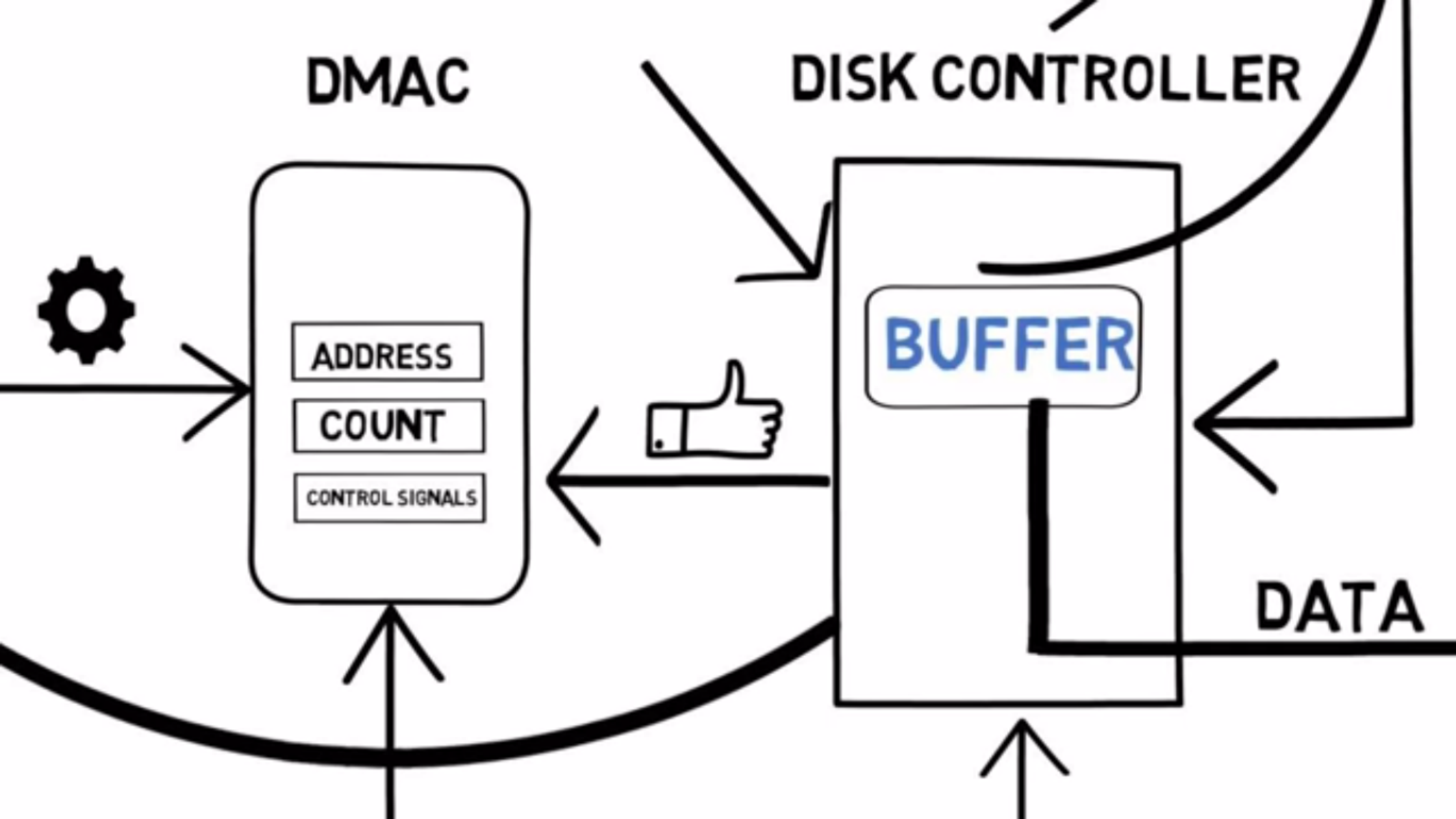

4 BLOCKS
CPU
DMAC
DISK CONTROLLER
MEMORY
BUS

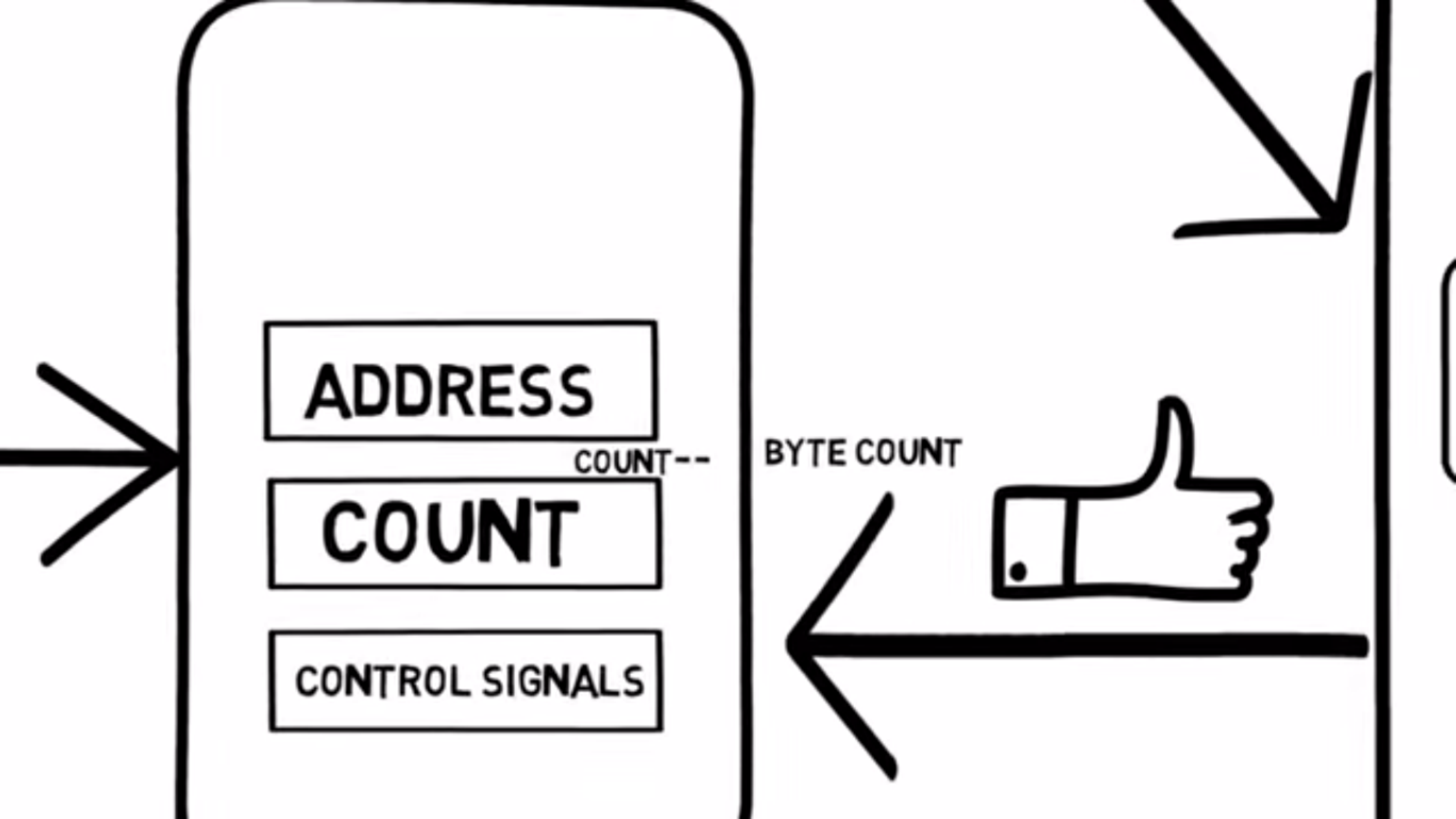

4 BLOCKS
CPU
DMAC
DISK CONTROLLER
MEMORY
ADDRESS
COUNT
CONTROL SIGNALS
BUS

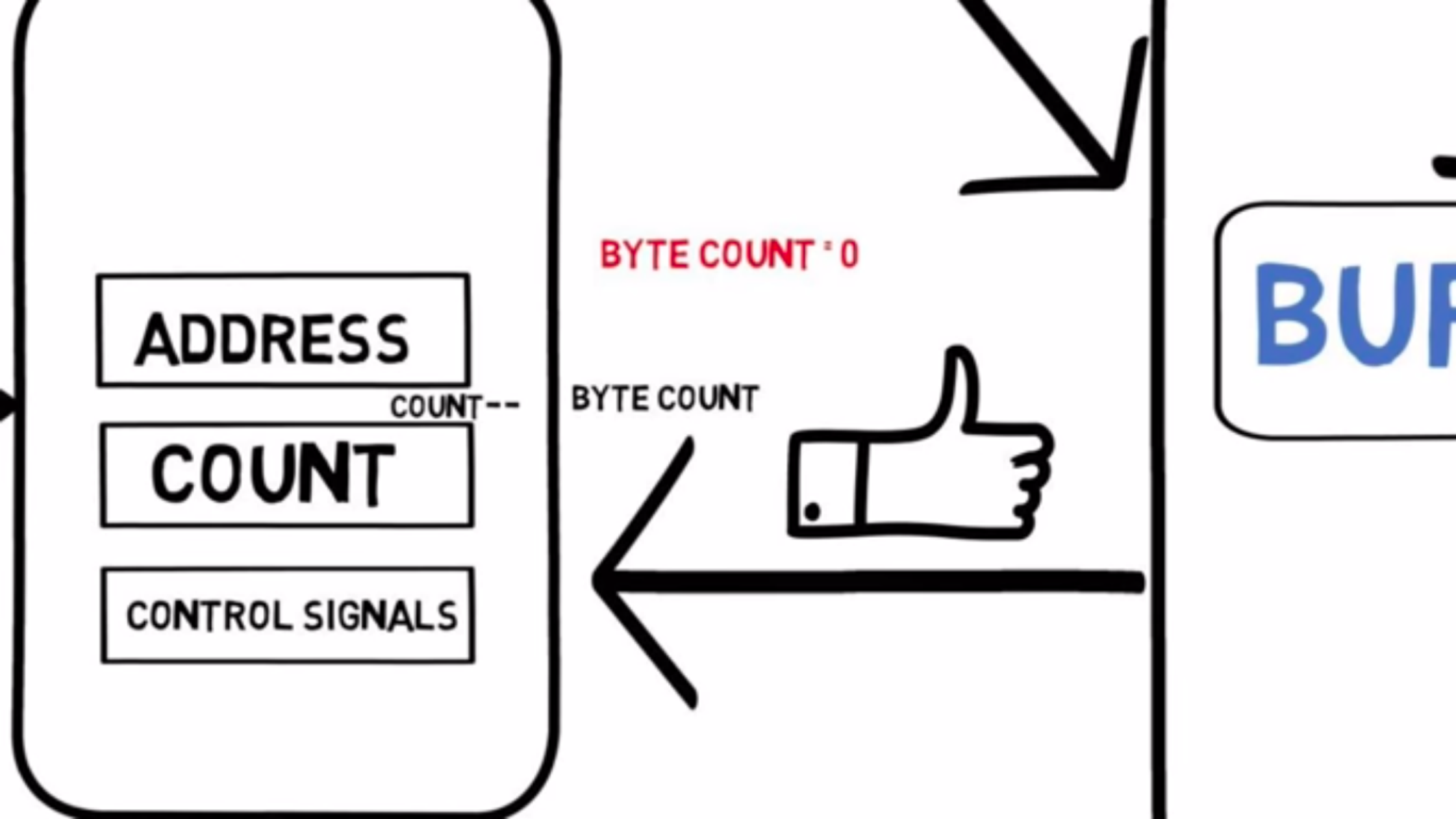

4 BLOCKS
READ
DMAC
DISK CONTROLLER
MEMORY
ADDRESS
COUNT
CONTROL SIGNALS

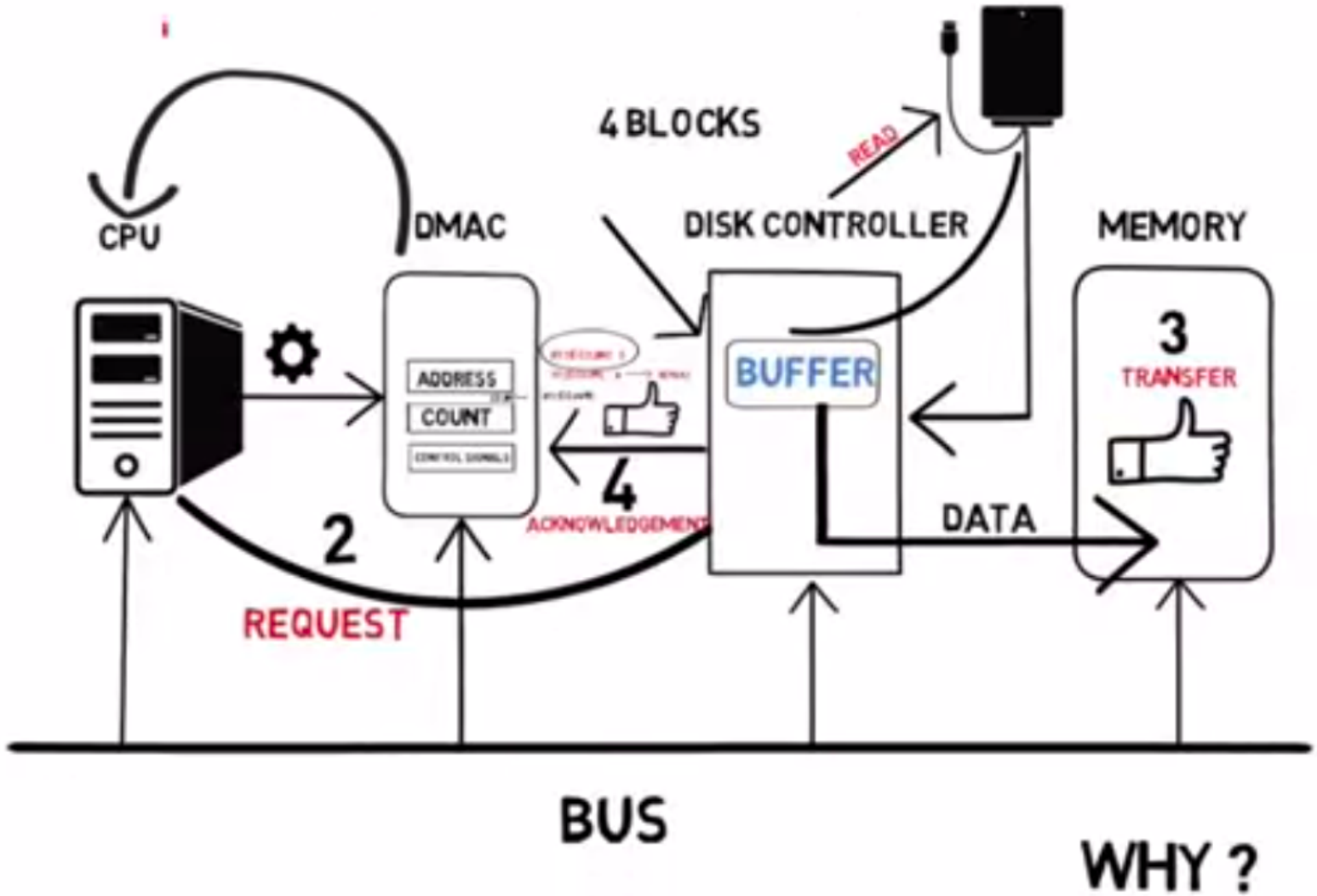

4 BLOCKS
READ
CPU
DMAC
DISK CONTROLLER
MEMORY
ADDRESS
COUNT
BUFFER
BUS


4 BLOCKS
READ
CPU
DMAC
DISK CONTROLLER
MEMORY
ADDRESS
COUNT
BUFFER
DATA
BUS
WHY ?


DMAC
DISK CONTROLLER
ADDRESS
COUNT
CONTROL SIGNALS
BUFFER
DATA


ADDRESS
COUNT--
COUNT
CONTROL SIGNALS
BYTE COUNT


BYTE COUNT = 0
ADDRESS
COUNT--
COUNT
BYTE COUNT
CONTROL SIGNALS
BUF


4 BLOCKS
READ
CPU
DMAC
DISK CONTROLLER
MEMORY
ADDRESS
COUNT
BUFFER
3
TRANSFER
4
ACKNOWLEDGEMENT
DATA
2
REQUEST
BUS
WHY ?