Universidade Federal de Santa Catarina
Centro Tecnológico – CTC
Departamento de Engenharia Elétrica

"EEL7020 – Sistemas Digitais"

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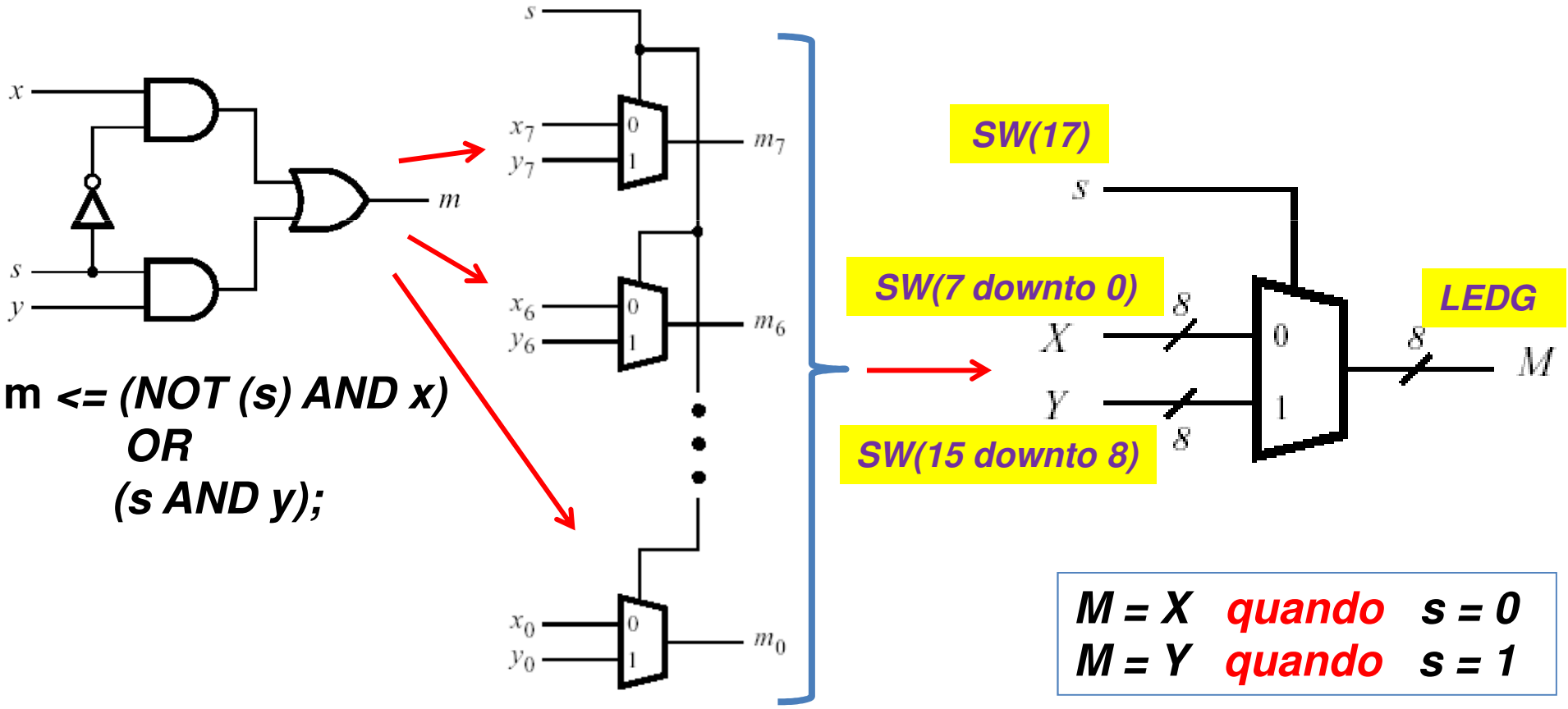
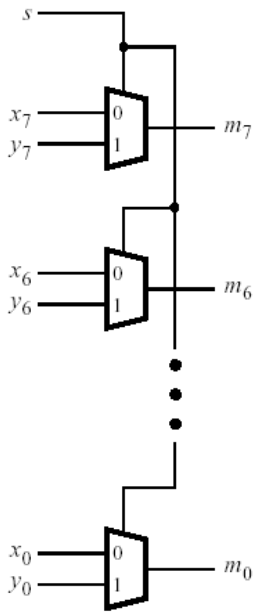
Projeto de multiplexador 2 x 1 de 8 bits

Projeto de multiplexador

Projetar um circuito em VHDL com duas entradas de 8 bits, X e Y, e produzir uma saída M de 8 bits. Se s = 0, M =X. Se S = 1, M = Y.



PARTE I

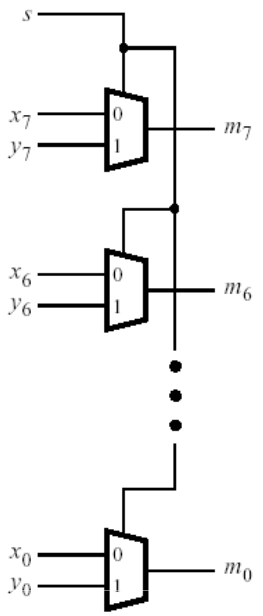



```
library ieee;
use ieee.std_logic_1164.all;
entity part1 is
      port (   SW     : in std_logic_vector(17 downto 0);
               LEDR : out std_logic_vector(17 downto 0);
               LEDG : out std_logic_vector(7 downto 0)
            );
end part1;
architecture behavior of part1 is
begin
      LEDG(0) <= (NOT SW(17) AND SW(15)) OR (SW(17) AND SW(7));
      LEDG(1) <= (NOT SW(17) AND SW(14)) OR (SW(17) AND SW(6));
      LEDG(2) <= (NOT SW(17) AND SW(13)) OR (SW(17) AND SW(5));
      LEDG(3) <= (NOT SW(17) AND SW(12)) OR (SW(17) AND SW(4));
      LEDG(4) <= (NOT SW(17) AND SW(11)) OR (SW(17) AND SW(3));
      LEDG(5) <= (NOT SW(17) AND SW(10)) OR (SW(17) AND SW(2));
      LEDG(6) <= (NOT SW(17) AND SW(9))  OR (SW(17) AND SW(1));
      LEDG(7) <= (NOT SW(17) AND SW(8))  OR (SW(17) AND SW(0));
      LEDR <= SW;
end behavior;
```

M *S* *X* *S* *Y*

m <= (NOT (s) AND x) OR (s AND y);

PARTE II



S = SW(17)
X = SW(7 downto 0)
Y = SW(15 downto 8)

```
library ieee;
use ieee.std_logic_1164.all;
entity part1 is
      port (   SW     : in std_logic_vector(17 downto 0);
               LEDR : out std_logic_vector(17 downto 0);
               LEDG : out std_logic_vector(7 downto 0)
            );
end part1;
```

M = LEDG

```
architecture behavior of part1 is
begin
      LEDG <= SW(7 downto 0) WHEN SW(17) = '1' ELSE SW(15 downto 8);
      LEDR <= SW;
end behavior;
```

M *X* *S* *Y*

Tarefa Adicional

```
library ieee;
use ieee.std_logic_1164.all;
entity part2 is
      port (   SW     : in std_logic_vector(1 downto 0);
               LEDR : out std_logic_vector(15 downto 0);
               LEDG : out std_logic_vector(7 downto 0)
               );
end part2;
architecture behavior of part2 is
begin

    LEDG <= ”00001111” WHEN SW = “00” ELSE
                ”11110000” WHEN SW = “01” ELSE “00000000”;
    LEDR <= x”5555” WHEN SW = “10” ELSE
                x”1111” WHEN SW = “11” ELSE
                x”0000” ;

end behavior;
```