11-12 TREE AND ARRAY MULTIPLIERS AND VARIATIONS IN MULTIPLIERS

Chapter Goals

Learn additional methods for synthesizing fast multipliers as well as other types of multipliers (bit-serial, modular, etc.)

Chapter Highlights

Building a multiplier from smaller units
Performing multiply-add as one operation
Using a multiplier for squaring is wasteful
Building modular multipliers

TREE AND ARRAY MULTIPLIERS AND VARIATIONS IN MULTIPLIERS: TOPICS

Topics in This Chapter
11.1. Full-Tree Multipliers
12.1 Divide-and-Conquer Designs
12.2 Additive Multiply Modules
12.5 The Special Case of Squaring
12.6 Modular Multipliers

11.1 FULL-TREE MULTIPLIERS

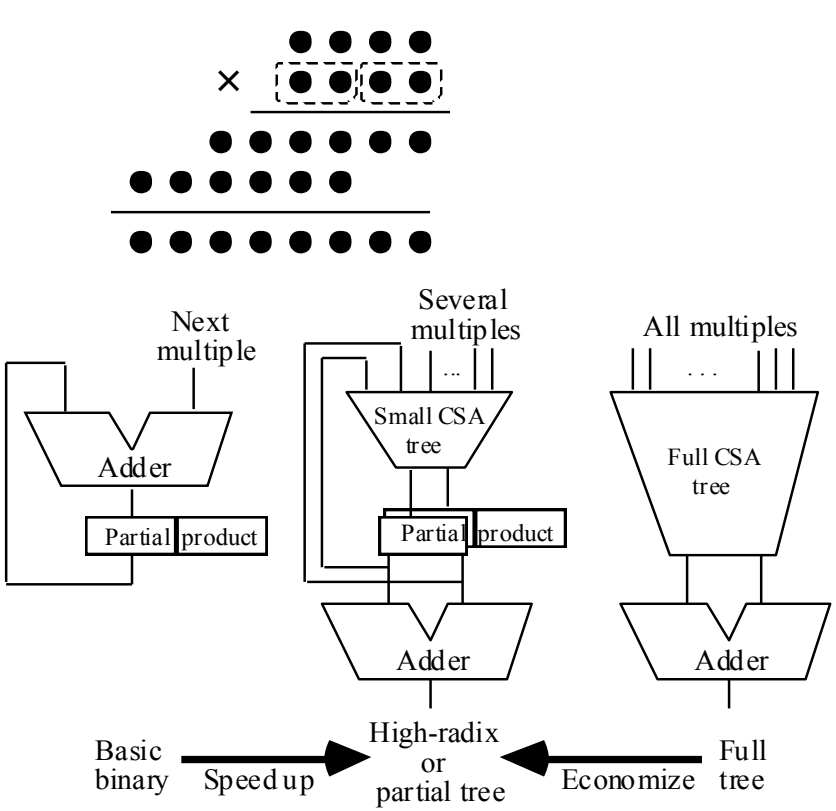


Fig. 10.13 High-radix multipliers as intermediate between sequential radix-2 and full-tree multipliers.

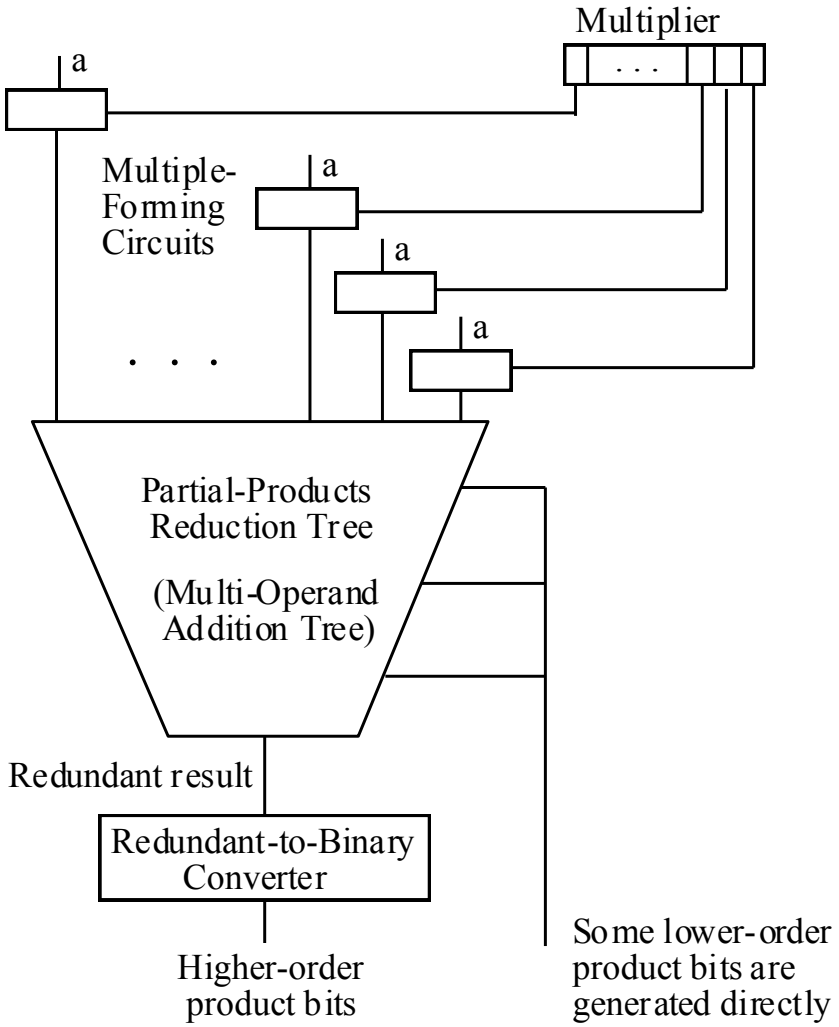
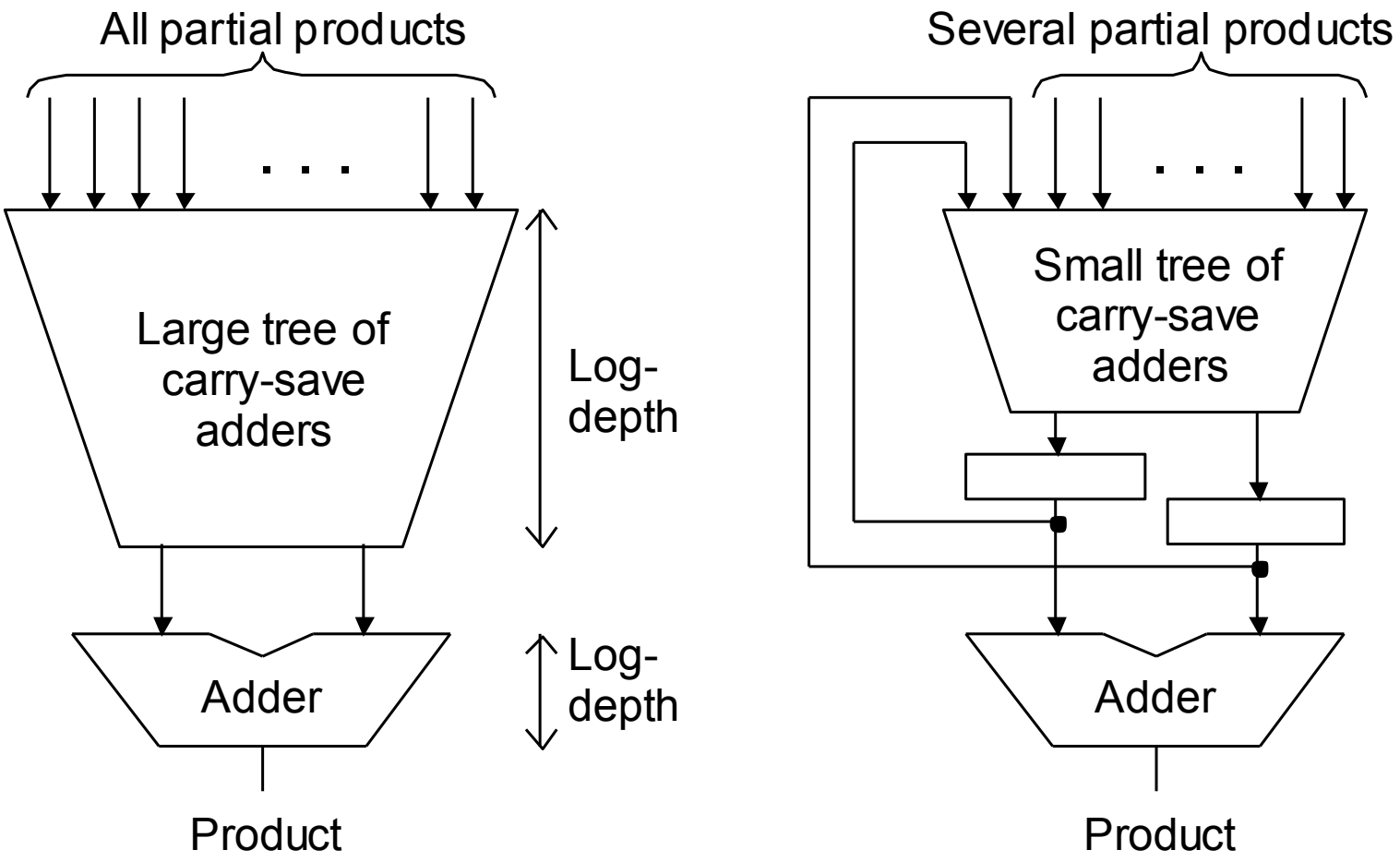


Fig. 11.1 General structure of a full-tree multiplier.

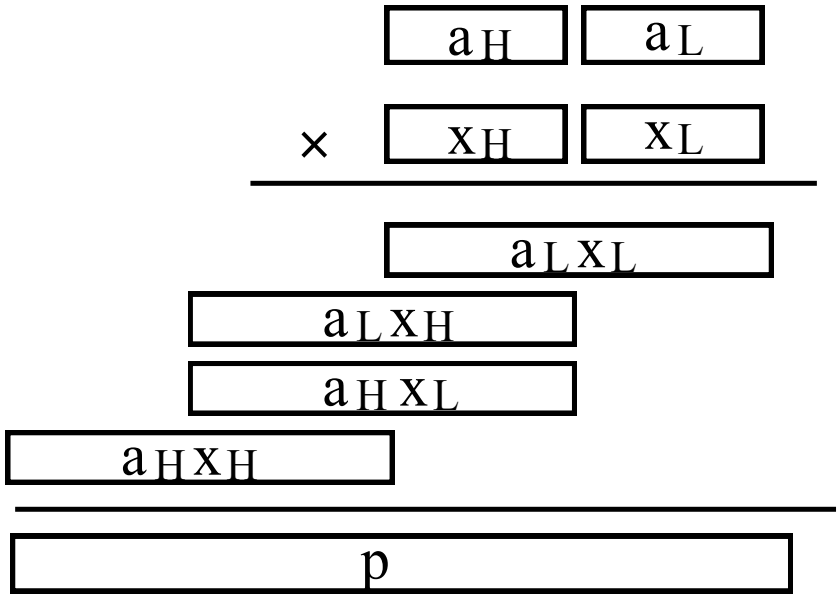
FULL-TREE VERSUS PARTIAL-TREE MULTIPLIER



Schematic diagrams for full-tree and partial-tree multipliers.

12.1 DIVIDE-AND-CONQUER DESIGNS

Building wide multiplier from narrower ones



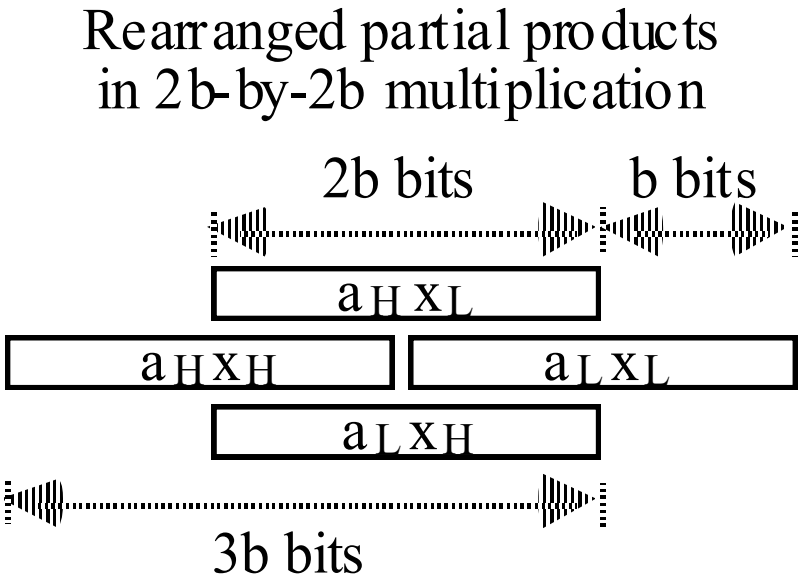


Fig. 12.1 Divide-and-conquer (recursive) strategy for synthesizing a $2b \times 2b$ multiplier from $b \times b$ multipliers.

GENERAL STRUCTURE OF A RECURSIVE MULTIPLIER

$2b \times 2b$ use (3; 2)-counters
$3b \times 3b$ use (5; 2)-counters
$4b \times 4b$ use (7; 2)-counters

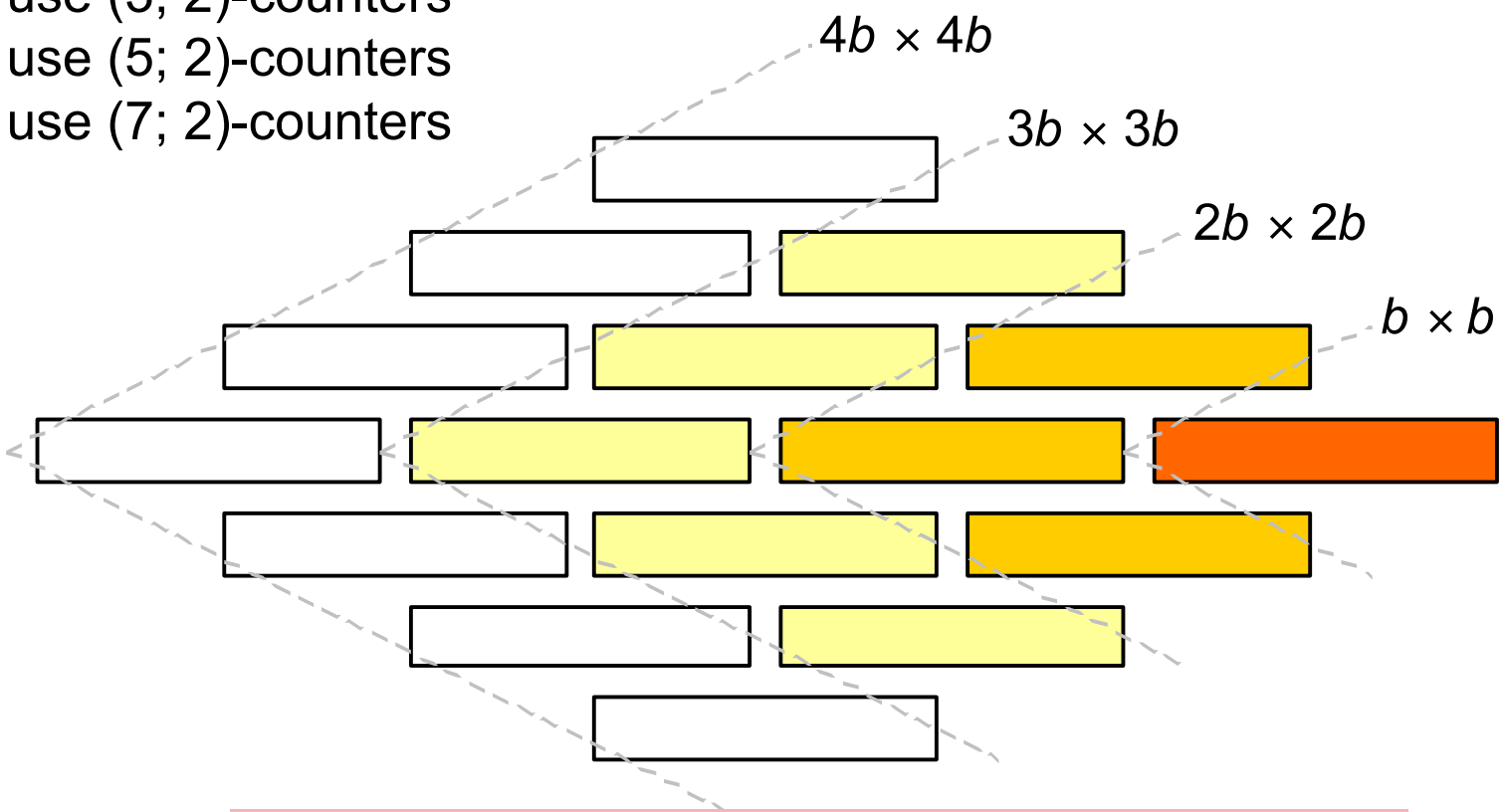
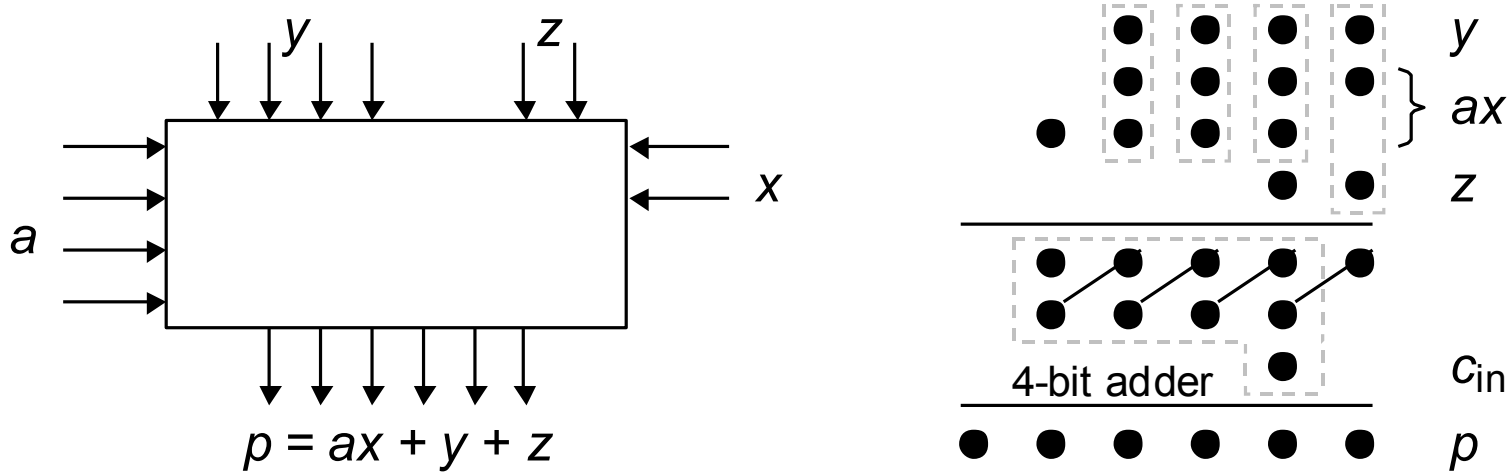


Fig. 12.2 Using $b \times b$ multipliers to synthesize $2b \times 2b$, $3b \times 3b$, and $4b \times 4b$ multipliers.

PROBLEMAS

Problema 11.1. Para uma multiplicação de dois operandos de 24 bits, aplique o método de dividir para conquistar e obtenha o custo e caminho critico dos blocos considerando A_{FA} e T_{FA} como a área e atraso por *Full-Adder*, e $0{,}5\times A_{FA}$ e $0{,}5\times T_{FA}$, para o *Half-Adder*, $(a/2)\times A_{FA}$ e $(a/2)\times T_{FA}$ para o (2^a*:1*) MUX.

12.2 ADDITIVE MULTIPLY MODULES



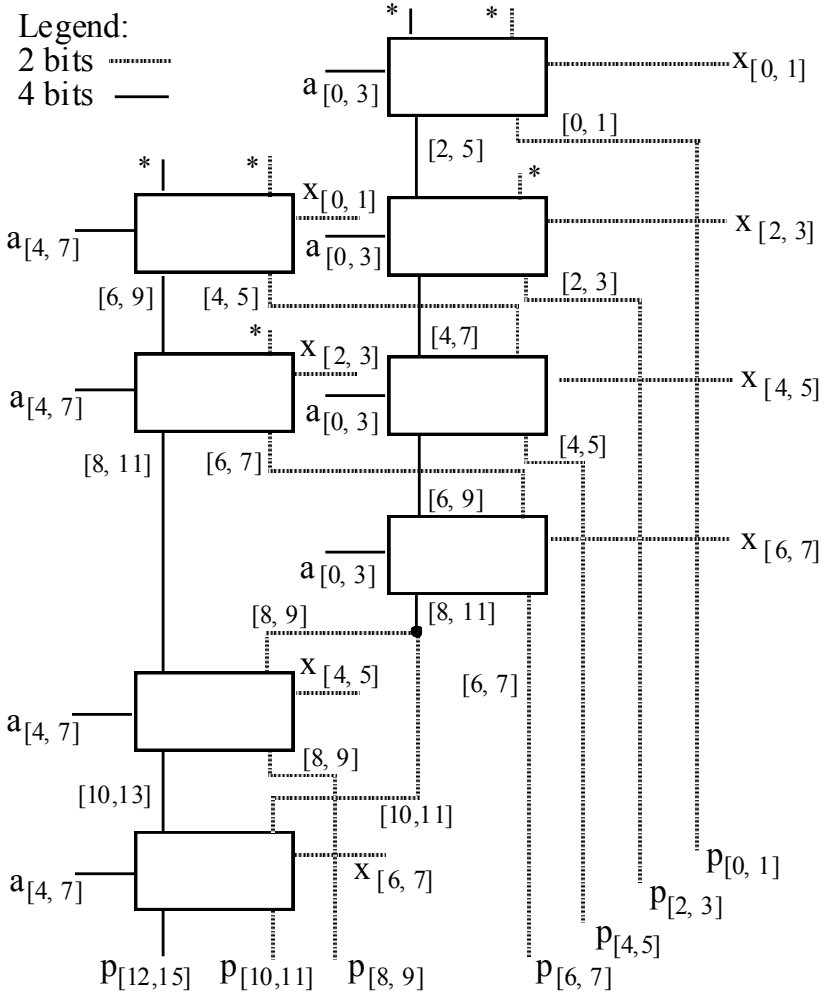
(a) Block diagram (b) Dot notation

Fig. 12.4 Additive multiply module with 2 × 4 multiplier (*ax*) plus 4-bit and 2-bit additive inputs (*y* and *z*).

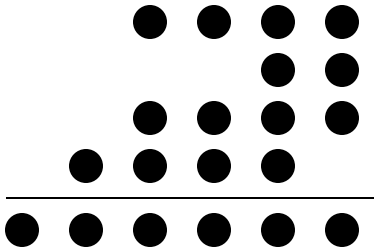
$b \times c$ AMM { *b*-bit and *c*-bit multiplicative inputs; *b*-bit and *c*-bit additive inputs; (*b* + *c*)-bit output

$$(2^b - 1) \times (2^c - 1) + (2^b - 1) + (2^c - 1) = 2^{b+c} - 1$$

MULTIPLIER BUILT OF AMMS



Understanding an 8 × 8 multiplier built of 4 × 2 AMMs using dot notation



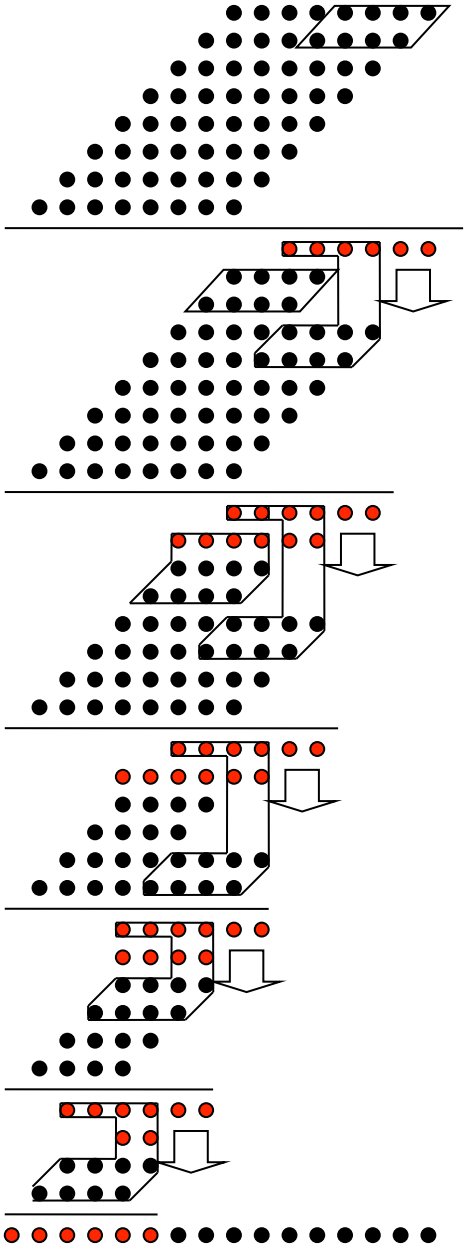


Fig. 12.5 An 8 × 8 multiplier built of 4 × 2 AMMs. Inputs marked with an asterisk carry 0s.

PROBLEMAS

Problema 12.1. Projete um AMM *2×2*, com duas entradas de soma de dois bits usando unicamente 4 full adders e 4 portas AND.

a) Mostre como conectar os AMMs projetados para projetar um multiplicador *4×4*.
b) Determine o caminho critico usando o Full adder como unidade de atraso.
c) Pode ser usado o multiplicador do apartado a como um AMM *4×4*?.

Problema 12.2. Projete os seguintes AMMs usando unicamente *2×4* AMMs:

a) *4×4* AMM;
b) *2×8* AMM;
c) *6×6* AMM
d) *4×8* AMM
e) *4×8* AMM (usando *4×4* AMMs).
f) Compare a eficiência de d) e e) em área e atraso considerando A_{FA} e T_{FA} como a área e atraso por *Full-Adder*, e $0{,}5\times A_{FA}$ e $0{,}5\times T_{FA}$, para o *Half-Adder.*

Problema 12.3. Projete o circuito AMM da seguinte expressão: $A\times B\times C+2^{b}D+2^{c}E+2^{a}F$, onde A, D tem a=4 bits, B, E tem b=3 bits e C, F tem c=2 bits.

12.5 THE SPECIAL CASE OF SQUARING

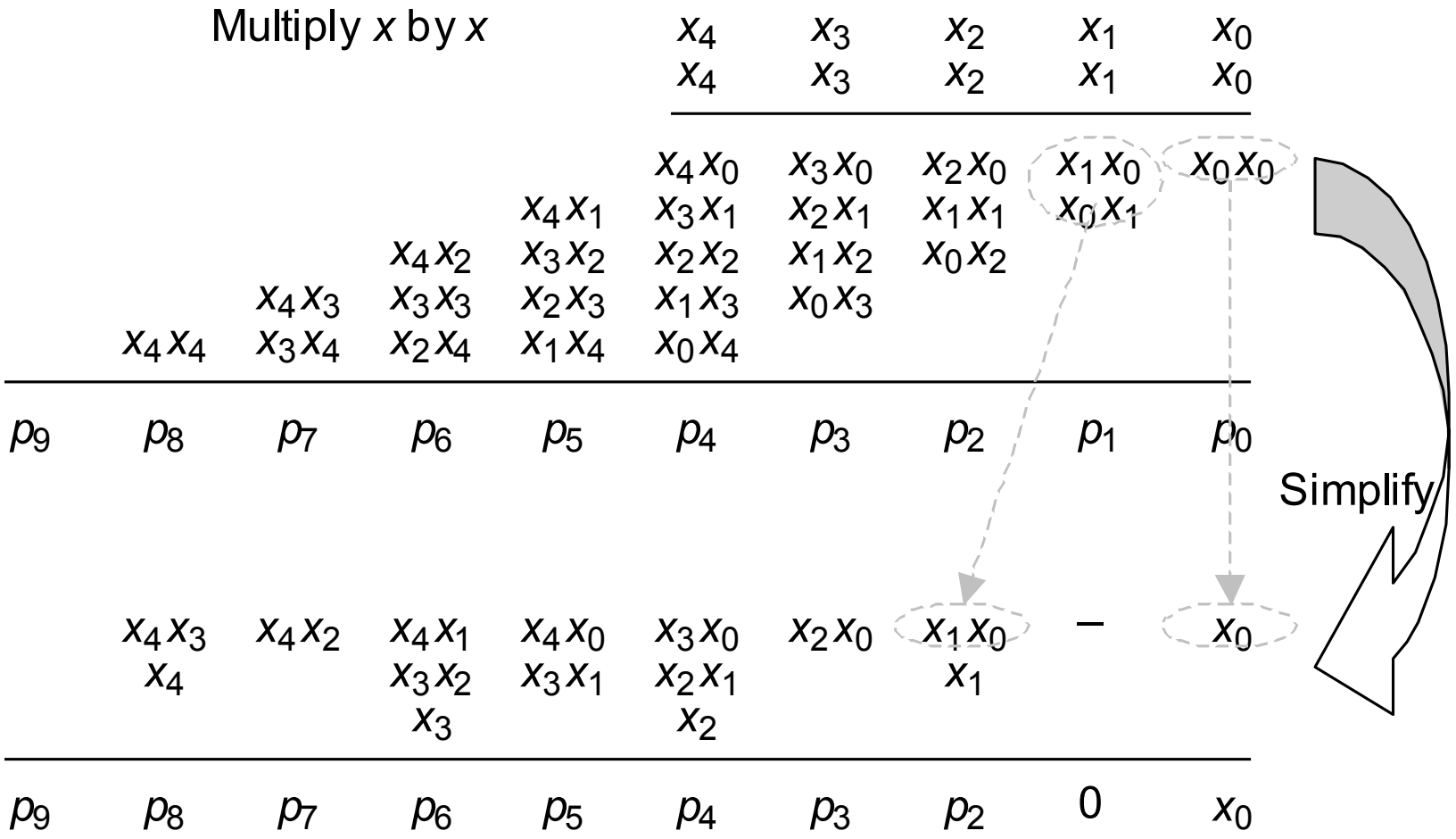


Fig. 12.18 Design of a 5-bit squarer.

PROBLEMAS

Problema 12.4. Projete a estrutura do multiplicador quadrático RNS para os seguintes módulos:

a) 29;

b) 31;

c) 13.