cadence™

# Getting Started with Allegro PCB Design CIS® L and XL

**Product Version 16.3**
**December 200b**

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

# Contents

# Getting Started with Allegro PCB Design CIS

## Welcome to Allegro PCB Design CIS

Allegro® PCB Design CIS is a complete printed circuit board (PCB) design solution that integrates PCB tools for creating design projects, managing libraries, capturing schematics, packaging, physical placement and routing, and producing manufacturing output.

Allegro PCB Design CIS contains the following tools:

- OrCAD® Capture CIS (henceforth referred to as Capture CIS), a design capture tool with a comprehensive component information system,
- Allegro PCB Editor, a comprehensive interactive PCB layout editor,
- Allegro PCB Router, a shape-based auto-interactive router, and
- an extensive range of mechanical interfaces and PCB database translators

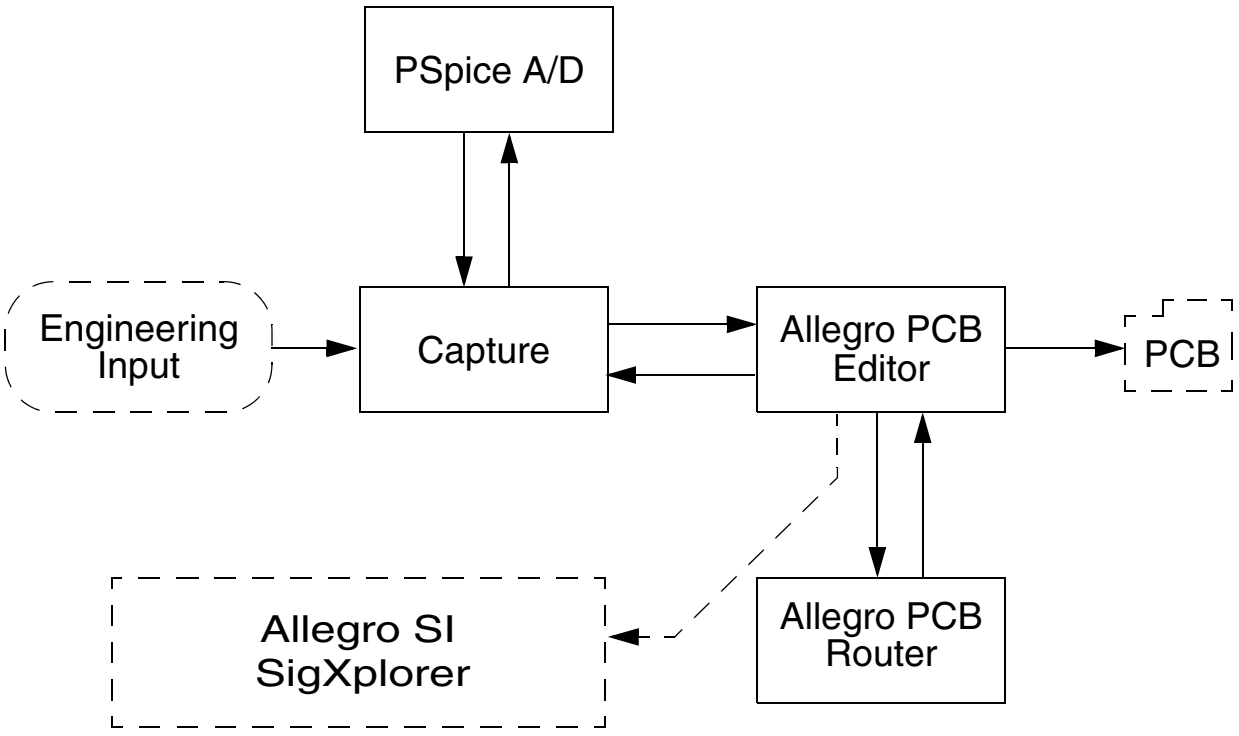
This document provides you with the information you need to get “up and running” with the Allegro PCB Design CIS tools. This document is organized as follows:

# High-level PCB Design Flow

The high-level project flow to create a PCB is as follows:

1. Begin a new project using Capture® CIS.
2. Use Capture CIS to create your design.
3. Netlist your design in Allegro PCB Editor® format.
4. Import the netlist into Allegro PCB Editor.
5. Place components on the board using Allegro PCB Editor.
6. Route the design using Allegro PCB Router®.
7. Create the manufacturing output using Allegro PCB Editor.

The following diagram shows the tool flow that you can use to create a printed circuit board design using Allegro PCB Design CIS.



**Note:** SigXplorer is a tool that you can purchase in addition to Allegro PCB Design CIS tools to analyze signal integrity on pre-route and post-route nets. For information about SigXplorer, see *Getting Started with Allegro PCB SI L*.

**Note:** Each Allegro PCB Design CIS tool has extensive online information available from the tool's graphical interface. To access this information, choose a topic from the Help menu or click on a Help button in any dialog box.

# Setting up a new project with Capture CIS

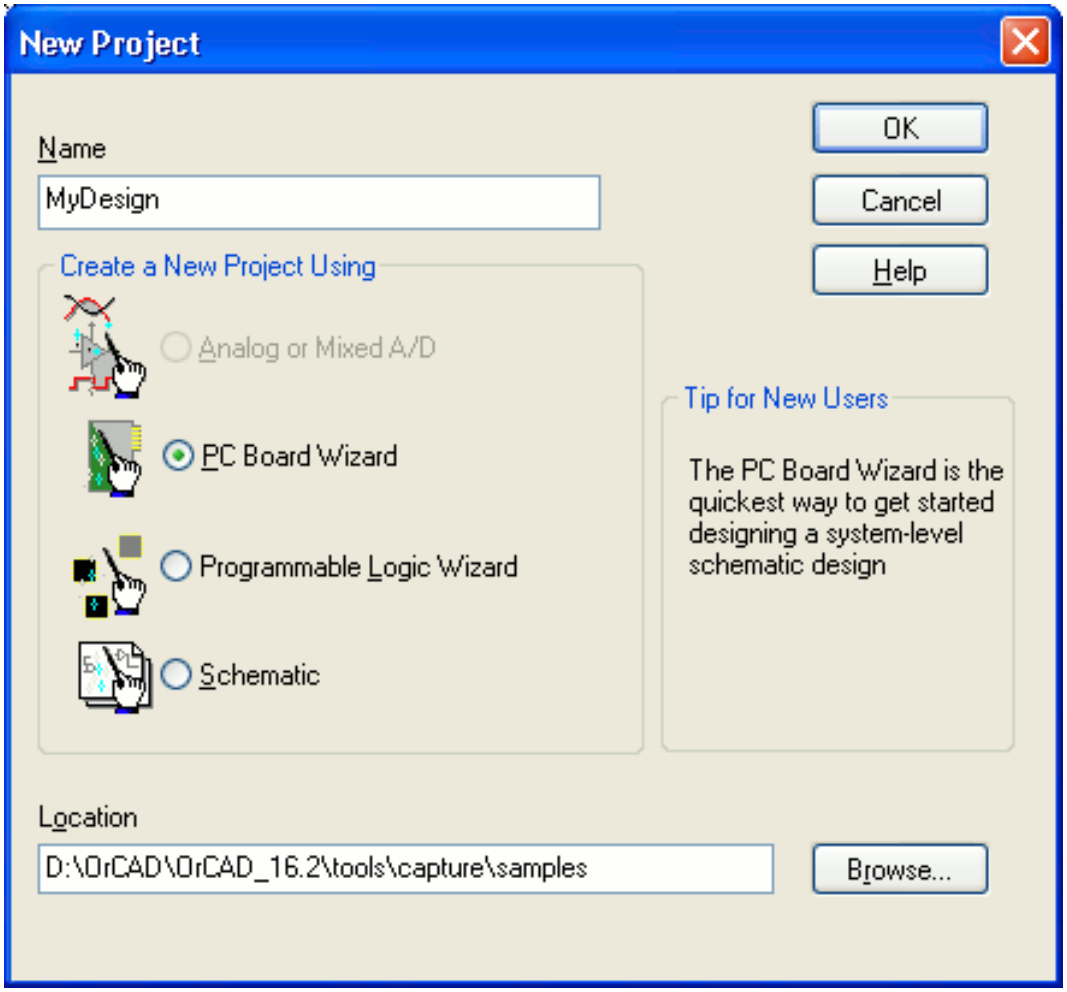
**Note:** It is recommended that you create a new folder using Windows Explorer for each new project and design. You can also create a new directory from the New Project dialog box while browsing for a project location.

To set up a project and directory structure with Capture CIS, perform the following steps:

1. From the Start menu, point to Programs, point to Cadence PSD 15.5, then choose Capture CIS.
2. From the File menu, point to New, then choose Project.

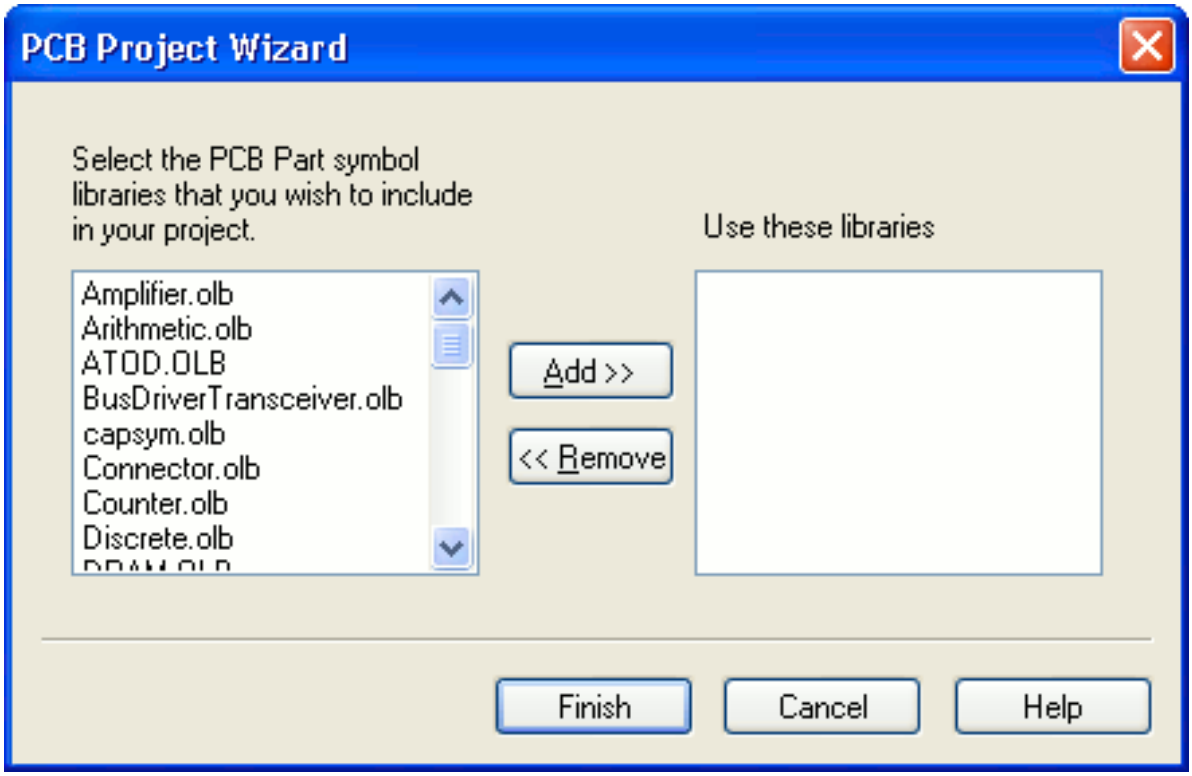
   The New Project wizard dialog box appears.

3. Choose a project type (Analog or Mixed-Signal circuit, PC Board, or Schematic) and enter the name of your new project in the Name text box of the New Project dialog box. You can accept the default location or change it.




4. Click OK to continue.

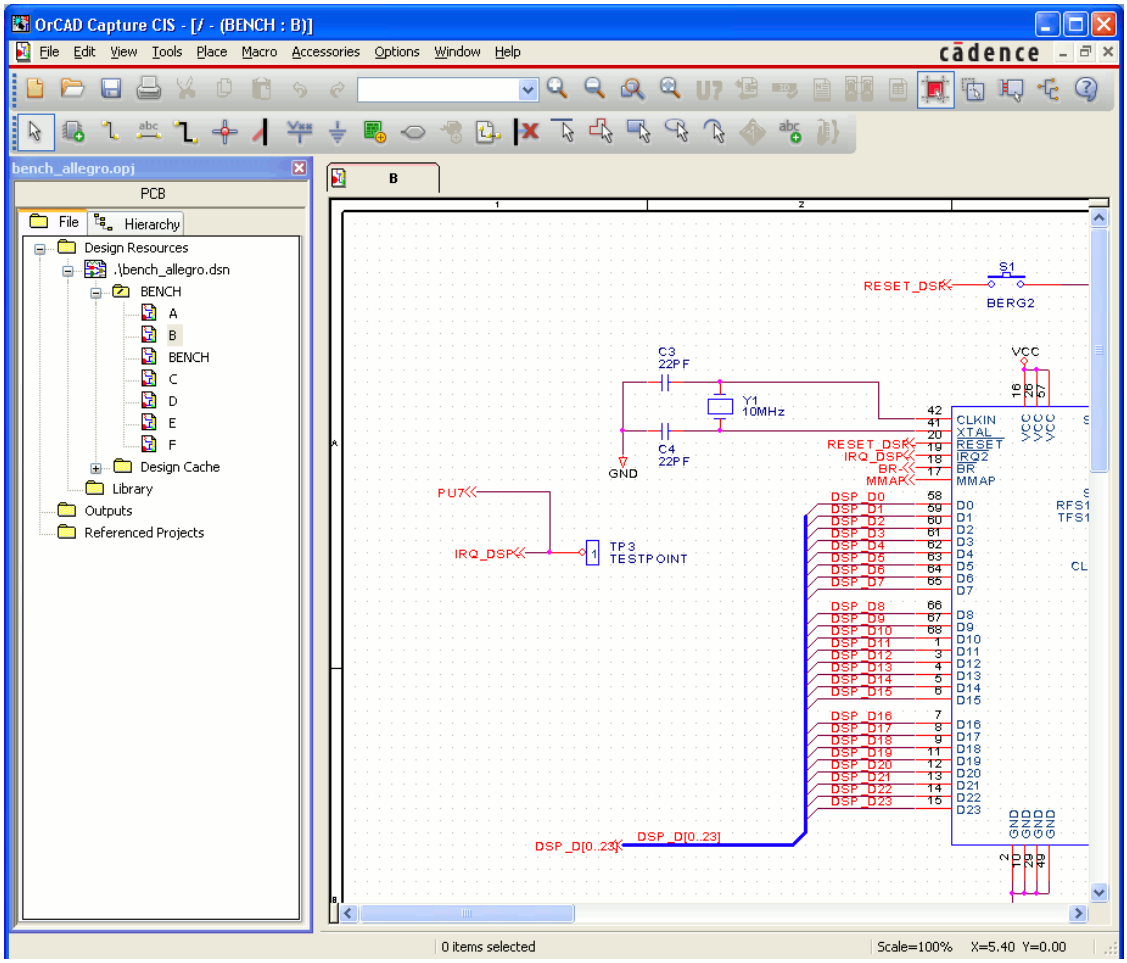
5. Select the libraries that you need for the project or enable project simulation if prompted. Different project types (Analog or Mixed Signal, PC Board Wizard, and so on) offer different library options.




6. Click Finish when you are done

# Using Capture CIS to create and design schematics

Capture CIS is a design environment that supports behavioral and structural design descriptions that are designed using text and graphics.




Capture CIS comes with a large library of schematic symbols and associated VHDL models, as well as the EDIF 2 0 0 schematic and netlist interfaces.

Capture CIS accommodates teams that work on complex design projects by supporting a top-down approach to design. Capture CIS incorporates hierarchical stack editing functions for quick architectural design.

A design architect can use Capture CIS to create a top-level schematic and refine underlying areas while team members work on their respective sub-designs. One engineer can work on a schematic by referencing another engineer's schematic externally through a hierarchical reference (hierarchical block).

## Starting Capture CIS

To start Capture CIS, from the Start menu, point to Programs, point to Cadence PSD 15.5, the choose Capture CIS.

## Capture CIS Design Flow

The schematic layout design process consists of the following general flow. You can tailor the tasks in the flow to your specific design needs. Refer to the online information in Capture CIS for more information about the operations in each step.

| | |
|---|---|
| **Step 1**<br>Develop libraries. | Create or modify symbols using the Part Editor.<br>■ From the File menu, point to New and choose Library,<br>or<br>■ From the File menu, point to Open and choose Library. |
| | Create graphical parts that represent schematic-to-Allegro PCB Editor mapping (pin name to pin number mapping). |
| **Step 2 (optional)**<br>Configure CIS database | From the Options menu, choose CIS Configuration |
| **Step 3**<br>Create a new project. | Create a new project in Capture CIS. |
| | Select the libraries. |
| **Step 4**<br>Create your design. | Set up the border, grid reference, page size, and title block as desired. Add any necessary items not set up in the design template. |
| | Create a new design. |
| | Place parts (from the CIS database or from libraries) on the page. |
| | Add connectivity to your design (wire it). |
| | Add hierarchical blocks and pins. Hierarchical pins and ports should have the appropriate type (Input, Output, Bidirectional, Passive, and so on). The hierarchical block goes on the parent schematic and the ports go on the child schematic(s). |
| | Add as many pages as are necessary to complete the design. |

| | |
|---|---|
| **Step 5**<br>If you are creating a hierarchical design, complete the hierarchical blocks. | Name the hierarchical pins so that they match the port names of the child schematic and connect the signals using off-page connectors for pages in the same level of hierarchy. |
| | Fill in the implementation properties of the hierarchical block to correctly reference the child schematic(s). If the child schematic is not created, descending the hierarchy will automatically create the child schematic using a default name. |
| **Step 6**<br>Create another schematic. | If you are designing hierarchically, repeat Step 5 to complete all hierarchical blocks. |
| **Step 7**<br>Assign constraints to your design. | Using the property editor, attach Allegro PCB Editor-specific properties to the components, pins, and signals. You use these properties to control the board layout process. You can also import this data into the high-speed Allegro SI environment.<br><br>**Note:** Every part must have a PCB footprint property defined. |
| **Step 8**<br>Annotate in Capture. | You can automatically assign reference designators using the Annotate tool (in the Capture Project Manager, from the Tools menu, choose Annotate) or assign reference designators manually in Capture in the property editor. |
| **Step 9 (optional)**<br>Create design variants | Create design variants |
| **Step 10 (optional)**<br>Generate BOM. | Generate Bill of Materials (BOM) |
| **Step 11**<br>Create the physical netlist. | To create the netlist for Allegro PCB Editor, do the following:<br>**1.** Select the DSN object in the Capture project manager, then choose Create Netlist from the Tools menu.<br>**2.** Select the Allegro tab.<br>**3.** Click the Setup button. Select (and edit, if necessary) the configuration file and specify the number of backups you want.<br>**4.** If you select the option to create an Allegro PCB Editor board, go to step 13. |
| **Step 12**<br>Import the netlist into Allegro PCB Editor. | Import the netlist into Allegro PCB Editor and create the Allegro PCB Editor board. |

| | |
|---|---|
| **Step 13**<br>Layout the board with Allegro PCB Editor. | See "Allegro PCB Editor design flow" on page 16. |
| **Step 14**<br>Back annotate any changes to the Capture CIS design. | Back annotate any changes to the Capture CIS design.<br>To back annotate, do the following:<br>**1.** Select the DSN object in the Capture project manager, then choose Back Annotate from the Tools menu.<br>**2.** Select the Allegro tab.<br>**3.** Specify the board file, the netlist directory, and the swap file path and name.<br>The netlist is generated from the design, the view files are extracted from the Allegro PCB Editor board file, then a swap file is created back annotating board information from Allegro PCB Editor to Capture CIS by comparing the netlist and view files. If you select the Update Schematic check box, your schematic will be back-annotated after the swap file is generated. If you did not select the Update Schematic check box, you can use the Layout tab to select your swap file or run another Allegro PCB Editor back annotation with the Update Schematic check box selected. |

## Exporting Capture CIS data for Allegro PCB Editor board layout

To export Capture CIS schematic data for Allegro PCB Editor processing, select the DSN object in the Capture project manager, then choose Create Netlist from the Tools menu. In the Create Netlist dialog box, choose the Allegro tab.

## Using Part Editor

The Part Editor is a utility in Capture CIS that creates and edits component data. Using the Part Editor, you can edit the schematic symbol, pin data, and part number information from a single environment.

You can create or modify parts and symbols using the Part Editor. From the File menu, point to New and choose Library--or--from the File menu, point to Open and choose Library. With the library open and selected in the project manager, from the Design menu choose New Part or New Symbol. Double-click on the part or symbol to edit it.

You can also open the Part Editor by editing a part in place. Select a part in the schematic editor, then from the Edit menu, choose Part.

The Part Editor ensures correct part generation through comprehensive error checking routines.

For more information about the Part Editor, see the *Capture Online Help*.

### Using PSpice A/D

PSpice simulates analog-only, mixed analog/digital, and digital-only circuits. After you prepare a design for simulation, you can use Capture to generate a circuit file set. The circuit file set, containing the circuit netlist and analysis commands, is read by PSpice for simulation. PSpice formulates the file set into meaningful graphical plots, which you can mark for display directly from your schematic page using markers.

For more information about PSpice, see the *PSpice Online Help*.

## Allegro PCB Editor for board layout

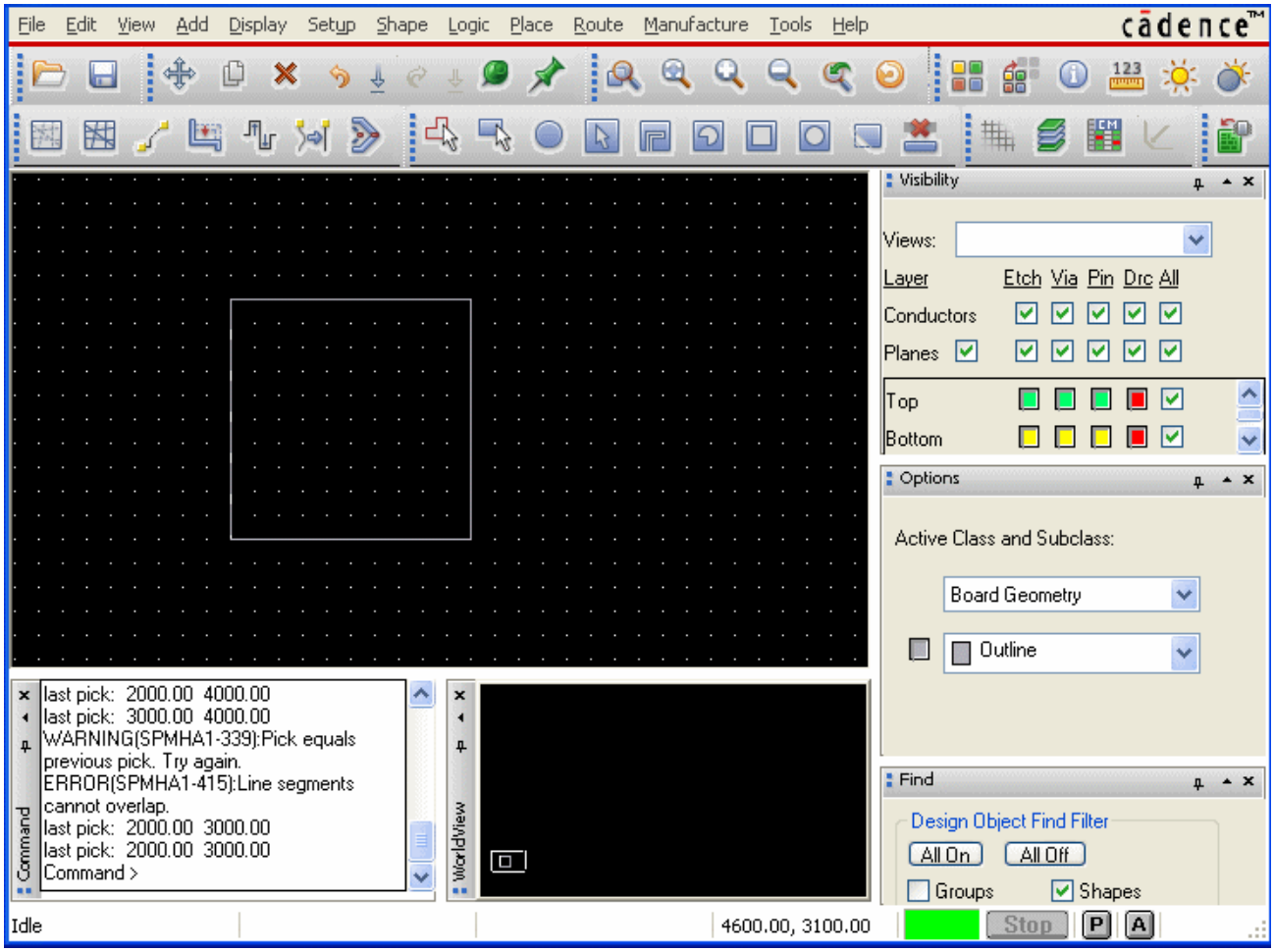
Allegro PCB Editor is the physical layout system for PCB design. With Allegro PCB Editor you can place and route a design, and then generate the output and documentation necessary for the manufacture of that design. Allegro PCB Editor's rules-driven editing tools provide you with instant feedback on design rule violations. Seamless integration with Allegro PCB Router provides access to interconnect routing of critical signals, buses, areas, or for the whole design. Allegro PCB Editor comes with a variety of third-party CAD interfaces, such as AutoCAD DXF and IDF, and third-party PCB database translators, such as PADS and PCAD.

### Starting Allegro PCB Editor

To start Allegro PCB Editor, from the Start menu, point to Programs, point to Cadence SPB 15.7, then choose Allegro PCB Editor.

The Cadence Product Choices dialog box appears if you have more than one license. This dialog box lets you choose from the available tools for which you have licenses. The Allegro

PCB Editor tool is licensed with Allegro PCB Design CIS L. For other Allegro PCB Editor products, see your Cadence representative.



## Allegro PCB Editor design flow

The physical layout process consists of the following general flow.

| | |
|---|---|
| **Step 1**<br>Develop libraries. | Create padstacks. |
| | Create symbols. |
| | Develop board templates. |
| **Step 2**<br>Transfer logic and physical data. | Transfer native logic using the files generated by Netrev. |
| **Step 3**<br>Prepare Allegro PCB Editor layout. | Create a new drawing. |
| | Set drawing size. |
| | Define cross section layers. |
| | Assign and define properties. |
| | Define constraints. |
| **Step 4**<br>Lay out the design in Allegro PCB Editor. | Define placement. |
| | Swap pins and gates. |
| | Add power and ground planes. |
| | Route connections. |
| **Step 5**<br>Prepare the final design in Allegro PCB Editor. | Run testprep. |
| | Run glossing. |
| | Rename reference designators. |
| | Run design rule checking. |
| | Create silkscreen. |
| **Step 6**<br>Synchronize design with changes made in board file | Back annotate changes to Capture. |
| **Step 7**<br>Generate manufacturing outputs. | Generate reports. |
| | Generate fabrication and assembly output. |
| | Create plot files. |
| | Create artwork. |

## Importing Capture CIS schematic data into Allegro PCB Editor

We recommend that you read the Allegro PCB Editor documentation before attempting to prepare your Capture schematic for netlisting to Allegro PCB Editor.

To import Capture CIS schematic design data into Allegro PCB Editor, in Allegro PCB Editor, from the File menu, point to Import, then choose Logic. The Import Logic dialog box appears. For information about this dialog box, click the Help button in the dialog box. Allegro PCB Editor reads and compiles the netlist.

*Important*

If you are planning to use the back annotation translation function later, then the netlist files created by Capture must not be manually modified on the Allegro PCB Editor side.

## Exporting Allegro PCB Editor data (back annotating) to Capture CIS

To use your Allegro PCB Editor board design data to update (back annotate) your schematic design in Capture, you can do any of the following.

- In Allegro PCB Editor, from the File menu, point to Export, then choose Logic. This dialog box lets you create schematic data files for use with Capture CIS.
- In Capture's project manager window, select the .DSN file. From the Tools menu, choose Back Annotate. In the Backannotate dialog box, click the Allegro tab and specify the board file and the netlist directory.

  **Note:** Use the Setup dialog box to select the appropriate configuration file for back annotating property information between Capture and Allegro PCB Editor. To access the Setup dialog box, click Setup in the Allegro tab in the Backannotate dialog box.

### Back annotation procedure

This function translates Allegro PCB Editor-produced back annotation files into a (.SWP) file which is then input to Capture's back annotation function.

*Important*

A valid Capture back annotation file can be created only if the original Capture-created netlist is used, without modification, for the board design.

The back annotation from Allegro PCB Editor to Capture is a three-step process. First, you re-annotate your components in Allegro PCB Editor, then export the design logic from Allegro PCB Editor to a Capture-compatible format, and finally back annotate in Capture to incorporate any changes to the design made in Allegro PCB Editor.

### Exporting Allegro PCB Editor data for Allegro PCB Router routing

To create data files for use with Allegro PCB Router, from the File menu, point to Export, then choose Router. The Export to Auto-Router dialog box appears. For information about this dialog box, click the Help button in the dialog box.

## Allegro PCB Router for automatic routing

Using its powerful shape-based architecture, the Allegro PCB Router defines the most efficient use of a PCB routing area. Allegro PCB Router performs design rule checks (DRCs) on Allegro PCB Editor constraints and design rules, including those that the engineer defines in Capture CIS.

Allegro PCB Router handles staggered pin components and routes through them easily. Its diagonal routing algorithms handle components of non-standard dimensions (that previously required manual routing).

The Allegro PCB Router is tightly integrated with the Allegro PCB Editor layout tool through the Allegro PCB Router interface.

### Starting Allegro PCB Router

You can start Allegro PCB Router from Allegro PCB Editor or as a stand-alone batch program as follows:

- To start Allegro PCB Router from Allegro PCB Editor, choose one of the following menu items:
  - From the Route menu, choose Route Automatic to set routing parameters and initiate routing of the entire board.
  - From the Route menu, choose Route Net(s) by Pick to route specific nets and components.
  - From the Route menu, choose Route Editor to update your design with information based on parameters that you set up in the Allegro PCB Router interface.

- From the Start menu, point to Programs, point to Cadence SPB, then choose Allegro PCB Router to update your design with information based on parameters that you set up in the Allegro PCB Router interface.

### Exporting Allegro PCB Router routing data (back annotating) to Allegro PCB Editor

Routing data is automatically added to a design if you use Allegro PCB Router from the Allegro PCB Editor interface.

If you use Allegro PCB Router as a batch program, you can generate routing data for Allegro PCB Editor by pointing to Write (from the File menu), then choosing Session from the Allegro PCB Router interface. The Write Session dialog box appears. Allegro PCB Router creates a session (.SES) file.

## Generating manufacturing output with Allegro PCB Editor

Allegro PCB Editor provides you with several commands that produce manufacturing output. These commands are available from the Manufacture menu. One of these commands is Artwork, which creates data for manufacturers to physically put the printed circuit design onto film. Allegro PCB Editor supports vector-based and raster-based artwork processes. For more information about the Manufacture menu commands, see the online information that is available from the Allegro PCB Editor interface.