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Project of a bandgap voltage reference and a temperature sensor for "energy harvest" systems

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To all the my friends that supported me and specially to my family

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Abstract

The objective of this thesis is to study the behaviour of a bandgap voltage reference and develop it in order to be more efficient than the existing ones. In this case having applicability in energy harvest, the main approach for this circuit is to reduce the power dissipation and at the same time guarantee a stable of the reference voltage. This can be achieved through the utilization of MOS transistors which can work with a lower voltage then bipolar transistors. The reference voltage circuit present in this thesis can work with a supply voltage as low as 500 mV.

In energy harvest systems besides the need to work with extremely low voltages, the sensitivity of the signals is very high, to temperature variation. So it was also important to work with an extended ranges of temperature.

For this work it was also developed a temperature sensor so that it has applicability in various fields. The sensor works by currents generated by the bandgap voltage reference, having similar results to a dual slope integrating analogue-to-digital converter, although its operation and logic are quite different.

The proposed solution is to implement a reference voltage generator powered by a voltage source of 500 mV, with a consumption of about 7 μ W. Having a temperature coefficient slightly below 74 ppm/°C and a temperature sensor with linearity quite satisfactory.

Keywords: Bandgap, Temperature Sensor, Temperature to digital converter

Resumo

O trabalho desenvolvido nesta tese tem como objetivo estudar o funcionamento de um gerador de tensão de referência e desenvolver o mesmo de forma a ter uma eficiência acima dos conhecidos atualmente. Tendo como aplicabilidade neste caso o "energy harvest",a principal abordagem para este circuito é a redução de consumo do circuito mantendo a estabilização do sinal de referência através de transistores CMOS que têm comportamentos menos lineares que os bipolares. Assim sendo após desenvolvimento do circuito, foi possível obter resultados interessantes através de uma alimentação ao circuito de 500 mV.

Em "energy harvest"além da necessidade de se trabalhar com tensões extremamente baixas, a sensibilidade dos sinais deve ser a máxima, uma vez que a variação de temperatura pode atingir valores demasiado variados. Assim foi também importante trabalhar com gamas de valores de temperatura alargadas.

Para este trabalho foi também desenvolvido um sensor de temperatura de forma a este ter uma aplicabilidade em diversas áreas. O sensor funciona através de correntes geradas pelo gerador de tensão de referência, tendo resultados semelhantes a um conversor de dupla rampa, embora o seu funcionamento e lógica sejam um pouco diferentes.

A solução proposta é a implementação de um gerador de tensão de referência alimentado por uma fonte de tensão de 500 mV, com um consumo de aproximadamente 7μW. Tendo uma estabilidade um pouco abaixo da espectável 74 ppm/°C e um sensor de temperatura com linearidade bastante satisfatória.

Palavras-chave: Gerador tensão referência, Sensor Temperatura, Conversor de temperatura para digital

Acronyms

V_{PTAT} - Proportional to absolute temperature voltage.

V_{CTAT} - Complementary to absolute temperature voltage.

V_{BE} - Voltage between a bipolar junction transistor base and emitter.

V_{GS} - Voltage between a MOS transistor gate and source.

V_{REF} - Reference voltage, the output fixed voltage independent of temperature variations.

ppm - Parts per million, accuracy unit used to determine the precision, in this case of a voltage reference design. For a 1 V reference, 1ppm is one-millionth of 1V, or 1μ V.

TC - Temperature coefficient, is the precision calculated dividing ppm by the temperature range, it allow us to obtain the variation in a Celsius degree.

Op-amp - Operational Amplifier, is a DC-coupled high-gain electronic voltage amplifier.

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1

Introduction

1.0.1 Background and Motivation

In the 60s and 70s the idea of creating a circuit without temperature dependence urged, the idea was firstly explored by several scientists ([Hil64], [Wid71],[Bro74]). The evolution is still in progress as to as minimize the voltage and power dissipation, increase the temperature range, decrease the area and the most important part, obtain a stable voltage reference minimizing the error. This evolution brought outstanding impacts allowing the use in several areas, namely energy harvesting in which guarantee stability in the output of the voltage signal received by external sources such as solar power, wind energy or thermal energy.

Later, different bandgap voltage reference structures will be studied and also the impact of the elements in the circuit. As the main goal of this circuit is to maintain the stability of the voltage reference with the lowest voltage supply possible, the voltage consumption of each element will be studied together with the linearity.

Energy harvesting is the process by which energy is derived from different types of external sources, captured and stored. Those external sources produce low voltage signals which can vary with the temperature(Solar power) or wind(Wind energy). In order to guarantee the best efficiency, the bandgap voltage reference has to dissipate the less power possible and supply the circuit with the minimum voltage possible.

The bandgap voltage reference is essential in the stabilization of the energy harvesting system output, guaranteeing a DC signal which voltage is upgraded by a DC-DC converter and posteriorly stored.

1.0.2 Thesis Organization

In addition to the introduction, this thesis is constituted by four more chapters.

In chapter 2, the development of the first bandgap by Hilbibier is shown, where the voltage variation of a silicon diode as function of temperature was obtained. Afterwards, different elements were used in the same circuit to realize the effects in terms of consumption, stability and factors referred in the last subsection. Finally, following the evolution of the bandgaps, the most efficient were considered and analysed (Widlar and Brokaw). Forward, three actual models of bandgaps will be presented, each one with different structures and using different elements.

In chapter 3, the implementation of each part of the circuit is explained. Firstly the fundamental part of the circuit (bandgap), then the amplifier is added to the circuit in order to force the same voltage in gates. Finally, a temperature sensor is added, through the use of a double ramp analog-to-digital converter, this element will allow to verify the voltage dependence with temperature.

In chapter 4, the simulation result of each part is detailed. Initially, the bandgap voltage reference circuit is simulated using an ideal amplifier, with an high gain in order to reduce the error between the two inputs. The amplifier is presented in a subsection with the respective element sizing and the simulation results (gain, phase margin and other simulations). In the end, the simulation of the temperature sensor and its reliability on turning the analog signal to digital is presented.

In chapter 5, the conclusions are taken by the comparison between several voltage reference and the analyse of the total performance of the circuit. After the conclusion, it is possible to consider a couple of improvements to alter the circuit to obtain a better performance in a future work.

1.0.3 Contribution

The main contribution of this paper is the implementation of a circuit with a very low voltage supply (500 mV) using only MOS transistors and resistors to develop the bandgap voltage reference. The bipolar transistors were avoided in order to obtain a very low voltage and stability obtained was similar or even better in several cases.

The MOS transistors are all in saturation with such a low voltage, otherwise few bandgaps work with such a low voltage. The main difficulty was the low range to size the MOS transistors in order to obtain a stable voltage reference.

This low voltage supply circuit was implemented after simulation of the circuits presented in chapter 2 and it was possible to conclude that the bipolar transistors weren't allowed, with a minimum consumption by the V_{BE} of 700 mV. The drop voltage in the resistors is adjustable by the ΔV_{GS} forming the PTAT voltage. Finally, the MOS transistors will work with voltage above 100mV and are useful not only to develop an amplifier or a current mirror, but also to generate the CTAT voltage.

In order to verify the circuit performance, a temperature sensor was also developed.

For that propose, it was used a PTAT current and a constant current to form a double ramp analog-to-digital converter.

2

State of Art

2.1 Principles of a Bandgap voltage reference circuits

In 1964 Hilbiber studied the possibility of creating an integrated circuit without low dependency of temperature. This uses an avalanche diode as a reference voltage source, the short-term stability of the produced reference voltage was 10-50 ppm within a certain temperature range. The problem was to extend this behaviour for a period longer than 1000 hours.

To solve this problem, a new reference voltage source was presented with a nominal output of 1.25670 V and a long-term stability for a period over 12000 hours.

For an ideal p-n junction, the forward voltage (V_F) and temperature dependence $(\frac{dV_F}{dT})$ are function of current density and junction impurity profile, that is given by Schockley's equation.(eq.2.1)

$$\begin{cases} p_n = \frac{(n_i)^2}{N_D} \qquad and \qquad n_p = \frac{(n_i)^2}{N_A} \\ I = I_S[e^{(\frac{qV}{kT})-1}] \end{cases} \tag{2.1}$$

Where $D_{p,n}$ are the diffusion coefficients of holes and electrons and $L_{p,n}$ are the diffusion lengths. From equation 2.1 is possible to verify that the base-emitter voltage for a transistor is a function of the base current.

where I_S is given by:

$$I_S = q(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p) \tag{2.2}$$

As observed by Hilbiber [Hil64], 2.1 and 2.2 it is possible to express (V_{BE}) in a Taylor's series expansion and obtain the temperature and current dependence as shown in Eq. 2.3.

$$V_{BE} = \frac{KT_0}{q}\left\{ln\frac{I_C}{I_S(T_0)} + \left[ln\frac{I_C}{I_S(T_0)} - (\beta + \frac{E_{G0}}{kT_0})\right]\left(\frac{T}{T_0} - 1\right)\right. \\ \left. -\frac{\beta}{2}\left(\frac{T}{T_0} - 1\right)^2 + ... + \frac{\beta(-1)^{n-1}}{n(n-1)}\left(\frac{T}{T_0} - 1\right)^n + ...\right\} \tag{2.3}$$

$$V_{BE} > \frac{4kT}{q} \qquad T < 2T_0$$

Where β is a constant which takes in consideration the temperature dependence of the diffusion coefficients and the diffusion lengths. As seen in Fig. 2.1 for the 2N917 and 2N1893 transistors, with the increasing of the junction doping density or current density, V_{BE} will increase and $\frac{dV_{BE}}{dT}$ will become less negative.

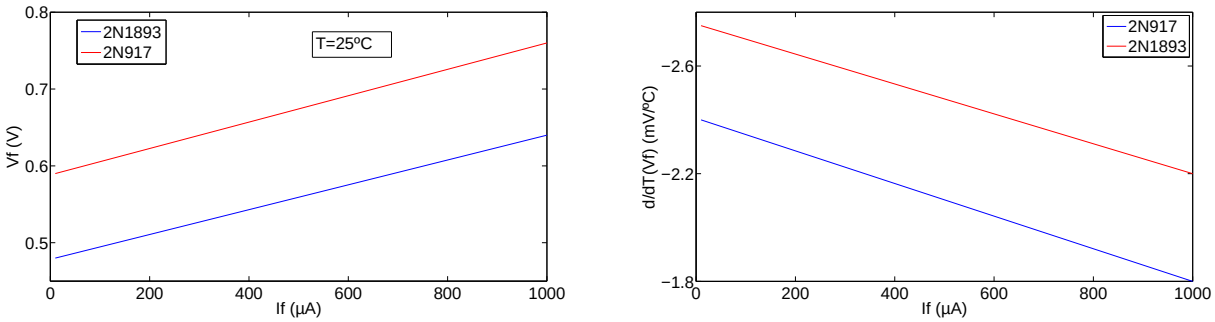

Figure 2.1: Forward voltage in order of current and temperature dependence of forward voltage in order of current in a diode configuration transistor.[Hil64]

Those different types of transistor have the same behaviour with different magnitudes, that is due to the emitter junction impurities that varies in those transistors affecting the forward voltage. In Fig. 2.1 the emitter current is represented, but if the gain is high, $I_B << I_C$, it is possible to consider by approximation $I_E = I_C$.

It is known that:

$$n_i^2 = C_0 T^3 \exp^{(\frac{-E_G}{kT})} \tag{2.4}$$

Thus,

$$I_S = qn_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) \tag{2.5}$$

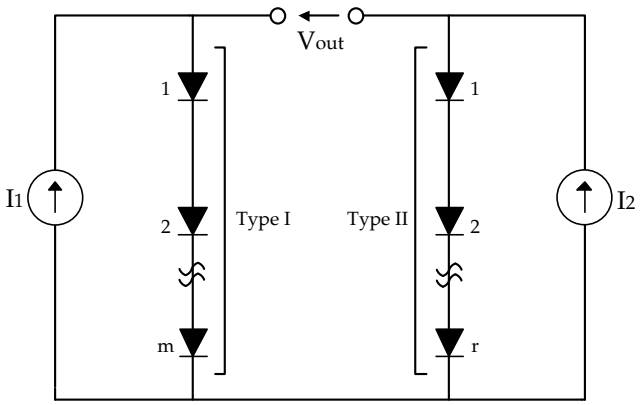

Figure 2.2: The basic circuit of the reference voltage source [Hil64].

which becomes,

$$I_S = C_1 T^{\beta_p} \exp^{(\frac{-E_G}{kT})} \tag{2.6}$$

for a p^+n junction and

$$I_S = C_2 T^{\beta_n} \exp^{(\frac{-E_G}{kT})} \tag{2.7}$$

for a n^+p junction.

As seen in Fig. 2.2, V_{out} is given by the difference between V_{BEm} and V_{BEr}. Eq. 2.10 shows the simplification of V_{out} equation. Where θ is represented in eq. 2.8 and ϕ is represented in eq.2.9.

$$\theta = r \ln \frac{I_{C2}}{I_{S2}(T0)} - m \ln \frac{I_{C1}}{I_{S1}(T0)} \tag{2.8}$$

$$\phi = r\beta_{II} - m\beta_I \tag{2.9}$$

$$V_{out} = \frac{KT_0}{q}\left[\theta + \left(\theta - \phi - \frac{E_{G0}}{kT_0}\right)\left(\frac{T}{T_0} - 1\right) - \frac{\phi}{2}\left(\frac{T}{T_0} - 1\right)^2\right] \tag{2.10}$$

Where E_{G0} is the energy gap voltage at 0°K. The voltage source used in the simulations introduces an error of 3 to 5 ppm and the diodes introduces an error of 150 ppm to 200 ppm. Those errors have origin in the type of material of the semiconductors.

To obtain a stable temperature point it is important to achieve a stable point which is the balance between the voltage drop of the resistor and the diodes or the MOS in diode configuration. The fig.2.3 shows the positive temperature dependency generated by the voltage between the two p-n junctions, which generate a proportional current that permits the creation of an equivalent voltage drop in the resistor. The figure also shows the negative temperature dependency generated by the V_{BE} voltage. The diodes have a negative dependency of the temperature decreasing 2.2mV/ºC[Raz02] and the resistor has the voltage drop generated by the current and an additional error as represented in eq.2.11.

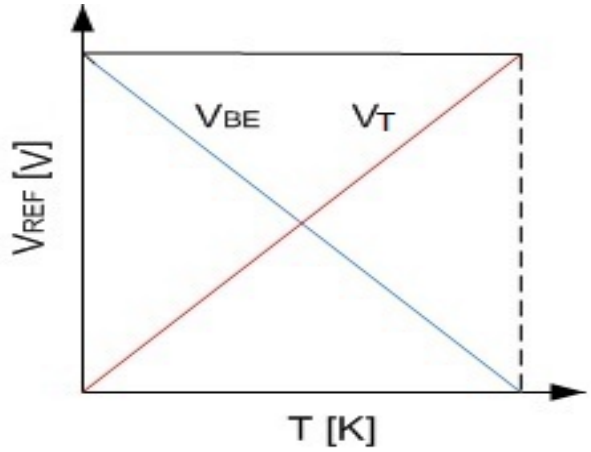

Figure 2.3: Temperature dependence of V_{BE} and Resistance with the graphics superimposed.

$$R = R_0[1 + \alpha(T - T_0)] \tag{2.11}$$

Where α is the temperature coefficient of the resistor.

The methodology described before is represented in fig.2.4, where the thermal voltage increases 0.086 mV/ºC and the V_{BE} decreases 2mV/ºC. The factor K is the multiplier for the ΔV_{BE} which will allow the variation of the proportional to absolute temperature voltage.

To demonstrate how a basic circuit works and understand how this balance between voltage drops in resistors and diode occur, the circuit in fig.2.5 was analyzed. The circuit shows in one side the voltage drop in V_{BE1} and on the other side a voltage drop in a resistor R and N*V_{BE2}. The current is assumed to be equal in both sides. The voltage drop in both V_{BE} is given in eq.2.12.

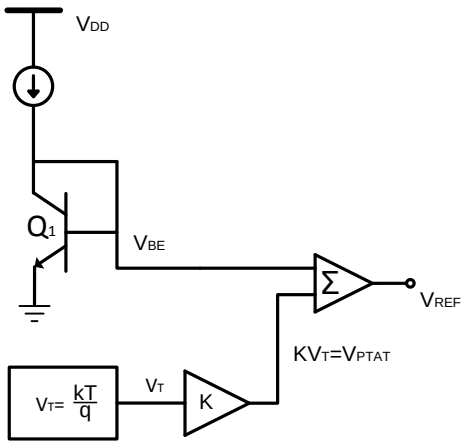

Figure 2.4: Block diagram of a bandgap voltage reference.[SH12]

$$V_{BE1} = nV_T ln\left(\frac{I_1}{I_S}\right) \tag{2.12}$$
$$V_{BE2} = nV_T ln\left(\frac{I_2}{NI_S}\right)$$

Assuming that the difference between V_1 and V_2 is null, it is possible to obtain eq.2.13.

$$V_{BE1} = RI_2 + V_{BE2} \tag{2.13}$$
$$RI_2 = V_{BE1} - V_{BE2}$$
$$RI_2 = V_T ln\left(\frac{NI_1}{I_2}\right)$$
$$Assuming\ ; I_x = I_1 = I_2,$$
$$I_x = \frac{V_T ln(N)}{R}$$

This demonstrate that the voltage drop in the resistor must be equal to the difference between V_{BE1} and V_{BE2}. As known, $V_T = \frac{kT}{q}$, where k is the Boltzmann Constant and q is the magnitude of the electrical charge on the electron which is also constant. Then, V_T is dependent of Temperature and the voltage drop is inversely dependent.

Another way to obtain the temperature voltage dependency is using MOS transistors, as shown in fig.2.6. The MOS transistors have a completely different behaviour, although if the MOS transistors operate on the weak inversion region, the function of the circuit is equivalent to eq. 2.14.

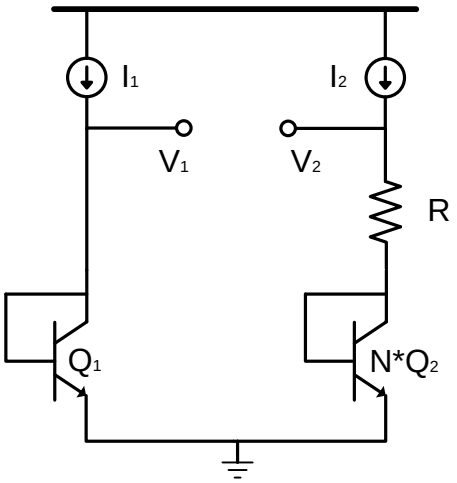

Figure 2.5: Basic circuit temperature-independent voltage operating with bipolar transistors.

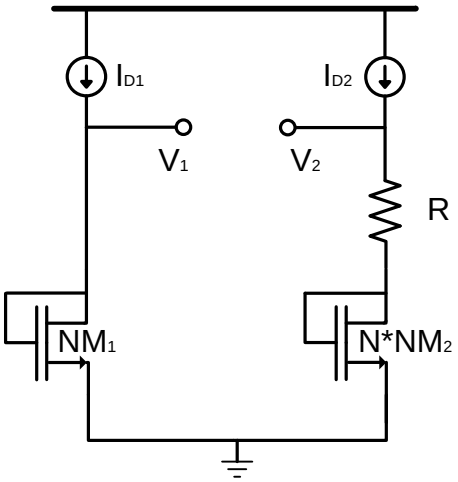

Figure 2.6: Basic circuit temperature-independent voltage using MOS transistors in the weak inversion region.

The mechanism of the bandgap circuit is very similar, but in this case the voltage drop will be V_{GS} instead of V_{BE}. The voltage drop in V_{GS} is shown in eq. 2.14

$$V_{GS1} = n\frac{kT}{q}ln\left(\frac{I_D}{A\mu_n C_{ox}(n-1)V_T^2}\right) + V_{THn} \tag{2.14}$$
$$V_{GS2} = n\frac{kT}{q}ln\left(\frac{I_D}{NA\mu_n C_{ox}(n-1)V_T^2}\right) + V_{THn}$$

Following the same steps as in circuit with bipolar transistors, the final equation is

obtained in eq.2.15.

$$
\begin{aligned}
V_{GS1} &= RI_2 + V_{GS2} \\
RI_2 &= V_{GS1} - V_{GS2} \\
RI &= V_T ln\left(\frac{NI_{D1}}{I_{D2}}\right) \\
Assuming\ ; I_x &= I_{D1} = I_{D2}, \\
I_x &= \frac{V_T ln(N)}{R}
\end{aligned}
\tag{2.15}
$$

As it is possible to observe, the equations 2.13 and 2.15 are equal. Although the transistors have different behaviours and different results as it will be shown next.

Next a few examples will be shown and compared, in order to conclude about the consumption, accuracy and other relevant factors of both.

2.2 Evolution of bandgap voltage reference circuits

After the study of Hilbiber, in 1971 Robert Widlar proposed the first bandgap circuit[Wid71]. As can be observed in fig. 2.7 the circuit developed by Widlar produced a voltage reference of 1.236 V with a variation of nearly 4 mV with a supply voltage of 7 to 9 V. Although it had poor performance, the main idea was there and a conventional bipolar bandgap reference circuit was created.

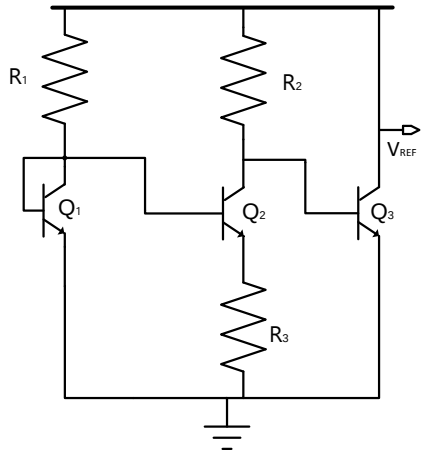

Figure 2.7: Low voltage reference in a simpler form.[Wid71]

Afterwards, in 1974 Brokaw developed a new voltage reference as shown in fig.2.8 with better performances namely the power dissipation, the voltage input and the current values, although the stability of the reference voltage deteriorated. This circuit works with an input voltage of 4 V generating a reference voltage of 2.5 V with an error of 2%.

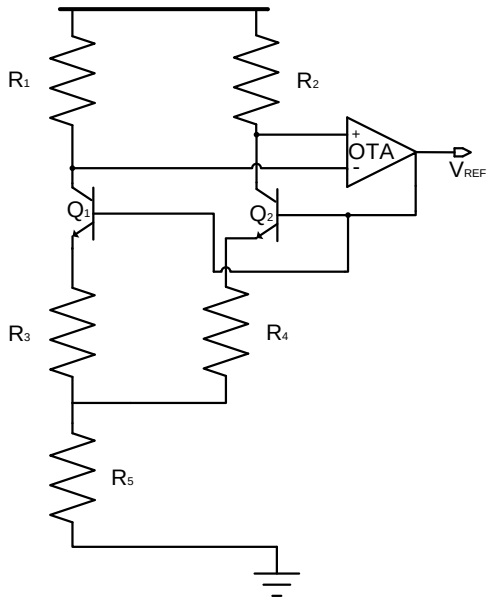

Figure 2.8: Low voltage reference developed by Brokaw.[Bro74]

2.2.1 Different Approaches on Voltage Reference Develop

During the development of a Voltage Reference Bandgap it is necessary to choose the elements of the circuit which guarantee a better performance and a low power dissipation. In this subsection it will be discussed the effects of the different elements in the circuit performance when applied to a conventional voltage reference circuit.

2.2.1.1 MOS vs Bipolar Transistors

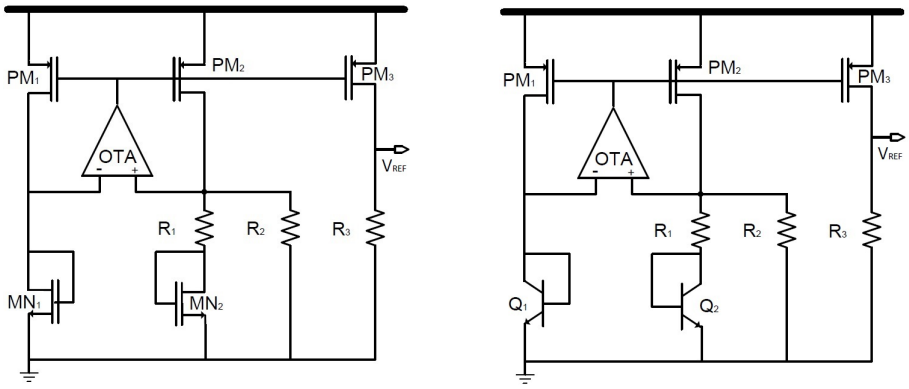

Figure 2.9: Conventional voltage reference circuit with (a) MOS transistors (b) Bipolar transistors.

Considering those two cases, primarily it is possible to verify that the second case needs a higher voltage supply. In order to guarantee the active zone of the transistors, at least 700 mV are needed for a bipolar transistor. Adding other elements, the supply voltage as to be at least 1 V. When using MOS transistors it is necessary to have a V_{DS}

higher than the V_{Dsat}, as known a MOS transistor only has a linear behaviour in the saturation zone. Usually circuits are developed with V_{Dsat} above 50 mV, in order to obtain a good margin. Comparing the voltage necessary to supply both transistors, it is possible to realize that MOS needs 14 times less voltage then the bipolar to conduct normally.

The equations of both circuits are similar as shown in eq. 2.16 and eq. 2.17. Considering that the voltage on the nodes A and B is equal due to the amplifier, it is possible to obtain the current flowing in resistor R_1 and R_2.

$$I_{R1} = \frac{V_{GS1} - V_{GS2}}{R_1} = \frac{\Delta V_{GS}}{R_1} \qquad (2.16)$$
$$I_{R2} = \frac{V_{GS1}}{R_2}$$

Assuming that the current that flows in point B is the reference, then

$$I_{REF} = I_{R1} + I_{R2}$$
$$V_{REF} = \frac{(\frac{W}{L})_{MP3}}{(\frac{W}{L})_{MP2}} R_3 \left[\frac{V_{GS1}}{R_2} + \frac{\Delta V_{GS}}{R_1} \right]$$

$$I_{R1} = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{\Delta V_{BE}}{R_1}$$
$$I_{R2} = \frac{V_{BE1}}{R_2}$$

$$Assuming\ the\ current\ that\ flows\ in\ point\ B\ is\ the\ reference\ then\ I_{REF} = I_{R1} + I_{R2}$$

$$V_{REF} = \frac{(\frac{W}{L})_{MP3}}{(\frac{W}{L})_{MP2}} R_3 \left[\frac{V_{BE1}}{R_2} + \frac{\Delta V_{BE}}{R_1} \right] \qquad (2.17)$$

Analysing the previous equations, it is possible to conclude that the difference between the two approaches has to be in the linearity of the coefficients of V_{BE} and V_{GS}. The temperature affects both V_DS and V_GS, which influences the current in the MOS transistors. In bipolar transistors only V_{BE} is affected.

2.2.1.2 MOS vs Resistor

As it will be seen next, some circuits do not use a resistor to measure the thermal voltage by the voltage drop. Those circuits also don't balance the Thermal voltage increase with the gate-source voltage to obtain V_{ref}. Instead the balance is made by summing the negative and positive gate-source voltage, allowing to obtain a stable V_{ref}.

This approach also do not need an amplifier which represents the major problem in reducing supply current value, so it use a supply current typically below 1μA, which is nearly impossible to obtain in a Bandgap with an ampop. On the other hand, in order to allow all the MOS transistors to work normally, the balance between the MOS transistors will force to increase the minimum voltage input, which as to be normally higher than 1

V.

As a result of this, the power consumption will be quite similar although the balance between gate-source voltages with source-gate voltages will allow a most stable voltage references.

2.3 CMOS Bandgap Voltage Reference Circuits Approaches

In this section, some examples of Bandgap Voltage Reference are presented. The circuits symbolize three different type of approaches. In the first, the use of Bipolar Transistors with some resistors to form the PTAT and CTAT voltages. In the second approach MOS transistors are used with some resistors to produce the same effect as in the first and in the last approach only MOS Transistors are used performing PTAT and CTAT by V_{SG} and V_{GS} respectively.

2.3.1 A Sub-1 V MOS Bandgap Reference

In this subsection the Bandgap Voltage Reference with current mode structure (fig. 2.10) using Bipolar Transistors to generate the PTAT and CTAT voltages will be used.

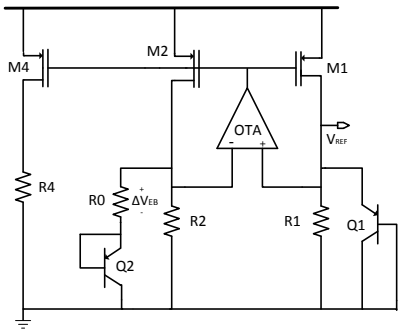

Figure 2.10: Bandgap reference with current mode structure [LY09].

The concept of this circuit is using two different currents, which are proportional to V_{BE}(CTAT) and V_T(PTAT). The PMOS transistors have the same lengths and the resistors R1 and R2 the same value, the use of an amplifier will force an equal voltage in the inputs. Using the current mirror will force the currents that flows in PM1, PM2 and PM4 transistors to be the same. Then, it is possible to obtain eq.2.18 and eq.2.19.

$$I_4 = I_1 = I_2 = \frac{V_{EB1}}{R_1} + \frac{V_T ln(N)}{R_0} \tag{2.18}$$

$$V_{REF} = I_4 R_4 = \frac{R_4}{R_1}\left(V_{EB1} + \frac{R_1}{R_0} V_T ln(N)\right) \tag{2.19}$$

Adjusting the values of the resistors ratio and the value N (multiplier of the transistor) it is possible to obtain a stable Voltage Reference value.

Another aspect to consider is the minimum voltage supply of the circuit and it is possible to calculate the value by eq.2.20.

$$minV_{DD} = \{max\{V_{REF} + V_{SDsat}, V_{EB1} + |V_{TP}| + 2V_{SDsat}\}\} \tag{2.20}$$

The minimum value for the voltage supply in this circuit will be round 900 mV. In this case, after the curvature compensation the circuit produced a V_{REF} of 635 mV, adding the 50 mV equivalent of the V_{SDsat}, the obtained value would be 685 mV. As known, to supply a V_{EB1} a minimum of 700 mV is required, so adding the $|V_{TP}|$ and $2V_{SDsat}$ the minimum of 900 mV are obtained for the voltage supply. The circuit performance is presented in table 2.1.

Parameter	**Value**
Supply Voltage	1.2V
Technology	0.13-μm MOS
Power Consumption at 27°C	29.2μW
Reference Voltage at 27°C	634.93 mV
TC(-40°C<T<125°C)	7.93 ppm
Minimum operating voltage	800 mV
Gain and Phase Margin	85 dB, 80°C

Table 2.1: Performance summary of the bandgap[LY09]

2.3.2 Bandgap Voltage Reference for 1.1V Supply in Standard 0.16 μm MOS

In 2012, another approach was used by Annema and Goksu. The most important goal of this circuit was to decrease the occupied area by the circuit to a minimum value, maintaining interesting results in terms of linearity. Consequently the use of opamps, high ohmic resistors or multiple diodes is not allowed.

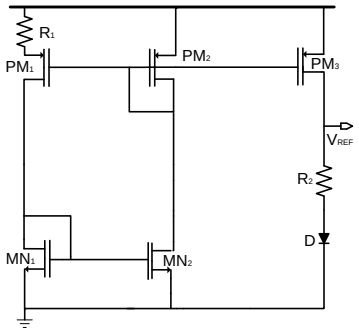

Figure 2.11: Schematic of the are efficient low-power sub-1 V BGVR circuit [AG12].

In the circuit shown in 2.11, it is assumed that the PMOS PM1 and PM2 are in weak inversion with exponential behaviour. Then, a PTAT voltage is defined by the ratio between the resistors R_1 and R_2 and by the ratio between the current factors of PM1 and PM2. The CTAT voltage is defined by the voltage drop in the diode. The voltage reference is represented in eq.2.21.

$$V_{REF} = \frac{kT}{q} N ln(A) + \frac{kT}{q} ln\left(\frac{I_C(T)}{I_{C,0}T^{\eta}}\right) + V_{gap,0} \tag{2.21}$$

In order to adjust the voltage reference to the limit, a fixed gap between V_{T1} and V_{T2} is added. This gap is adjusted by the variation of the gate length of the transistors as presented in fig.2.12. The small gate length in PM1 will traduce in a higher value for V_{T1} due to the short channel effect and a larger gate length will traduce in a shorter V_T2 as it is shown in fig.2.12. As known V_T has a positive TC, so it is added to eq.2.21, as seen in eq.2.22.

$$V_{REF} = N\left[\frac{kT}{q} ln(A) - \Delta V_T\right] + \frac{kT}{q} ln\left(\frac{I_C(T)}{I_{C,0}T^{\eta}}\right) + V_{gap,0} \tag{2.22}$$

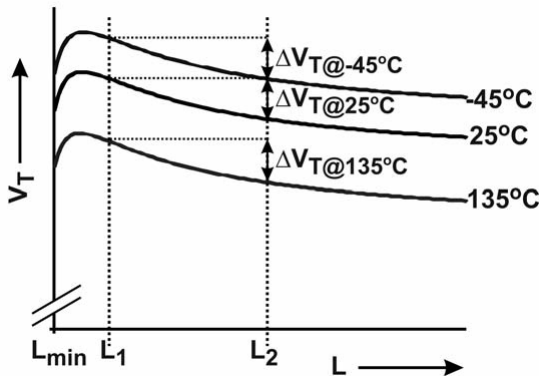

Figure 2.12: Threshold-voltage dependency on transistor length [AG12].

Afterwards, regulated cascodes were inserted in the circuit resulting in the performance of the circuit, shown in tab.2.2. Although this circuit has a low current value, it only works with a supply voltage above 1.1 V.

2.3.3 Voltage Reference Circuit Consisting of Subthreshold MOSFETs

A new approach appeared in the last years, the idea is to develop a bandgap voltage reference circuit without resistors or bipolar transistors. The main idea is to balance the V_{GS} forming the CTAT voltage with V_{SG} formed by the PTAT voltage.

The circuit is divided in 2 parts, the part of the current source subcircuit and a bias voltage subcircuit.

Parameter	**Value**
Supply Voltage	>1.1V
Technology	0.16-μm MOS
Current Supply at 27°C	1.4μA
Reference Voltage at 27°C	944 mV
TC(untrimmed)(-45°C<T<135°C)	30 ppm/°C
Area	0.0025mm^2

Table 2.2: Performance summary of the bandgap[AG12]

The current source circuit is a self-biasing circuit that uses a PMOS resistor instead of resistors. This part also generates the current I_P. The part of the bias voltage circuit is composed by the transistor M4 and 2 coupled pairs(M3-M6 and M5-M7). All MOSFETs are in subthreshold region, excepting MR1 that operates in strong-inversion. This circuit combines 2 PTAT voltages with 2 CTAT voltage, as demonstrated in eq.2.3.3.

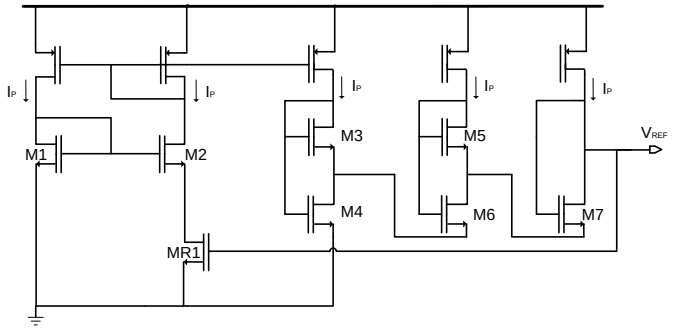

Figure 2.13: Schematic of Reference Voltage[KUA09].

$$
\begin{aligned}
V_{REF} &= V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \\
&= V_{GS4} + \eta V_T ln\left(\frac{2K_3K_5}{K_6K_7}\right) \\
&= V_{TH} + \eta V_T ln\left(\frac{3I_P}{K_4I_0}\right) + \eta V_T ln\left(\frac{2K_3K_5}{K_6K_7}\right)
\end{aligned}
\tag{2.23}
$$

As known, the thermal voltage V_T has a positive TC and the threshold voltage V_{TH} has a negative TC. Adjusting the sizes of transistors is it possible to obtain a stable voltage reference.

As known, V_{GS} has coefficients with a worst linearity than V_{BE}, consequently the TC error of the circuit should be larger, instead of this V_{GS} cancels each other non linearity factors. Although the circuit works with supply voltages below 1 V, as shown in fig. 2.14, in the table is represented a minimum voltage supply of 1.4 V. Probably with a shorter voltage supply the TC error will be larger, in table Tabletab3 is represented the circuit

performance.

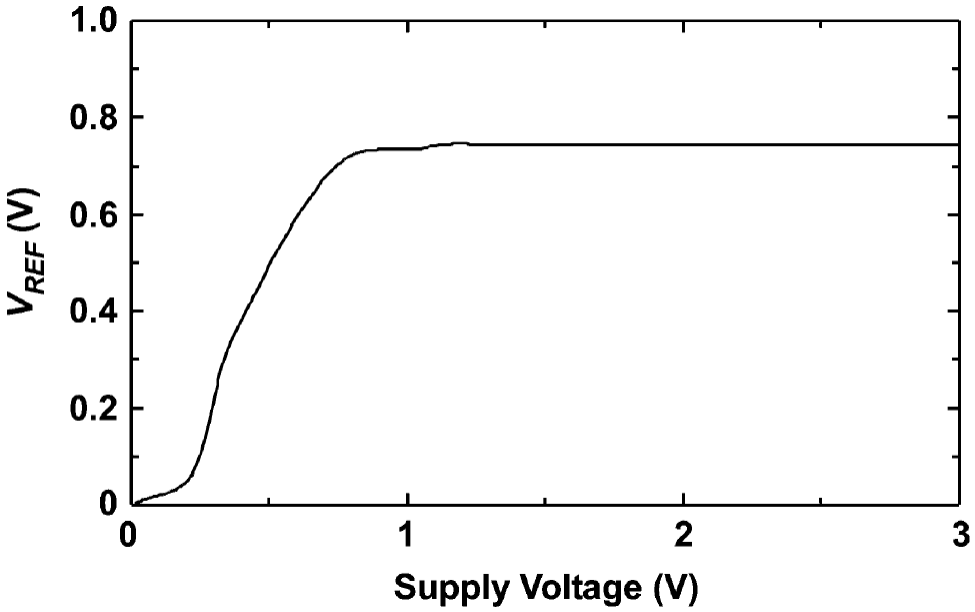

Figure 2.14: Voltage Reference as function of voltage supply[KUA09].

Parameter	**Value**
Supply Voltage	1.4 V - 3 V
Technology	0.35-μm MOS
Power Supply at 27ºC	0.3μW
Reference Voltage at 27ºC	745 mV
TC(untrimmed)(-20ºC<T<80ºC)	7 ppm/ºC
PSRR	-45 dB (@100 Hz)
Area	0.055mm^2

Table 2.3: Performance of the bandgap[KUA09]

3

Proposed Low Voltage CMOS bandgap circuit

3.1 Overview

After the presentation of the different approaches to develop a bandgap, the main goal was to obtain the minimum supply voltage possible. In order to achieve a low power consumption, the supply current was also reduced to the minimum value. As seen in chapter 2, in order to obtain interesting values for the supply voltage, the bipolar transistors weren't used in the design of the circuit. In this chapter, the development of the circuit is divided in different parts:

- Bandgap;
- Amplifier;
- Temperature Sensor.

In fig.3.1 is represented the block diagram of the temperature sensor.

In fig.3.2 is represented the functional scheme of the circuit, divided in 3 major blocks:
- Bandgap Voltage Reference;
- Analog-to-digital converter;
- Control.

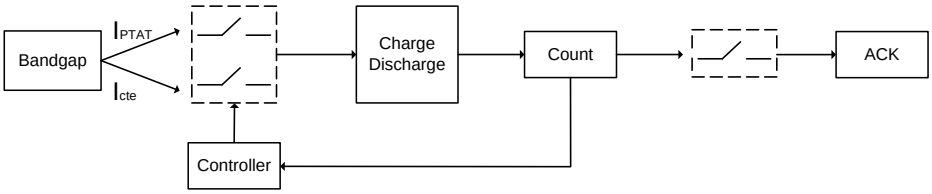

Figure 3.1: Temperature sensor scheme.

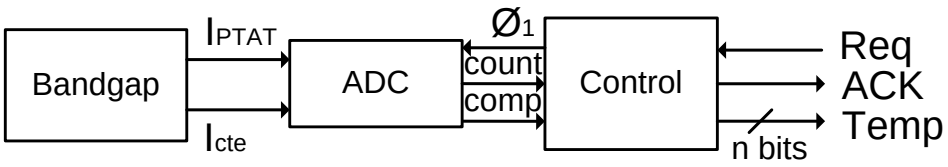

Figure 3.2: Functional scheme of the temperature sensor.

To resume the scheme, initially the control produce a request as an input to receive a temperature output, then the control sends a signal to start the count in the ADC. The PTAT current is routed to the integrating capacitor, finalizing the count, the control sends a signal to change the integrating current to constant. The comparison with zero is made, the signal is send to the control which switch the interrupter and send as output the n_{bits} counted and the acknowledgement.

3.2 Bandgap Voltage Reference

In this section core of the bandgap circuit design will be presented. As mentioned before, the transistors used in this circuit were all MOS to decrease the circuit power dissipation. The op-amp (AMPOP) is inserted in the circuit in order to force the same voltage working as a current mirror in the nodes A and B. The transistors M_7, M_8 and M_9 work in weak inversion and M_1 to M_6 in saturation mode. The current of I_3 is controlled by the resistors R_1 and R_2 as demonstrated in eq. 3.1.

$$V_A = V_B \tag{3.1}$$
$$I_2 = I_{R1} + I_{R2}$$

As referred before transistors M_7, M_8 and M_9 work in weak inversion, in those cases the current that flows varies exponentially with V_{GS} as shown in eq. 3.2.

$$\begin{aligned} I_{DS} &= I_{D0} e^{\frac{V_{GS}-V_{TH}}{nV_T}} \\ where, I_{D0} &= I_t \frac{W}{L} \\ and, I_t &= 2n\tau_n C_o x \left(\frac{kT}{q}\right)^2 \\ V_{GS} &= nV_T ln\left[\frac{I_{DS}L}{I_t W}\right] + V_{th} \end{aligned} \tag{3.2}$$

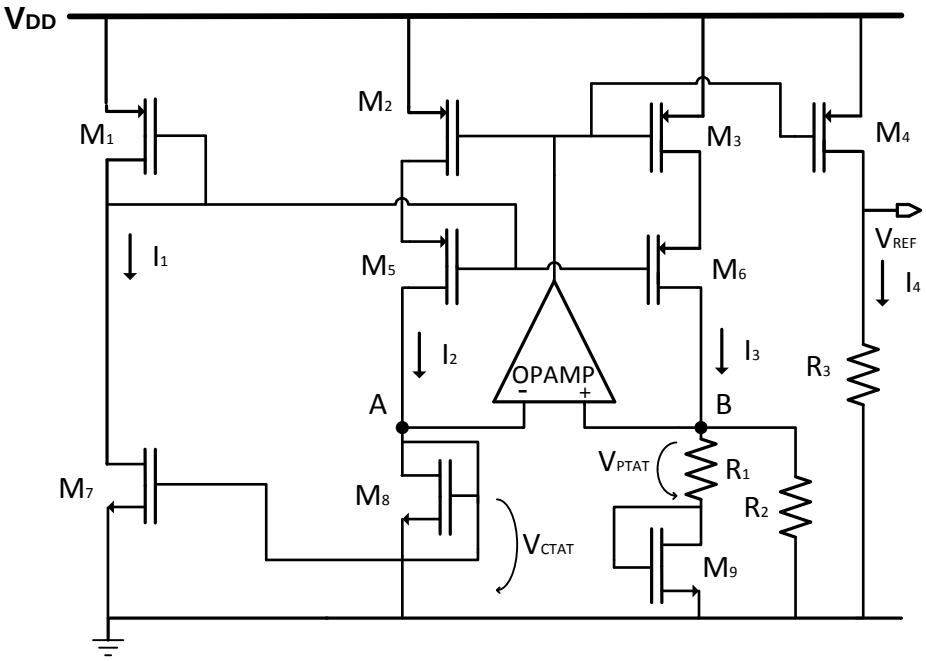

Figure 3.3: Reference voltage circuit designed.

Differentiating V_{GS} in order of temperature as showed in eq. 3.3, it is possible to conclude that V_{GS} varies negatively with the temperature increase.

$$\frac{\partial V_{GS}}{\partial T} = \frac{V_{GS}}{T} - 2n\frac{k}{q} \tag{3.3}$$

As known, k is the Boltzmann's constant($1.38 * 10^{-23}$J/K) and q is the magnitude of electron charge($1.6 * 10^{-19}$C), differentiating the V_T in order of temperature as presented in eq. 3.4.

$$\frac{\partial V_T}{\partial T} = \frac{k}{q} = \frac{1.38 * 10^{-23} J/K}{1.6 * 10^{-19} C} = 0.086 mV/^{o}C \tag{3.4}$$

In this circuit, the design methodology used is similar as the ones described in chapter 2

as demonstrated in eq. 3.5.

$$V_{CTAT} = V_{R2} = V_{GS8} = nV_T ln\left[\frac{I_{DS8}L_8}{I_t W_8}\right] + V_{th}$$

$$V_{GS9} = nV_T ln\left[\frac{I_{DS9}L_9}{I_t W_9}\right] + V_{th}$$

$$V_{GS8} = V_{R1} + V_{GS9}$$

$$V_{PTAT} = V_{R1} = \Delta VGS = n\frac{nKT}{q} ln(m)$$

$$where\ m\ is\ the\ ratio\ between\ the\ lengths\ of\ M_8\ and\ M_9,$$

$$I_{R1} = n\frac{V_T}{R_1} ln(m)$$

$$I_{R2} = \frac{V_{GS8}}{R_2} = \frac{V_B}{R_2} = \frac{V_A}{R_2}$$

$$I_1 = I_2 = I_3 = \frac{V_A}{R_2}$$

$$V_{REF} = \left[\frac{V_{GS8}}{R_2} + n\frac{nkT}{qR_1} ln(m)\right] R_3 \tag{3.5}$$

The most important step in this circuit is the insertion of a current mirror in order to obtain the minor error between I_1 and I_2. This step allows the circuit to work with a power supply voltage source of 500 mV and guarantee a larger voltage range to obtain the most stable V_{REF}.

3.3 Operational Amplifier

In the previous analysis, it was assumed that the reference voltage was being simulated using an ideal amplifier with a gain of 1000. Therefore, a low power MOS operational amplifier was designed in order to obtain a large gain value and a phase margin of 60º. The schematic of this operational amplifier is represented in fig.3.4.

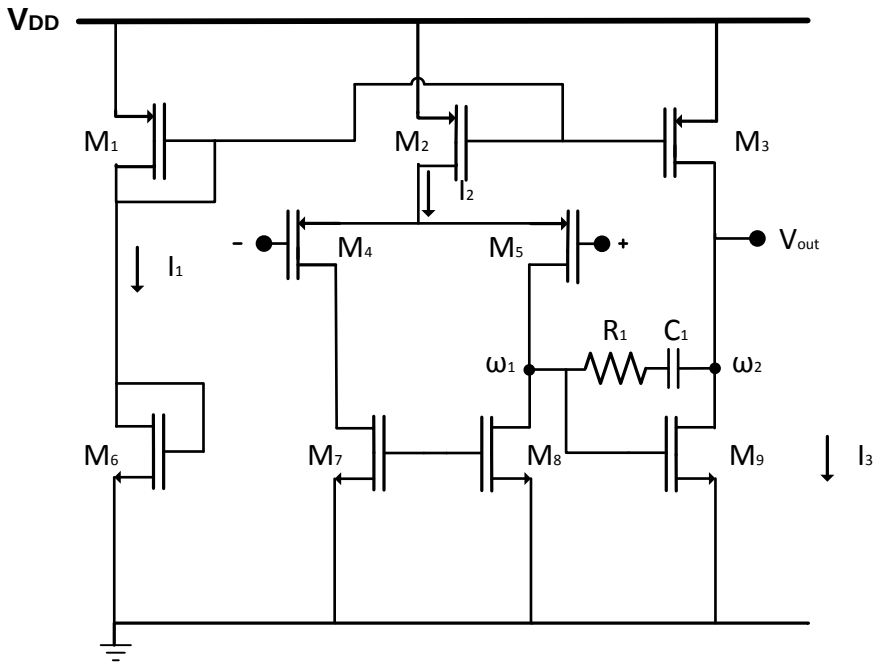

Figure 3.4: Low power CMOS operational amplifier.

With the transistors operating on the saturation mode, the drain current is controlled by V_{GS} and is less dependent of the drain voltage. The expression is represented in eq. 3.6.

$$
\begin{aligned}
I'_{D(Sat)} &= \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS}) \\
I'_{D(Sat)} &= I_{D(Sat)}(1+\lambda V_{DS}) \\
I_{D(Sat)} &= \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2
\end{aligned}
\tag{3.6}
$$

In order to calculate the gain, it is necessary to obtain the transconductances(gm) and the common source output conductance(Gds) of each transistors. Through eq. 3.6 and eq. 3.7, the calculation of Gds and gm of each transistor is represented in table 3.1. [PA09] As known to 130nm CMOS technology,

$\mu_n = 259.530 * 10^-4m^2/Vs$

$\mu_p = 109.976 * 10^-4m^2/Vs$

$t_{ox} = 4.1 * 10^-9m$

$\epsilon ox = 3.97 * 8.854 * 10^-12F/m$

$Cox = \epsilon ox/t_{ox} = 8.57 * 10^-3F/m^2$

$$\lambda = \frac{I'_{D(Sat)-I_{D(Sat)}}}{V_{DS}I_{D(Sat)}}$$
$$Gds = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{I'_{D(Sat)-I_{D(Sat)}}}{V_{DS}} = \lambda I_{D(Sat)}$$
$$gm = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{2I_D}{V_{GS} - V_{TH}} \tag{3.7}$$

Gds/gm	**Value**
gds_3	$7.317 * 10^{-8}$
gds_5	$2.7138 * 10^{-7}$
gds_8	$1.97607 * 10^{-7}$
gds_9	$1.12598 * 10^{-7}$
gm_5	$3.19 * 10^{-5}$
gm_9	$5.524 * 10^{-6}$

Table 3.1: gds's and gm's in transistors M_3, M_5, M_8 and M_9.

Replacing the values calculated above, the circuit's gain is represented eq. 3.8.

$$A_v = 2gm_5(rds_5//rds_8)gm_9(rds_3//rds_9)$$
$$A_v = 4045.2246$$
$$=> A_v(dB) = 20log_{10}(4045.2246) = 72.14dB \tag{3.8}$$

A phase margin of 60 degrees will be considered, in order to obtain a stable amplifier. A lower phase margin will increase the peak in response of a pulse, inversely a faster phase margin will decrease the response to a pulse and increase the time to rise the step final value. [War96]

$$\omega_1 = \frac{1}{gm_5 * (rds5//rds_8) * (rds_3//rds_9) * C_C}$$
$$\omega_1 = 588.6Hz \tag{3.9}$$

$$C_1 = C_{db5} + C_{db8} + C_{gs9}$$
$$C_2 = C_{db9} + C_{db3} + C_{gd3} + C_L$$
$$\omega_2 = \frac{gm_9}{C_1C_2 + C_2C_C + C_1C_C}$$
$$\omega_2 = 35.8MHz \tag{3.10}$$

Where C_L is the capacitance seen by the device driving the load, C_{db} the parasitic capacitances between drains and bulks, C_{gs} the parasitic capacitance between gate and source and C_{gd} the parasitic capacitance between gate and drain. Due to the short distance between the two poles, the compensation capacitor was inserted (C_C), moving the first pole to lower frequency and the second pole to higher frequencies.[Goe10]

$$\omega_z = -\frac{1}{(\frac{1}{gm_9} - R_C)C_C}$$
$$\omega_z = -958,38MHz \tag{3.11}$$

The R_C is the compensation resistance which allow to move the zero to a position where it doesn't interferes with the high gain pole and the phase margin. As shown in eq. 3.11 the zero value is distant of the second pole value, however at high temperatures the non influence of the zero in the phase margin is not guaranteed.

Consequently, the gain-bandwidth product is, represented in eq. 3.12.

$$GBW = \frac{gm_5}{C_C}$$
$$GBW = pole_1 A_v = \frac{1}{gm_5(rds_5//rds_8)(rds_3//rds_9)C_C} gm_1 gm_2 R_1 R_2 = \frac{3.19 * 10^{-5}}{2.68 * 10^{-12}}$$
$$GBW = 6.88MHz \tag{3.12}$$

Posteriorly the comparison with the real values will be made.

3.4 Temperature Sensor

In addiction to the voltage reference circuit, a temperature sensor was developed. The temperature sensor produces a digital output code that is proportional to the temperature. The main goal is to achieve the maximum linearity in the temperature curve and to obtain the most approximated value in the range of values.

The state diagram is represented in fig. 3.5. Using the PTAT current, which is a theoretical linear increasing curve with temperature and a constant current with temperature, the reference current. The 2 currents were mirrored and controlled through logic gates. The main idea was to initially insert the proportional to temperature current. During the counting the capacitor is charged and a linear increasing voltage curve will be generated. After counting 2^{nbits} clock periods, the constant current will be inserted in the circuit, inverting the two switches. The capacitor will discharge and its voltage will decreases until this voltage reaches zero. Reaching zero, the switch in the capacitor will be activated and the capacitor will stop discharging, generating a constant zero voltage. In fig.3.5 a state

diagram is represented.

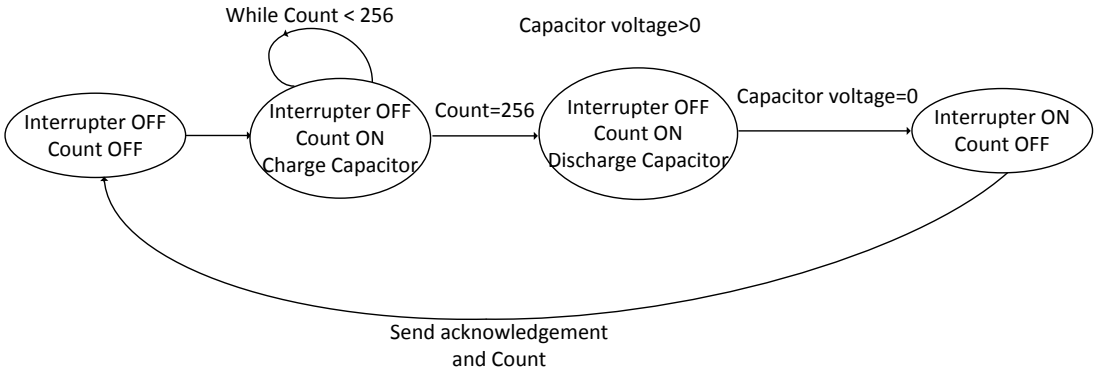

Figure 3.5: Temperature sensor state diagram.

This ADC has the same effect has a double ramp ADC, as consequence of this state diagram the theoretical result is represented in fig.3.6. The 3 main states are presented with the respective working parts highlighted in the circuit. Analysing the figure, it is exposed that the increasing curve represented is the PTAT current flowing in the circuit. The figure peak represents the final count of the 256 periods and the activation of the interrupt and consequently insertion of the constant current in the circuit. Reaching zero, the circuit resets.

The equation 3.13 is used to size the circuit and obtain the maximum performance.

$$\begin{aligned} T_{CLK} &= \frac{T_{int}}{n^{bits}} \\ V_{peak} &= \frac{I_{CTE}}{C} T_{int} \end{aligned} \tag{3.13}$$

The current value jointly with the capacitor value and the integration time, which is defined by the clock time and the number of bits in the counter. Theoretically considering:
- T_{CLK}=500 ns;
- I_{CTE}=200 nA;
- C=100 pF.

$$\begin{aligned} T_{int} &= T_{CLK} n^{bits} \\ T_{int} &= 1 * 10^{-6} 256 = 0.256ms \\ V_{peak} &= \frac{I_{CTE}}{C} T_{int} \\ V_{peak} &= \frac{I_{CTE}}{C} T_{int} = \frac{200 * 10^{-9} 0.128 * 10^{-3}}{100{*}10{-}12} = 256mV \end{aligned} \tag{3.14}$$

The values obtained in eq. 3.14 were considered as the objective while designing the temperature sensor.

In the discharge part of the capacitor, the calculation process is represented in eq.3.15.

$$\begin{aligned} V_{peak} &= \frac{I_{PTAT}}{C} T_{int} \\ V_{peak} &= \frac{I_{CTE}}{C} N * T_{clk} \\ \frac{I_{CTE}}{C} N * T_{clk} &= \frac{I_{PTAT}}{C} T_{int} \\ I_{CTE} N &= 256 I_{PTAT} \\ N &= \frac{256 I_{PTAT}}{I_{CTE}} \end{aligned} \tag{3.15}$$

The N parameter represents the digital code which varies with the temperature that is represented in the equation by the PTAT current parameter. That N factor corresponds to a certain point in which the voltage achieves 0 volts($t_{discharge}$).

The $t_{discharge}$ is calculated in eq. 3.16.

$$T_{discharge} = T_{charge} \frac{V_{PTAT}}{V_{CTE}} \tag{3.16}$$

The equation demonstrates the $t_{discharge}$ is directly proportional to the PTAT voltage which is proportional to the temperature.

In fig. 3.7 is represented the temperature sensor, which includes the sensor, the counter and the comparator. The designed counter is a 8-bit synchronous counter. Although the synchronous counter as a great consumption, the precision is compensates this fact. The 8-bit synchronous counter performs operations based on every clock tick, in other hand the asynchronous counter can propagate errors. In an asynchronous counter, the forward JK flip-flop only receive a clock when the previous state passes the value zero. In the synchronous counter, all the JK flip-flops receive constantly clocks, forcing the count to be correct, but dissipating more power.

In fig.3.9 is represented the various 3 input AND, in which is inserted a 2 input NAND, a 3 input NAND with an inverter. As known, the NAND logic output only returns zero when all the inputs are "high" (1). The different inputs are connected to the gates of the transistors M_1/M_5, M_2/M_6 and M_3/M_7, If all the PMOS transistors receive "high" (1) in the gates, then they won't conduct and the output will be zero. if only one of those signals takes the value zero, then one of the PMOS will conduct and the output will be "high" (1).

In the inverter, the signal received from the NAND output enters in M_4 gate, and if the signal is "high" (1) the transistor does not conduct providing a 0 output. Contrarily if the M_4 gate receives zero, the transistor will conduct and the output will be "high" (1).

In fig.3.10 is represented the JK flip-flop scheme, which applies the logic gates represented in fig.3.9, the objective was to obtain the state table represented in tab.3.2.

J	**K**	Q_{next}
0	0	Q
0	1	0
1	0	1
1	1	Q_{neg}

Table 3.2: JK flip-flop state table.

In this case the main objective of the JK flip-flop is to toggle the state. This change of state is coordinated by the clock frequency and changes the output to the opposite value entry.

A comparator was also developed in order to detect the moment when the zero voltage is reached. The main objective is to control the switch and activate it in order to reject voltages below zero voltage, this information will help verifying the linearity of the circuit and posteriorly will sent as acknowledgement.

The comparator is based on the amplifier used in the bandgap voltage reference, the widths and lengths were changed in the transistor in order to achieve the desired gain and detect the interception of the voltage in zero. The compensation capacitor and the compensation resistor were removed to improve the time response of the comparator and decrease the time response to the moment when the voltage in the capacitor reach zero volts.

As an addition to the amplifier 2 inverters were inserted to increase the gain of the amplifier and detect more precisely the moment when the voltage is zero.

The transistors of the interrupter were also sized to detect faster and efficiently the interception. The logic used in this case is simple, the comparator inputs were placed in the polarity of the capacitor, in order to detect when the difference between them is zero. When achieved the zero value, the comparator outputs zero directly to the PMOS transistor and "high" (1) to the NMOS transistor of the interrupter. The output will set on the interrupter and stop the discharge in the capacitor.

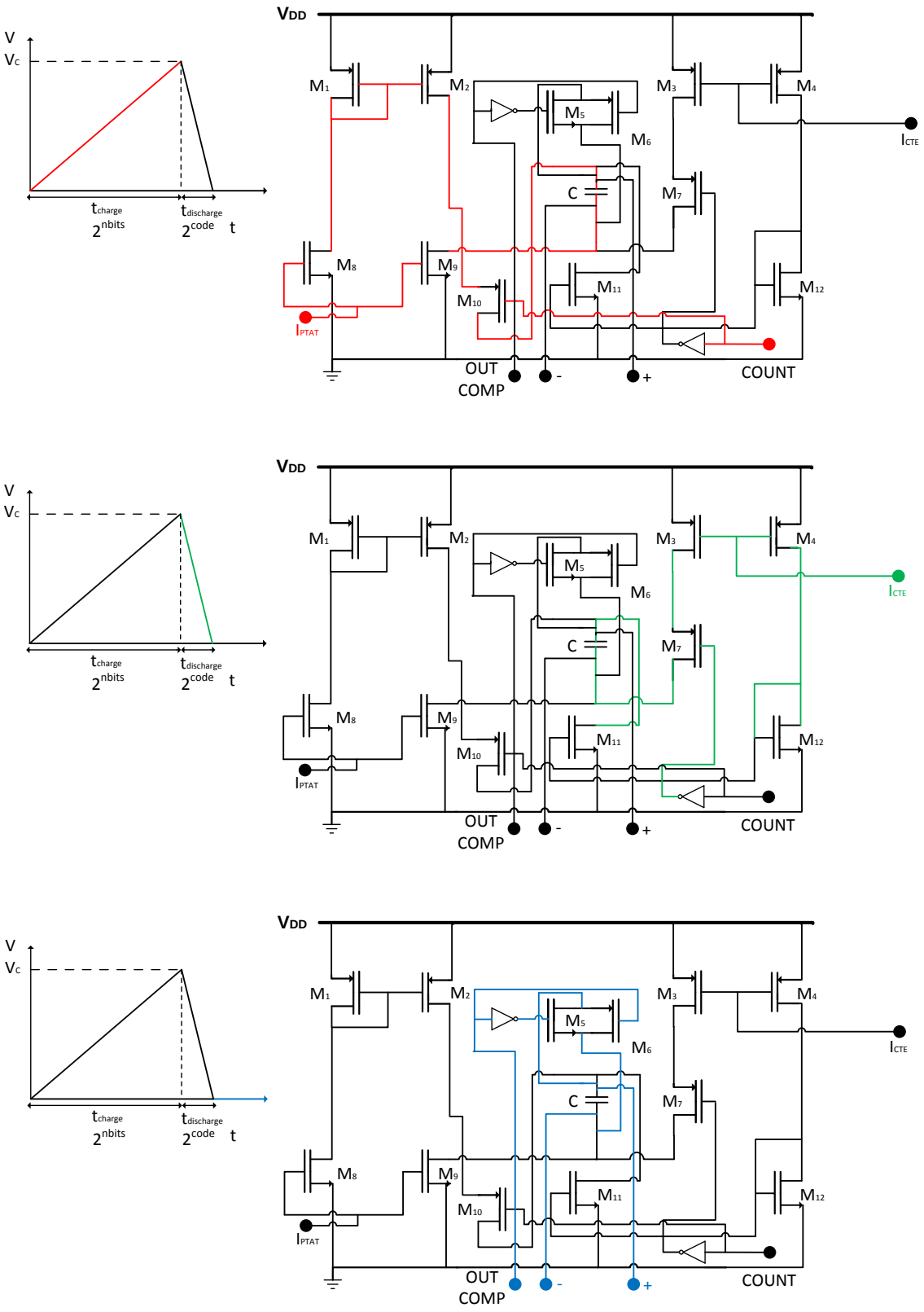

Figure 3.6: Theoretic operation of the proposed ADC.

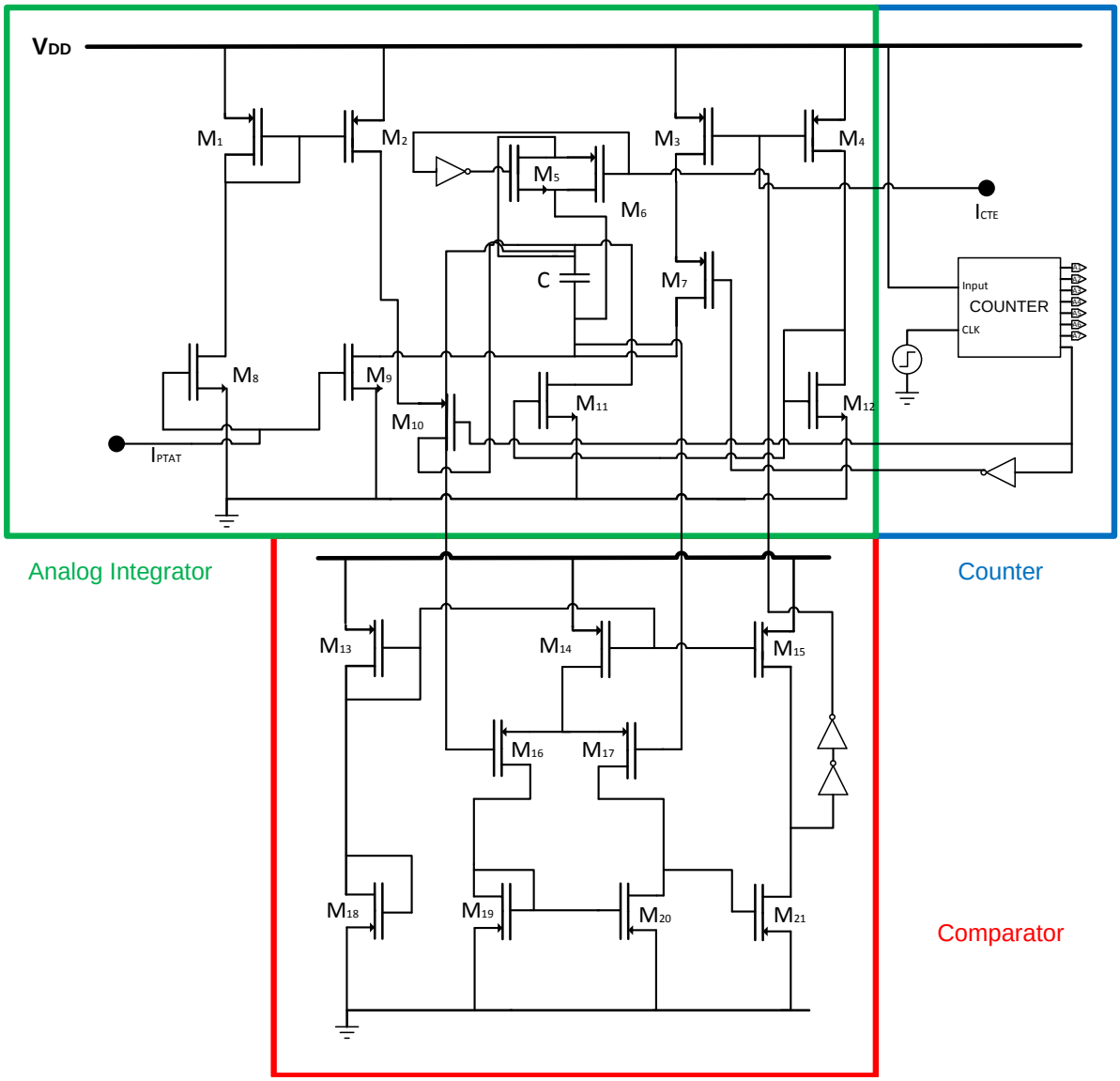

Figure 3.7: Temperature sensor scheme.

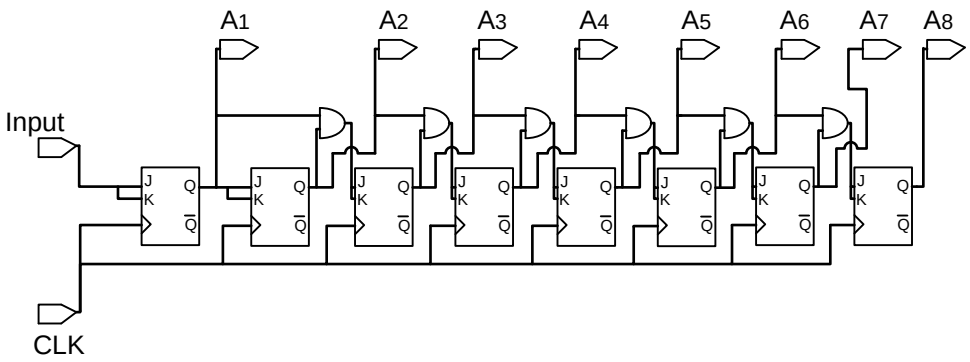

Figure 3.8: Synchronous 8-bit counter scheme.

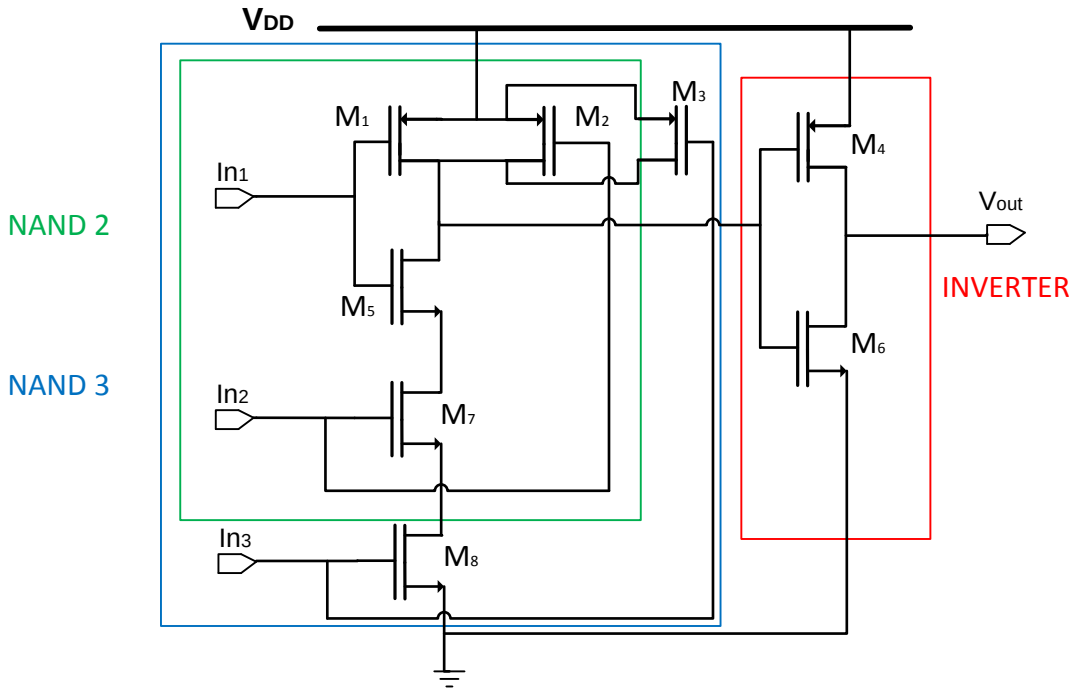

Figure 3.9: 3 input And scheme.

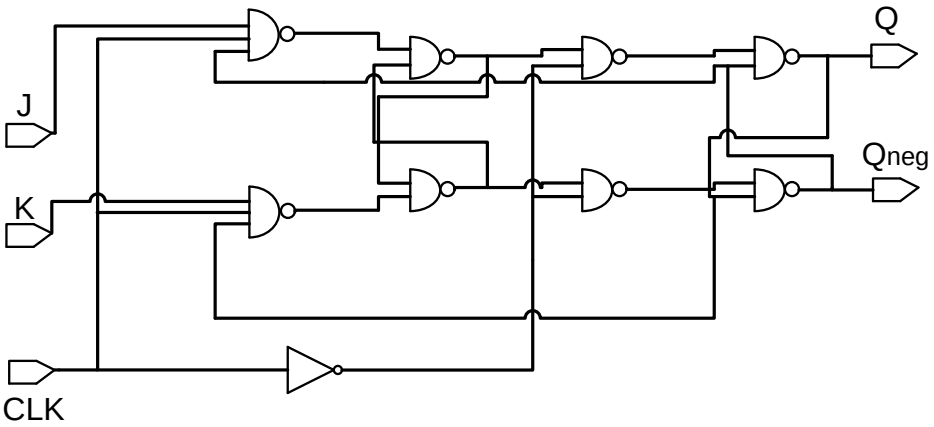

Figure 3.10: J-K flip-flop scheme.

4

Simulation results

4.1 Bandgap Voltage Reference

All the simulations were realized with Cadence software(Spectre-Virtuoso), using the models from the 0.13 μm CMOS technology. All the PMOS bulks were connected to V_{DD} and the NMOS bulks were connected to ground.

The input voltage (V_{DD}) was set to 500mV, assigning a great importance in this particular performance. After the calculations to size the transistors and resistors, represented in tab. 4.1. The main objective at this point was to obtain the most stable V_{REF} balanc-

Component	W/l
M_1	$1\mu/2\mu$
M_2	$4\mu/2\mu$
M_3	$4\mu/2\mu$
M_4	$1\mu/2\mu$
M_5	$20\mu/1\mu$
M_6	$20\mu/1\mu$
M_7	$4\mu/2\mu$
M_8	$10\mu/2\mu$
M_9	$102\mu/2\mu$
R_1	$65k\Omega$
R_2	$475k\Omega$
R_3	$400k\Omega$

Table 4.1: Bandgap voltage reference component values.

ing the proportional to absolute temperature(V_{PTAT}) and the complementary to absolute

temperature(V_{CTAT}). Those voltages are shown in fig.4.1.

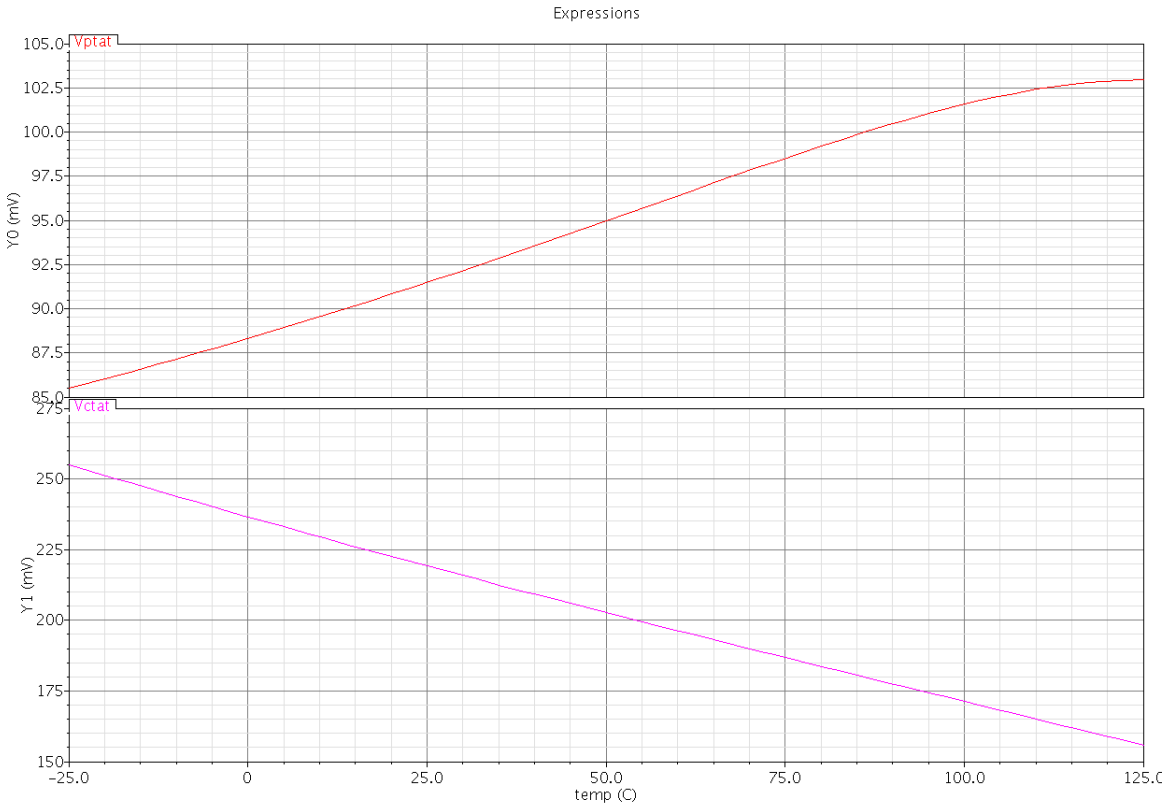

Figure 4.1: Proportional to absolute temperature and complementary to absolute temperature.

As showed in the previous chapter the reference voltage depends of the PTAT current and CTAT current, where PTAT current is the ratio between PTAT voltage and R_1 and the CTAT current is the ratio between CTAT voltage and R_2. Adjusting the resistors R_1, R_2 and the $\frac{W}{L}$ of transistors M_8 and M_9 it is possible to obtain a stable V_{REF}. Posteriorly R_3 allow us to define the value of the voltage reference signal.

In fig. 4.2 is represented the voltage reference curve for a range of 150º, between -25ºC and 125ºC.

Analysing the curve, it is possible to verify a maximum of 190,295 mV and a minimum of 188,85 mV, consequently a variation of 2,027 mV. Considering a typical ambient temperature of 27ºC which is actually the default value in Cadence spectre to normal DC simulation, the value obtained is 188,308 mV.

The normal linearity measurement to voltage reference is the error in parts per million (ppm) by degrees Celsius (ºC). In eq. 4.1 is represented the temperature coefficient (TC) calculation.

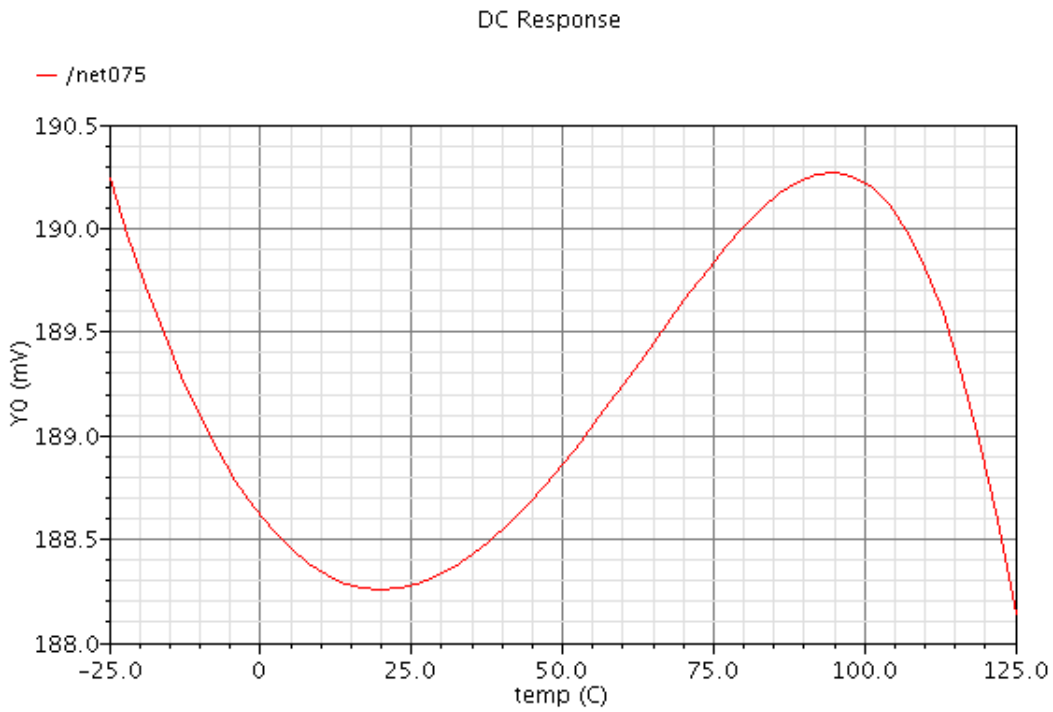

Figure 4.2: Bandgap voltage reference results.

$$TC(ppm) = \frac{\Delta V_{REF} * 1,0 * 10^6}{V_{REF}@27^oC} = \frac{2,11 * 10^{-3} * 1,0 * 10^6}{188,268 * 10^{-3}} = 11205ppm$$
$$TC(ppm/^oC) = \frac{11205}{150} = 74ppm/^oC \quad (4.1)$$

Another very important aspect considered in this circuit is the current dissipation of the circuit. In this component, using an ideal amplifier with a similar gain to the calculated theoretically, the current consumption obtained was 4,837 μA at 27ºC. Consequently a power consumption of 2,42 μW at 27ºC.

In fig. 4.3 is represented the simulated supply voltage dependences of the bandgap reference with typical working temperature of 27ºC.

As shown in fig. 4.4 although the overshoot varies, even with the temperature variance the stability is guaranteed to an input voltage of 500 mV. At this temperature, the stability is not guaranteed for an input voltage inferior of 500 mV. To verify the stability of V_{REF} and the non dependence of temperature, a parametric analysis was made to vary the temperature value.

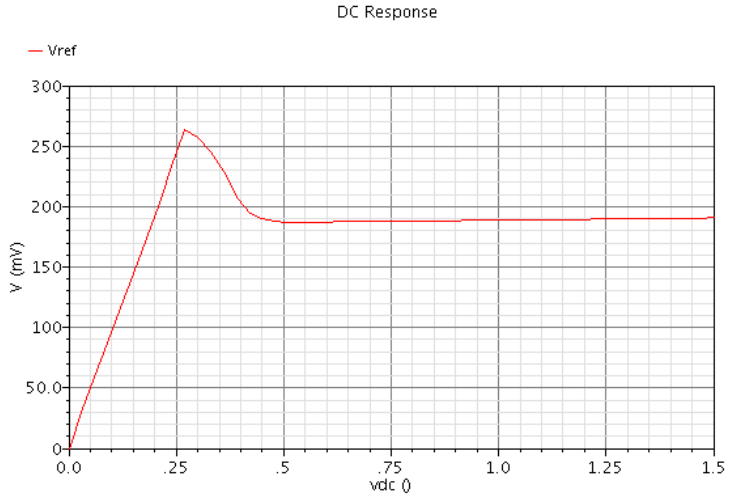

Figure 4.3: Reference voltage variation with the power supply voltage.

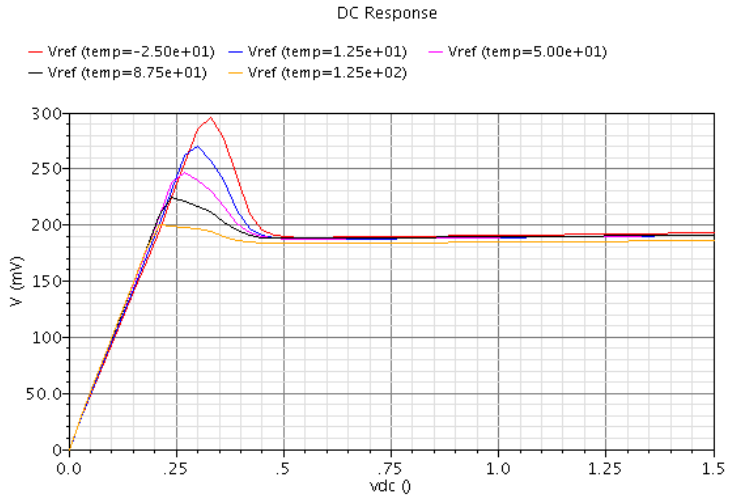

Figure 4.4: Reference voltage variation for different temperatures and power supply voltage.

4.2 Operational Amplifier

With the inclusion of an operational amplifier, the current consumption of the bandgap circuit increased to 7μA. That corresponds to an increase of 2,57μA in comparison with the ideal amplifier.

The widths and lengths of the transistors as result of the designed of circuit are represented in tab.4.2

Component	W/l
M_1	$4\mu/1\mu$
M_2	$15\mu/1\mu$
M_3	$2\mu/1\mu$
M_4	$30\mu/2\mu$
M_5	$30\mu/1\mu$
M_6	$1\mu/1\mu$
M_7	$6\mu/2\mu$
M_8	$6\mu/2\mu$
M_9	$4\mu/1\mu$
R_C	$183k\Omega$
C_C	$464fF$

Table 4.2: Amplifier component sizes.

To achieve the best performance by the reference voltage circuit, a well designed amplifier circuit is needed. It is designed to obtain a gain of 72 dB which was in line with the theoretical one, in order to obtain the same voltage in the nodes where the PTAT and CTAT voltages are measured. A Gain Bandwidth near 6 MHz and a correspondent Phase Margin of 60º. It is also important to verify the poles position and the non influence of the zero in the phase margin. In fig.4.6 is represented the DC Gain and Phase of the amplifier.

As observed in the figure, the Gain Bandwidth value was 6,201 MHz which is similar to the calculated theoretically(6,88MHz). As intended the Phase Margin was set to 60º by variation of the parameters which influence the poles. The low and high frequency poles value also seem to correspond to the theoretical calculation and the zero doesn't interferes with the high pole frequency. So the zero was set to a frequency higher than the last pole.

As the temperature varies the Gain and Phase will change, despite of this variation the Gain remains higher, although it decreases to 65 dB when the temperature achieves 125º. As regards to the Phase, the phase margin changes with the temperature variation. With low temperature at high frequencies the zero seems to affects the phase with a small increase as seen in fig.4.6. Another fact that can be retired from the figure is the increase of Gain bandwidth with the temperature decrease.

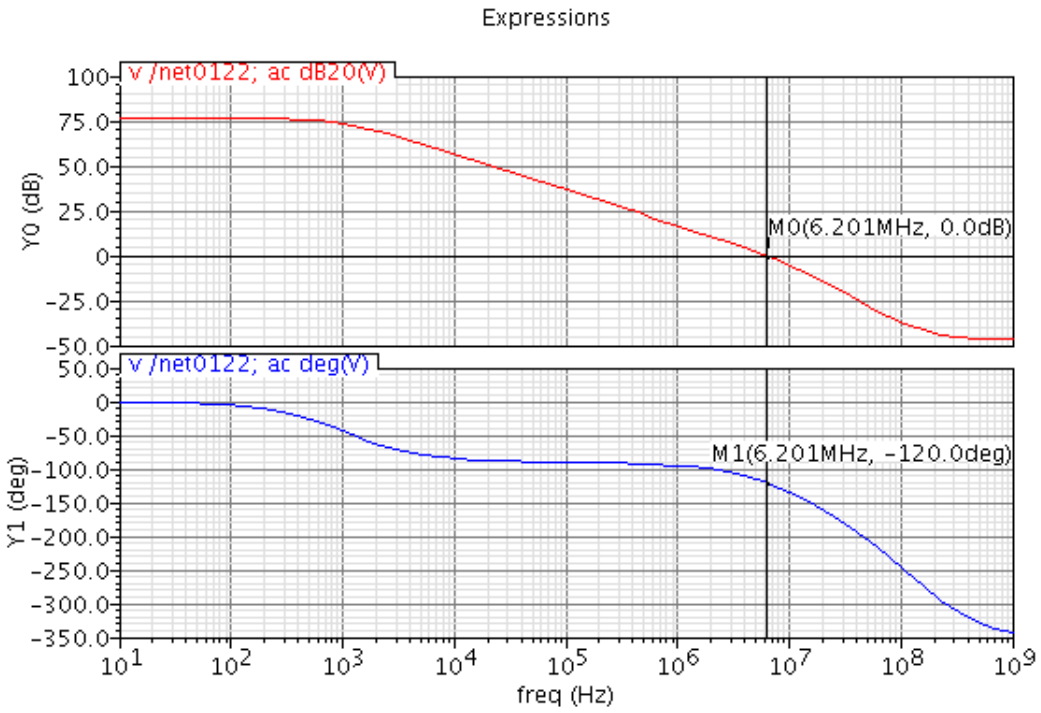

Figure 4.5: Bode diagram.

A process corner simulation with different corners is important, most of manufacturers vary in the parameters used to fabricate integrated circuits.[WH05] This corners represent the extreme variations of the parameters. Those variations are made in temperature, clock frequency and voltage. In this case, the corners used are SS(slow-slow), TT(typical-typical) and FF(fast-fast) and represent the carrier mobilities that are higher and lower than normal. As shown in fig.4.7 this corners represent different results.

As observed, the corners with different parameters change the phase margin, 20º to SS and -45º to FF. As the poles and zero values are adjusted to a typical corner, then the other corners will move the poles and zeros to other frequencies. Another point to analyse is the increase of Gain bandwidth frequency with the faster corner, in the opposite higher Gain is produced by the slower corner.

The alternation between different corners, will also change the bandgap behaviour. In tab.4.3 is represented the temperature coefficient and the voltage reference for each corner.

Process Corner	Voltage Reference	Temperature Coefficient
TT	188,3	74 ppm/°C
SS	188,3	73 ppm/°C
FF	188,6	85 ppm/°C

Table 4.3: Effects of corners in the bandgap

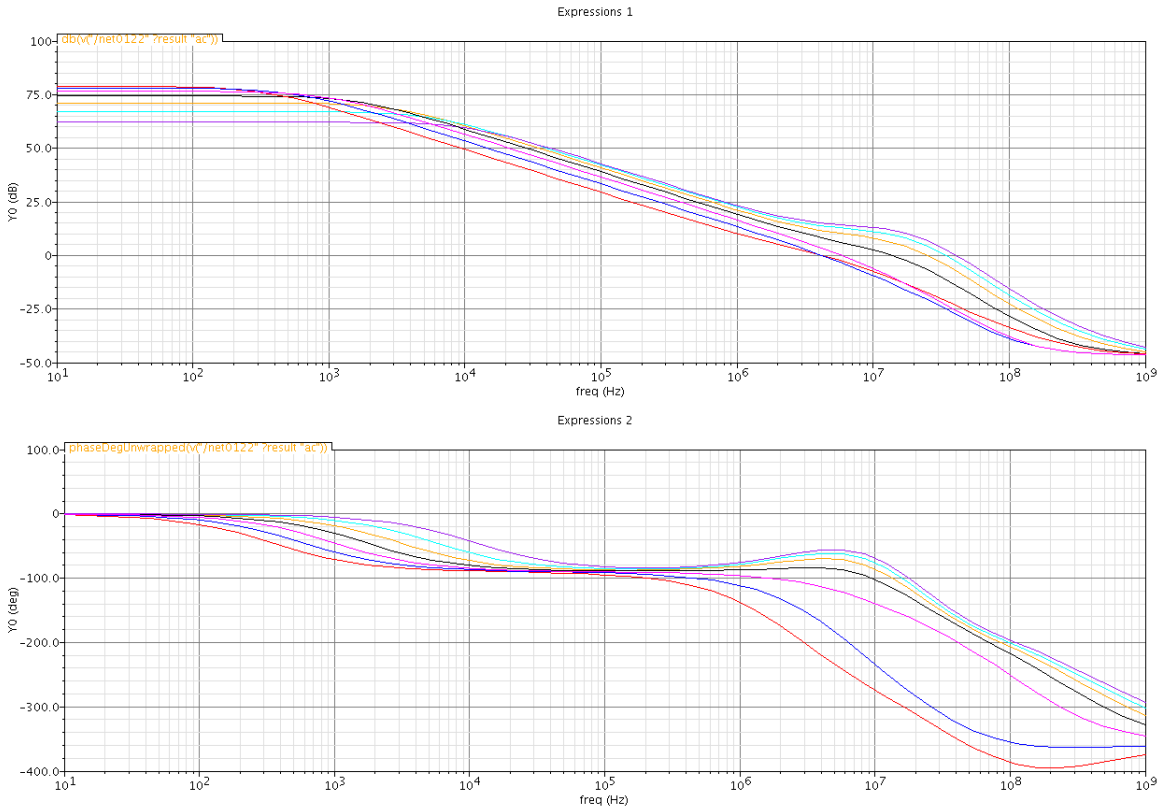

Figure 4.6: Bode diagram with temperature variation.

As expected the FF(fast-fast) produced the worst results, that result can be explained by the low gain in comparison with the other corner simulations. As referred anteriorly, a low gain produces a bigger offset in the node where the PTAT and CTAT voltages are measured, that error will propagate to the voltage reference. In other hand the SS(slow-slow) produces a better result, in this case a bigger gain reduces the offset and the Temperature Coefficient.

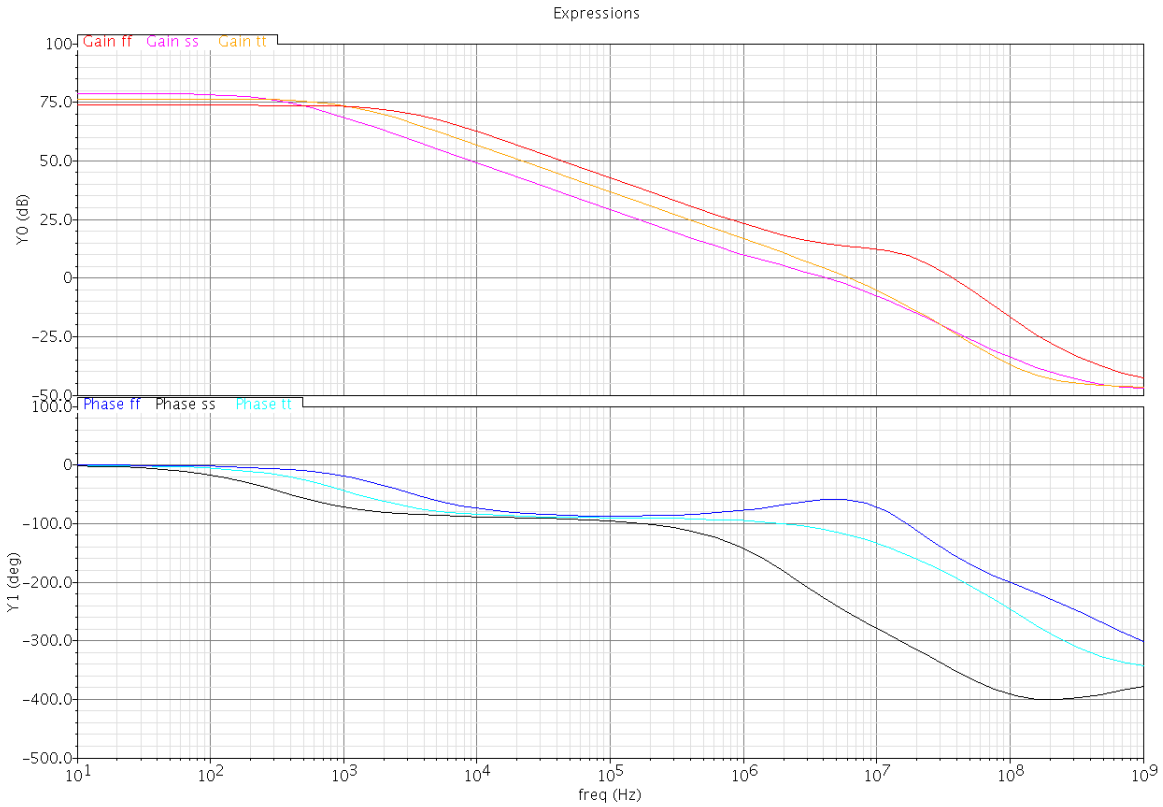

Figure 4.7: Bode diagram with different process corners.

4.3 Temperature Sensor

The design of the circuit consists in count 2^8 with a PTAT current flowing the circuit and charging the capacitor. After this period, the current flowing in the circuit is switched to constant current. In fig.4.8 is represented the two currents inserted in the circuit. The PTAT current increases 400 nA between -55ºC and 125ºC, as shown in the figure the linearity is almost perfect. The constant current has the same behaviour of the reference voltage and varies 15 nA, which is not relevant taking in consideration the magnitude of the currents.

In order to work correctly, the constant current must be similar to the PTAT current at his higher value. This fact will allow us to have also a 256 bits maximum count in the discharge time which represents 125ºC and obtain a variable key in this range. As observed in the picture the currents matches in the 125ºC to a current of 546 nA.

Using the eq. 3.15, is now possible to calculate the linearity of the temperature sensor. For example measuring the currents to -25ºC, 0ºC, 25ºC, 50ºC, 75ºC and 100ºC. The results are calculated in eq. 4.2

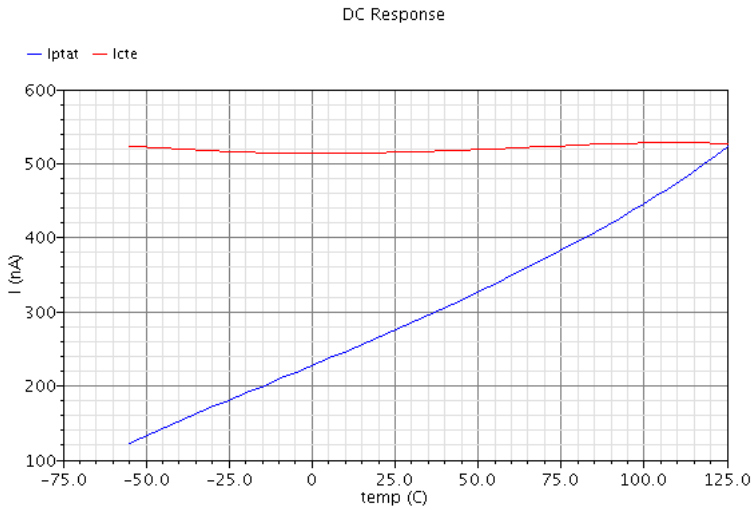

Figure 4.8: Mirrored proportional to absolute temperature and constant currents.

$$N = \frac{256 I_{PTAT}}{I_{CTE}}$$

$$To \quad -25^{o}C$$

$$N = \frac{256 * 181,4 * 10^{-9}}{515 * 10^{-9}} = 90,17 \simeq 90$$

$$To \quad 0^{o}C$$

$$N = \frac{256 * 227,5 * 10^{-9}}{515 * 10^{-9}} = 113,09 \simeq 113$$

$$To \quad 25^{o}C$$

$$N = \frac{256 * 275,3 * 10^{-9}}{515 * 10^{-9}} = 136,85 \simeq 136$$

$$To \quad 50^{o}C$$

$$N = \frac{256 * 327 * 10^{-9}}{515 * 10^{-9}} = 162,55 \simeq 163$$

$$To \quad 75^{o}C$$

$$N = \frac{256 * 383,1 * 10^{-9}}{515 * 10^{-9}} = 190,43 \simeq 190$$

$$To \quad 100^{o}C$$

$$N = \frac{256 * 446,3 * 10^{-9}}{515 * 10^{-9}} = 221,85 \simeq 222 \tag{4.2}$$

To analyse the values, the results were transposed to a graphic represented by fig. 4.9

As represented by the graph, the obtained points are in line with the linear regression, with an average error of 1,4≃1 code. To verify the linearity of the curve, the PTAT current was subtracted of the constant current as shown in fig. 4.10. The result is in line with the calculated and the curve is almost linear, with the curve tendency increasing more than expected after 100ºC.

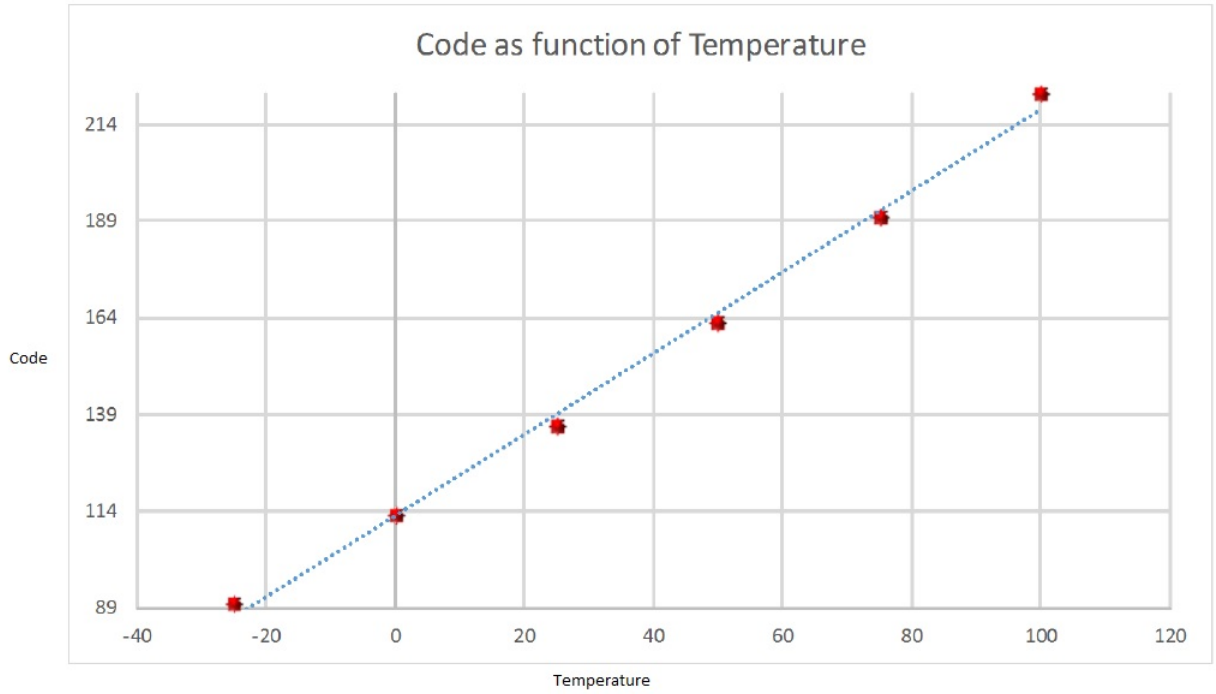

Figure 4.9: Code as function of temperature.

In tab.4.4 is represented the transistors sizes and the capacitance value.

In fig.4.11 is represented the behaviour of the temperature sensor at 27°C with an ideal and a real comparator, firstly while the counter counts 2^8 periods the PTAT current is inserted in the circuit. This increasing current generates a proportional voltage which is switched in the final of the count and finally the capacitor interrupt is activated and force the voltage to zero. As seen in the previous chapter, the peak voltage value is adjustable through the constant current, the capacitor capacity and the integration time (controlled by the clock frequency). In terms of stability, it was important to balance the multiple factors, but the most important fact to consider is the capacitor size which could occupy a large area in the circuit.

As seen in fig.4.11, the results are quite similar, although the reaction time of an ideal comparator is instantaneous. The real comparator presents a delay of 0,5μs which corresponds to 2 clocks, this delay can introduce a small error when the code/acknowledgement is sent.

Using this result it is also possible to calculate the least significant bit(LSB) voltage.

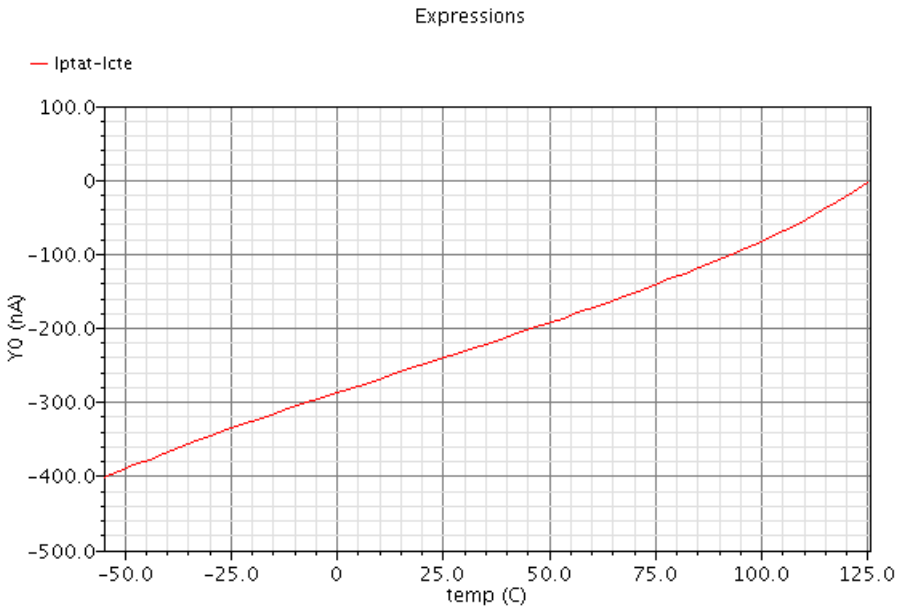

Figure 4.10: Difference between proportional to absolute temperature and constant currents.

The V_{LSB} is the minimum voltage of each level that an ADC can convert. The calculation of V_{LSB} is represented in eq. 4.3.

$$\begin{aligned} V_{LSB} &= \frac{V_{REF}}{2^{nbits}} \\ V_{LSB} &= \frac{188 * 10^{-3}}{2^8} \\ V_{LSB} &= 0,73mV \end{aligned} \tag{4.3}$$

Attributing a major importance to the capacitor size, results in a minimum value of 20pF, the minimum current designed for this circuit was near 500 nA and the main problem stood in the clock frequency. Those low currents and shorter capacitor led to a clock frequency of 4 MHz. Although the power dissipation increases, the vantages are notorious.

In addition to the advantages referred before, the linearity of the output code achieves better results. The balance made in the designed circuit was mostly in the frequency clock and the capacitor, in order to have a peak voltage below 400 mV, to avoid the loss of linearity and at the same time avoid increasing the capacitor to higher sizes.

In fig.4.12 the currents were set to a minimum value of 0ºC and a maximum value of 75ºC. To 0ºC the interception with the zero voltage should be faster than the represented, however either the difference time of 25ºC to 50ºC or the difference time of 50ºC and 75ºC are similar. The delay in the interception with zero voltage subsisted to every temperature variation, although in both cases the delay is 2 clocks as referred before, which is not a large error taking in consideration its magnitude.

Component	W/l
M_1	$1\mu/1\mu$
M_2	$1\mu/1\mu$
M_3	$1\mu/2\mu$
M_4	$1\mu/2\mu$
M_5	$10\mu/2\mu$
M_6	$10\mu/2\mu$
M_7	$100\mu/120n$
M_8	$32\mu/120n$
M_9	$32\mu/120n$
M_{10}	$100\mu/120n$
M_{11}	$4\mu/2\mu$
M_{12}	$4\mu/2\mu$
C	$20pF$
M_{13}	$4\mu/1\mu$
M_{14}	$15\mu/1\mu$
M_{15}	$2\mu/1\mu$
M_{16}	$2\mu/1\mu$
M_{17}	$2\mu/1\mu$
M_{18}	$1\mu/1\mu$
M_{19}	$6\mu/2\mu$
M_{20}	$6\mu/2\mu$
M_{21}	$1.2\mu/1\mu$

Table 4.4: Analogue-to-digital converter sizes.

At right in fig.4.12 is represented the behaviour of the transistors that compose the switch. As the voltage achieves zero voltage, the switch is activated, when NMOS receives 500 mV and the PMOS receives 0 V.

To verify some of the points mentioned in the last chapter, in fig. 4.13 is represented a variation of the capacitance value. As demonstrated in eq.3.15, the capacitance value is inversely proportional to the peak voltage and the figure proves it.

Another important fact is the influence of the capacitor in the discharge time, as also shown in eq.3.15, the discharge time is directly proportional to the capacitance value.

An aspect to emphasize also is the voltage cut, when becomes linear as observed in the last part of the figure, where the capacitor is 30 pF and the voltage peak is higher in those 3 cases.

The fig.4.14 represents the variation of the magnitude of the PTAT current, as expected the sensor response is the inverse of the capacitance variance, in this case the current is directly proportional to the peak voltage and also cuts in a certain point of voltage. With the decreasing of voltage, the discharge period is larger.

To finalize, the variation of the clock frequency, the results are represented in fig.4.15 and demonstrates that the increase to the double clock period, as a result in a very large charge period and the voltage easily reach the maximum cut voltage in the charge period.

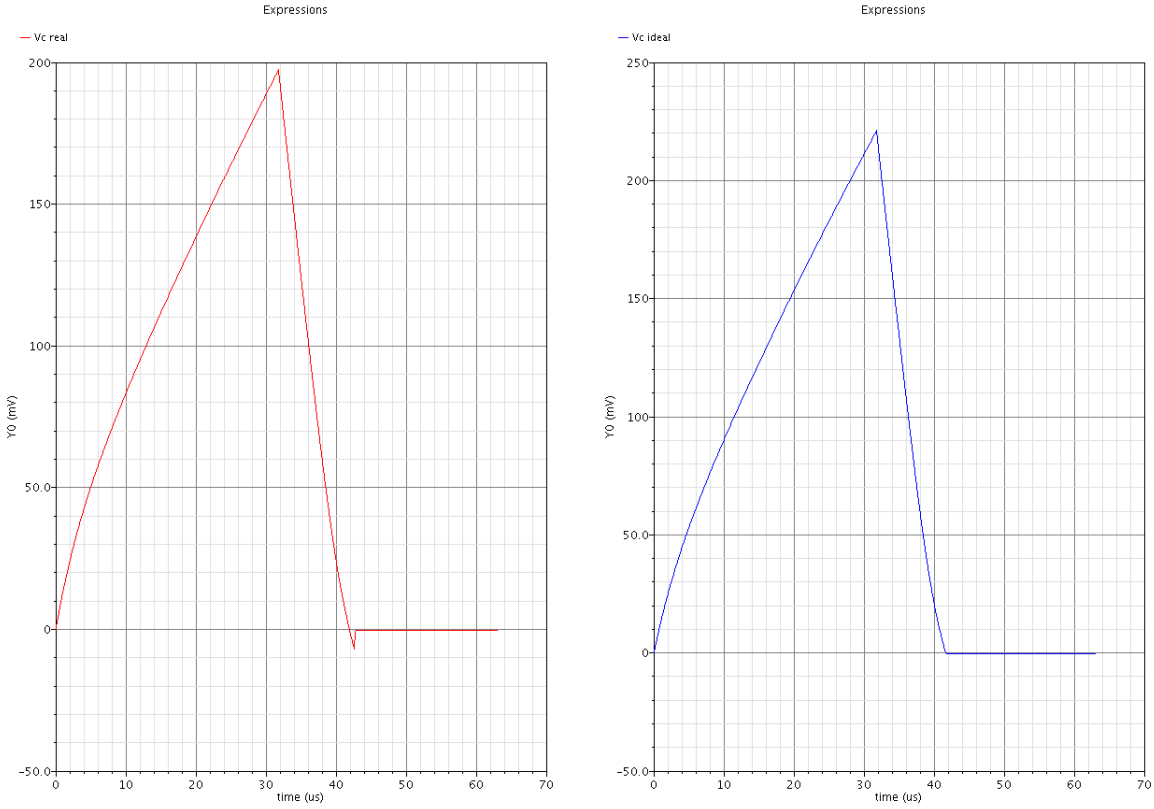

Figure 4.11: Temperature sensor behaviour.

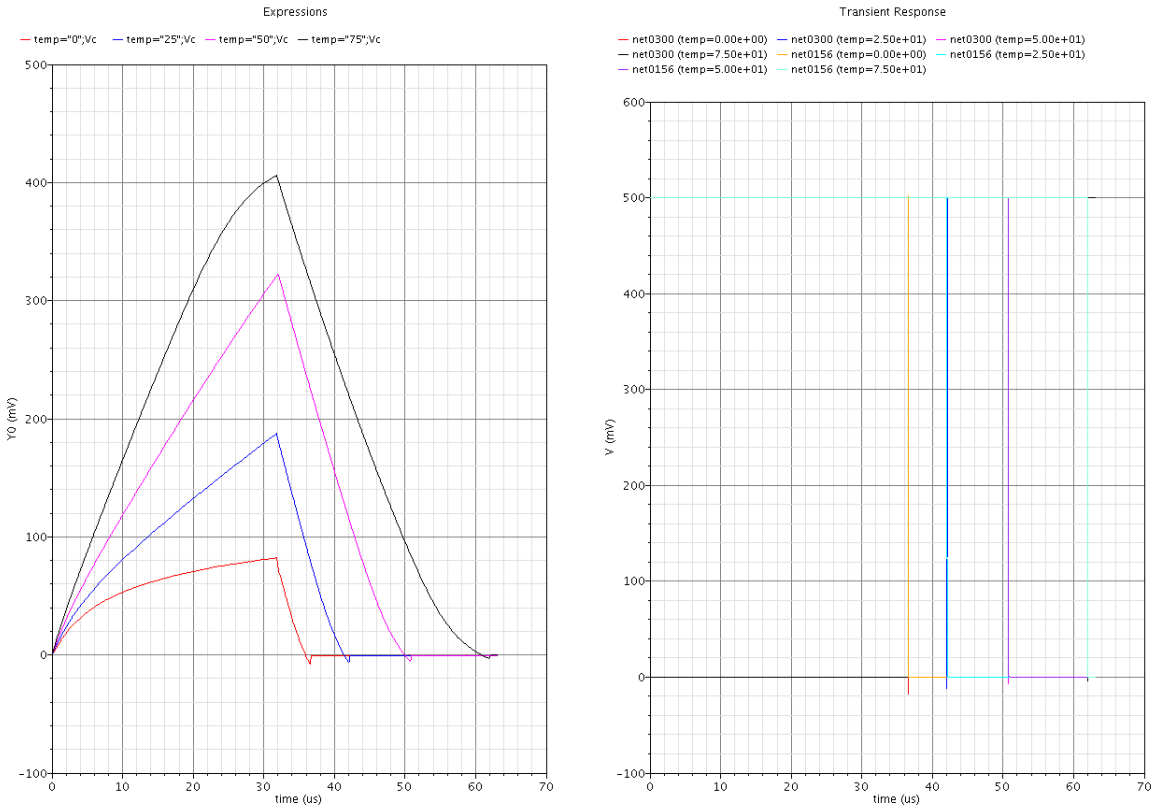

Figure 4.12: Temperature sensor behaviour to different temperatures.

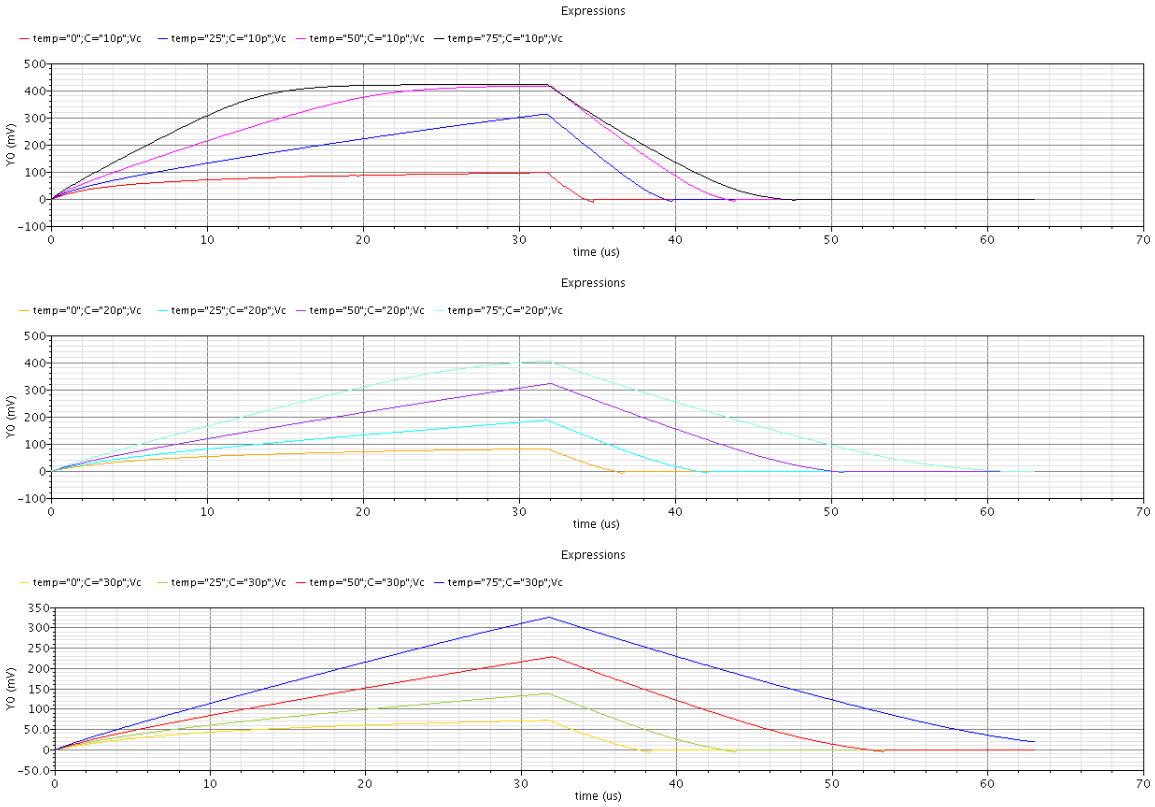

Figure 4.13: Temperature sensor behaviour for different capacitance values.

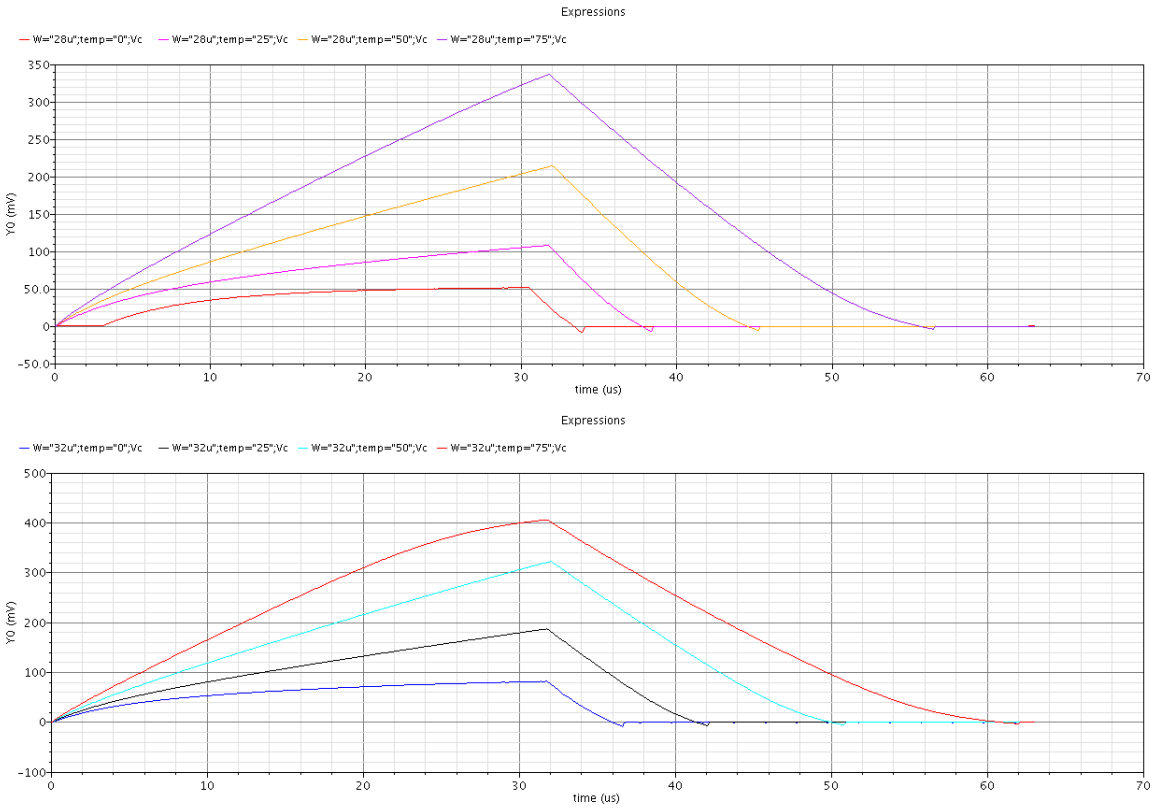

Figure 4.14: Temperature sensor behaviour of the PTAT current magnitude variation.

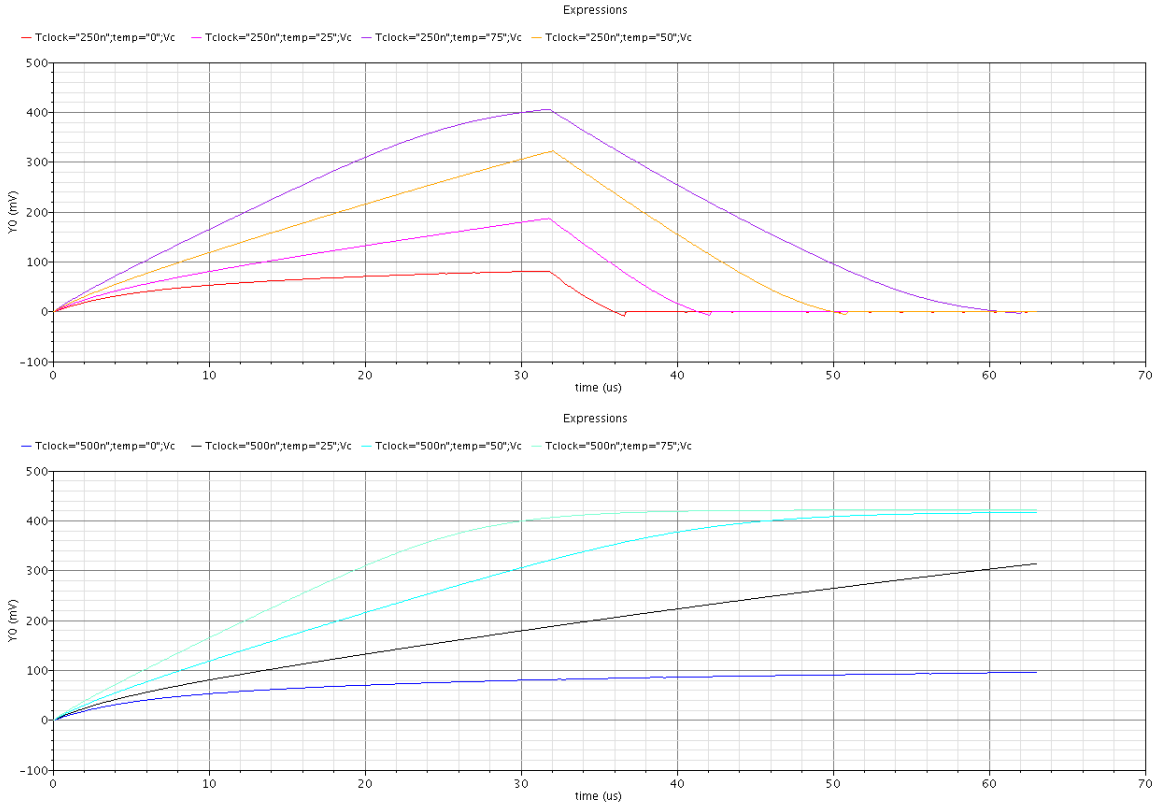

Figure 4.15: Temperature sensor behaviour to different clock frequencies.

5

Conclusion and Future Work

5.1 Conclusion

The proposed objective of this thesis was to develop a bandgap voltage reference with a preferential low voltage operation and assuring the stability in the reference voltage. The bandgap reference voltage which included the design of an amplifier with the function of assuring a voltage drop of the CTAT(complementary to absolute temperature) inversely proportional to the PTAT(proportional to absolute temperature).

A temperature sensor was also designed, in this part the main objective was to convert the temperature to a digital code. Using the PTAT and constant currents generated by the bandgap and mirroring them to an integrating capacitor and adding a counter allowed to obtain a similar double ramp analog-to-digital(ADC) converter. To stop the voltage of reaching negative values in the discharge time of the capacitor, a comparator was designed to detect the zero and posteriorly send the code.

In chapter 2, the basic topologies and design approaches of bandgap circuits were presented. The three principal topologies were studied, it was important to verify the vantage and disadvantages of each circuit.

The bandgap circuits based on bipolar transistors had a better performance in terms of voltage reference stability, the major problem was the minimum voltage supply, which was near 900 mV. An high minimum voltage supply with the addiction of an amplifier in the circuit will reflect in a higher power dissipation.

The bandgap circuit proposed in this thesis is based on MOS transistors. This approach was the one that offered the last compromises between the different goals such as

low voltage operation, low power dissipation and voltage stability. The power dissipation depends in a great part of the developed amplifier, although the studied values were interesting.

Finally, the bandgap circuit composed only of MOS transistors which requires a minimum voltage supply similar to the bipolar transistors bandgaps. Its stability is almost perfect due to the balance between V_{GS} and V_{SG} which is a very interesting approach. The power dissipation is also the lowest, since the circuit doesn't require an amplifier, the current consumption will be very low. In table 5.1 is represented a comparison between the circuits studied and the one developed to this thesis.

[1] - Sub-1 V CMOS Bandgap Reference
[2] - Bandgap Voltage Reference for 1.1V Supply in Standard 0.16 μm CMOS
[3] - Voltage Reference Circuit Consisting of Subthreshold MOSFETs

Parameters	**[1]**	**[2]**	**[3]**	**This project**
Reference voltage at 27ºC	634,93 mV	944 mV	745 mV	188 mV
Supply voltage	1,2 V	1,1 V	1,4 V	500 mV
TC	7,93 ppm/ºC	30 ppm/ºC	7 ppm/ºC	74 ppm/ºC
Temperature range	-40ºC<T<125ºC	-45ºC<T<135ºC	-20ºC<T<80ºC	-25ºC<T<125ºC
Current supply	24μA	1,4μA	214 nA	7 μA
Technology	0,13 μm CMOS	0,16 μm CMOS	0,35 μm CMOS	0,13 μm CMOS
Area	-	0,0025 mm^2	0,055 mm^2	-

Table 5.1: Performances of the studied circuits and the developed to this thesis.

In chapter 3, the design of the different parts of the circuit was presented. The most challenging point of this circuit was to obtain an interesting performance of all the components with a voltage supply of only 500 mV. Starting with the bandgap, the designed circuit had some interesting points to emphasize, the use of a mirrored current which allowed the circuit to obtain a better stability in the reference voltage. An high gain was necessary and a phase margin of 60º, in order to produce a shorter voltage offset between the nets in which the PTAT and CTAT voltage were obtained.

Then the temperature sensor was developed, the PTAT and constant currents were mirrored from the bandgap, which allowed to create an integrator circuit which is part of a double ramp ADC. A synchronous counter and some logic gates were also developed to control the temperature sensor. To finish a comparator was developed to detect the moment in which the voltage reaches zero volts and stuck it in that value, generating a key that will be equivalent to a certain temperature.

In chapter 4, the simulated results are presented and the results were mostly the expected in all parts. All the circuit is supplied by 500 mV including the temperature sensor, the bandgap voltage reference was 188 mV with a TC of 74 ppm/^{o}C between -25^{o}C and 125^{o}C. The resulting power supply was 7 μA which is also an interesting value, that results in a power dissipation of 3,5 μW. The amplifier was also very efficient with a gain of 72 dB and a phase margin of 60^{o} which was the necessary to force a minimum offset between the two nets where the PTAT and CTAT voltage are measured.

The temperature sensor performed some interesting results, starting with a linear code generation to associate with the temperature range. The obtained curves to the ramp were also very linear and the comparator was effective, although the delay of 2 clock periods. The worst performance was the clock frequency which was very high 4 MHz, resulting in an increase of the power consumption. In the case of the capacitor size, it's a relatively high value which will result in a greater area then the expected.

To resume the circuit has a total current consumption of 11,4 μA, which will result in a power dissipation of 5,7 μW. Which is a very interesting value for the complexity of the circuit.

5.2 Future Work

In this circuit, some aspects should be considered to achieve a better performance in a future work. Starting with the bandgap, although this methodology was capable to work normally with a voltage supply of 500 mV, the "Voltage Reference Circuit Consisting of Subthreshold MOSFETs" example in which is based a bandgap with MOS transistors only produces interesting results. The combination of a great stability with a low power dissipation and an interesting area succinct a great analyse, in order to test those type of circuits and improve their performance. I am convinced about the power dissipation saved by the absence of an amplifier which is the great factor of the current consumption. Analysing the temperature sensor, some correction should be made posteriorly. The delay in the zero voltage detection by the comparator can generate an error about 1^{o}C in the sensor output. There is always a chance to improve the results and performance of the key generation, with an adjust in the circuit and transistors even more precisely sized, the accuracy of the temperature sensor will be improved.
In general, it also would be useful to test the circuit with different temperature sensors, and improve the results, which was the more difficult part of this thesis.

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