Ex 1:

In Fig. 10.67, $I_{EE} = 1$ mA and $V_A = 5$ V. Calculate the voltage gain of the circuit. Note that the gain is independent of the tail current.

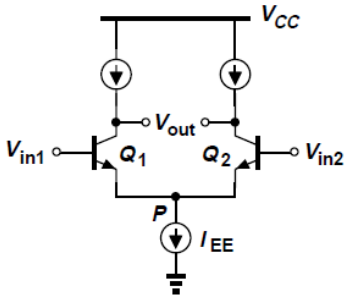

Figure 10.67

Ex 2:

Consider the circuit illustrated in Fig. 10.102. Assume a small dc drop across R_1 and R_2.

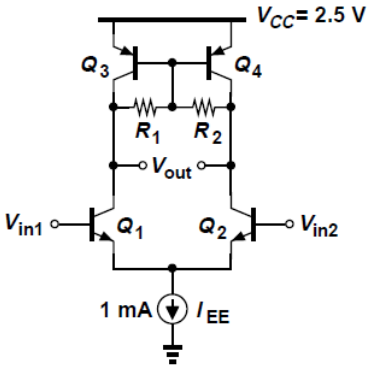

Figure 10.102

(a) Select the input CM level to place Q_1 and Q_2 at the edge of saturation.
(b) Select the value of R_1 $(= R_2)$ such that these resistors reduce the differential gain by no more than 20%.

Ex 3:

Design the circuit of Fig. 10.96 for a gain of 50 and a power budget of 1 mW. Assume

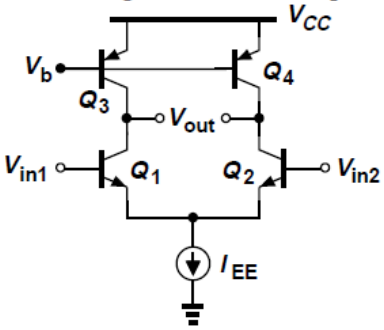

Figure 10.96

$V_{A,n} = 6$ V and $V_{CC} = 2.5$ V.

Ex: 4

Assuming perfect symmetry and $V_A < \infty$, compute the differential voltage gain of each stage depicted in Fig. 10.69.

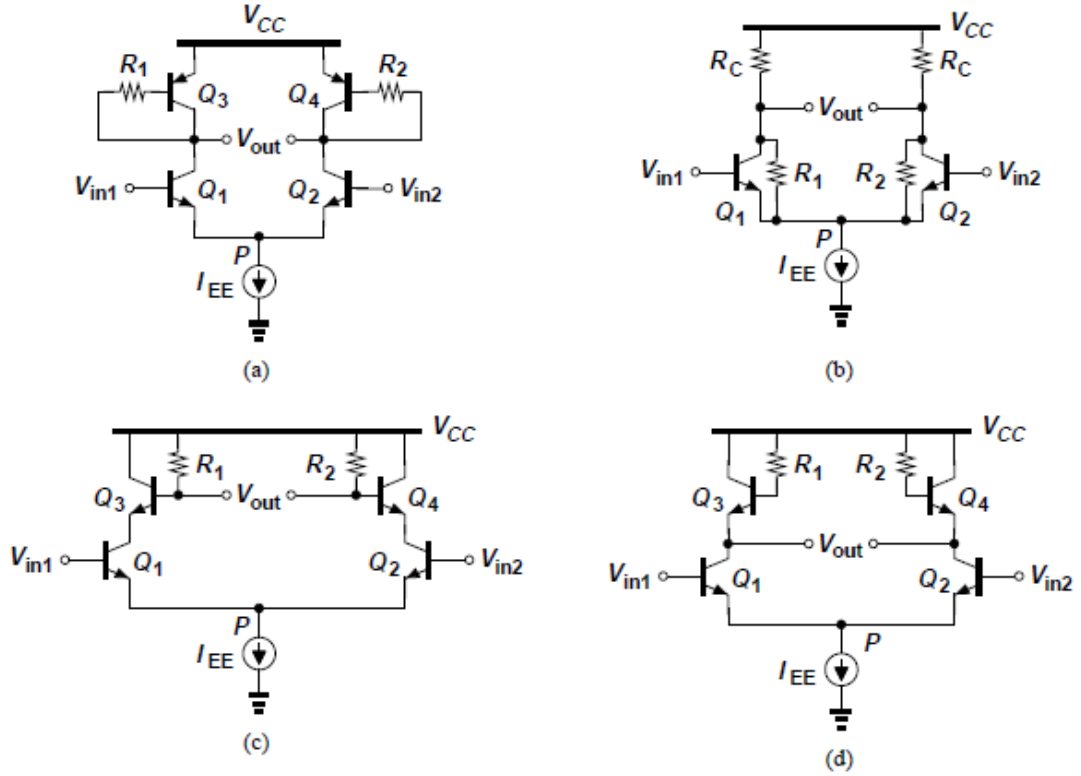

Figure 10.69