

OrCAD Capture Known Problems and Solutions

**Product Version 16.6
October 2012**

© 1996–2012 Cadence Design Systems, Inc. All rights reserved.

Portions © Apache Software Foundation, Sun Microsystems, Free Software Foundation, Inc., Regents of the University of California, Massachusetts Institute of Technology, University of Florida. Used by permission. Printed in the United States of America.

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

OrCAD Capture contains technology licensed from, and copyrighted by: Apache Software Foundation, 1901 Munsey Drive Forest Hill, MD 21050, USA © 2000-2005, Apache Software Foundation. Sun Microsystems, 4150 Network Circle, Santa Clara, CA 95054 USA © 1994-2007, Sun Microsystems, Inc. Free Software Foundation, 59 Temple Place, Suite 330, Boston, MA 02111-1307 USA © 1989, 1991, Free Software Foundation, Inc. Regents of the University of California, Sun Microsystems, Inc., Scriptics Corporation, © 2001, Regents of the University of California. Daniel Stenberg, © 1996 - 2006, Daniel Stenberg. UMFPACK © 2005, Timothy A. Davis, University of Florida, (davis@cise.ulf.edu). Ken Martin, Will Schroeder, Bill Lorensen © 1993-2002, Ken Martin, Will Schroeder, Bill Lorensen. Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, Massachusetts, USA © 2003, the Board of Trustees of Massachusetts Institute of Technology. vtkQt, © 2000-2005, Matthias Koenig. All rights reserved.

Trademarks: Trademarks and service marks of Cadence Design Systems, Inc. contained in this document are attributed to Cadence with the appropriate symbol. For queries regarding Cadence's trademarks, contact the corporate legal department at the address shown above or call 800.862.4522.

Open SystemC, Open SystemC Initiative, OSCI, SystemC, and SystemC Initiative are trademarks or registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission.

All other trademarks are the property of their respective holders.

Restricted Permission: This publication is protected by copyright law and international treaties and contains trade secrets and proprietary information owned by Cadence. Unauthorized reproduction or distribution of this publication, or any portion of it, may result in civil and criminal penalties. Except as specified in this permission statement, this publication may not be copied, reproduced, modified, published, uploaded, posted, transmitted, or distributed in any way, without prior written permission from Cadence. Unless otherwise agreed to by Cadence in writing, this statement grants Cadence customers permission to print one (1) hard copy of this publication subject to the following conditions:

1. The publication may be used only in accordance with a written agreement between Cadence and its customer.
2. The publication may not be modified in any way.
3. Any authorized copy of the publication or portion thereof must include all original copyright, trademark, and other proprietary notices and this permission statement.
4. The information contained in this document cannot be used in the development of like products or software, whether for internal or external use, and shall not be used for the benefit of any other party, whether or not for consideration.

Disclaimer: Information in this publication is subject to change without notice and does not represent a commitment on the part of Cadence. Except as may be explicitly set forth in such agreement, Cadence does not make, and expressly disclaims, any representations or warranties as to the completeness, accuracy or usefulness of the information contained in this document. Cadence does not warrant that use of such information will not infringe any third party rights, nor does Cadence assume any liability for damages or costs of any kind that may result from use of such information.

Restricted Rights: Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Contents

<u>CCR 1065649: Issues in backward compatibility of 16.6 designs with 16.5 and 16.3 releases</u>	5
<u>CCR 943666 ENH: Flexibility to name a Bus member in NetGroup as ?BUS[MSB..LSB]?</u>	6
<u>CCR 730224: Library gets uprev'ed without any uprev message.</u>	6
<u>CCR 725742: Capture does not generate error and may allow you to create recursive design with hierarchical design.</u>	6
<u>CCR 724760: Iref generated for buses connected to OPCs.</u>	6
<u>CCR 724738: Update/Replace cache not working properly on user defined pin shapes.</u>	7
<u>CCR 722555: Cannot dock command windows if unselect Allow docking.</u>	7
<u>CCR 701056: capture crashes due stale old workspace data in registry.</u>	8
<u>CCR 700463: Pin shape issues.</u>	8
<u>CCR 700407: Pin is removed if using IEEE symbols or picture in pin shapes.</u>	8
<u>CCR 687342: IREF not generated for External designs till page number is manually updated.</u>	8
<u>CCR 425315: The Archive Project utility does not archive the PSpice Advanced Analysis (AA) <i>opamp</i> models</u>	9
<u>CCR 37520: Relative path should be added to place port macros.</u>	9
<u>CCR 31067: Need to run back annotation and update design twice if pin swapping and gate swapping is done for the same section in Allegro PCB Editor board.</u>	9
<u>CCR 22098: DEVICE property in Capture version 9.2 and later.</u>	9
<u>CCR 21123: Testbench should be invoked with VHDL editor.</u>	10
<u>CCR 228624: Pads and wirelist netlists do not display visible Power pins connected to an external power.</u>	10
<u>No CCR: Search functionality in the Cadence Help viewer may generate incomplete or inconsistent returns</u>	10

OrCAD Capture Known Problems and Solutions

OrCAD Capture Known Problems and Solutions

Product Version 16.6 October 2012

This Known Problems and Solutions document describes important Cadence Change Requests (CCRs) for OrCAD® Capture and tells you how to solve or work around these problems. For information about CCRs that are fixed for this release, see the OrCAD Capture: What's New document.

Important: Only known problems and solutions available at release time are available in this document.

CCR 1065649: Issues in backward compatibility of 16.6 designs with 16.5 and 16.3 releases

Description: If you open a design with any of the following 16.6 features in either 16.5 or 16.3, the designs will be corrupted and the tool might crash:

- CIS linking for external parts
- Netgroup aware net aliases
- Waive DRC
- User assigned reference

Solution: Before opening the design, install the following HotFixes depending on the SPB release you are using:

- For Cadence SPB 16.3: Install HotFix 055
- For Cadence SPB 16.5: Install HotFix 033

OrCAD Capture Known Problems and Solutions

October 2012

CCR 943666 ENH: Flexibility to name a Bus member in NetGroup as ?BUS[MSB..LSB]?

Description: Now Bus [MSB . . LSB] is allowed resulting in the correct order for input pin of Netgroup block. But the pin name and order is incorrect if autowire is done for entry pin or for Netgroup Bus. Bus name is not taken into consideration and results in flat NetGroup name members.

CCR 730224: Library gets uprev'ed without any uprev message.

Description: Open a 16.2 library in 16.3 and perform the following operations:

1. Right-click the part and choose "Split part". Save the part.

Right-click the library (version 16.2) and choose either "New part from spreadsheet" or "New Symbol".

For the above operations, the 16.2 library is upgraded without any message to user.

2. Open a 16.2 library in 16.3 and perform the Save As command. For the upgrade message, choose Yes and save it to another name. A backup of the new library is made instead of a backup of the original library new library.

Solution: When upgrading a library (<library name>.olb), Capture preserves the original copy of the library in the old database format. This file is saved with the name <library name>_2_0_0.OBK at same location. You can rename this file as <library name>.OLB to retrieve the original library.

CCR 725742: Capture does not generate error and may allow you to create recursive design with hierarchical design.

Description: Capture may allow you to create a recursive design hierarchy tree if a schematic level operation is performed in Project Manager window

Solution: None.

CCR 724760: Iref generated for buses connected to OPCs.

Description:

On a design, if the port is a bus and the bus bit is an off-page connector or the net name is the same as the bus bit, the IREF is not generated.

If the off-page connector is a bus and the bit is an off-page connector or the net name is the same as the bus bit, the IFREF is not generated.

Solution: None

CCR 724738: Update/Replace cache not working properly on user defined pin shapes.

Description: Choose any user-defined pin shape in the design cache and replace it with any other user shape. Changes are reflected in the schematic editor, pin shape changed to the new one. Edit part, notice that Capture still shows old pin shape not the replaced one.

If you close the part editor and update current without any change, pin shape gets reverted to previous shape. Similar is the case on update cache. Make some changes and then update, changes are not visible in part editor.

Cleanup cache will even remove the pin shape shown in part editor. But when you try to place same part from design cache still shows old shape which is removed from cache. Move the part or reopen design, changed pin shapes not retained, reverted to the previous part.

Solution: If you do Replace cache on a user-defined pin shape say A with B in the design, then all instances of the user defined pin shape A will be replaced with B in the design and Pin Shape property on the pins will be updated to new pin Shape value.

This property is an instance override. At any time, you want to revert to library level pin shape value, you can use Delete property in property editor and it will delete the instance override and the same will be reflected on the schematic.

However, if you do an Edit part, then it will still show the part level user defined shape and not the instance override that exists in the schematic. This is by design.

CCR 722555: Cannot dock command windows if unselect Allow docking.

Description: User cannot dock the command window if the user selects the Allow docking option and then de-selects the option.

Solution: None

OrCAD Capture Known Problems and Solutions

October 2012

CCR 701056: capture crashes due stale old workspace data in registry.

Description: Capture crashes when a user tries to access *Place – Autowire – Connect to Bus* menu item.

Solution: Remove the following registry key
HKEY_CURRENT_USER\Software\OrCAD\CaptureWorkSpace\16.3.0 then re-launch Capture.

CCR 700463: Pin shape issues.

Description:

- ☐ Replace a pin with a user-defined pin shape. The pin is not attached to the part boundary. There is no extra space between the shape and its bounding box.
- ☐ The pin shape created and the pin shape shown on the part editor are different depending on the shape designed.

Solution: None

CCR 700407: Pin is removed if using IEEE symbols or picture in pin shapes.

Description: Create a pin shape using IEEE symbols or picture. Replace a pin with this shape, pin is removed. Zoom all, you will notice that pin name appears in the corner of the page. Update so that you can check on schematic. On schematic nothing can be seen and the pin is removed.

Solution: You cannot use IEEE symbols, text or images when creating a pin shape.

CCR 687342: IREF not generated for External designs till page number is manually updated.

Description: Generating IREF for design with single hierarchical block that references an external design (i.e design is in instance mode) causes a page number error. Using the Annotate command does not update the pages. Similar is the case for a design with hierarchical parts.

Solution: Before generating the IREF, you need to update the pages manually.

CCR 425315: The Archive Project utility does not archive the PSpice Advanced Analysis (AA) *opamp* models

Description: If you instantiate a part from the OPA.OLB, for example, *CA1458*, and create an archive, OrCAD Capture does not archive the model used by the part. The reason for this behavior is that the value of the *Implementation* property on the part is *awbca1458*, where as the library does not have this model. Instead the part contains models, like *awbca1458_1*, *awbca1458_2*, and *awbca1458_3*. Note that the Netlisting / Simulation and Edit PSpice Model is successful and it works by appending the Implementation with the value of the property LVEL to arrive at one of the above mentioned values.

Solution: We do not have a workaround at this time.

CCR 37520: Relative path should be added to place port macros.

Description: The PORTIN.BAS (Place Input Port) and PORTOUT.BAS (Place Output Port) macros shipped with Capture do not work because they have the wrong path set for the CAPSYM.OLB library.

Solution: Open the PORTIN.BAS and PORTOUT.BAS files located in the `\tools\capture\macros\` directory in a text editor and correct the path for the CAPSYM.OLB library.

CCR 31067: Need to run back annotation and update design twice if pin swapping and gate swapping is done for the same section in Allegro PCB Editor board.

Solution: If you have done pin swapping and gate swapping for the same section in your Allegro PCB Editor board, you need to run back annotation (and update your design) two times.

CCR 22098: DEVICE property in Capture version 9.2 and later.

Description: The `DEVICE` property that was used in previous releases, is used differently in Capture 9.2 and later. However, the existence of this property in your design library can cause problems with the Capture-Allegro PCB Editor interface.

Solution: In cases where your design library includes the `DEVICE` property (an anachronism from previous releases), you can avoid having to remove the property from each part in your library by employing the `IGNORE_PROP` property. To ignore the `DEVICE` property on a

OrCAD Capture Known Problems and Solutions

October 2012

complete design, define `IGNORE_PROP` as an environmental/system variable and assign it a value of "DEVICE".

As with all environmental variables, `IGNORE_PROP` is specific to a system login. You must have administrative privileges to define `IGNORE_PROP` as a system variable. Also, you must restart Capture in order to read the new variable settings.

CCR 21123: Testbench should be invoked with VHDL editor.

Description: When you edit a simulation testbench from the NCVHDL Preroute (or Postroute) Simulation dialog box, the tool should open the testbench file with the VHDL editor, thereby highlighting VHDL keywords and other language features. However, the tool currently opens the file in the default text editor tool for the host system.

Solution: Generate the testbench file normally, include it in the project, and then open it from the project manager as a VHDL file. This will invoke the VHDL editor.

CCR 228624: Pads and wirelist netlists do not display visible Power pins connected to an external power.

Description: This problem arises when you make Power pin visible for a component by checking the Power Pin Visible check box in the Edit Properties dialog box and connect it. Now, when you create a netlist, the Power pins do not appear in the netlist.

Solution: Before you create a netlist:

- Close the design file and reopen it.
OR
- Edit the part to make Power pins visible.
OR
- Drag the part slightly.

No CCR: Search functionality in the Cadence Help viewer may generate incomplete or inconsistent returns

Description: Search functionality in the Cadence Help viewer may generate incomplete or inconsistent returns.

OrCAD Capture Known Problems and Solutions

October 2012

Solution: Perform the following steps:

1. Close all instances of Cadence Help.
2. Delete the `.config` directory (automatically created the first time you run the viewer) on your computer.
 - ❑ On Solaris, AIX, and Linux operating systems, `.config` is created in your home directory.
 - ❑ On Windows, `.config` is created in your `C:\Documents and Settings\username` directory.
3. If the contents of the `doc` directory in your Cadence installation hierarchy was recently changed, enter `cdnshelp -refresh` at your system's command prompt to refresh the list of documents in the `doc` directory.

Note: You must have write permissions to over-write the files.
4. Restart Cadence Help.
5. If you performed step 3, above, select *File – Refresh Index* in the Cadence Help GUI to refresh the Search index.

Perform this procedure any time the contents of the documentation in your Cadence installation hierarchy may have changed or following the download of a software hot-fix, ISR, and so on.

OrCAD Capture Known Problems and Solutions

October 2012