cadence®

# PSpice: What's New

**Product Version 16.6**
**October 2012**

Cadence Design Systems, Inc. (Cadence), 2655 Seely Ave., San Jose, CA 95134, USA.

# Contents

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# What’s New in PSpice 16.6

This chapter describes the new features in the PSpice 16.6 release.

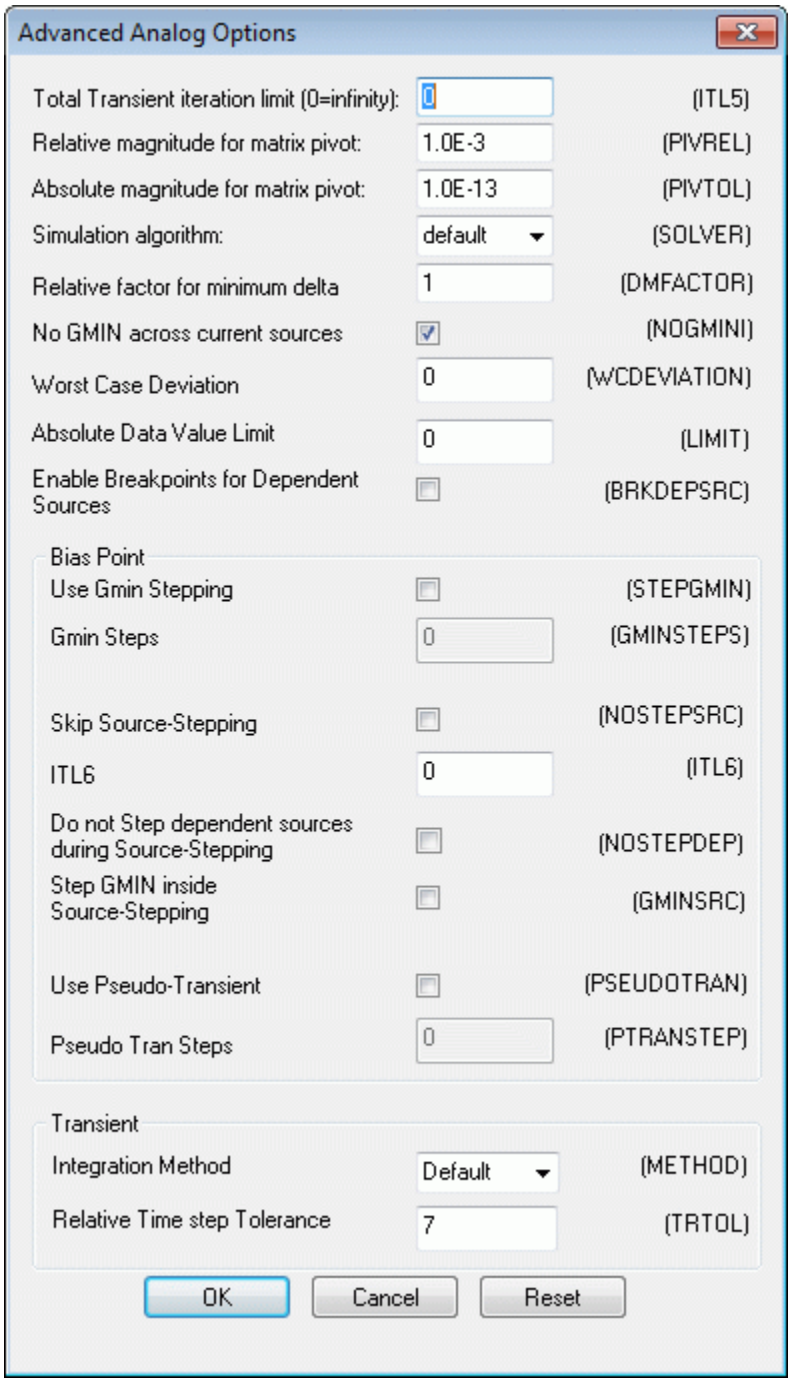
# New Features

PSpice[1] 16.6 brings you the following new features and enhancements:



1. Depending on the license and installation, either PSpice or AMS Simulator is installed. The new features only available with the AMS Simulator license are also listed in this manual.

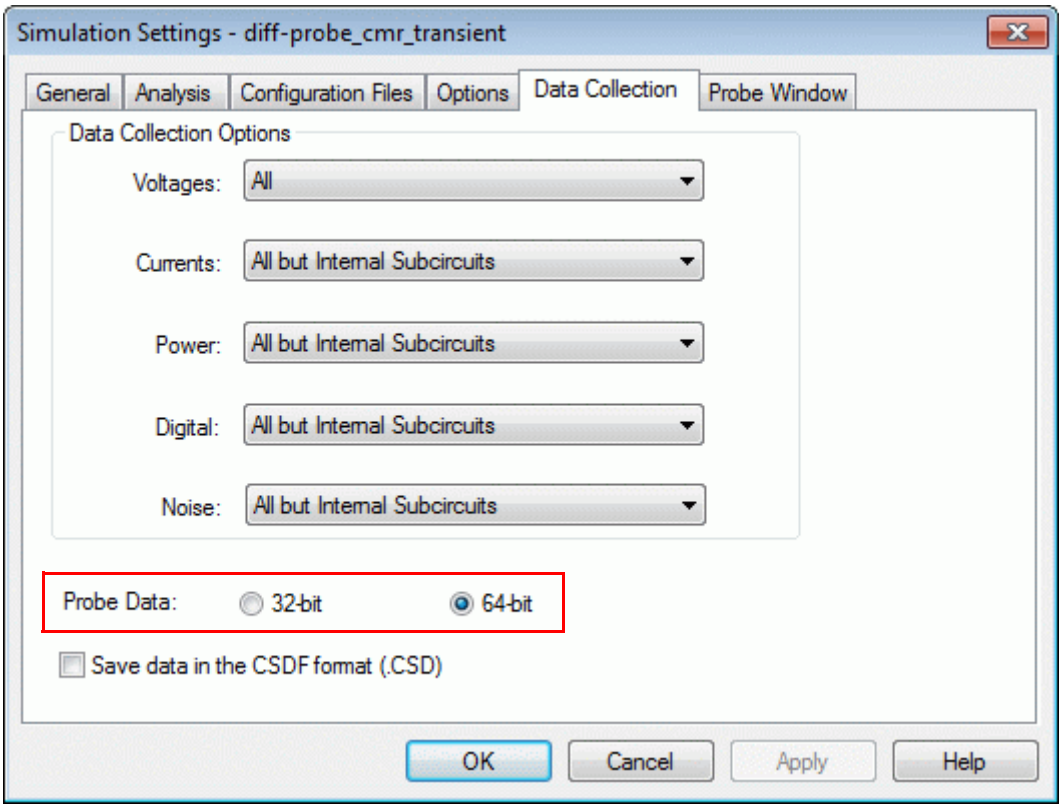
## Advanced Options




Many new options have been added to the Advanced Analysis Options dialog box in the following areas:

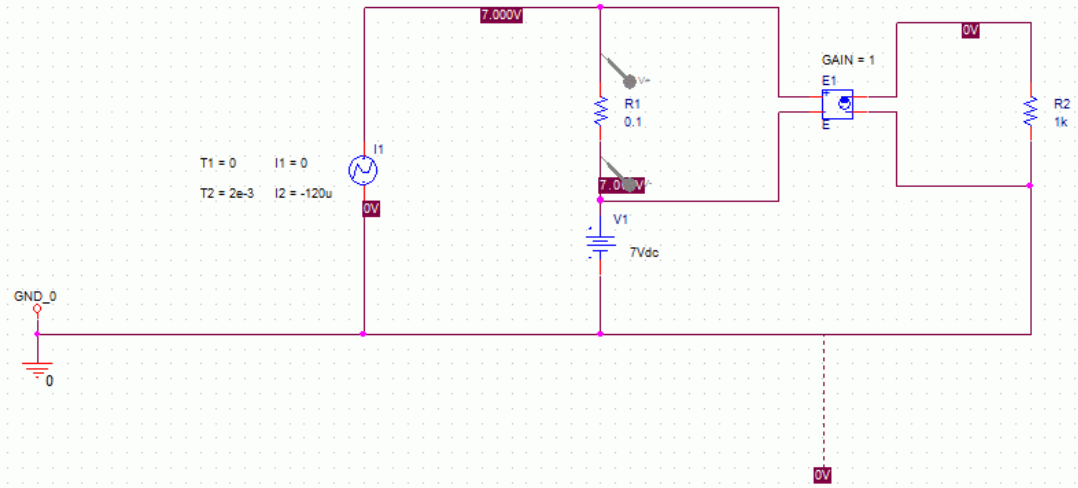
- Bias-Point Convergence
- Integration Method
- Voltage Limiting
- Worst-case Deviations
- Max-Time Step Control
- Pseudo Transient
- Relative Tolerance

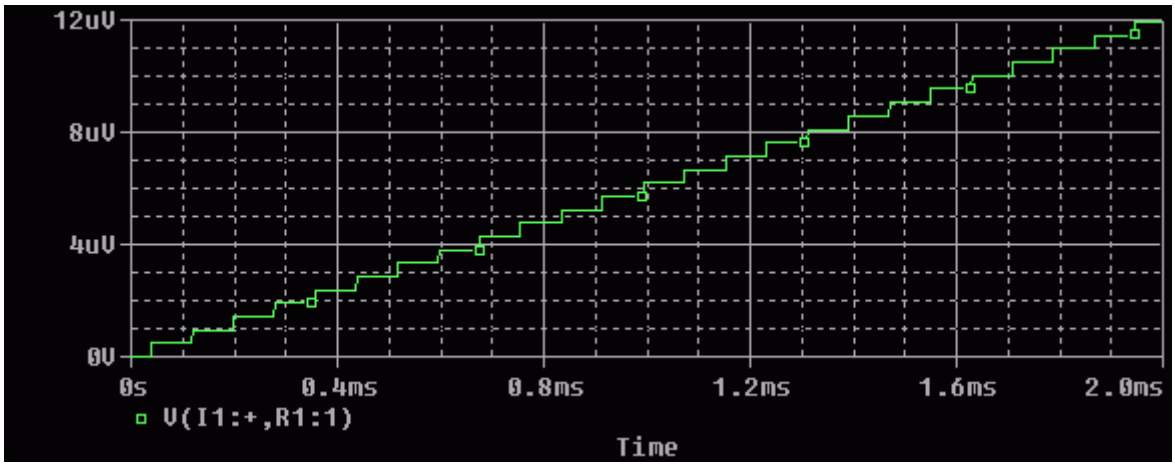
## Probe DAT Version Upgrade - 64-Bit Data Precision



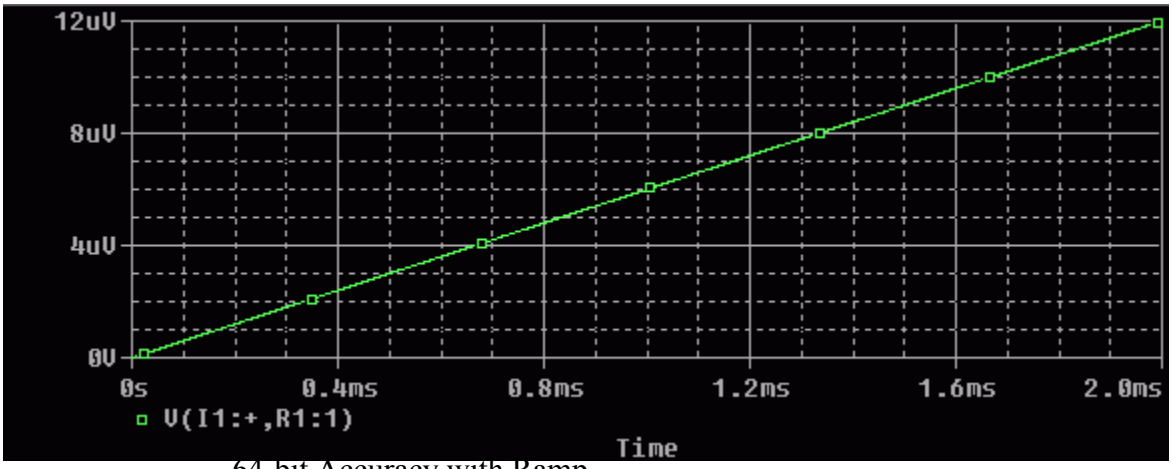

In 16.6, PSpice provides 64-bit data precision, by default. This ensures a higher precision compared to the 32-bit data. For example, when a very small amplitude voltage is superimposed on a large voltage, the resulting voltage loses its resolution, displaying staircase waveforms. In the following circuit, for instance, simulating with 32-bit precision

results in staircase waveforms. With 64-bit precision, for the same circuit, a perfect ramp waveform is displayed.




32-bit Accuracy without Ramp




64-bit Accuracy with Ramp

## Undo Support for Capture Netlists

Allow you to modify parameters, edit components and connectivities, and generate all supported capture netlists without losing undo-redo information on schematic.

- *Edit – Undo*
- *Edit – Redo*

## Enhanced IBIS Support

You can now translate vendor supplied IBIS or DML models for any version supported by signoise for a defined list of keywords (See Supported Keywords on page 14). The IBIS translator converts a IBIS or DML file and creates a PSpice library (`lib)` file for simulation. This `.lib` file can be used in both OrCAD Capture and Design Entry HDL for simulation in PSpice.

You can translate IBIS models:

- Using Model Editor
- Using the orPSpiceParsers Command

Both the Model Editor and command create the following files:

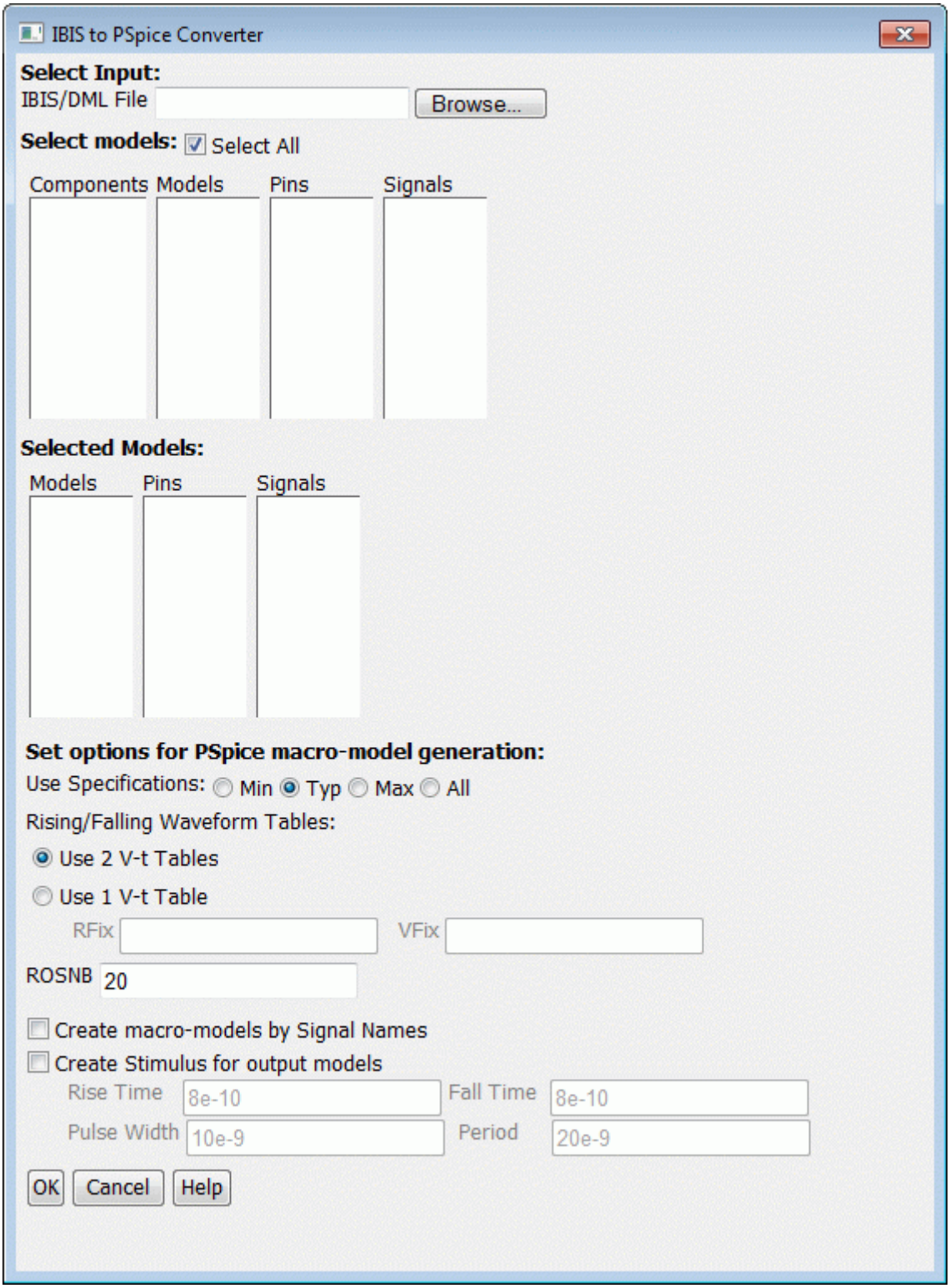
- A library file with the name `<Input File Name>.lib`. This file contains PSpice macro-models for all Buffer Models defined in the IBIS file. It might also contain wrapper models for all Signals defined in the IBIS file.

  The models corresponding to IBIS buffer models are named `<File Name>_<Component Name>_[Min|Max|Typ]` and the models corresponding to IBIS signals are named `<Signal Name>_[Min|Max|Typ]`.

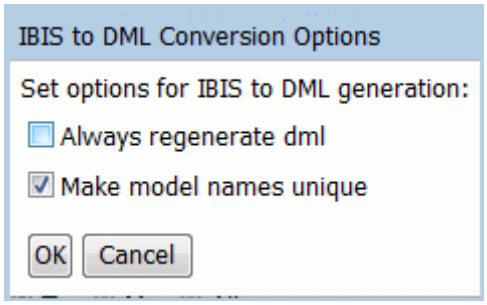
- A log file with the name `ibis2pspice.log`.

### Using Model Editor

In Model Editor open the new *IBIS to PSpice Converter* dialog box by choosing *Model – IBIS Translator*.


IBIS to PSpice Converter
Select Input:
IBIS/DML File
Browse...
Select models:
Select All
Components
Models
Pins
Signals
Selected Models:
Models
Pins
Signals
Set options for PSpice macro-model generation:
Use Specifications:
Min
Typ
Max
All
Rising/Falling Waveform Tables:
Use 2 V-t Tables
Use 1 V-t Table
RFix
VFix
ROSNB
20
Create macro-models by Signal Names
Create Stimulus for output models
Rise Time
8e-10
Fall Time
8e-10
Pulse Width
10e-9
Period
20e-9
OK
Cancel
Help

When you specify a IBIS or DML file, you can specify settings in the *IBIS to DML Conversion Options* dialog box.




In the IBIS to DML Conversion Options dialog box, select:

- *Always regenerate dml to* regenerate DML files. IBIS files are first converted to their equivalent dml files, and the dml files are then read. If *Always regenerate dml* is not selected, IBIS to dml conversion is not done if a dml file with the same name is already available and the dml is more recent that the IBIS file.
- *Make model names unique* to create models with unique names by prepending the file name to the model name.

In the IBIS Translator dialog box:

- Check *Select All* if you want to select all models. To select individual models, deselect *Select All* and then select the listed models.
- Select a *Use Specifications* option to select the type of models you want to generate: `typ` (Typical), `max` (Maximum), `min` (Minimum), or `all`. The default is `typ`.
- Select either *Use 2 V-t Tables* (default) to use two rising/falling waveform tables or *Use 1 V-t table* to use a single waveform table.

  If you select Use 1 V-t Tables, you can also specify the RFix and VFix values for the table that you want to be used for generating the PSpice model. By default, the V-t table with the lowest RFix will be used.

### Using the `orPSpiceParsers` Command

To translate IBIS models from the command prompt, enter the following command:

```
orPSpiceParsers.exe <IBIS File Name>|<DML File Name>
[parameter1,[parameter2]..]
```

Where parameter can be any of the following optional parameters:

| | |
|---|---|
| `-model <Model Name>` | Generates a sub-circuit for only the specified model in the output lib |
| `-type <typ\|max\|min>` | Generates model of the specified type, namely: `typ` (Typical), `max` (Maximum), `min` (Minimum), or `all`. The default is `typ`. |
| `-RFix <value> -VFix <value>` | Specifies the V-t table to be used for generating the output characteristics of the model. The default is to use V-t table with minimum `RFix`. |
| `-Use2Vt` | Uses two Rising/Falling waveform tables. By default, only one table is used. |
| `-ROSNB <value>` | Specifies the value of snub resistance to be added across `L_pkg`. By default `ROSNB = 20 ohms`. |
| `-stim` | Specifies that a stimulus is created automatically for the output and IO buffers. |
| `-pinModels` | Specifies that wrapper models for all signals defined in the IBIS file are also created. By default, PSpice macro-models are created only for the buffer models defined in the IBIS file. |

### Supported Keywords

Irrespective of the IBIS version, the translator supports the following keywords.

```
[Package]
                    R_pkg
                    L_pkg
                    C_pkg
[Pin]
                    signal_name
```

```
                    model_name
                    R_pin
                    L_pin
                    C_pin
[Model]
                    Model_type
                    Polarity, Enable
                    Vinl
                    Vinh
                    C_Comp
[Pulldown]
[Pullup]
[GND Clamp]
[POWER Clamp]
[Rising Waveform]
                    R_Fixture
                    V_Fixture
[Falling Waveform]
                    R_Fixture
                    V_Fixture
[Ramp]
```

## Multi-Core Engine Support

PSpice suports multi-core in 16.6. You can specify the number of threads or the engine default by setting the `THREADS` option, the syntax being:

```
.options THREADS=<value>
```

Where, value can be any postive integer. A value of `0` sets the engine default. Set the value to `1` for single thread.

## Configuring Menus and Toolbars

You can now customize the menus and toolbars in PSpice, PSpice Advanced Analysis, and Model Editor. As a result, any TCL methods that you want to be able to run from the menus is possible. You can also specify your own icons for the menus or toolbar items. The resource files for menus and toolbars including the icons are located at:

`<Cadence_installation>\share\orResources`

You can add menus through XML files where you specify:

- the menu label
- name of TCL method to be called on menu click
- location of the menu in existing menu items
- TCL method to enable and grey out the menu item
- an optional icon

You can also add dynamic menu items using TCL code.

**Note:** The pop-up menus cannot be customized.

## Encryption Enhancements



### New Algorithm

16.6 comes with the new AES 256-bit Encryption algorithm. This makes the encryption utility of PSpice and Model Editor both faster and more robust. You will still be able to decrypt models encrypted using DES algorithm in earlier releases.

### Command Line Modes

The `PSpiceEnc` command now has a new option to specify modes. The syntax being `mode <n>` or `Mode <n>`, where n can be `0`, `2`, or `3` as described below:

- `0`: Uses 16.5 version of encryption.
- `2`: Uses DES Encryption with advanced data security (available in 16.5).

- `3`: Uses AES Encryption. This is the default for 16.6 and later releases.

## New Models

| Model Types | Library | New Models |
|---|---|---|
| schottky diodes | `schottky` | `105` |
| Bridge rectifiers | `diode_fullbridge` | `119` |
| | `dual_diode` | |
| High speed diodes | `diode` | `26` |
| Zener diodes | `zener` | `11` |
| Ferrite metal core models for power application and signal conditioning | `magnetic` | `399` |
| Controllers for switching regulators | `micrel_stepdown_regulator` | `61` |
| Power Management: Special Purpose ICs | `micrel_stepup_regulator` | `29` |
| IGBT Module | `special_purpose_ics` | `3` |
| Analog Switches | `IGBT` | `3` |

# Fixed CCRs

The following lists the problems reported and fixed in PSpice 16.6. For detailed information about a fixed problem, contact your customer support.

| CCR ID | Description |
|---|---|
| CCMPR00008512 | Enhance Analog Data tips to display the bias information |
| CCMPR00010678 | Have the ability to reduce the resolution of data read into |
| CCMPR00011695 | Simulation seems to hang with large DAT output |
| CCMPR00022475 | spice concepthdl : visibility on each operating node |
| CCMPR00022614 | Stimulus editor crashes with the sequence of steps |
| CCMPR00025822 | Bias point (voltage and current) display in ConceptHDL |
| CCMPR00105149 | missing cd4046 part directory in Concept mix_misc library |
| CCMPR00177776 | AA controller should allow expressions for components |
| CCMPR00227655 | Curly brackets {} expressions should be supported in AA flow |
| CCMPR00416436 | how to pass parameter value in sensitivity analysis ? |
| CCMPR00555140 | Wrong error Vj is negative reported by simulator - Vj cannot be negative |
| CCMPR00624867 | Include the expression value in Sensitivity analysis |
| CCMPR00647097 | Cut paste moves traces but not moved correctly. |
| CCMPR00842675 | Default Maximum time step shows incorrect results |
| CCMPR00871572 | Enhancement: Add AutoConverge in probe window when convergence error occurs. |
| CCMPR00874962 | Temperature sweep generates Vj is negative |
| CCMPR00878355 | Unable to simulate with sub-circuit based part of a design which got created using Create Netlist > Pspice tab. |
| CCMPR00878770 | unix2dos should not be required on encrypted model |
| CCMPR00892333 | Ability to “save as” Capture-Pspice project directly along with all project related files. |
| CCMPR00892494 | Enhancement: Full encryption of spice model. |
| CCMPR00893597 | Material information disappears when you click next button under Data Entry > Core Details > Core. |

| | |
|---|---|
| CCMPR00916131 | Enhancement : Upgrading dat file version to support higher precision |
| CCMPR00940954 | Temperature sweep doesn't work if VJ is negative |
| CCMPR00955644 | Enhancement : Reduce memory footprint while reading multisection data files. |
| CCMPR00968479 | ENH:Update some pspice templates |
| CCMPR00973928 | BUG:Current source has opposite direction |
| CCMPR01023286 | BUG: Edit profile in pspice AA parametric plotter doesnt erset to 1000 |
| CCMPR01023336 | ENH:Include basic fuse part in pspie standard libraries |
| CCMPR01028606 | Copy paste of trace having -sign turns trace into expression |

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# What’s New in PSpice 16.5

This chapter describes the new features in the PSpice 16.5 release.

# New Features

PSpice[1] 16.5 brings you the following new features and enhancements:

- New PSpice Models in 16.5
- Partial Design Simulation

## New PSpice Models in 16.5

16.5 library has a range of new models that can be used in diverse applications. Following is a list of the model categories:

- MOSFET Drivers
- Alkaline Battery
- Supervisory IC
- Optocouplers
- Voltage Mode Control PWM Controller Models
- Offline IC Switches
- Power Inductors
- Solid State Relays
- Charge Pump-based DC/DC Regulator
- Integration of Operational Amplifier Models from Vendor

### MOSFET Drivers

Two new Dual Advanced Synchronous Rectified Buck MOSFET drivers, **ISL6614** and **ISL6612**, have been added with protection features.

The models are in the `swit_reg` library.

The following MOSFET drivers from MICREL have also been added: **MIC4120**, **MIC4123**, **MIC4124**, **MIC4125**, **MIC4126**, **MIC4127**, **MIC4128**, **MIC4129**, **MIC4223**, **MIC4224**, **MIC4225**, **MIC4416**, **MIC4417**, **MIC4451**, **MIC4452**

1. Depending on the license and installation, either PSpice or AMS Simulator is installed. The new features only available with the AMS Simulator license are also listed in this manual.

The models are in the `mfet_drvr` library.

### Alkaline Battery

**MX1500** a non-rechargeable 1.5V Alkaline (manganese dioxide) battery model has been added. The model has nominal voltage of 1.5V and operating voltage range of 0.75V to 1.6V.

This model is in the `battery` library.

### Supervisory IC

5 new supervisory IC models have been added for power monitoring in your microprocessor-based circuits.

- Microprocessor supervisory circuits
  - Models: **MIC705**, **MIC706**, **MIC707**, **MIC708**
- Microprocessor reset circuit
  - Model: **MIC809-5**

The models are in the `mic_sup` library.

### Optocouplers

18 new Optocoupler models have been added to the `mii_opto` library. The part numbers added are: **3N243**, **3N244**, **3N245**, **3N261**, **3N262**, **3N263**, **4N47**, **4N48**, **4N49**, **MII66158**, **MII66163**,**MII66164**, **MII66183**, **MII66189**, **MII66193**, **MII66223**, **MII66225**, **MII66227**

### Voltage Mode Control PWM Controller Models

The 22 new voltage mode control PWM controller models have been added for devices from leading IC manufacturers. These PWM models can be used in diverse fields such as:

- For voltage control for ASIC, CPU, DSP Core, and I/O.
- In power supply, such as in base-station, DDR, RAID control, Telecom and Networking, server and desktop computer subsystem, and distributed systems.
- As general DC-DC converters
- At distributed points of load power architectures

The PWM models are in the `swit_reg` library.

- Step-down regulator with integrated switches
  - Model: **MAX8643, MAX8643A**
- Step-down regulator with integrated switches (4A, 2MHz )
  - Model: **MAX15038, MAX15039**
- Internal-switch step-down regulator
  - Model: **MAX8566**
- Dual Step-Down Regulator
  - Model: **MAX8855**
- Step-down DC-DC regulator with internal switches
  - Model: **MAX15041**
- Low pin count, synchronous Buck controller with Power Good
  - Models: **TPS40192**, **TPS40193**
- Synchronous Buck controller with high current gate driver
  - Models: **TPS51163**
- Efficient integrated 8A sync Buck regulator for DDR applications
  - Models:**IR3831**, **IR3841**
- Efficient integrated 14A sync Buck regulator
  - Models: **IR3840**
- Efficient integrated 6A sync Buck regulator
  - Models: **IR3842**
- Efficient power step-down DC-DC converters
  - Models: **MAX5090A**, **MAX5090B**, **MAX5090C**
- Efficient power step-down DC-DC converters (500mA output current)
  - Models: **MAX5033A**, **MAX5033B**, **MAX5033C**, **MAX5033D**

### Offline IC Switches

Following four part numbers have been added for Offline IC Switches from Power Integration: **LNK302**, **LNK304**, **LNK305**, **LNK306.**

These models are available in the `swit_reg` library.

### Power Inductors

44 new models have been added for Power Inductors from Coilcraft.

These models are available in the `coilcraft_ind` library.

### Solid State Relays

The following Solid State Relays have been added: **HSR312**, **HSR312L**, **HSR412**, **HSR412L**, **CPC117N**, **CPC1150N**, **LH1501BAB**

These models are available in the `ssr` library.

### Charge Pump-based DC/DC Regulator

The following Charge Pump-based DC/DC regulators have been added: **TPS60500**, **TPS60501**, **TPS60502**, **TPS60503**, **LM2771**, **LTC3250**.

These models are available in the `cp_cnvtr` library.

### Integration of *Operational Amplifier Models* from Vendor

22 models from Microchip Technology have been integrated with PSpice.

These models are available in the `microchip_opamp` library.

## Partial Design Simulation

The 16.5 release comes with the productivity enhancing feature of partial design simulation. You can now identify individual components of any design, and, using the partial design simulation feature, simulate only selected portions. Using this feature, you can simulate different circuits in the design with different simulation profiles. You can also netlist only a particular portion of the design. In addition, you can compare and merge portions of a design quickly.

**Note:** This feature is available only with OrCAD Capture CIS.

For more information, see the *Using Partial Design Simulation* section in the *Designing for other EDA applications* chapter of the *OrCAD Capture User Guide*.

# Fixed CCRs

The following lists the problems reported and fixed in PSpice 16.5. For detailed information about a fixed problem, contact your customer support.

| CCR ID | Description |
|---|---|
| 575976 | Request for 66183 Optocoupler Model. |
| 596671 | Outputs from ADC from datacon library are not proper |
| 744656 | New PWM Controller PSpice model support |
| 747356 | Unmodeled pin exists |
| 749603 | Xtal library for crystals are not generating correct frequency |
| 750192 | IRHLUB7970Z4 model in the irf.olb library shows incorrect IDSS |
| 752902 | Capture crash on add library in place part, if syntax error in prp |
| 755933 | Question on BSIM Models |
| 764271 | AMS can not take values like 2k2 |
| 767454 | Bias display in hierarchy |
| 770472 | Invalid parameter error while simulating AD768 |
| 772464 | Error on part 14538 present in library IEC/CMOS2.OLB |
| 774174 | Pinout of Diode Part-Symbol in Library Does Not match IPC |
| 775009 | Error when simulate circuit with MAT01 |
| 776823 | Description of GaussUser distribution |
| 810126 | Description of GaussUser distribution |
| 816422 | Enhancement request to allow more value pair "_npairs" inside vpwl_re_forever source |
| 846248 | BJT description in pspcref guide under MOSFET section from 16.2 |