cadence®

OrCAD Capture: What's New

Product Version 16.6
October 2012

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Contents

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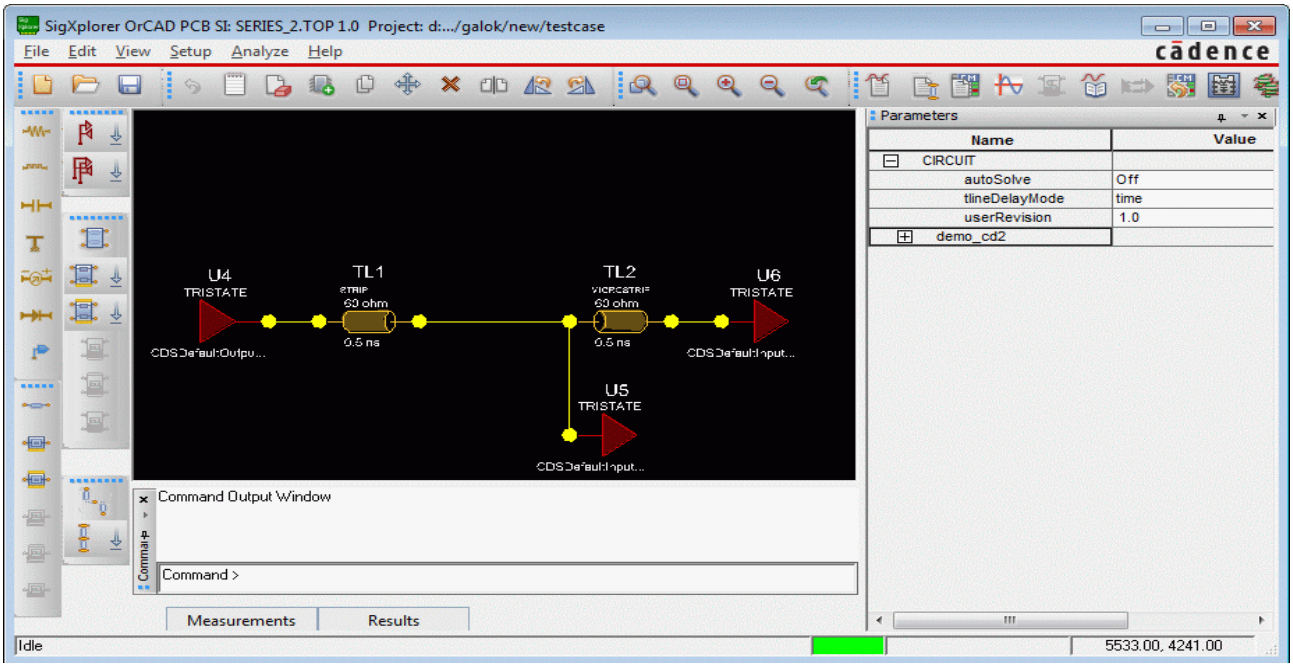
What’s New in OrCAD Capture 16.6

This chapter contains the following sections describing the OrCAD Capture 16.6 (henceforth referred to as Capture) release.

New Features and Enhancements

Capture 16.6 release brings you the following new features and enhancements:

Capture -SigXplorer Flow for Signal Integrity



You can now Launch SigXplorer on a flat net from OrCad Capture to perform Signal Integrity (SI) analyses and associate the Electrical Constraint set (Electrical Cset) to the flat net back to Capture from Signal Explorer. The complete topology file is also embedded into the DSN. OrCAD Capture also supports a distributed design environment for SI analysis by allowing you to export the net connectivity as topology files that can be updated using SigXplorer and then imported to OrCAD Capture.

OrCAD Capture provides you capabilities to set up SI libraries, assign SI models and then explore the signals in SigXplorer. You can also export and import Electrical Csets in Capture. In addition, you can audit Electrical Csets and model assignments.

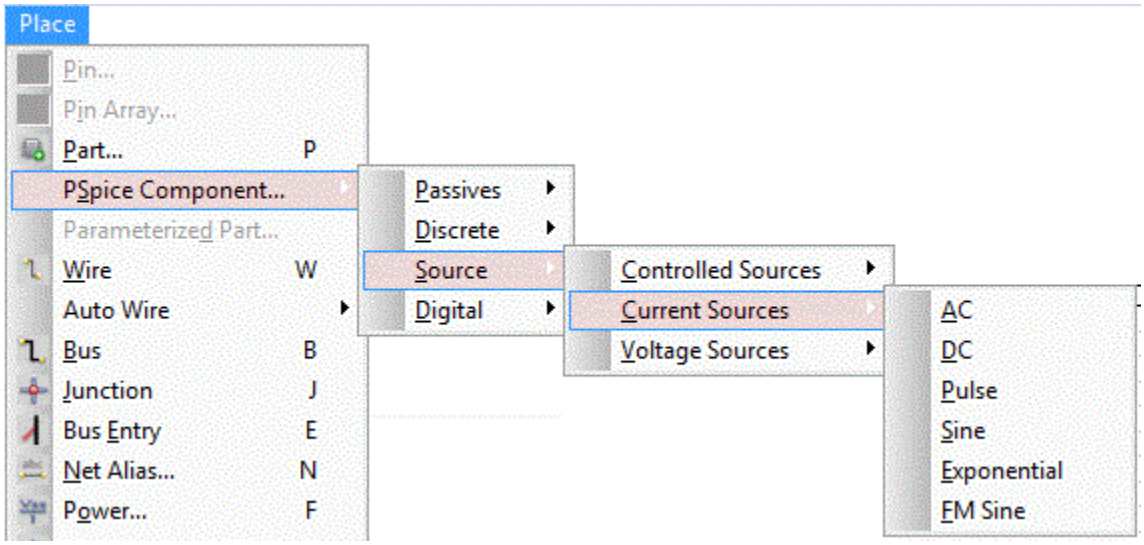
You can import the topology files to Allegro Constraint Manager and perform audit on topology files.

Video

To view a demonstration of this feature, click here.

Note: All Signal Integrity tasks are available under the *SI Analysis* menu in OrCAD Capture.

Placing PSpice Components from Menu



In 16,6, you can place PSpice components directly by choosing *Place – PSpice Component*. The menu items list parts categorized as the following:

Note: The devices added using this menu have ideal SPICE models

- Passive: R, C, L, Potentiometer, Coupling, Tline Ideal, Tline Lossy.
- Discrete: Diode, NPN, PNP, NPN Darlington, PNP Darlington
- Source:
  - Controlled sources: VCVS, VCCS, CCVS, CCCS
  - Current Sources: Ac, DC, Pulse, Sine, Exponential, FM Sine
  - Voltage Sources: AC, DC, Pulse, sine, Exponential, FM Sine
- Digital:
  - Gates: AND, OR, NAND, NOR, XOR, INV
  - Flip Flop: D, JK, RS, T
  - ADC: 8Bit, 10Bit, 12Bit
  - DAC: 8Bit, 10Bit, 12Bit
  - Memory:
    - RAM: 8kx1, 8Kx8

- ROM: 32KX1

Configuring Menus and Toolbars

You can now customize the menus and toolbars in OrCAD Capture, PSpice, PSpice Advanced Analysis, and Model Editor. As a result, any TCL methods that you want to be able to run from the menus is possible. For all menus in Capture, you can now customize the menu labels and status messages barring the menus being loaded from plug-ins such as the PSpice and PICFlow menus. You can also specify your own icons for the menus or toolbars items and customize the tool tip as well. The resource files for menus and toolbars including the icons are located at:

```
<Cadence_installation>\share\orResources
```

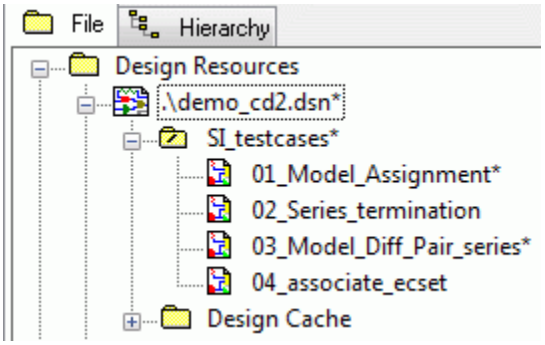
You can add menus through XML files where you specify:

- the menu label
- name of TCL method to be called on menu click
- location of the menu in existing menu items
- TCL method to enable and grey out the menu item
- an optional icon

You can also add dynamic menu items using TCL code.

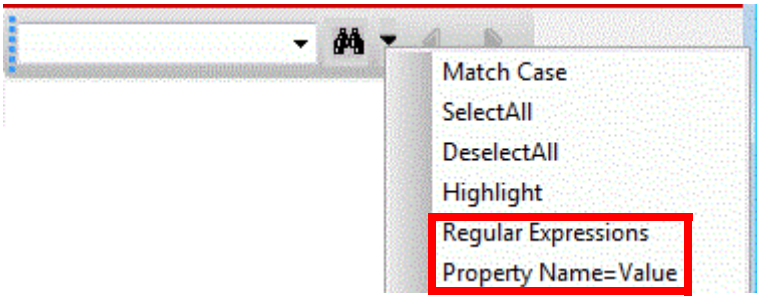
Note: The pop-up menus cannot be customized.

Enhanced Save Function for Design and Library



Pages that are changed and need to be saved are marked by the asterisk (*) symbol in the Project Manager. When you save a design, the marked pages are saved.

Enhancements in the Find Function



Two new advanced search features have been added in the Find toolbar in 16.6:

- Property Name Value support: Now you can search for any object type in capture by providing its complete property name and value pair as a search string. To search for an object with a specific property name-value pair, choose *Property Name=Value* option from the Find drop-down menu and specify the property name-value pair. For example, to search for parts with PCB Footprint value starting with `dip2`, use the search string `PCB Footprint=dip2*`.

  Note: Note that wildcard and question mark entries are only supported for the value string. You need to provide the complete property name in the search string.

- Regular Expressions support: To search using a regular expression, select *Regular Expressions* option from the Find drop-down menu and specify the regular expression as the search string. Find now supports all TCL regular expressions in the search string. For example, to search for all parts with references containing `R` or `C` followed by any number between `2` and `9`, use the search string `Part Reference=(C|R)[2-9]` with both *Property Name=Value* and *Regular Expressions* option selected.

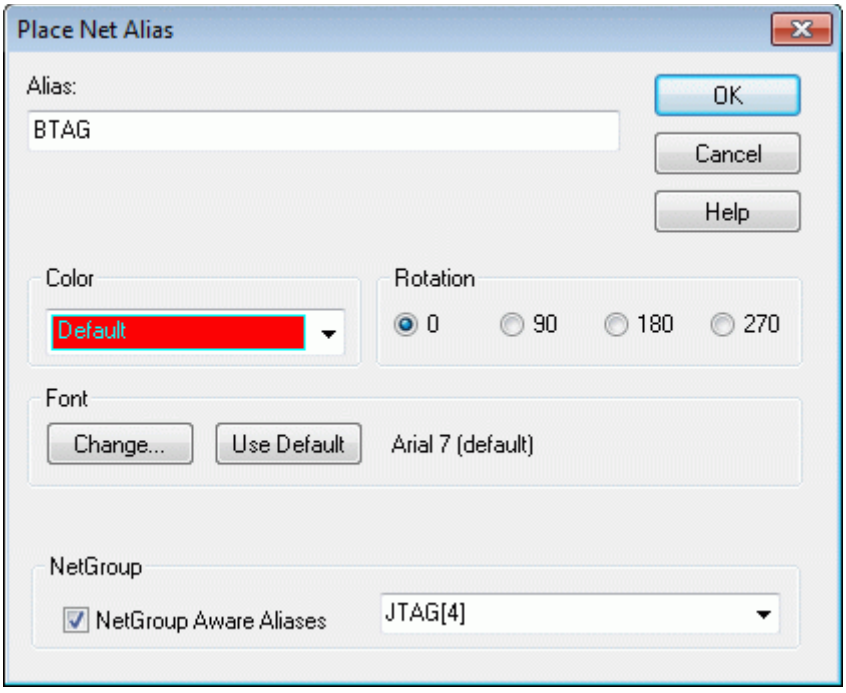
  Note: Note that with Regular Expressions search feature enabled, Find performs a complete match for a search string containing alpha-numeric characters, underscore (_) or space unlike the standard regular expression search in TCL. For any other characters or patterns in the search string, standard TCL regular expression search behavior is observed.

  Note: With *Property Name=Value* search enabled along with *Regular Expressions* search option, regular expressions search is supported only for the property value string.

Enhancements in the NetGroup Use Model

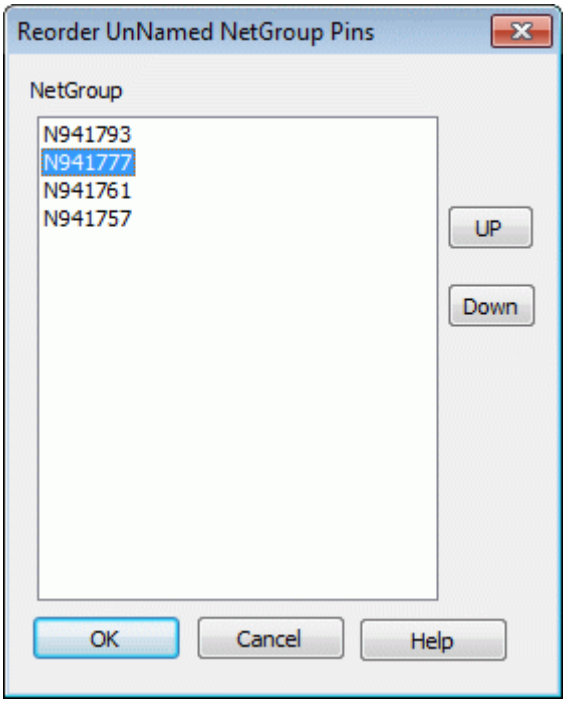
In 16.6 the NetGroup use model is aligned with the Bus use model to present an intuitive environment to the user.

Assign a NetGroup to a Bus



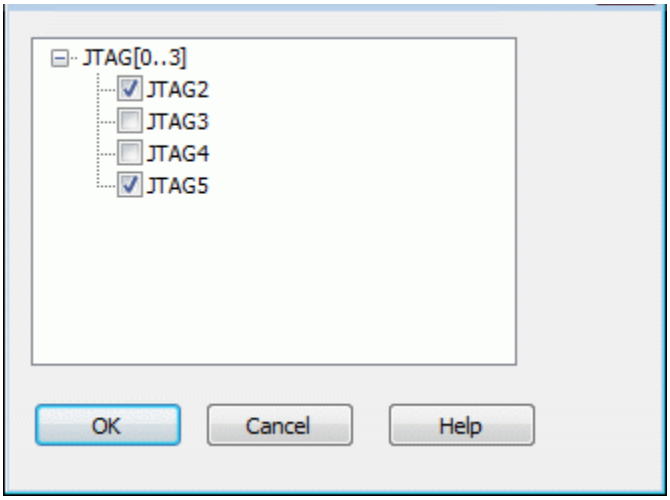
You can now place NetGroup aware aliases on a bus instance by selecting *NetGroup Aware Aliases*. You can either select an existing NetGroup from the list or edit the list to specify a new NetGroup. The width of the alias is updated from the specified NetGroup.

Reorder Pins in an Unnamed NetGroup



You can now reorder pins in an unnamed NetGroup. From the pop-up menu for an unnamed NetGroup on your schematic, choose *Reorder pins for UnNamed NetGroup*.

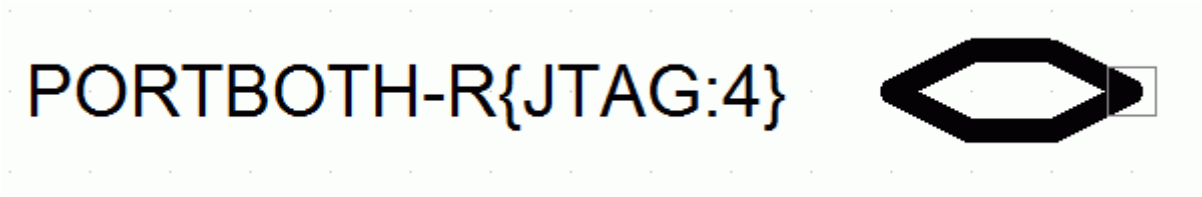
Add and Remove Pins from a NetGroup



You can now add or remove pins by choosing the *Add/Remove Pins on NetGroup Block* option for a placed NetGroup block.

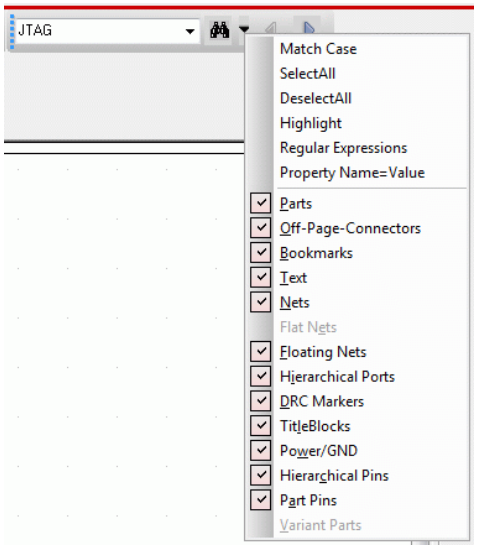
Visible NetGroup References

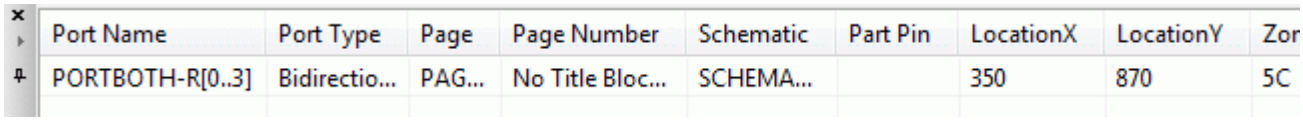
You can easily determine if any component in a design references a NetGroup by looking at the design, which shows the instance name followed by the NetGroup name and width in curly braces. For example, a hierarchical port `PORTBOTH-R` referencing the NetGroup `JTAG[0..3]` with width `4` is shown on the design as `PORTBOTH-R{JTAG:4}`.



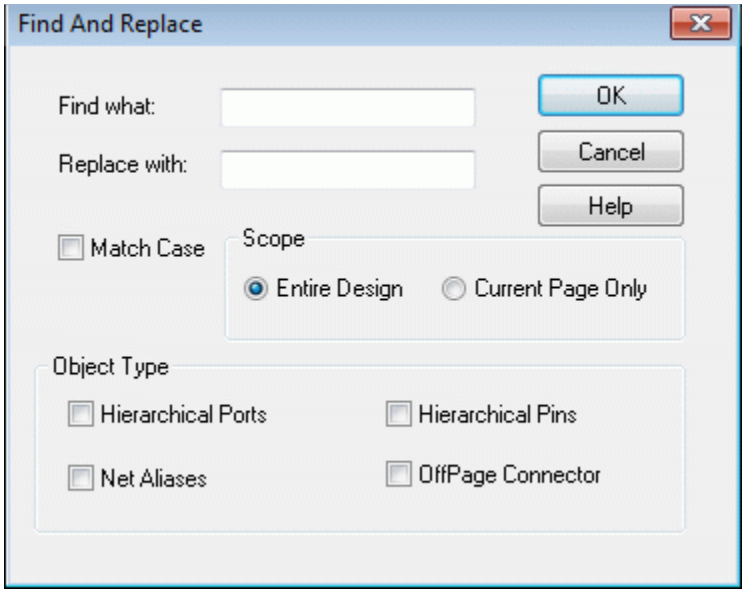
Find NetGroup References

When you search for a NetGroup, the result displays all objects, based on the filter, that reference NetGroups. For example, if your search for a NetGroup JTAG and a hierarchical port references this NetGroup, the result will display the port as shown in the figure.





Global Replace for OffPage

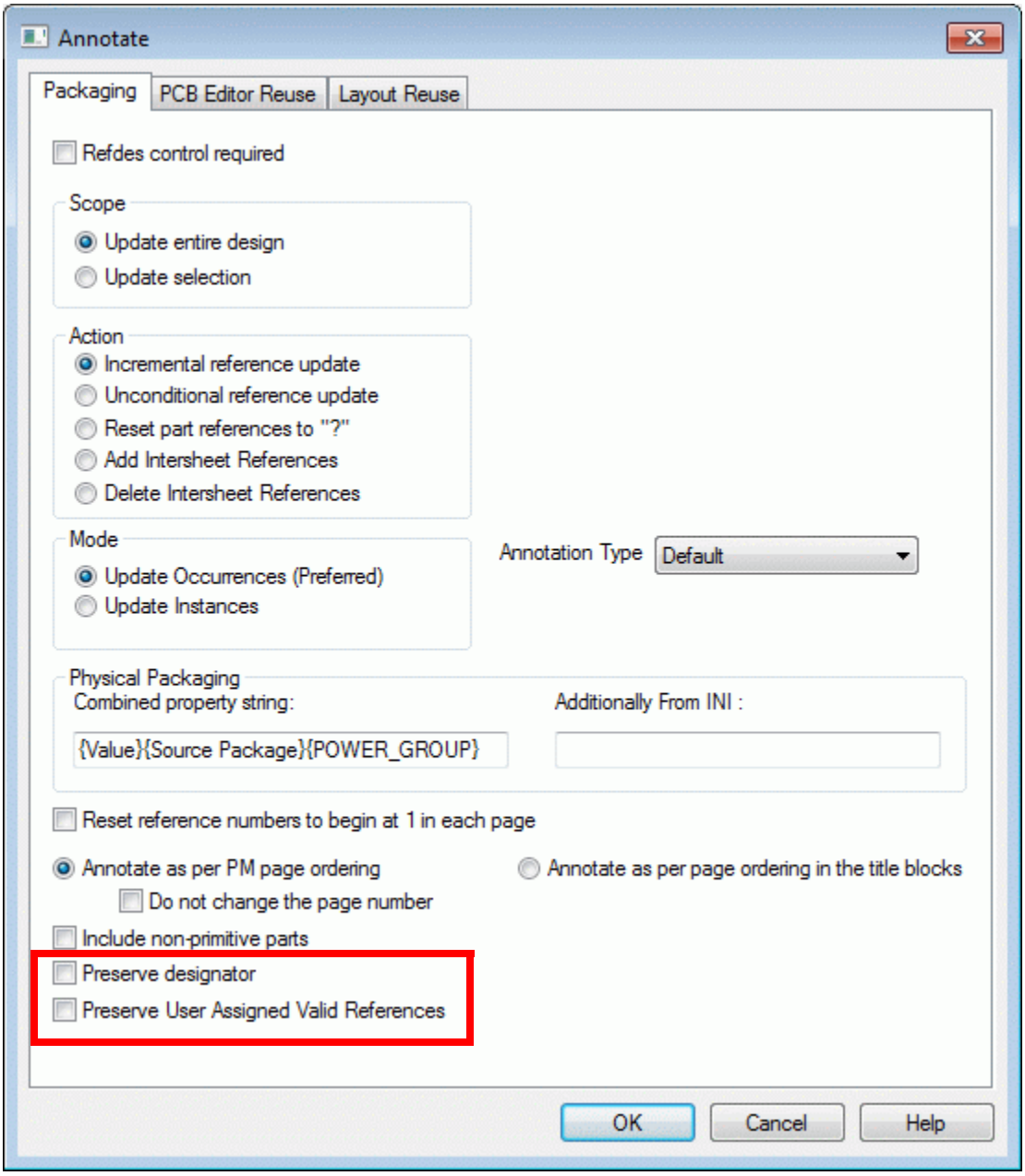


The Find and Replace dialog box (*Edit – Global Replace*) now has an option, *OffPage Connector*, to find and replace offpage connectors.

Enhancements in Cache Updates

You can now choose *Replace Cache* option from the pop-up menu for multiple cache parts.

Setting the User Assigned Flag



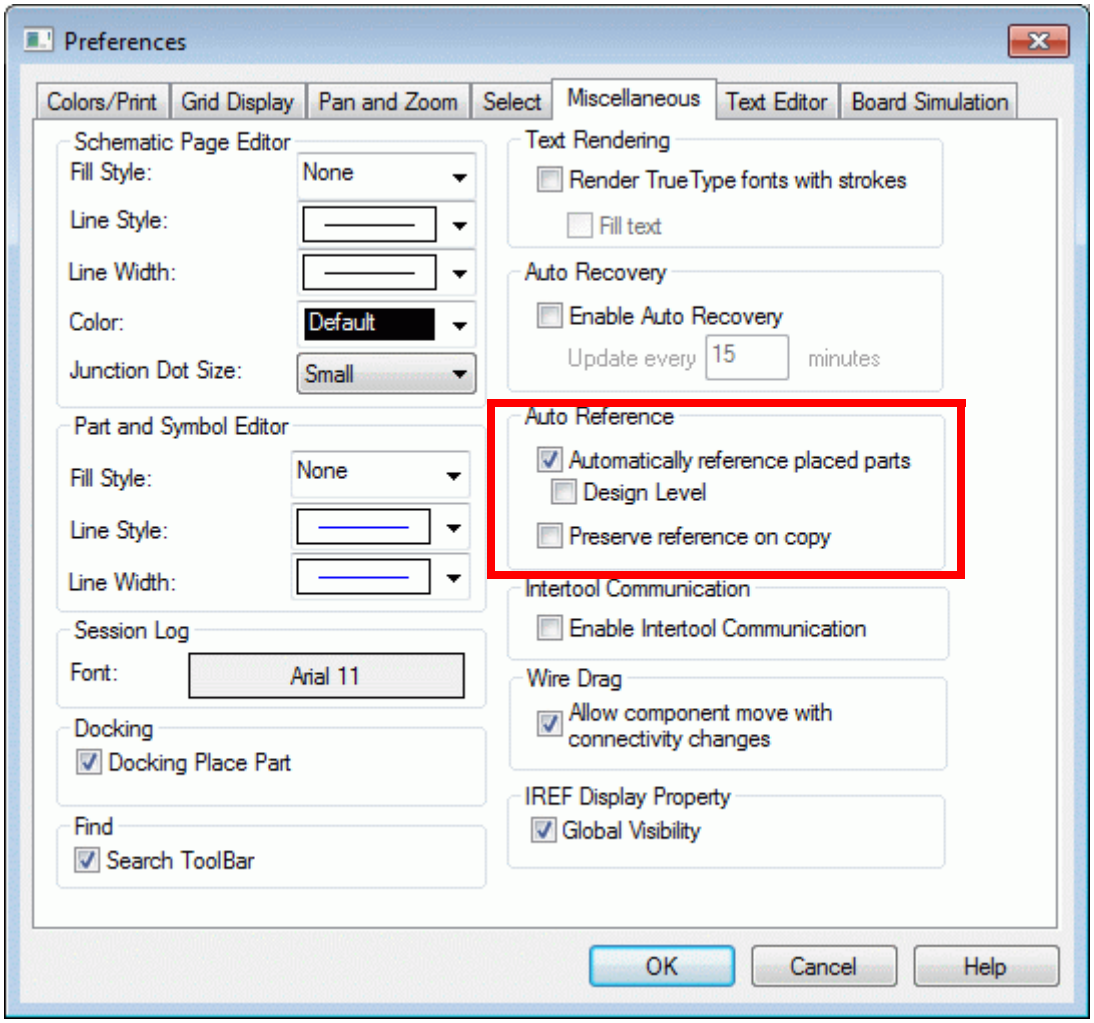
You can now set the newly added *User Assigned Flag* in OrCAD Capture to preserve designators and references in conjunction with the *Preserve designator* and *Preserve User Assigned Valid References* in the Annotate window.

You can mark references as user assigned by choosing *User Assigned Flag – Set* from pop-up menu of the part in the schematic editor or from the pop-up menu of the Reference property in the Property Editor.

OrCAD Capture marks a reference as user assigned if:

- Reference is changed in the Property Editor
- Reference is changed in the Schematic canvas
- Reference is changed in board (Back-annotation)

Design Level Auto Reference



In 16.6, in addition to schematic level annotation, you can also perform design level annotation by selecting the *Design Level* option in the Miscellaneous tab of the Preferences dialog box. You can also choose to preserve references when you copy by selecting the *Preserve reference on copy* option.

Database Compaction and Transaction

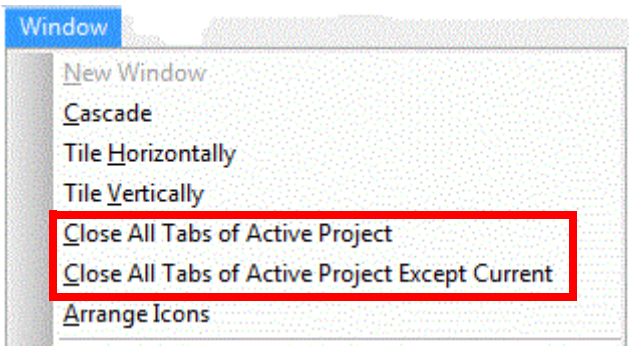
OrCAD Capture 16.6 DSN and OLB files are enhanced to:

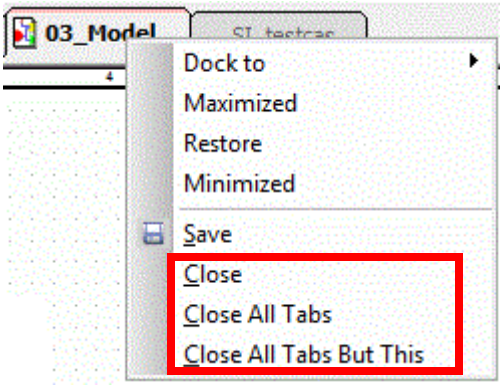
- Reduce size on deletion of image files
- Prevent corruption through enhanced database transaction

Browsing Designs Created Using Earlier Versions

You can open designs created using earlier version without uprevving the designs. You need to uprev such designs only when you save them.

Closing all Tabs



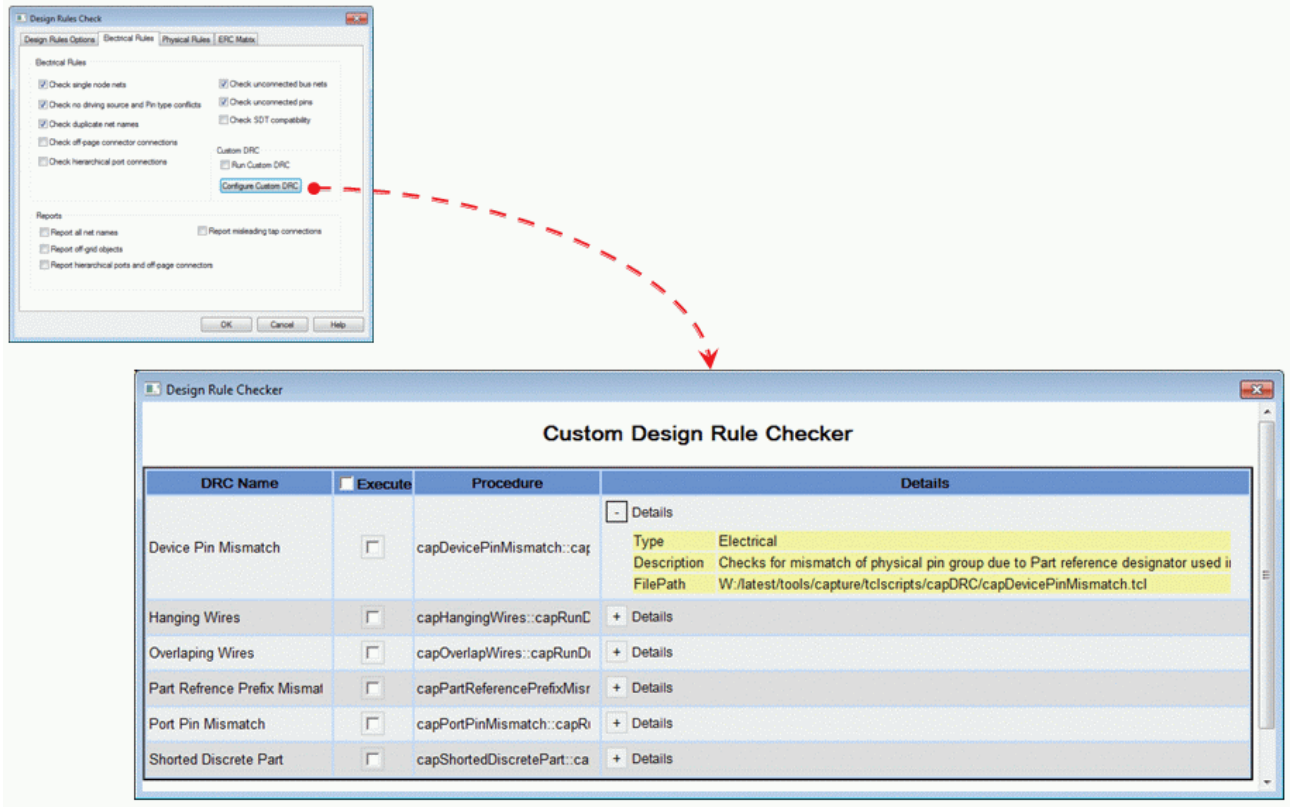


Now you can close all open tabs from the menu items with one click.

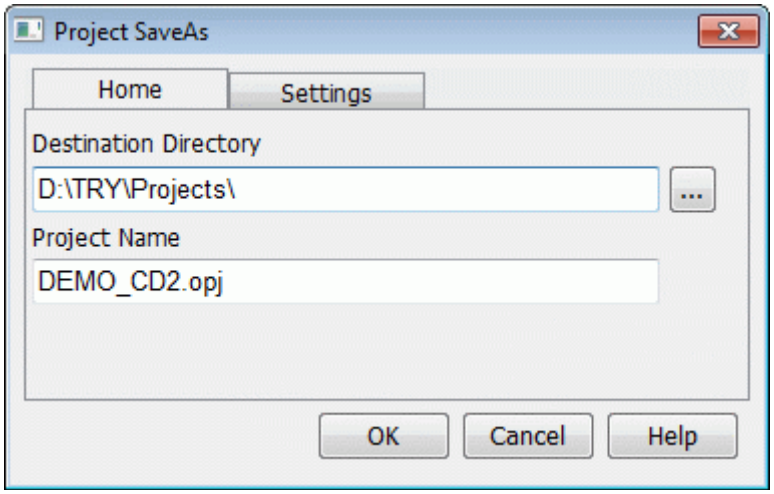
Design Rule Check (DRC) Enhancements

You can now selectively waive DRC by choosing the *Waive DRC* option from the pop-up menu for the DRC on the canvas.

You can also add you own DRC using TCL scripts. To do so, click *Configure Custom DRC* from the Electrical Rules tab of the Design Rules Check dialog box (*Tools – Design Rules Check*).



Project Save As Enhancements

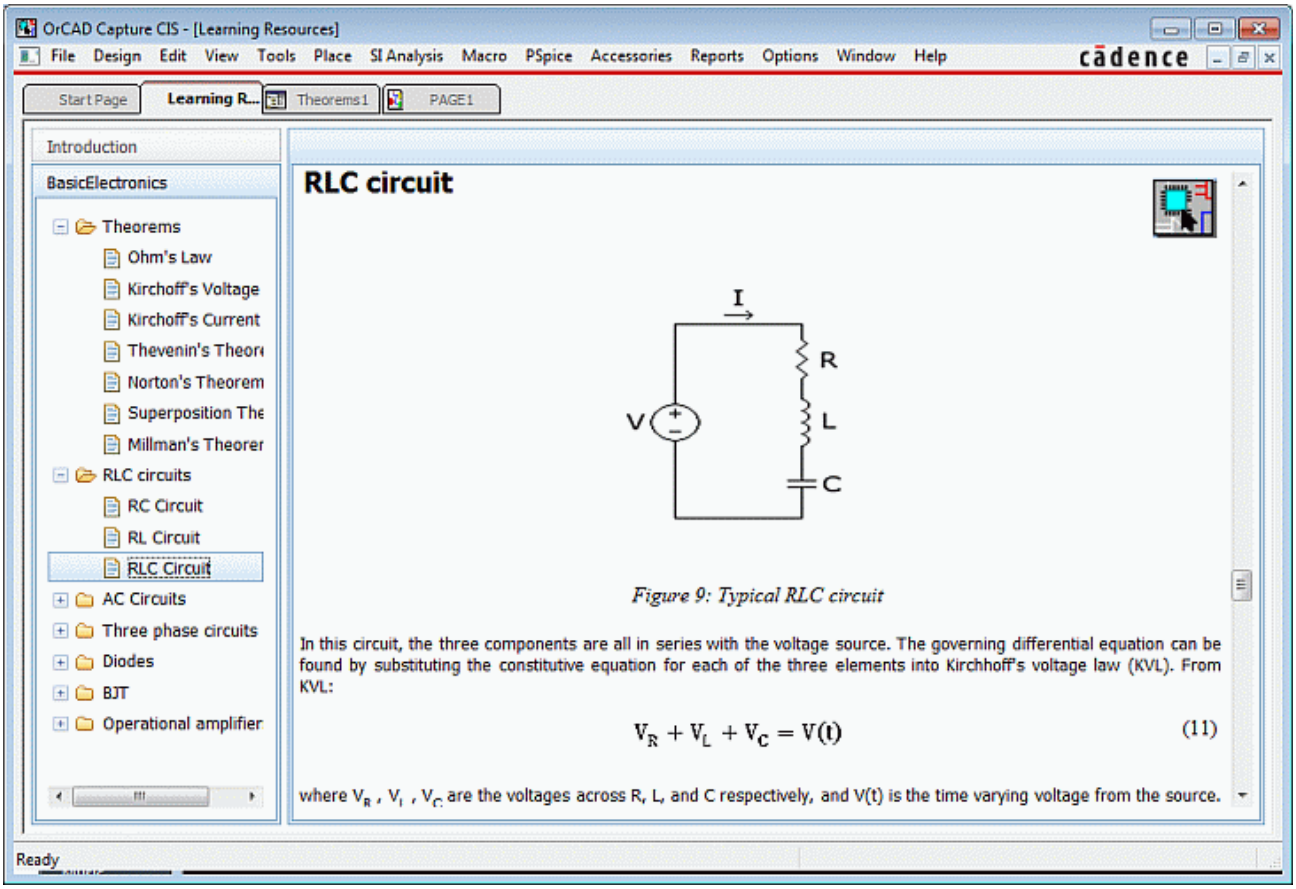


Project Save As functionality has been enhanced in 16.6 with the capability to save the associated files present inside or outside the project directory along with the project at the

new location while maintaining their internal and external links. Associated files include referred projects, designs, libraries, simulation profiles, output files and so on.

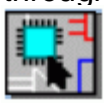
While saving a project in 16.6, you can specify a project name that is different from the design name.The Project Save As settings can be customized using the Settings tab of the dialog box which gives you the option to copy the design file along with the project and rename it. You can also selectively specify to copy the referred files present within or outside the project folder.

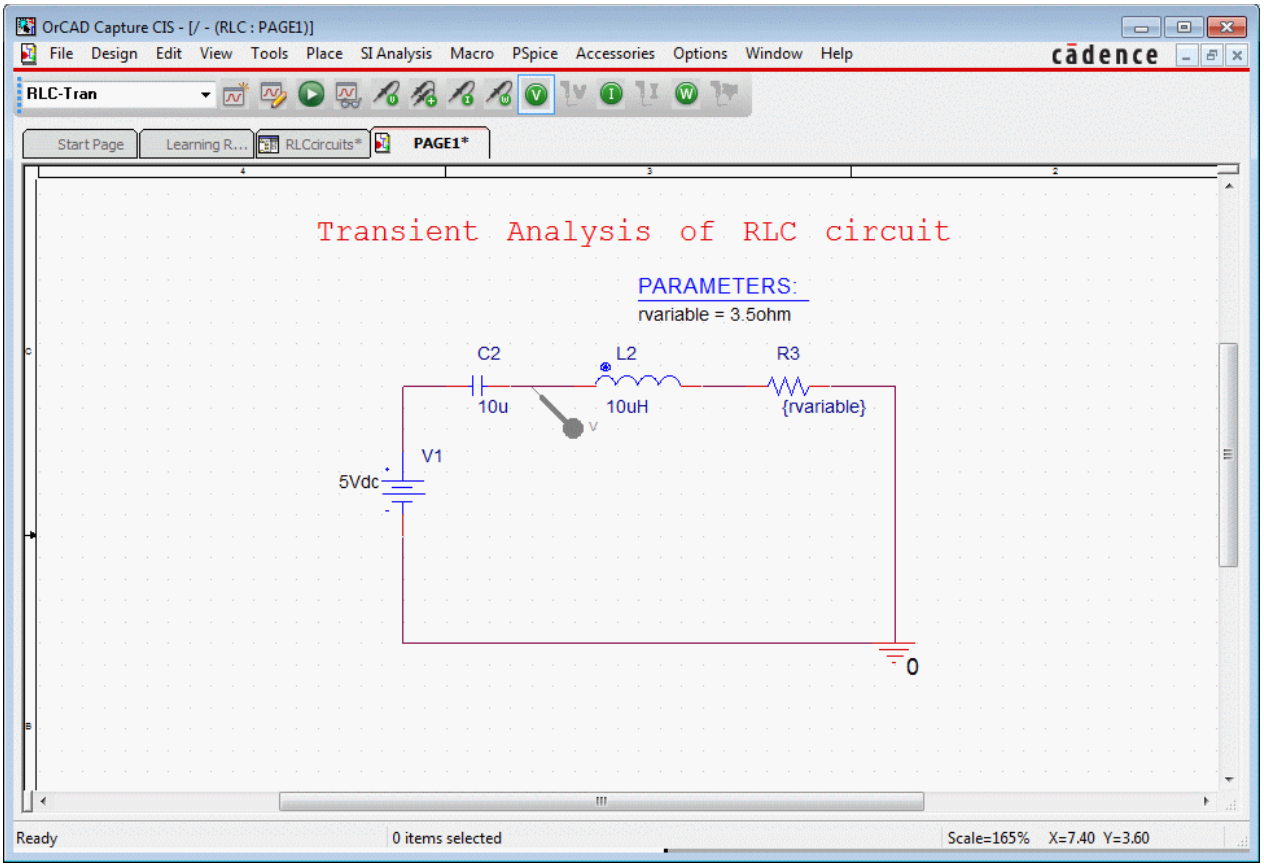
Learning Resources



To aid learning of various Electrical and Electronics Engineering concepts using OrCAD Capture and PSpice, a new option – *Learning Resources* – is made available in the OrCAD Capture Help menu.

The learning material covers several diverse topics, ranging from basic theorems to some of the advanced topics in the field of Electrical & Electronics Engineering. It also introduces basic Electronics Design Automation (EDA) concepts.

This is an interactive learning material that uses design created in Capture to explain the concepts. As you go through the module, you open the circuit relevant to the current module by clicking the icon () on the right.



When you choose *Help – Learning Resources* in OrCAD Capture, depending upon the installed resource modules, you may see one or more learning modules on different topics listed in the left pane. You can augment the list by installing additional learning resources.

Note: Ensure that Windows Internet Explorer 7 or or a later version is available in your system to be able to use Learning Resources.

Fixed CCRs

The following lists the problems reported and fixed in Capture16.6. For detailed information about a fixed problem, contact your customer support.

CCR ID	Description
12577	Resetting part references to ? resets the package designation
13642	Problems with replace cache when parts are copied to new DSN
20701	Annotation only change designator, treat reference as hard
28078	Connectivity incorrectly re-evaluated when port mirrored
33956	Ability to set gate id, annotate, keep gate assign, set refs
35310	Copying parts to a hierarchical page does not auto reference
55359	Two grid gap appears while placing wires
74510	Ability to turn off specific DRC markers.
111399	Option of invisible net alias
114709	Wire is missing at the starting upto 1.5 grid (approx.)
115833	Placing Sections of Heterogeneous parts need enhancement.
124736	Enhancement in DRC report
153574	Option of display enable/disable for Net Alias
158361	Capture Place wire looks unconnected
163978	DRC exception table or ignore option at pin level
176359	ABLE TO IGNORE DRC ON SELECTED NETS/ PINS
196584	drawing wires taking lots of time
232731	Why capture places Heterogeneous parts wrongly?
258906	Make net alias invisible in Capture

CCR ID	Description
270946	Wanted to lock some Part Reference values during annotation
273524	Duplicate references in Capture
294858	Capture hangs due to any operation on this design
337644	Edit while Place does not work for heterogeneous part
338235	Automatic synchronization for externally referenced designs
339378	Automatic synchronization for externally referenced designs
361079	Cannot see lengthy paths in "Select Directory"
373714	Reference"SATA0" will become "SATA"
377353	Performance issue in Capture while working with big design
381773	Why does CIS hourglass when copy pasting 1 part
381801	Method to lock "Designator"
385581	Option to lock refdes
396374	Hard_Location for part references
397503	Edit while Place does not work for heterogeneous part
435034	Auto reference placed parts does not work for hierarchical designs (DSN)
464453	Getting DSM0020: Unable to Paste Object Error
477438	Allegro Design Entry operating very slowly
479199	Replace cache doesn't work on same library path
480002	Global replace for Off page connector
509528	Replace Cache is not updating the timestamp resulting error DSM0020: Unable to paste object.
533895	DRC A method to check the Reference Designator Prefix

CCR ID	Description
536039	Why capture places Heterogeneous parts wrongly?
542653	Slow Capture Performance while selecting multiple nets
545360	Global Replace command not working for a bus
570012	Global replace for Off page connectors and Power/ Gnd
585841	Add PARTGROUP to Annotation and to the Heterogeneous part itself
620319	Automatic synchronization for externally referenced designs
621054	Renamed net in netlist isolates components from the rest of the net.
628823	Enhancement to enlarge select directory window size horizontally.
650011	Add PARTGROUP to Annotation and to the Heterogeneous part itself
650130	Option to disable power nets from cross probing
652202	Update the Select Directory window to current Windows look and feel
653792	ALG0078 while creating netlist
656562	Capture.ini path should be user's home location
673323	Star in tab system not functioning in same way for library and design
682645	Add PARTGROUP to Annotation and to the Heterogeneous part itself
691018	Option to lock refdes
691502	Option to lock refdes
692025	Close all the schematic pages
693632	Property similar to hard location which when put on a part will be skipped while annotation even with Unconditional refer

CCR ID	Description
694609	Property similar to hard location which when put on a part will be skipped while annotation even with unconditional refer
702468	Enhancement for advanced search parts with specific property values.
713626	Closing Multiple Schematic Pages at once
726621	Command to close all open tabs of a design except "Project Manager".
736980	Add PARTGROUP to Annotation and to the Heterogeneous part itself
740538	Option to close all opened schematic pages only in Capture.
743894	Add PARTGROUP to Annotation and to the Heterogeneous part itself
750501	Method to lock "Designator"
751388	Function to close all open tabs of a design except "Project Manager".
756925	Capture update file or directory browser to new Windows style
767749	Graphic line property like color does not change after save
776027	Ability to re-size the "Select directory" for netlist window.
788944	Add PARTGROUP to Annotation and to the Heterogeneous part itself
790111	Why capture gives "could not find .dsn" message when opening pspice design for the second time?
790414	P-CAD schematics get crash when converted to Capture.
791392	DRC check where two terminals of any discrete part tied to same POWER/GND net
795861	Add PARTGROUP to Annotation and to the Heterogeneous part itself

CCR ID	Description
797862	Ability to open 16.2 design (only to view) in v16.3 without converting it
797898	Option to retain schematic level property while linkdatabase part.
800346	Way to auto increment refdes across schematic folders within design
819020	Getting DSM0020: Unable to Paste Object Error
821994	Move Pin Text when creating a new symbol
834091	Ability to move pin name and pin numbers at library level
845314	Ability to ignore parts during annotation
846373	Date format under Design Properties
848582	Command to close all open tabs of a design except "Project Manager"
849408	Designator doesn't gets assigned to heterogeneous part if designator is changed after selecting part
850844	exclude a selection within a page from annotation
851830	Ability to disable cross-probing for specific net in one direction (Allegro to Capture).
852836	Ascend hierarchy option grayed out
854472	Select Directory window is very narrow. Directory selection is difficult for long directory names
858454	Component gets locked if project closed with Part Editor open
866699	Ability to crossprobe with filter like parts / nets
866784	Ability to move pin name at library level
869528	Refdes increment on copying part is not with respect to occurrence value.
872379	Closing schematic windows or tabs all in one
873521	Could not find *.dsn warning when opening project

CCR ID	Description
873550	Function to sort parts by library name in Design Cache
879218	Copying a pin with help of CTRL key is giving error for overlapping pins
882575	Option to disable cross probing for power/ground nets.
884192	DRC for H-pin and H-Port mismatch
887096	Editing excel doc (OLE object) after zooming into schematic affects size of spreadsheet on schematic
887202	Intersheet reference for H-ports should be like as of offpage connectors
889816	Cross probing of power nets from Allegro causes Capture to hang
889826	Diff Pairs not being created automatically even with _P & _N net syntax
890720	Script to place the entire Orcad library in one DSN file at once
894726	ISO 8601 for naming archive
895496	Capture should remember the docked position for a project
896315	Heterogeneous part's section not updated on changing it
896817	New TCL/TK commands help for attached file containing CIS TCL interfaces
898029	To show net alias clearly in print out if alias has underscore
904366	Junction dots get added or deleted which changes in the net name when rotating the design
905538	User should be able to change the bundle block
907977	Cadence Product Choices dialogue box is not wide enough to display entire name of products
908810	Web resources link are not pointing to correct pages

CCR ID	Description
908893	TCL: Waiving DRC's in Capture as being done in PCB Editor
914262	Disable CIS warning Cannot place database part
921919	The H block reference must be picked from occurrence value
925830	Option to lock refdes
930217	Net aliases doesn't gets assigned to bus bits if bus name is checked in NETGROUP.
931719	Option to lock refdes
931781	For Link "selected occurrence only" - DoNot Display Update Symbol Dialog
935147	ORCAD Suppress Warning in Create Netlist>Setup issue while creating Netlist
938730	While auto referencing the parts to be placed, Capture doesn't look for similar refdes existing in the lower hierarchy
942514	Docking state of Project manager window is not remembered when a project is closed and reopened
944045	User would like to be able to replace cache on several parts at once
952741	Uprev process should save the existing 16.2 design on open
964950	Modifying pin names using Split part command is not updating the part.
968679	Option to close all open schematic pages.
969564	Waive DRC option in Capture, as is available in PCB Editor
970133	Properties displayed in datatip should be customizable
975684	Reviewing lower version design on higher version should not change the database format

CCR ID	Description
977238	Last column in browse spreadsheet can't be increased in width till other columns are narrowed
979770	Update netgroup box at change
982720	Option to preserve section of homogeneous package in annotation.
985385	Data-tip of pins should be more informative
988097	Add Off page connector in Global Replace dialogue box.
989103	How to create a new menu with TCL script in Capture
992941	ERROR(ORCAP-19005) occurs when user tries to open second Capture application
997521	Back annotation doesn't work if user renames refdes as per grid based
998469	Add 'NET_SHORT=YES' as default in allegro.cfg
999421	Enclosed Polyline goes black and white when moved
1000127	Incremental annotation creates duplicate refdes
1000419	Net properties to be displayed on tooltip
1000506	Replace part in Design Cache not updating the values when same library is selected
1001684	Backannotation does not work if refdes is lowercase
1005805	Project Manager not docked as set
1010988	ADD ISO 8601 Date Time format to Capture
1011871	The H block reference must be picked from occurrence value
1012008	Option to remove symbols (! and ^) from Irefs.
1012459	The error message "ERROR(ORCAP-19005)" is not descriptive
1014750	Bus shown as bundle in netgroup
1019868	Warning(ORCAP-1589) Net has two or more aliases

CCR ID	Description
1023433	Finer mouse zooming
1024471	DRC doesn't report if both the pins of a 2 pin device are connected to same net.
1029589	Drawing diagonal wires in Fisheye view mode causes crash
1031521	While auto referencing the parts to be placed, Capture doesn't look for similar refdes existing in the lower hierarchy
1033179	Finding Power\GNDs in Capture highlights other power and GND symbols.
1033822	Function to only annotate newly added parts in bottom design of hierarchy
1041492	Pin names of pins placed on right boundary of part must start from same X location
1044724	Suppress warning feature not working correctly.

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What’s New in OrCAD Capture 16.5

This chapter contains the following sections describing the OrCAD Capture 16.5 (henceforth referred to as Capture) release.

New Features and Enhancements

Capture 16.5 release brings you the following new features and enhancements:

Usability Enhancements

In OrCAD 16.5, OrCAD Capture ships with enhancements to provide an improved usability experience to users. These include features that like object locking and placement reports.

Following are some of the usability enhancements in 16.5:

Graphical Operation (GOp) Locking

The GOp locking feature in Capture now allows you to lock the different parts of a schematic design. You an lock the objects on a page, you can lock a page, a folder or even the complete design. This feature will prevent you from inadvertently moving or deleting parts of a design that are locked. You will need to explicitly unlock the part of a design that you want to alter.

Placement Report

You can now generate a report of the X and Y locations of the placements of the parts on a schematic.

This report, generated as a .CSV file, provides the following details of the parts:

- Reference designator
- Part name
- Schematic name
- Sheet number
- File system location of the part library

- X co-ordinate location
- Y co-ordinate location

For more information see Creating a placement report.

Find Result Reports

After you execute the Find command on a design, you can generate a report (in CSV or HTML format) for the results from the command. If you run the Find command to search for different types of objects in a design, the search results will display in different tabs of the Find window. In this case, you can export the data from each tab.

Introduction of NetGroup

OrCAD Capture introduces the concept of the **NetGroup** that allows you to create groups of nets. A NetGroup can include a group of scalar nets, vector nets or a combination of both scalar and vector nets.

Capture allows you to create **Named** NetGroups that can be used across a design or exported to other designs. Alternatively, for one-time use, you can create an **Unnamed** /**Ad-hoc** NetGroup.

The new **NetGroup Connector** can be used to intelligently merge and tap out signals. It can also be used to generate net names for connected signals.

Fixed CCRs

The following lists the problems reported and fixed in Capture16.5. For detailed information about a fixed problem, contact your customer support.

CCR ID	Description
9624	Bus elements should be allowed to have two name (bundled bus
18949	intersheet references
44619	intersheet reference Y direction option
218072	write session log as a file in working dir to debug crash
278638	EMI: Intersheet refs fail with error8001 due to dup titleblk
295079	Create a bundled net
521754	Assign nets to Bus
569920	Enhancement:generic bus names
676210	Enhancement for correlate lower level pages with H blockes in PDF
695197	MMBT2222A/SOT has incorrect pinout
709341	function "DisplayProperty" puts property in wrong place
715550	Enhancement: get current location and perform the operation usign macro
721008	Need to create multiple libraries like RESISTOR.OLB automatically
721242	Update cache should reset the visible property locations
722344	Ability to have more than one array of nets travel on a bus
732850	Copying to Type column in Split Part view is not working
734334	Incorrect DOC description for DRC warning DRC0042

CCR ID	Description
734365	What kind of problem user may experience at board level if user violates warning DRC0042?
737660	Why lock files are generated whenever a power symbol is placed from the library 'sources.olb'.
740341	Draw Tool Bar re-appears automatically even if it is unchecked under Tools > Customize
749163	The special character { is corrupting BOM report.
749211	Capture crash while doing a controled annotation on the design
749215	Incorrect pins descriptions on OP467/SO in OPAMP.OLB
749663	Enhancement request on Push Occ properties to instance window
750436	Error [ALG0080] Inconsistent pin-number values
753933	Why Schematic Page Count and Schematic Page Number values are 0 in property editor of title block
761666	Tcl Script opens as text file when executed from Windows Command line with Capture already open.
766459	Problems with DRC0037 warning
768671	OrCAD DSN File Page Lock Function
769737	Unable to move properties
769849	visible property cannot be moved
770068	Step for unlocking part is missing in capture user guide.
772322	Unable to disable Draw Toolbar
774862	Users can not reposition the displayed name and value of a new added property in Capture CIS ISR 007
785742	Enhancement to add one common property to all the parts in library at once.
788270	Capture crashes while doing Clean up cache

CCR ID	Description
793284	Draw toolbar re-appears
795323	Tools > Create Netlist should not launch PCB Editor even on failure of netlist
798486	Time stamp in DRC report
803345	Enhance Doc to update that 'Update/Replace Cache' does not always change the PCB Footprint/Package property
804601	New added property value on symbol is not moving
807938	ENH - Place Pin Arry does not remember all previous settings
807973	Error in Existing pin overlayed dialog
827547	UNDO/REDO Data on Save option is absent
828001	Goto Bookmark works only for selected page
833050	TCL command for PAGE RENMAE doesn't invokes the rename dialogue box.
837715	Cannot Place No Connect if not on Toolbar