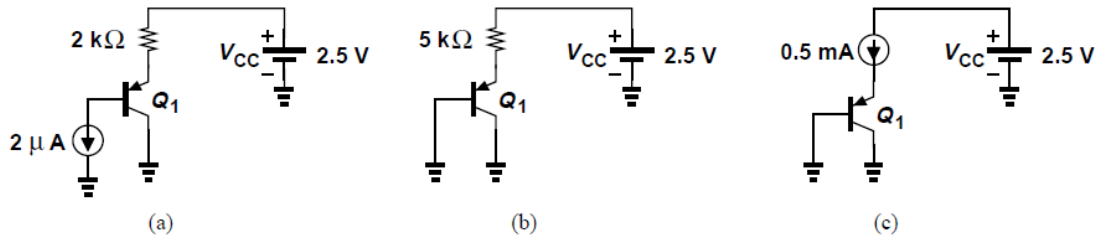
# LISTA DE EXERCICIOS #1

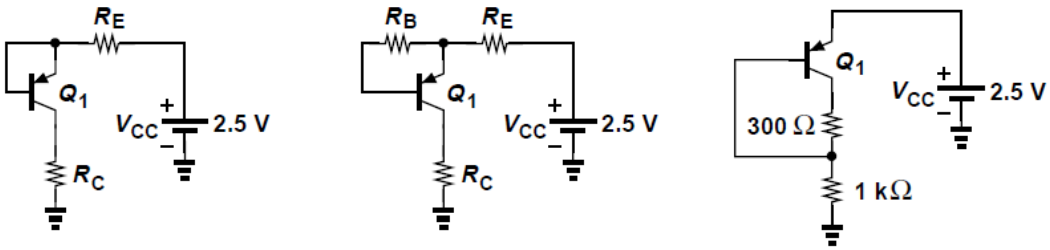
**44.** Determine the operating point and the small-signal model of $Q_1$ for each of the circuits shown in Fig. 4.75. Assume $I_S = 3 \times 10^{-17}$ A, $\beta = 100$, and $V_A = \infty$.




(a) (b) (c)

**Figure 4.75**

**52.** Determine the region of operation of $Q_1$ in each of the circuits shown in Fig. 4.80. Assume $I_S = 5 \times 10^{-16}$ A, $\beta = 100$, $V_A = \infty$.




(a) (b) (c)

**53.** Consider the circuit shown in Fig. 4.81, where, $I_{S1} = 3I_{S2} = 5 \times 10^{-16}$ A, $\beta_1 = 100$, $\beta_2 = 50$, $V_A = \infty$, and $R_C = 500\,\Omega$.

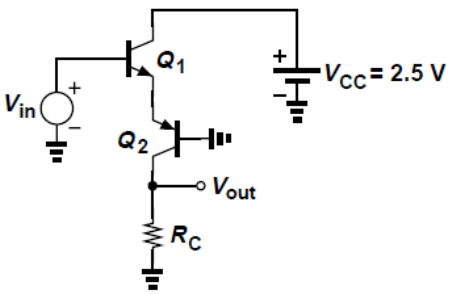



**Figure 4.81**

(a) We wish to forward-bias the collector-base junction of $Q_2$ by no more than 200 mV. What is the maximum allowable value of $V_{in}$?

(b) With the value found in (a), calculate the small-signal parameters of $Q_1$ and $Q_2$ and construct the equivalent circuit.

**6.57** The NMOS transistor in the circuit of Fig. P6.57 has $V_t = 0.5$ V, $k_n'W/L = 2$ mA/V$^2$, and $V_A = 20$ V.

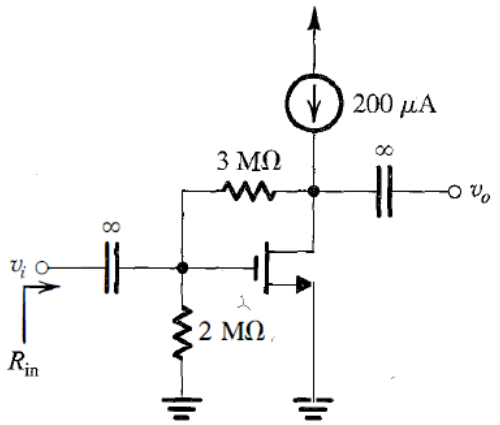



**FIGURE P6.57**

(a) Neglecting the dc current in the feedback network and the effect of $r_o$, find $V_{GS}$ and $V_{DS}$. Now, find the dc current in the feedback network, and verify that you were justified in neglecting it.
(b) Find the small-signal voltage gain, $v_o/v_i$. What is the peak of the largest output sine-wave signal that is possible while the NMOS remains in saturation? What is the corresponding input signal?
(c) Find the small-signal input resistance $R_{in}$.

**6.124** The BJTs in the Darlington follower of Fig. P6.124 have $\beta_0 = 100$. If the follower is fed with a source having a 100-kΩ resistance and is loaded with 1 kΩ, find the input resistance and the output resistance (excluding the load). Also find the overall voltage gain, both open-circuited and with load.

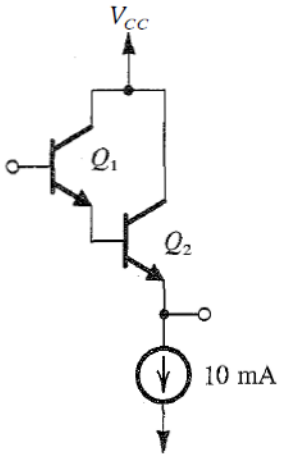



**FIGURE P6.124**