Agilent Technologies

Advanced Design System 1.5

Power Amplifier DesignGuide

December 2000

Notice

The information contained in this document is subject to change without notice.

Agilent Technologies makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Agilent Technologies shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

Warranty

A copy of the specific warranty terms that apply to this software product is available upon request from your Agilent Technologies representative.

Restricted Rights Legend

Use, duplication or disclosure by the U. S. Government is subject to restrictions as set forth in subparagraph (c) (1) (ii) of the Rights in Technical Data and Computer Software clause at DFARS 252.227-7013 for DoD agencies, and subparagraphs (c) (1) and (c) (2) of the Commercial Computer Software Restricted Rights clause at FAR 52.227-19 for other agencies.

Agilent Technologies
395 Page Mill Road
Palo Alto, CA 94304 U.S.A.

Power Amplifier DesignGuide User Manual

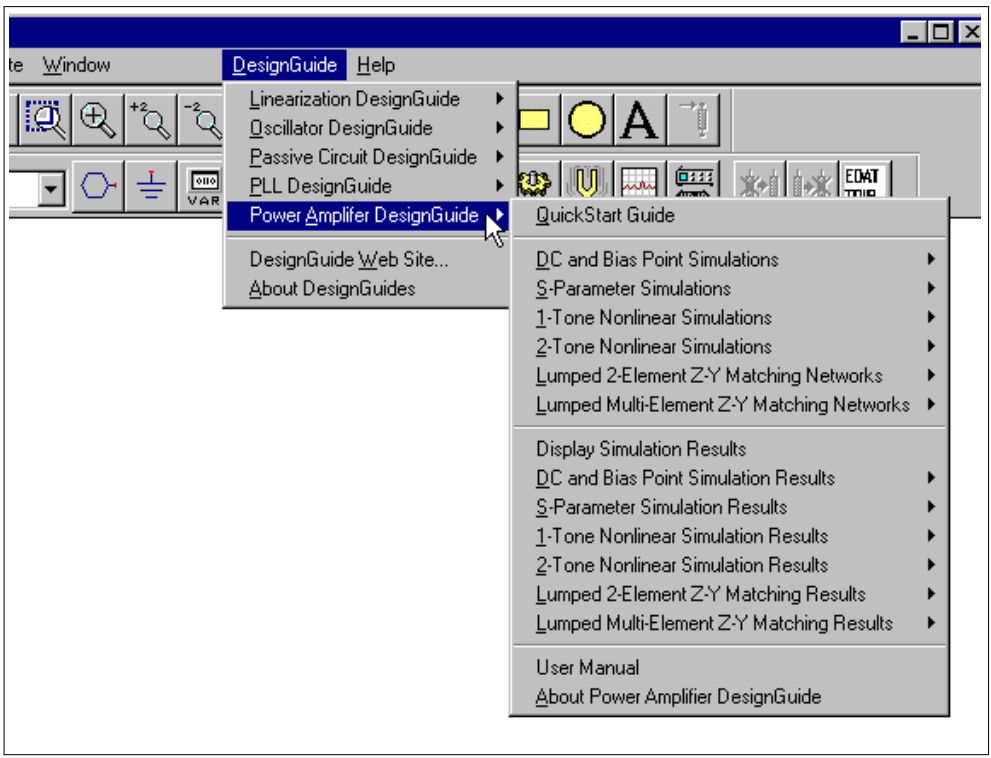
Chapter 1: Power Amplifier QuickStart Guide

The *Power Amplifier QuickStart Guide* is intended to help you get started using the Power Amplifier DesignGuide effectively. For detailed reference information, refer to chapters 2 through 8 of this manual.

The *Power Amplifier DesignGuide* includes many useful simulation setups and data displays for power amplifier design. The simulation setups are categorized by the type of simulation desired and the type of model available. Most of the simulation set-ups are for analysis, but there are some for synthesizing impedance matching networks. The DesignGuide is not a complete solution for power amplifier designers, but provides some useful tools. Subsequent releases of this DesignGuide will include an expanded range of features.

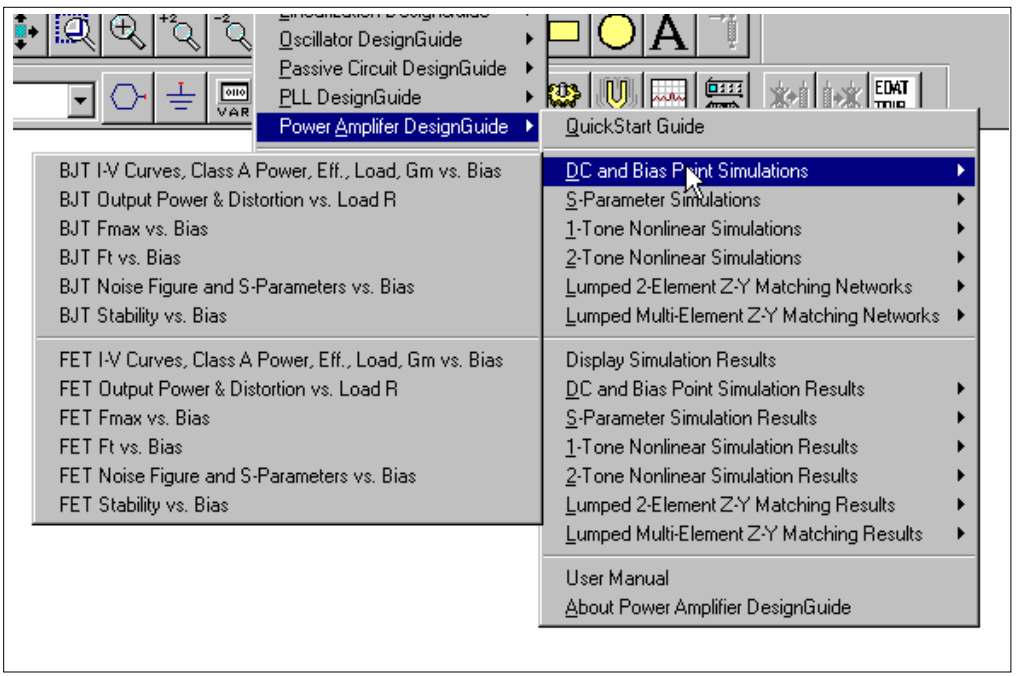
Using the Power Amplifier DesignGuide

The features and content of the *Power Amplifier DesignGuide* are accessible from the *DesignGuide* menu found in any Advanced Design System Schematic window, as shown here.



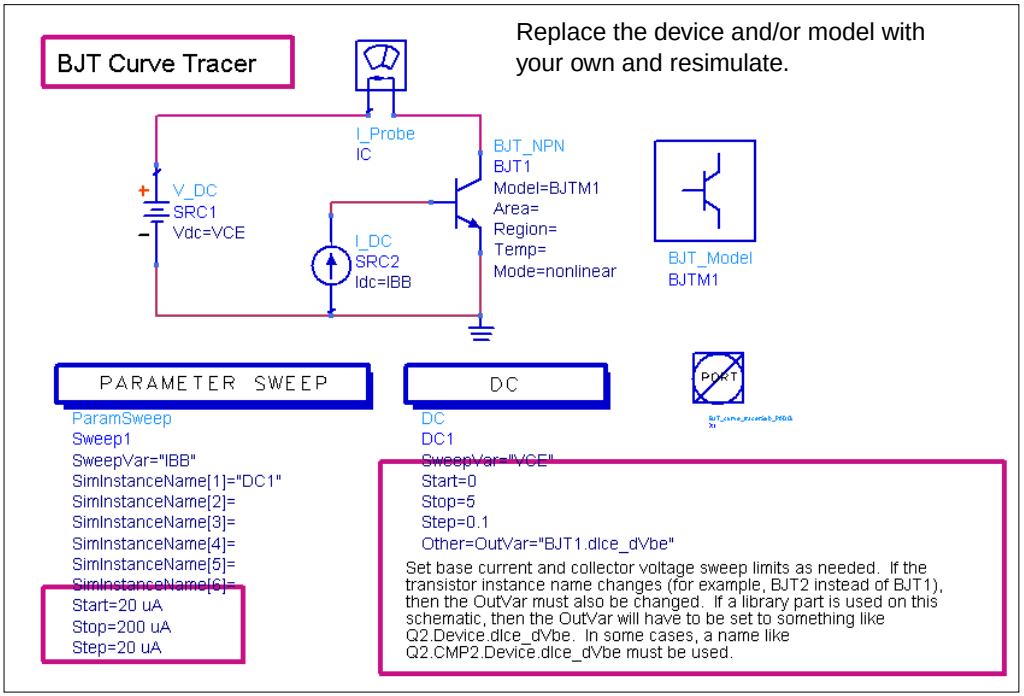
The first six menu selections from *DC and Bias Point Simulations* through *Lumped Multi-Element Z-Y Matching Networks* are for selecting simulation setups, which are further categorized, as explained in subsequent sections of this document. There is a corresponding set of menu selections under *Display Simulation Results*. These are for selecting data displays to view your simulation output.

Each of the six menu selections from *DC and Bias Point Simulations* to *Lumped Multi-Element Z-Y Matching Networks* have additional selections. The menu for schematics for DC and bias point simulations appears as follows.



Selecting one of these menu items, such as *BJT I-V Curves*, copies a schematic into your current project that is set up for generating a bipolar junction transistor's current-versus-voltage curves.

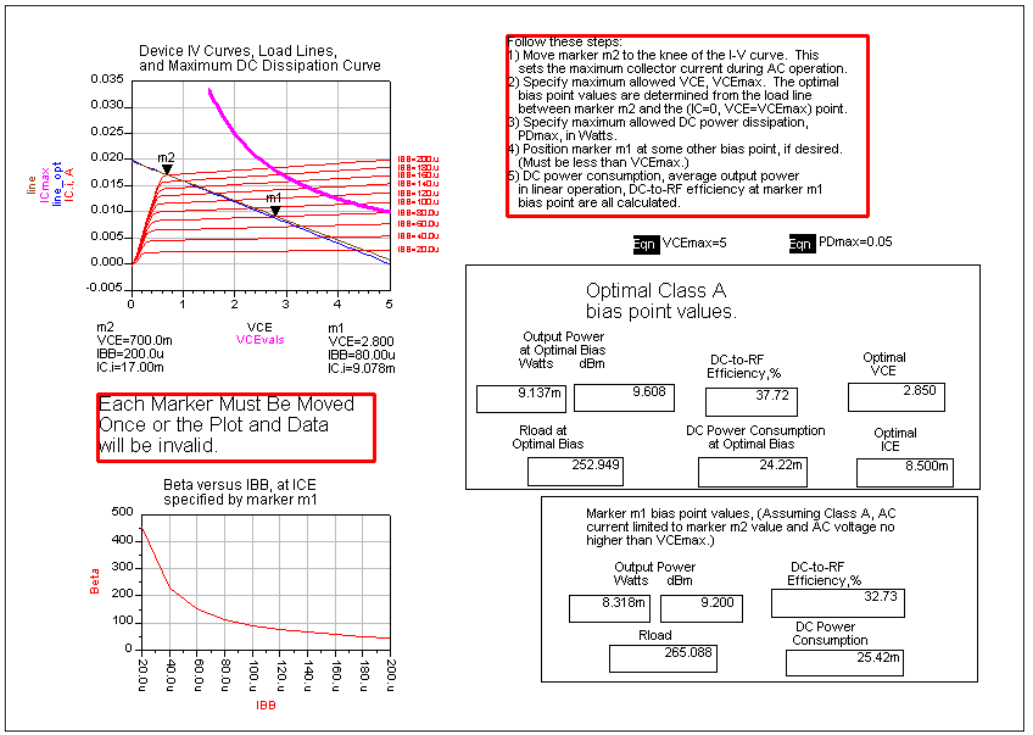
The BJT I-V curve schematic appears as follows.



Each schematic has a sample device that has already been simulated. The simulated results are displayed in a data display file that opens automatically after the schematic is copied into your project. Modify the BJT by editing its model, or delete the device and replace it with a different one. The red boxes enclose parameters you should set, such as the range of base currents and the range of collector voltages. After making modifications, run a simulation and the data display will update.

Note All schematics have a sample device and/or model, or a sample amplifier. The first data display that opens after you make a menu selection has pre-simulated data from the device or amplifier. You must replace the device or amplifier on the schematic and run a new simulation. The data display should be updated with the new data.

Following are the results of the simulation.

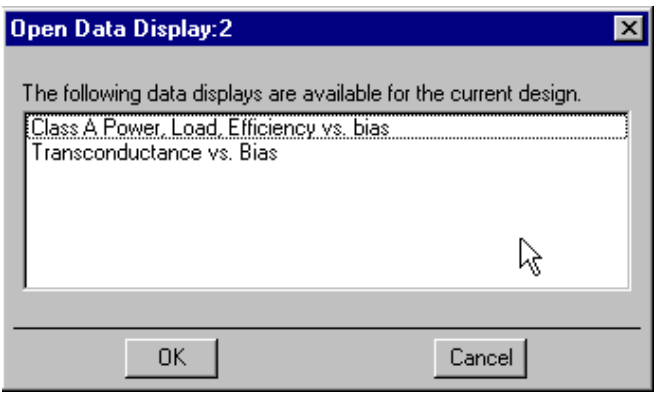


Most of the information on this data display and on others in the DesignGuide is in a format that engineers can easily understand.

Tips

- We have minimized the visibility of equation syntaxes that you should not need to modify.
- Information about items on a data display that you would want to modify is enclosed in red boxes.
- Equations that you should not need to modify have been hidden.
- Some of the schematics have more than one corresponding data display. Those that do have a note indicating so. The other data displays are accessed via the corresponding menu selection under *Display Simulation Results*.

- When you select one of the menu picks under *Display Simulation Results*, if there is only one data display that corresponds to the particular schematic, that data display will be opened. If there is more than one data display that corresponds to that schematic, a dialog box appears, allowing you to select from several different data displays, as shown here.



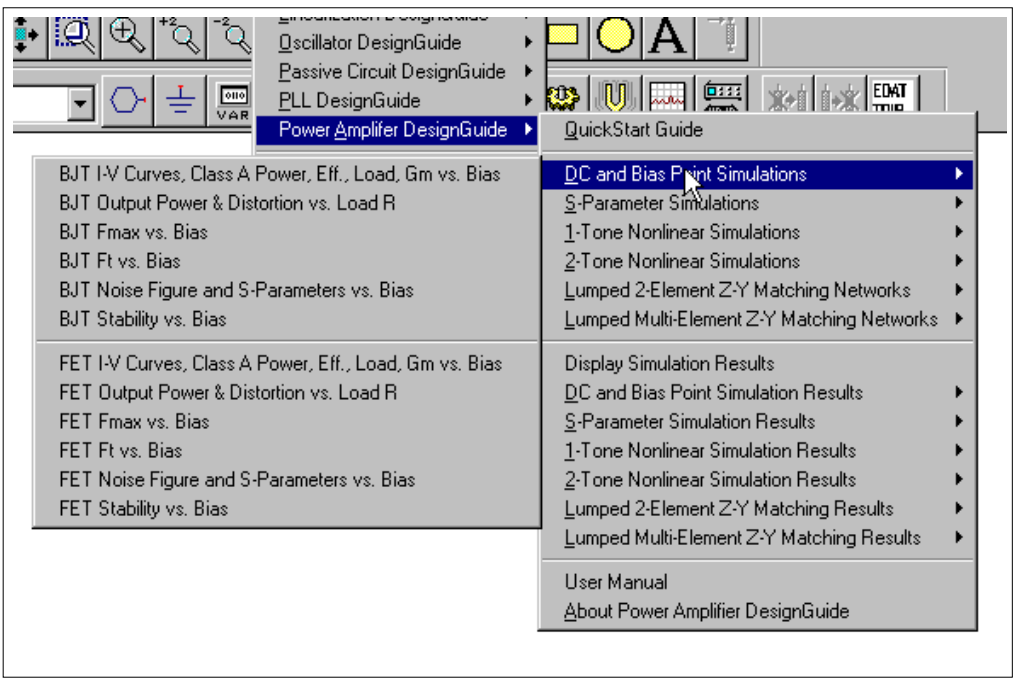
If you select the menu command from a schematic that you have renamed, be sure to set the default dataset name on the data display window (which will usually correspond to the new name of your schematic) after you have run a simulation from the renamed schematic.

Selecting the Appropriate Simulation Type

The Power Amplifier DesignGuide is divided into six categories for different simulation types. Your design objective and the type of models you have available will determine which menu selections you select first.

DC and Bias Point Simulations

If you have a Nonlinear FET or BJT model available, you can start with *DC and Bias Point Simulations*, as shown here.



These selections can be used to determine data such as the following:

- I-V curves of a device
- Approximate class A output power and optimal bias point
- Gm, fmax, and ft versus bias
- Noise figure and S-parameters versus bias

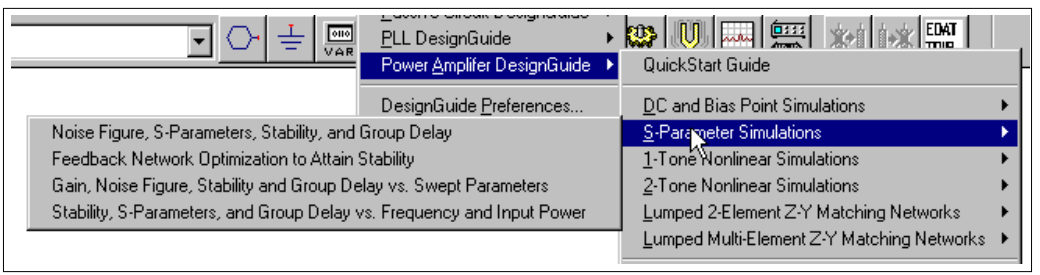
- Optimal source and load impedances for maximum gain or minimum noise figure, versus bias

---

Note While this DesignGuide is targeted to power amplifier designers, some of the schematics and data displays are quite useful for small-signal or low-noise amplifier designers as well.

S-Parameter Simulations

If you have only S-parameters (possibly with noise data) available, or want to simulate an amplifier's small-signal performance, start with *S-Parameter Simulations*, as shown here.

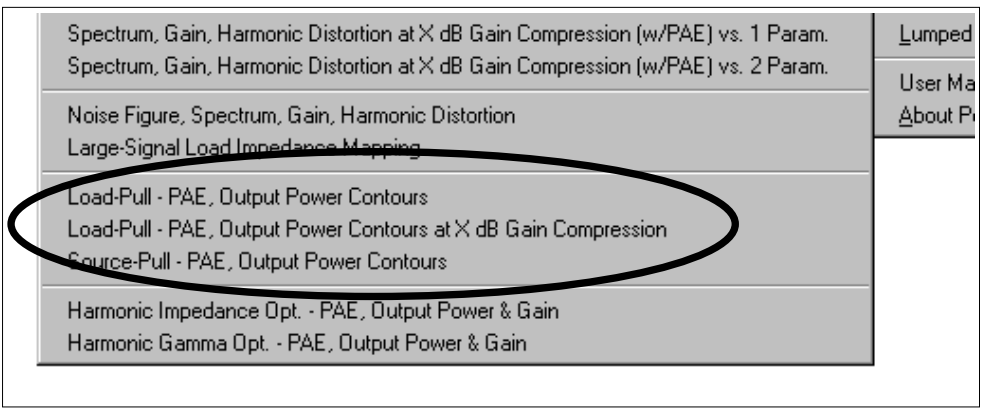


These can be used to determine data such as the following:

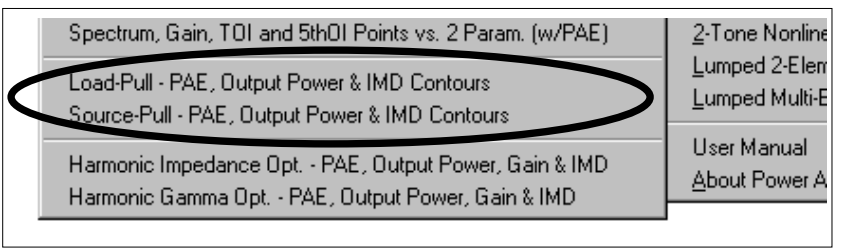
- Noise figure and NFmin, maximum available gain, and S-parameters
- Optimal source and load impedances to attain the minimum noise figure or maximum gain
- Feedback network element values to attain stability
- Noise and available gain circles
- Stability circles and stability factors
- Stability and S-parameters versus power (actually these require a nonlinear model.)
- Group Delay

Nonlinear Simulations

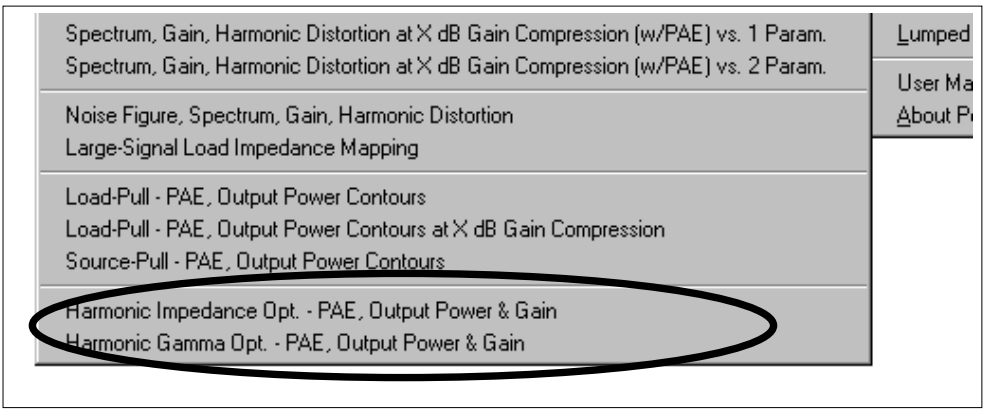
If you have a nonlinear device model available and want the optimal source and load impedances at the fundamental frequency (to maximize output power and/or power-added efficiency), use Load-Pull or Source-Pull schematics in *1-Tone Nonlinear Simulations*, as shown here.



If you have a nonlinear device model available and want the optimal source and load impedances at the fundamental frequency (to maximize output power and/or power-added efficiency, or minimize third- or fifth-order intermodulation distortion), use Load-Pull or Source-Pull schematics in *2-Tone Nonlinear Simulations*, as shown here.

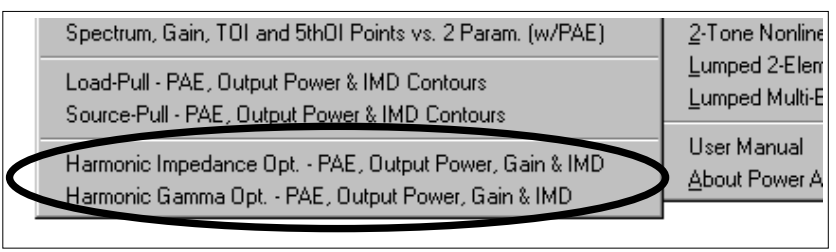


If you have a nonlinear device model available and want the optimal source and load impedances at the fundamental *and* harmonic frequencies (to maximize output power and/or power-added efficiency), use the Harmonic Impedance Opt or Harmonic Gamma Opt schematics in *1-Tone Nonlinear Simulations*, as shown here.



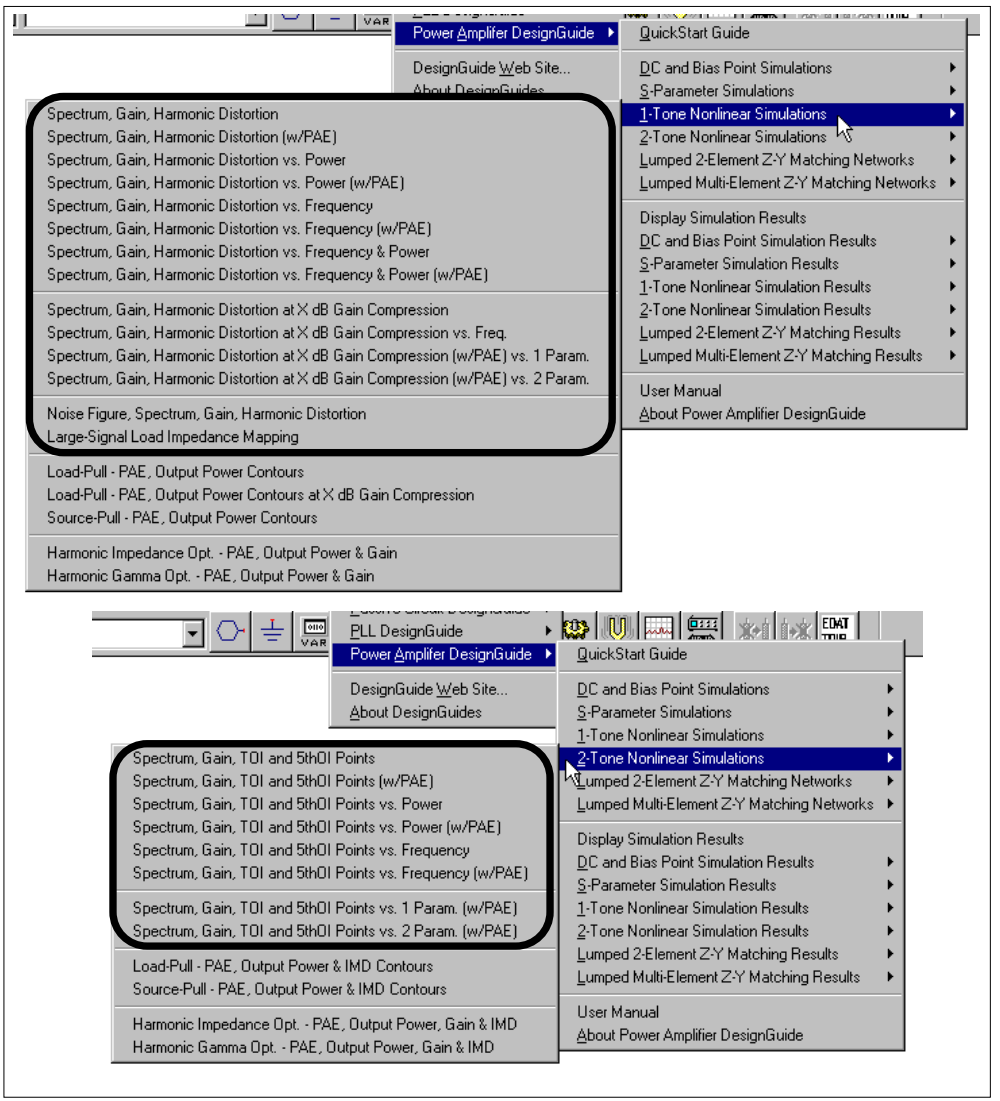
The difference between the two optimizations is that in one case, you specify the ranges of allowed real and imaginary impedances, and in the other, you specify the allowed reflection coefficients as circular regions on the Smith Chart.

If you have a nonlinear device model available and want the optimal source and load impedances at the fundamental *and* harmonic frequencies (to maximize output power and/or power-added efficiency, and minimize intermodulation distortion), use the Harmonic Impedance Optimization or Harmonic Gamma Optimization schematics in *2-Tone Nonlinear Simulation*, as shown here.

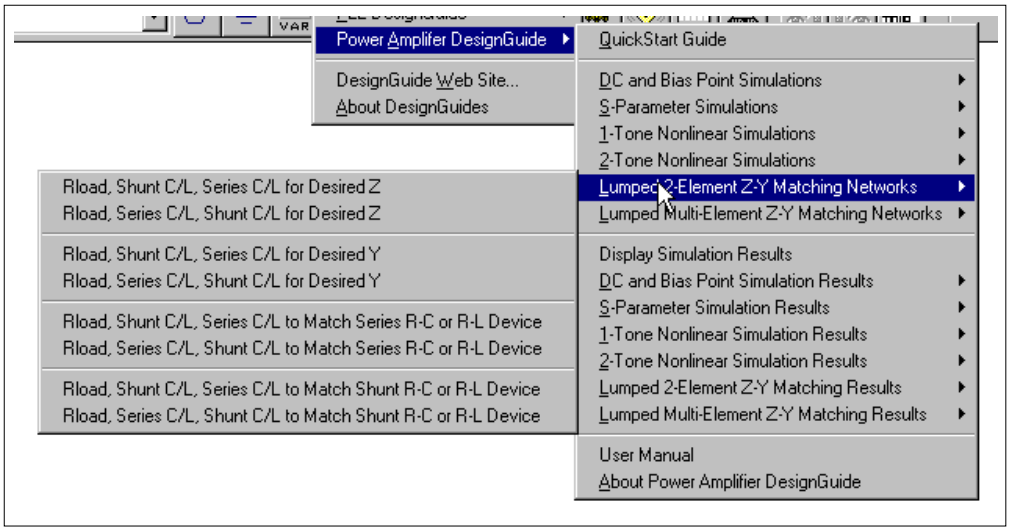


Again, the difference between the two optimizations is that in one case, you specify the ranges of allowed real and imaginary impedances, and in the other case you specify the allowed reflection coefficients as circular regions on the Smith Chart.

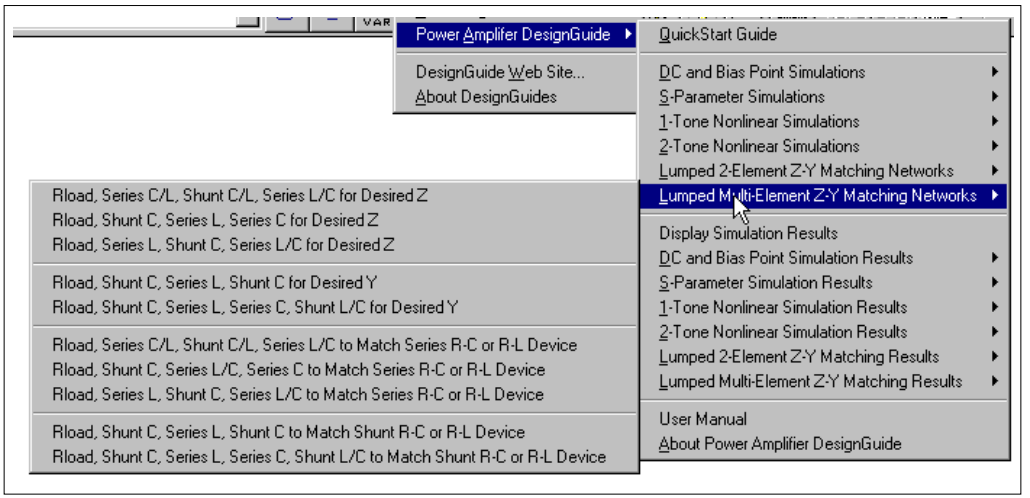
If you already have an amplifier design, and you want to characterize the nonlinear performance over frequency, power, and other swept parameters, select the appropriate schematic from *1-Tone Nonlinear Simulations*, as shown here in the first example, or *2-Tone Nonlinear Simulation*, as shown in the second example.



If you want to generate an arbitrary impedance or admittance, or match to a device's equivalent input or output circuit, using ideal, lumped elements only, use one of the schematics under *Lumped 2-Element Z and Y Matching Network*, as shown here.



Lumped, multi-element matching networks can also be used, as shown here.



Note In the ADS 1.3 product suite, E-Syn or the new RF Compiler provide better solutions for network matching applications. The Passive Circuit DesignGuide includes impedance matching capabilities.

Chapter 2: Introduction

The *Power Amplifier DesignGuide* has many simulation setups and data displays that are useful for power amplifier design. The simulation setups are categorized by the type of simulation desired and the type of model available. Most of the simulation setups are for analysis, but there are also some for synthesizing impedance matching networks.

Note This manual assumes that you are familiar with all of the basic ADS program operations. For additional information, refer to the ADS *User's Guide*.

This manual is organized as follows:

- Reference tables in this chapter, listing all simulation setups, with links to the appropriate manual pages for detailed information
- Chapters for each type of simulation setup, as identified on the DesignGuide menu (which is accessed from ADS Schematic window). Detailed information on each simulation setup is included.

Hint The first six selections from the Power Amplifer DesignGuide menu (*DC and Bias Point Simulations* through *Lumped Multi-Element Z-Y Matching Network*s) are for selecting simulation setups, as shown in the QuickStart manual. There is a corresponding set of menu selections under *Display Simulation Result*s. These are for selecting data displays to view your simulation output.

List of Available Data Displays

The tables that follow list all data displays that are included with each simulation.

Table 2-1 shows all data displays included for DC and Bias Point Simulations.

Table 2-1. DC and Bias Point Simulations

Simulation	Data Displays
BJT I-V Curves, Class A Power, Eff., Load, Gm vs. Bias	Class A Power, Load, Efficiency vs. bias (BJT_ClassA_calcs.dds)
	Transconductance vs. bias (BJT_IV_gm.dds)
BJT Output Power & Distortion vs. Load R	BJT_dynamic_LL.dds
BJT Fmax vs. Bias	BJT_fmax_vs_bias.dds
BJT Ft vs. Bias	BJT_ft_vs_bias.dds
BJT Noise Figure and S-Parameters vs. Bias	BJT Noise Figure and S-Parameters vs. Bias (BJT_IV_NF_SP.dds)
	BJT Matching for Noise Figure or Gain (BJT_NF_Matching.dds)
	Available Gain, Noise, and Stability Circles (Circles_Ga_NF_Stability_BJT.dds)
	Available Gain, Power Gain, and Stability Circles (Circles_Ga_Gp_Stability_BJT.dds)
BJT Stability vs. Bias	BJT_Stab_vs_bias.dds
FET I-V Curves, Class A Power, Eff., Load, Gm vs. Bias	Class A Power, Load, Efficiency vs. bias (FET_ClassA_calcs.dds)
	Transconductance vs. bias (FET_IV_gm.dds)
FET Output Power & Distortion vs. Load R	FET_dynamic_LL.dds
FET Fmax vs. Bias	FET_fmax_vs_bias.dds
FET Ft vs. Bias	FET_ft_vs_bias.dds
FET Noise Figure and S-Parameters vs. Bias	FET Noise Figure and S-Parameters vs. Bias (FET_IV_NF_SP.dds)
	FET Matching for Noise Figure or Gain (FET_NF_Matching.dds)
	Available Gain, Noise, and Stability Circles (Circles_Ga_NF_Stability_FET.dds)
	Available Gain, Power Gain, and Stability Circles (Circles_Ga_Gp_Stability_FET.dds)

Table 2-2 shows all data displays used for S-Parameter Simulations.

Table 2-2. S-Parameter Simulations

Simulation	Data Displays
Noise Figure, S-Parameters, Stability, and Group Delay	NFmin, Matching for Gain and Noise Figure (NF_GA_Matching.dds)
	Available Gain, Noise, and Stability Circles (Circles_Ga_NF_Stability.dds)
	Available Gain, Power Gain, and Stability Circles (Circles_Ga_Gp_Stability.dds)
	Source and Load Stability Circles and Factors (NF_Stab_Circles.dds)
	S-Parameters on Smith Chart and Polar Plots (S_Params_Quad_Smith_Plr.dds)
	S-Parameters on Smith Chart and Rect. Plots (S_Params_Quad_dB_Smith.dds)
	Group Delay (GroupDelay.dds)
	Noise Figure and Optimal Source Gamma for NFmin (NoiseFigure.dds)
Feedback Network Optimization to Attain Stability	Gain_and_Stab_opt.dds
Gain, Noise Figure, Stability and Group Delay vs. Swept Parameters	Gain, Noise Figure and Matching vs. Swept Parameters (NF_GA_Matching_sweep.dds)
	Stability Factor and Noise Figure vs. Swept Parameters (NF_Stability_sweep.dds)
	S-Parameters and Gain vs. Swept Parameters (SP_sweep.dds)
	Group Delay vs. Swept Parameters (GroupDelay_sweep.dds)
Stability, S-Parameters, and Group Delay vs. Frequency and Input Power	Stability and S-Parameters vs. Frequency and Input Power (Stab_vs_freq_pwr.dds)
	Group Delay versus Frequency and Input Power (GroupDelay_vsFreqPwr.dds)

Table 2-3 shows all data displays used for 1-Tone Nonlinear Simulations.

Table 2-3. 1-Tone Nonlinear Simulations

Simulation	Data Displays
Spectrum, Gain, Harmonic Distortion	HB1Tone.dds
Spectrum, Gain, Harmonic Distortion (w/PAE)	HB1TonePAE.dds
Spectrum, Gain, Harmonic Distortion vs. Power	Spectrum, Gain, Harm. Distortion vs. Power (HB1TonePswp.dds)
Spectrum, Gain, Harmonic Distortion vs. Power (w/PAE)	(HB1TonePAE_Pswp.dds
Spectrum, Gain, Harmonic Distortion vs. Frequency	HB1TonePswp.dds
Spectrum, Gain, Harmonic Distortion vs. Frequency (w/PAE)	HB1TonePAE_Fswp.dds
Spectrum, Gain, Harmonic Distortion vs. Frequency & Power	Spectrum, Gain, Harm. Distortion vs. Frequency and Power (HB1ToneFPswp.dds)
	AM-to-AM, AM-to-PM Distortion vs. Frequency and Power (HB1ToneFPswpAMtoPM.dds)
Spectrum, Gain, Harmonic Distortion vs. Frequency & Power (w/PAE)	Spectrum, Gain, Harm. Distortion vs. Frequency and Power (HB1TonePAE_FPswp.dds)
	AM-to-AM, AM-to-PM Distortion vs. Frequency and Power (HB1TonePAE_FPswpAMtoPM.dds)
Spectrum, Gain, Harmonic Distortion at X dB Gain Compression	HB1ToneGComp.dds
Spectrum, Gain, Harmonic Distortion at X dB Gain Compression vs. Freq.	HB1ToneGCompFswp.dds
Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 1 Param.	HB1ToneGComp1swp.dds
Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 2 Param.	HB1ToneGComp2swp.dds
Noise Figure, Spectrum, Gain, Harmonic Distortion	HB1ToneNoise.dds
Large-Signal Load Impedance Mapping	LoadMapper.dds
Load-Pull - PAE, Output Power Contours	HB1Tone_LoadPull.dds
Load-Pull - PAE, Output Power Contours at X dB Gain Compression	HB1Tone_LoadPull_GComp.dds
Source-Pull - PAE, Output Power Contours	HB1Tone_SourcePull.dds

Table 2-3. 1-Tone Nonlinear Simulations (continued)

Simulation	Data Displays
Harmonic Impedance Opt. - PAE, Output Power & Gain	PAE, Output Power, Gain, Dissipation (HarmZopt1tone.dds)
	Source and Load Harmonic Impedances (HarmZopt1toneSC.dds)
	Input and Output Waveforms and Dynamic Load Line (HarmZopt1toneTime.dds)
Harmonic Gamma Opt. - PAE, Output Power & Gain	PAE, Output Power, Gain, Dissipation (HarmGammaOpt1tone.dds)
	Source and Load Harmonic Impedances (HarmGammaOpt1toneSC.dds)
	Input and Output Waveforms and Dynamic Load Line (HarmGammaOpt1toneTime.dds)

Table 2-4 shows all data displays used for 2-Tone Nonlinear Simulations.

Table 2-4. 2-Tone Nonlinear Simulations

Simulation	Data Displays
Spectrum, Gain, TOI and 5thOI Points	HB2Tone.dds
Spectrum, Gain, TOI and 5thOI Points (w/PAE)	HB2TonePAE.dds
Spectrum, Gain, TOI and 5thOI Points vs. Power	HB2TonePswp.dds
Spectrum, Gain, TOI and 5thOI Points vs. Power (w/PAE)	HB2TonePAE_Pswp.dds
Spectrum, Gain, TOI and 5thOI Points vs. Frequency	HB2ToneFswp.dds
Spectrum, Gain, TOI and 5thOI Points vs. Frequency (w/PAE)	HB2TonePAE_Fswp.dds
Spectrum, Gain, TOI and 5thOI Points vs. 1 Param. (w/PAE)	HB2TonePAE_1swp.dds
Spectrum, Gain, TOI and 5thOI Points vs. 2 Param. (w/PAE)	HB2TonePAE_2swp.dds
Load-Pull - PAE, Output Power & IMD Contours	Load-Pull - PAE, Output Power & IMD Contours (HB2Tone_LoadPull.dds)
	Load-Pull - Contours and Spectrum (HB2Tone_LoadPullmore.dds)

Table 2-4. 2-Tone Nonlinear Simulations (continued)

Simulation	Data Displays
Source-Pull - PAE, Output Power & IMD Contours	Source-Pull - PAE, Output Power & IMD Contours (HB2Tone_SourcePull.dds)
	Source-Pull - Contours and Spectrum (HB2Tone_SourcePullmore.dds)
Harmonic Impedance Opt. - PAE, Output Power, Gain & IMD	PAE, Output Power, Gain, IMD, Dissipation (HarmZopt2tone.dds)
	Source and Load Harmonic Impedances (HarmZopt2toneSC.dds)
	Input and Output Waveforms and Dynamic Load Line (HarmZopt2toneTime.dds)
Harmonic Gamma Opt. - PAE, Output Power, Gain, & IMD	PAE, Output Power, Gain, IMD, Dissipation (HarmGammaOpt2tone.dds)
	Source and Load Harmonic Impedances (HarmGammaOpt2toneSC.dds)
	Input and Output Waveforms and Dynamic Load Line (HarmGammaOpt2toneTime.dds)

Table 2-5 shows all data displays used for Lumped 2-Element Z-Y Matching Networks.

Table 2-5. Lumped 2-Element Z-Y Matching Networks

Simulation	Data Displays
Rload, Shunt C/L, Series C/L for Desired Z	Zdesired1.dds
Rload, Series C/L, Shunt C/L for Desired Z	Zdesired2.dds
Rload, Shunt C/L, Series C/L for Desired Y	Ydesired1.dds
Rload, Series C/L, Shunt C/L for Desired Y	Ydesired2.dds
Rload, Shunt C/L, Series C/L to Match Series R-C or R-L Device	Zmatch1.dds
Rload, Series C/L, Shunt C/L to Match Series R-C or R-L Device	Zmatch2.dds
Rload, Shunt C/L, Series C/L to Match Shunt R-C or R-L Device	Ymatch1.dds
Rload, Series C/L, Shunt C/L to Match Shunt R-C or R-L Device	Ymatch2.dds

Table 2-6 shows all data displays used for Lumped Multi-Element Z-Y Matching Networks.

Table 2-6. Lumped Multi-Element Z-Y Matching Networks

Simulation	Data Display
Rload, Series C/L, Shunt C/L, Series L/C for Desired Z	Zdesired1M.dds
Rload, Shunt C, Series L, Series C for Desired Z	Zdesired2M.dds
Rload, Series L, Shunt C, Series L/C for Desired Z	Zdesired3M.dds
Rload, Shunt C, Series L, Shunt C for Desired Y	Ydesired1M.dds
Rload, Shunt C, Series L, Series C, Shunt L/C for Desired Y	Ydesired2M.dds
Rload, Series C/L, Shunt C/L, Series L/C to Match Series R-C or R-L Device	Zmatch1M.dds
Rload, Shunt C, Series L/C, Series C to Match Series R-C or R-L Device	Zmatch2M.dds
Rload, Series L, Shunt C, Series L/C to Match Series R-C or R-L Device	Zmatch3M.dds
Rload, Shunt C, Series L, Shunt C Shunt R-C or R-L Device	Ymatch1M.dds
Rload, Shunt C, Series L, Series C, Shunt L/C to Match Shunt R-C or R-L Device	Ymatch2M.dds

Chapter 3: DC and Bias Point Simulations

The templates in the DC and Bias Point Simulations menu are concerned with choosing a bias point, and its effects on output power, gain, noise figure, transconductance, etc.

DC and Bias Point Simulation > BJT I-V Curves, Class A Power, Eff., Load, Gm vs. Bias

Description

This simulation setup generates the I-V curves of a BJT. Various data dependent on the I-V curves, such as transconductance, class A output power, and efficiency are also shown. Both the base current and the collector-to-emitter voltage are swept.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Setting

Sweep ranges for base current and collector voltage

Data Display Outputs

Class A Power, Load, Efficiency vs. bias (BJT_ClassA_calcs.dds):

- Device I-V curves
- Load line set by placing a marker on the I-V curves at the knee, and by a user-specifiable maximum VCE.
- Maximum allowed DC power dissipation curve, with maximum dissipation set by user.
- Given the load line specified by the knee of the I-V curves and the maximum VCE:
  - Optimum collector voltage and collector current, for maximum power delivered to the load while in Class A operation
  - Corresponding load resistance
  - Corresponding maximum output power
  - Corresponding DC power consumption
  - Corresponding DC-to-RF efficiency
- Given a different bias point, specified by a different marker:
  - Load line between that marker and the marker at the knee of the I-V curve
  - Resistance of this load line
  - DC power consumption at this bias point

- Output power, assuming the device remains in Class A operation (AC voltage does not exceed user-specified VCE, and does not enter the knee region)
- DC-to-RF efficiency at this bias point

- Device beta versus base current at the VCE specified by one of the markers

---

Note The estimate of DC-to-RF efficiency and output power are only approximate, since no high-frequency effects are modeled in this simulation.

Transconductance vs. bias (BJT_IV_gm.dds) data display also uses the data from the BJT_curve_tracer schematic, and outputs:

- Device I-V curves
- DC transconductance (Gm) versus VCE
- DC transconductance (Gm) versus IBB and VCE
- DC transconductance (Gm) versus collector current
- Collector current versus base current at one VCE
- Table of transconductance values

Schematic Name

BJT_curve_tracer

Data display name(s)

BJT_ClassA_calcs.dds

BJT_IV_gm.dds

DC and Bias Point Simulation > BJT Output Power & Distortion vs. Load R

Description

This simulation setup generates the I-V curves of a BJT and simulates the power delivered to a load resistor as a function of the resistance value, at one bias point.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

Sweep ranges for base current, collector voltage and load resistance; bias point and frequency for output power versus load resistance simulation

Data Display Outputs

- Device I-V curves
- Load lines for each of the load resistances
- Power delivered to the load as a function of load resistance
- Output power and harmonic distortion at each load resistance

Schematic Name

BJT_dynamic_LL

Data Display Name(s)

BJT_dynamic_LL.dds

Note

The load power simulations will show less than optimal results as the simulation frequency is increased, because only a resistive load is presented to the device. Also, no impedance matching is included at the input.

DC and Bias Point Simulation > BJT Fmax vs. Bias

Description

This simulates the maximum frequency of oscillation (the frequency at which the maximum available gain drops to 0 dB), versus bias current, for a particular value of VCE. It should help you determine how high in frequency a device can be used.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

VCE, base current sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- The maximum available gain versus base current and frequency
- dB(S21) versus base current and frequency
- The maximum frequency of oscillation, which is dependent on a marker that you move to select the value of collector current

Schematic Name

BJT_fmax_vs_bias

Data Display Name(s)

BJT_fmax_vs_bias.dds

DC and Bias Point Simulation > BJT Ft vs. Bias

Description

This simulates a device's ft, the frequency at which the short-circuit current gain drops to unity, versus bias current, for a particular value of VCE. It should help you determine how high in frequency a device can be used.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

VCE, base current sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- Short circuit current gain versus base current and frequency
- Frequency at which the short-circuit current gain drops to 0 dB, at the collector bias current specified by a movable marker

Schematic Name

BJT_ft_vs_bias

Data Display Name(s)

BJT_ft_vs_bias.dds

DC and Bias Point Simulation > BJT Noise Figure and S-Parameters vs. Bias

Description

This simulates the S-parameters and noise parameters of a device, versus bias voltage and current, at a single frequency. You specify the collector voltage sweep range and the base current sweep range, and the single frequency for S-parameter and noise analysis. The optimal source and load impedances for minimum noise figure and for maximum gain are computed, as well as the available gain circles, power gain circles, noise circles, and source and load stability circles.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

Sweep ranges for base current and collector voltage and frequency for S-parameter analysis.

Data Display Outputs

BJT Noise Figure and S-Parameters vs. Bias (BJT_IV_NF_SP.dds):

- Minimum noise figure versus VCE and base current
- dB(S21), dB(S12), dB(S11), and dB(S22) versus collector voltage and base current
- DC I-V curves
- Maximum available gain versus base current and collector voltage
- dB(S21) versus collector current at a collector voltage selected by moving a marker on the I-V curve
- VCE, IC, DC power consumption, S-parameters, maximum available gain, and minimum noise figure at a bias point selected by moving a marker on the I-V curves.

BJT Matching for Noise Figure or Gain (BJT_NF_Matching.dds):

- Minimum noise figure versus collector voltage and base current
- Associated power gain (with input matched for minimum noise figure and output conjugately matched) versus collector voltage and base current

- Minimum noise figure versus collector current at a collector voltage selected by moving a marker on the I-V curves.
- DC I-V curves
- Smith chart with traces of the optimal source reflection coefficients for minimum noise figure, and the following reflection coefficients (gammas) at the selected bias point:
  - Gamma source for minimum noise figure
  - Gamma load for maximum power gain when input is terminated for minimum noise figure
  - Gamma source for simultaneous conjugate match (without regard to noise)
  - Gamma load for simultaneous conjugate match (without regard to noise)
- Listing columns of data corresponding to the bias point selected by moving a marker on the I-V curves:
  - VCE
  - IC
  - Approximate DC power consumption
  - S-parameters, dB
  - Maximum available power gain, dB
  - Minimum noise figure, dB
  - Sopt for minimum noise figure in polar coordinates and in magnitude and phase
  - Zopt for minimum noise figure
  - Associated power gain in dB, if the input is matched for minimum noise figure and then the output is matched for maximum power gain
  - Corresponding load impedance for associated power gain
  - Source and load impedances for simultaneous conjugate matching (without regard to noise)
  - Input and output impedances when source and load are terminated in 50 ohms
  - Stability factor, K

- Frequency of the S-parameter simulations

Available Gain, Noise, and Stability Circles (Circles_Ga_NF_Stability_BJT.dds):

All at one bias point selected by moving a marker on the device's I-V curves:

- Stability factor, K, and source stability circles. Note that the Smith Chart size is fixed, so if the stability circles are far outside the Smith Chart, they will not be displayed. If you change the Smith Chart scaling to Auto Scale, the circles will be visible.
- Available gain and noise circles
- Minimum noise figure, source impedance (Zopt) required to achieve this noise figure, and the optimal load impedance for power transfer when the source impedance is Zopt
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1)
- Noise figure with the simultaneous conjugate match condition
- Noise figure, transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith Chart. This is useful if you must make some compromise between noise and gain, or if you need to avoid an unstable region.

Available Gain, Power Gain, and Stability Circles
(Circles_Ga_Gp_Stability_BJT.dds):

All at one bias point selected by moving a marker on the device's I-V curves:

- Stability factor, K, and source and load stability circles. Note that the Smith Chart size is fixed, so if the stability circles are far outside the Smith Chart, they will not be displayed. If you change the Smith Chart scaling to Auto Scale, the circles will be visible.
- Available gain and power gain circles, on different Smith Charts
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1)
- Transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith Chart. This is useful if you need to avoid an unstable region.

- Transducer power gain, and optimal source impedance if the load impedance is chosen arbitrarily by moving a marker (GammaL) on a Smith Chart. This is useful if you need to avoid an unstable region.

Schematic Name

BJT_IV_NF_SP

Data Display Names

BJT_IV_NF_SP.dds

BJT_NF_Matching.dds

Circles_Ga_NF_Stability_BJT.dds

Circles_Ga_Gp_Stability_BJT.dds

DC and Bias Point Simulation > BJT Stability vs. Bias

Description

This simulates the S-parameters of a transistor, with the base current swept and the emitter bias voltage constant, to determine the stability factors as a function of base current. It should help you determine the dependence of the stability factor on the bias point.

Needed to Use Schematic

Nonlinear BJT model

Main Schematic Settings

VCE, base current sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- Stability measure, B1, versus base current and frequency
- Stability factor, K, versus base current and frequency
- Geometrically-derived load stability factor, mu, versus base current and frequency
- Geometrically-derived source stability factor, mu_prime, versus base current and frequency

Schematic Name

BJT_Stab_vs_bias

Data Display Name(s)

BJT_Stab_vs_bias.dds

DC and Bias Point Simulation > FET I-V Curves, Class A Power, Eff., Load, Gm vs. Bias

Description

This simulation setup generates the I-V curves of a FET. Various data dependent on the I-V curves, such as transconductance, class A output power, and efficiency are also shown. Both the gate and drain voltages are swept.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

Sweep ranges for gate and drain voltages

Data Display Outputs

Class A Power, Load, Efficiency vs. bias (FET_ClassA_calcs.dds):

- Device I-V curves
- Load line set by placing a marker on the I-V curves at the knee, and by a user-specifiable maximum VDS
- Maximum allowed DC power dissipation curve, with maximum dissipation set by user.
- Given the load line specified by the knee of the I-V curves and the maximum VDS:
  - Optimum drain voltage and drain current, for maximum power delivered to the load while in Class A operation
  - Corresponding load resistance
  - Corresponding maximum output power
  - Corresponding DC power consumption
  - Corresponding DC-to-RF efficiency
- Given a different bias point, specified by a different marker:
  - Load line between that marker and the marker at the knee of the I-V curve
  - Resistance of this load line
  - DC power consumption at this bias point

- Output power, assuming the device remains in Class A operation (AC voltage does not exceed user-specified VDS, and does not enter the knee region)
- DC-to-RF efficiency at this bias point

Note The estimates of DC-to-RF efficiency and output power are only approximate, since no high-frequency effects are modeled in this simulation.

Transconductance vs. bias (FET_IV_gm.dds) data display also uses the data from the FET_curve_tracer schematic, and outputs:

- Device I-V curves
- DC transconductance (Gm) versus VDS
- DC transconductance (Gm) versus VGS and VDS
- DC transconductance (Gm) versus drain current
- Drain current versus gate voltage at one VDS
- Table of transconductance values

Schematic Name

FET_curve_tracer

Data Display Name(s)

FET_ClassA_calcs.dds

FET_IV_gm.dds

DC and Bias Point Simulation > FET Output Power & Distortion vs. Load R

Description

This simulation setup generates the I-V curves of a FET and simulates the power delivered to a load resistor as a function of the resistance value, at one bias point.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

Sweep ranges for gate voltage, drain voltage and load resistance; bias point and frequency for output power versus load resistance simulation

Data Display Outputs

- Device I-V curves
- Load lines for each of the load resistances
- Power delivered to the load as a function of load resistance
- Output power and harmonic distortion at each load resistance

Schematic Name

FET_dynamic_LL

Data Display Name(s)

FET_dynamic_LL.dds

Note

The load power simulations are going to show less than optimal results as the simulation frequency is increased, because only a resistive load is presented to the device. Also, no impedance matching is included at the input.

DC and Bias Point Simulation > FET Fmax vs. Bias

Description

This simulates the maximum frequency of oscillation (the frequency at which the maximum available gain drops to 0 dB), versus bias voltage, for a particular value of VDS. It should help you determine how high in frequency a device can be used.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

VDS, gate voltage sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- The maximum available gain versus gate voltage and frequency
- dB(S21) versus gate voltage and frequency
- The maximum frequency of oscillation, which is dependent on a marker that you move to select the value of drain current

Schematic Name

FET_fmax_vs_bias

Data Display Name(s)

FET_fmax_vs_bias.dds

DC and Bias Point Simulation > FET Ft vs. Bias

Description

This simulates a device's ft, the frequency at which the short-circuit current gain drops to unity, versus gate voltage, for a particular value of VDS. It should help you determine how high in frequency a device can be used.

Needed to Use Schematic

Nonlinear FET model.

Main Schematic Settings

VDS, gate voltage sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- Short circuit current gain versus gate voltage and frequency
- Frequency at which the short-circuit current gain drops to 0 dB, at the drain bias current specified by a movable marker

Schematic Name

FET_ft_vs_bias

Data Display Name(s)

FET_ft_vs_bias.dds

DC and Bias Point Simulation > FET Noise Figure and S-Parameters vs. Bias

Description

This simulates the S-parameters and noise parameters of a device, versus bias voltages, at a single frequency. You specify the gate and drain voltage sweep ranges, and the single frequency for S-parameter and noise analysis. The optimal source and load impedances for minimum noise figure and for maximum gain are computed, as well as the available gain circles, power gain circles, noise circles, and source and load stability circles.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

Sweep ranges for gate and drain voltages and frequency for S-parameter analysis

Data Display Outputs

FET Noise Figure and S-Parameters vs. Bias (FET_IV_NF_SP.dds):

- Minimum noise figure versus VGS and VDS
- dB(S21), dB(S12), dB(S11), and dB(S22) versus VGS and VDS
- DC I-V curves
- Maximum available gain versus VGS and VDS
- dB(S21) versus drain current at a drain voltage selected by moving a marker on the I-V curves
- VDS, IDS, DC power consumption, S-parameters, maximum available gain, and minimum noise figure at a bias point selected by moving a marker on the I-V curves.

FET Matching for Noise Figure or Gain (FET_NF_Matching.dds):

- Minimum noise figure versus VGS and VDS
- Associated power gain (with input matched for minimum noise figure and output conjugately matched) versus VGS and VDS
- Minimum noise figure versus drain current at a drain voltage selected by moving a marker on the I-V curves.

- DC I-V curves
- Smith chart with traces of the optimal source reflection coefficients for minimum noise figure, and the following reflection coefficients (gammas) at the selected bias point:
  - Gamma source for minimum noise figure
  - Gamma load for maximum power gain when input is terminated for minimum noise figure
  - Gamma source for simultaneous conjugate match (without regard to noise)
  - Gamma load for simultaneous conjugate match (without regard to noise)
- Listing columns of data corresponding to the bias point selected by moving a marker on the I-V curve:
  - VDS
  - IDS
  - Approximate DC power consumption
  - S-parameters, dB
  - Maximum available power gain, dB
  - Minimum noise figure, dB
  - Sopt for minimum noise figure in polar coordinates and in magnitude and phase
  - Zopt for minimum noise figure
  - Associated power gain in dB, if the input is matched for minimum noise figure and then the output is matched for maximum power gain
  - Corresponding load impedance for associated power gain
  - Source and load impedances for simultaneous conjugate matching (without regard to noise)
  - Input and output impedances when source and load are terminated in 50 ohms
  - Stability factor, K
  - Frequency of the S-parameter simulations

Available Gain, Noise, and Stability Circles (Circles_Ga_NF_Stability_FET.dds):

All at one bias point selected by moving a marker on the device's I-V curves:

- Stability factor, K, and source stability circles. Note that the Smith Chart size is fixed, so if the stability circles are far outside the Smith Chart, they will not be displayed. If you change the Smith Chart scaling to Auto Scale, the circles will be visible.
- Available gain and noise circles
- Minimum noise figure, source impedance (Zopt) required to achieve this noise figure, and the optimal load impedance for power transfer when the source impedance is Zopt
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1)
- Noise figure with the simultaneous conjugate match condition
- Noise figure, transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith Chart. This is useful if you must make some compromise between noise and gain, or if you need to avoid an unstable region.

Available Gain, Power Gain, and Stability Circles
(Circles_Ga_Gp_Stability_FET.dds):

All at one bias point selected by moving a marker on the device's I-V curves:

- Stability factor, K, and source and load stability circles. Note that the Smith Chart size is fixed, so if the stability circles are far outside the Smith Chart, they will not be displayed. If you change the Smith Chart scaling to "Auto Scale" then the circles will be visible.
- Available gain and power gain circles, on different Smith Charts
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1)
- Transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith Chart. This is useful if you need to avoid an unstable region.
- Transducer power gain, and optimal source impedance if the load impedance is chosen arbitrarily by moving a marker (GammaL) on a Smith Chart. This is useful if you need to avoid an unstable region.

Schematic Name

FET_IV_NF_SP

Data Display Names

FET_IV_NF_SP.dds

FET_NF_Matching.dds

Circles_Ga_NF_Stability_FET.dds

Circles_Ga_Gp_Stability_FET.dds

DC and Bias Point Simulation > FET Stability vs. Bias

Description

This simulates the S-parameters of a transistor, with the gate voltage swept and the drain bias voltage constant, to determine the stability factors as a function of gate voltage. It should help you determine the dependence of the stability factor on the bias point.

Needed to Use Schematic

Nonlinear FET model

Main Schematic Settings

VDS, gate voltage sweep limits, and frequency range for S-parameter simulation

Data Display Outputs

- Stability measure, B1, versus gate voltage and frequency
- Stability factor, K, versus gate voltage and frequency
- Geometrically-derived load stability factor, mu, versus gate voltage and frequency
- Geometrically-derived source stability factor, mu_prime, versus gate voltage and frequency

Schematic Name

FET_Stab_vs_bias

Data Display Name(s)

FET_Stab_vs_bias.dds

Chapter 4: S-Parameter Simulations

The templates in the S-Parameter Simulations are for simulating the small-signal characteristics, such as noise figure, available gain, stability, group delay, etc., of a device or an amplifier. Except for the last one, these simulations do not require a nonlinear model, but an amplifier with nonlinear models can be used.

S-Parameter Simulations > Noise Figure, S-Parameters, Stability, and Group Delay

Description

This simulates the S-parameters, noise figure, stability, and group delay of any two-port network, versus frequency. You may use it with an S-parameter data file, or with a nonlinear amplifier model.

Needed to Use Schematic

Any linear or nonlinear model, including measured S-parameters

Main Schematic Settings

Frequency sweep range

Data Display Outputs

NFmin, Matching for Gain and Noise Figure (NF_GA_Matching.dds):

- Minimum noise figure versus frequency
- dB(S21), maximum available gain, and associated gain (when the input is matched for NFmin and the output is then conjugately matched), versus frequency
- Stability factor versus frequency
- Smith chart with traces of the optimal source reflection coefficients for minimum noise figure, and the following reflection coefficients (gammas) at a frequency selected by moving a marker:
  - Gamma source for minimum noise figure
  - Gamma load for maximum power gain when input is terminated for minimum noise figure
  - Gamma source for simultaneous conjugate match (without regard to noise)
  - Gamma load for simultaneous conjugate match (without regard to noise)
- Listing columns of data corresponding to the frequency point selected by moving a marker:
  - S-parameters, dB
  - Maximum available power gain, dB
  - Minimum noise figure, dB

- Sopt for minimum noise figure in polar coordinates and in magnitude and phase
- Zopt for minimum noise figure
- Associated power gain in dB, if the input is matched for minimum noise figure and then the output is matched for maximum power gain
- Corresponding load impedance for associated power gain
- Source and load impedances for simultaneous conjugate matching (without regard to noise)
- Stability factor, K

Available Gain, Noise, and Stability Circles (Circles_Ga_NF_Stability.dds):

All at one frequency selected by moving a marker:

- Stability factor, K, and source stability circles. Note that the Smith Chart size is fixed, so if the stability circles are far outside the Smith Chart, they will not be displayed. If you change the Smith Chart scaling to Auto Scale, the circles will be visible.
- Available gain and noise circles
- Minimum noise figure, source impedance (Zopt) required to achieve this noise figure, and the optimal load impedance for power transfer when the source impedance is Zopt
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1)
- Noise figure with the simultaneous conjugate match condition
- Noise figure, transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith Chart. This is useful if you must make some compromise between noise and gain, or if you need to avoid an unstable region.

Available Gain, Power Gain, and Stability Circles (Circles_Ga_Gp_Stability.dds):

All at one frequency selected by moving a marker:

- Stability factor, K, and source and load stability circles. Note that the Smith Chart size is fixed, so if the stability circles are far outside the Smith Chart, they will not be displayed. If you change the Smith Chart scaling to Auto Scale, the circles will be visible.

- Available gain and power gain circles, on different Smith Charts
- Maximum available gain, and the source and load impedances required for simultaneous conjugate matching (only valid if K>1)
- Transducer power gain, and optimal load impedance if the source impedance is chosen arbitrarily by moving a marker (GammaS) on a Smith Chart. This is useful if you need to avoid an unstable region.
- Transducer power gain, and optimal source impedance if the load impedance is chosen arbitrarily by moving a marker (GammaL) on a Smith Chart. This is useful if you need to avoid an unstable region.

Source and Load Stability Circles and Factors (NF_Stab_Circles.dds) data display also uses the data from the NF_SP_Stability schematic, and outputs:

- Geometrically-derived source and load stability factors (mu and mu_prime) versus frequency. These are the minimum distances to the source and load stability circles.
- Smith chart showing source and load stability circles and the source reflection coefficient for minimum noise figure, and the load reflection coefficient for maximum power gain when the input is terminated for minimum noise figure. These two reflection coefficients are at a frequency point specified by moving a marker.
- Smith chart with the optimal source reflection coefficients for minimum noise figure versus frequency, and the following reflection coefficients (gammas) at a frequency selected by moving a marker:
- Gamma source for minimum noise figure
- Gamma load for maximum power gain when input is terminated for minimum noise figure
- Gamma source for simultaneous conjugate match (without regard to noise)
- Gamma load for simultaneous conjugate match (without regard to noise)
- Minimum noise figure at the selected frequency
- Maximum power gain if the source is matched for noise and then the output is conjugately matched

S-Parameters on Smith Chart and Polar Plots (S_Params_Quad_Smith_Plr.dds) data display also uses the data from the NF_SP_Stability schematic, and outputs:

- S11 and S22 on Smith Charts, also with a circle of constant VSWR
- S21 and S12 (linear units) on polar plots

S-Parameters on Smith Chart and Rect. Plots (S_Params_Quad_dB_Smith.dds) data display also uses the data from the NF_SP_Stability schematic, and outputs:

- S11 and S22 on Smith Charts, also with a circle of constant VSWR
- dB(S21) and dB(S12) on rectangular plots

Group Delay (GroupDelay.dds) data display also uses the data from the NF_SP_Stability schematic, and outputs:

- Group Delay in seconds, versus frequency.

Note This plot may be jagged if measured S-parameter data is simulated, and the number of measured points is small.

Noise Figure and Optimal Source Gamma for NFmin (NoiseFigure.dds):

- Minimum noise figure and noise figure with the system impedance, Z0, versus frequency
- Smith chart with the optimal source reflection coefficient for minimum noise figure, versus frequency and the optimal source reflection coefficient at one frequency selected by moving a marker
- Listing columns of data corresponding to the frequency point selected by moving a marker:
  - Minimum noise figure, dB
  - Zopt for minimum noise figure

Schematic Name

NF_SP_Stability

Data Display Names

NF_GA_Matching.dds

Circles_Ga_NF_Stability.dds

Circles_Ga_NF_Stability.dds

NF_Stab_Circles.dds

S_Params_Quad_Smith_Plr.dds

S_Params_Quad_dB_Smith.dds

GroupDelay.dds

NoiseFigure.dds

S-Parameter Simulations > Feedback Network Optimization to Attain Stability

Description

This schematic optimizes component values in input, output, and feedback stabilization networks, to stabilize a 2-port network, minimize the minimum noise figure, and maximize gain (dB(S21).) You may delete components or modify the structure of the stabilization networks.

Needed to Use Schematic

Any linear or nonlinear model, including measured S-parameters

Main Schematic Settings

Type of optimization algorithm (gradient, random, genetic, etc.), goal weighting, goal values, and frequency ranges over which noise figure and gain goals will be evaluated.

Data Display Outputs

- Geometrically-derived source and load stability factors
- Gain, dB(S21)
- Minimum noise figure
- Values of optimized components

Schematic Name

Gain_and_Stab_opt

Data display name

Gain_and_Stab_opt.dds

Note

The optimization results may vary substantially, depending on the type of optimization algorithm used (set on the Nominal Optimization controller) and on the goals. Noise figure and gain have been included as optimization goals. Otherwise, the optimizer might find a stable network, but with poor performance as an amplifier. The feedback network topology might be modified, but the data display will also have to be adjusted. For example, if you use a transmission line (instead of lumped elements) to attain stability and optimize the length and/or width of the line, these parameters can be displayed on the data display by inserting new listing columns.

S-Parameter Simulations > Gain, Noise Figure, Stability and Group Delay vs. Swept Parameters

Description

This schematic sweeps two parameters in a circuit to determine how gain, noise figure, matching impedances, stability and group delay depend on the two parameters. Often this sort of a simulation provides designers with more insight than an optimization. You must decide which two parameters to sweep, and you may modify the network to be simulated.

Needed to Use Schematic

Any linear or nonlinear model, including measured S-parameters

Main Schematic Settings

Network topology, two parameters to sweep and their sweep ranges, frequency range for S-parameter simulation

Data Display Outputs

Gain, Noise Figure and Matching vs. Swept Parameters
(NF_GA_Matching_sweep.dds)

- Minimum noise figure versus frequency
- dB(S21), maximum available gain, and associated gain (when the input is matched for NFmin and the output is then conjugately matched), versus frequency
- dB(S21), maximum available gain, and associated gain (when the input is matched for NFmin and the output is then conjugately matched), versus each swept parameter, with the other parameter held constant, at one frequency selected by a marker
- Stability factor versus frequency
- Smith chart with traces of the optimal source reflection coefficients for minimum noise figure, and the following reflection coefficients (gammas) at a frequency selected by moving a marker:
  - Gamma source for minimum noise figure
  - Gamma load for maximum power gain when input is terminated for minimum noise figure
  - Gamma source for simultaneous conjugate match (without regard to noise)

    - Gamma load for simultaneous conjugate match (without regard to noise)
- Listing columns of data corresponding to the frequency point selected by moving a marker:
    - S-parameters, dB
    - Maximum available power gain, dB
    - Minimum noise figure, dB
    - Sopt for minimum noise figure in polar coordinates and in magnitude and phase
    - Zopt for minimum noise figure
    - Associated power gain in dB, if the input is matched for minimum noise figure and then the output is matched for maximum power gain
    - Corresponding load impedance for associated power gain
    - Source and load impedances for simultaneous conjugate matching (without regard to noise)
    - Stability factor, K

Stability Factor and Noise Figure vs. Swept Parameters (NF_Stability_sweep.dds) data display also uses the data from the NF_SP_sweep schematic, and outputs:

- Stability factor, K, versus both swept parameters and frequency
- Stability factor, K, versus both swept parameters, at one frequency selected by moving a marker
- Minimum noise figure versus both swept parameters and frequency
- Minimum noise figure versus both swept parameters, at one frequency selected by moving a marker

S-Parameters and Gain vs. Swept Parameters (SP_sweep.dds) data display also uses the data from the NF_SP_sweep schematic, and outputs at a frequency selected by moving a marker:

- S-parameters versus both parameters
- Minimum noise figure versus both swept parameters
- Maximum available gain versus both swept parameters

Group Delay vs. Swept Parameters (GroupDelay_sweep.dds) data display also uses the data from the NF_SP_sweep schematic, and outputs:

- Group delay versus both swept parameters and frequency
- Group delay at one combination of the swept parameters, versus frequency

Schematic Name

NF_SP_sweep

Data Display Names

NF_GA_Matching_sweep.dds

NF_Stability_sweep.dds

SP_sweep.dds

GroupDelay_sweep.dds

Note

Some of the simulation results on these data displays can be obtained via the ADS 1.3 tuning feature. However, these data displays show the results in a format that may make it easier for you to analyze the data and determine what the optimal parameter values are.

S-Parameter Simulations > Stability, S-Parameters, and Group Delay vs. Frequency and Input Power

Description

This schematic simulates the large-signal S-parameters of a device, versus frequency and input power. The stability factor, K, is computed from these S-parameters, using the standard formula found in textbooks. This simulation setup differs from the LSSP controller in that small-signal mixer mode is used to inject a small signal at the output of the device, while the input is being driven by a large signal source. This gives a much more realistic simulation of S12 and S22.

Needed to Use Schematic

Nonlinear model, or an amplifier with nonlinear device models

Main Schematic Settings

Ranges over which to sweep the input signal frequency and power

Data Display Outputs

Stability and S-Parameters vs. Frequency and Input Power (Stab_vs_freq_pwr.dds):

- S-Parameters versus input frequency and input power
- Stability factor, K, versus input frequency and input power

Group Delay versus Frequency and Input Power (GroupDelay_vsFreqPwr.dds) data display also uses the data from the Stab_vs_freq_pwr schematic, and outputs:

- Group delay versus frequency, with the input power selected by moving a marker

Schematic Name

Stab_vs_freq_pwr

Data Display Names

Stab_vs_freq_pwr.dds

GroupDelay_vsFreqPwr.dds

Note

The stability factor is only computed at the frequency of the input signal. The stability factor at higher and lower frequencies is not computed.

Chapter 5: 1-Tone Nonlinear Simulations

The templates in the 1-Tone Nonlinear Simulations are for simulating the large-signal characteristics of an amplifier or device, such as gain, harmonic distortion, power-added efficiency, gain compression, etc. Setups for simulating these versus frequency, power, and arbitrary swept parameters are included. Load- and Source-pull simulations and impedance optimization setups are also included. These simulations do require nonlinear model(s).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion

Description

This is the most basic simulation setup, and it simulates the spectrum, output power, power gain, and harmonic distortion of a device or amplifier. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and available source power

Data Display Outputs

- Output spectrum and voltage waveform
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc

Schematic Name

HB1Tone

Data Display Name

HB1Tone.dds

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion (w/PAE)

Description

This simulation setup is identical to the HB1Tone schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, and harmonic distortion of a device or amplifier. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the notes, below.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main schematic settings

Input frequency, available source power, and bias settings

Data Display Outputs

- Output spectrum and input and output voltage waveforms
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Power-added efficiency (Pout at fundamental minus Available source power)/(DC power consumption)
- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier

Schematic Name

HB1TonePAE

Data Display Name

HB1TonePAE.dds

Note

Only bias supplies on the highest level schematic will be included in the PAE calculation. So, for example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high node*) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Power

Description

This simulation setup is identical to the HB1Tone schematic, except that available source power is swept. It simulates the spectrum, output power, power gain, gain compression, phase distortion, and harmonic distortion of a device or amplifier, all versus available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and available source power sweep range. The available source power sweep is divided into two parts (one coarse, and the other fine), for better resolution when the amplifier is being driven into compression.

Data Display Outputs

Spectrum, Gain, Harm. Distortion vs. Power (HB1TonePswp.dds):

All versus available source power:

- Output spectrum and voltage waveforms
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Phase shift and gain reduction (relative to simulation at lowest input power level), for use in the GComp7 section of S2D data file, for behavioral modeling

AM-to-AM, AM-to-PM Distortion vs. Power (HB1TonePswpAMtoPM.dds) data display also uses the data from the HB1TonePswp schematic, and outputs:

All versus available source power:

- AM-to-AM, AM-to-PM, characteristics
- Output power

- Gain
- Phase shift and gain reduction (relative to simulation at lowest input power level), for use in the GComp7 section of S2D data file, for behavioral modeling.
- Output Voltage waveforms

Schematic Name

HB1TonePswp

Data Display Names

HB1TonePswp.dds

HB1TonePswpAMtoPM.dds

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Power (w/PAE)

Description

This simulation setup is identical to the HB1TonePswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, gain compression, high supply current, DC power consumption, thermal dissipation, and harmonic distortion, of a device or amplifier, all versus available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the note on the following page.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Bias settings, input frequency and available source power sweep range. The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression.

Data Display Outputs

All versus available source power:

- Output spectrum and input and output voltage waveforms
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Power-added efficiency (Pout at fundamental minus Available source power)/(DC power consumption)
- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier
- Gain compression between any two simulation points specified via markers

The *AM-to-AM, AM-to-PM Distortion vs. Power* (HB1TonePswpAMtoPM.dds) data display, accessed by selecting *1-Tone Nonlinear Simulation Results* > *Spectrum, Gain, Harmonic Distortion vs. Power Results* will also display data from the *HB1TonePAE_Pswp* schematic, but you will have to set the default dataset name after opening the data display.

Schematic Name

HB1TonePAE_Pswp

Data Display Name

HB1TonePAE_Pswp.dds

Note

Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Frequency

Description

This simulation setup is similar to the HB1TonePswp schematic, except that the input signal frequency is swept. It simulates the spectrum, voltage waveform, output power, power gain, group delay, and harmonic distortion of a device or amplifier, all versus frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency sweep range and available source power

Data Display Outputs

All versus frequency:

- Output spectrum and voltage waveform, at a frequency selected by moving a marker
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Group delay

Schematic Name

HB1ToneFswp

Data Display Name

HB1ToneFswp.dds

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Frequency (w/PAE)

Description

This simulation setup is identical to the HB1ToneFswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, voltage waveform, output power, power gain, high supply current, DC power consumption, thermal dissipation, and harmonic distortion, of a device or amplifier, all versus frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the notes, below.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Bias settings, input frequency sweep range and available source power

Data Display Outputs

All versus frequency:

- Output spectrum, at a frequency selected by moving a marker
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Power-added efficiency (Pout at fundamental minus Available source power)/(DC power consumption)
- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier

Schematic Name

HB1TonePAE_Fswp

Data Display Name

HB1TonePAE_Fswp.dds

Note

Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the Vs_low node) * (the DC current in the *Is_low* current probe).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Frequency & Power

Description

This simulation setup is identical to the HB1TonePswp schematic, except that frequency is swept in addition to available source power. It simulates the spectrum, output power, power gain, gain compression, phase distortion, harmonic distortion, and group delay of a device or amplifier, all versus available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

input frequency sweep range and available source power sweep range. The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression.

Data Display Outputs

Spectrum, Gain, Harm. Distortion vs. Frequency and Power (HB1ToneFPswp.dds):

- All versus available source power, at a frequency selected by moving a marker:
  - Output power
  - Transducer power gain (power delivered to the load minus power available from the source)
  - Harmonic distortion up to the 5th, in dBc
  - Phase shift and gain reduction (relative to simulation at lowest input power level), for use in the GComp7 section of S2D data file, for behavioral modeling
- Group delay at one input power level selected by moving a marker
- Output spectrum at one input power and frequency, both selected by moving markers

AM-to-AM, AM-to-PM Distortion vs. Frequency and Power (HB1ToneFPswpAMtoPM.dds) data display also uses the data from the HB1ToneFPswp schematic, and outputs:

- All versus available source power, at a frequency selected by moving a marker:
  - AM-to-AM, AM-to-PM, characteristics
  - Output power
  - Gain
  - Phase shift and gain reduction (relative to simulation at lowest input power level), for use in GComp7 section of S2D data file, for behavioral modeling.
- Transducer power gain plots, versus frequency

Schematic Name

HB1ToneFPswp

Data Display Names

HB1ToneFPswp.dds

HB1ToneFPswpAMtoPM.dds

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion vs. Frequency & Power (w/PAE)

Description

This simulation setup is identical to the HB1ToneFPswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It simulates the spectrum, output power, power gain, gain compression, phase distortion, harmonic distortion, power-added efficiency, high supply current, DC power consumption, and thermal dissipation of a device or amplifier, all versus available source power and frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the note on the following page.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Bias settings, input frequency sweep range and available source power sweep range. The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression.

Data Display Outputs

Spectrum, Gain, Harm. Distortion vs. Frequency and Power (HB1TonePAE_FPswp.dds):

- All versus available source power, at a frequency selected by moving a marker
  - Output power
  - Transducer power gain (power delivered to the load minus power available from the source)
  - Harmonic distortion up to the 5th, in dBc
  - Power-added efficiency
  - DC power consumption
  - High supply current
  - Thermal dissipation
  - Input and output voltage waveforms
- Gain compression between two power levels selected by markers

- Output spectrum at one input power and frequency, both selected by moving markers

AM-to-AM, AM-to-PM Distortion vs. Frequency and Power (HB1TonePAE_FPswpAMtoPM.dds) data display also uses the data from the HB1ToneFPswp schematic, and outputs:

- All versus available source power, at a frequency selected by moving a marker:
  - AM-to-AM, AM-to-PM, characteristics
  - Output power
  - Gain
  - Phase shift and gain reduction (relative to simulation at lowest input power level), for use in the GComp7 section of S2D data file, for behavioral modeling.
- Transducer power gain plots, versus frequency

Schematic Name

HB1TonePAE_FPswp

Data Display Names

HB1TonePAE_FPswp.dds

HB1TonePAE_FPswpAMtoPM.dds

Note

Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion at X dB Gain Compression

Description

This is similar to the HB1Tone simulation setup, and it simulates the spectrum, output power, power gain, and harmonic distortion of a device or amplifier at the X dB power gain compression point. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency, the amount of power gain compression, in dB, and the source and load impedances at the fundamental and harmonic frequencies

Data Display Outputs

All at the X dB gain compression point:

- Output spectrum and voltage waveform
- Fundamental output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc

Schematic Name

HB1ToneGComp

Data Display Name

HB1ToneGComp.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable. This gain compression simulation

might not work well on amplifiers that have low gain at low signal level (like Class B amplifiers) or ones that have excessive gain expansion. In this case, use one of the simulation setups that explicitly sweeps power.

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion at X dB Gain Compression vs. Freq.

Description

This is similar to the HB1ToneFswp simulation setup, and it simulates the spectrum, output power, power gain, harmonic distortion, and group delay of a device or amplifier at the X dB power gain compression point, versus frequency. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. This simulation is repeated at each input frequency in a range you specify. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Range of input frequencies, the amount of power gain compression, in dB, and the source and load impedances at the fundamental and harmonic frequencies

Data Display Output

All at the X dB gain compression point, and versus input frequency:

- Output spectrum and voltage waveform at a frequency selected by moving a marker
- Fundamental output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Group Delay

Schematic Name

HB1ToneGCompFswp

Data Display Name

HB1ToneGCompFswp.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable. This gain compression simulation might not work well on amplifiers that have low gain at low signal level (like Class B amplifiers) or ones that have excessive gain expansion. In this case, use one of the simulation setups that explicitly sweeps power.

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 1 Param.

Description

This simulates the spectrum, output power, power gain, harmonic distortion, power-added efficiency, etc. of a device or amplifier at the X dB power gain compression point, versus an arbitrary swept parameter. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

The arbitrary swept parameter and its range of values, the amount of power gain compression, in dB, and the source and load impedances at the fundamental and harmonic frequencies.

Data Display Outputs

All at the X dB gain compression point, and versus the arbitrary, swept parameter:

- Output spectrum at one parameter value selected by moving a marker
- Fundamental output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc
- Power-added efficiency
- Supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier

Schematic Name

HB1ToneGComp1swp

Data Display Name

HB1ToneGComp1swp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
3. This gain compression simulation might not work well on amplifiers that have low gain at low signal level (like Class B amplifiers) or ones that have excessive gain expansion.

1-Tone Nonlinear Simulations > Spectrum, Gain, Harmonic Distortion at X dB Gain Compression (w/PAE) vs. 2 Param.

Description

This simulates the spectrum, output power, power gain, harmonic distortion, power-added efficiency, etc. of a device or amplifier at the X dB power gain compression point, versus two arbitrary swept parameters. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

The arbitrary swept parameters and their range of values, the amount of power gain compression, in dB, and the source and load impedances at the fundamental and harmonic frequencies.

Data Display Outputs

All at the X dB gain compression point:

- Output spectrum at one set of parameter values selected by moving markers
- Output voltage waveforms for all values of parameter 2, with parameter 1 selected by moving a marker
- Plots of fundamental output power, power-added efficiency, transducer power gain (power delivered to the load minus power available from the source), high supply current, and third harmonic distortion, all versus both swept parameters
- Tables of data versus swept parameter 2, with swept parameter 1 fixed (selected by moving a marker):
  - Harmonic distortion up to the 5th, in dBc
  - Power-added efficiency
  - Transducer power gain
  - Supply current

- DC power consumption
- Thermal power dissipation in the device or amplifier

Schematic Name

HB1ToneGComp2swp

Data Display Name

HB1ToneGComp2swp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
3. This gain compression simulation might not work well on amplifiers that have low gain at low signal level (like Class B amplifiers) or ones that have excessive gain expansion.

1-Tone Nonlinear Simulations > Noise Figure, Spectrum, Gain, Harmonic Distortion

Description

This simulates the spectrum, output power, transducer power gain, and harmonic distortion of a device or amplifier at a single RF frequency and power, as well as its noise figure within a narrow band of frequencies around the RF frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, range of noise frequencies

Data Display Outputs

- Noise figure with Z0 ohm source impedance
- Minimum noise figure with the optimal source impedance
- Optimal source impedance and reflection coefficient versus noise frequency
- Output spectrum and voltage waveform
- Output power
- Transducer power gain (power delivered to the load minus power available from the source)
- Harmonic distortion up to the 5th, in dBc

Schematic Name

HB1ToneNoise

Data Display Name

HB1ToneNoise.dds

1-Tone Nonlinear Simulations > Large-Signal Load Impedance Mapping

Description

This simulates the input reflection coefficient of a device, as a function of the impedance presented to its output (the load impedance). If the load impedances map to the outside of the Smith chart when looking into the input port, the device is potentially unstable. The input signal power can be set arbitrarily. The load values correspond to several of the main lines on the Smith chart. A sample device is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, maximum number of load impedances simulated and maximum load reflection coefficient (between 0 and 1).

Data Display Outputs

- Smith chart with simulated load impedances
- Input reflection coefficients that correspond to the load impedances
- Maximum output power, power gain, and load impedance corresponding to the maximum (from among the load impedances simulated)
- Output power, power gain, and voltage gain that correspond to a marker on the input reflection coefficient plot

Schematic Name

LoadMapper

Data Display Name

LoadMapper.dds

1-Tone Nonlinear Simulations > Load-Pull - PAE, Output Power Contours

Description

This simulates the output power and power-added efficiency contours of a device or amplifier at a single RF frequency and power, as a function of the load reflection coefficient, at the fundamental frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, circular region of the Smith chart, specifying load reflection coefficients, load impedances at harmonic frequencies (Z_l_2 - Z_l_5), and source impedances at the fundamental and harmonic frequencies (Z_s_fund - Z_s_5.)

Data Display Outputs

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- The simulated load impedances on a Smith chart, and the PAE, power delivered, and the impedance corresponding to a marker location

Schematic Name

HB1Tone_LoadPull

Data Display Name

HB1Tone_LoadPull.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is

computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some load impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results > Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid using load impedances within the unstable region if the load stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

1-Tone Nonlinear Simulations > Load-Pull - PAE, Output Power Contours at X dB Gain Compression

Description

This simulates the output power and power-added efficiency contours of a device or amplifier at a single RF frequency at the X dB power gain compression point, as a function of the load reflection coefficient, at the fundamental frequency. You can specify the amount of gain compression, X, in dB. The simulator then increases the available source power to the device until the power gain has been reduced by X dB, relative to its small-signal value. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, circular region of the Smith chart, specifying load reflection coefficients, load impedances at harmonic frequencies (Z_l_2 - Z_l_5), and source impedances at the fundamental and harmonic frequencies (Z_s_fund - Z_s_5.)

Data Display Outputs

All at the X dB gain compression point:

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- The simulated load impedances on a Smith chart, and the PAE, power delivered, and the impedance corresponding to a marker location

Schematic Name

HB1Tone_LoadPull_GComp

Data Display Name

HB1Tone_LoadPull_GComp.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some load impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results > Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid using load impedances within the unstable region if the load stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

1-Tone Nonlinear Simulations > Source-Pull - PAE, Output Power Contours

Description

This simulates the output power and power-added efficiency contours of a device or amplifier at a single RF frequency and power, as a function of the source reflection coefficient, at the fundamental frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Input frequency and power, circular region of the Smith chart, specifying source reflection coefficients, source impedances at harmonic frequencies (Z_s_2 - Z_s_5), and load impedances at the fundamental and harmonic frequencies (Z_l_fund - Z_l_5.)

Data Display Outputs

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- The simulated source impedances on a Smith chart, and the PAE, power delivered, and the impedance corresponding to a marker location

Schematic Name

HB1Tone_SourcePull

Data Display Name

HB1Tone_SourcePull.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results > Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid using source impedances within the unstable region if the source stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

1-Tone Nonlinear Simulations > Harmonic Impedance Opt. - PAE, Output Power & Gain

Description

This setup determines the optimal source and load impedances to present to a device. It optimizes the source and load fundamental and harmonic impedances (up to the 5th) simultaneously, to maximize power-added efficiency, and deliver a specified power to the load. It differs from the load- and source-pull simulations in that it varies both source and load impedances simultaneously, and it varies harmonic impedances. A sample device is provided. You must replace this device with your own device, and modify the biases, as needed.

Needed to Use Schematic

A device using a nonlinear model

Main Schematic Settings

Input frequency and range of allowed values for the available source power, desired power delivered to the load and minimum power-added efficiency. Also, the range of allowed source and load impedances must be specified, in terms of real and imaginary parts, at the fundamental and harmonic frequencies.

Data Display Outputs

For the best impedance values found during the optimization:

- Power-added efficiency
- Power delivered to the load in dBm and Watts
- Power available from the source and power (at the fundamental frequency) delivered to the device
- Operating power gain (power delivered to the load / power delivered to the device)
- Transducer power gain (power delivered to the load / power available from the source)
- Thermal dissipation in the device
- DC power consumption
- Total input power (DC power consumption + power delivered to the device at fundamental and all harmonic frequencies)

- Total output power (power delivered to the load at fundamental and all harmonic frequencies)
- Output spectrum (dBm) and harmonic distortion in dBc.

Source and Load Harmonic Impedances (HarmZopt1toneSC.dds):

- Smith chart showing the optimal source impedances at fundamental and harmonic frequencies
- Smith chart showing the optimal load impedances at fundamental and harmonic frequencies
- Smith charts showing the source and load impedances renormalized to an arbitrary impedance
- Listings of optimal source and load impedances and reflection coefficients

Input and Output Waveforms and Dynamic Load Line (HarmZopt1toneTime.dds):

- Input and output voltages versus time
- Input and output currents versus time
- Input current versus input voltage and output current versus output voltage

Schematic Name

HarmZopt1tone

Data Display Names

HarmZopt1tone.dds

HarmZopt1toneSC.dds

HarmZopt1toneTime.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some load and source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results > Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid using load and source impedances within the unstable region if the load and source stability circles are inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.
3. The schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > 1-Tone Nonlinear Simulations > Harmonic Gamma Opt. - PAE, Output Power & Gain* might be better to use if you must specify ranges of impedances that avoid unstable regions of the Smith chart.
4. If you don't think that impedances at the fourth and fifth harmonics (for example) are going to have much effect on the performance of the device, you can fix these values by changing the word *opt* in their equation definitions to *noopt*. This will speed up the optimization.
5. The speed and success of the optimization will depend on the parameters that you set on the Nominal Optimization controller. Refer to the ADS *Optimization and Statistical Design* manual for more details.

1-Tone Nonlinear Simulations > Harmonic Gamma Opt. - PAE, Output Power & Gain

Description

This setup determines the optimal source and load impedances to present to a device. It is very similar to the Harmonic Impedance Opt. setup previously described, except that allowed source and load reflection coefficients are defined as circular regions of the Smith chart, instead of defining ranges of impedances. It optimizes the source and load fundamental and harmonic reflection coefficients (up to the 5th) simultaneously, to maximize power-added efficiency, and deliver a specified power to the load. It differs from the load- and source-pull simulations in that it varies both source and load reflection coefficients simultaneously, at both fundamental and harmonic frequencies. A sample device is provided. You must replace this device with your own device, and modify the biases, as needed.

Needed to Use Schematic

A device using a nonlinear model

Main Schematic Settings

Input frequency and range of allowed values for the available source power, desired power delivered to the load and minimum power-added efficiency. Also, the range of allowed source and load reflection coefficients must be specified, as circular regions of the Smith chart, at the fundamental and harmonic frequencies.

Data Display Outputs

PAE, Output Power, Gain, Dissipation (HarmGammaOpt1tone.dds):

For the best impedance values found during the optimization:

- Power-added efficiency
- Power delivered to the load in dBm and Watts
- Power available from the source and power (at the fundamental frequency) delivered to the device
- Operating power gain (power delivered to the load / power delivered to the device)
- Transducer power gain (power delivered to the load / power available from the source)
- Thermal dissipation in the device

- DC power consumption
- Total input power (DC power consumption + power delivered to the device at fundamental and all harmonic frequencies)
- Total output power (power delivered to the load at fundamental and all harmonic frequencies)
- Output spectrum (dBm) and harmonic distortion in dBc.

Source and Load Harmonic Impedances (HarmGammaOpt1toneSC.dds):

- Smith chart showing the optimal source impedances at fundamental and harmonic frequencies
- Smith chart showing the optimal load impedances at fundamental and harmonic frequencies
- Smith charts showing the source and load impedances renormalized to an arbitrary impedance
- Listings of optimal source and load impedances and reflection coefficients

Input and Output Waveforms and Dynamic Load Line (HarmGammaOpt1toneTime.dds):

- Input and output voltages versus time
- Input and output currents versus time
- Input current versus input voltage and output current versus output voltage

Schematic Name

HarmGammaOpt1tone

Data Display Names

HarmGammaOpt1tone.dds,

HarmGammaOpt1toneSC.dds

HarmGammaOpt1toneTime.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is

computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some load and source reflection coefficients, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results > Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid using load and source reflection coefficients within the unstable region if the load and source stability circles are inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

3. If you don't think that reflection coefficients at the fourth and fifth harmonics (for example) are going to have much effect on the performance of the device, you can fix these values by changing the word *opt* in their equation definitions to *noopt*. These equations can be seen by editing the VAR block, *Load_Gamma_Parameters*, and modifying the equation for angle_L_4th, for example. If you set this equal to 0 rather than *0 opt(-pi to pi)*, then the angle of the reflection coefficient will be fixed at 0 radians. The variable *sample_radius_L_4th* as well as the variables for the 5th harmonic and for the load can be modified in the same way. This will speed up the optimization.

4. The speed and success of the optimization will depend on the parameters that you set on the Nominal Optimization controller. Refer to the ADS *Optimization and Statistical Design* manual for more details.

Chapter 6: 2-Tone Nonlinear Simulations

The templates in the 2-Tone Nonlinear Simulations are for simulating the large-signal characteristics of an amplifier or device, such as gain, harmonic distortion, power-added efficiency, gain compression, intermodulation distortion, etc. Setups for simulating these versus frequency, power, and arbitrary swept parameters are included. Load- and Source-pull simulations and impedance optimization setups are also included. These simulations do require nonlinear model(s).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points

Description

This is the most basic simulation setup, and it simulates the spectrum, output power, power gain, and harmonic distortion of a device or amplifier. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, available source power (from both tones), and maximum order of the intermodulation terms to be computed. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

- Broadband output spectrum and spectrum centered on the two fundamental output tones
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones))
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms

Schematic Name

HB2Tone

Data Display Name

HB2Tone.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points (w/PAE)

Description

This simulation setup is identical to the HB2Tone schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and you can modify the biases, as described in the notes, below.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, available source power (from both tones), maximum order of the intermodulation terms to be computed, and the bias settings. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

- Broadband output spectrum and spectrum centered on the two fundamental output tones
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones))
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
- Power-added efficiency (Output power (*both tones*) minus power available from the source (*both tones*)/(DC power consumption)
- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier (DC power consumption plus power delivered to the device at all frequencies minus power delivered to the load at all frequencies)

Schematic Name

HB2TonePAE

Data Display Name

HB2TonePAE.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. Power

Description

This simulation setup is identical to the HB2Tone schematic, except that available source power (in both tones) is swept. It simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus the available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s).

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, maximum order of the intermodulation terms to be computed, and swept values of the available source power (from both tones). The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the available source power (in both tones):

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one available source power selected by moving a marker)
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column
- Gain compression
- Plots of third- and fifth-order intermodulation distortion versus output power
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms

Schematic Name

HB2TonePswp

Data Display Name

HB2TonePswp.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. Power (w/PAE)

Description

This simulation setup is identical to the HB2TonePswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus the available source power. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, maximum order of the intermodulation terms to be computed, and swept values of the available source power (from both tones). The available source power sweep is divided into two parts, one coarse, and the other fine, for better resolution when the amplifier is being driven into compression. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the available source power (in both tones):

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one available source power selected by moving a marker)
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column
- Gain compression
- Plots of third- and fifth-order intermodulation distortion versus output power
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
- Power-added efficiency (Output power (both tones) minus power available from the source (both tones))/(DC power consumption), in a plot and a listing column

- High supply current
- DC power consumption
- Thermal power dissipation in the device or amplifier (DC power consumption + power delivered to the device at all frequencies minus power delivered to the load at all frequencies)

Schematic Name

HB2TonePAE_Pswp

Data Display Name

HB2TonePAE_Pswp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation.For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. Frequency

Description

This simulation setup is identical to the HB2Tone schematic, except that the center frequency of the two input tones is swept. It simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Range of center frequencies of the two input tones, the frequency spacing between them, maximum order of the intermodulation terms to be computed, and the available source power (from both tones). The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the center frequency of the two tones:

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one center frequency selected by moving a marker)
- Output power (both tones), in a plot and a listing column
- Transducer power gain (power (both tones)) delivered to the load minus power available from the source (both tones), in a plot and a listing column
- Plots of third- and fifth-order intercept points
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms

Schematic Name

HB2ToneFswp

Data Display Name

HB2ToneFswp.dds

Note

When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. Frequency (w/PAE)

Description

This simulation setup is identical to the HB2ToneFswp schematic, except that it includes two current probes and named voltage nodes for calculating power-added efficiency. It also simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus frequency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Range of swept center frequencies of the two input tones, the frequency spacing between them, the maximum order of the intermodulation terms to be computed, available source power from both tones, and the bias settings. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the center frequency of the two tones:

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one frequency selected by moving a marker)
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column
- Plots of third- and fifth-order intermodulation distortion
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
- Power-added efficiency (Output power (both tones) minus power available from the source (both tones))/(DC power consumption), in a plot and a listing column
- High supply current
- DC power consumption

- Thermal power dissipation in the device or amplifier (DC power consumption plus power delivered to the device at all frequencies minus power delivered to the load at all frequencies)

Schematic Name

HB2TonePAE_Fswp

Data Display Name

HB2TonePAE_Fswp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the `Vs_high` node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. 1 Param. (w/PAE)

Description

This setup simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus one arbitrary swept parameter. It includes two current probes and named voltage nodes for calculating power-added efficiency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

The arbitrary swept parameter and its range of values, the center frequency of the two input tones, the frequency spacing between them, the maximum order of the intermodulation terms to be computed, available source power from both tones, and the bias settings. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the swept parameter:

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one of the swept parameter values selected by moving a marker)
- Output power (both tones)
- Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column
- Plots of third- and fifth-order intermodulation distortion
- Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
- Power-added efficiency (Output power (both tones) minus power available from the source (both tones))/(DC power consumption), in a plot and a listing column
- High supply current
- DC power consumption

- Thermal power dissipation in the device or amplifier (DC power consumption plus power delivered to the device at all frequencies minus power delivered to the load at all frequencies)

Schematic Name

HB2TonePAE_1swp

Data Display Name

HB2TonePAE_1swp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Spectrum, Gain, TOI and 5thOI Points vs. 2 Param. (w/PAE)

Description

This setup simulates the spectrum, output power, power gain, and intermodulation distortion of a device or amplifier all versus two arbitrary swept parameters. It includes two current probes and named voltage nodes for calculating power-added efficiency. A sample power amplifier is provided. You must replace this amplifier with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

The arbitrary swept parameters and their ranges of values, the center frequency of the two input tones, the frequency spacing between them, the maximum order of the intermodulation terms to be computed, available source power from both tones, and the bias settings. The source and load impedances at the fundamental and harmonic frequencies can also be set.

Data Display Outputs

All versus the swept parameters (Param1 and Param2):

- Broadband output spectrum and spectrum centered on the two fundamental output tones (at one pair of swept parameter values selected by moving two markers)
- Tables of data versus swept parameter 2, with swept parameter 1 fixed (selected by moving a marker):
  - Output power (both tones)
  - Input and output third-order intercept and fifth-order intercept points, calculated using the low side intermodulation and high side intermodulation distortion terms
  - Power-added efficiency (Output power (both tones) minus power available from the source (both tones))/(DC power consumption), in a plot and a listing column
  - Transducer power gain (power (both tones) delivered to the load minus power available from the source (both tones)), in a plot and a listing column

  - Supply current
  - DC power consumption
  - Thermal power dissipation in the device or amplifier (DC power consumption + power delivered to the device at all frequencies minus power delivered to the load at all frequencies)
- Contour plots of output power (both tones) and power-added efficiency
- Maximum output power and power-added efficiency
- Contour plots of third- and fifth-order intermodulation distortion
- Minimum 3rd- and 5th-order intermodulation distortion levels, in dBc

Schematic Name

HB2TonePAE_2swp

Data Display Name

HB2TonePAE_2swp.dds

Notes

1. When simulating a device, setting the source and load impedances at the fundamental and harmonic frequencies might be useful. However, when simulating an amplifier that already has source and load impedance matching networks, just leaving all these impedances at 50 ohms might be suitable.
2. Only bias supplies on the highest level schematic will be included in the PAE calculation. For example, if you replace the sample amplifier with one with the bias supplies included in the subcircuit, those supplies will not be included in the PAE calculation. On the highest level schematic, you can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2-Tone Nonlinear Simulations > Load-Pull - PAE, Output Power & IMD Contours

Description

This simulates the output power, power-added efficiency, and 3rd- and 5th-order intermodulation distortion contours of a device or amplifier with two input tones at one power level, as a function of the load reflection coefficient, at the fundamental frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, available source power (from both tones), maximum order of the intermodulation terms to be computed, and the bias settings. The load reflection coefficients are specified by defining a circular region of the Smith chart. Load impedances at harmonic frequencies (Z_l_2 - Z_l_5), and source impedances at the fundamental and harmonic frequencies (Z_s_fund - Z_s_5) can also be specified.

Data Display Outputs

Load-Pull - PAE, Output Power & IMD Contours (HB2Tone_LoadPull.dds):

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- Contours of equal 3rd- and 5th-order intermodulation distortion (IMD), on a Smith chart
- Minimum 3rd- and 5th-order IMD, in dBc
- Contours of equal 3rd- and 5th-order IMD, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal 3rd- and 5th-order IMD, on a rectangular plot

Load-Pull - Contours and Spectrum (HB2Tone_LoadPullmore.dds):

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- Contours of equal 3rd- and 5th-order intermodulation distortion (IMD), on a Smith chart
- Minimum 3rd- and 5th-order IMD, in dBc
- Contours of equal 3rd- and 5th-order IMD, on a rectangular plot
- The simulated load impedances on a Smith chart, and the PAE, power delivered, 3rd- and 5th-order intermodulation distortion and the impedance corresponding to a marker location

Schematic Name

HB2Tone_LoadPull

Data Display Names

HB2Tone_LoadPull.dds

HB2Tone_LoadPullmore.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some load impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results > Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid

using load impedances within the unstable region if the load stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

2-Tone Nonlinear Simulations > Source-Pull - PAE, Output Power & IMD Contours

Description

This simulates the output power, power-added efficiency, and 3rd- and 5th-order intermodulation distortion contours of a device or amplifier with two input tones at one power level, as a function of the source reflection coefficient, at the fundamental frequency. A sample device is provided. You must replace this device with your own device or amplifier, and modify the biases, as needed.

Needed to Use Schematic

A device or an amplifier using nonlinear model(s)

Main Schematic Settings

Center frequency of the two input tones, the frequency spacing between them, available source power (from both tones), maximum order of the intermodulation terms to be computed, and the bias settings. The source reflection coefficients are specified by defining a circular region of the Smith chart. Source impedances at harmonic frequencies (Z_s_2 - Z_s_5), and load impedances at the fundamental and harmonic frequencies (Z_l_fund - Z_l_5) can also be specified.

Data Display Outputs

Source-Pull - PAE, Output Power & IMD Contours (HB2Tone_SourcePull.dds):

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- Contours of equal 3rd- and 5th-order intermodulation distortion (IMD), on a Smith chart
- Minimum 3rd- and 5th-order IMD, in dBc
- Contours of equal 3rd- and 5th-order IMD, on a Smith chart renormalized to an arbitrary impedance
- Contours of equal 3rd- and 5th-order IMD, on a rectangular plot

Source-Pull - Contours and Spectrum (HB2Tone_SourcePullmore.dds):

- Contours of equal power-added efficiency and power delivered, on a Smith chart
- Maximum power-added efficiency, in percent and maximum power delivered in dBm
- Contours of equal power-added efficiency and power delivered, on a rectangular plot
- Contours of equal 3rd- and 5th-order intermodulation distortion (IMD), on a Smith chart
- Minimum 3rd- and 5th-order IMD, in dBc
- Contours of equal 3rd- and 5th-order IMD, on a rectangular plot
- The simulated source impedances on a Smith chart, and the PAE, power delivered, 3rd- and 5th-order intermodulation distortion and the impedance corresponding to a marker location

Schematic Name

HB2Tone_SourcePull

Data Display Names

HB2Tone_SourcePull.dds

HB2Tone_SourcePullmore.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).
2. For some source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection DesignGuide > *Power Amplifier DesignGuide* > *S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results* > *Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid

using source impedances within the unstable region if the source stability circle is inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

2-Tone Nonlinear Simulations > Harmonic Impedance Opt. - PAE, Output Power, Gain & IMD

Description

This setup determines the optimal source and load impedances to present to a device. It optimizes the source and load fundamental and harmonic impedances (up to the 5th) simultaneously, to maximize power-added efficiency, deliver a specified power to the load, and minimize 3rd-, 5th-, and 7th-order intermodulation distortion. It differs from the load- and source-pull simulations in that it varies both source and load impedances simultaneously, and it varies harmonic impedances. A sample device is provided. You must replace this device with your own device, and modify the biases, as needed.

Needed to Use Schematic

A device using a nonlinear model

Main Schematic Setting

Input frequencies of the two tones and range of allowed values for the available source power, desired power delivered to the load, minimum power-added efficiency, and maximum intermodulation distortion levels. Also, the range of allowed source and load impedances must be specified, in terms of real and imaginary parts, at the fundamental and harmonic frequencies.

Data Display Outputs

PAE, Output Power, Gain, IMD, Dissipation (HarmZopt2tone.dds)

For the best impedance values found during the optimization:

- Power-added efficiency
- Power delivered to the load in dBm and Watts
- Power available from both sources and power (at both fundamental frequencies) delivered to the device
- Operating power gain (power delivered to the load / power delivered to the device)
- Transducer power gain (power delivered to the load / power available from the source)
- Thermal dissipation in the device
- DC power consumption

- Total input power (DC power consumption + power delivered to the device at fundamental and all harmonic frequencies)
- Total output power (power delivered to the load at fundamental and all harmonic frequencies)
- Output spectrum (dBm) and intermodulation distortion in dBc.

Source and Load Harmonic Impedances (HarmZopt2toneSC.dds):

- Smith chart showing the optimal source impedances at baseband, fundamental and harmonic frequencies
- Smith chart showing the optimal load impedances at baseband, fundamental and harmonic frequencies
- Smith charts showing the source and load impedances renormalized to an arbitrary impedance
- Listings of optimal source and load impedances and reflection coefficients

Input and Output Waveforms and Dynamic Load Line (HarmZopt2toneTime.dds):

- Input and output voltages versus time
- Input and output currents versus time
- Input current versus input voltage and output current versus output voltage

Schematic Name

HarmZopt2tone

Data Display Names

HarmZopt2tone.dds

HarmZopt2toneSC.dds

HarmZopt2toneTime.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some load and source impedances, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results > Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid using load and source impedances within the unstable region if the load and source stability circles are inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

3. The schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > 2-Tone Nonlinear Simulations > Harmonic Gamma Opt. - PAE, Output Power, Gain & IMD* might be better to use if you must specify ranges of impedances that avoid unstable regions of the Smith chart.

4. If you don't think that impedances at the fourth and fifth harmonics (for example) are going to have much effect on the performance of the device, you can fix these values by changing the word *opt* in their equation definitions to *noopt*. This will speed up the optimization.

5. The speed and success of the optimization will depend on the parameters that you set on the Nominal Optimization controller. Refer to the ADS *Optimization and Statistical Design* manual for more details.

2-Tone Nonlinear Simulations > Harmonic Gamma Opt. - PAE, Output Power, Gain, & IMD

Description

This setup determines the optimal source and load impedances to present to a device. It is very similar to the Harmonic Impedance Opt. setup previously described, except that allowed source and load reflection coefficients are defined as circular regions of the Smith chart, instead of defining ranges of impedances. It optimizes the source and load fundamental and harmonic reflection coefficients (up to the 5th) simultaneously, to maximize power-added efficiency, deliver a specified power to the load, and minimize 3rd-, 5th-, and 7th-order intermodulation distortion. It differs from the load- and source-pull simulations in that it varies both source and load reflection coefficients simultaneously, at both fundamental and harmonic frequencies. A sample device is provided. You must replace this device with your own device, and modify the biases, as needed.

Needed to Use Schematic

A device using a nonlinear model

Main Schematic Settings

Input frequency and range of allowed values for the available source power, desired power delivered to the load, minimum power-added efficiency, and maximum intermodulation distortion levels. Also, the range of allowed source and load reflection coefficients must be specified, as circular regions of the Smith chart, at the fundamental and harmonic frequencies.

Data Display Outputs

PAE, Output Power, Gain, IMD, Dissipation (HarmGammaOpt2tone.dds):

For the best impedance values found during the optimization:

- Power-added efficiency
- Power delivered to the load in dBm and Watts
- Power available from both sources and power (at both fundamental frequencies) delivered to the device
- Operating power gain (power delivered to the load / power delivered to the device)
- Transducer power gain (power delivered to the load / power available from the source)

- Thermal dissipation in the device
- DC power consumption
- Total input power (DC power consumption + power delivered to the device at fundamental and all harmonic frequencies)
- Total output power (power delivered to the load at fundamental and all harmonic frequencies)
- Output spectrum (dBm) and intermodulation distortion in dBc.

Source and Load Harmonic Impedances (HarmGammaOpt2toneSC.dds):

- Smith chart showing the optimal source impedances at baseband, fundamental and harmonic frequencies
- Smith chart showing the optimal load impedances at baseband, fundamental and harmonic frequencies
- Smith charts showing the source and load impedances renormalized to an arbitrary impedance
- Listings of optimal source and load impedances and reflection coefficients

Input and Output Waveforms and Dynamic Load Line (HarmGammaOpt2toneTime.dds):

- Input and output voltages versus time
- Input and output currents versus time
- Input current versus input voltage and output current versus output voltage

Schematic Name

HarmGammaOpt2tone

Data Display Names

HarmGammaOpt2tone.dds

HarmGammaOpt2toneSC.dds

HarmGammaOpt2toneTime.dds

Notes

1. You can delete one of the two supplies and/or replace the voltage sources with current sources, and the PAE calculation will still be valid. You can modify the components in the bias network, realizing that the DC power consumption is

computed as (the DC voltage at the *Vs_high* node) * (the DC current in the *Is_high* current probe) + (the DC voltage at the *Vs_low* node) * (the DC current in the *Is_low* current probe).

2. For some load and source reflection coefficients, the device might be unstable. For this reason, you might want to simulate the stability circles of the device at a particular bias point, to check for instabilities. To do this, copy the biased device into the schematic generated from the menu selection *DesignGuide > Power Amplifier DesignGuide > S-Parameter*. The stability circles can be displayed by selecting *S-Parameter Simulation Results > Noise Figure, S-Params., Stability, and Group Delay Results*, then *Source and Load Stability Circles and Factors*. Avoid using load and source reflection coefficients within the unstable region if the load and source stability circles are inside the Smith chart. You might also want to use some of the other DesignGuide schematics to test for stability with a large input signal.

3. If you don't think that reflection coefficients at the fourth and fifth harmonics (for example) are going to have much effect on the performance of the device, you can fix these values by changing the word *opt* in their equation definitions to *noopt*. These equations can be seen by editing the VAR block, *Load_Gamma_Parameters*, and modifying the equation for angle_L_4th, for example. If you set this equal to 0 rather than *0 opt(-pi to pi*), the angle of the reflection coefficient will be fixed at 0 radians. The variable *sample_radius_L_4th* as well as the variables for the 5th harmonic and for the load can be modified in the same way. This will speed up the optimization.

4. The speed and success of the optimization will depend on the parameters that you set on the Nominal Optimization controller. Refer to the ADS *Optimization and Statistical Design* manual for more details.

Chapter 7: Lumped 2-Element Z-Y Matching Networks

The templates in the Lumped 2-Element Z-Y Matching Networks are for synthesizing an arbitrary impedance or admittance, or for matching to a device's equivalent circuit that is modeled as an R-C or R-L network. The matching networks use only lumped, ideal elements, and the impedance match is only for a single frequency, so the capabilities of these templates are rather limited. You might wish to use E-Syn or the Passive Circuit DesignGuide for impedance matching.

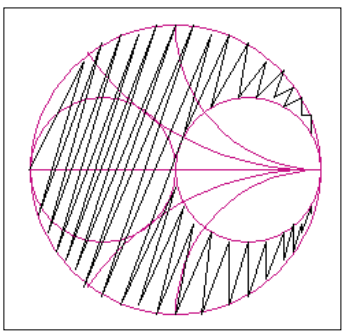
Lumped 2-Element Z-Y Matching Networks > Rload, Shunt C/L, Series C/L for Desired Z

Description

This schematic synthesizes two different networks that convert a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via shunt C – series L and shunt L – series C ladder networks.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Only impedances in one region (hashed in the figure shown here) of the Smith chart can be generated with these networks, but the next schematic will generate impedances outside this region.



Main Schematic Settings

Desired impedance, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart

- Reflection coefficient (dB) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Zdesired1

Data Display Name

Zdesired1.dds

Lumped 2-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L for Desired Z

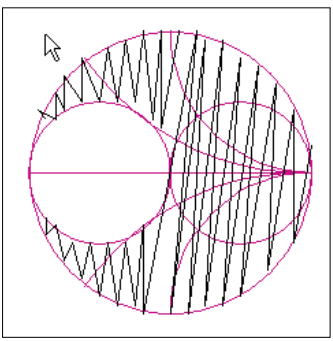
Description

This schematic synthesizes two different networks that convert a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via series L – shunt C and series C – shunt L ladder networks.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display,

---

Only impedances in one region (hashed in the figure shown here) of the Smith chart can be generated with these networks, but the previous schematic will generate impedances outside this region..



Main Schematic Settings

Desired impedance, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart

- Reflection coefficient (dB) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Zdesired2

Data Display Name

Zdesired2.dds

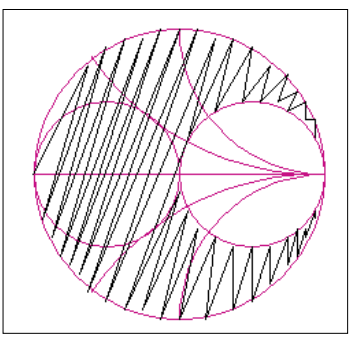
Lumped 2-Element Z-Y Matching Networks > Rload, Shunt C/L, Series C/L for Desired Y

Description

This schematic synthesizes two different networks that convert a load resistance to an arbitrary admittance at a single frequency. Starting from a resistance, RL, the network generates an admittance via shunt C – series L and shunt L – series C ladder networks.

Note For certain desired admittances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Only admittances in one region (hashed in the figure shown here) of the Smith chart can be generated with these networks, but the next schematic will generate impedances outside this region.



Main Schematic Settings

Desired admittance, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated admittances versus frequency, on a Smith chart

- Reflection coefficient (dB) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Ydesired1

Data Display Name

Ydesired1.dds

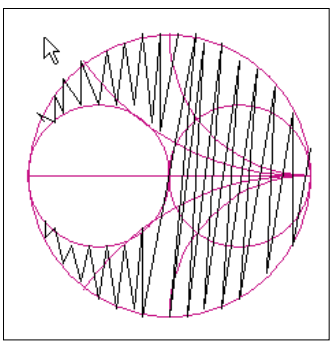
Lumped 2-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L for Desired Y

Description

This schematic synthesizes two different networks that convert a load resistance to an arbitrary admittance at a single frequency. Starting from a resistance, RL, the network generates an impedance via shunt L – series C and shunt C – series L ladder networks.

Note For certain desired admittances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Only admittances in one region (hashed in the figure shown here) of the Smith chart can be generated with these networks, but the previous schematic will generate impedances outside this region.



Main Schematic Settings

Desired impedance, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated admittances versus frequency, on a Smith chart

- Reflection coefficient (dB) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Ydesired2

Data Display Name

Ydesired2.dds

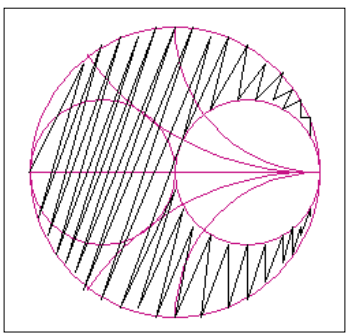
Lumped 2-Element Z-Y Matching Networks > Rload, Shunt C/L, Series C/L to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of two networks in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via shunt C – series L and shunt L - series C ladder networks.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

The impedance of the equivalent circuit must be in one region of the Smith chart, which is shown on the schematic and in the figure shown here. If the impedance of the device's equivalent circuit is outside the hashed region, then use the next schematic to perform the transformation.



Main Schematic Settings

Device equivalent circuit (*Series R-C* or *Series R-L*) component values, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart
- Reflection coefficient (dB and on a Smith chart) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Zmatch1

Data Display Name

Zmatch1.dds

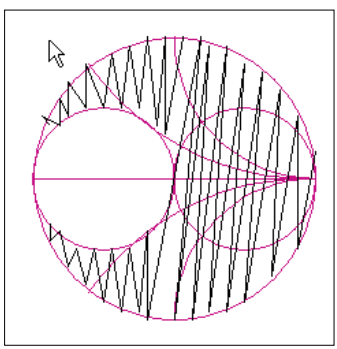
Lumped 2-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of two networks in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via series C – shunt L and series L - shunt C ladder networks.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

The impedance of the equivalent circuit must be in one region of the Smith chart, which is shown on the schematic and in the figure shown here. If the impedance of the device's equivalent circuit is outside the hashed region, then use the previous schematic to perform the transformation.



Main Schematic Settings

Device equivalent circuit (*Series R-C* or *Series R-L*) component values, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart
- Reflection coefficient (dB and on a Smith chart) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Zmatch2

Data Display Name

Zmatch2.dds

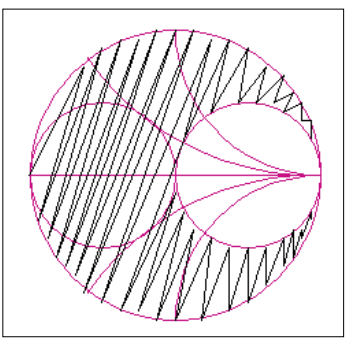
Lumped 2-Element Z-Y Matching Networks > Rload, Shunt C/L, Series C/L to Match Shunt R-C or R-L Device

Description

Given a shunt R-C equivalent input or output circuit of a device, this schematic computes component values of two networks to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via shunt C – series L and shunt L - series C ladder networks.

Note For certain desired admittances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

The admittance of the equivalent circuit must be in one region of the Smith chart, which is shown on the schematic and in the figure shown here. If the admittance of the device's equivalent circuit is outside the hashed region, then use the next schematic to perform the transformation.



Main Schematic Settings

Device equivalent circuit (*Shunt R-C* or *Shunt R-L*) component values, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated impedances versus frequency, on a Smith chart

- Reflection coefficient (dB and on a Smith chart) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Ymatch1

Data Display Name

Ymatch1.dds

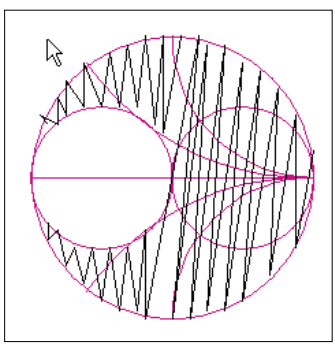
Lumped 2-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L to Match Shunt R-C or R-L Device

Description

Given a shunt R-C equivalent input or output circuit of a device, this schematic computes component values of two networks in order to conjugately match the device to an output resistance. (The shunt R-C network can be converted to a shunt R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via series C – shunt L and series L - shunt C ladder networks.

Note For certain desired admittances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

The admittance of the equivalent circuit must be in one region of the Smith chart, which is shown on the schematic and in the figure shown here. If the admittance of the device's equivalent circuit is outside the hashed region, then use the previous schematic to perform the transformation.



Main Schematic Settings

Device equivalent circuit (*Shunt R-C* or *Shunt R-L*) component values, load resistance, frequency of match

Data Display Outputs

- L and C component values of the two networks
- Generated admittances versus frequency, on a Smith chart
- Reflection coefficient (dB and on a Smith chart) presented to the external load resistor, versus frequency, for both networks. This is a perfect match at the matching frequency, but not at other frequencies.

Schematic Name

Ymatch2

Data Display Name

Ymatch2.dds

Chapter 8: Lumped Multi-Element Z-Y Matching Networks

The templates in the Lumped Multi-Element Z-Y Matching Networks are for synthesizing an arbitrary impedance or admittance, or for matching to a device's equivalent circuit that is modeled as an R-C or R-L network. The matching networks use only lumped, ideal elements, and the impedance match is only for a single frequency (although in all cases, Q of the network may be specified), so the capabilities of these templates are rather limited. You might wish to use E-Syn or the Passive Circuit DesignGuide for impedance matching.

Lumped Multi-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L, Series L/C for Desired Z

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via a series C – shunt C – series L ladder network.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Impedances in one region of the Smith chart cannot be generated with these networks, but the next schematic will generate impedances in this forbidden region, which is shown on the schematic.

Main Schematic Settings

Desired impedance, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Generated impedance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired impedance

Schematic Name

Zdesired1M

Data Display Name

Zdesired1M.dds

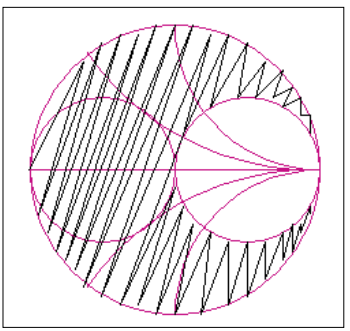
Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Series C for Desired Z

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via a shunt C – series L – series C ladder network.

Note For certain desired impedances, the calculated inductor value will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

Only impedances in one region (hashed in the figure shown here) of the Smith chart can be generated with this network, and this forbidden region is shown on the schematic.



Main Schematic Settings

Desired impedance, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Generated impedance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired impedance

Schematic Name

Zdesired2M

Data Display Name

Zdesired2M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Series L, Shunt C, Series L/C for Desired Z

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary impedance at a single frequency. Starting from a resistance, RL, the network generates an impedance via a series L – shunt C – series L ladder network.

Note For certain desired impedances, one of the calculated inductor values will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

One limitation of this network is that it cannot generate impedances such that *real(Zdesired)*(1+Q**2)/RL <1*.

Main Schematic Settings

Desired impedance, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Generated impedance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired impedance

Schematic Name

Zdesired3M

Data Display Name

Zdesired3M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Shunt C for Desired Y

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary admittance at a single frequency. Starting from a resistance, RL, the network generates an admittance via a shunt C – series L – shunt C ladder network.

If

*(1/real(Ydesired)/RL is > (Q**2 +1)*

this network cannot be used.

Main Schematic Settings

Desired admittance, load resistance, frequency of match, Q of admittance transformation network

Data Display Outputs

- L and C component values of the network
- Generated admittance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired admittance

Schematic Name

Ydesired1M

Data Display Name

Ydesired1M.dds

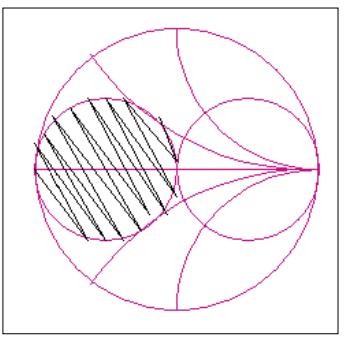
Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Series C, Shunt L/C for Desired Y

Description

This schematic synthesizes a network that converts a load resistance to an arbitrary admittance at a single frequency. Starting from a resistance, RL, the network generates an admittance via a shunt C – series L – series C - shunt L ladder network.

Note For certain desired admittances, one of the calculated inductor values will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

Only admittances in one region (hashed in the figure shown here) of the Smith chart can be generated with this network.



Main Schematic Settings

Desired admittance, load resistance, frequency of match, Q of admittance transformation network

Data Display Outputs

- L and C component values of the network
- Generated admittance versus frequency, on a Smith chart
- Reflection coefficient versus frequency (dB) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the complex conjugate of the desired admittance

Schematic Name

Ydesired2M

Data Display Name

Ydesired2M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Series C/L, Shunt C/L, Series L/C to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of a network in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via a series C – shunt C – series L ladder network.

Note For certain desired impedances, some of the calculated component values will be negative. These negative components must be replaced with positive ones. For example, negative inductors must be replaced by positive capacitors and negative capacitors must be replaced by positive inductors. The correct component values when such replacements are necessary are calculated on the data display.

Main Schematic Settings

Device equivalent circuit (Series R-C or Series R-L) component values, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Zmatch1M

Data Display Name

Zmatch1M.dds

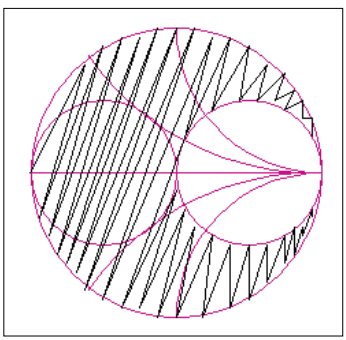
Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L/C, Series C to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of a network in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via a shunt C – series L – series C ladder network.

Note For certain desired impedances, the calculated inductor value will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

Only impedances in one region (hashed in the figure shown here) of the Smith chart can be generated with this network (the resistance of the device must be less than the external load resistance).



Main Schematic Settings

Device equivalent circuit (Series R-C or Series R-L) component values, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network

- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Zmatch2M

Data Display Name

Zmatch2M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Series L, Shunt C, Series L/C to Match Series R-C or R-L Device

Description

Given a series R-C equivalent input or output circuit of a device, this schematic computes component values of a network in order to conjugately match the device to an output resistance. (The series R-C network can be converted to a series R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via a series L – shunt C – series L ladder network.

Note For certain desired impedances, one of the calculated inductor values will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

One limitation of this network is that it cannot perform the impedance transformation if *Rdev*(1+Q**2)/RL <1*, where *Rdev* is the device's resistance, and *RL* is the external load resistance.

Main Schematic Settings

Device equivalent circuit (Series R-C or Series R-L) component values, load resistance, frequency of match, Q of impedance transformation network

Data Display Outputs

- L and C component values of the network
- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Zmatch3M

Data Display Name

Zmatch3M.dds

Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Shunt C Shunt R-C or R-L Device

Description

Given a shunt R-C equivalent input or output circuit of a device, this schematic computes component values of two networks to conjugately match the device to an output resistance. (The shunt R-C network can be converted to a shunt R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the network generates the complex conjugate admittance via a shunt C – series L – shunt C ladder network. If *Rdev / RL is > (Q**2 +1*), where *Rdev* is the device's resistance and *RL* is the external load resistance, then this network cannot be used.

Main Schematic Settings

Device equivalent circuit (Shunt R-C or Shunt R-L) component values, load resistance, frequency of match, Q of admittance transformation network

Data Display Outputs

- L and C component values of the network
- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Ymatch1M

Data Display Name

Ymatch1M.dds

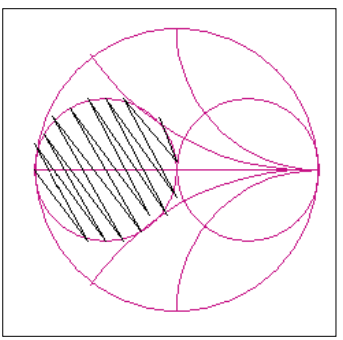
Lumped Multi-Element Z-Y Matching Networks > Rload, Shunt C, Series L, Series C, Shunt L/C to Match Shunt R-C or R-L Device

Description

Given a shunt R-C equivalent input or output circuit of a device, this schematic computes component values of a network in order to conjugately match the device to an output resistance. (The shunt R-C network can be converted to a shunt R-L network if the capacitance is set to a negative value, with formula given on the schematic.) Starting from a resistance, RL, the networks generate the complex conjugate impedance via a shunt C – series L – series C - shunt L ladder network.

Note For certain desired admittances, one of the calculated inductor values will be negative. This negative inductor must be replaced with a capacitor. The correct capacitor value when such a replacement is necessary is calculated on the data display.

Admittances in only one region (hashed in the figure shown here) of the Smith chart can be generated with this network. Rdev must be < RL, where Rdev is the device's resistance and RL is the external load resistance.



Main Schematic Settings

Device equivalent circuit (Shunt R-C or Shunt R-L) component values, load resistance, frequency of match, Q of admittance transformation network

Data Display Outputs

- L and C component values of the network

- Reflection coefficient versus frequency (dB and on a Smith chart) looking back into the network from the output resistor, RL, when the other end of the network is terminated in the device's equivalent circuit

Schematic Name

Ymatch2M

Data Display Name

Ymatch2M.dds

Index