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CS4290

Cache Coherence Experiments

Procedure

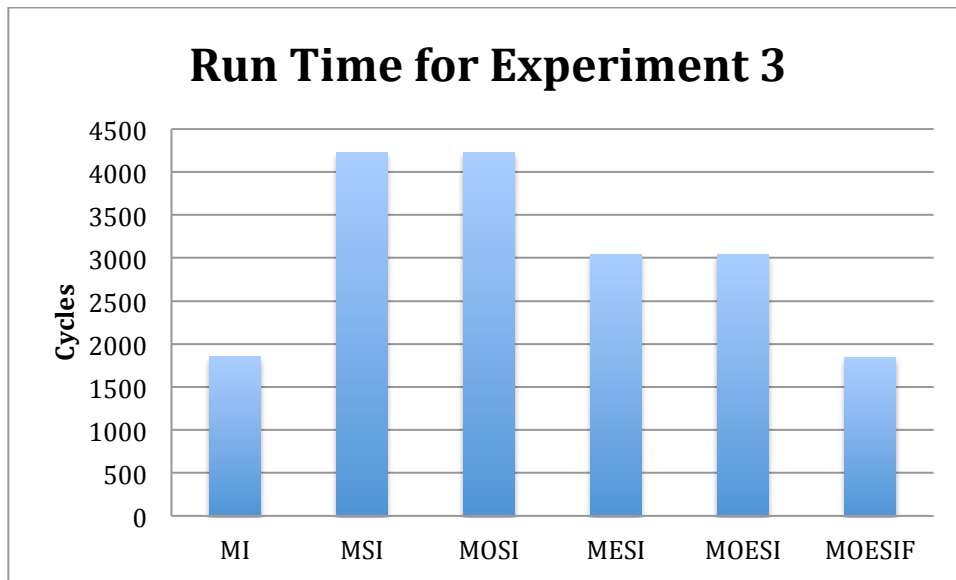
The first thing I looked at when I was going through each experiment is the traces for each processor. I looked at each trace briefly and tried to find patterns in the traces like a lot of memory accesses of one address over several processors or several processors trying to write to an address. These patterns gave me some idea on which protocol might be the best one to use.

The next thing I did was ran the experiment using all of the protocols and looked at the statistics outputted for each protocol. I looked at the run-time cycles and picked the protocol that gave the shortest run-time as the best protocol. If all of the protocols gave similar run-times I looked at the number of cache misses. Minimizing this will minimize the calls to memory. Next, I would look at cache-to-cache transfers. Maximizing this will mean fewer calls to memory. Finally, if for some reason those are all similar, I looked at the silent-upgrades because maximizing these will minimize the data bus use.

Experiment 3

The first thing I noticed with the traces for experiment three is that the processors make use of different addresses except for the first few accesses. Each processor does one read on the address and then multiple writes on the same address. This is not good for the MSI protocol because the shared state doesn't have intervention so every read will have to go to memory. It isn't good for the MOSI for the same reason since the O state is for dirty data and we can only get there from the modified state. This works with the MESI and MOESI state because the each processor is accessing different data later on in the traces so they may stay in the exclusive state. The MOESIF will also work because of the exclusive state. I decided to choose the MOESIF protocol because it uses the least number of cycles, the least number of cache misses, the most number of silent upgrades, and the most cache-to-cache transfers.

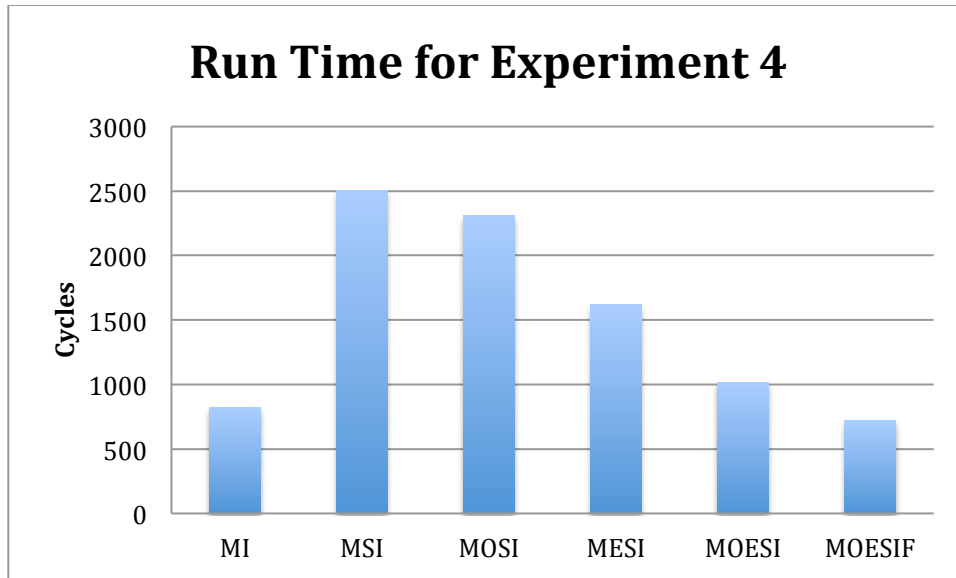
| Experiment 3 | Run Time | \$-Misses | \$-Accesses | Silent Upgrades | \$-\$ Transfers |
|--------------|----------|-----------|-------------|-----------------|-----------------|
| MI | 1859 | 49 | 200 | 0 | 36 |
| MSI | 4227 | 56 | 200 | 0 | 20 |
| MOSI | 4227 | 56 | 200 | 0 | 20 |
| MESI | 3039 | 48 | 200 | 8 | 23 |
| MOESI | 3039 | 48 | 200 | 8 | 23 |
| MOESIF | 1848 | 48 | 200 | 8 | 35 |



Experiment 4

Looking at these traces, it looks like a producer/consumer setup where P0 is the producer and the rest of the processors are the consumers. In this case, since only one of the processors is writing to the data and the others are just reading the data, I think any protocol with the Owner state may suffice. From the execution time graphs, I choose MOESIF as the protocol to use because it uses far less cycles than the other protocols. It also has more cache-to-cache transfers so there are less memory accesses.

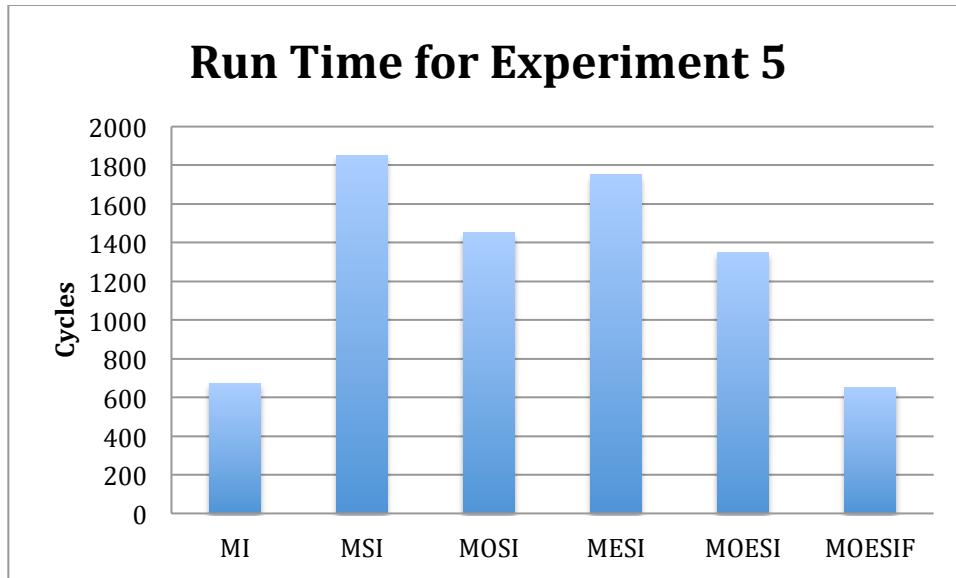
| Experiment4 | Run Time | \$-Misses | \$-Accesses | Silent Upgrades | \$-\$ Transfers |
|-------------|----------|-----------|-------------|-----------------|-----------------|
| MI | 822 | 29 | 60 | 0 | 24 |
| MSI | 2508 | 27 | 60 | 0 | 5 |
| MOSI | 2308 | 27 | 60 | 0 | 7 |
| MESI | 1618 | 19 | 60 | 3 | 5 |
| MOESI | 1018 | 19 | 60 | 3 | 11 |
| MOESIF | 718 | 19 | 60 | 3 | 14 |



Experiment 5

This trace has processors that all access mostly the same data and reads and write interspersed. Because of this, I would chose a protocol with the Owner state because dirty data is allowed along with multiple processors having the data in the shared state. The exclusive state protocols don't work as well because the data is going to be dirty from the few writes that are intermixed with the reads. The execution graph below shows that MOESIF is the best choice again because it uses the least number of cycles and has the most cache-to-cache transfers.

| Experiment 5 | Run Time | \$-Misses | \$-Accesses | Silent Upgrades | \$-\$ Transfers |
|--------------|----------|-----------|-------------|-----------------|-----------------|
| MI | 672 | 23 | 37 | 0 | 19 |
| MSI | 1850 | 21 | 37 | 0 | 5 |
| MOSI | 1450 | 21 | 37 | 0 | 9 |
| MESI | 1750 | 21 | 37 | 0 | 6 |
| MOESI | 1350 | 21 | 37 | 0 | 10 |
| MOESIF | 650 | 21 | 37 | 0 | 17 |



Experiment 7

This last trace has a lot of processors accessing only a few addresses. Most of the accesses are reads with a few writes placed in between. Because of the many reads, I would use MOESI. First, the cycle time for the MOESI and the MOESIF are the same and is the lowest run time in cycles of all the protocols. The MOESI and MOESIF all have the same statistics so I would choose MOESI because it is not as difficult to implement.

| Experiment 7 | Run Time | \$-Misses | \$-Accesses | Silent Upgrades | \$-\$ Transfers |
|--------------|-------------|-----------|-------------|-----------------|-----------------|
| MI | 3980 | 115 | 952 | 0 | 88 |
| MSI | 7157 | 79 | 952 | 0 | 17 |
| MOSI | 6057 | 79 | 952 | 0 | 28 |
| MESI | 4488 | 55 | 952 | 24 | 17 |
| MOESI | 3388 | 55 | 952 | 24 | 28 |
| MOESIF | 3388 | 55 | 952 | 24 | 28 |

Run Time for Experiment 7

