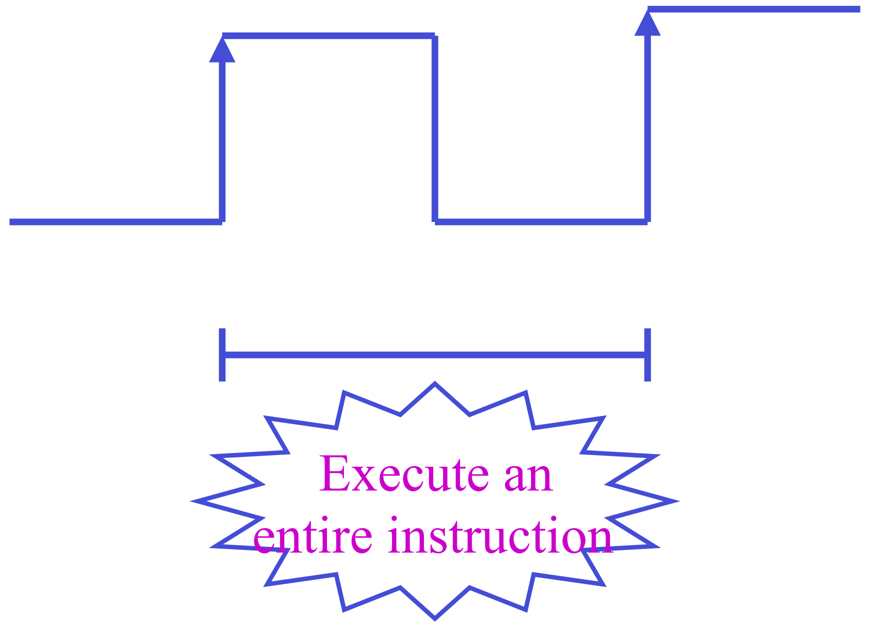
Single Cycle CPU

Jason Mars

The Big Picture: The Performance Perspective



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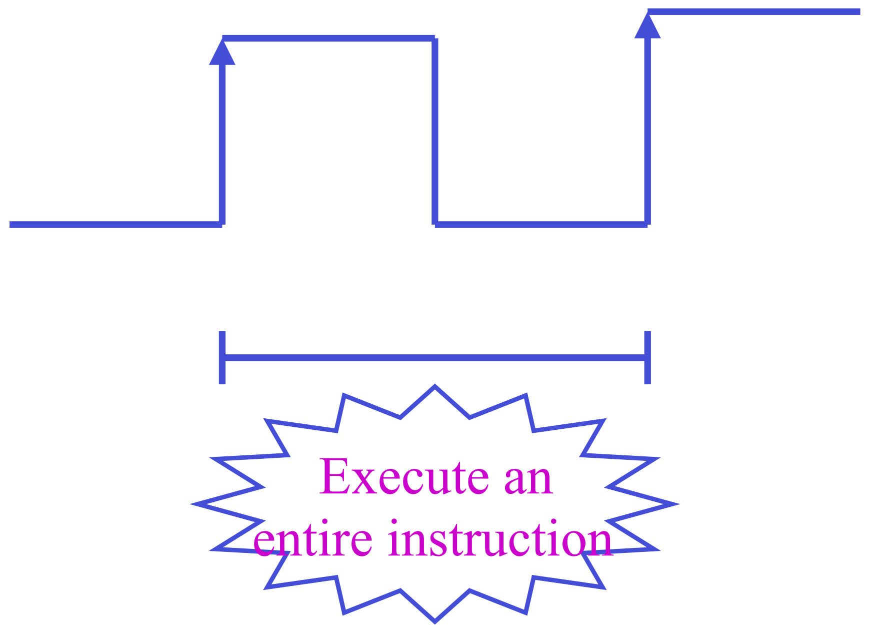
  - Clock cycles per instruction



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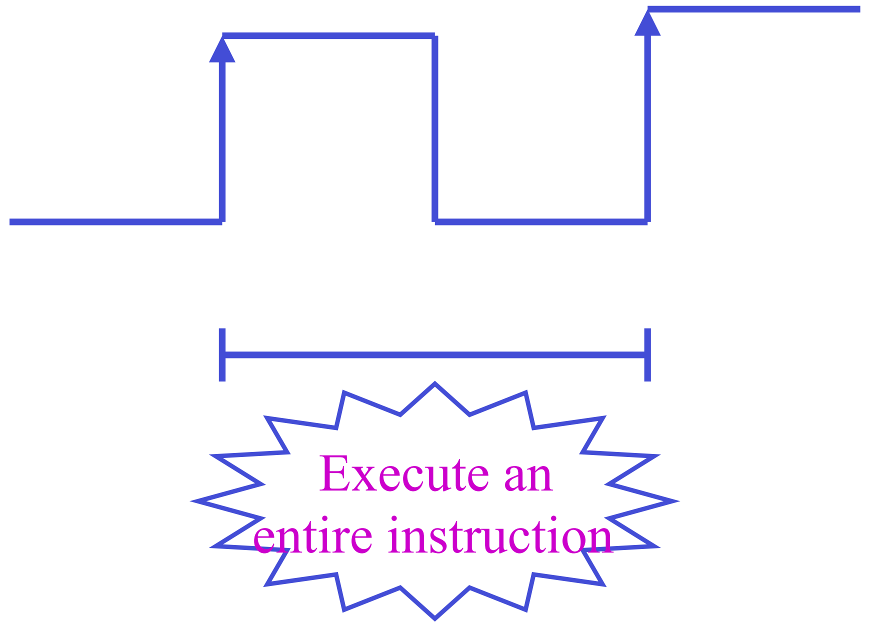

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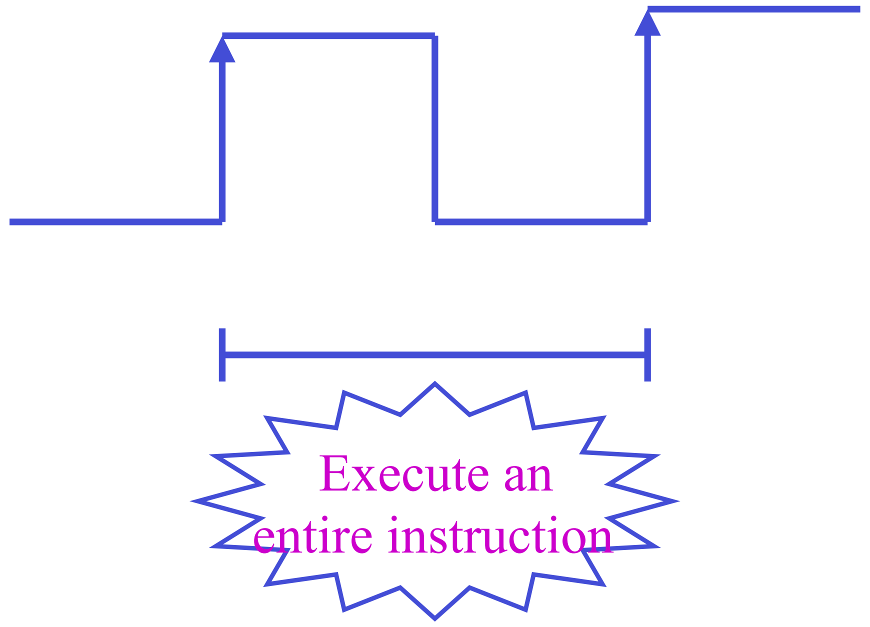
- ET = Insts * CPI * Cyc Time



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  - arithmetic-logical instructions: add, sub, and, or, slt
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    - use the instruction to decide exactly what to do

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- All instructions use the ALU after reading the registers
  - memory-reference? arithmetic? control flow?

Review: MIPS Instruction Formats

- All instructions 32-bits long
- 3 Formats:

R-Type

6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
opcode	rs	rt	rd	shift amount	funct

I-Type

6 bits	5 bits	5 bits	16 bits
opcode	rs	rt	immediate / offset

J-Type

6 bits	26 bits
opcode	target

The MIPS Subset

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- BRANCH:
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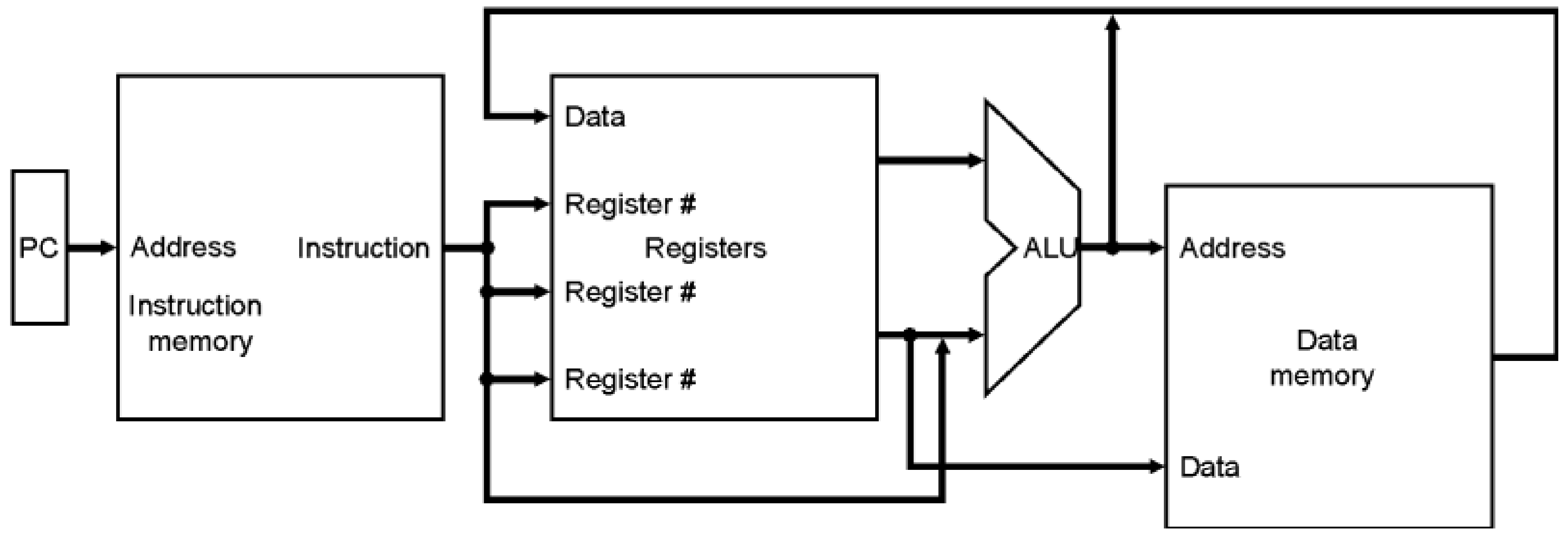
  program counter

Where We're Going...



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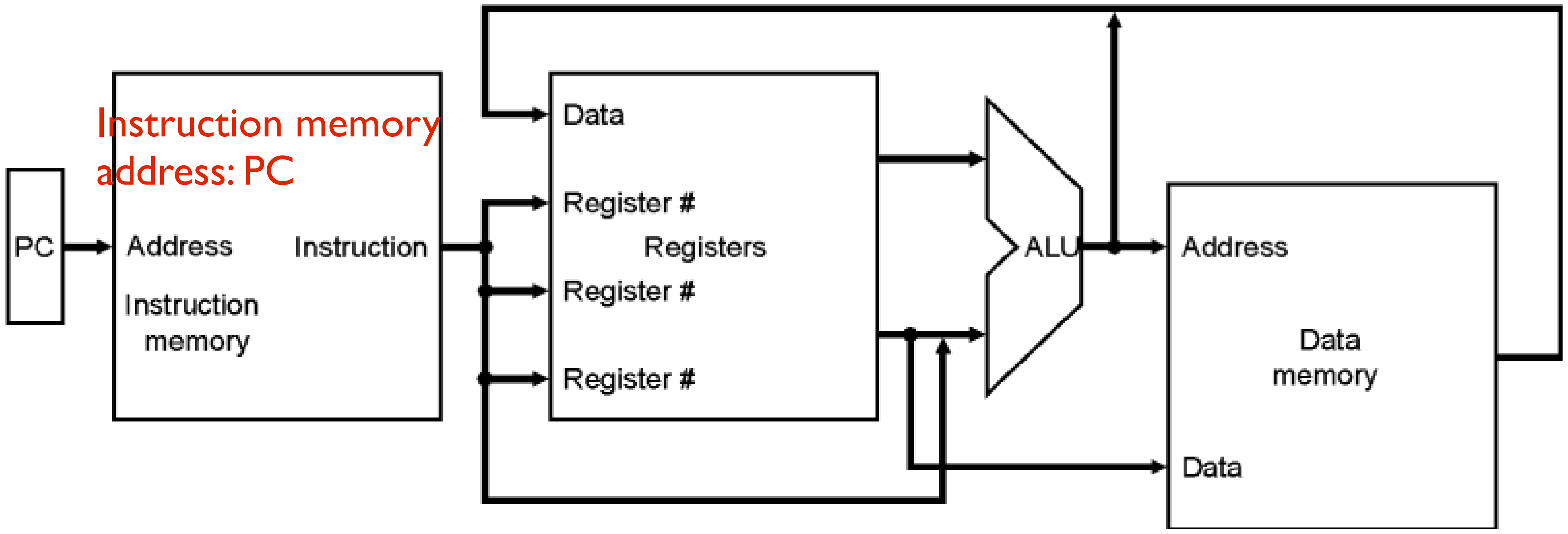

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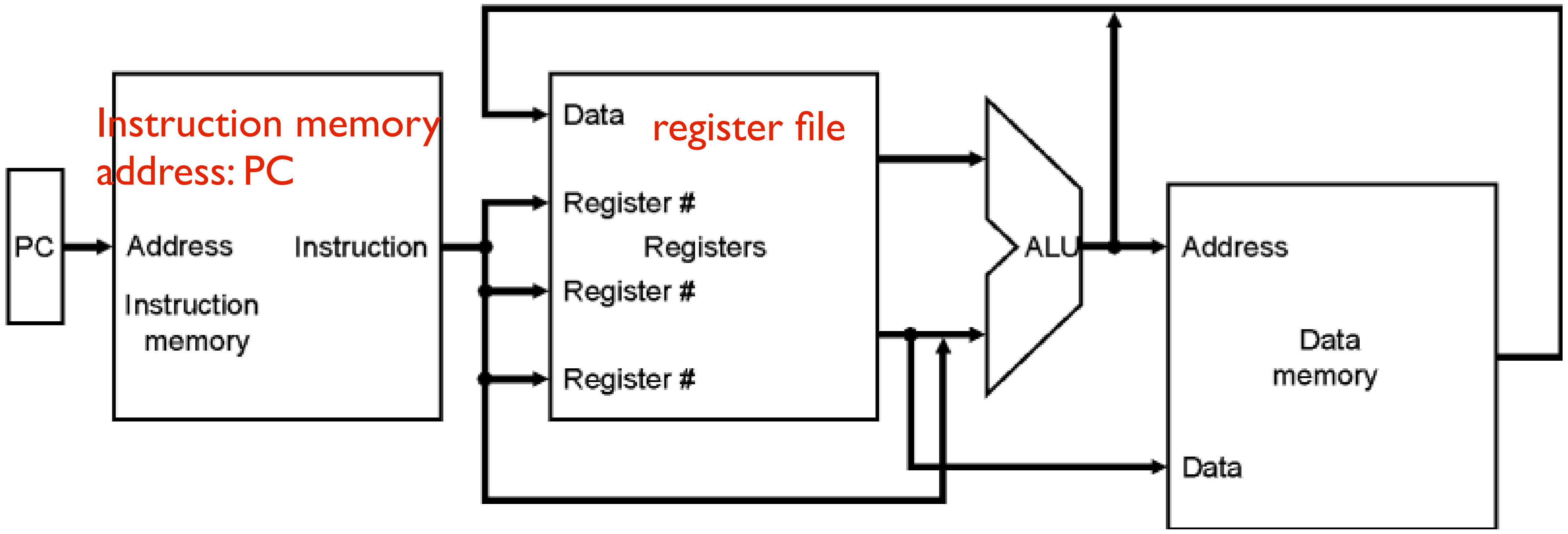

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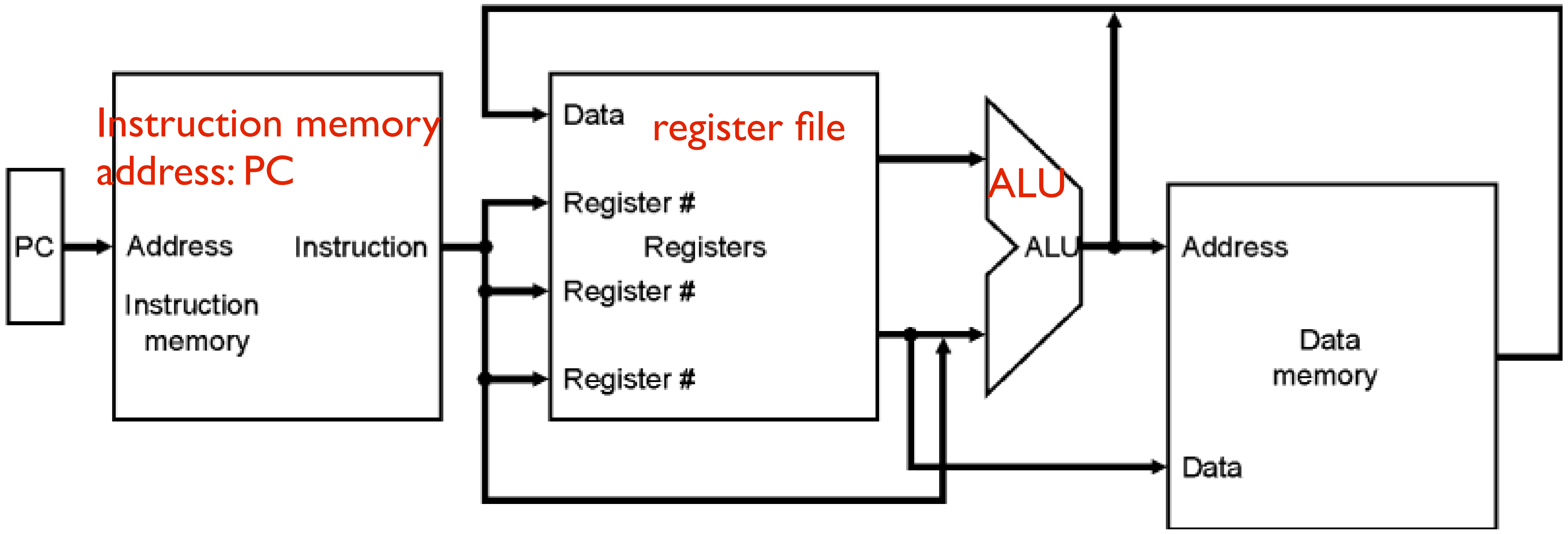

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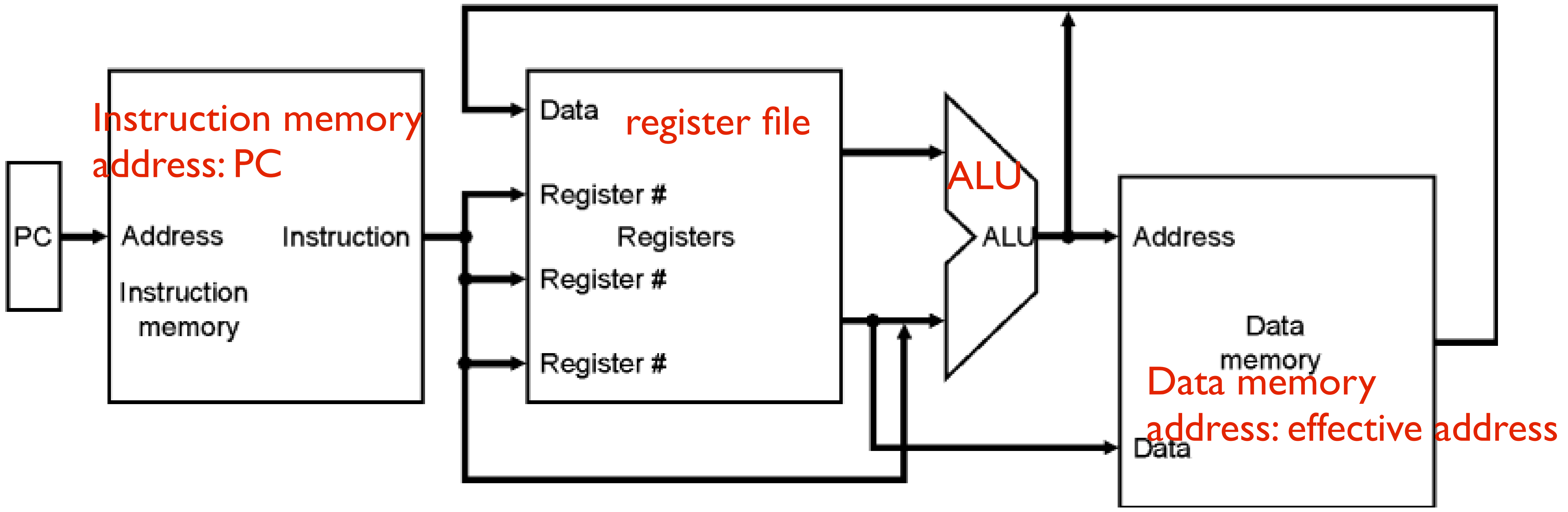

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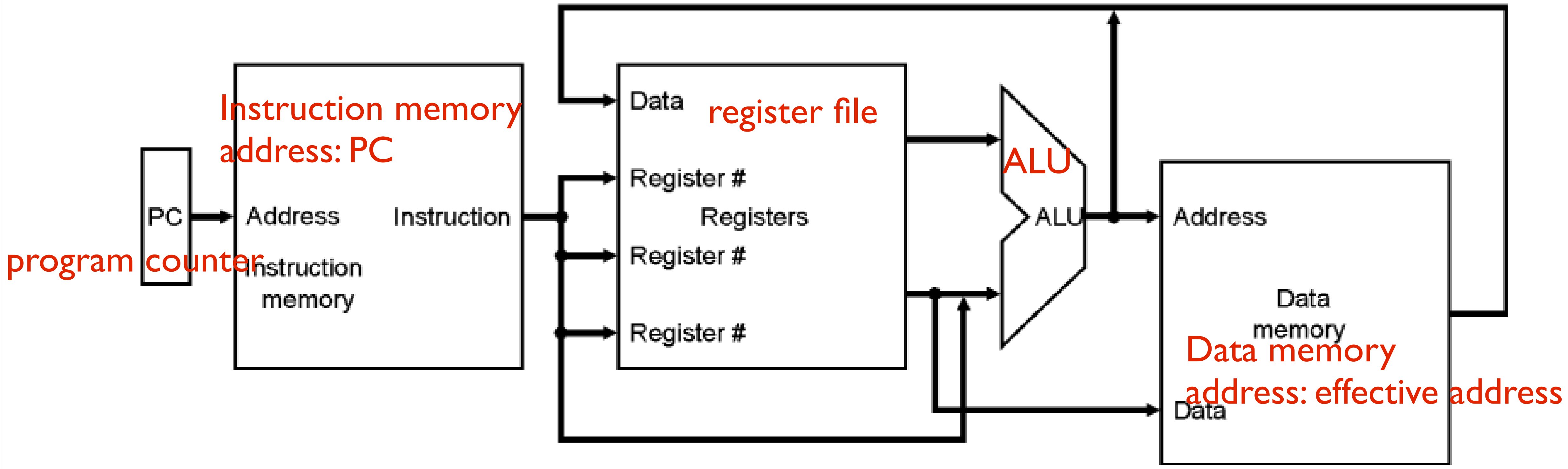

Review: Two Type of Logical Components

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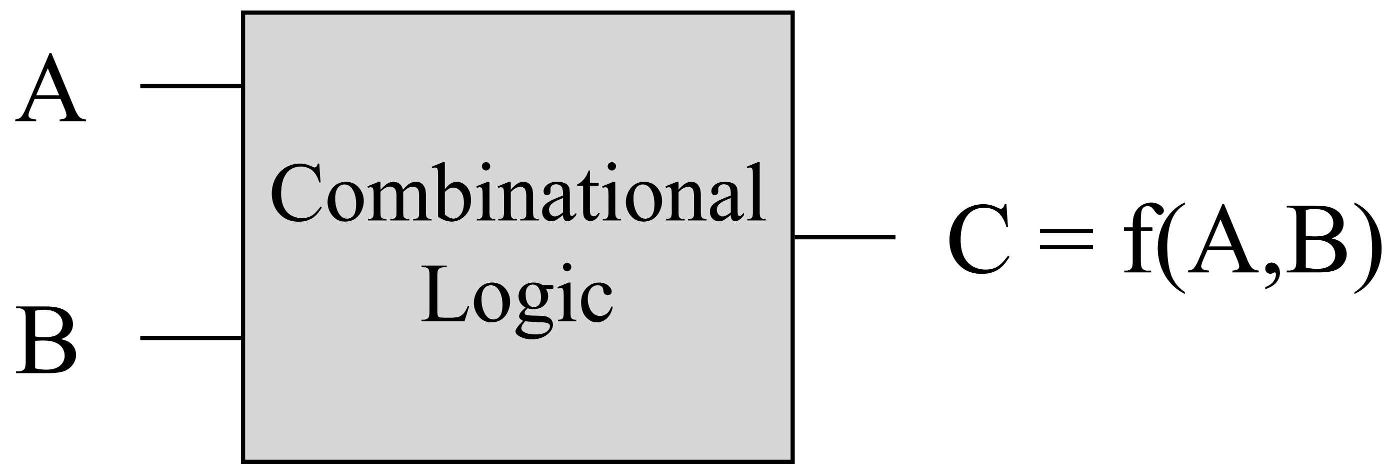

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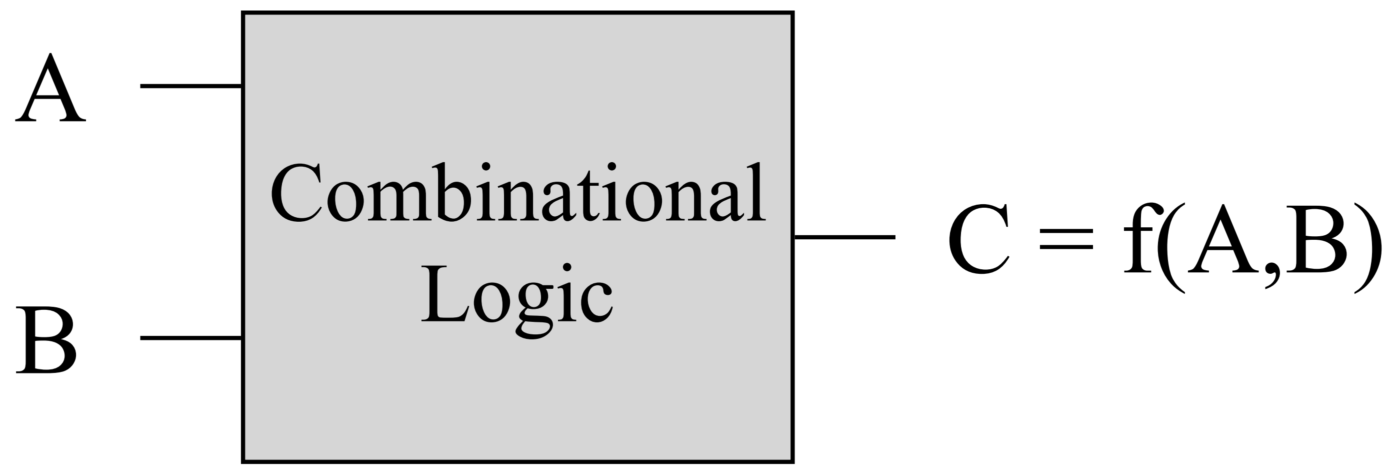
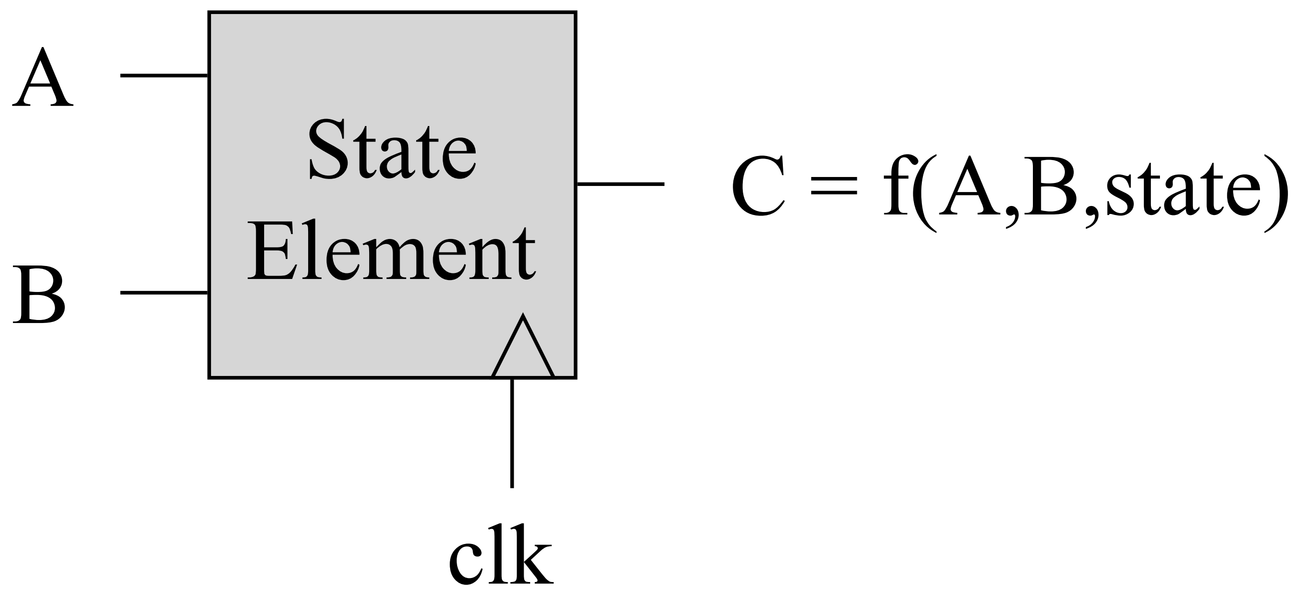
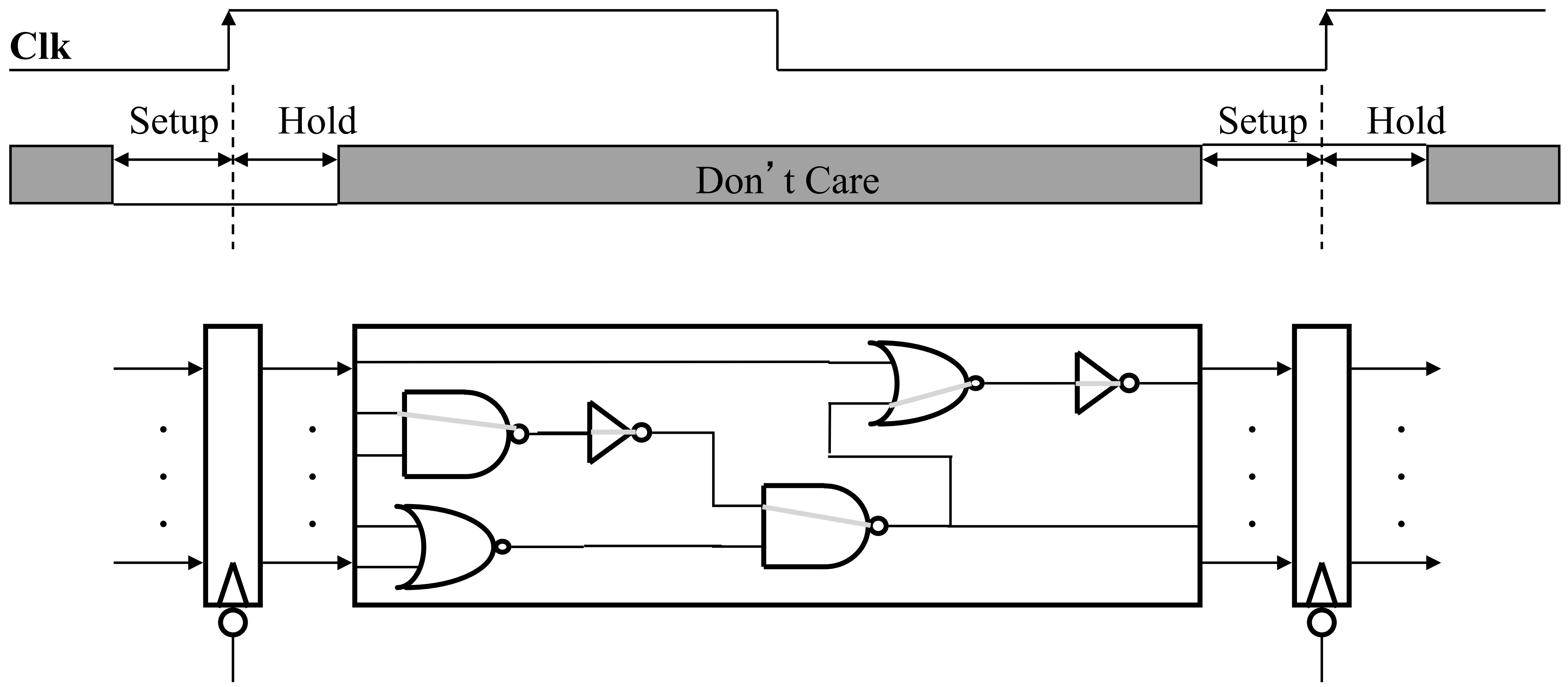




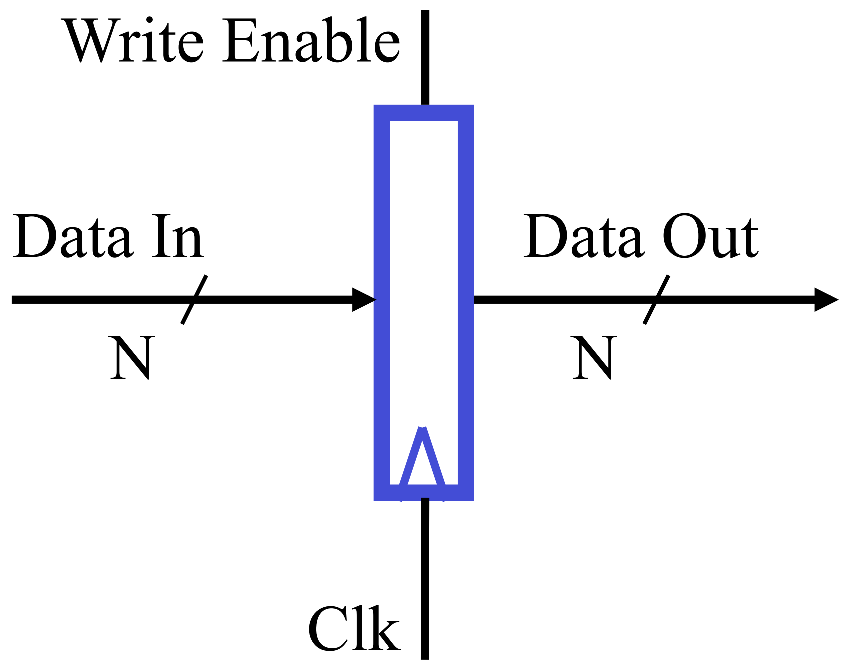
Clocking Methodology



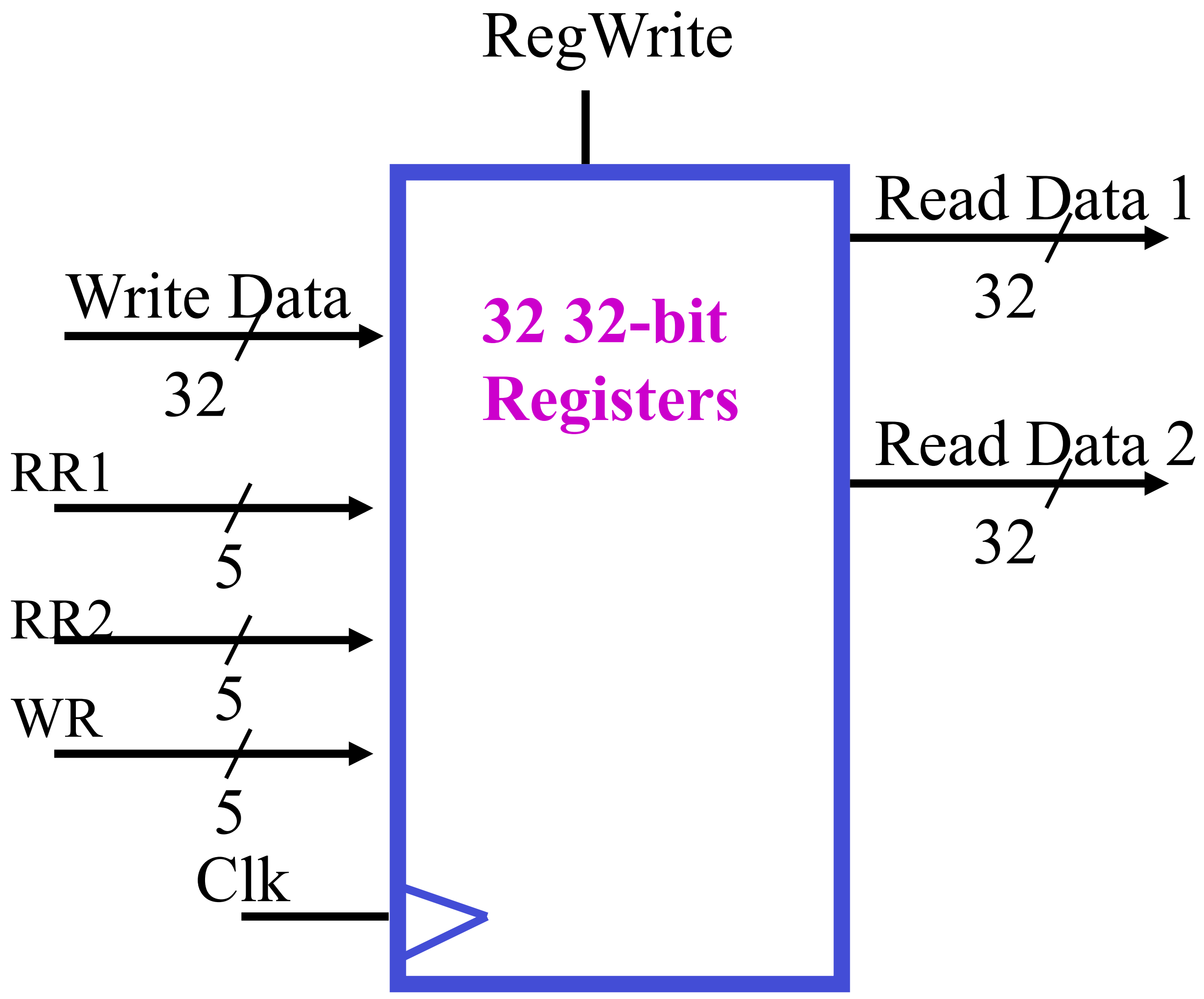
- All storage elements are clocked by the same clock edge

Storage Element: The Register

- Register
  - Similar to the D Flip Flop except
    - N-bit input and output
    - Write Enable input
- Write Enable:
  - 0: Data Out will not change
  - 1: Data Out will become Data In (on the clock edge)



Storage Element: Register File



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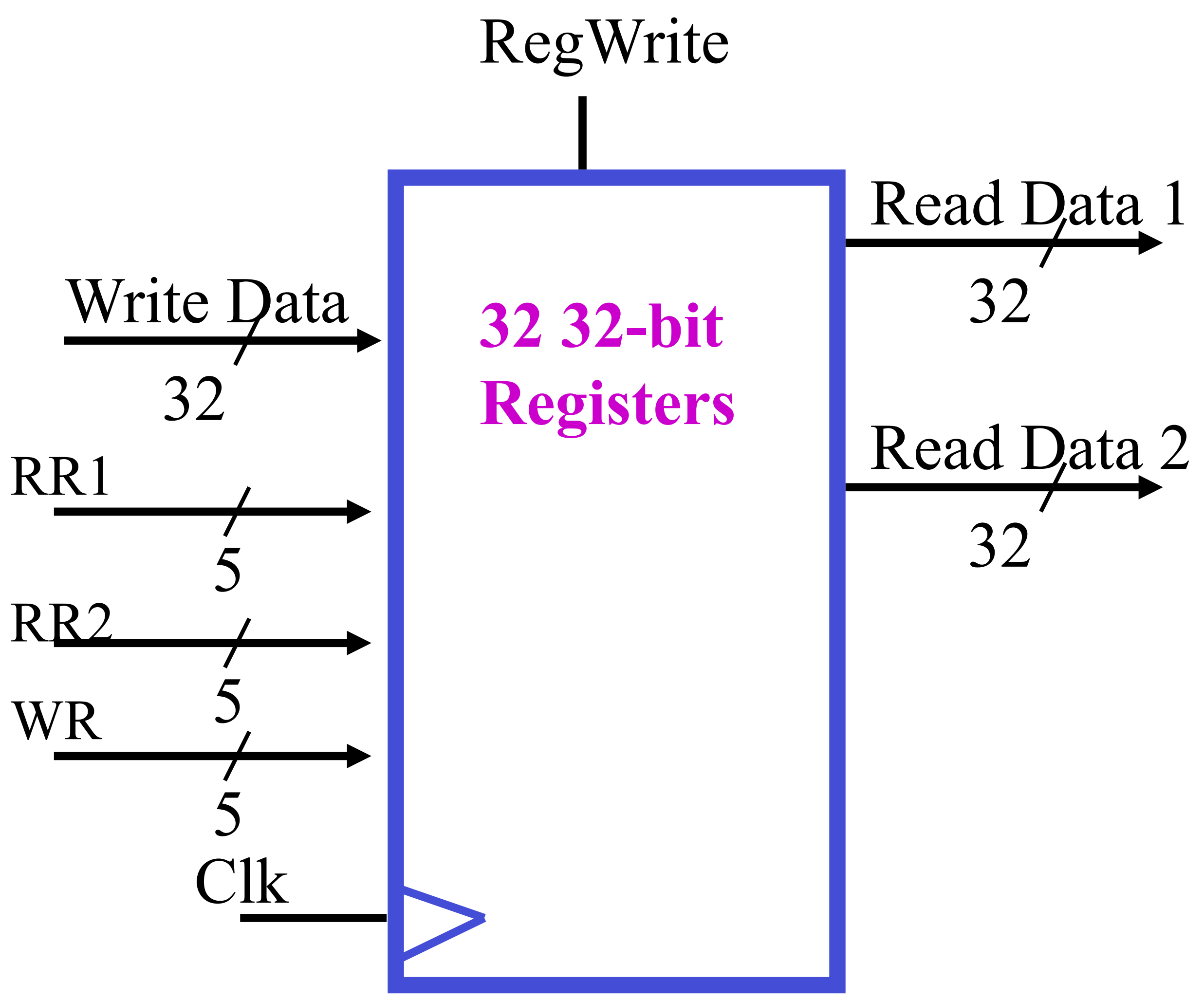
- Register File consists of (32) registers:



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- Register File consists of (32) registers:
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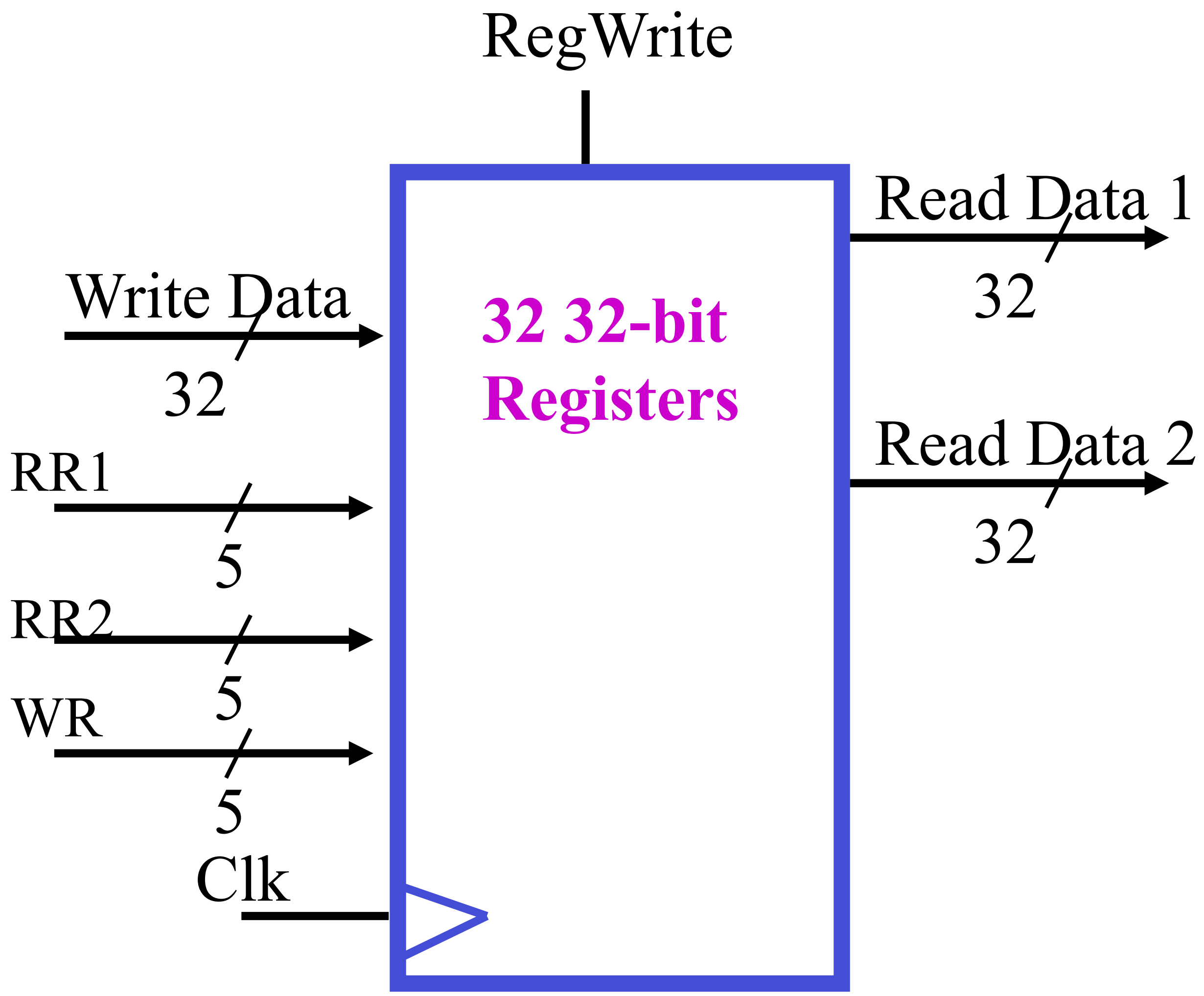

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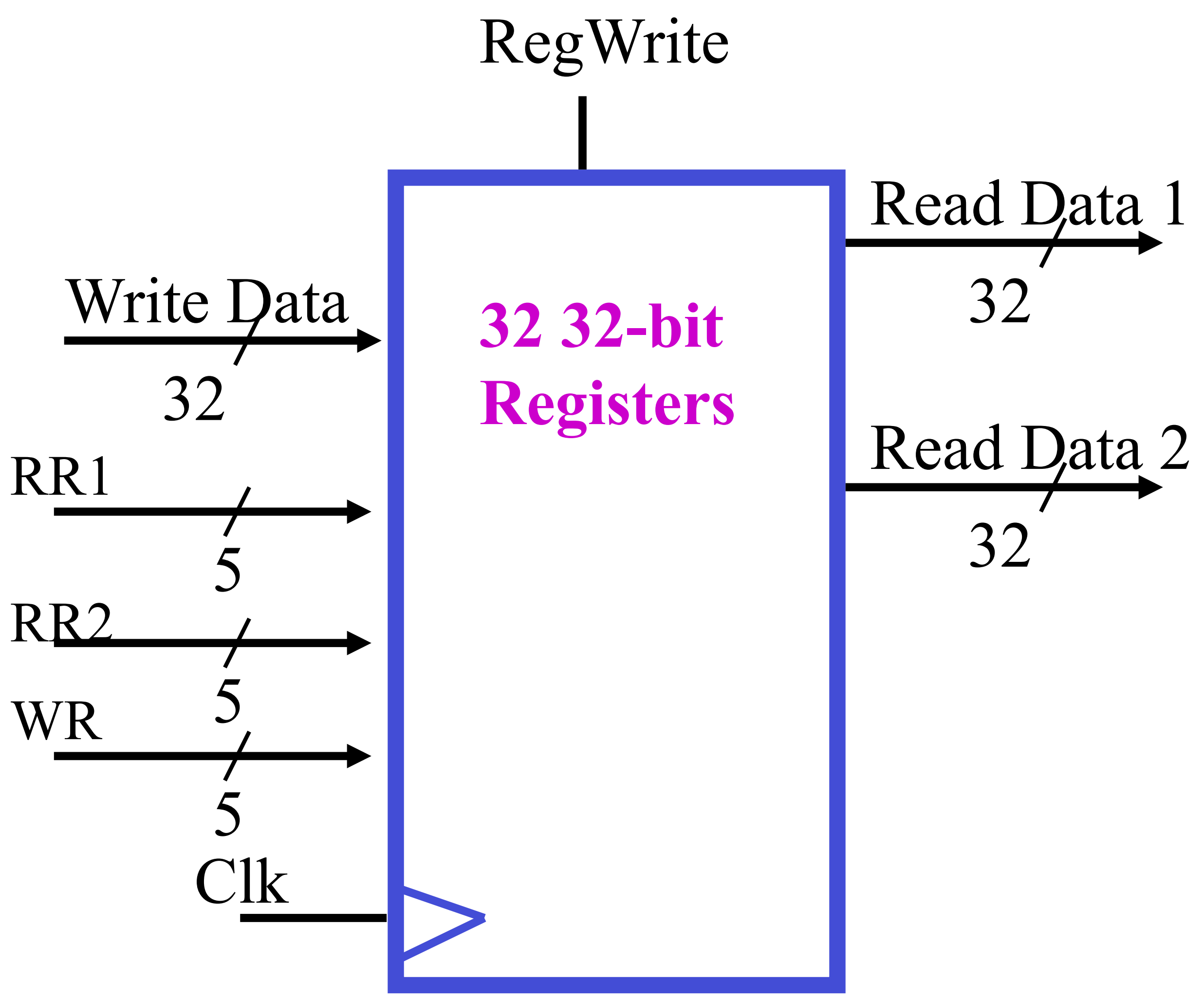

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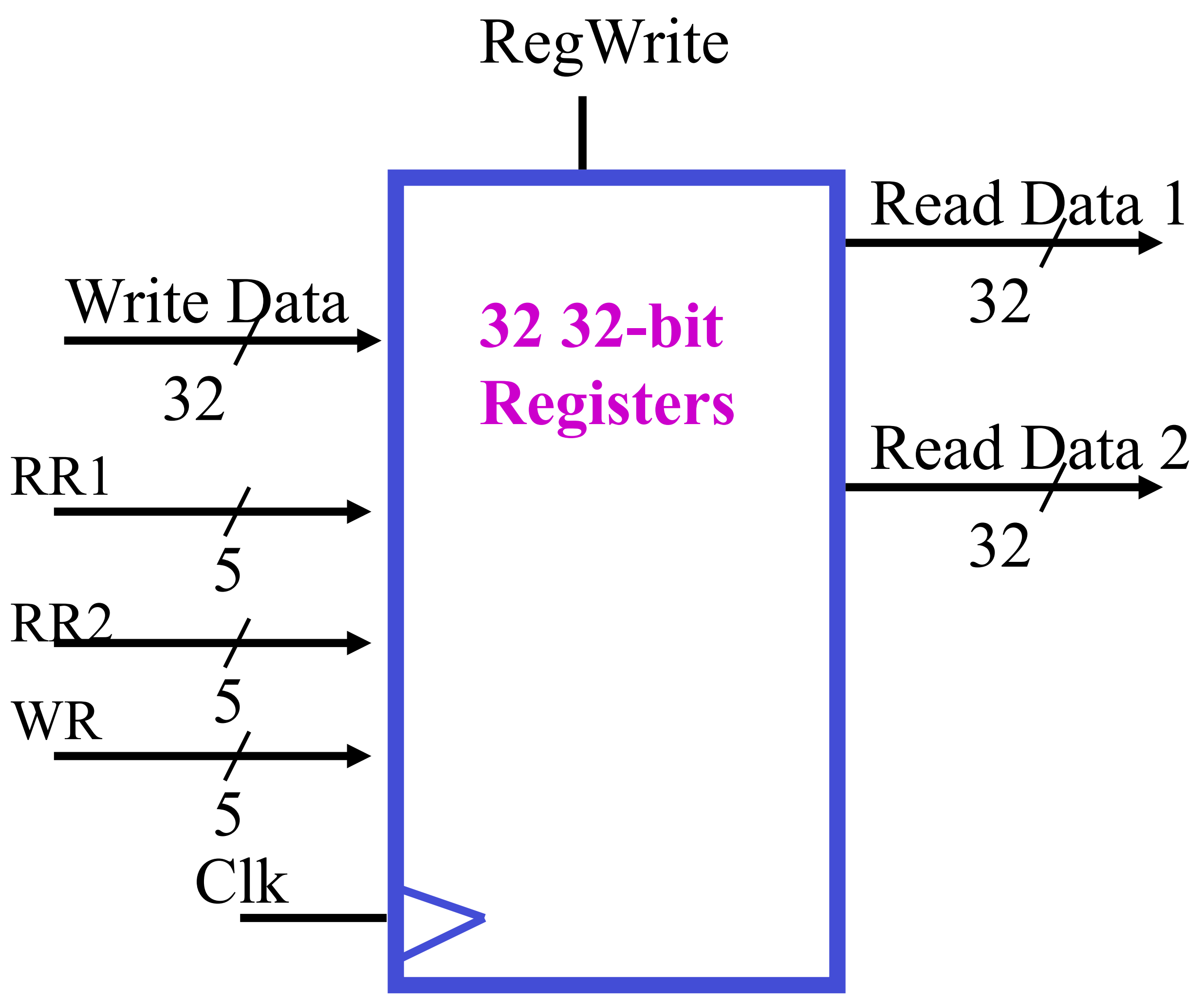

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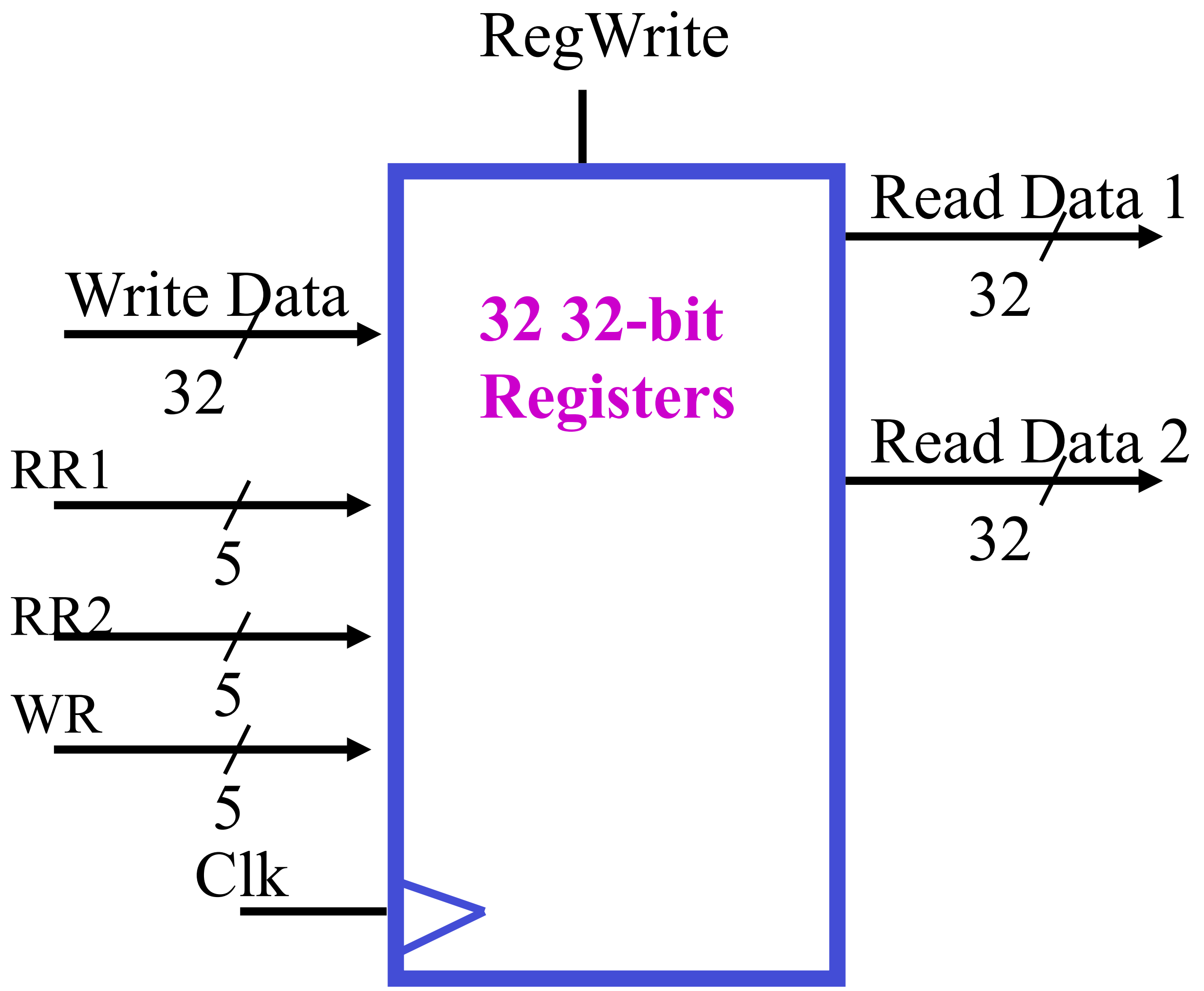

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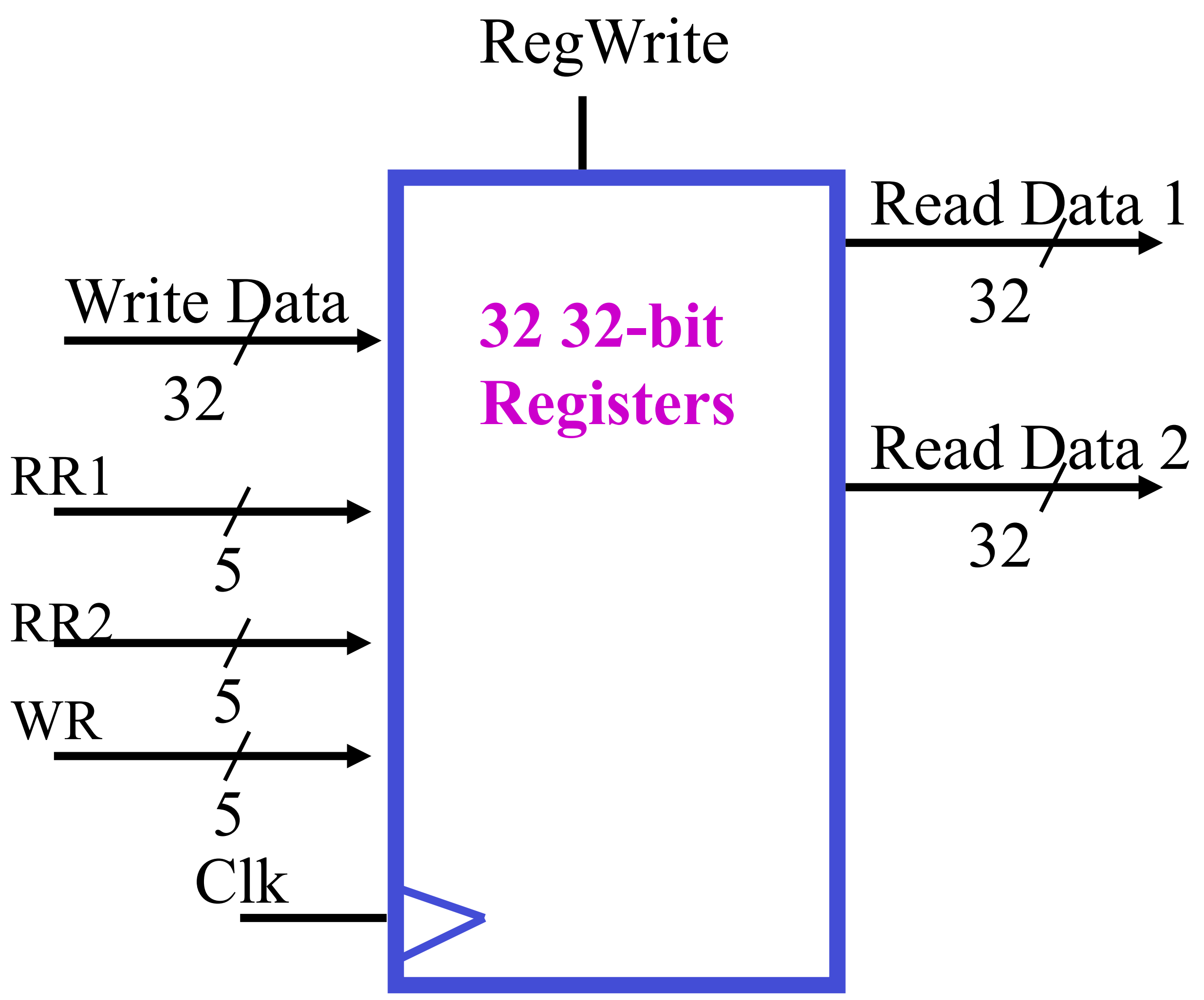

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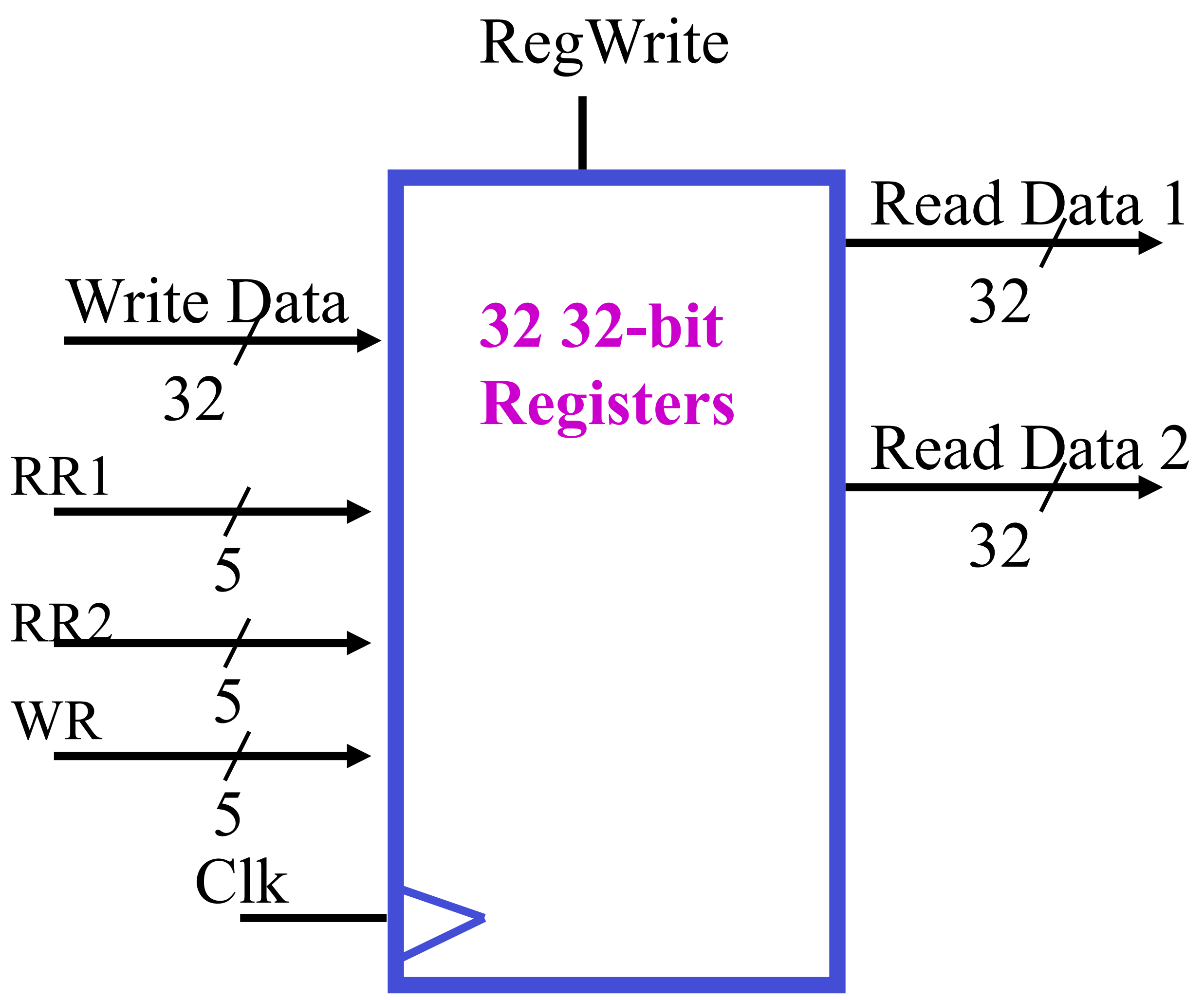

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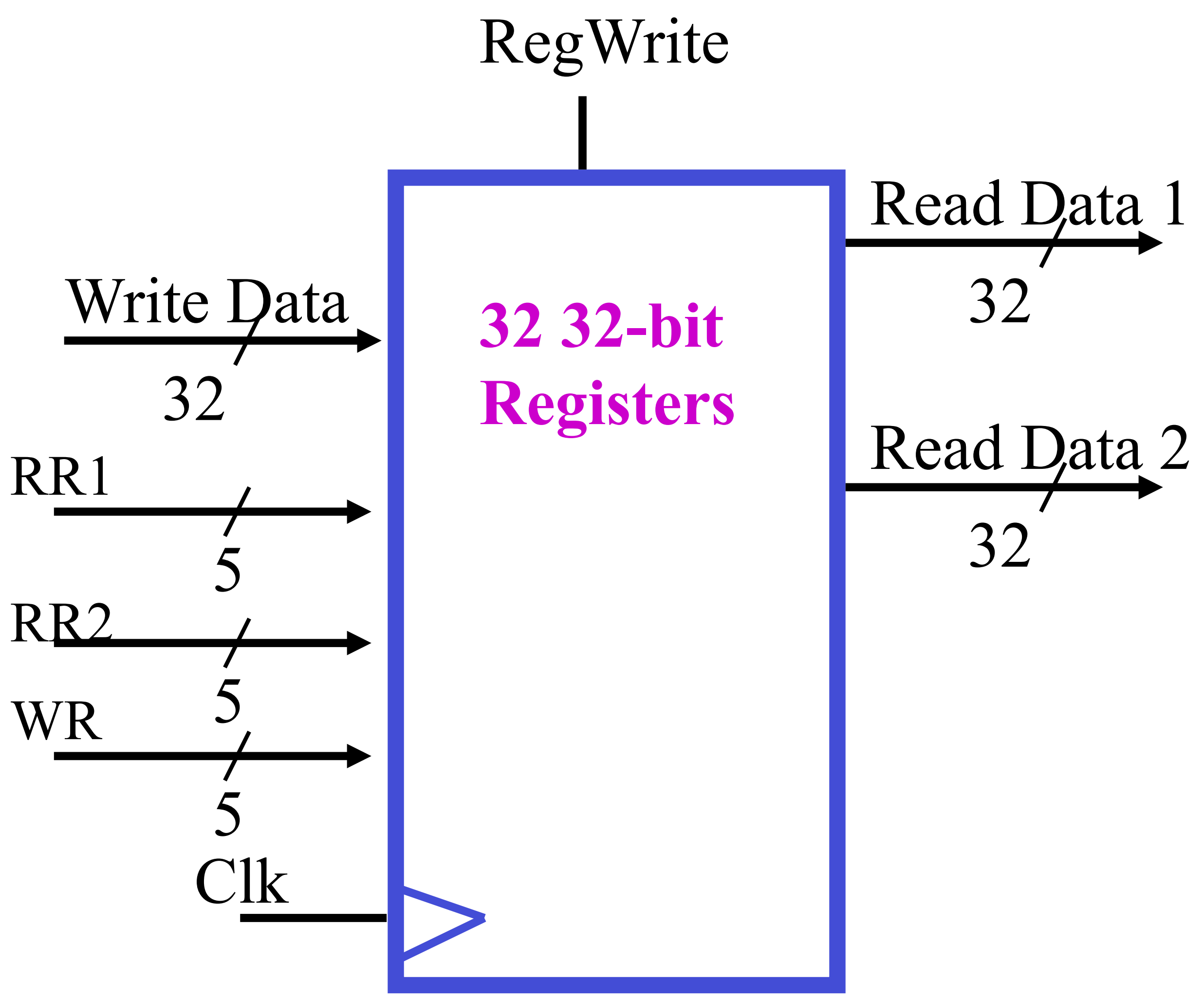

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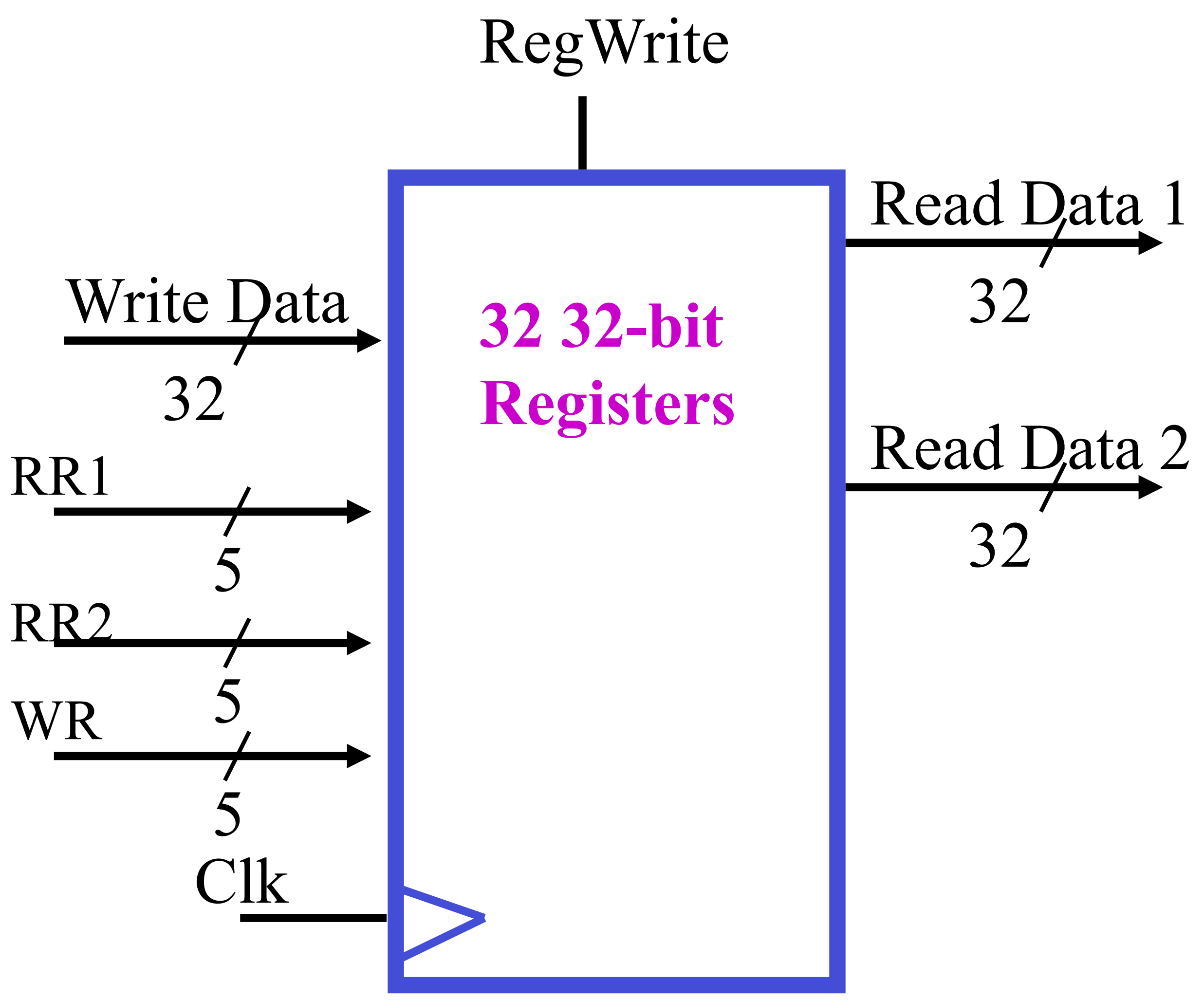
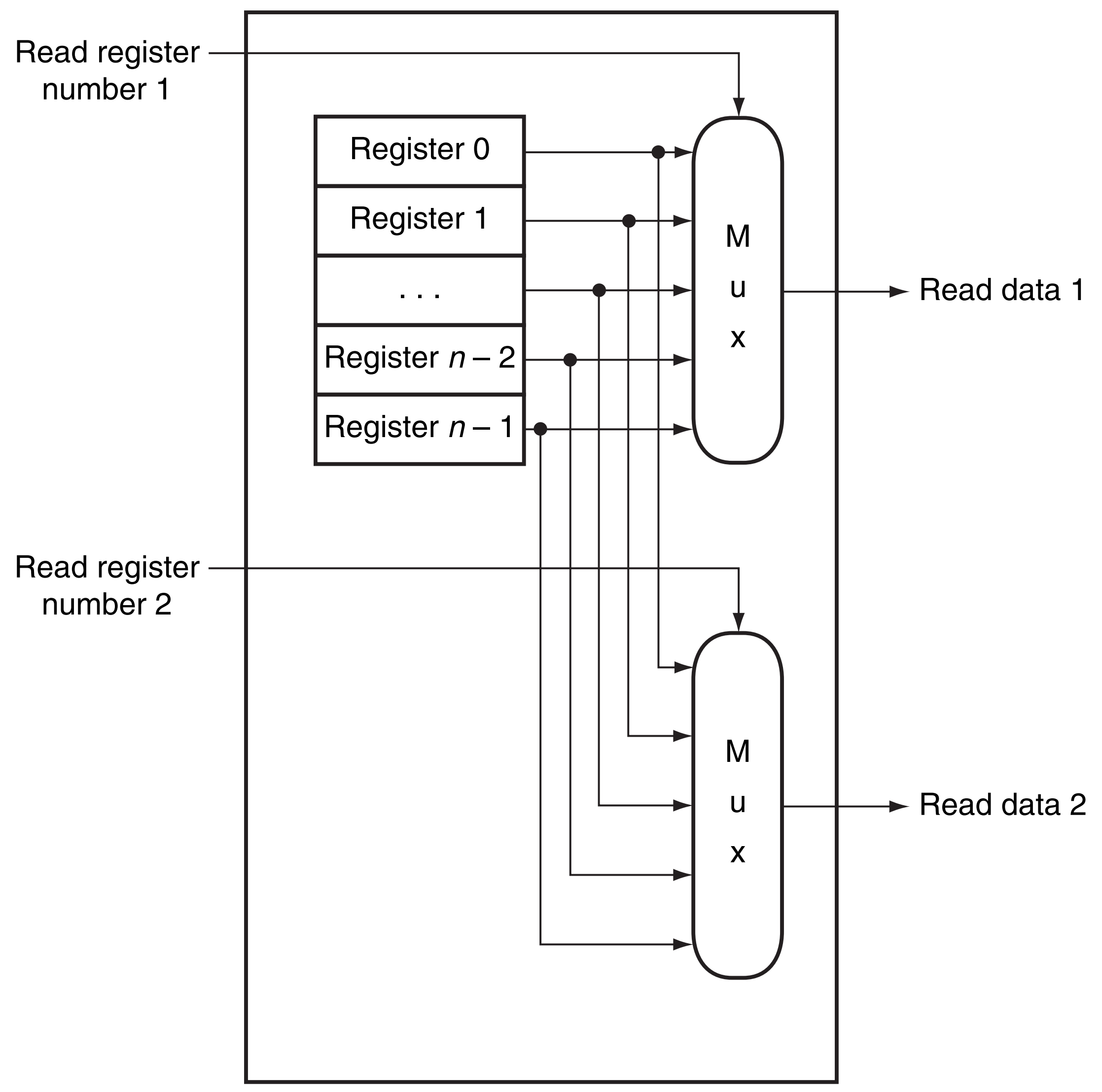
- Clock input (CLK)

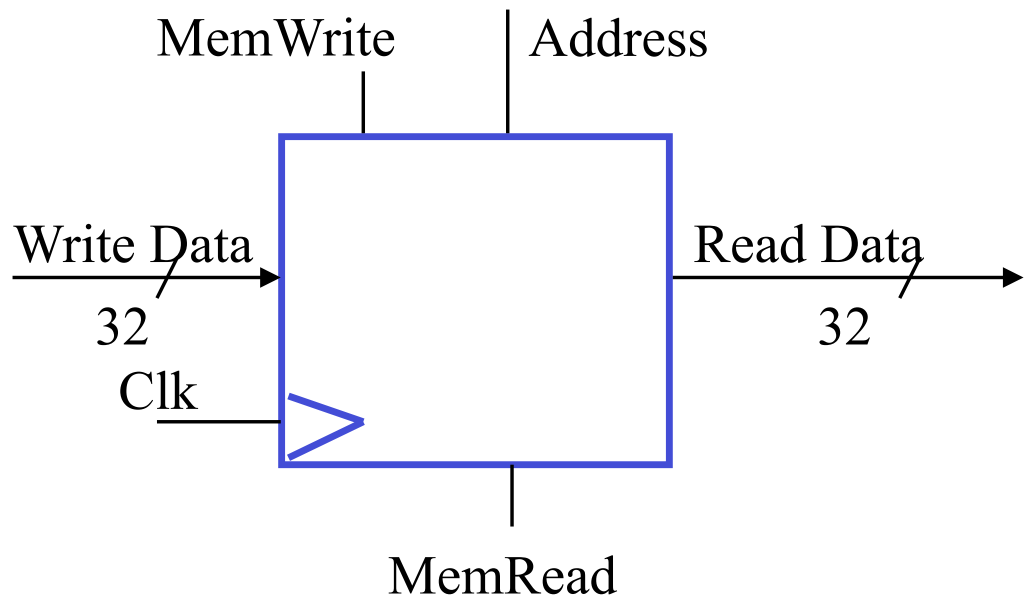


Inside the Register File



- The implementation of two read ports register file
  - n registers
  - done with a pair of n-to-1 multiplexors, each 32 bits wide.

Storage Element: Memory



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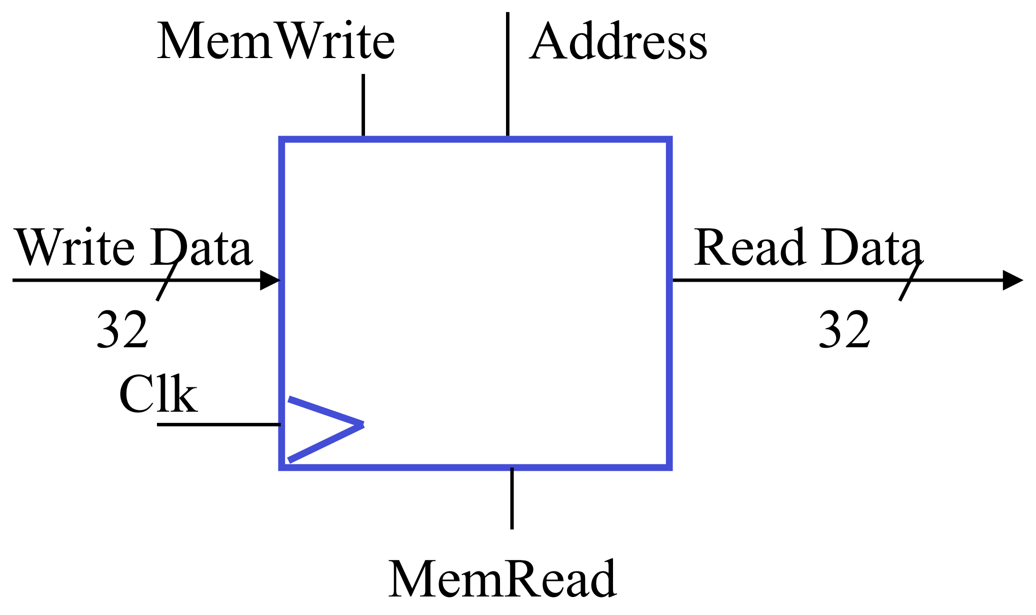
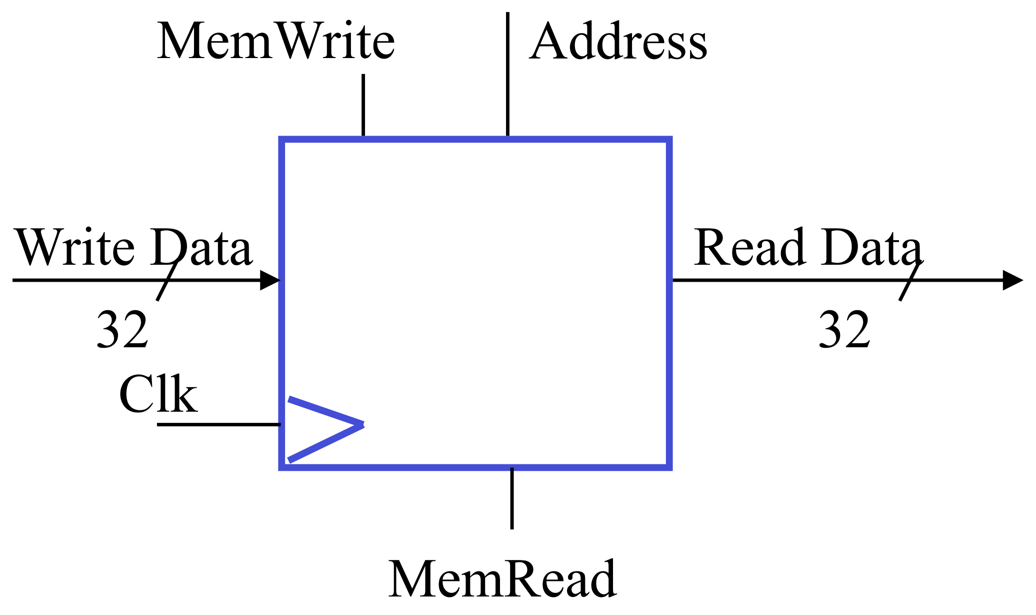


Storage Element: Memory

- Memory
    - Two input buses: WriteData, Address



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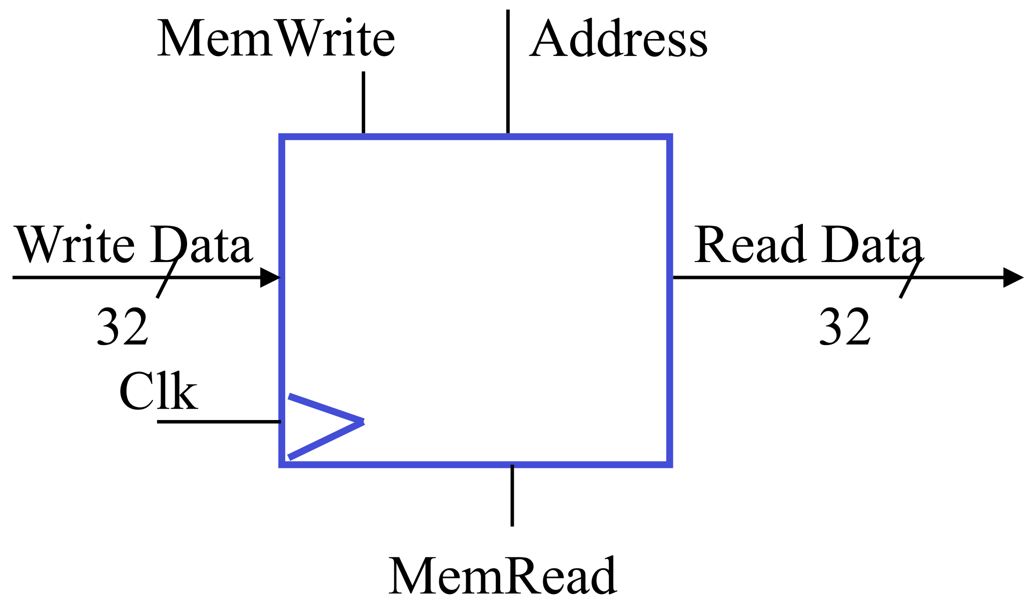

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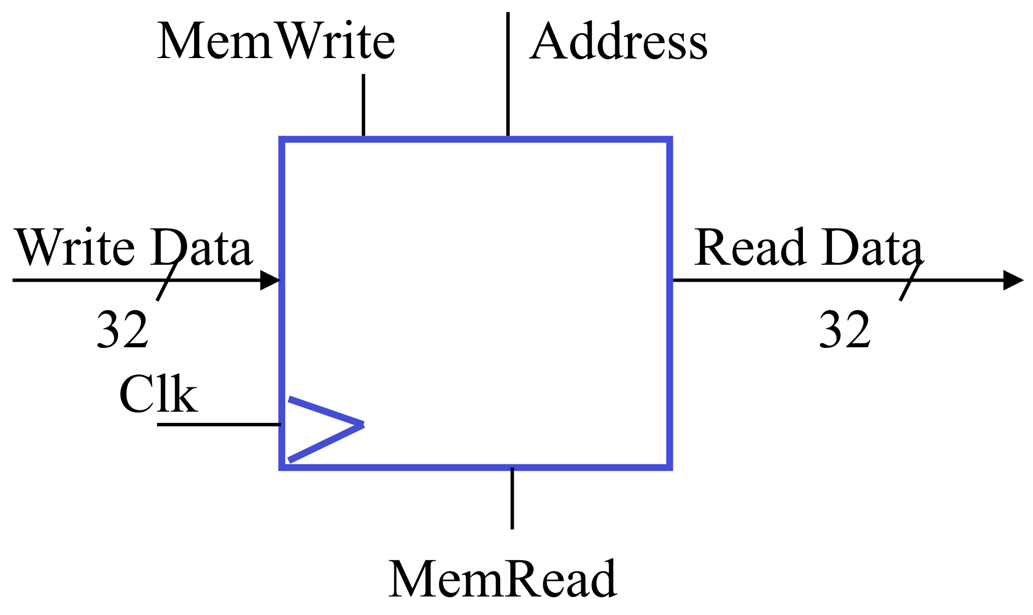

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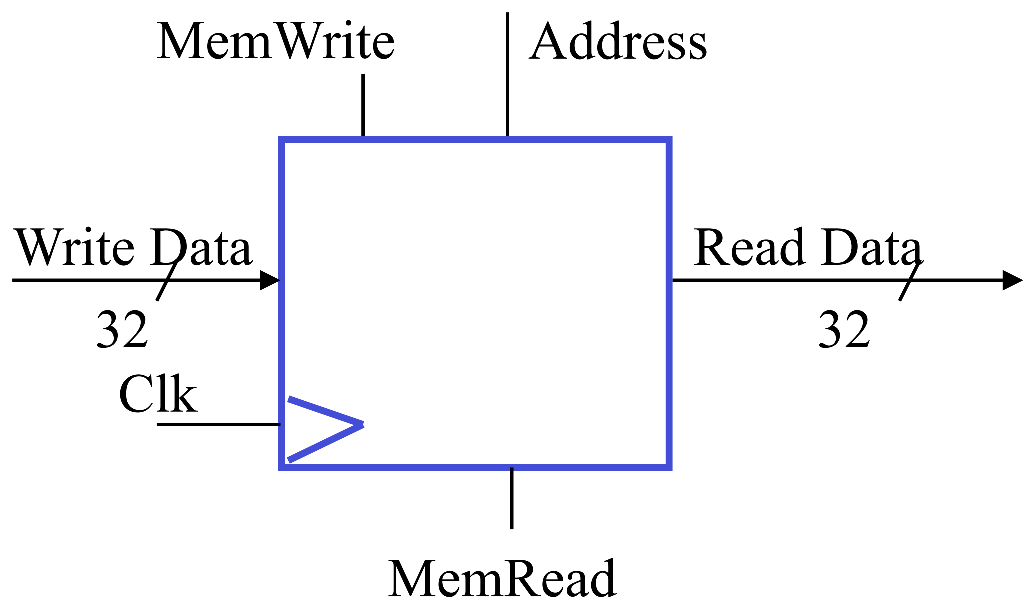

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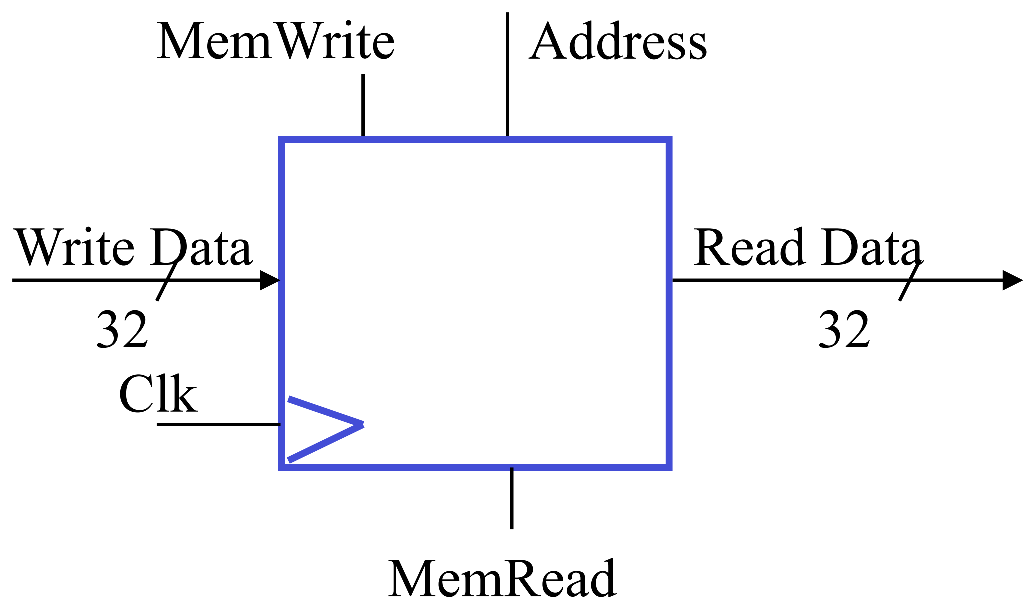

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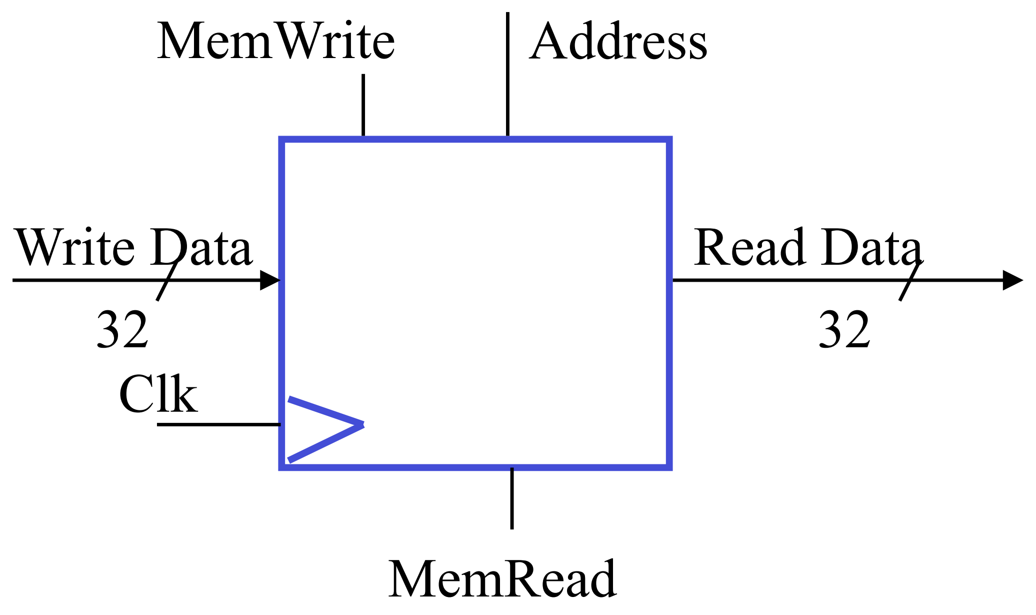

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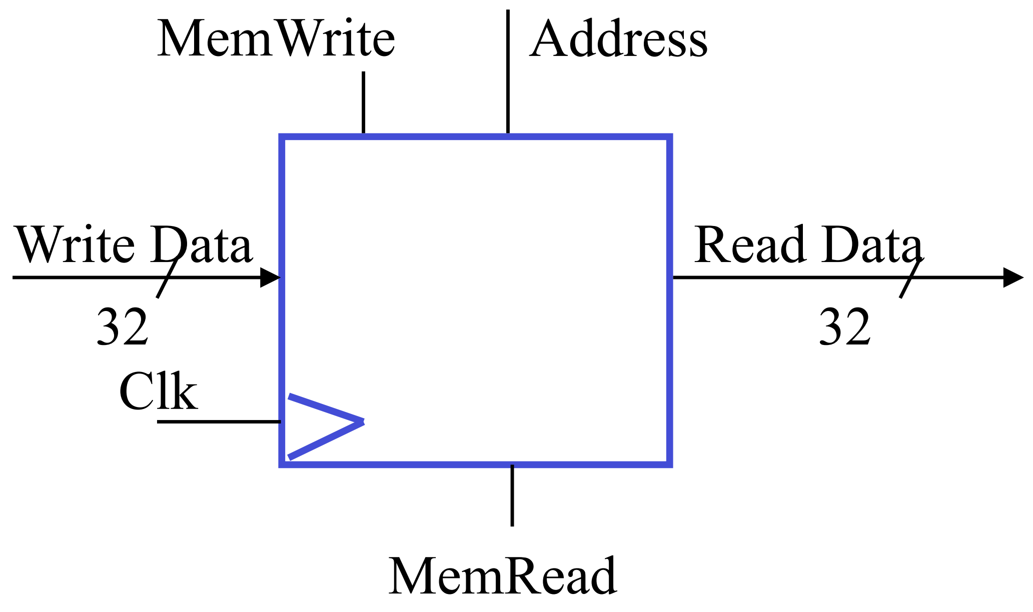

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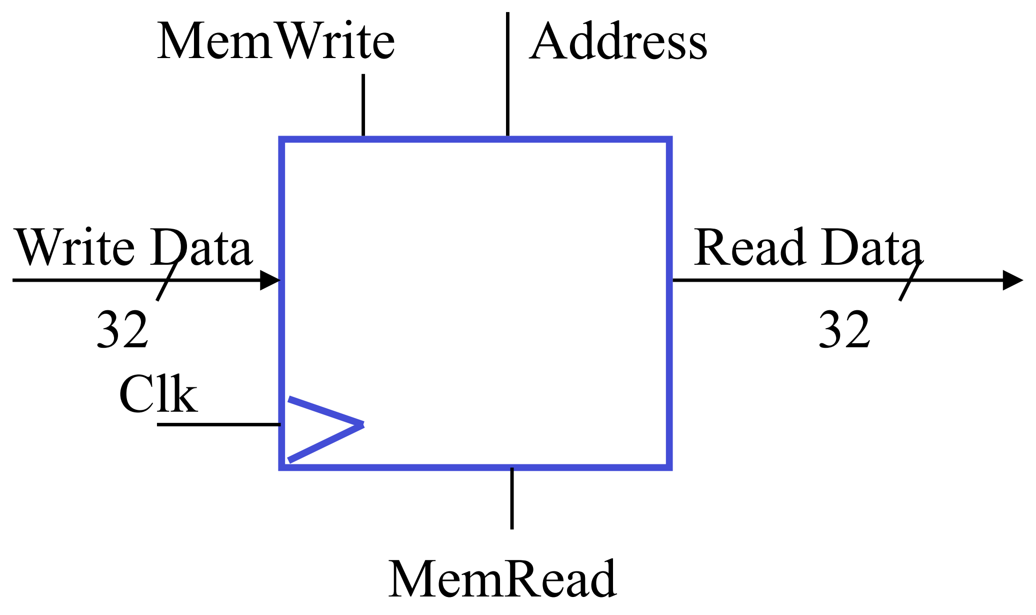

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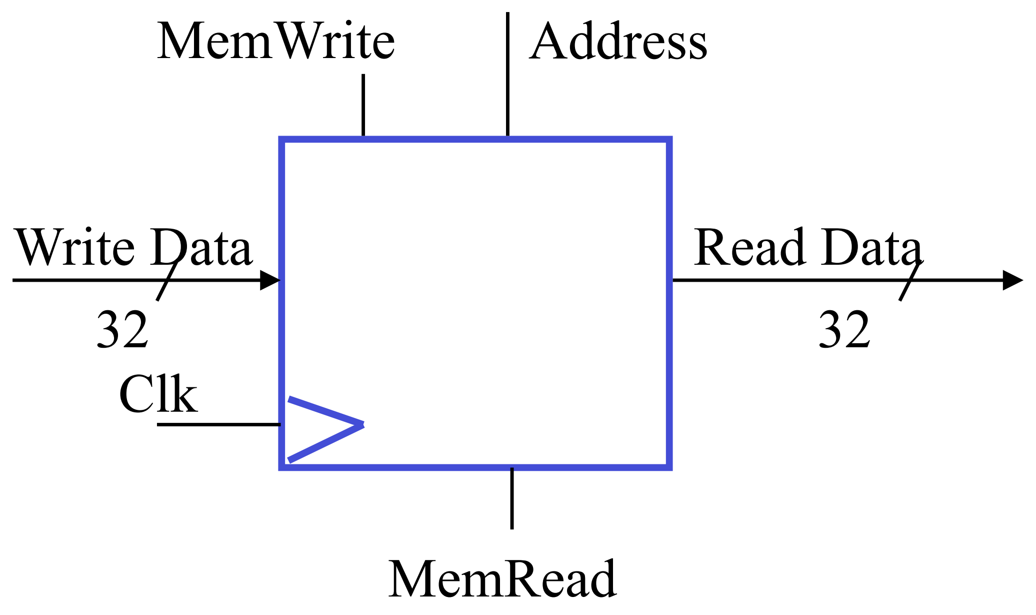
    - Address valid => ReadData valid after "access time."

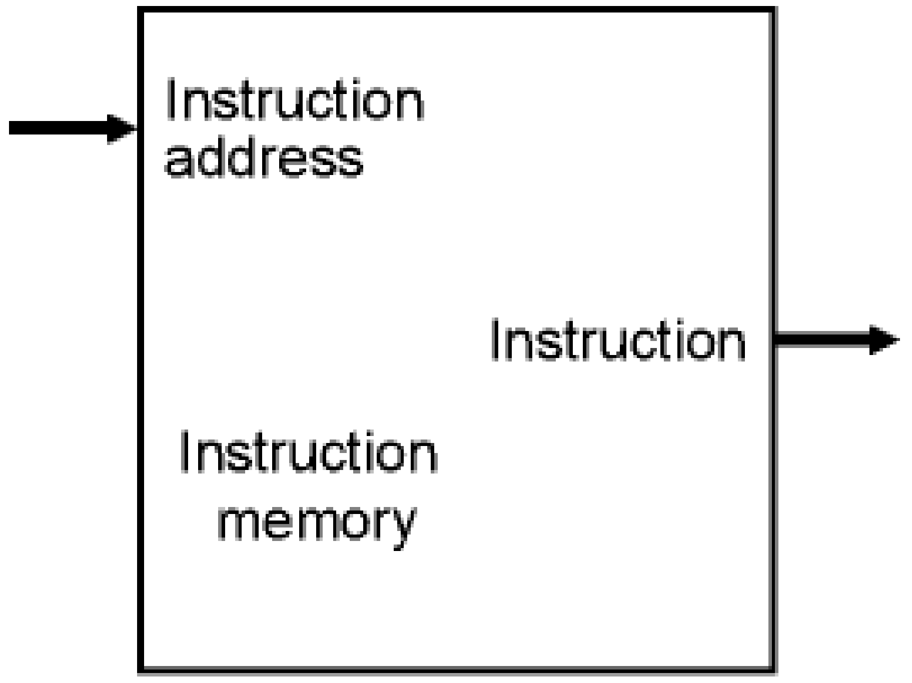


RTL: Register Transfer Language

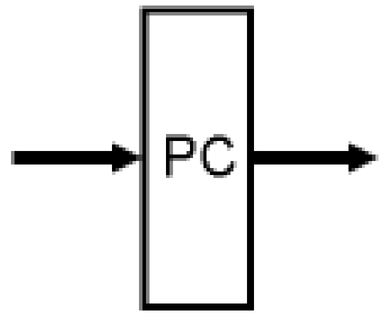
- Describes the movement and manipulation of data between storage elements:

```
R[3] <- R[5] + R[7]
PC <- PC + 4 + R[5]
R[rd] <- R[rs] + R[rt]
R[rt] <- Mem[R[rs] + immed]
```

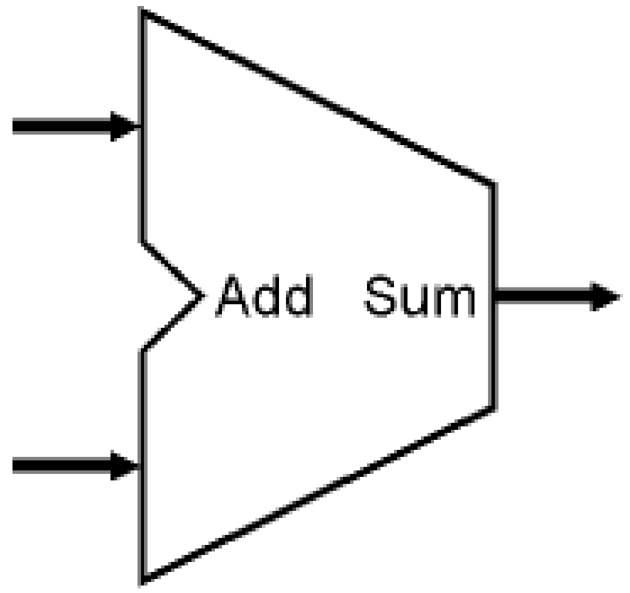
Instruction Fetch and Program Counter Management



a. Instruction memory



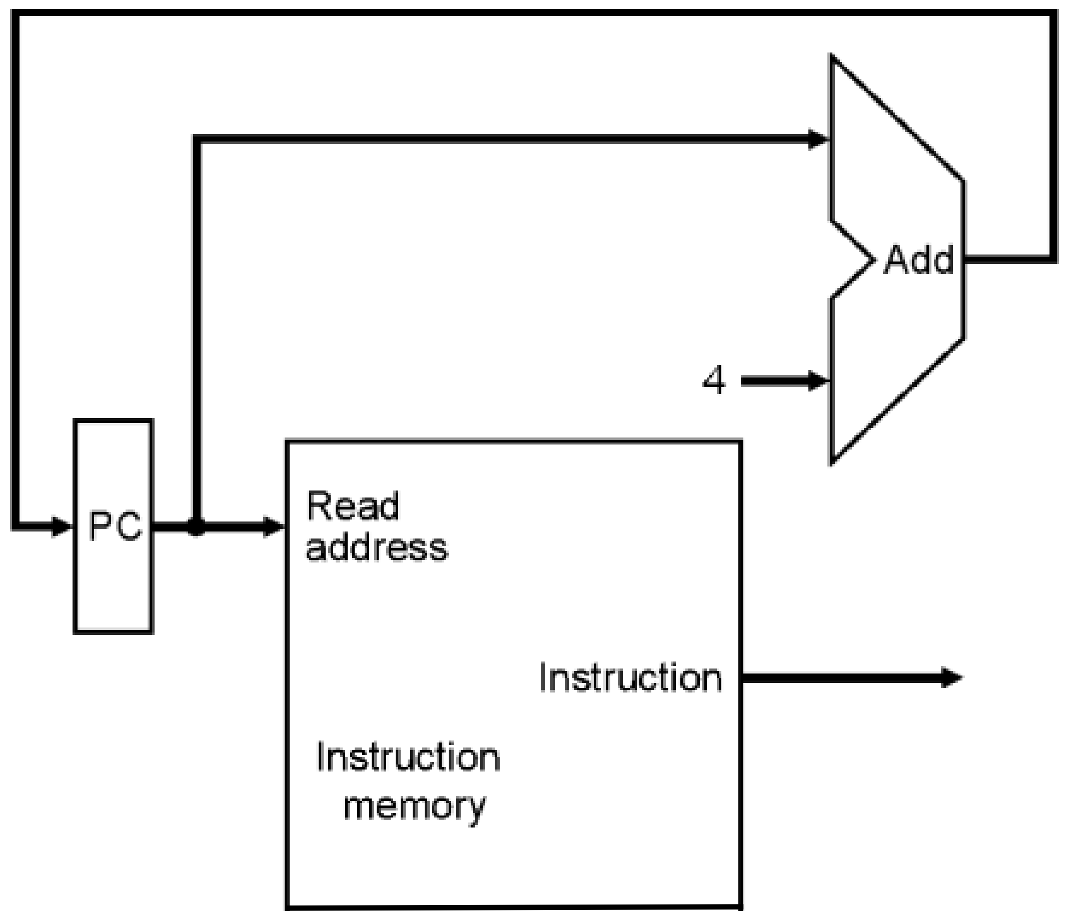
b. Program counter



c. Adder

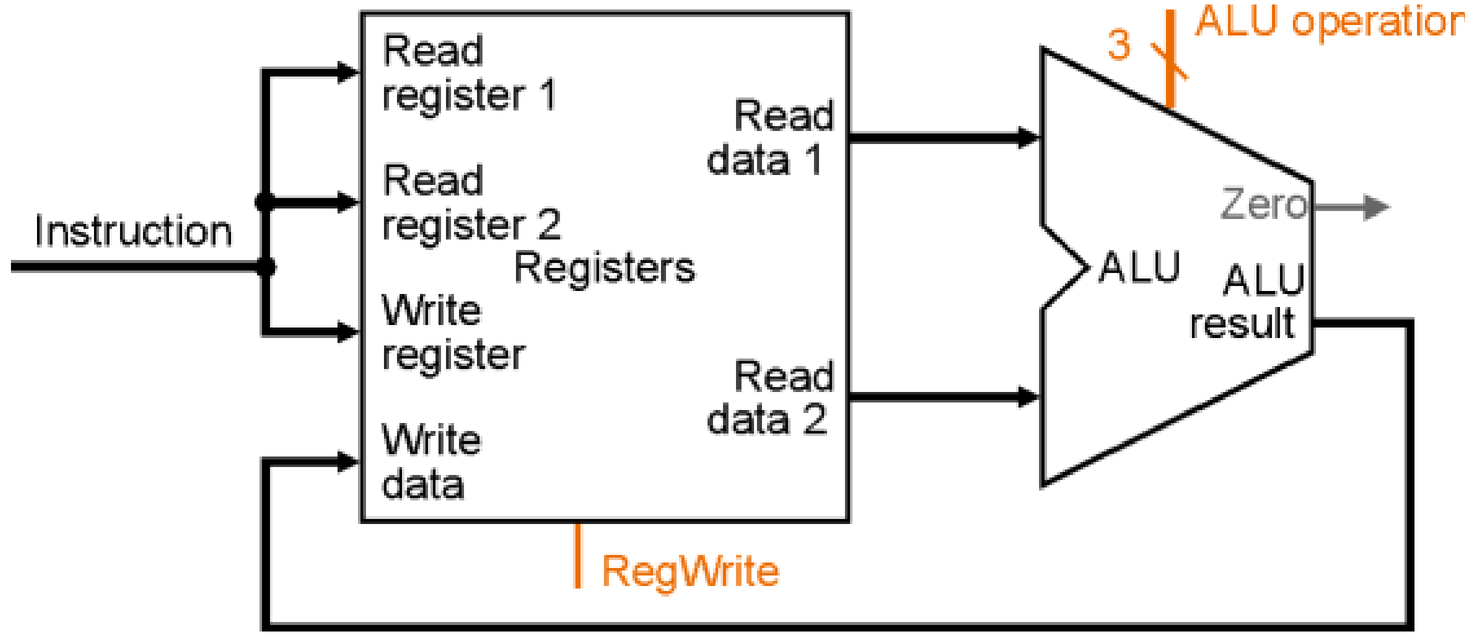
Overview of the Instruction Fetch Unit

- The common RTL operations
  - Fetch the Instruction: inst <- mem[PC]
  - Update the program counter:
    - Sequential Code: PC <- PC + 4
    - Branch and Jump   PC <- “something else”



Datapath for Register-Register Operations

6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
opcode	rs	rt	rd	shift amount	funct



Datapath for Register-Register Operations

- R[rd] <- R[rs] op R[rt] Example: *add   rd, rs, rt*

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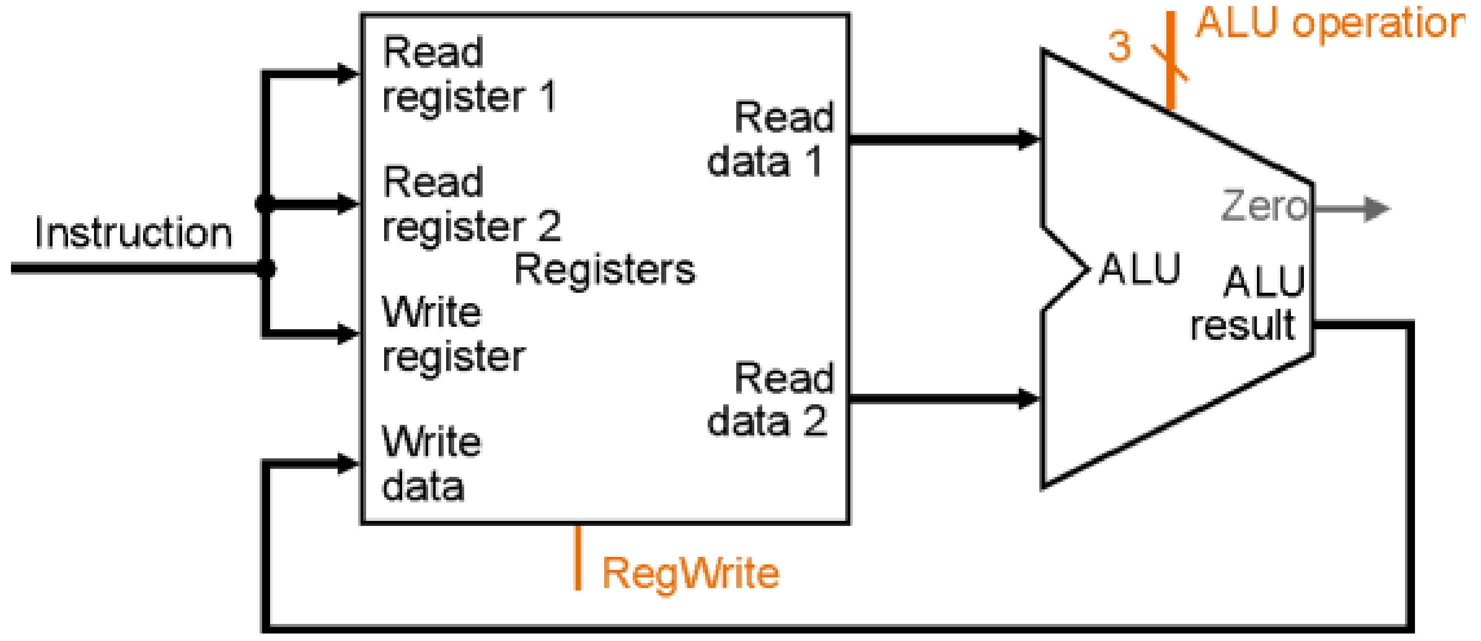

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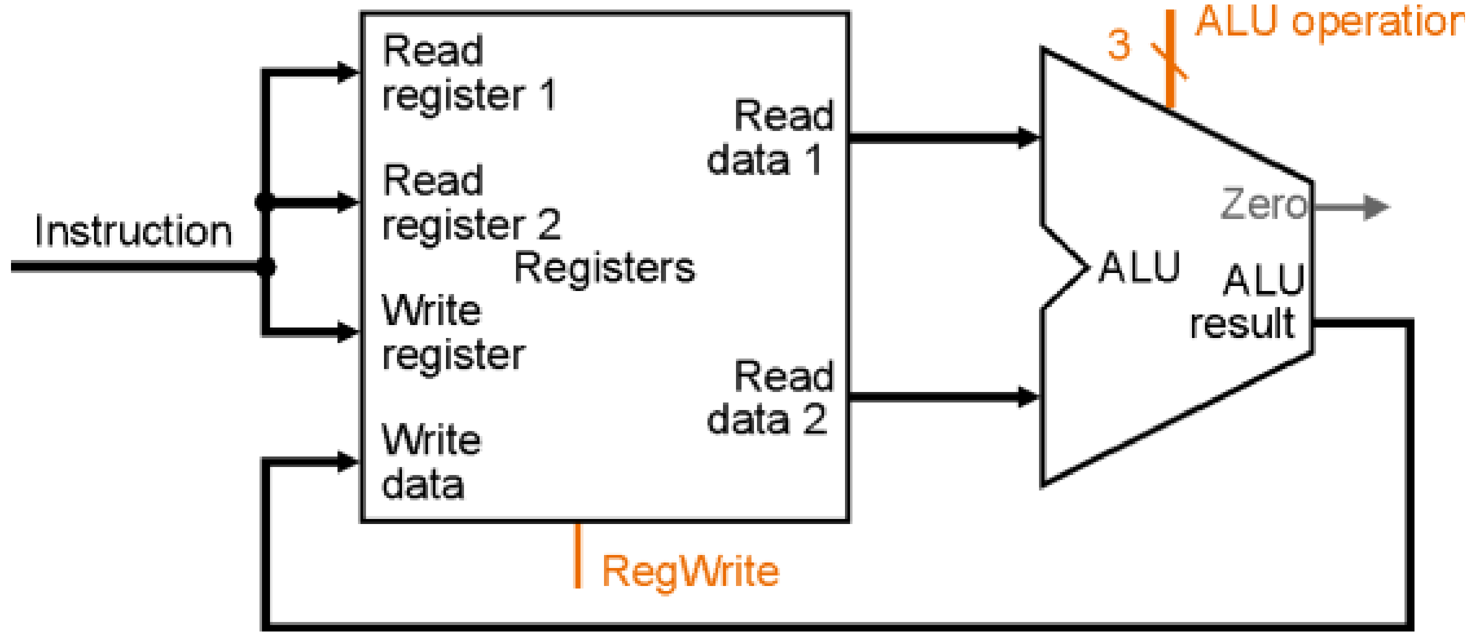

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  - ALUoperation and RegWrite: control logic after decoding instruction

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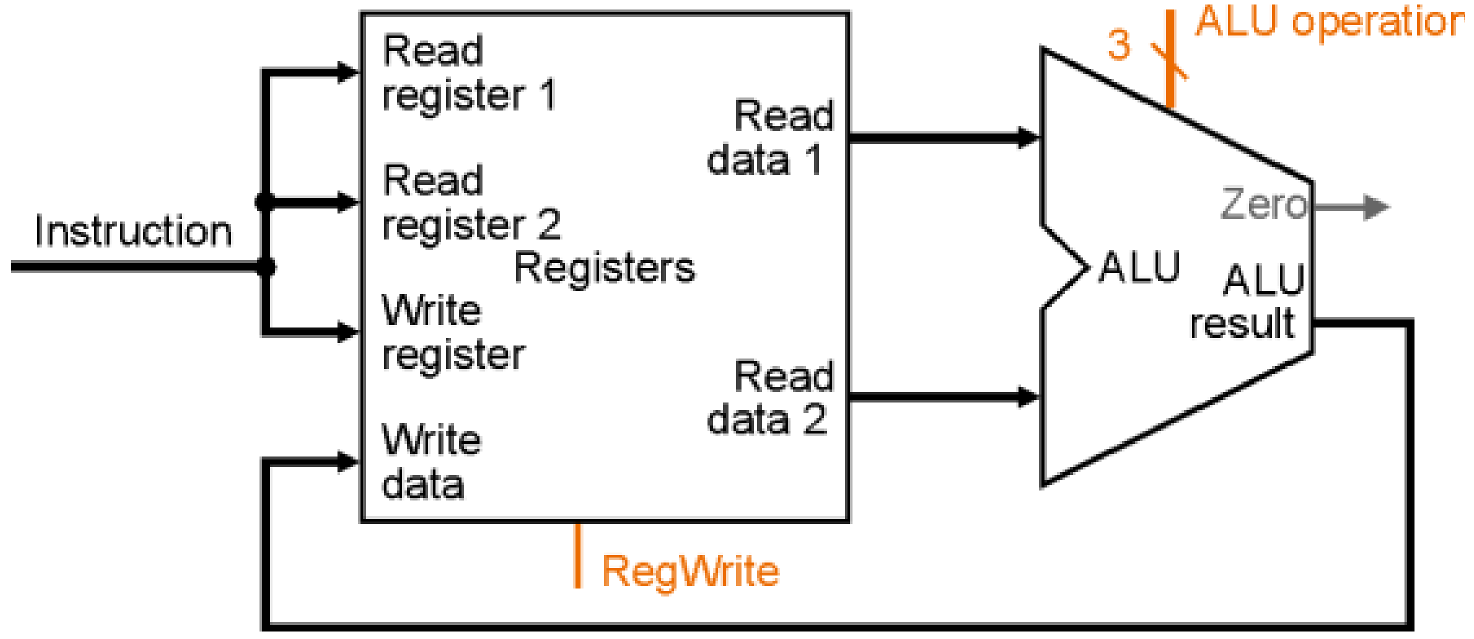
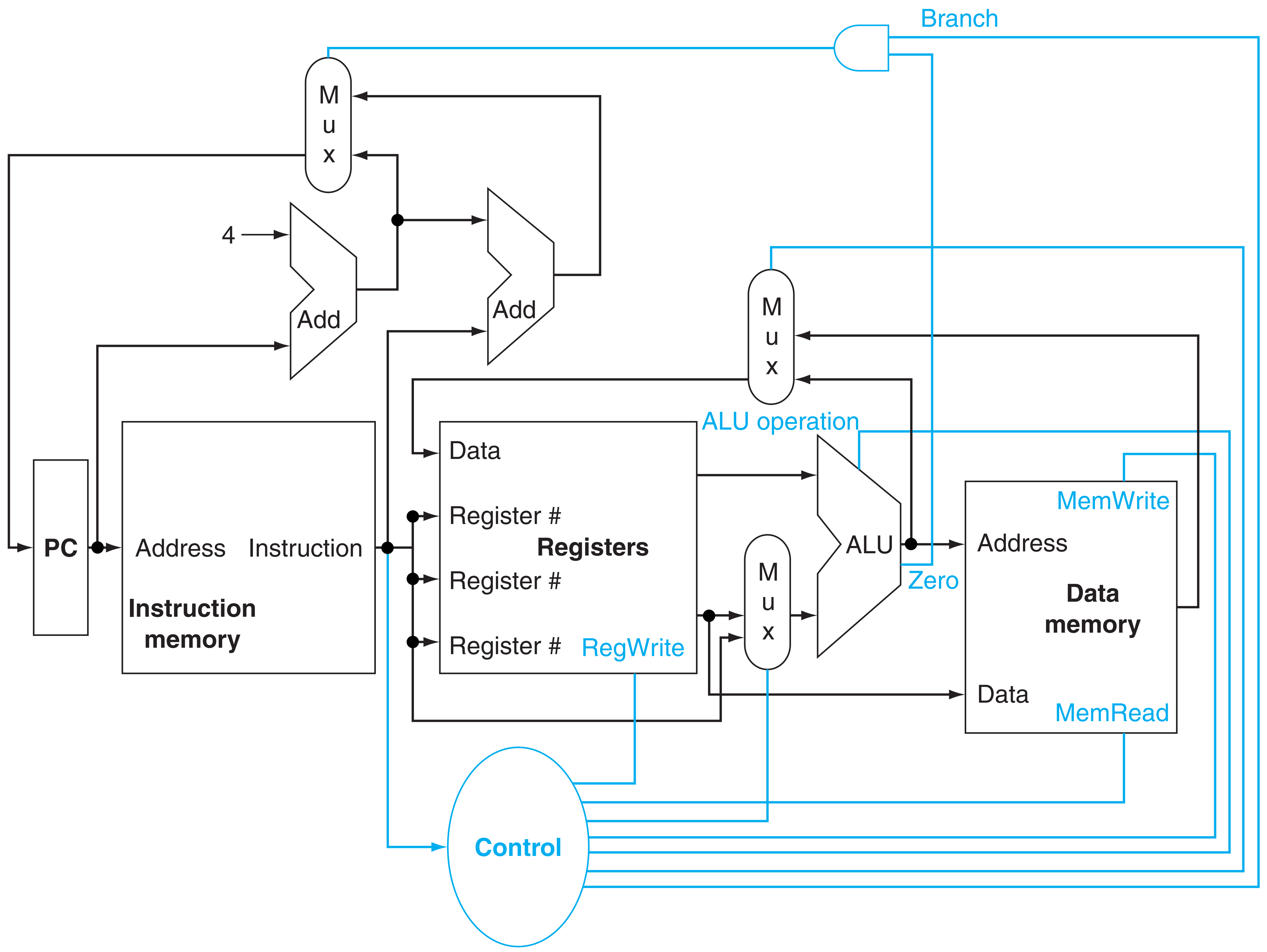


Control Logic??



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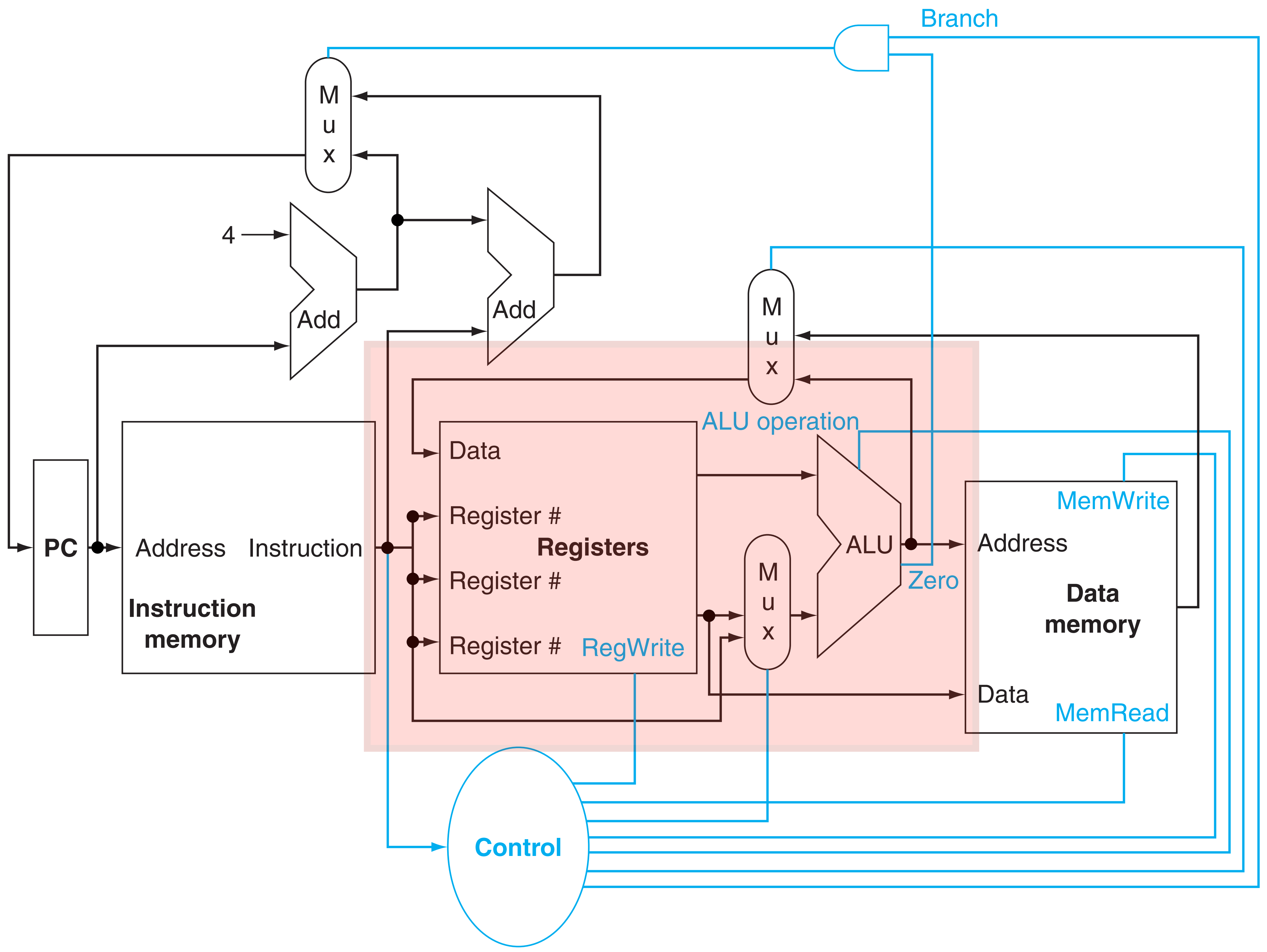

Datapath for Load Operations

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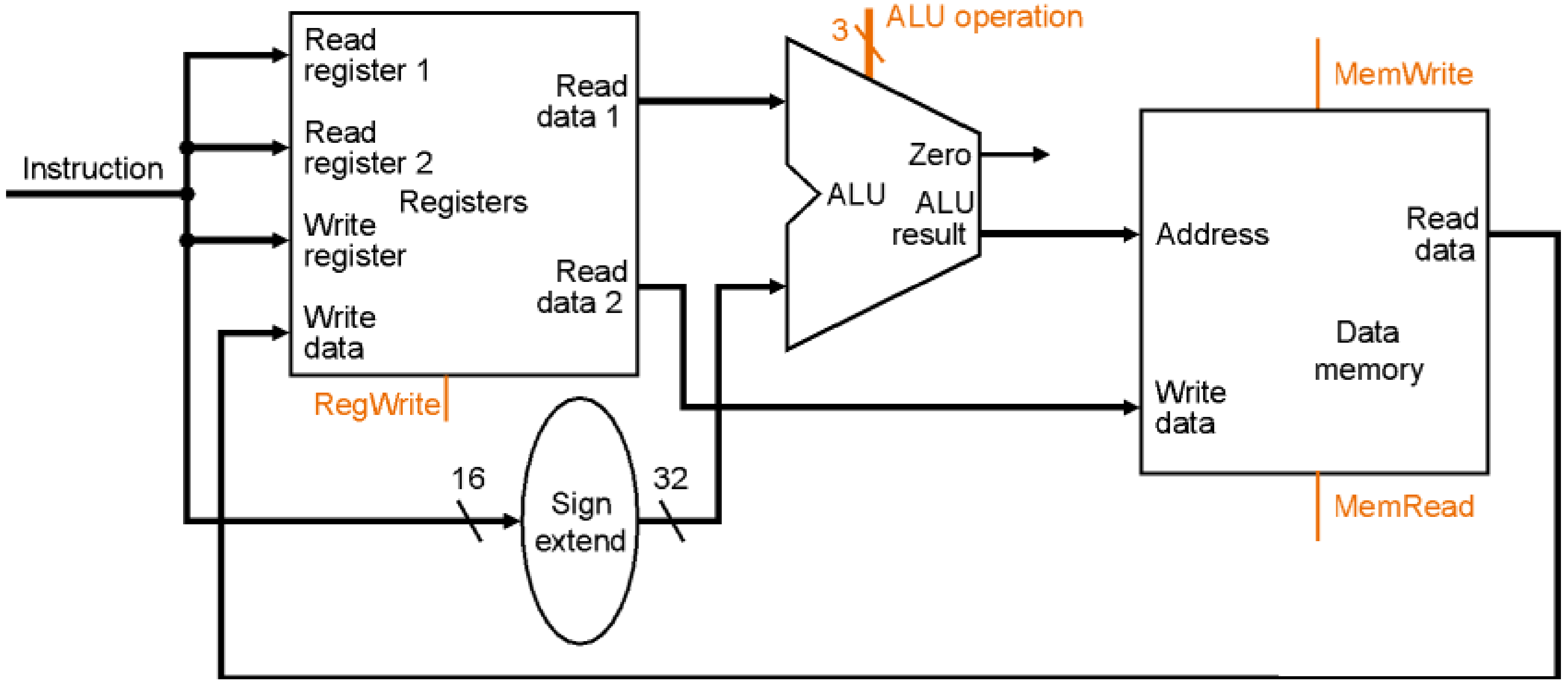

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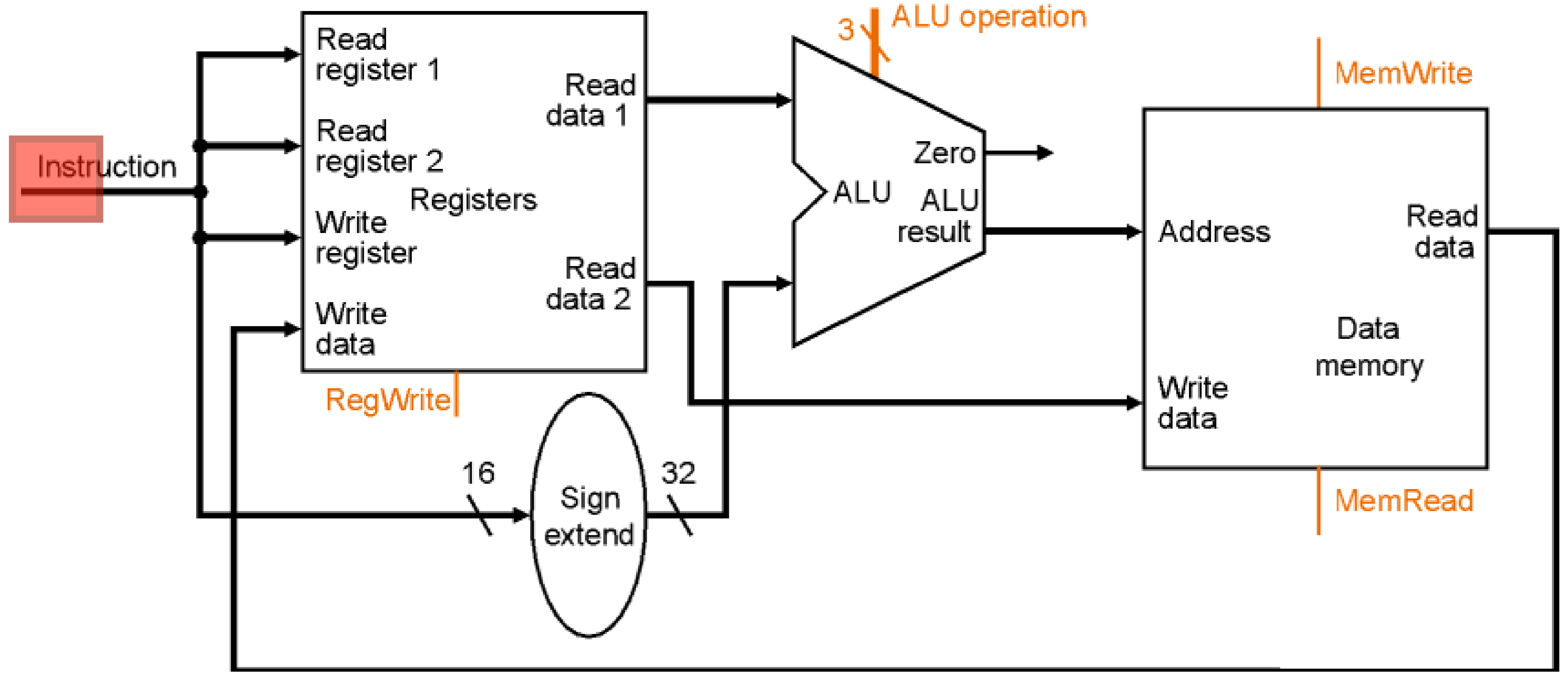

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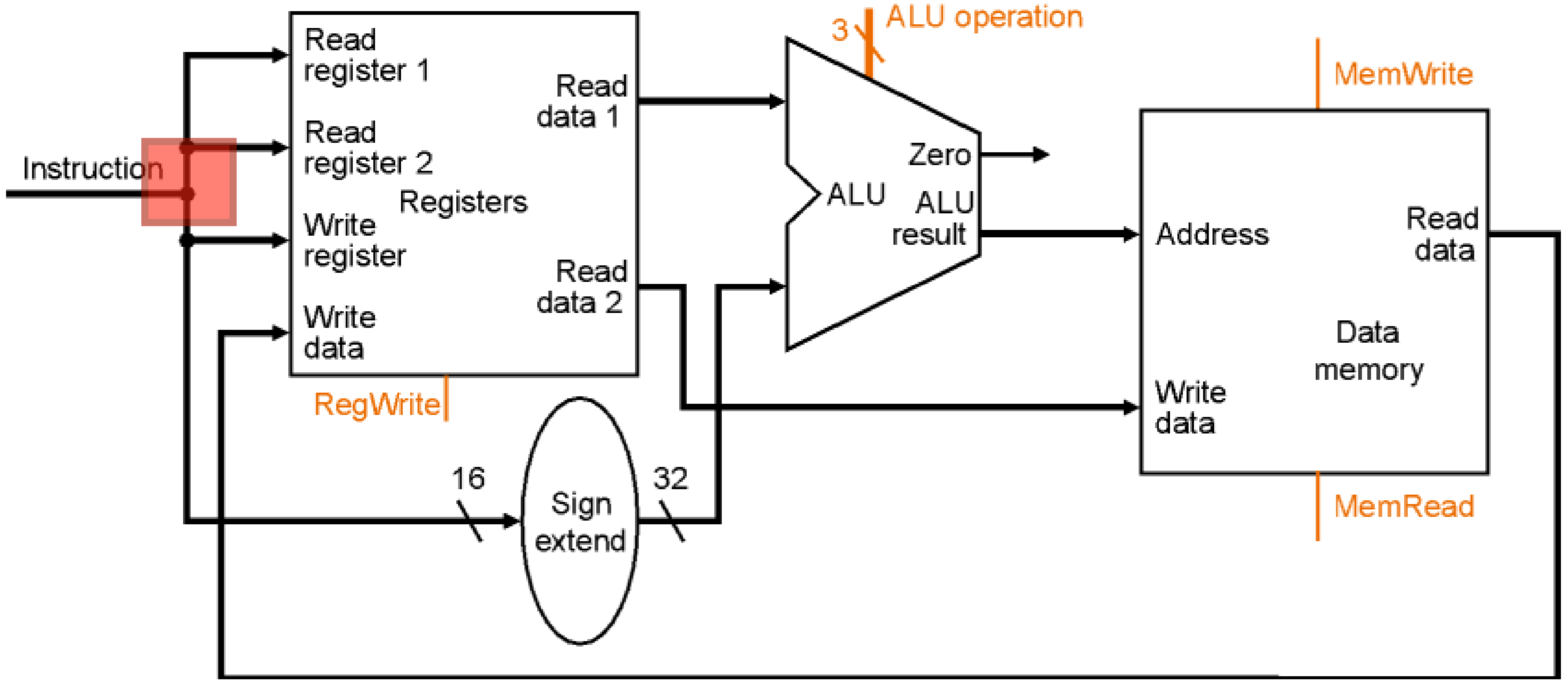

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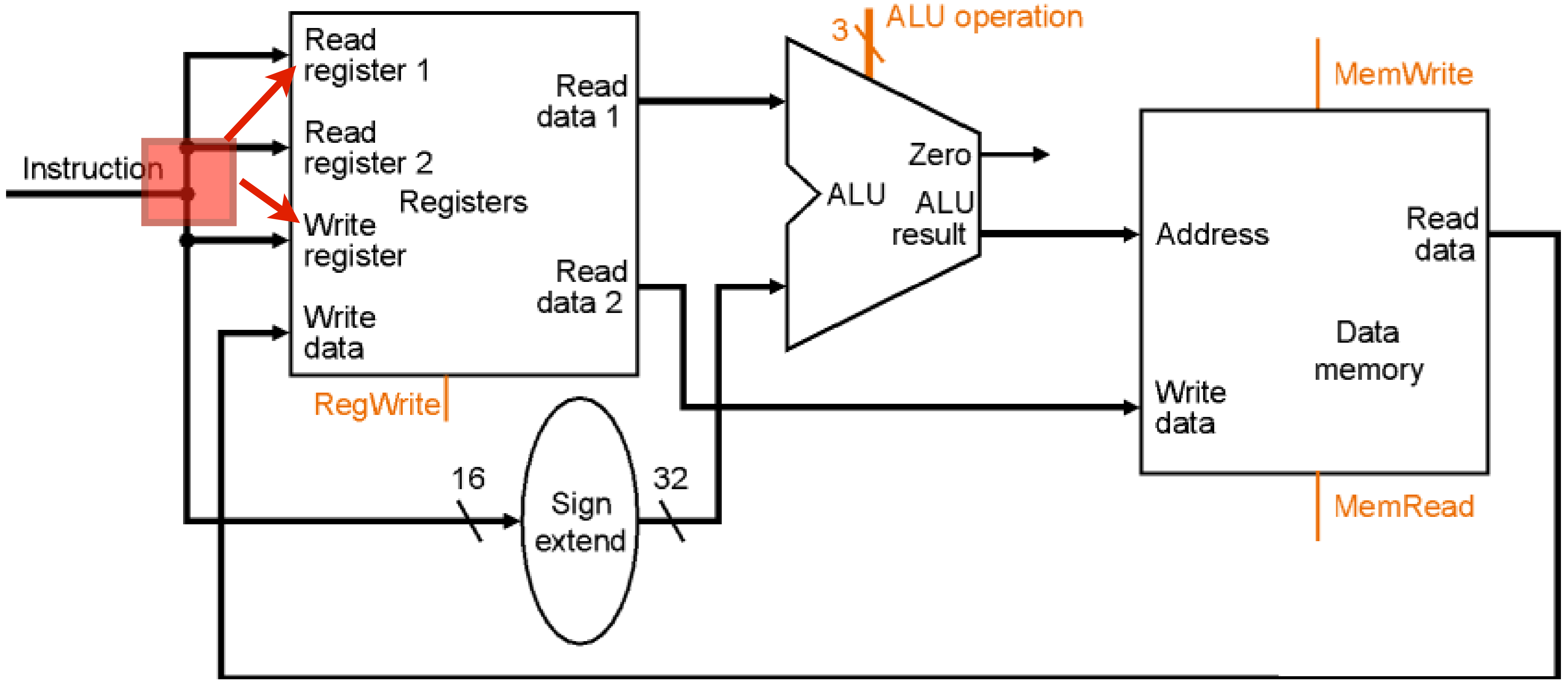

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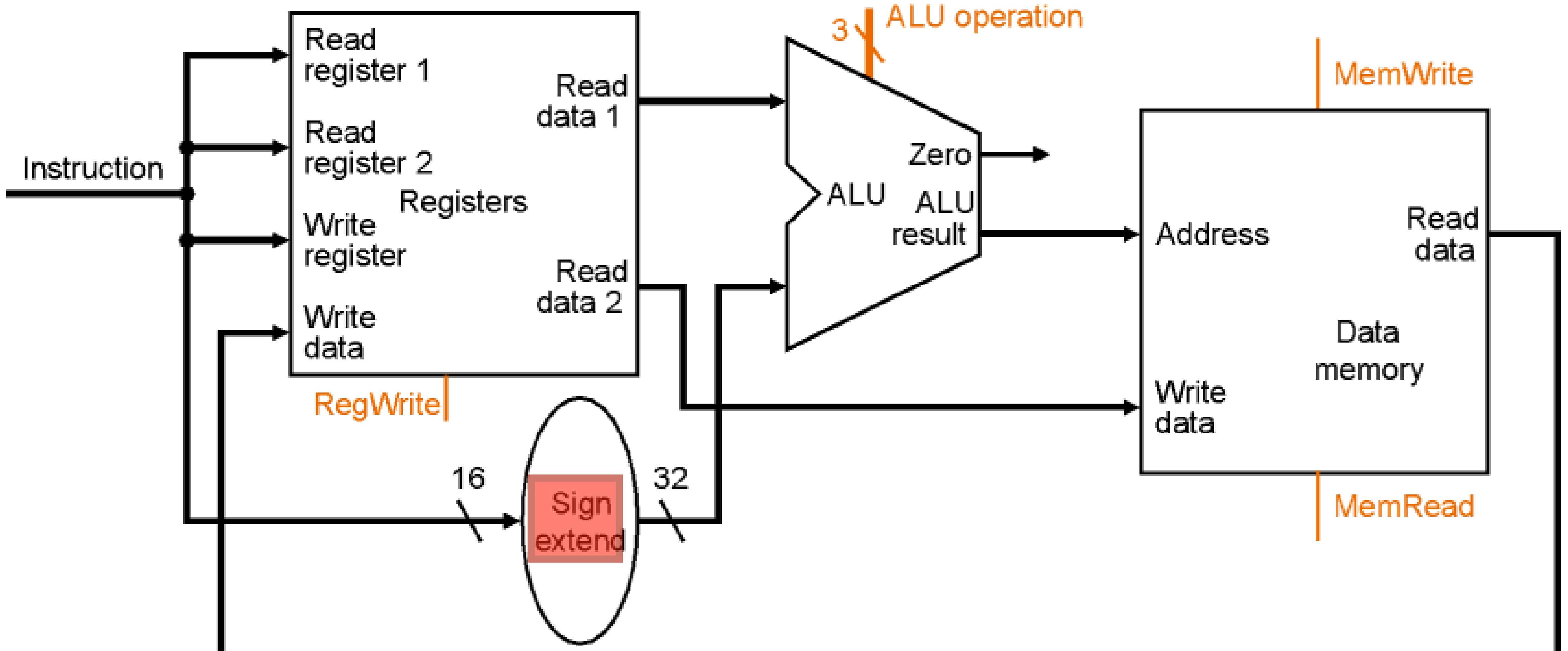

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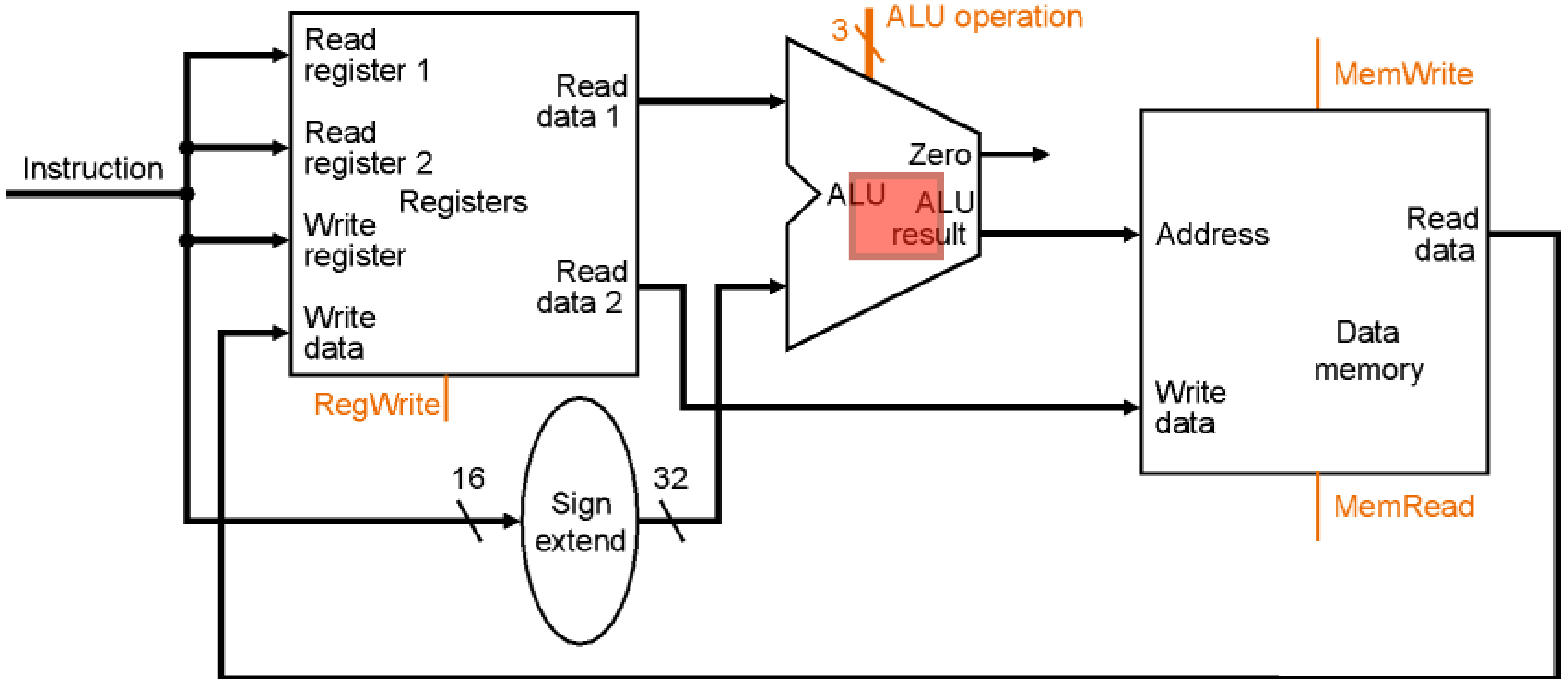

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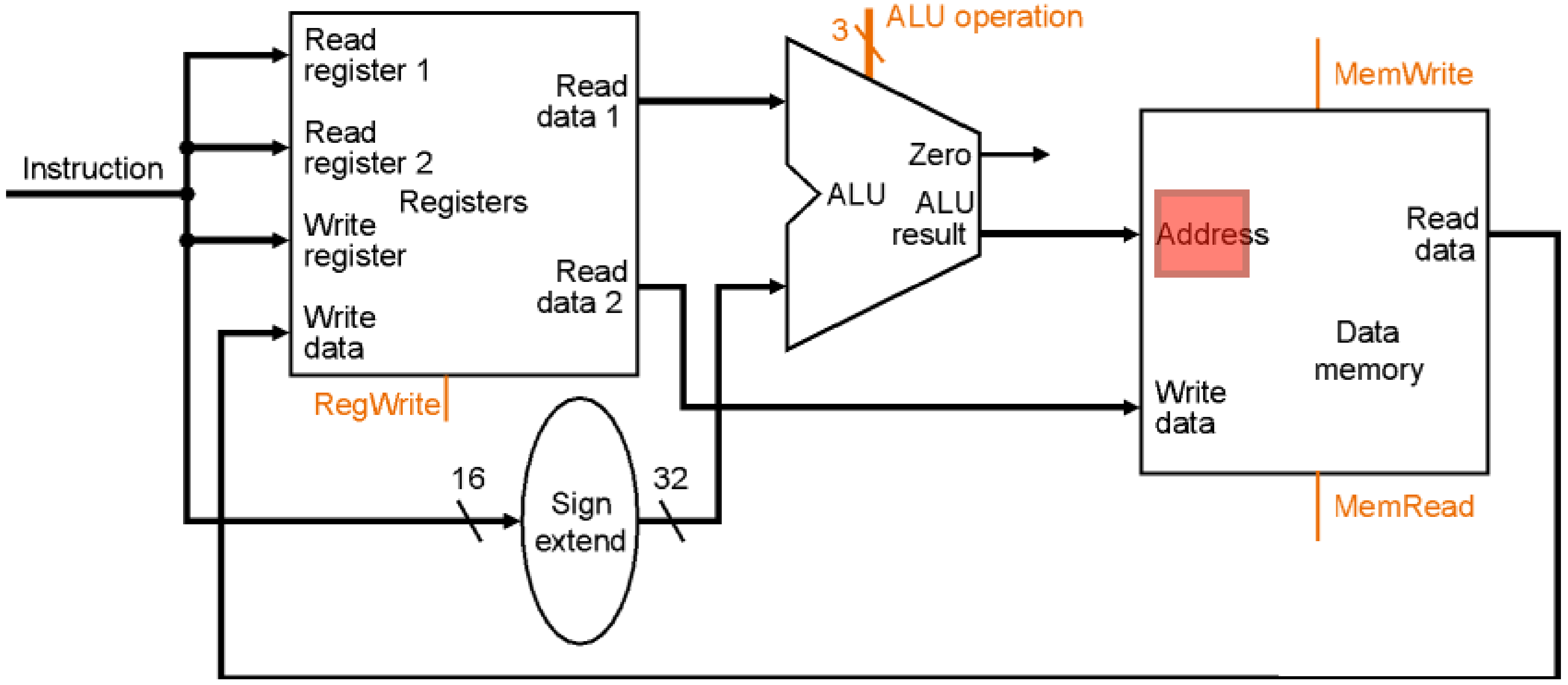

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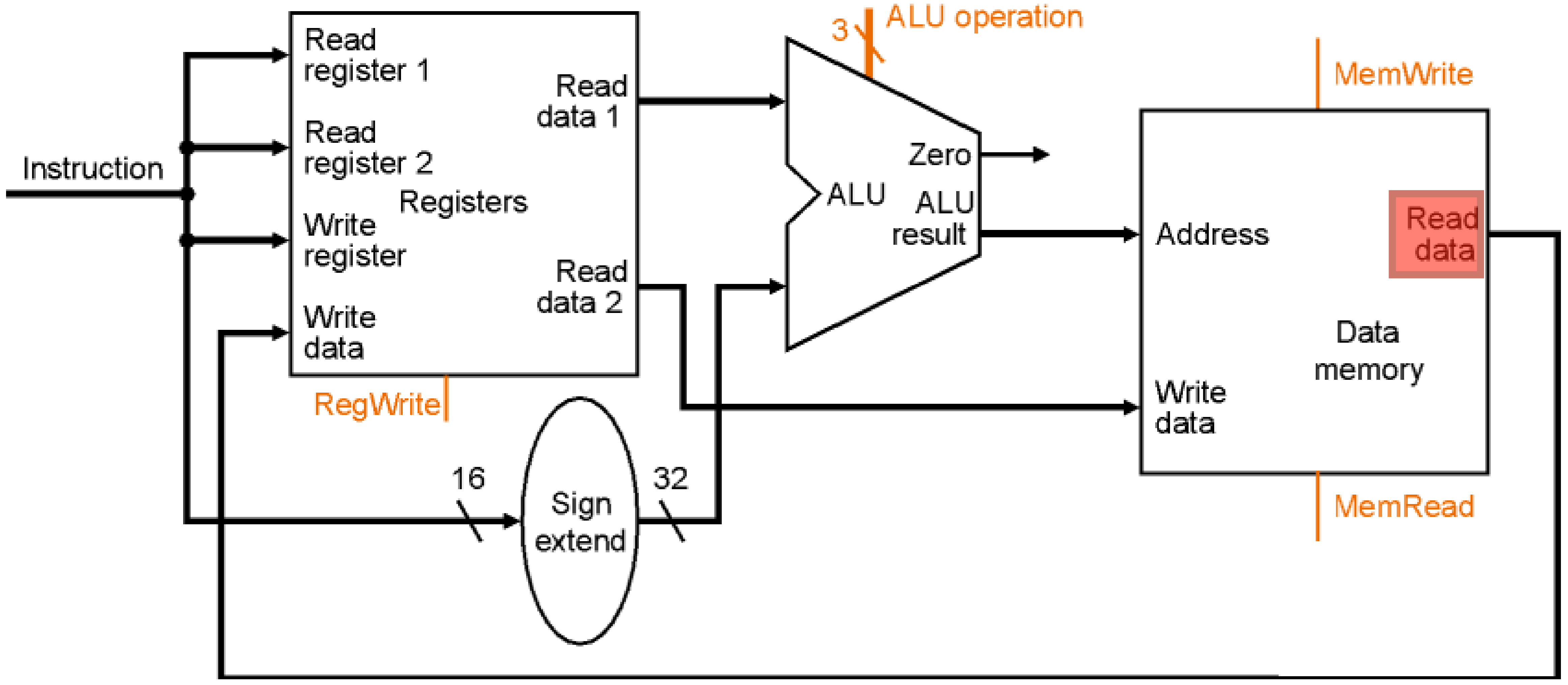

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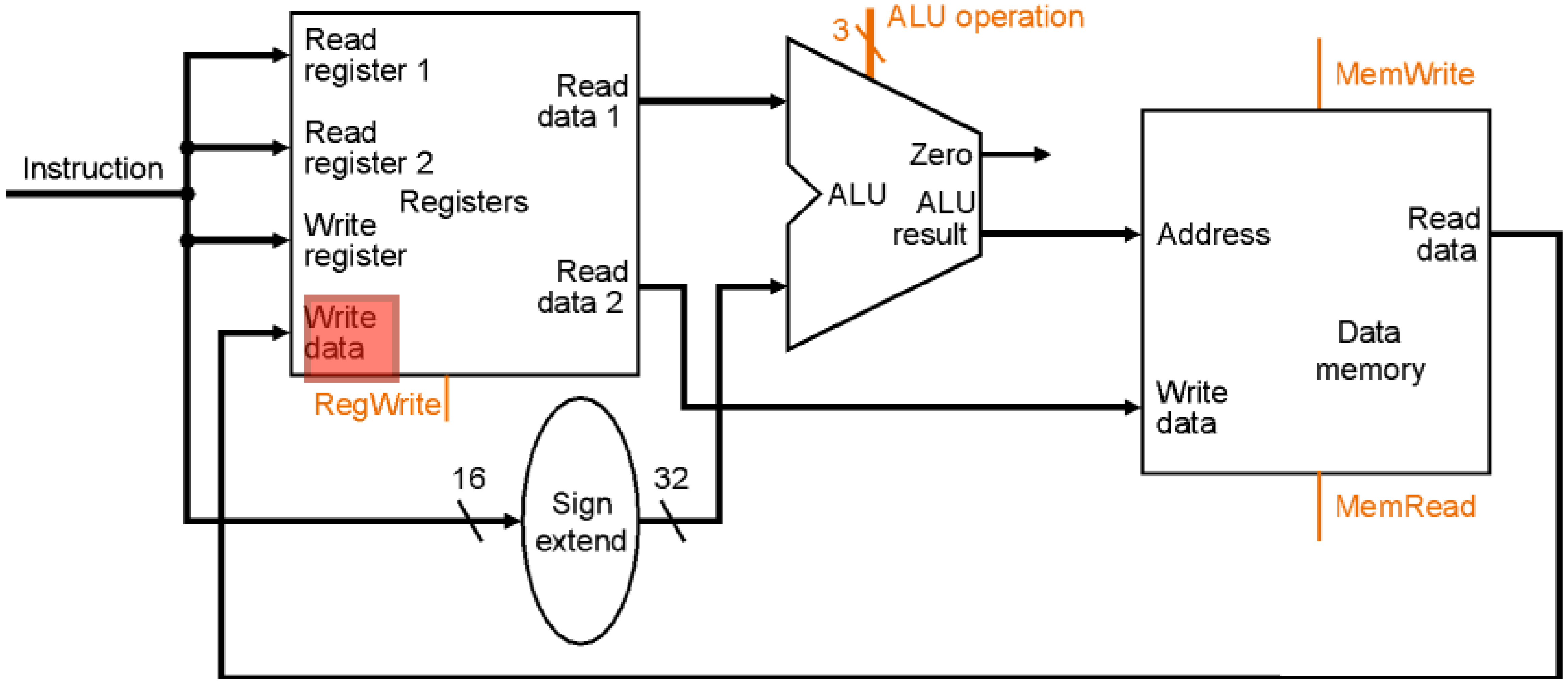

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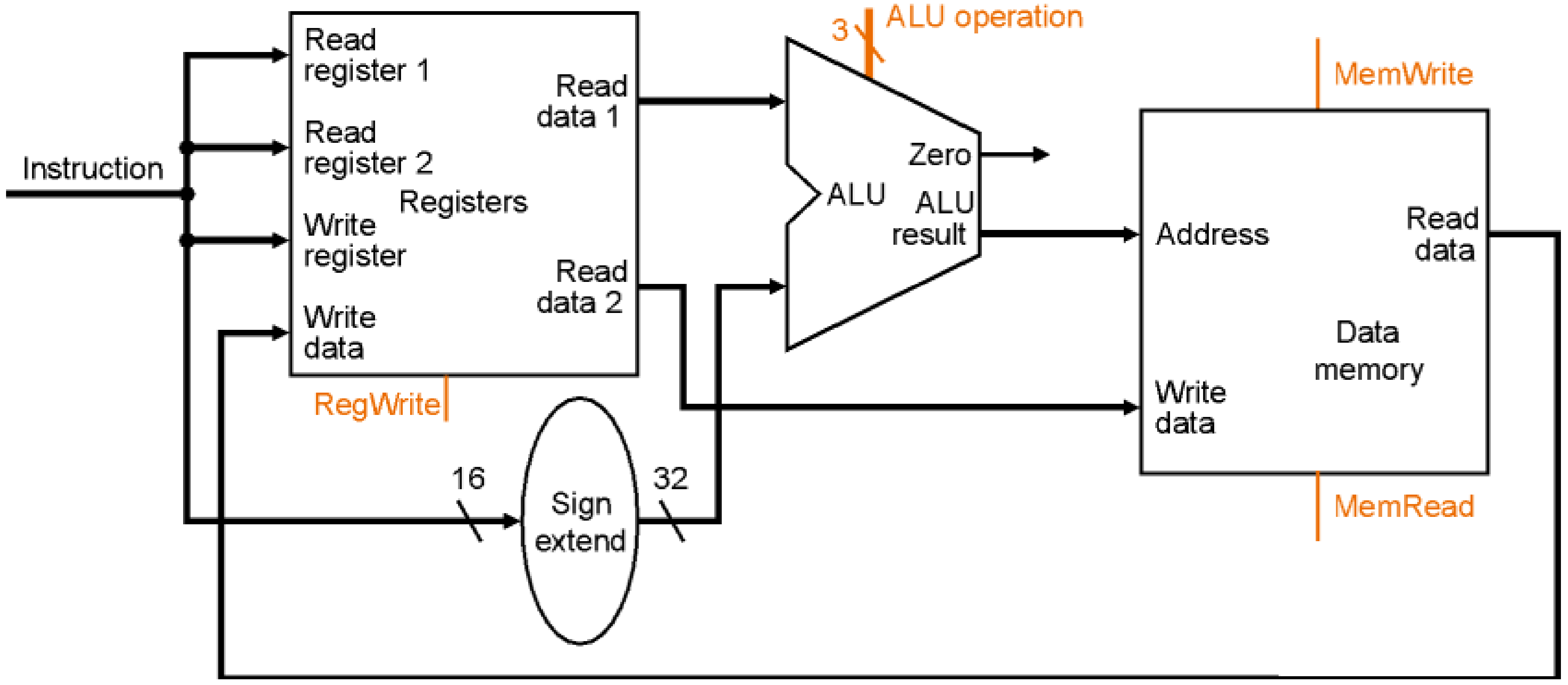

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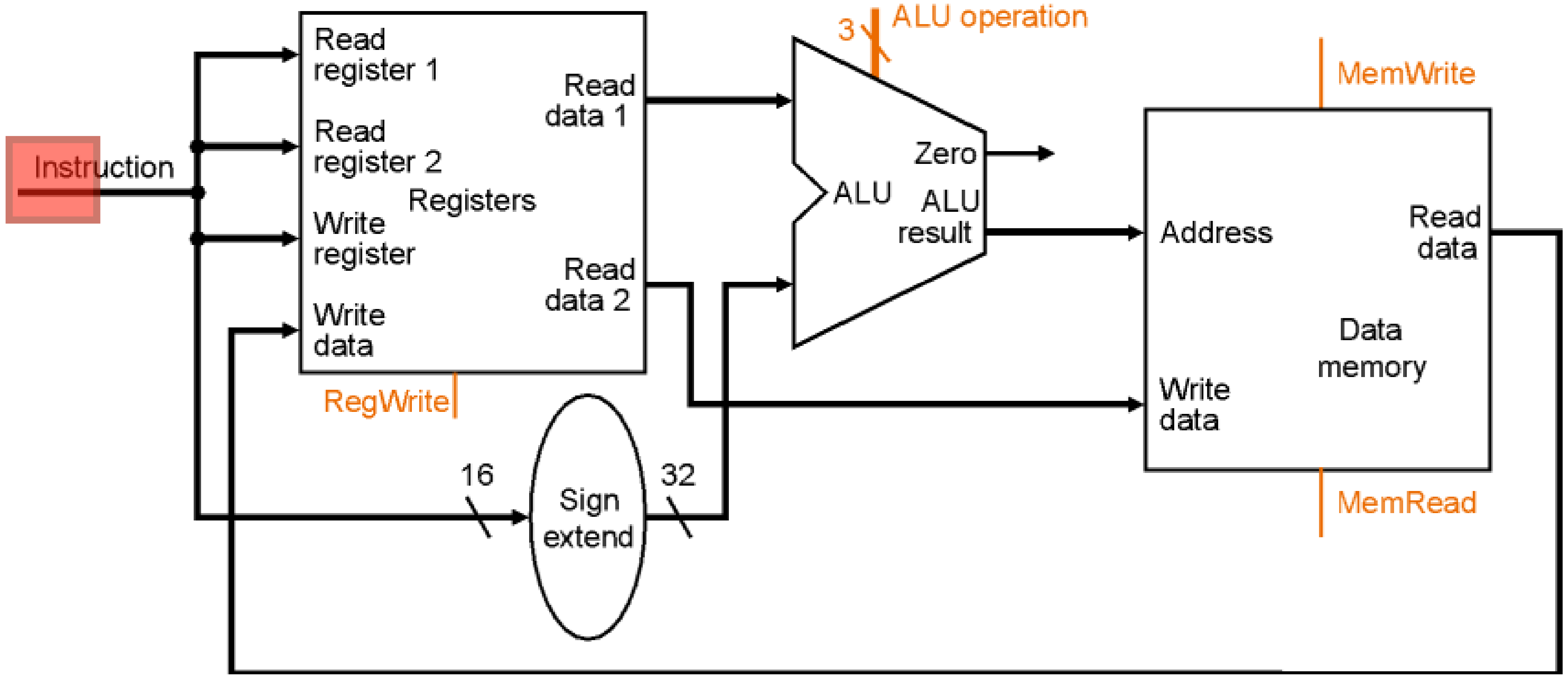

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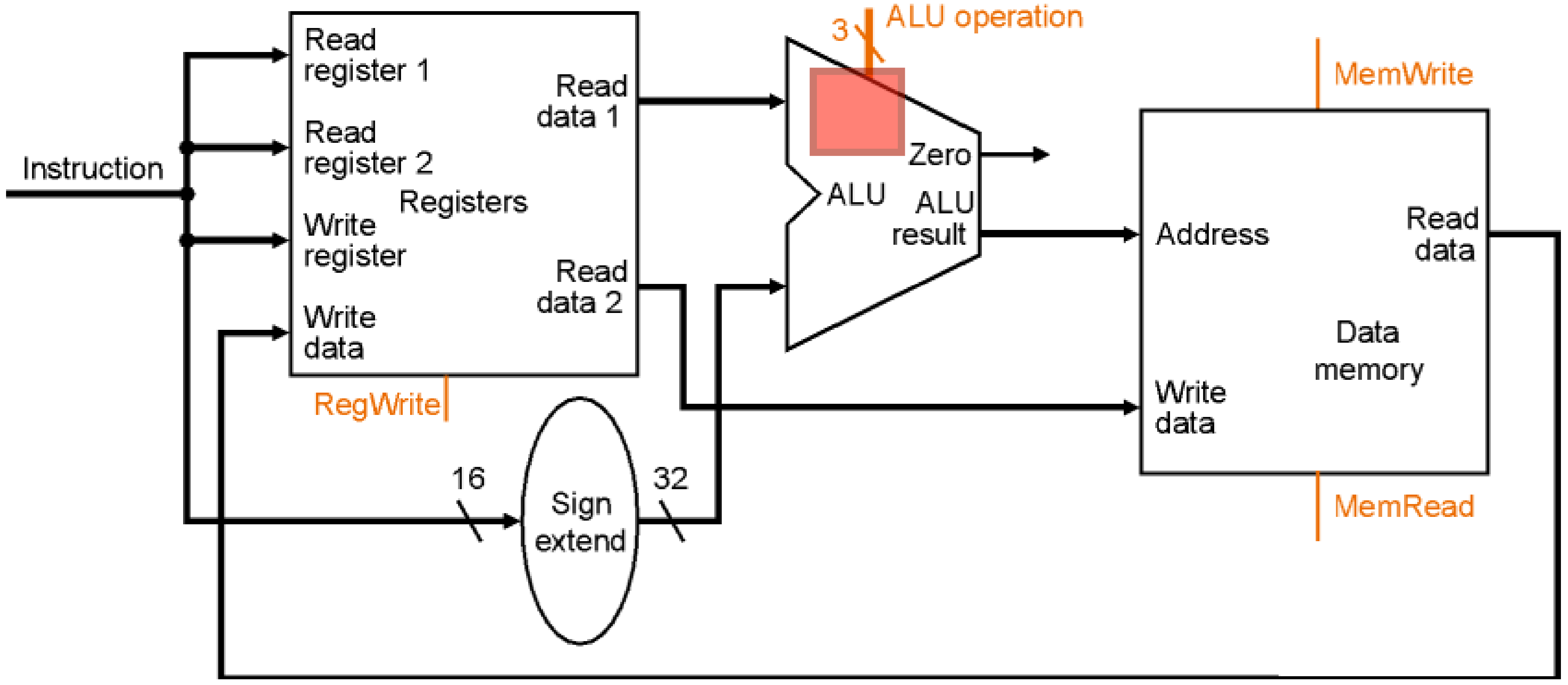

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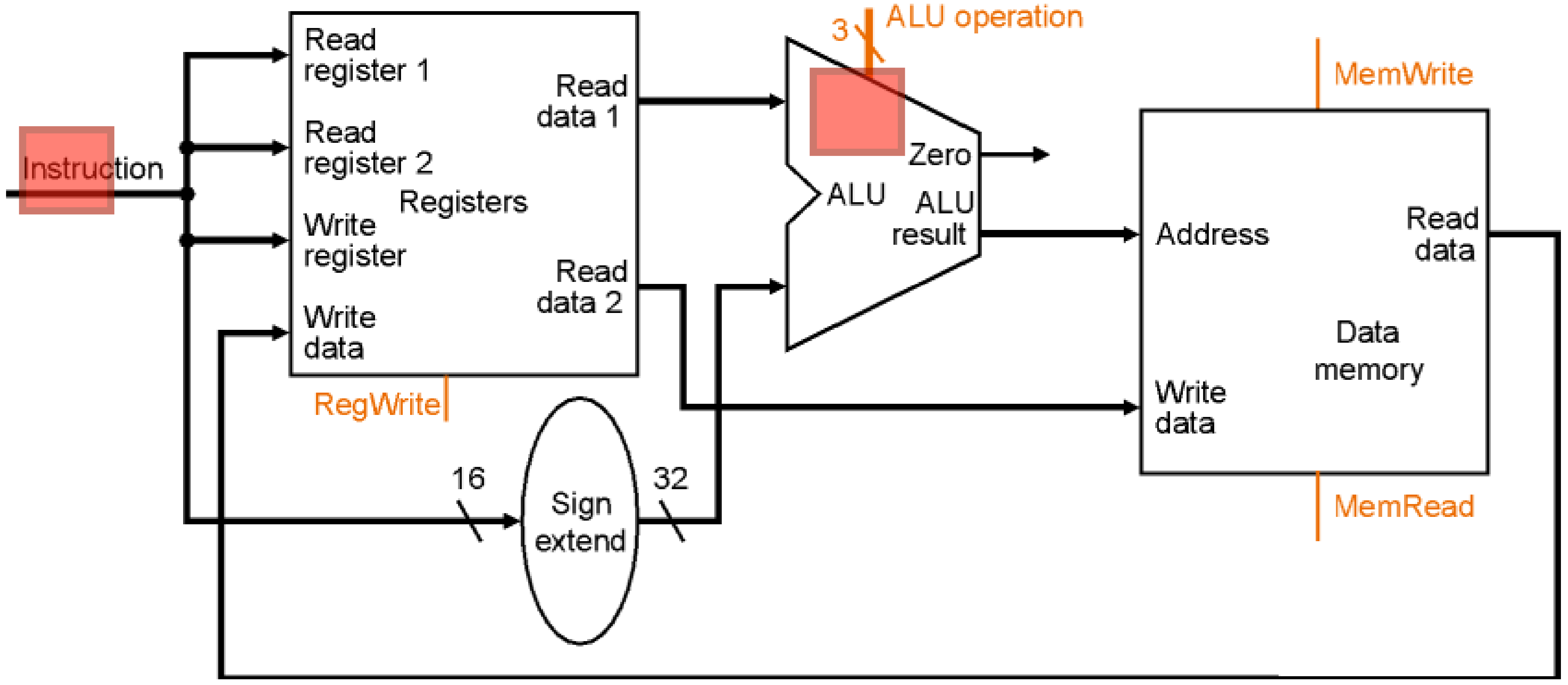

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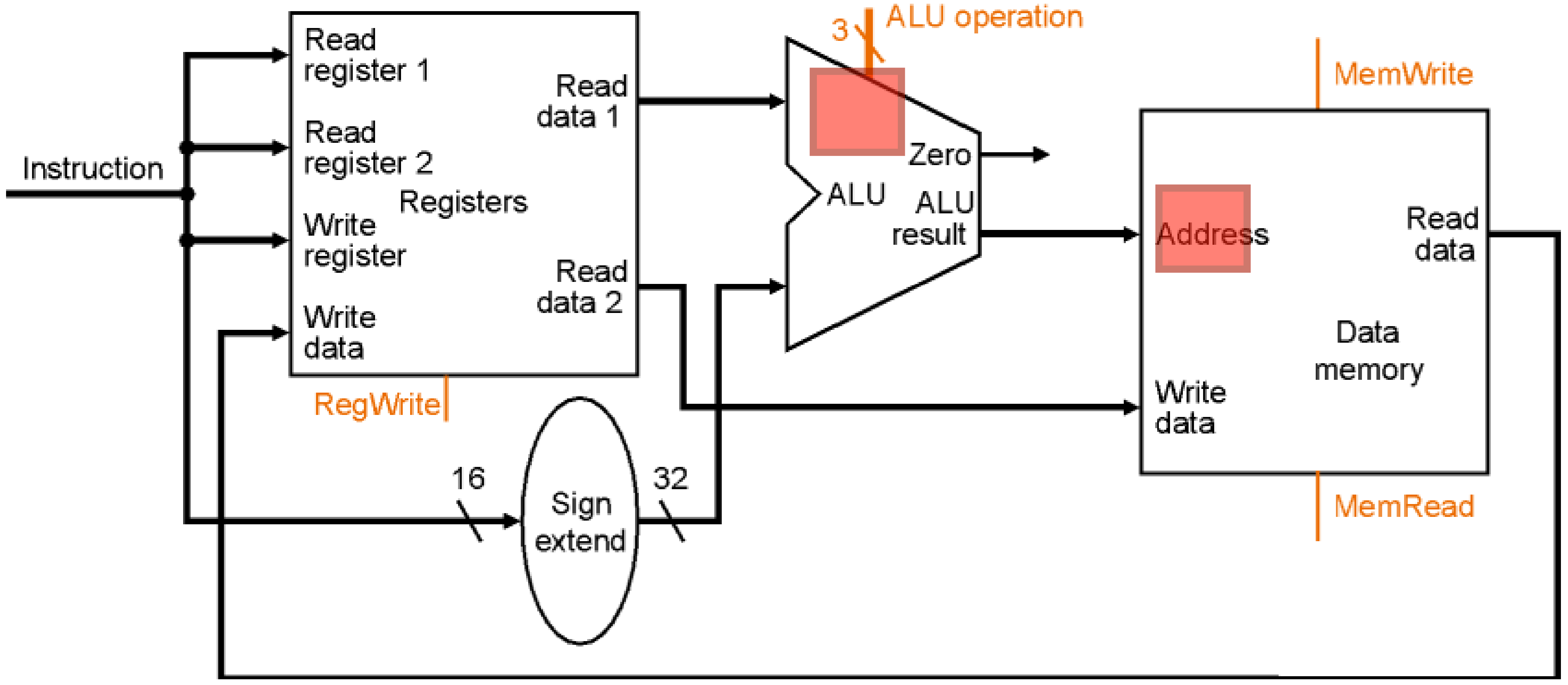

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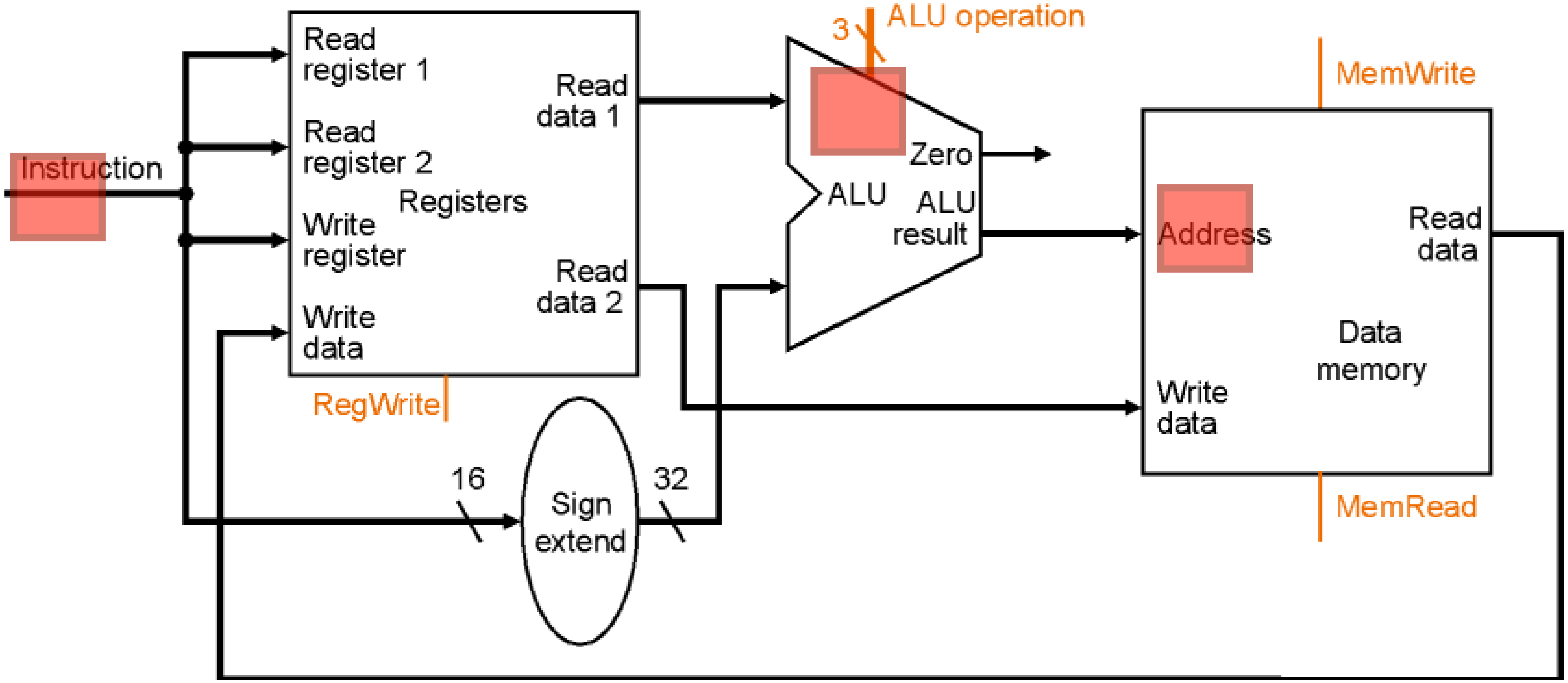

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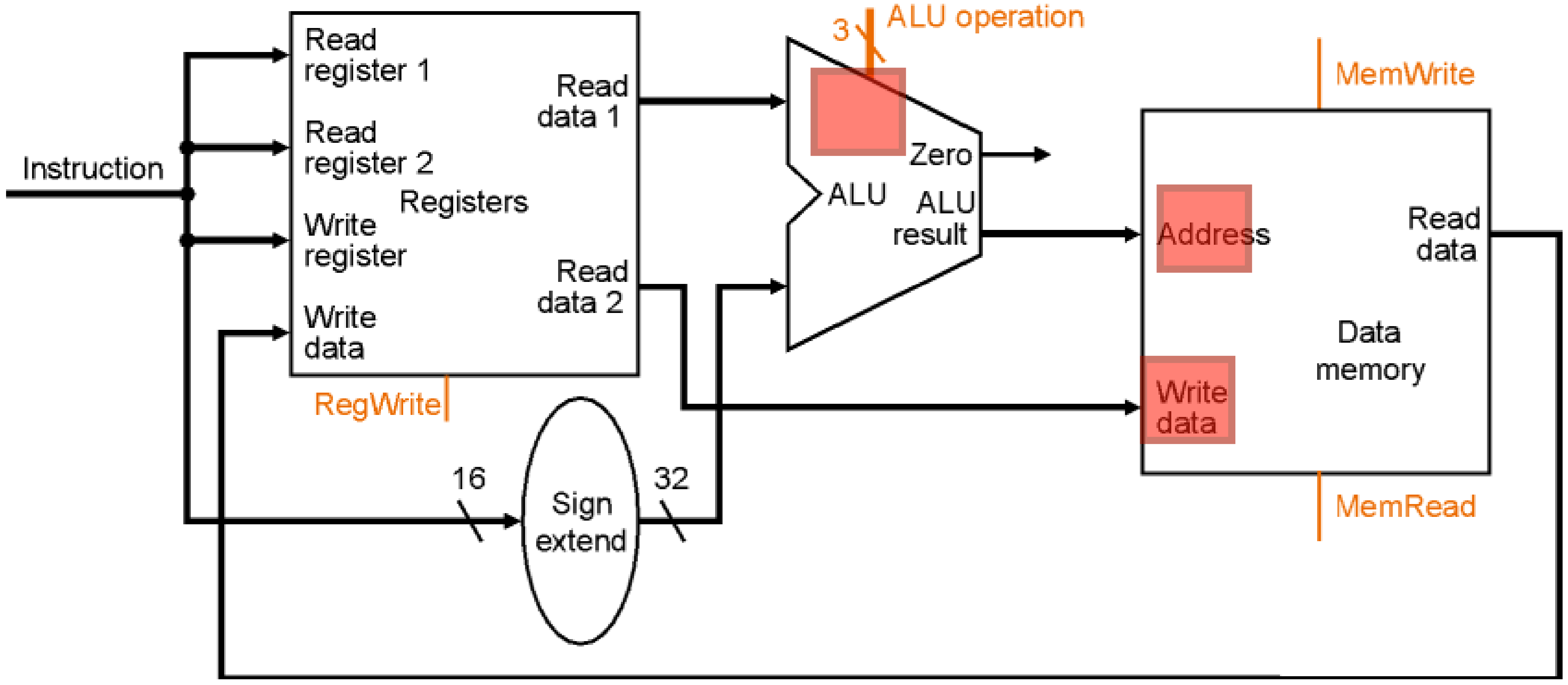

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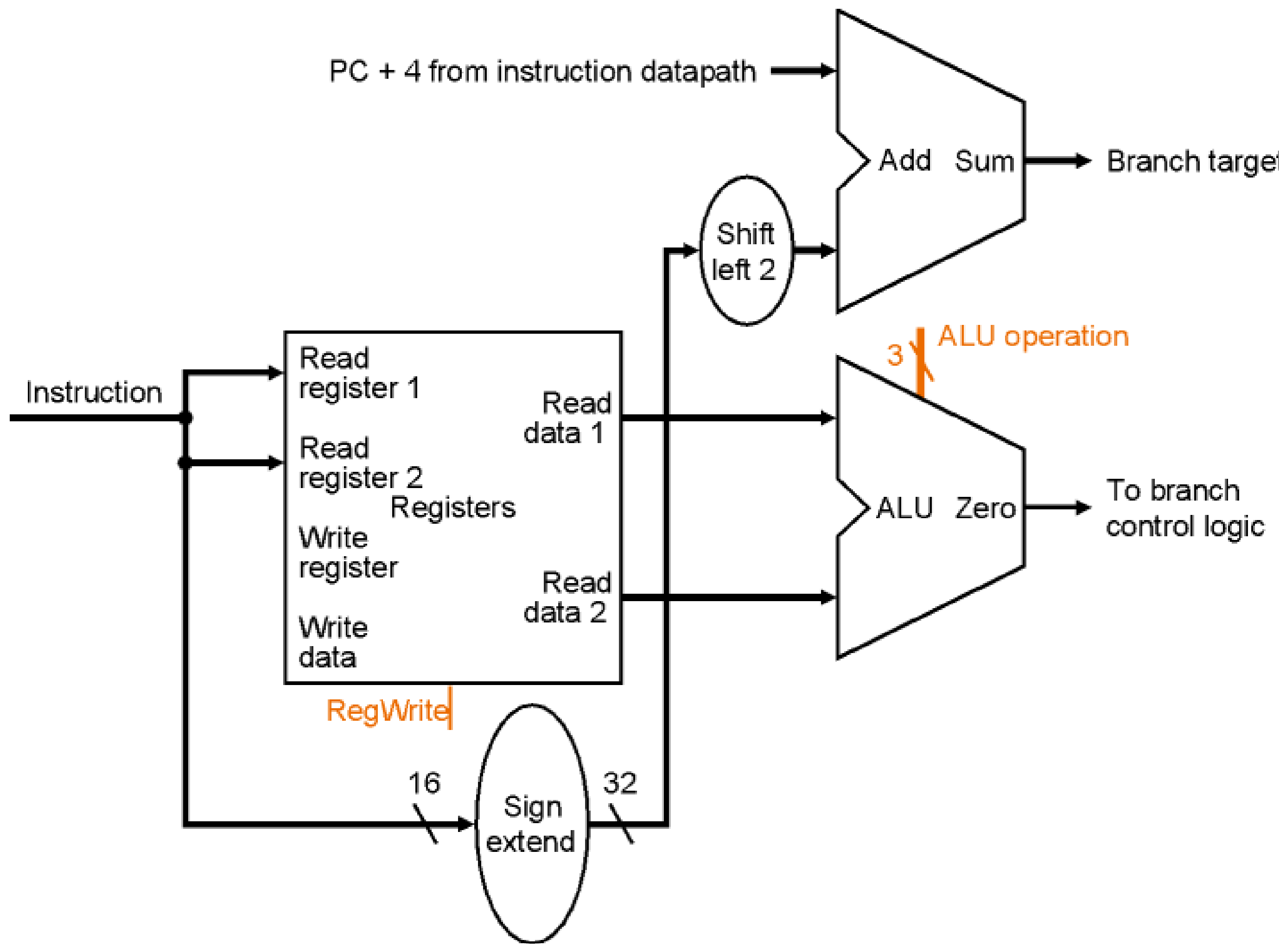

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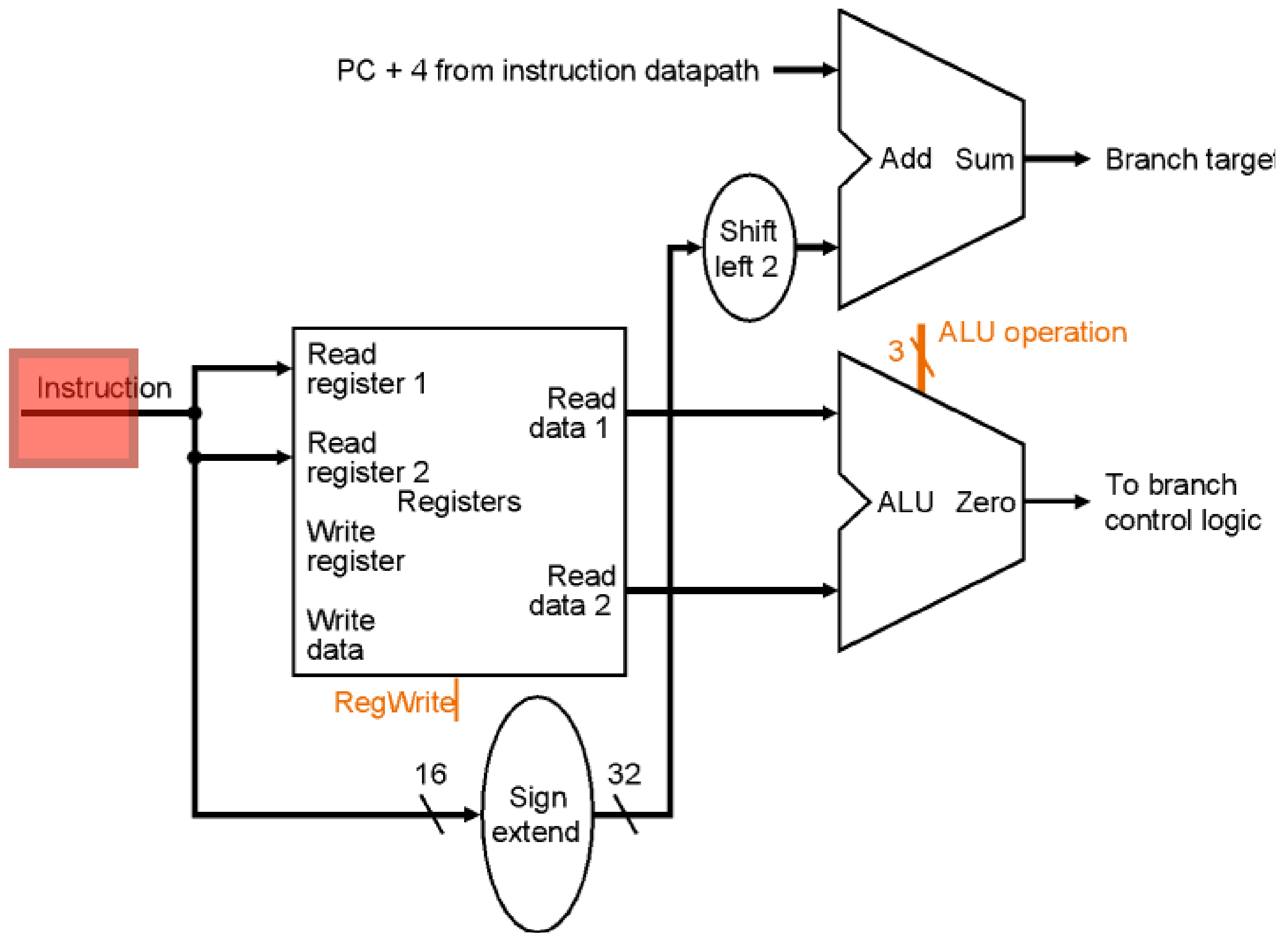

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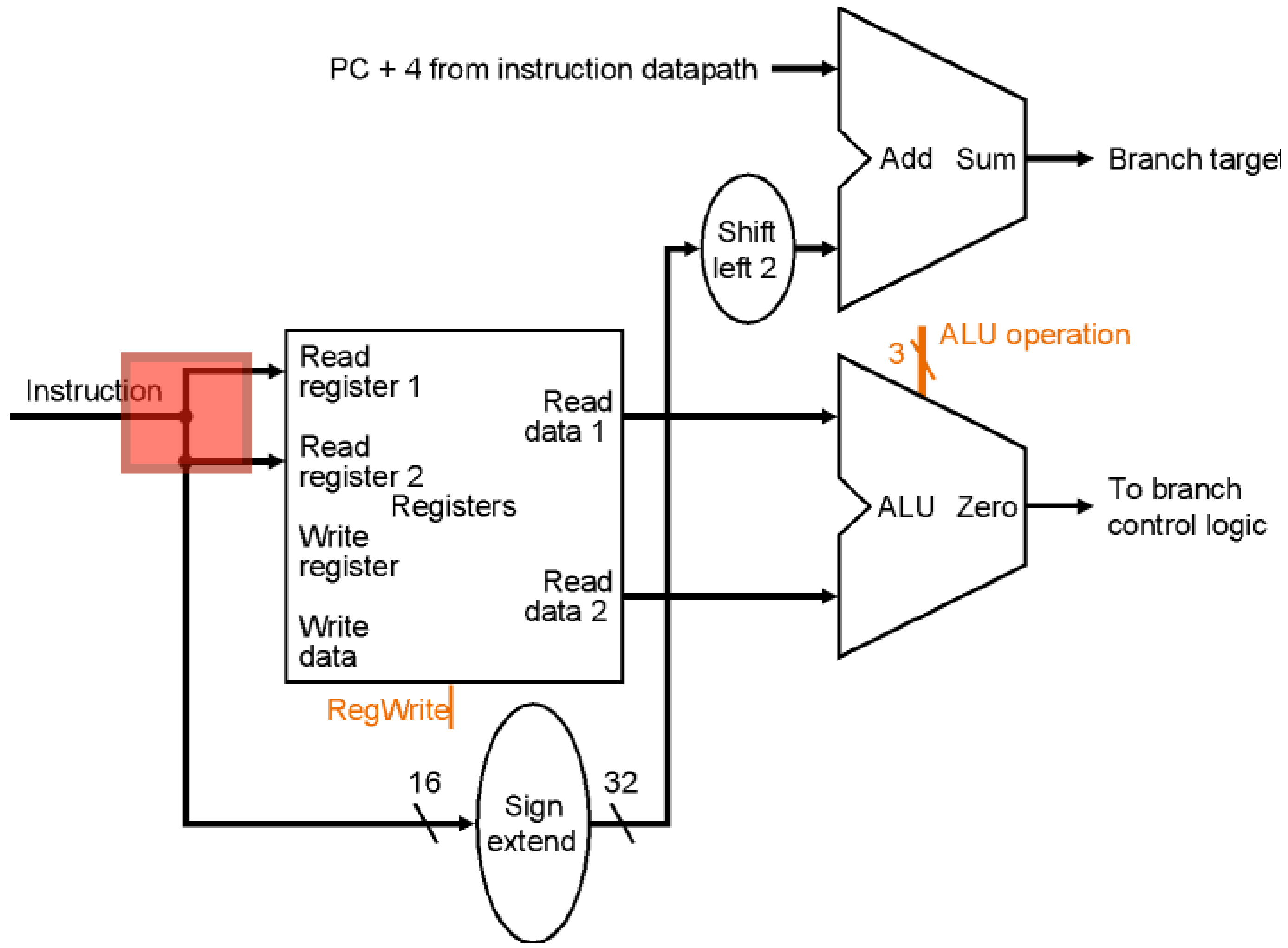

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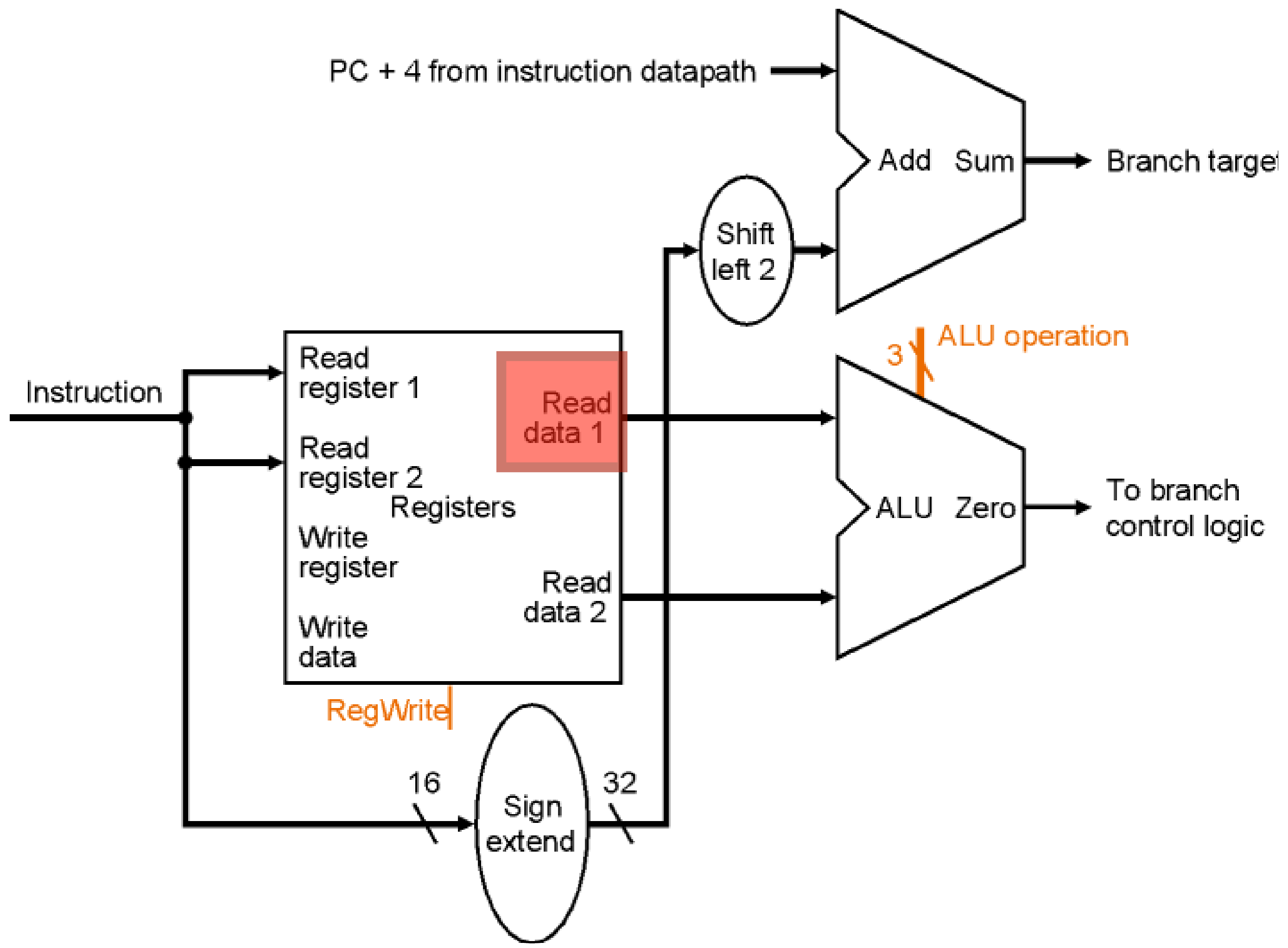

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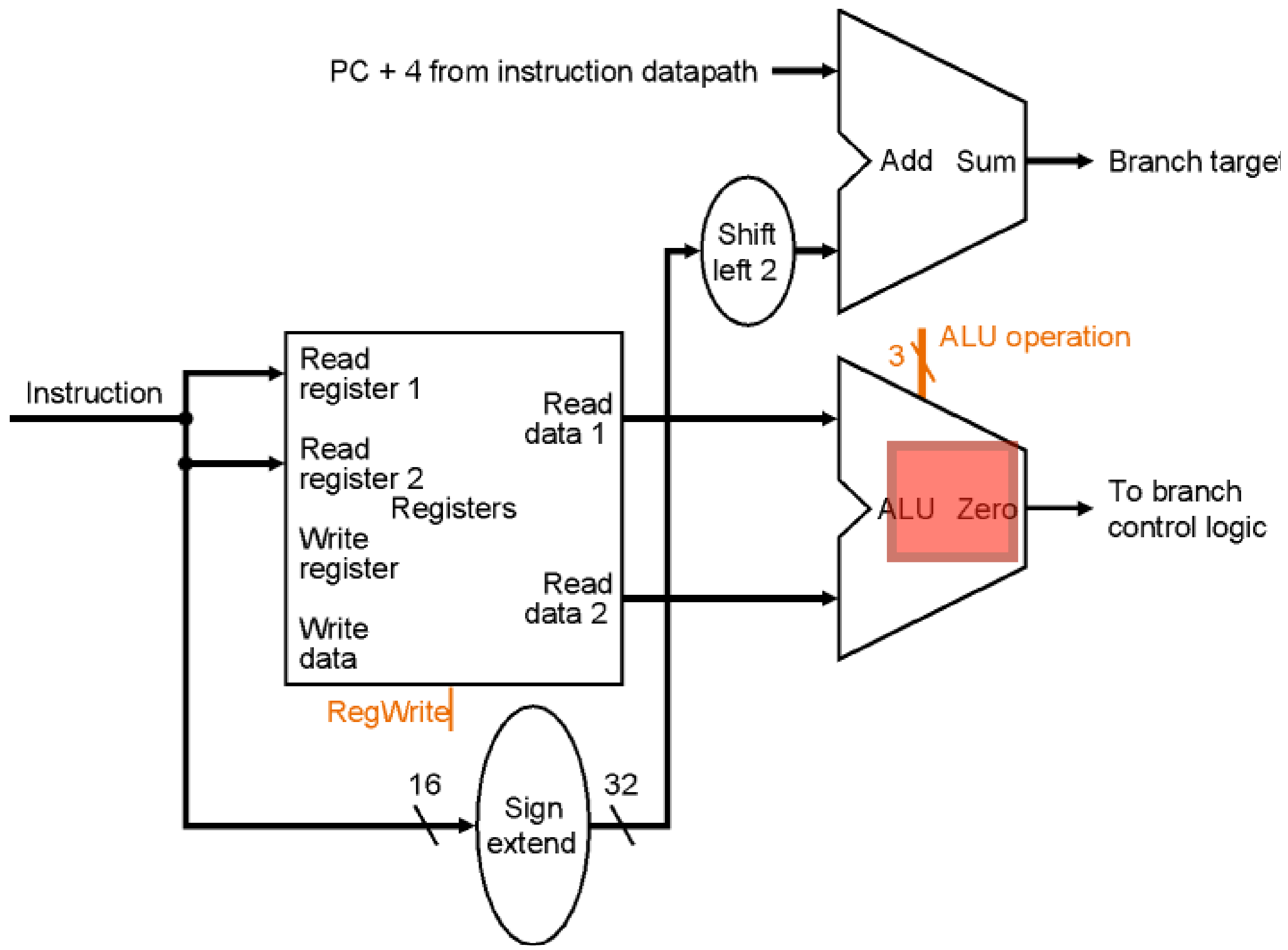

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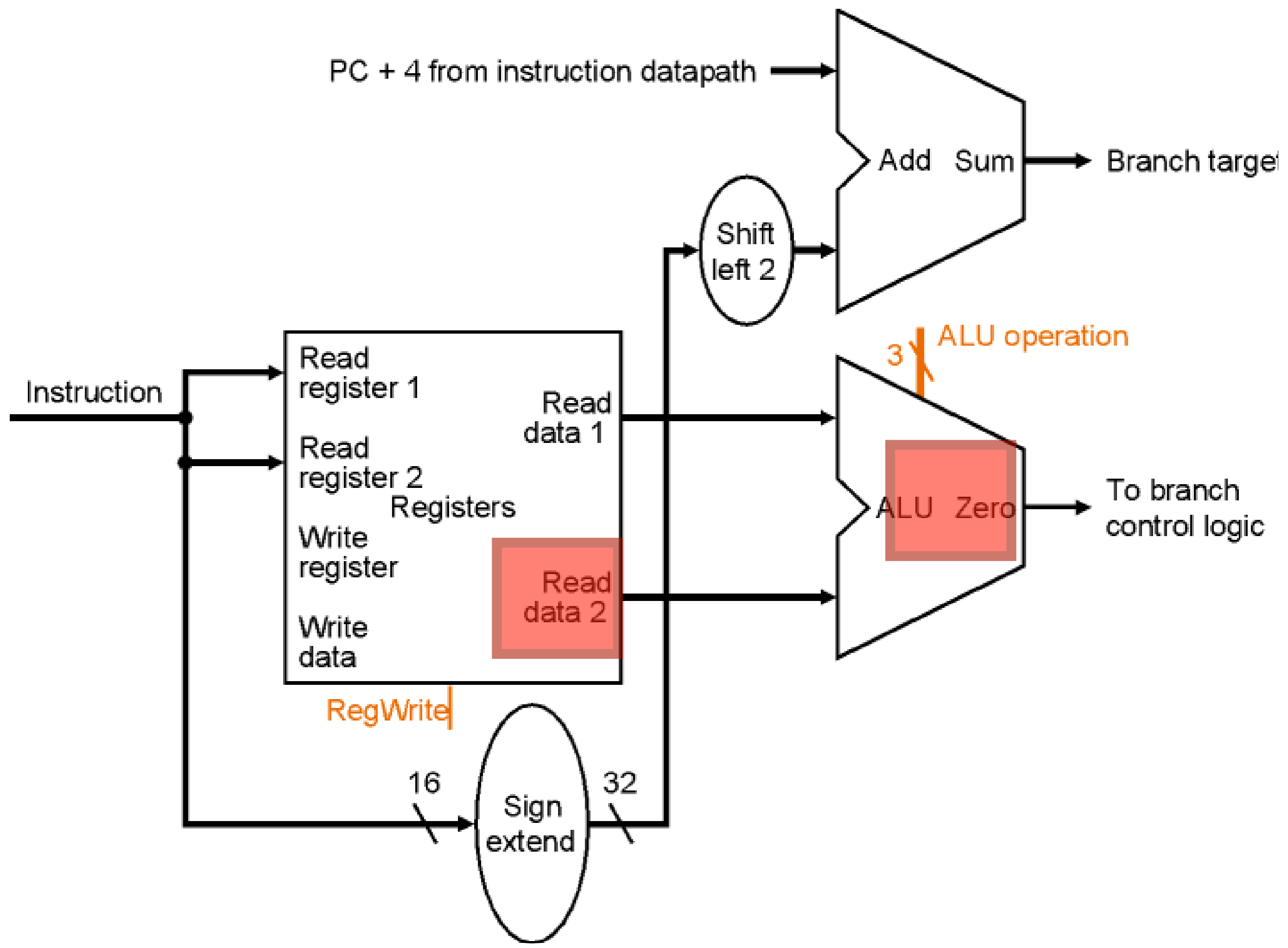

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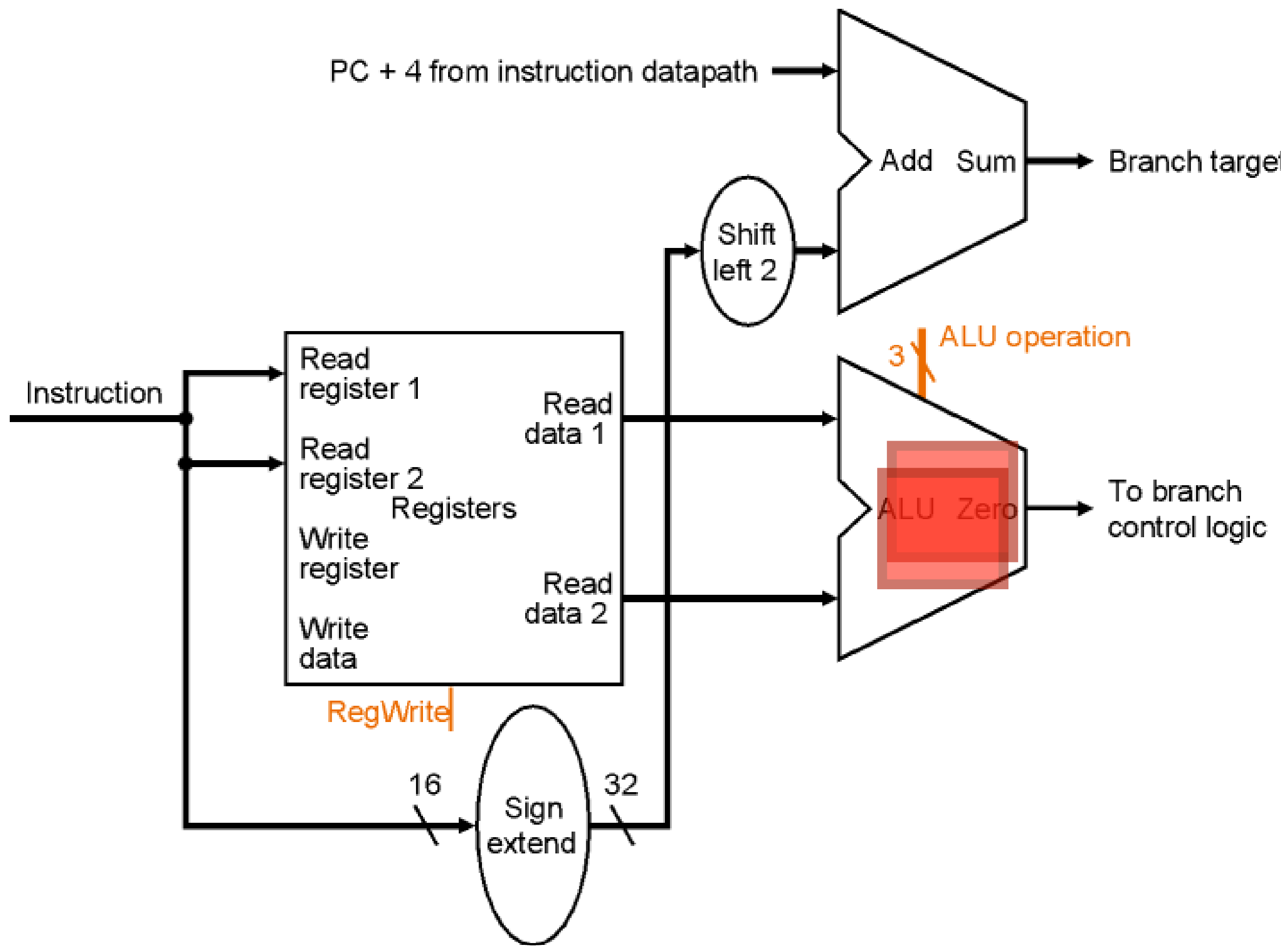

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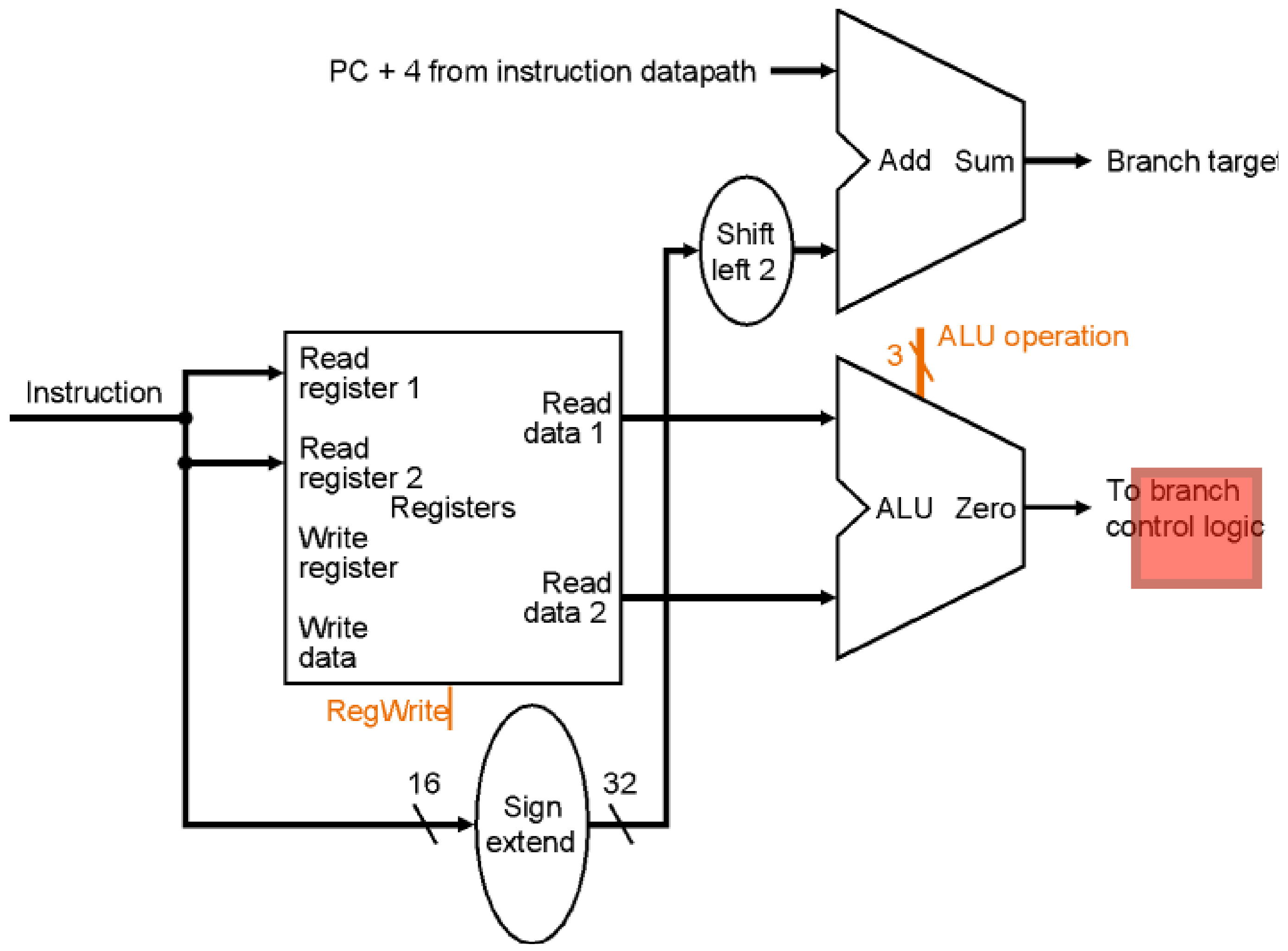

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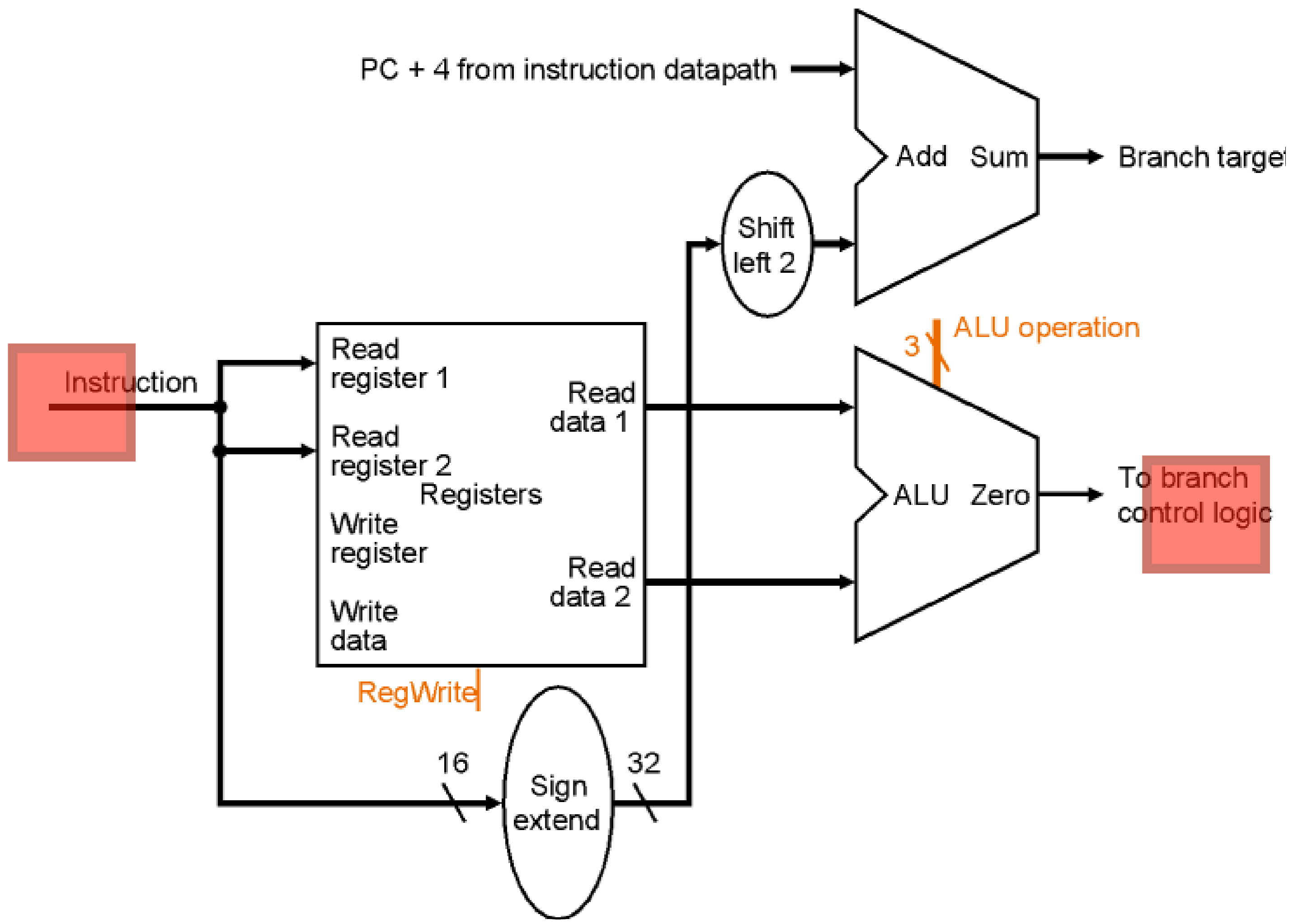

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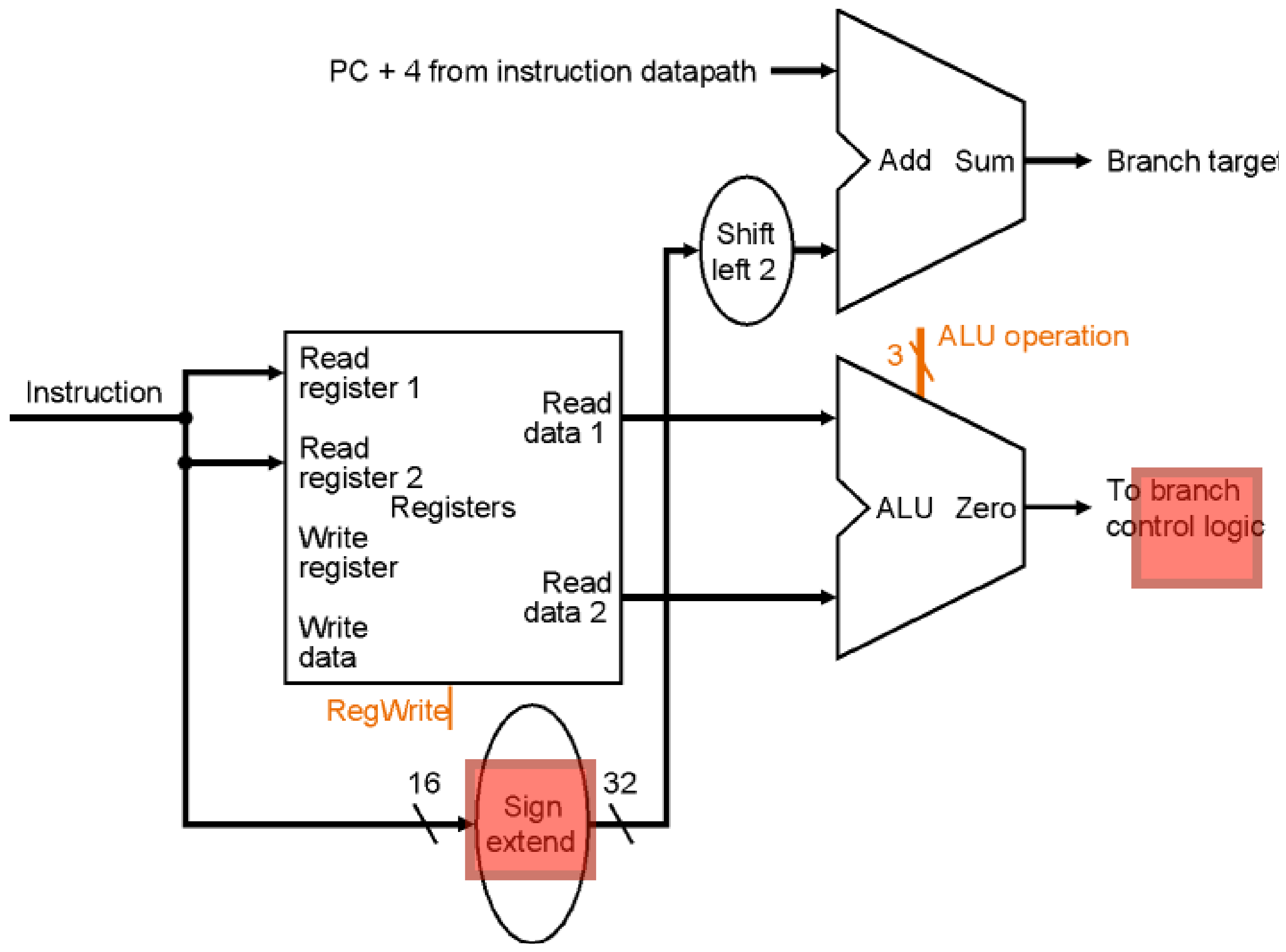

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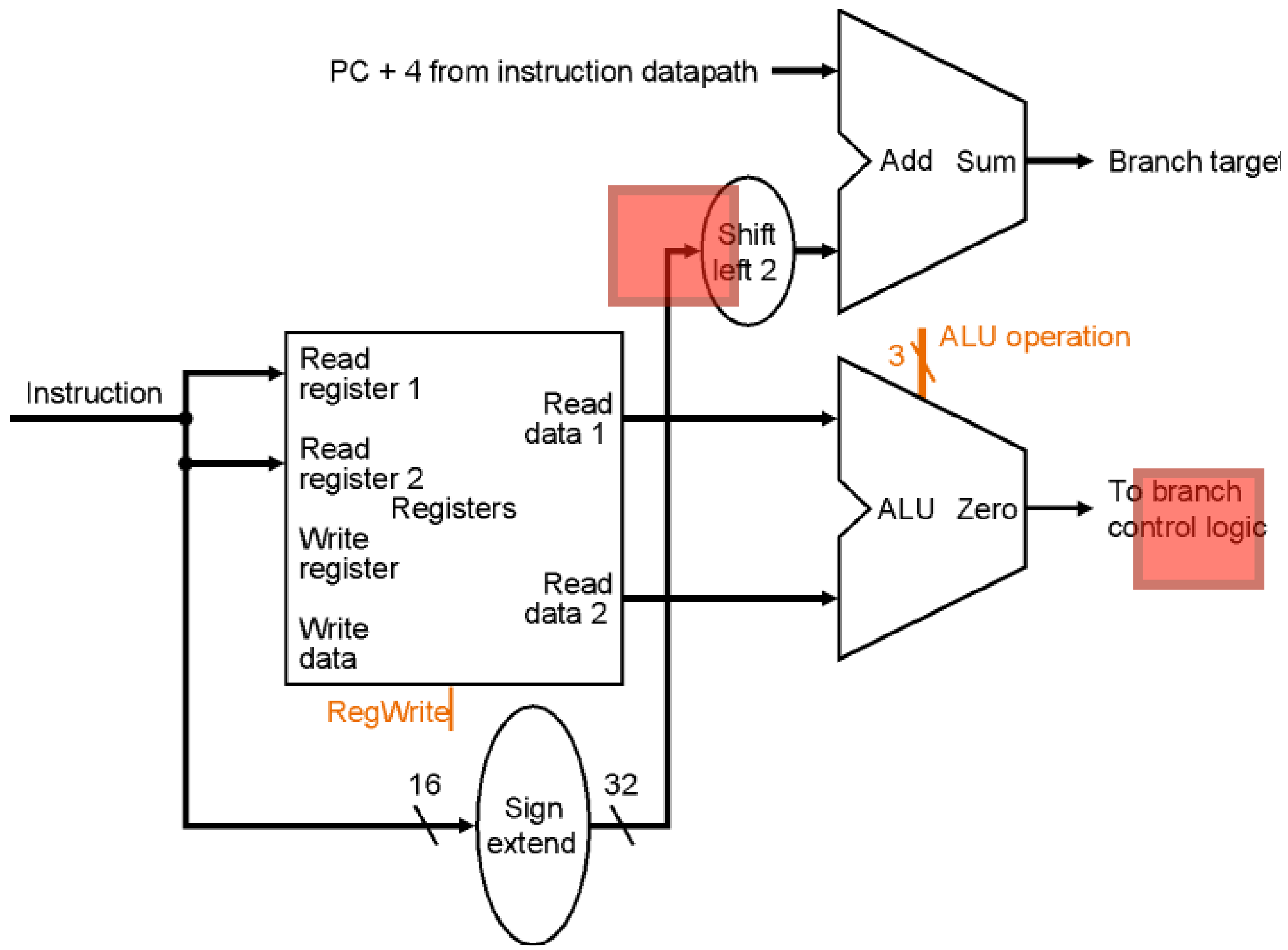

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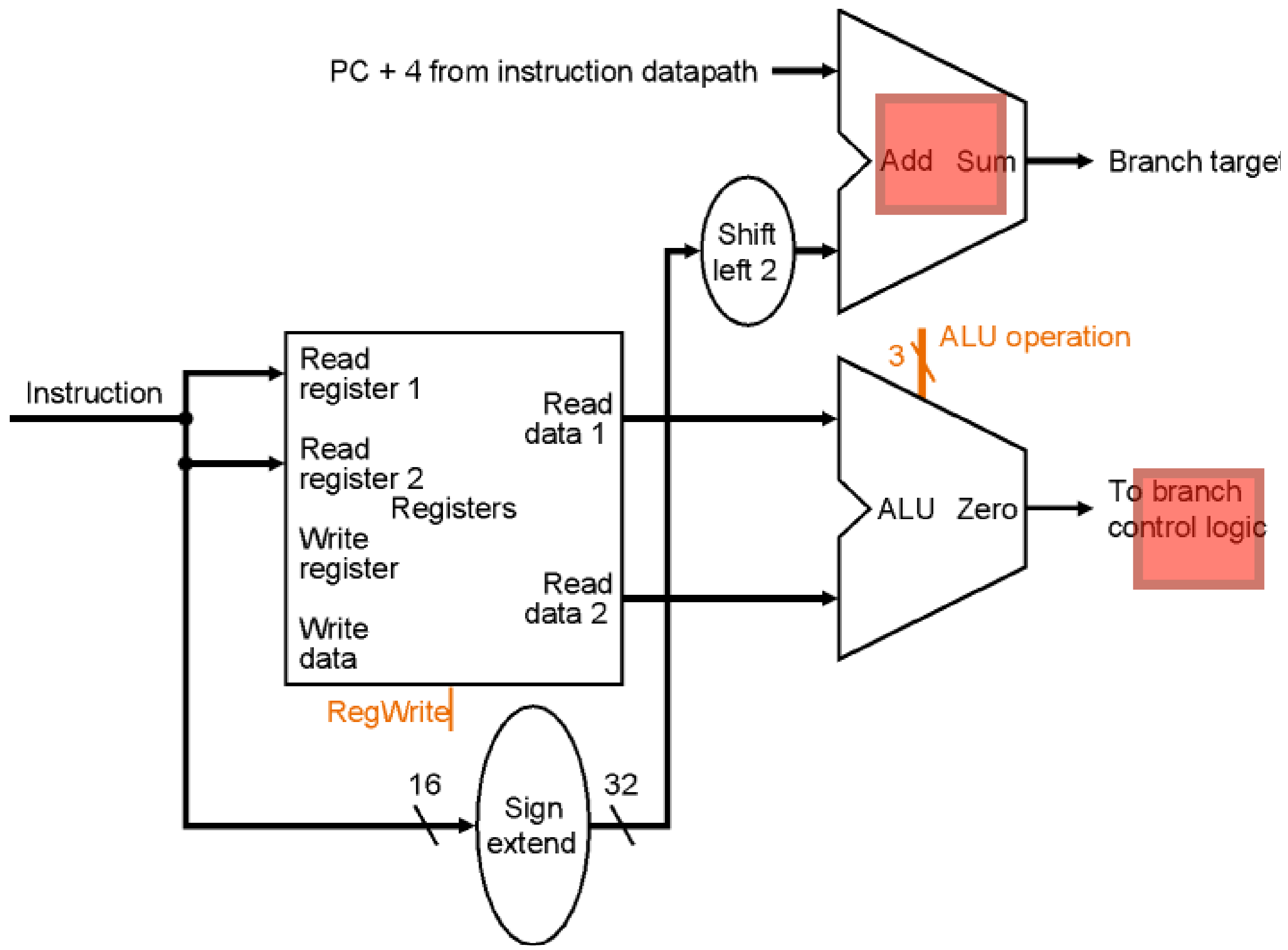

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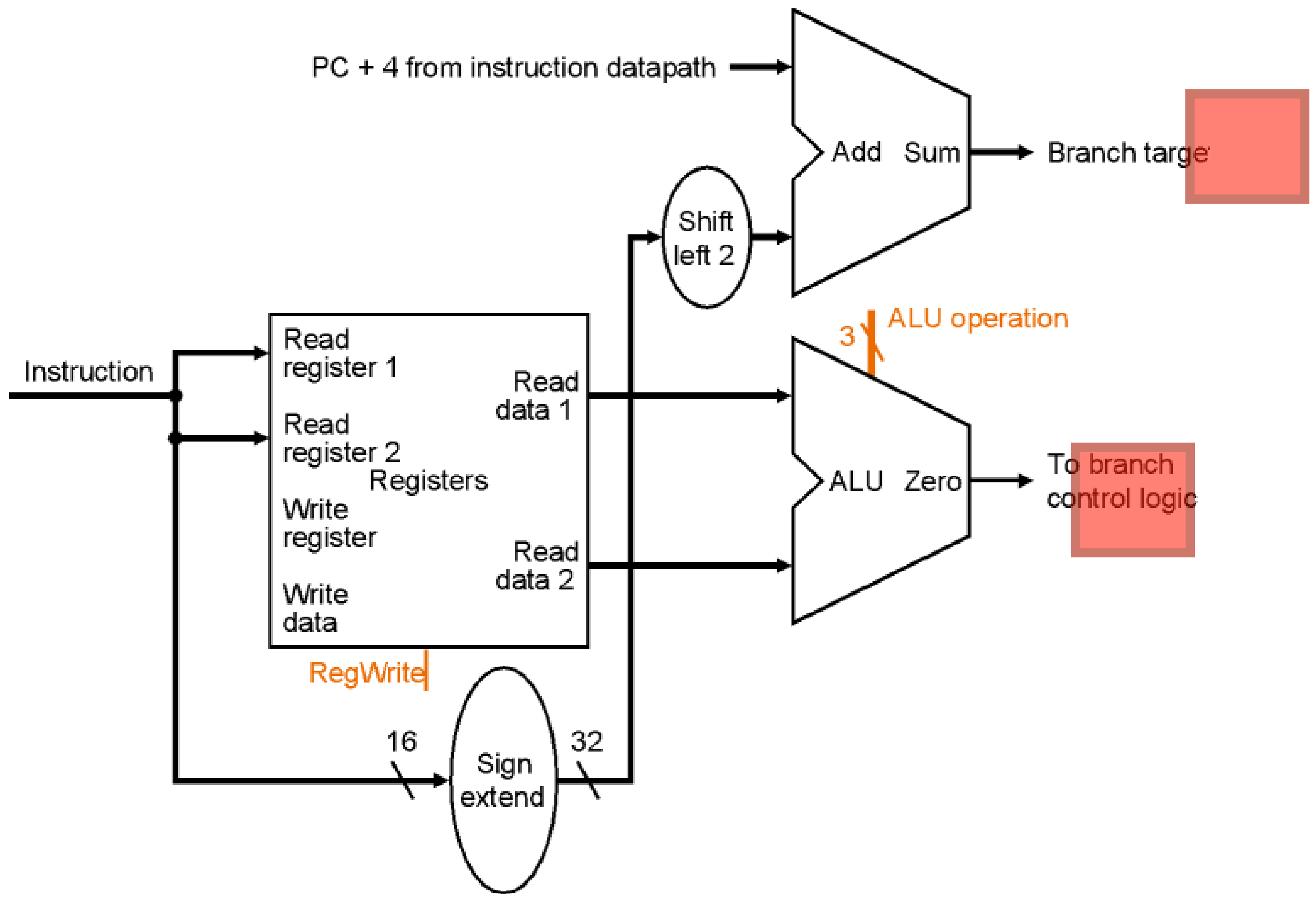

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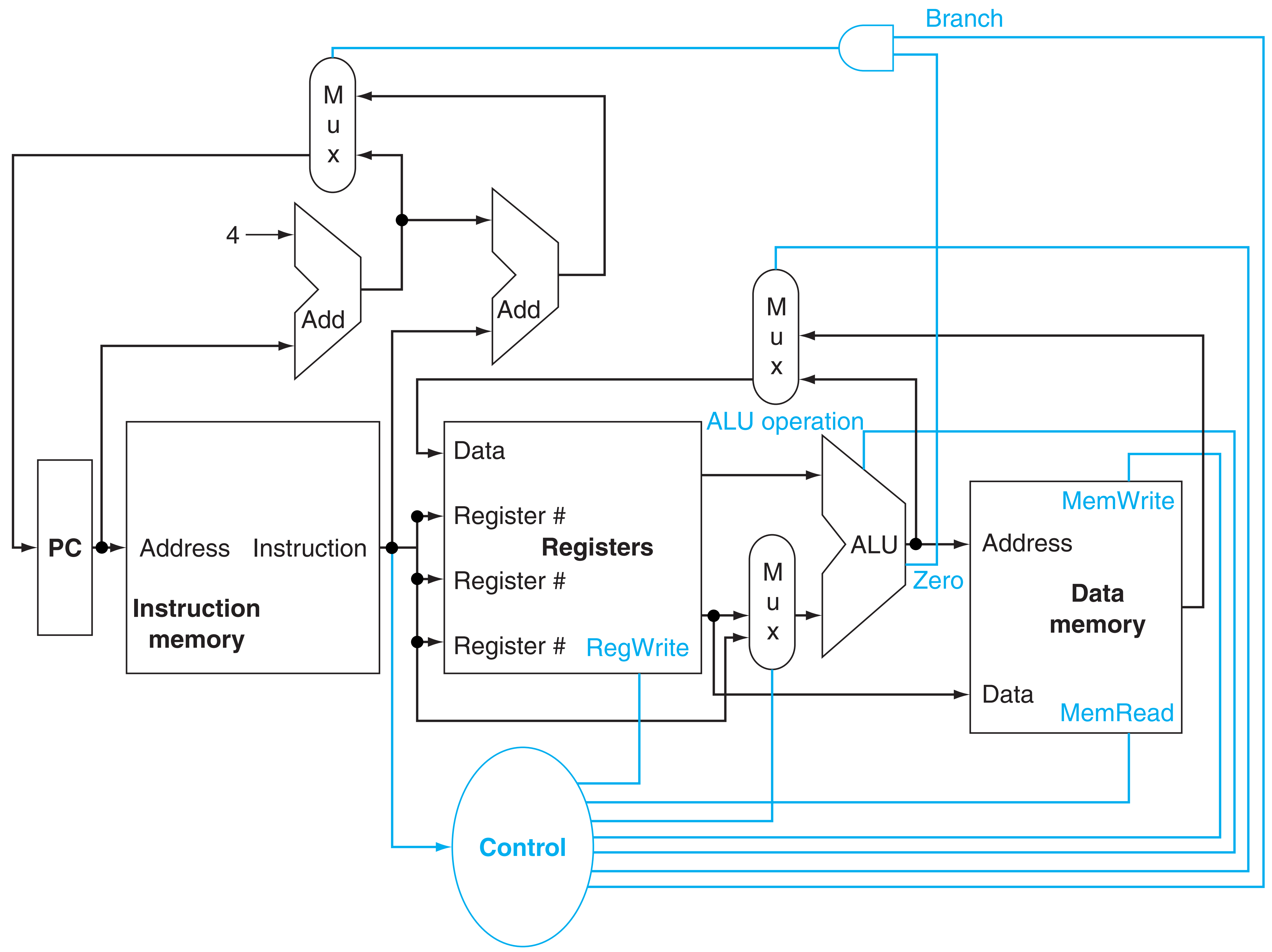

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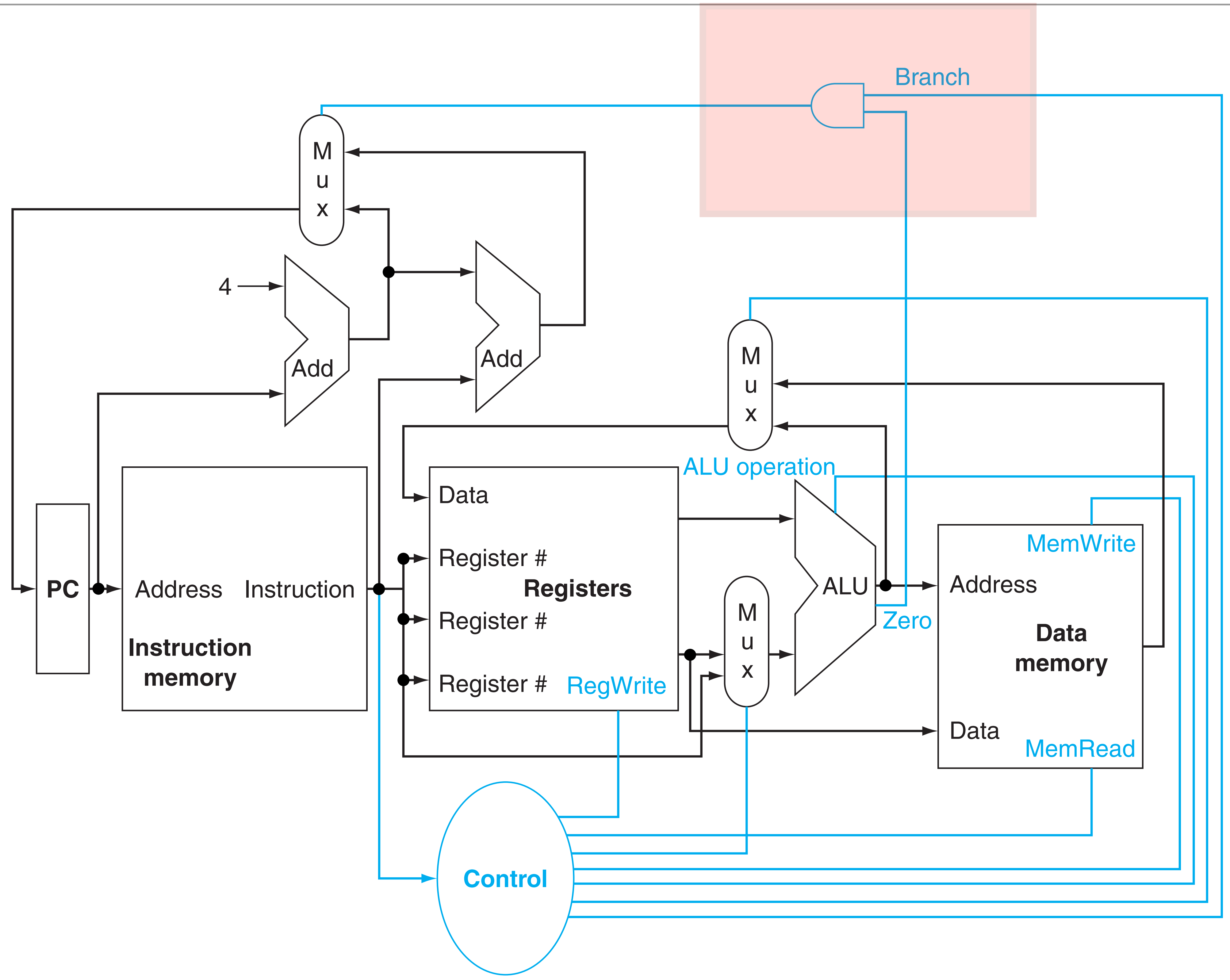

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- In theory, the PC is a 32-bit byte address into the instruction memory:
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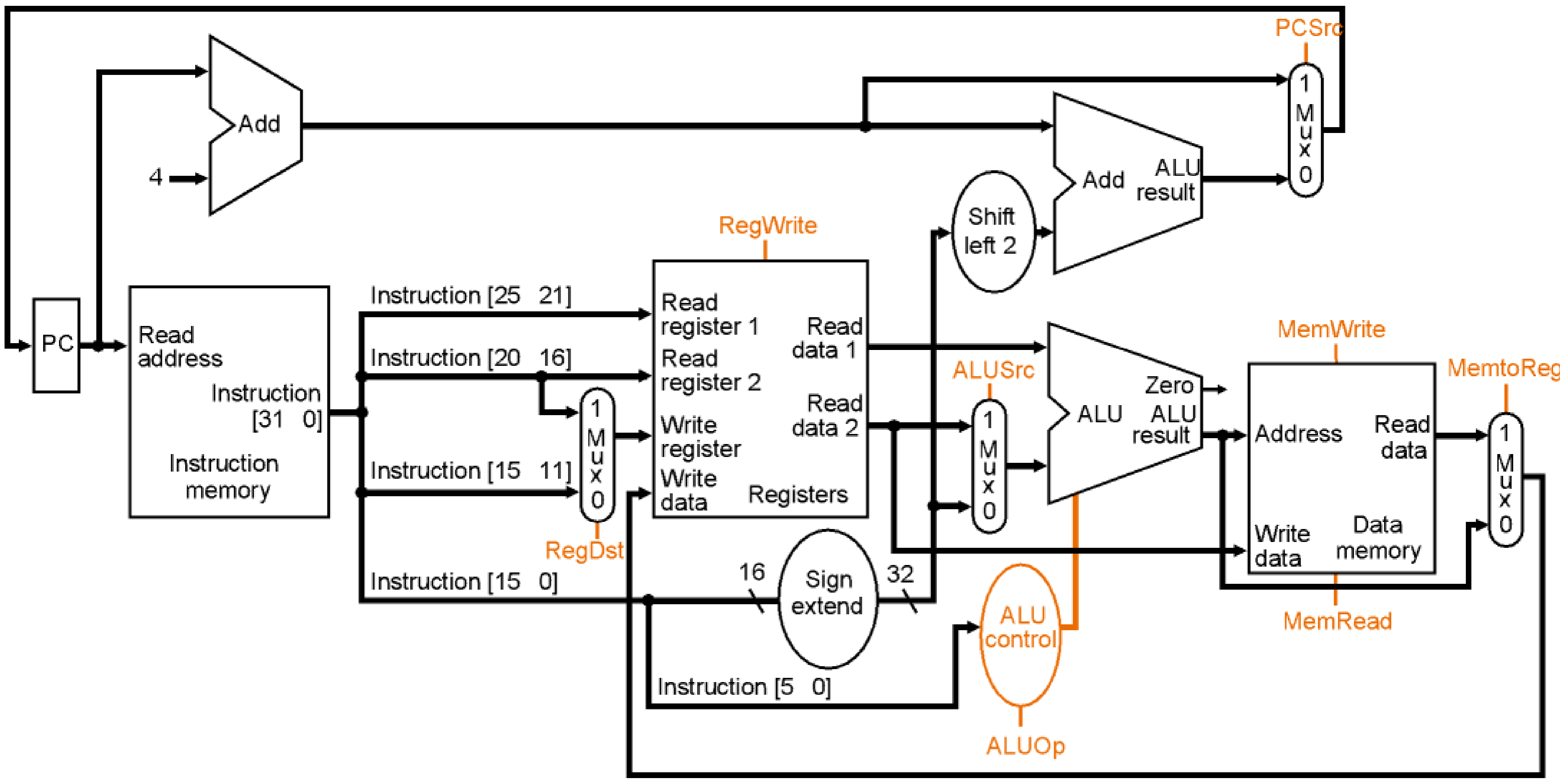
- In practice, we can simplify the hardware by using a 30-bit PC<31:2>:
  - Sequential operation: PC<31:2> = PC<31:2> + 1
  - Branch operation: PC<31:2> = PC<31:2> + 1 + SignExt[Imm16]
  - In either case: Instruction Memory Address = PC<31:2> concat "00"

Putting it All Together: A Single Cycle Datapath

- We have everything except control signals



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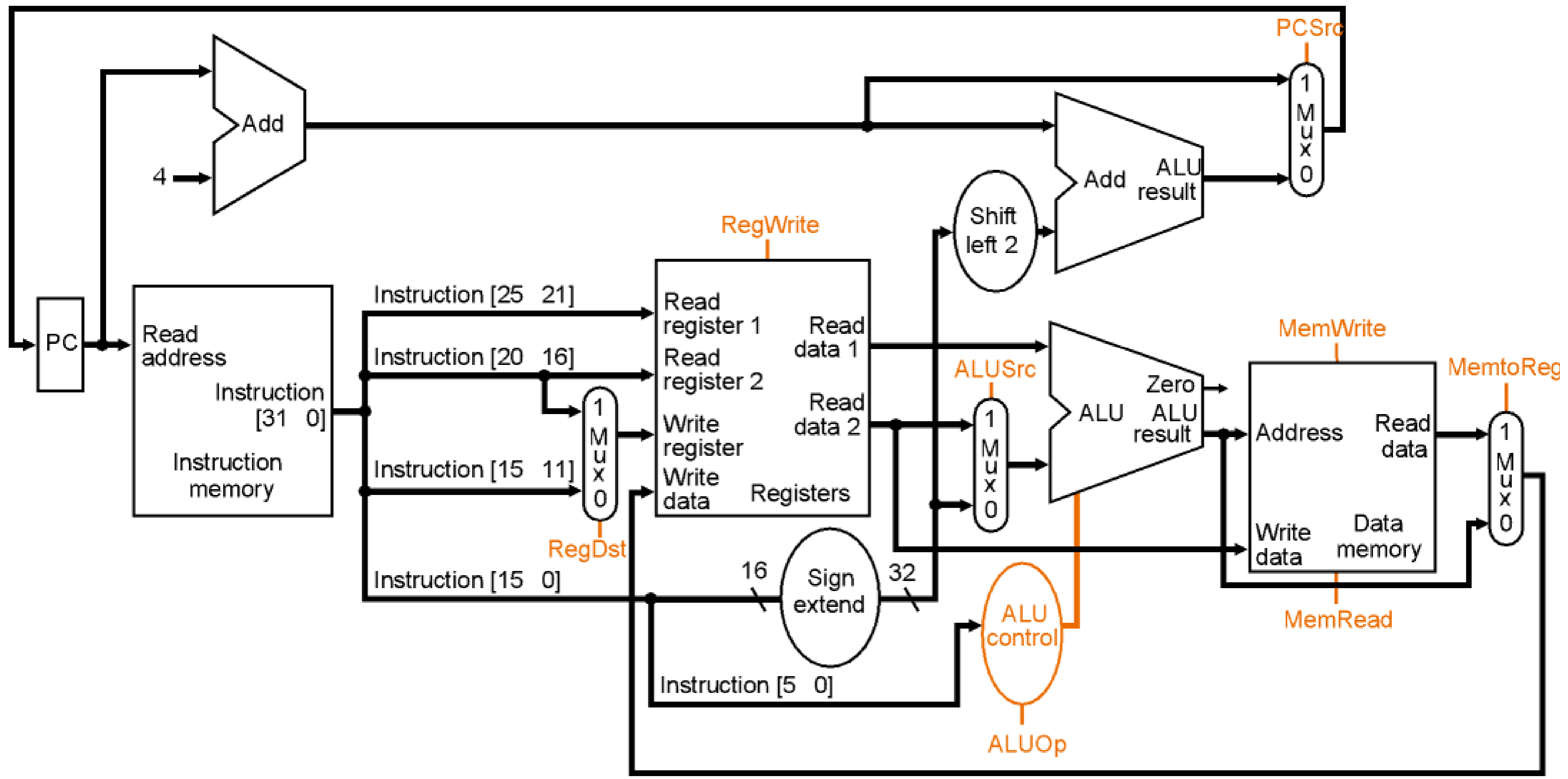

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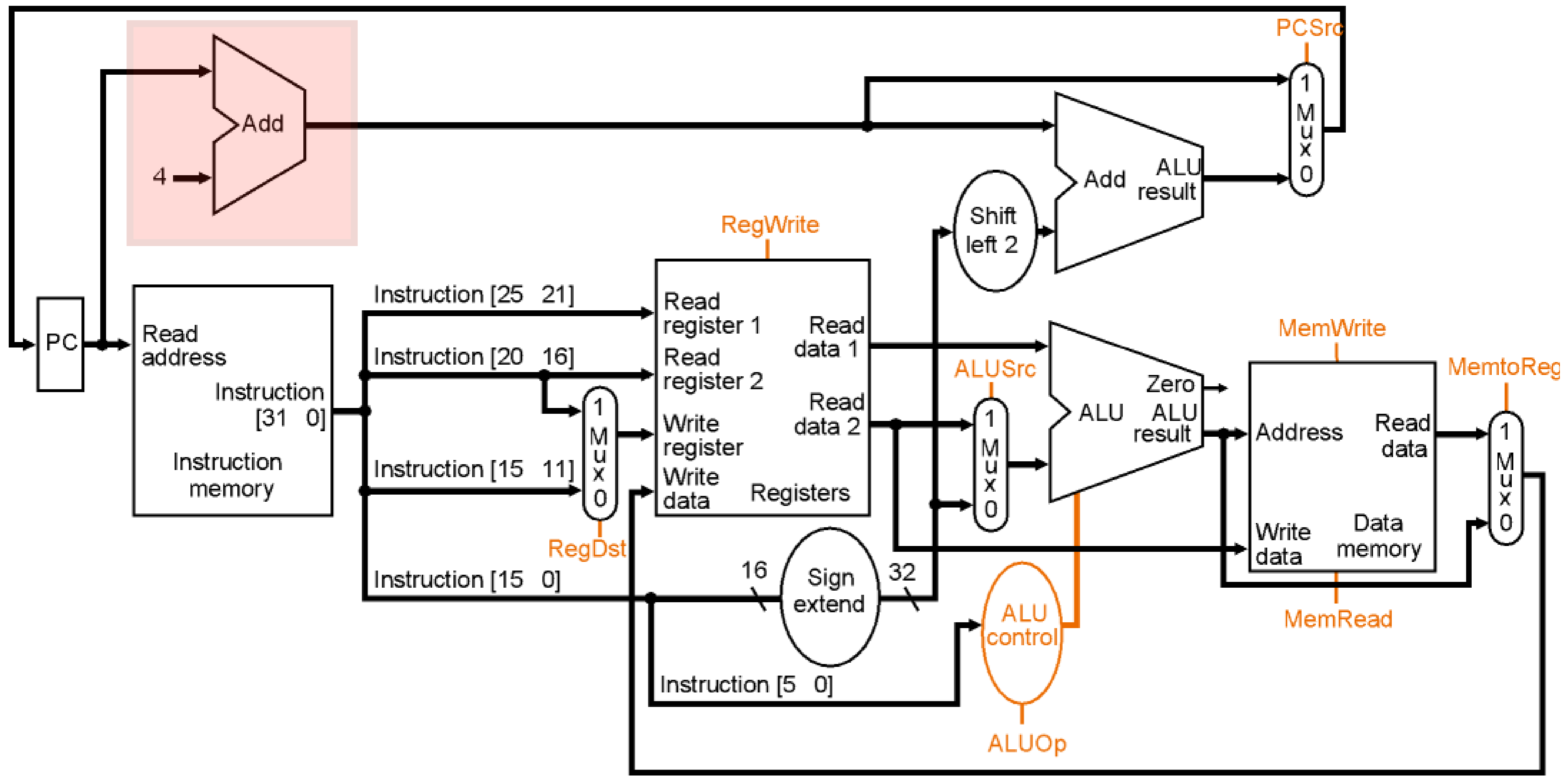

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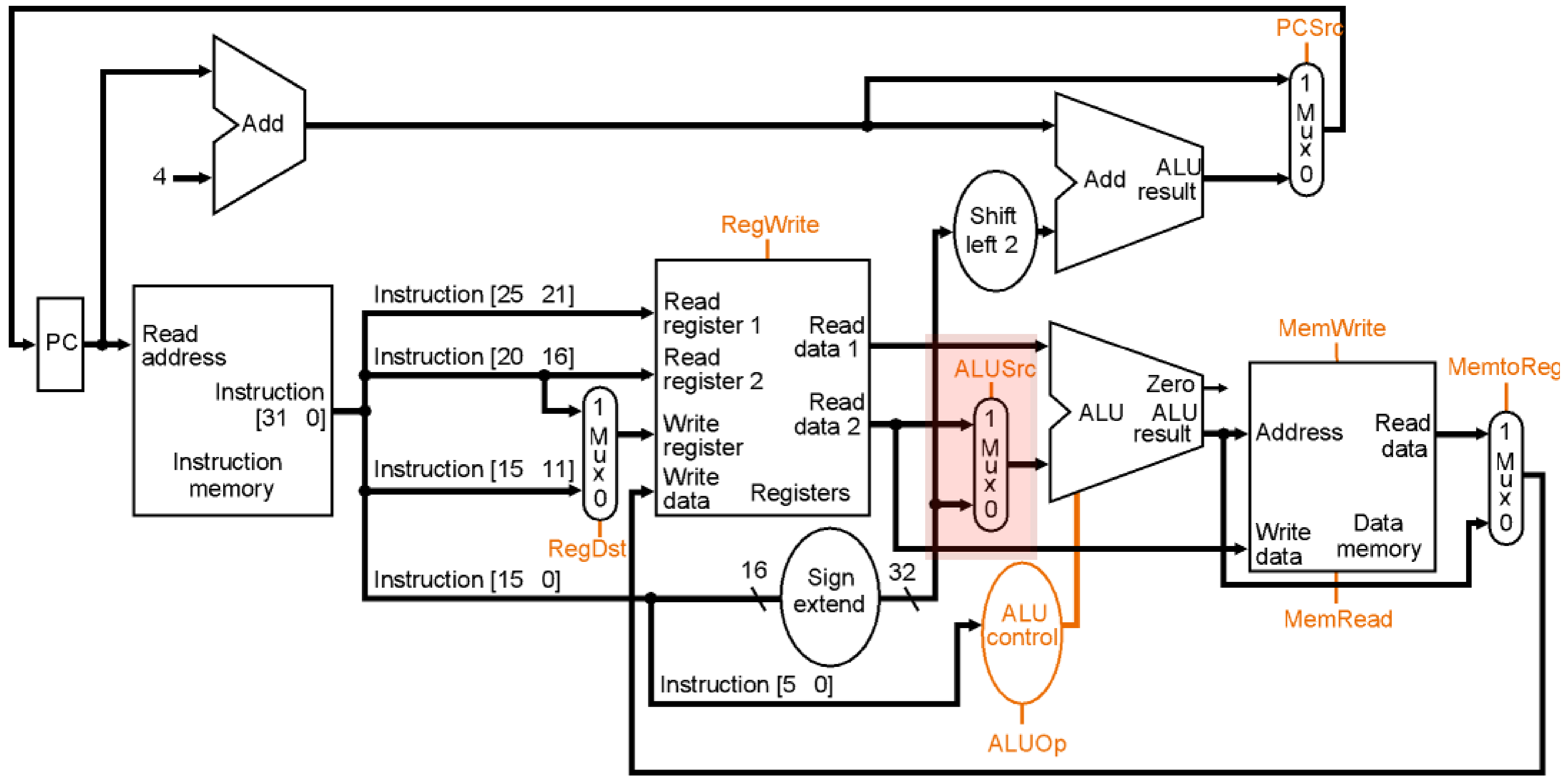

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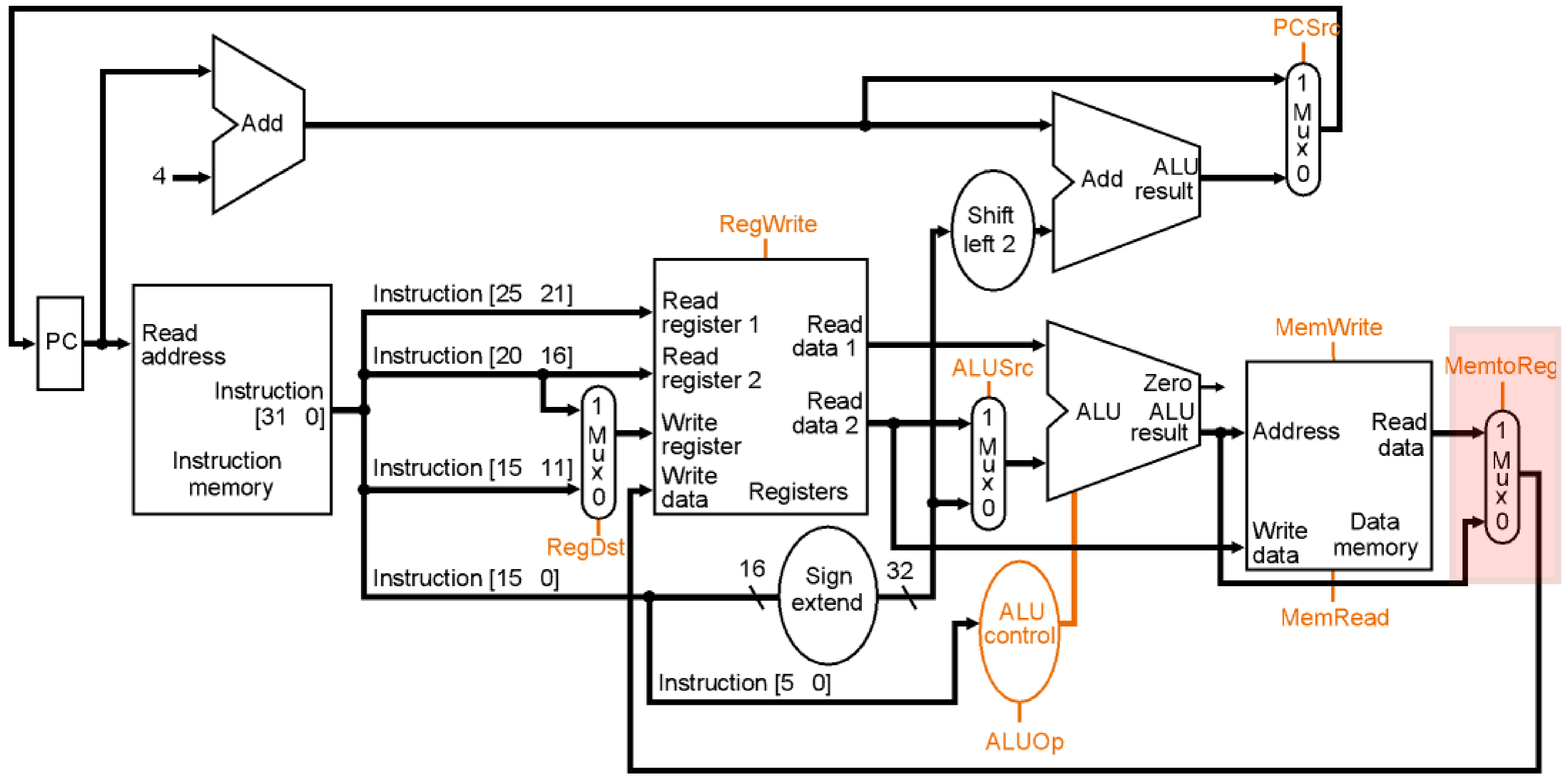

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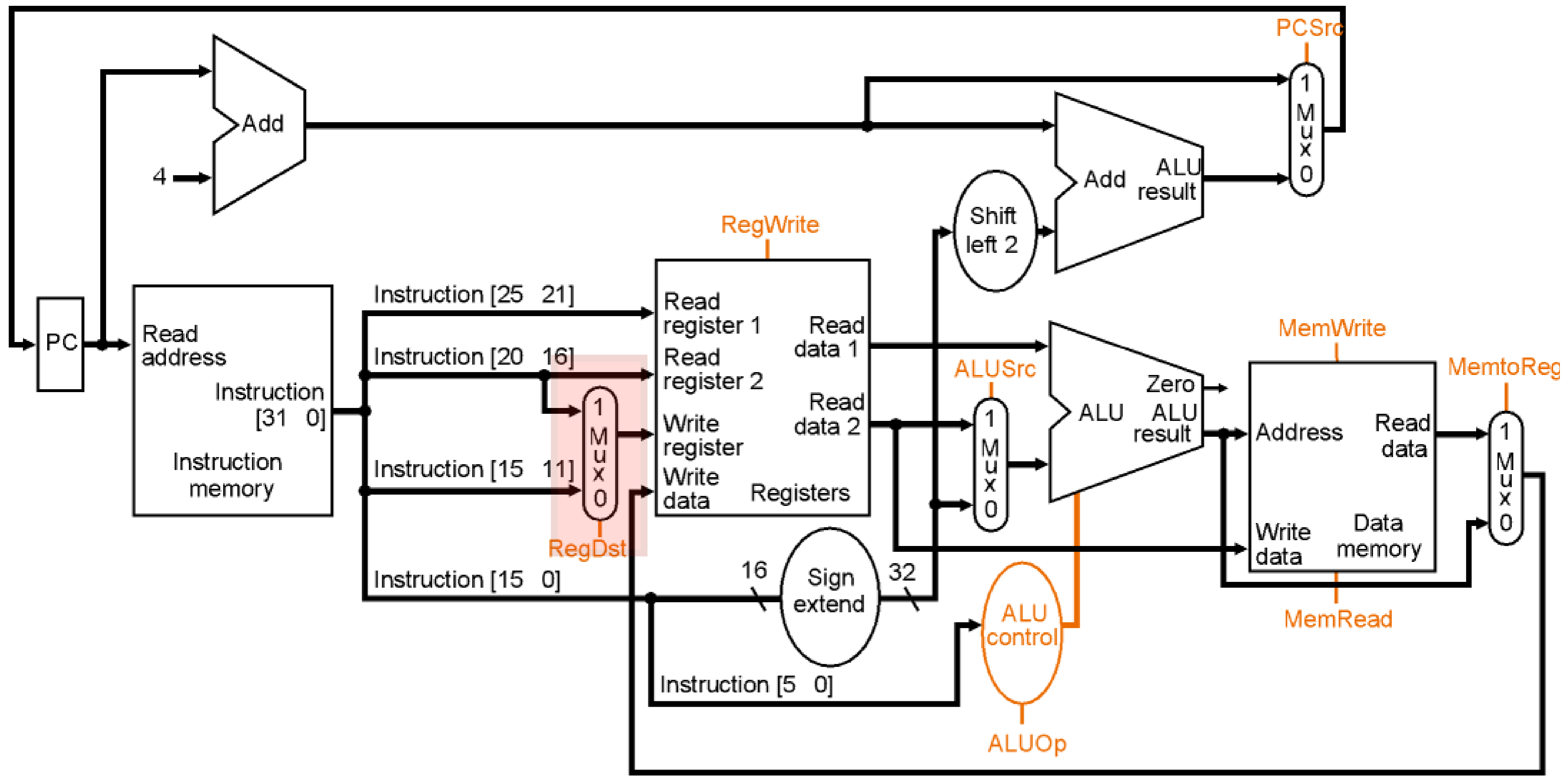

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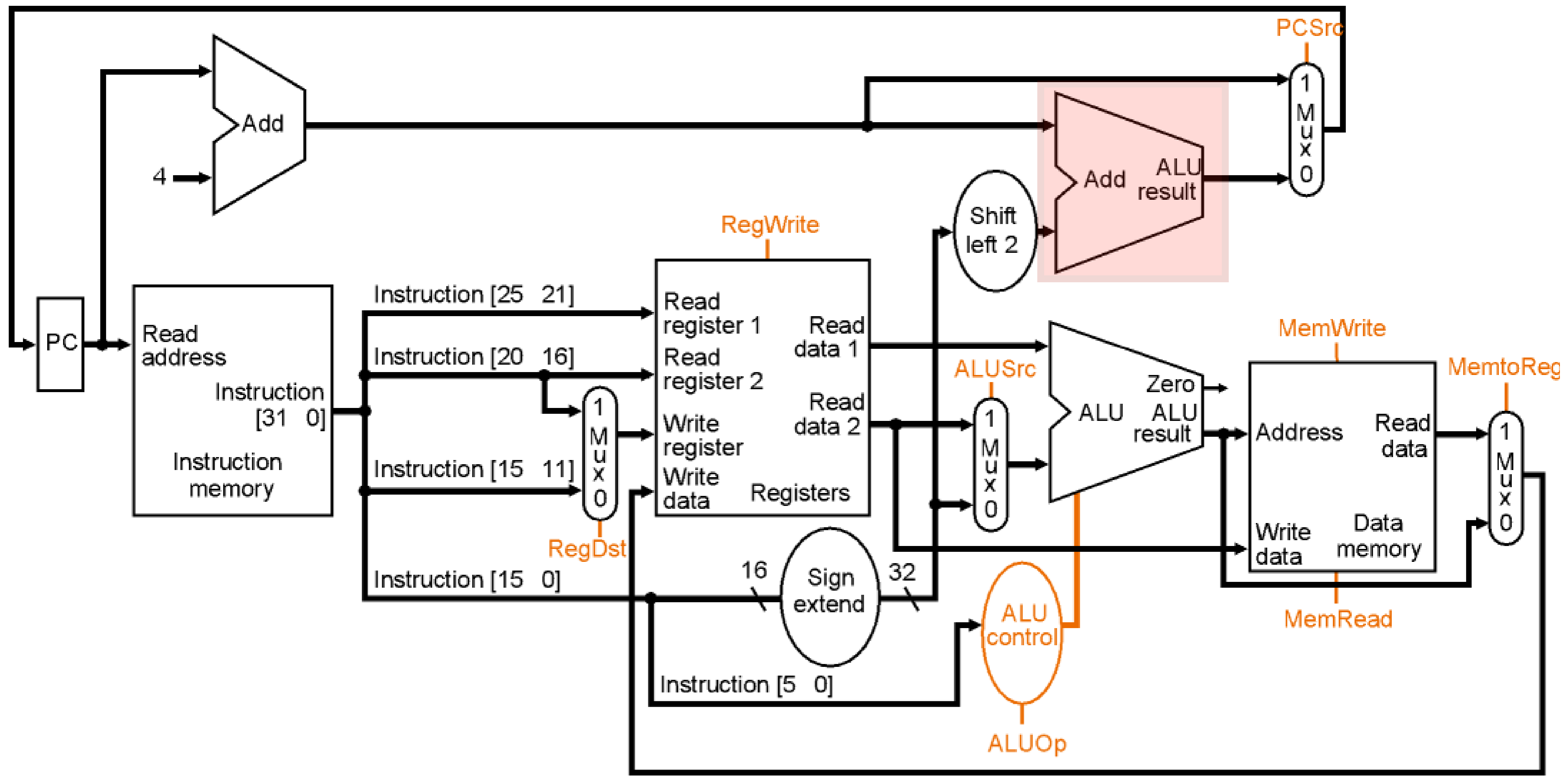

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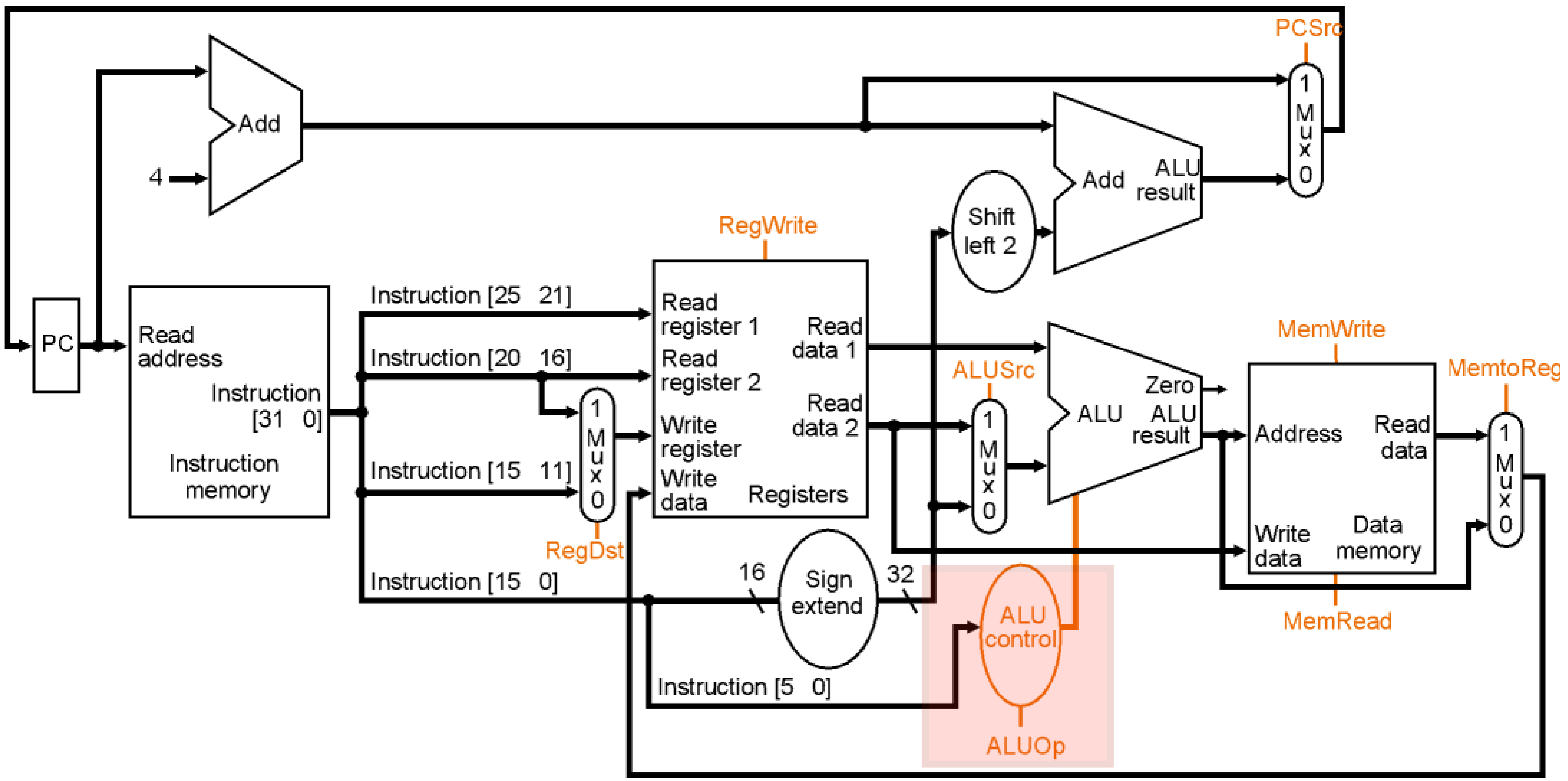

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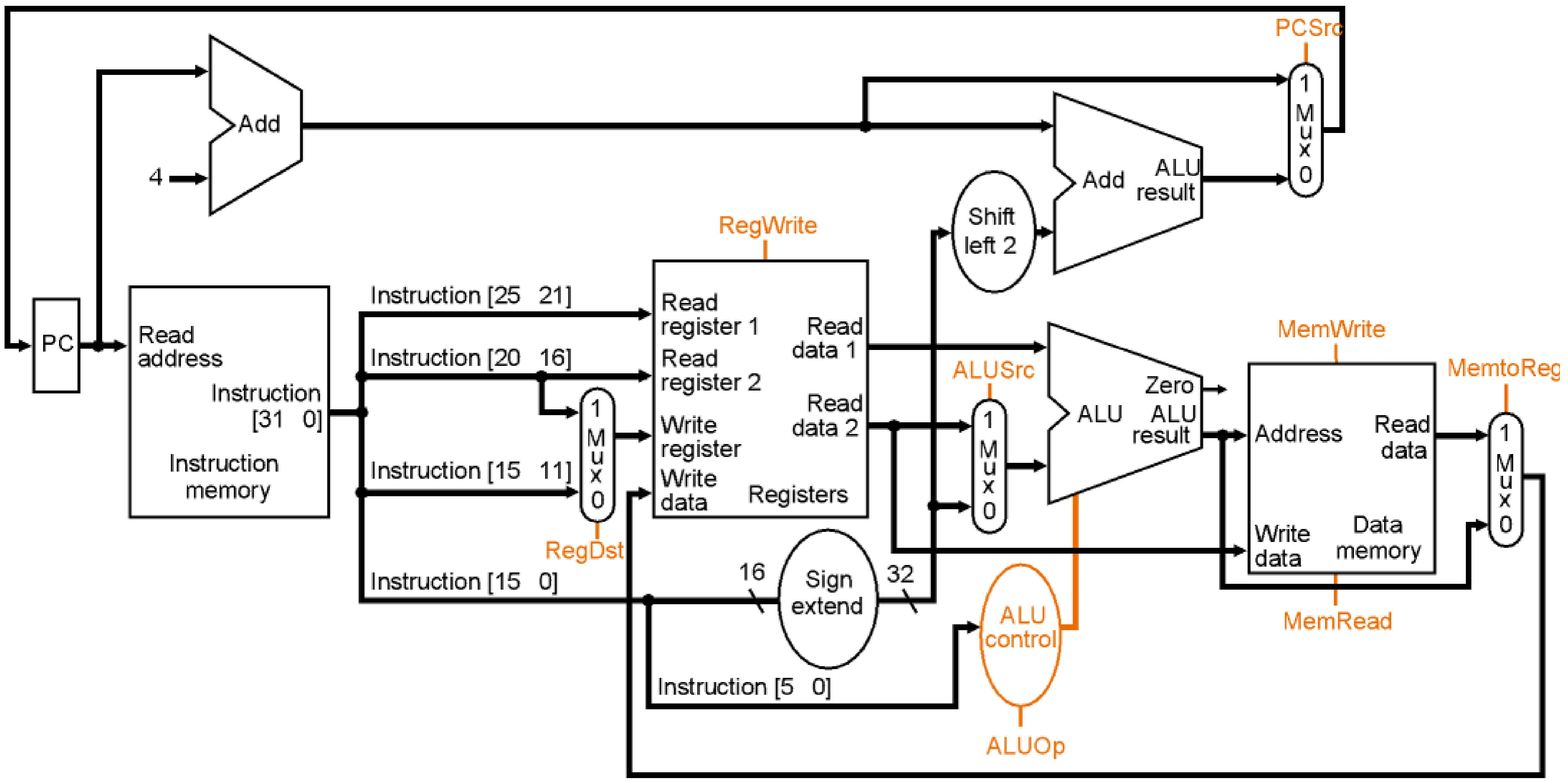

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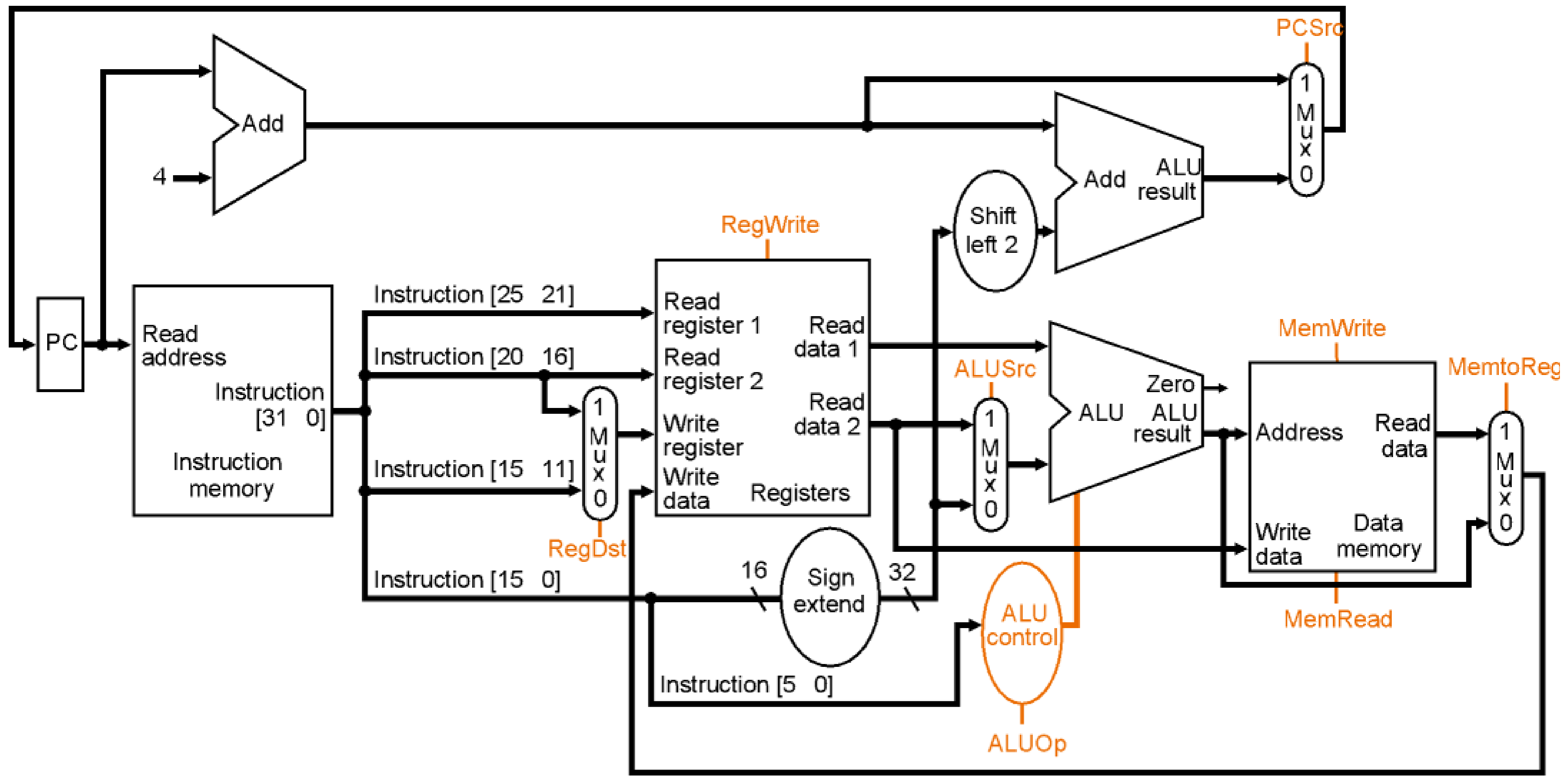

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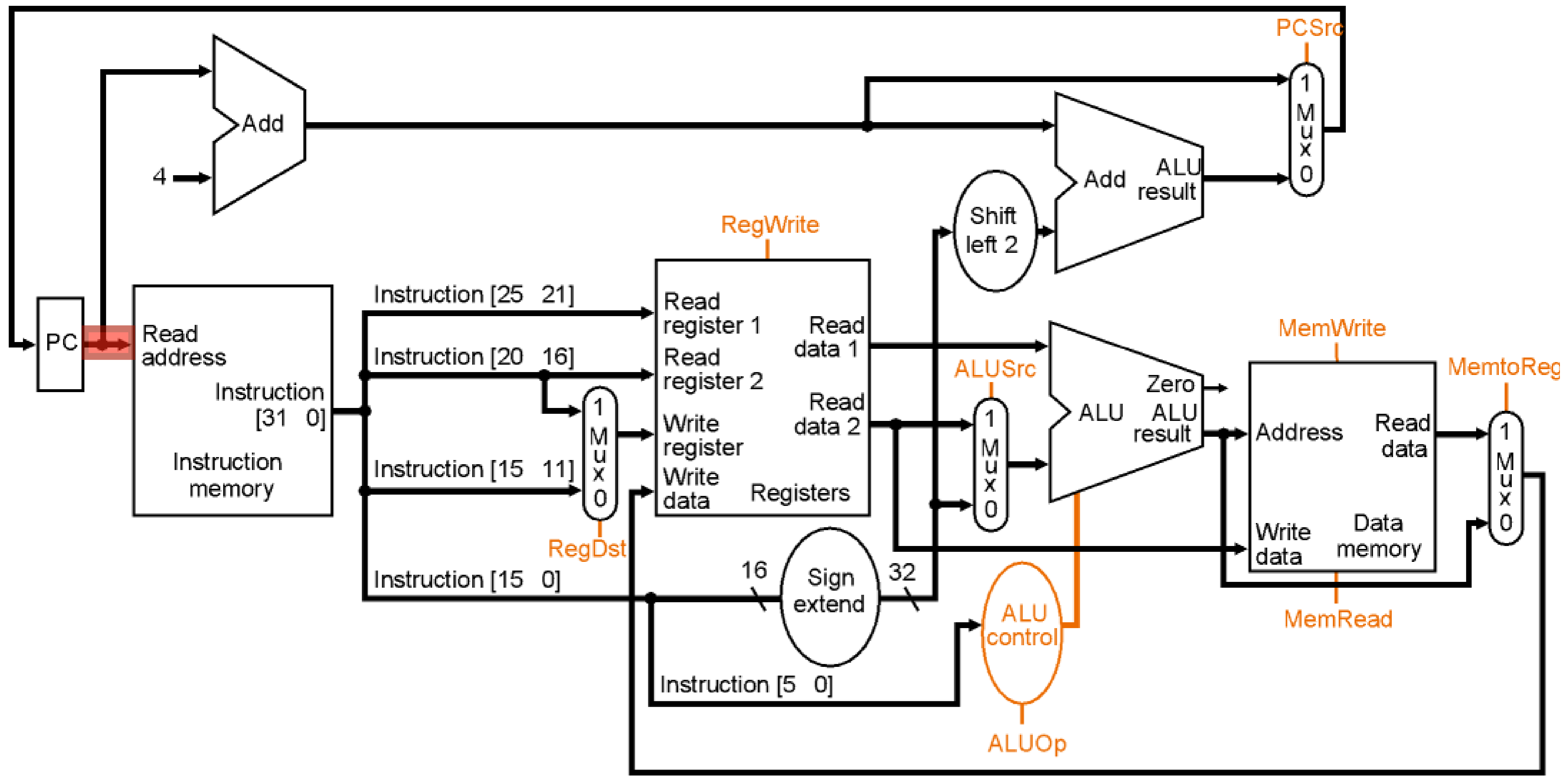

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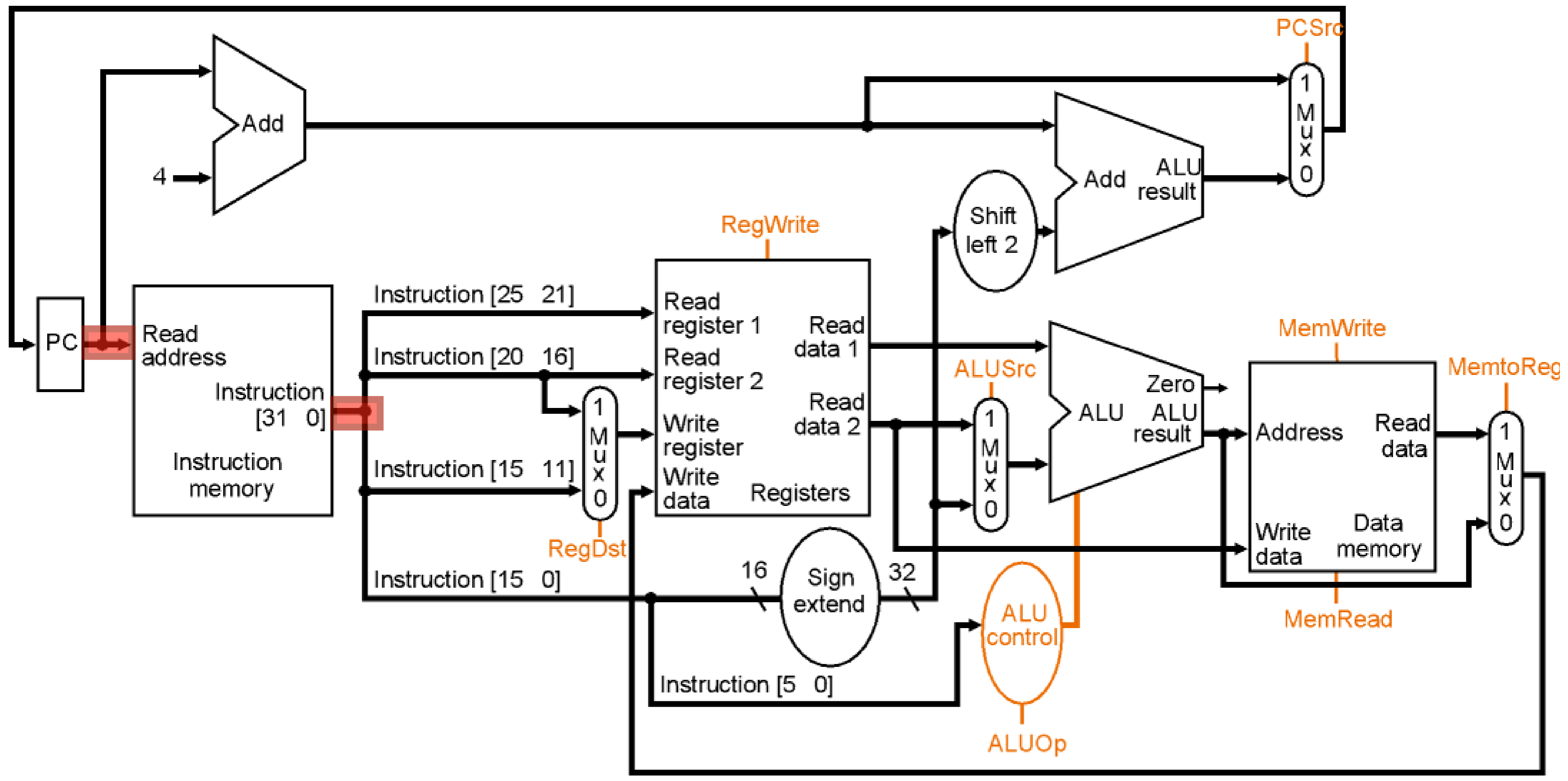

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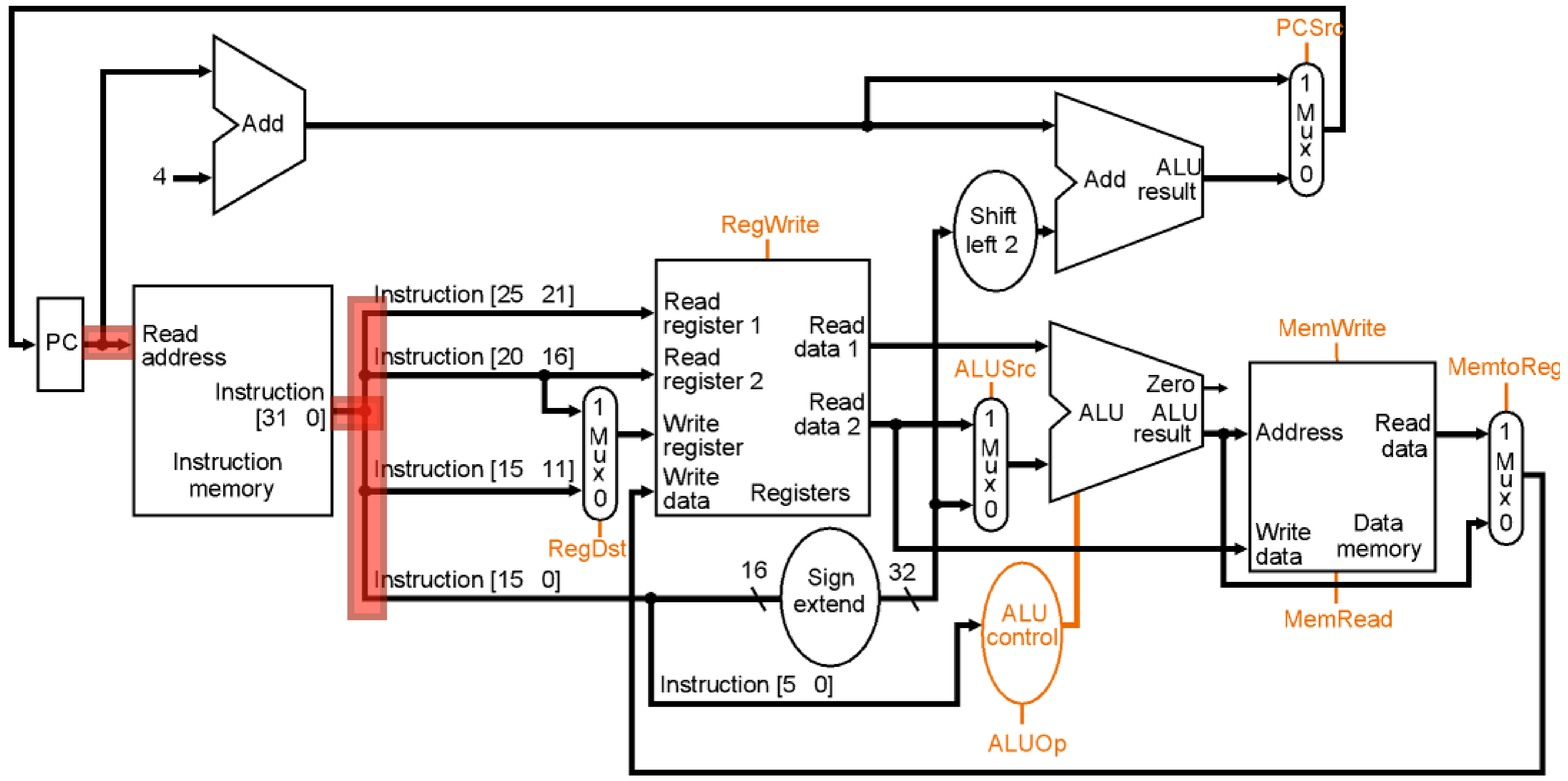

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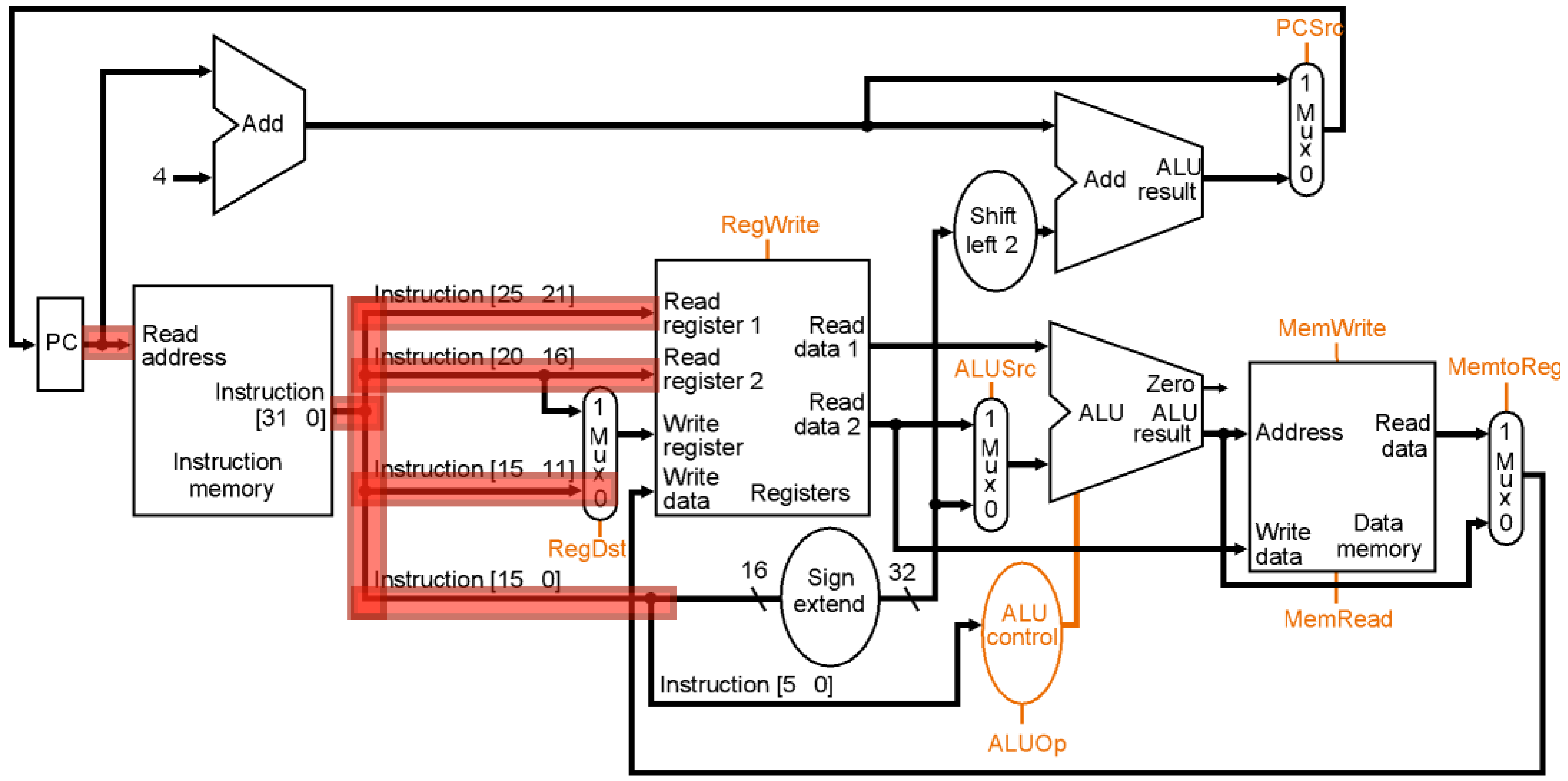

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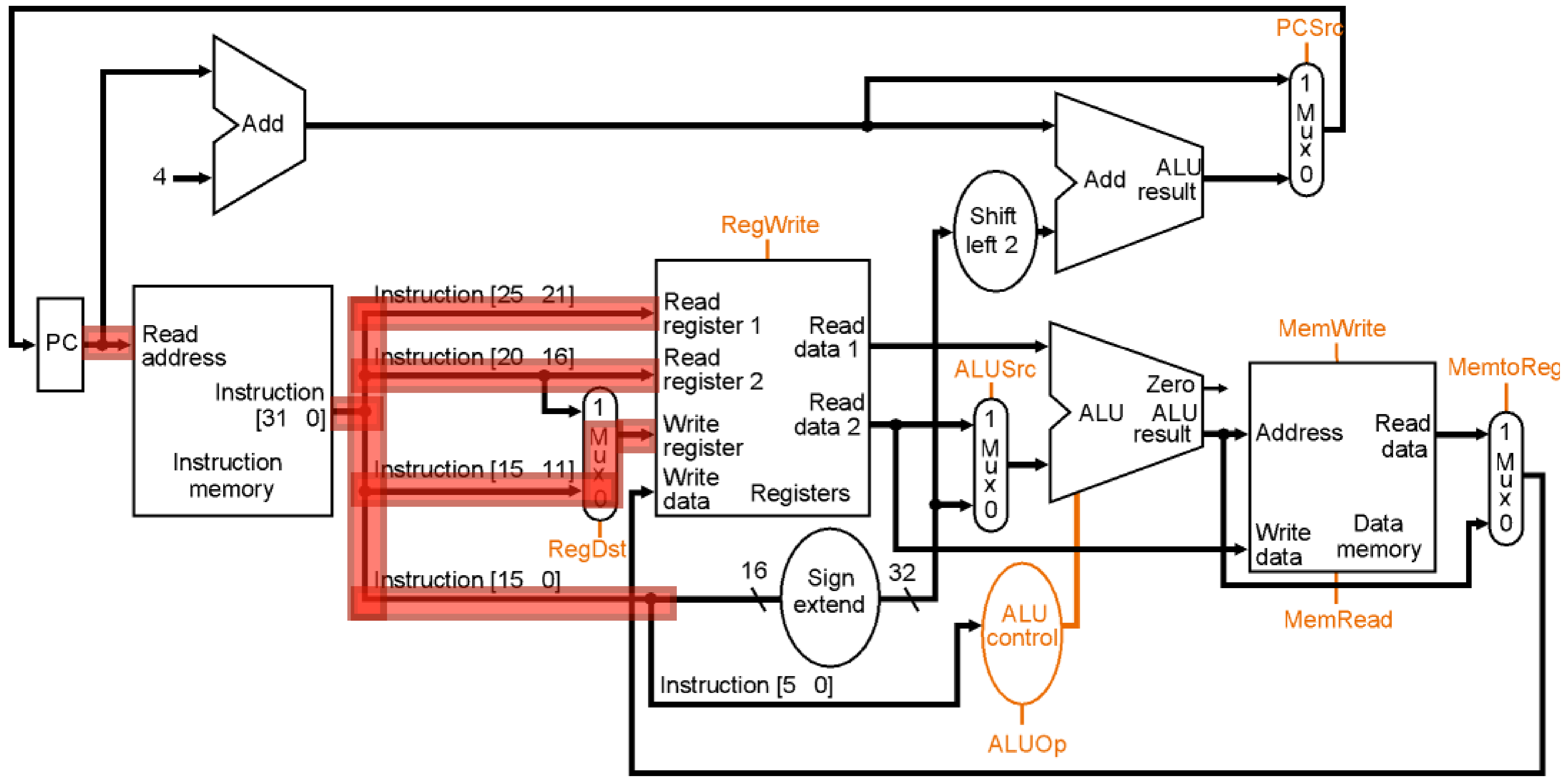

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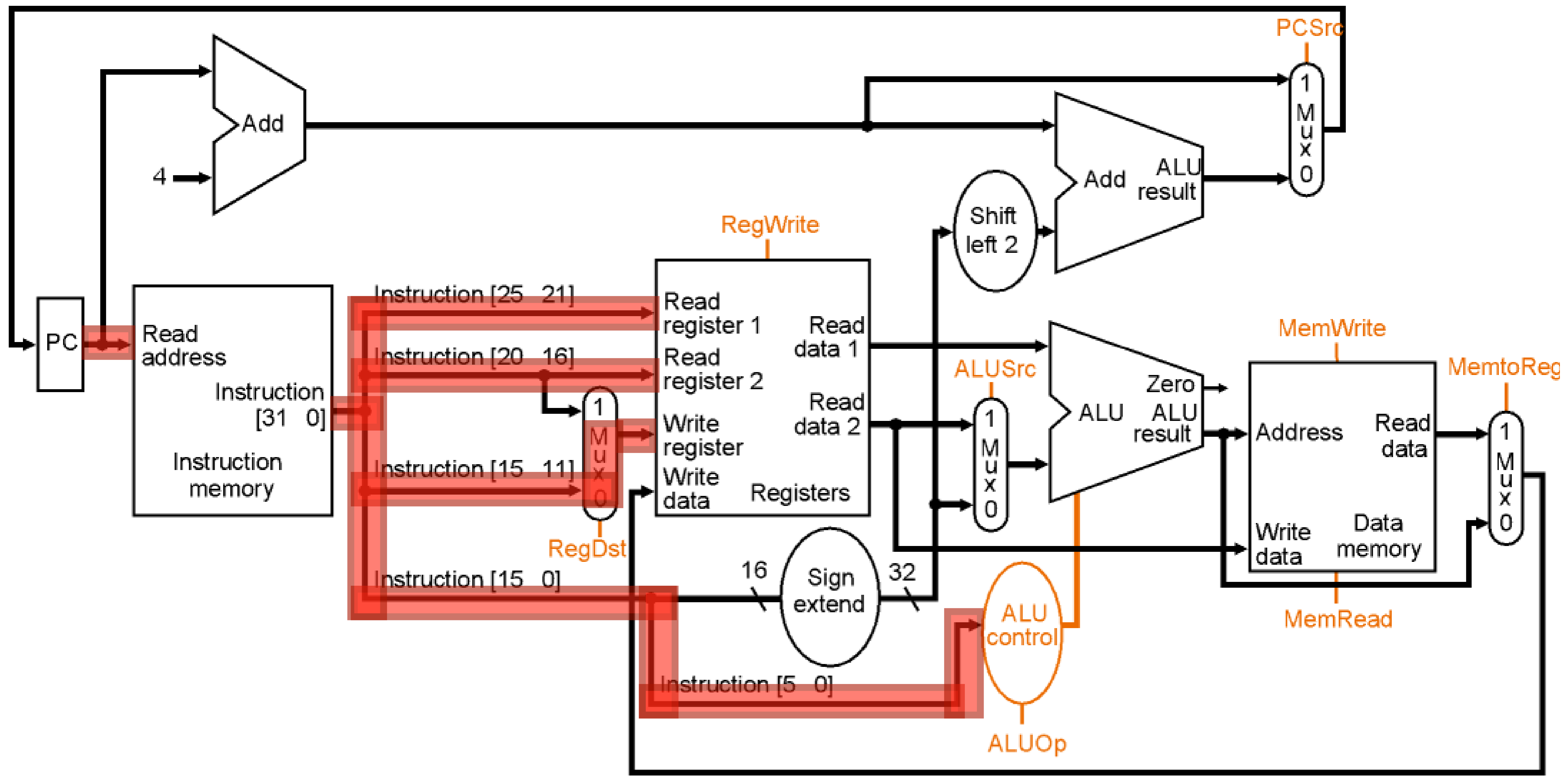

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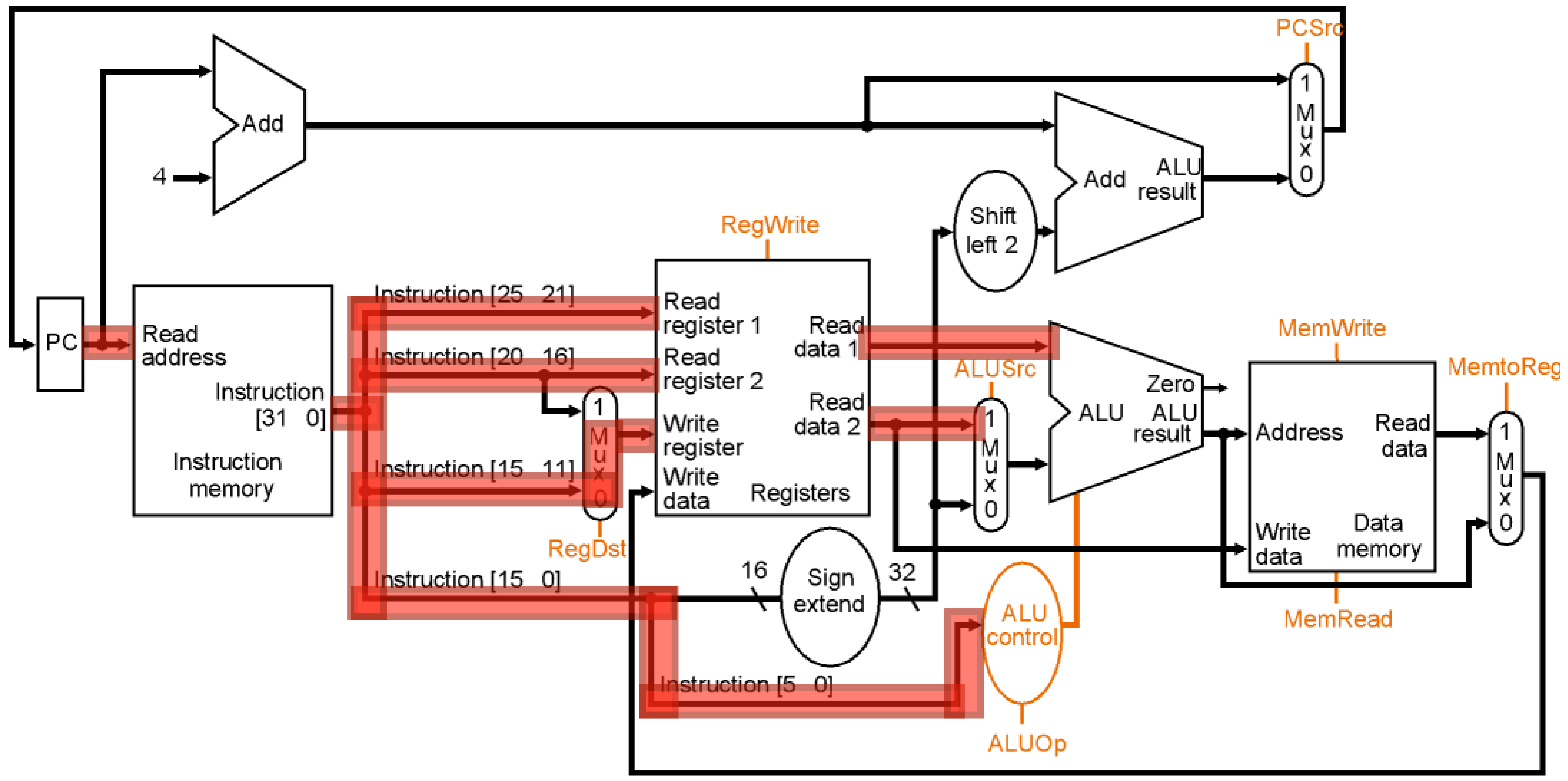

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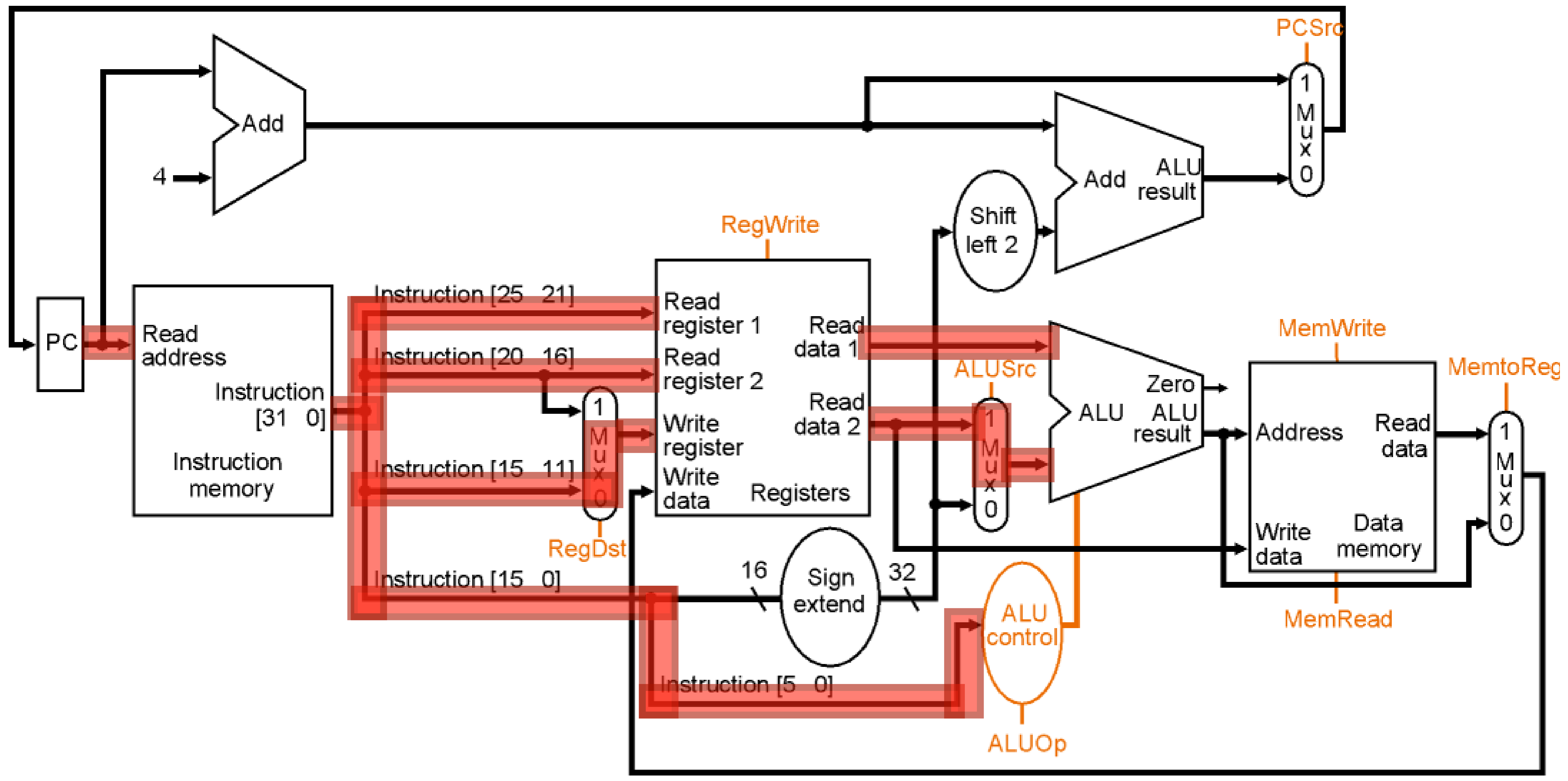

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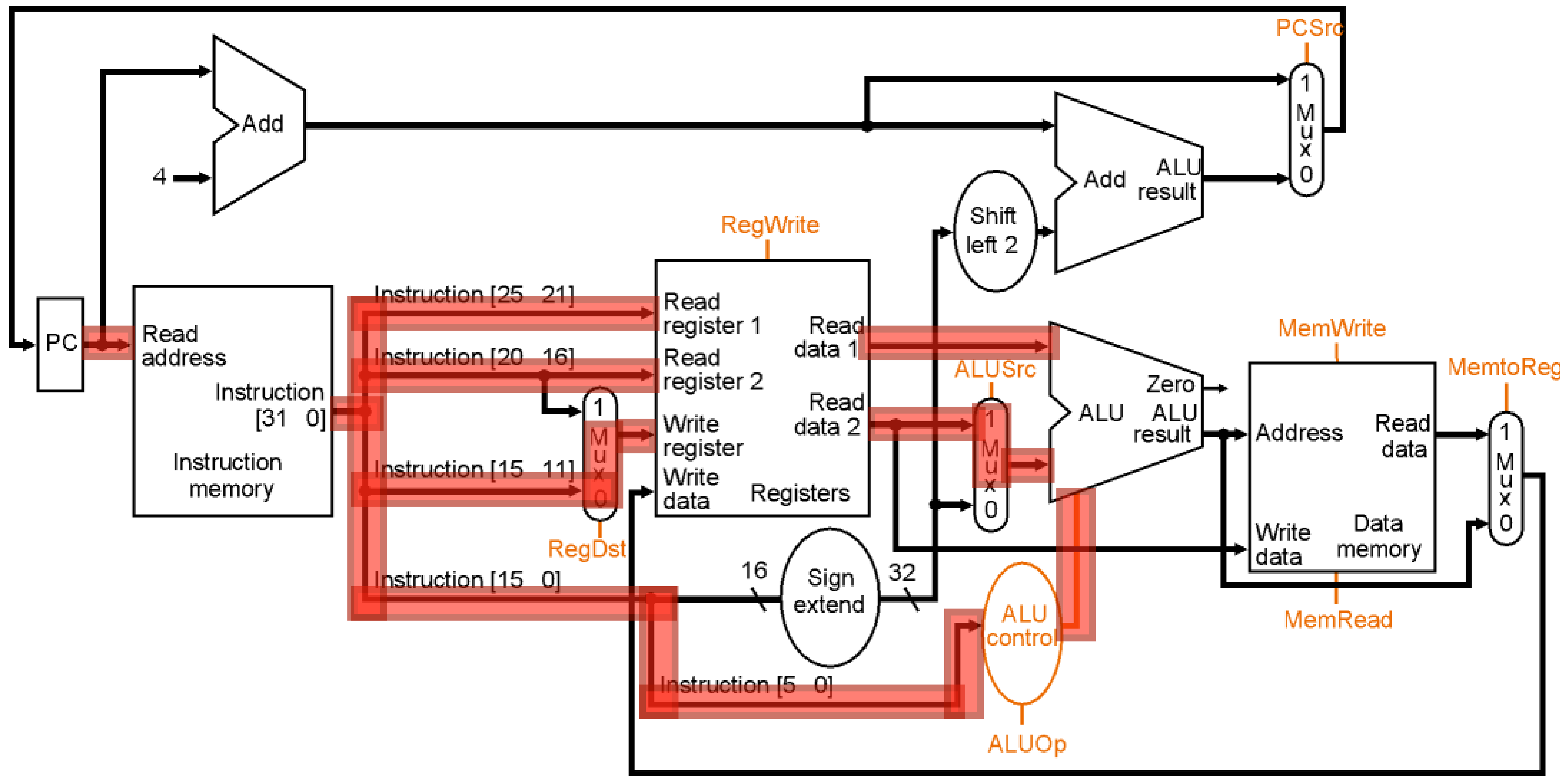

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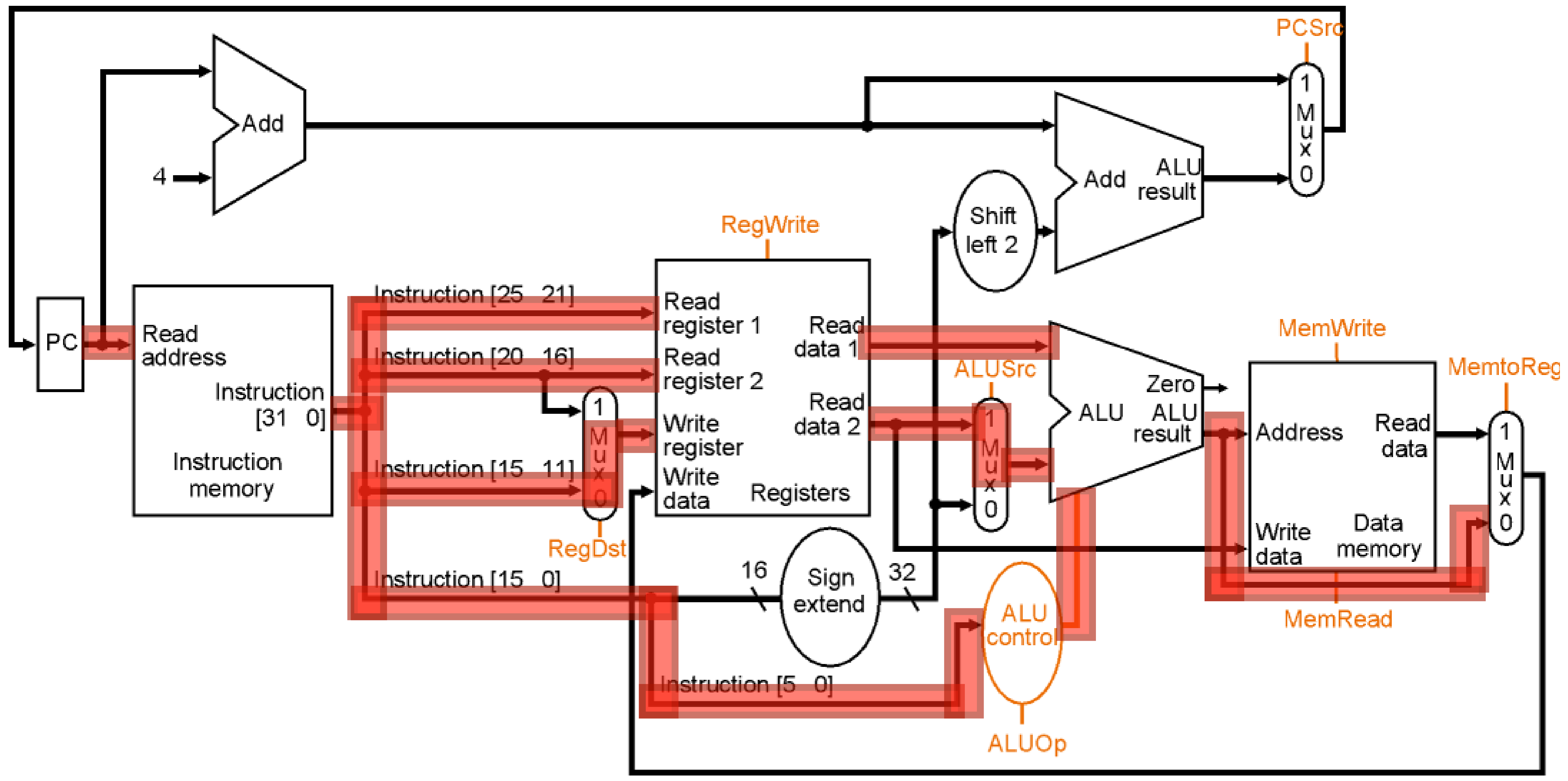

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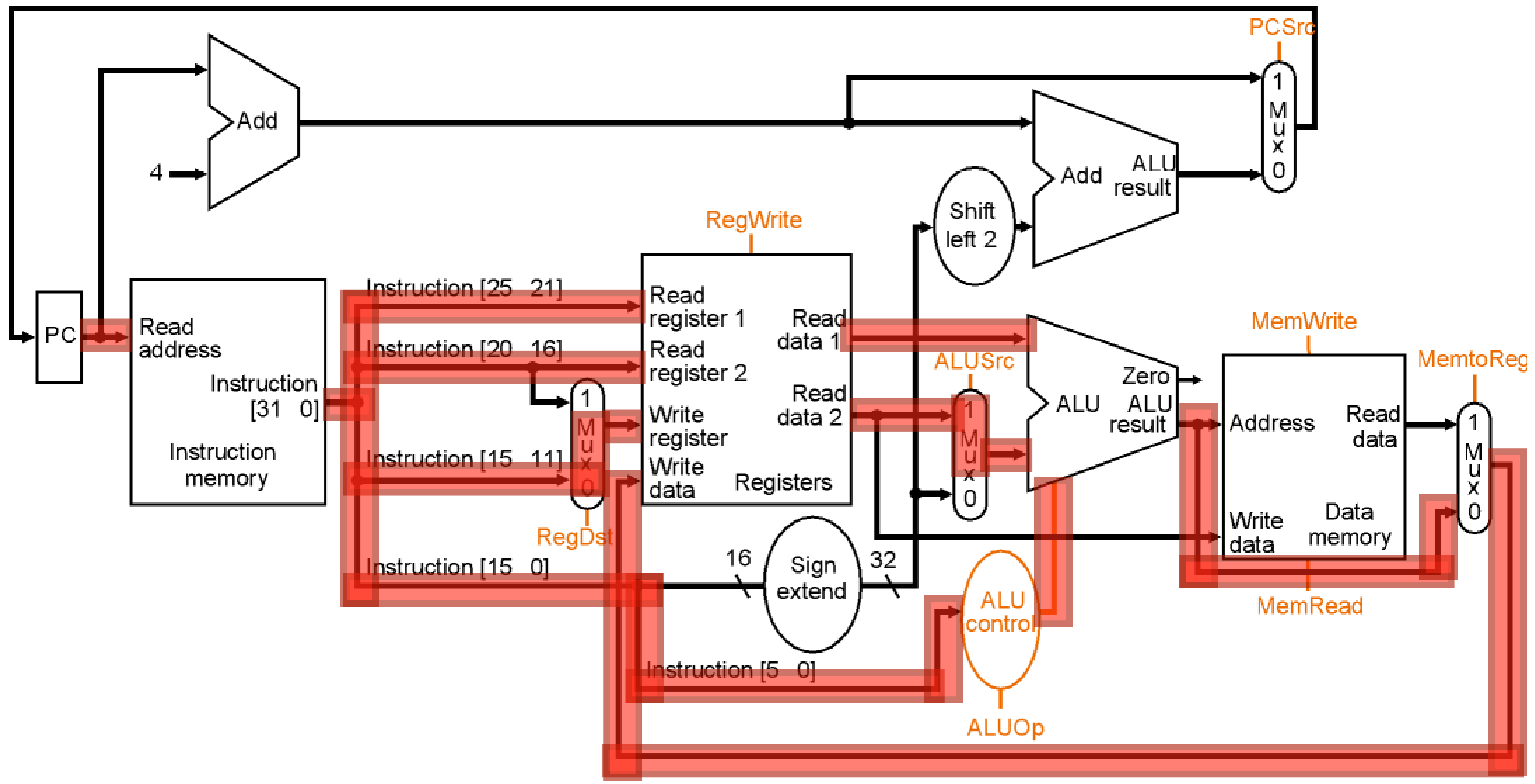

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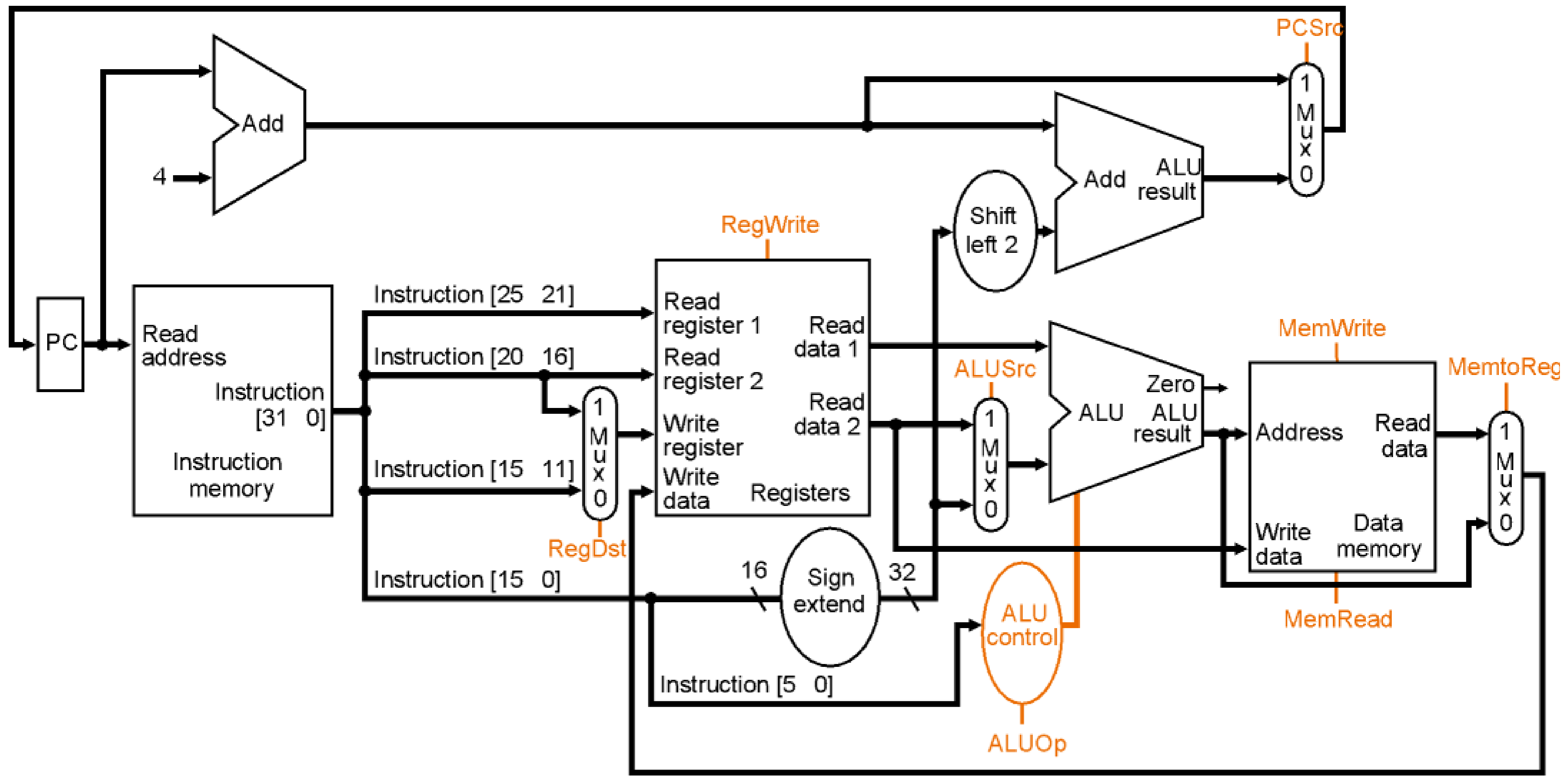

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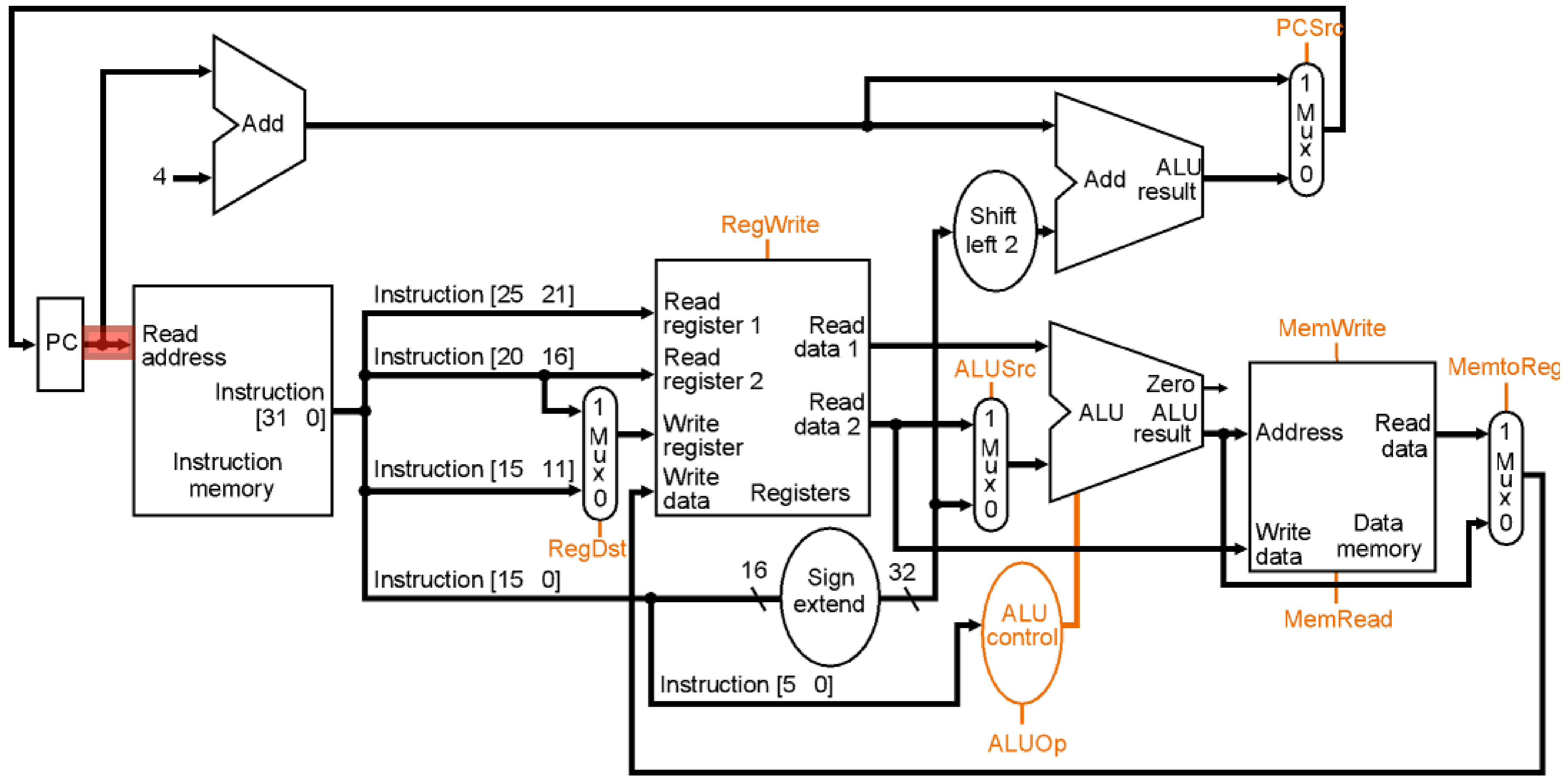

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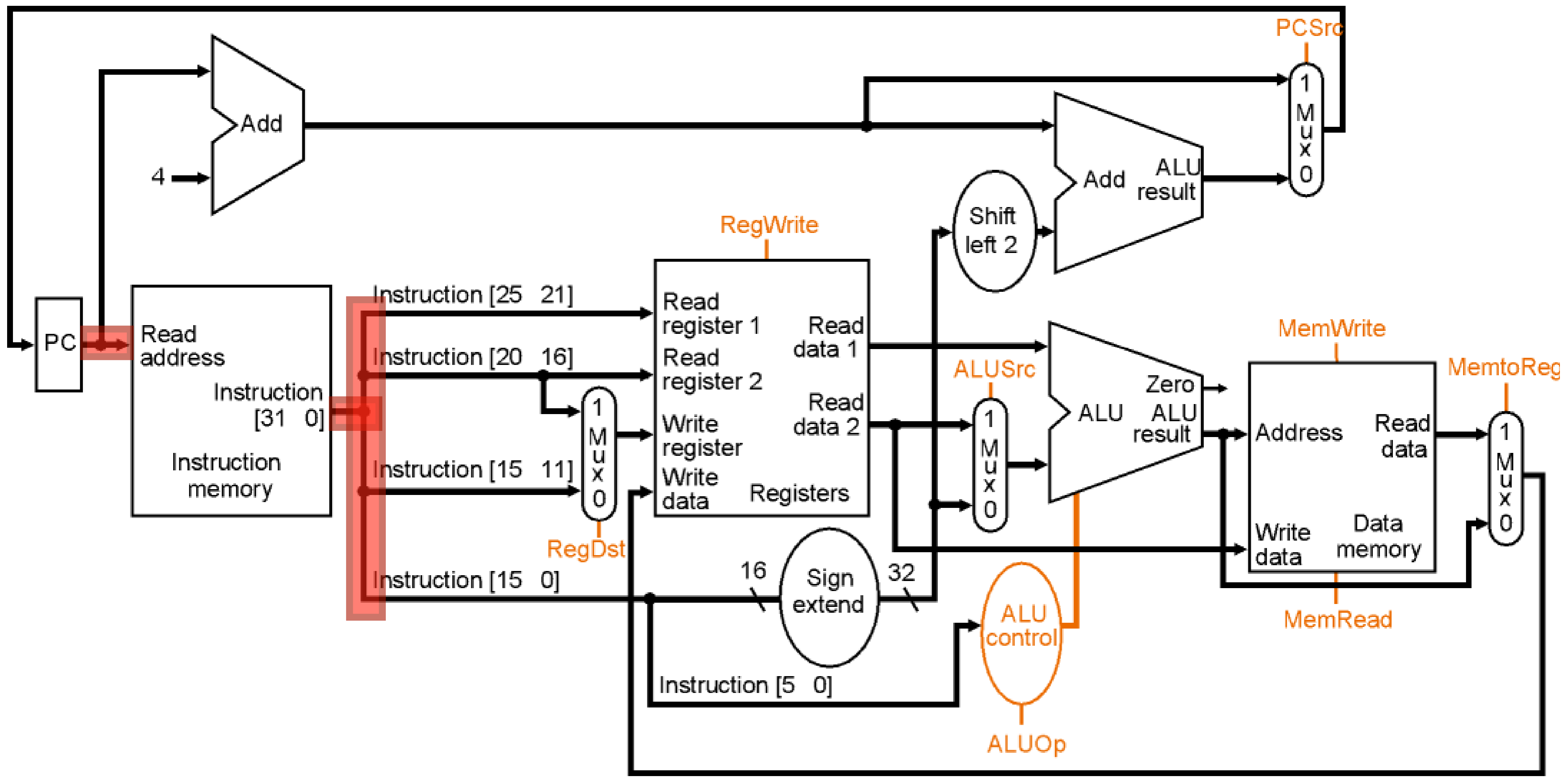

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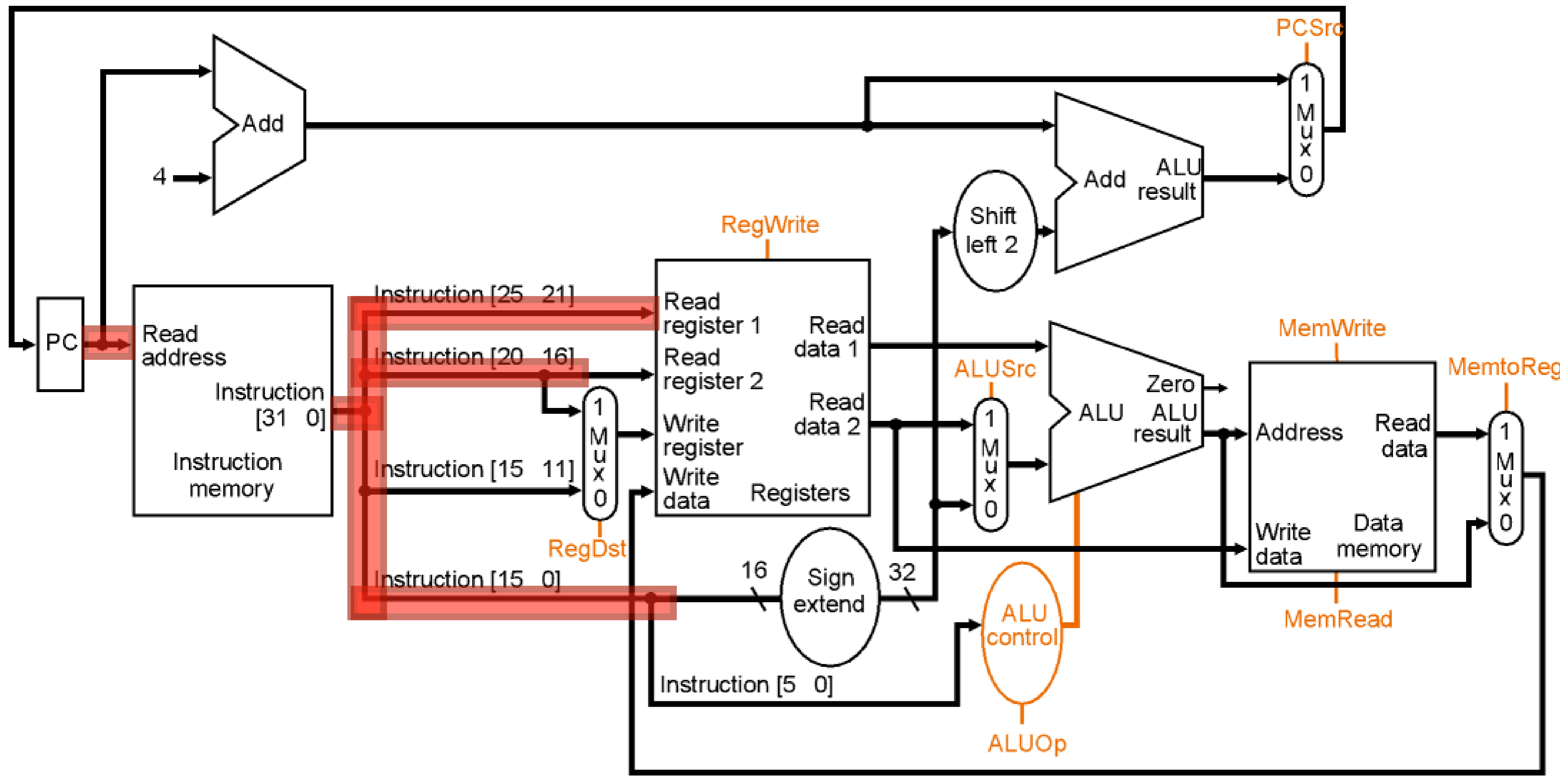

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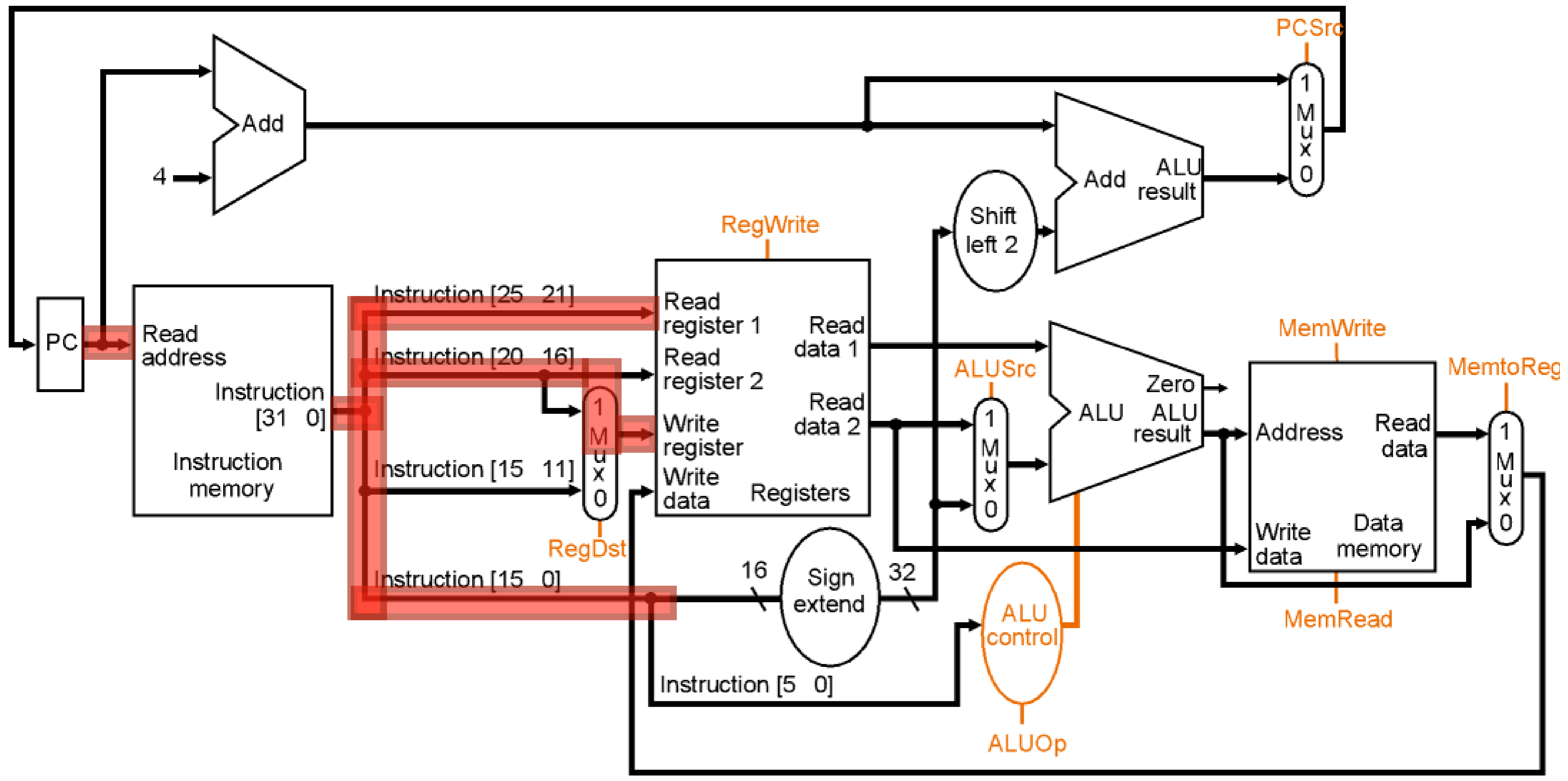

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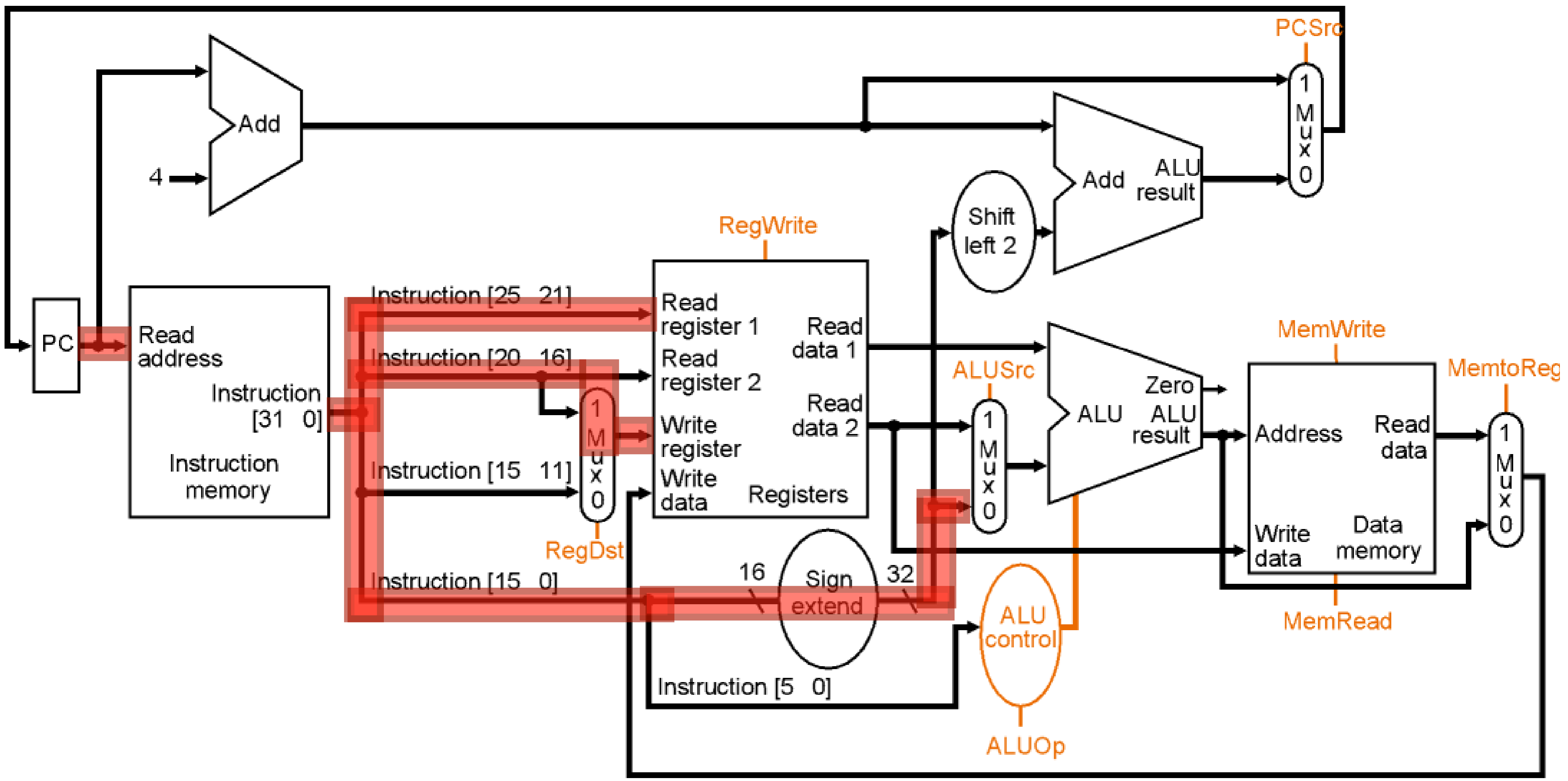

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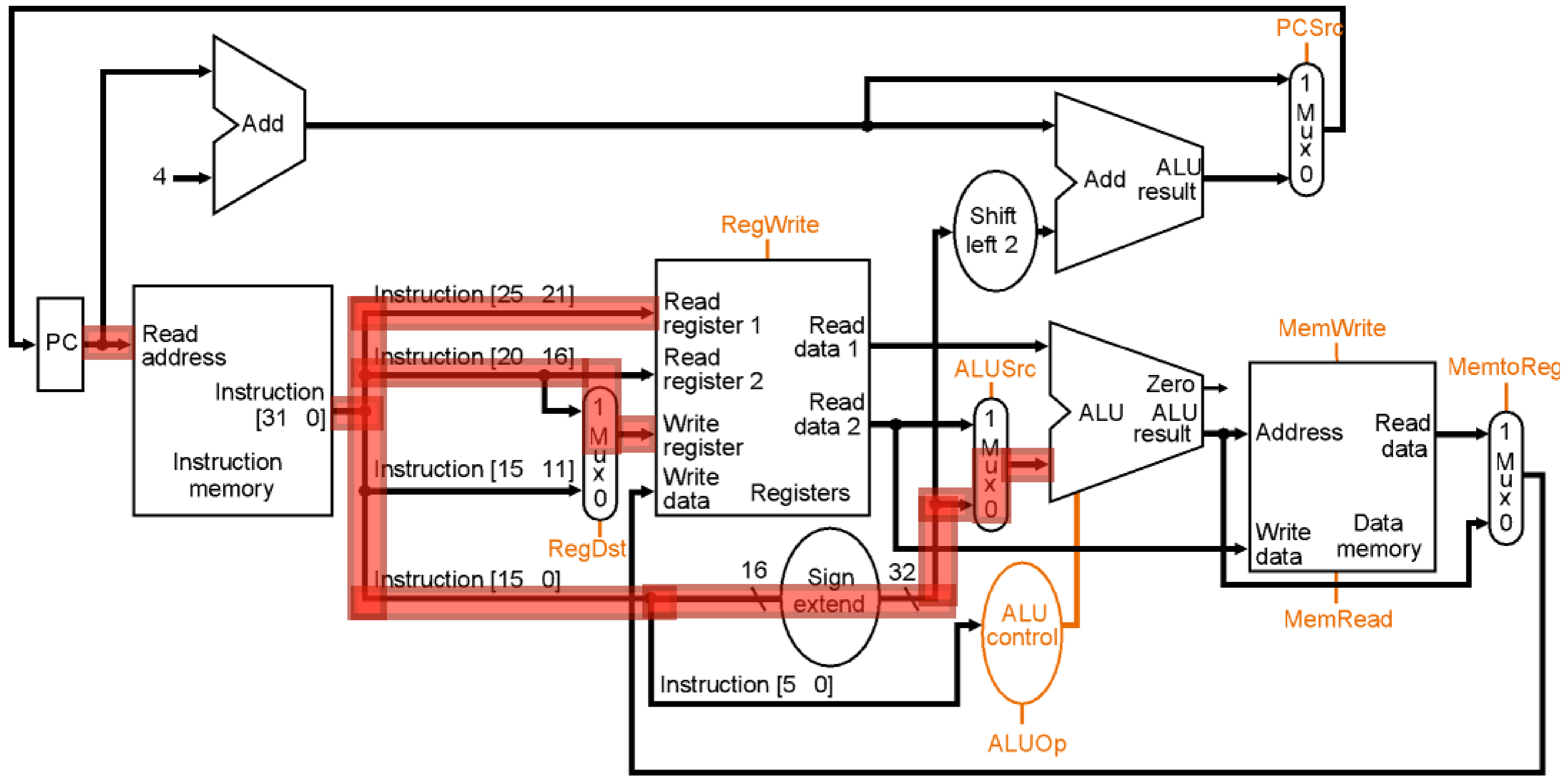

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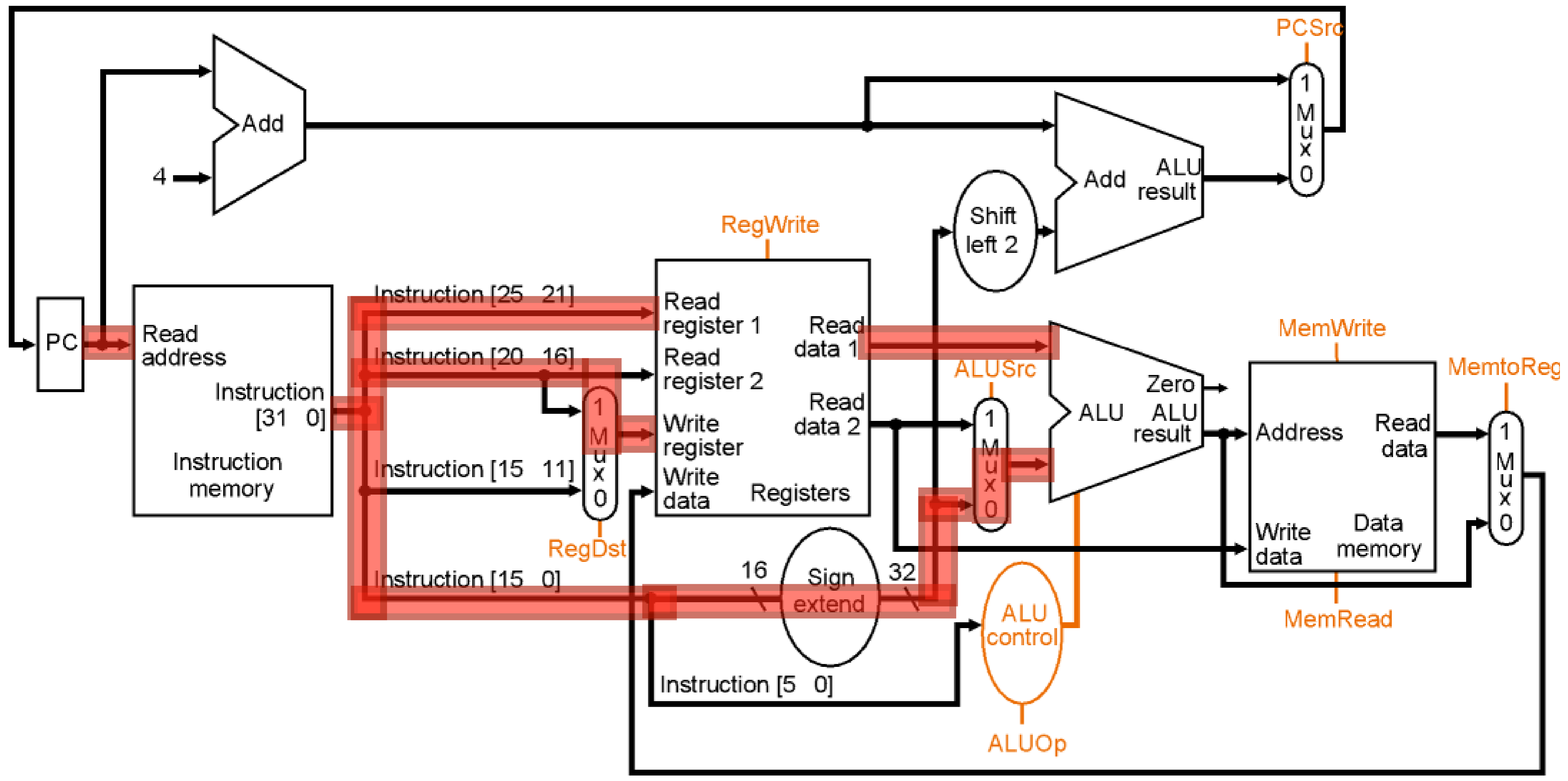

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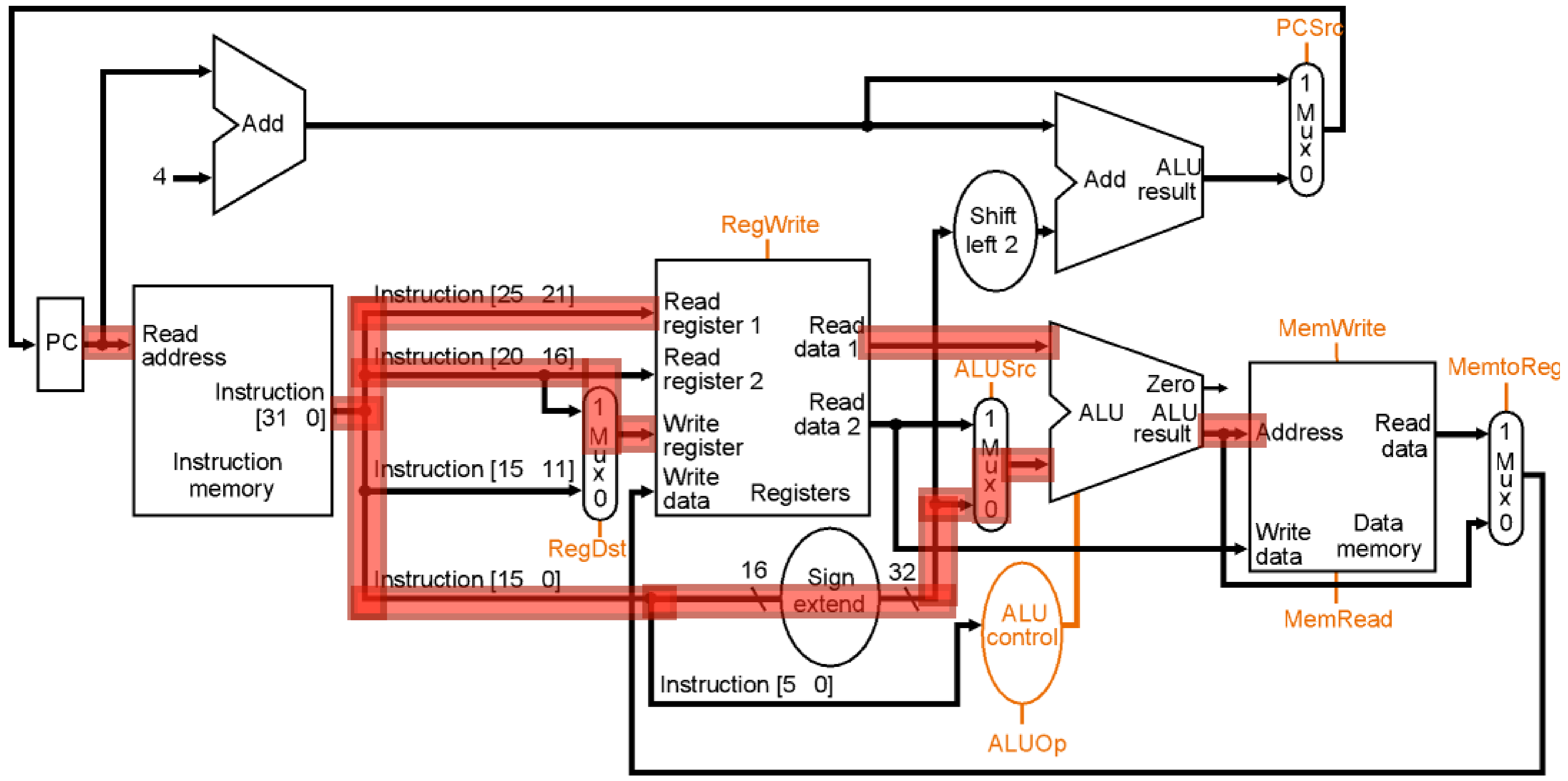

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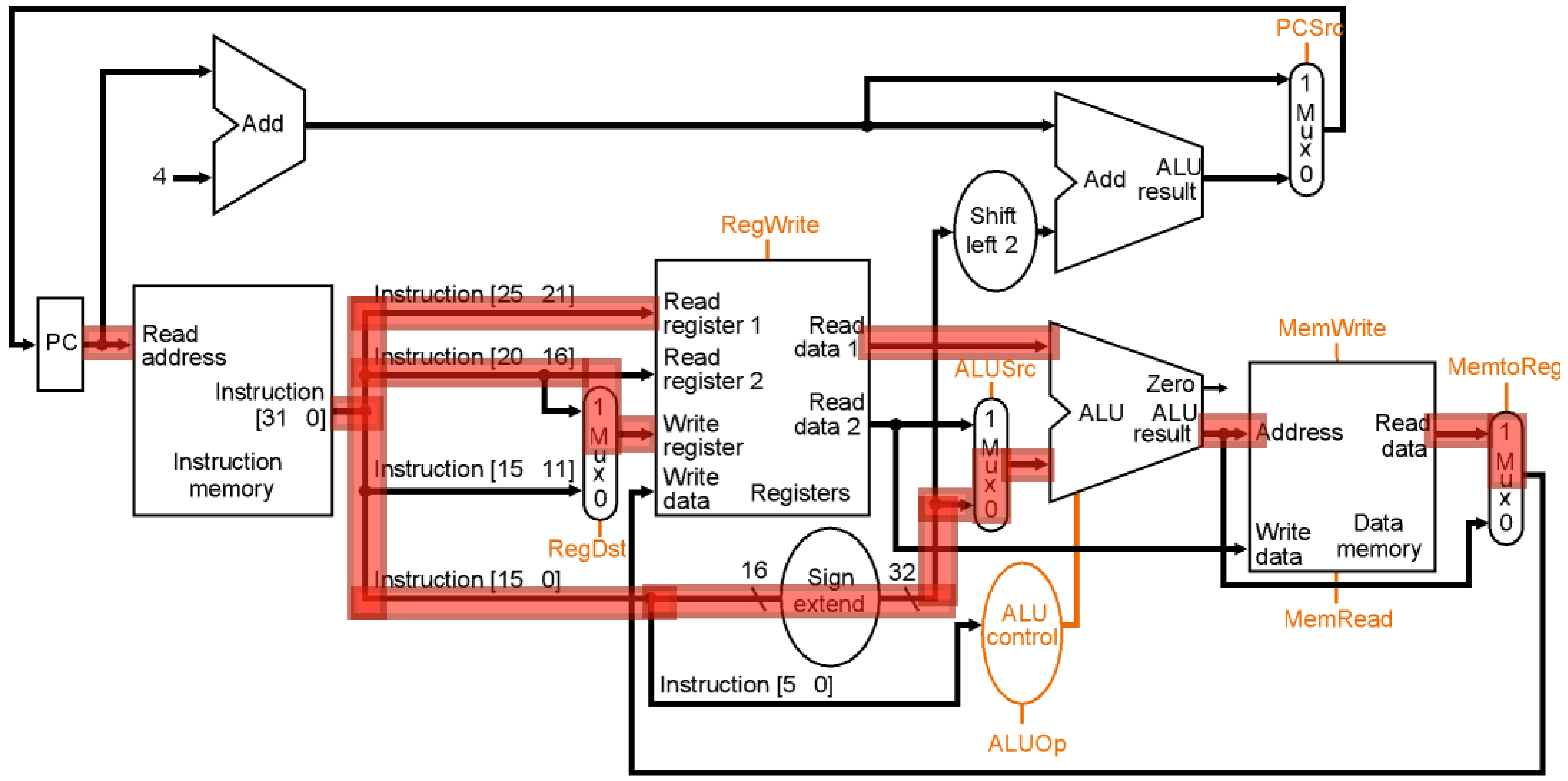

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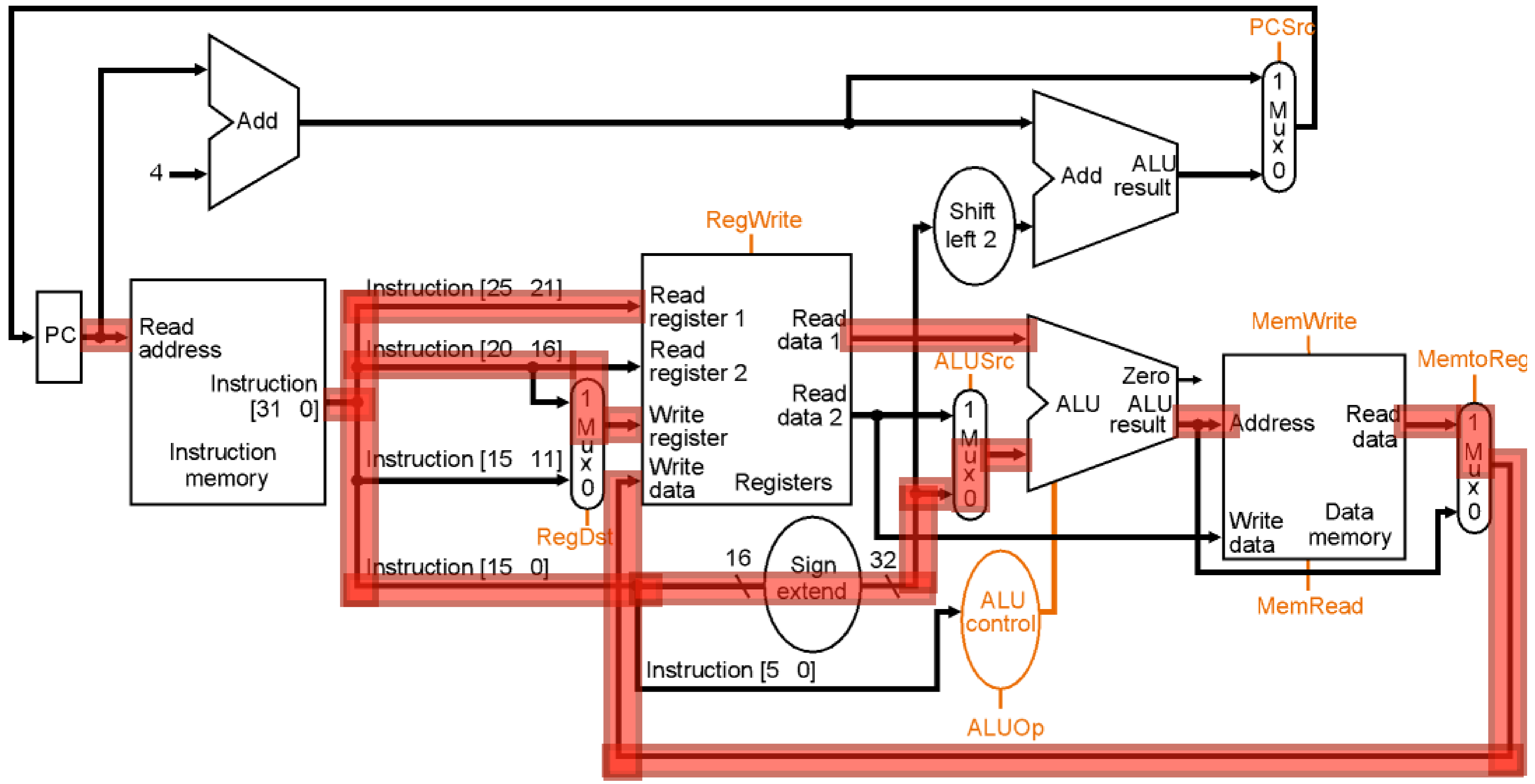

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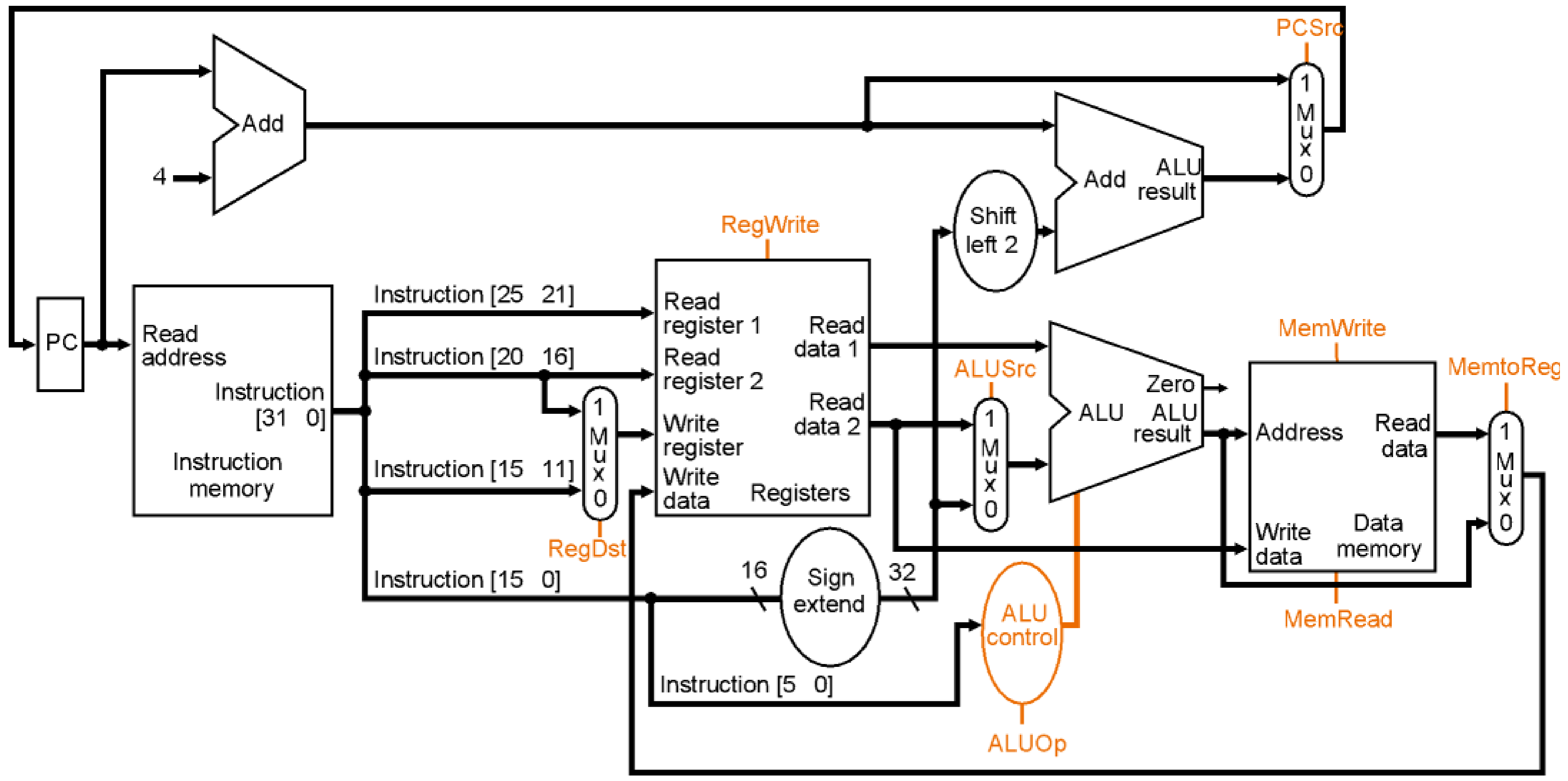

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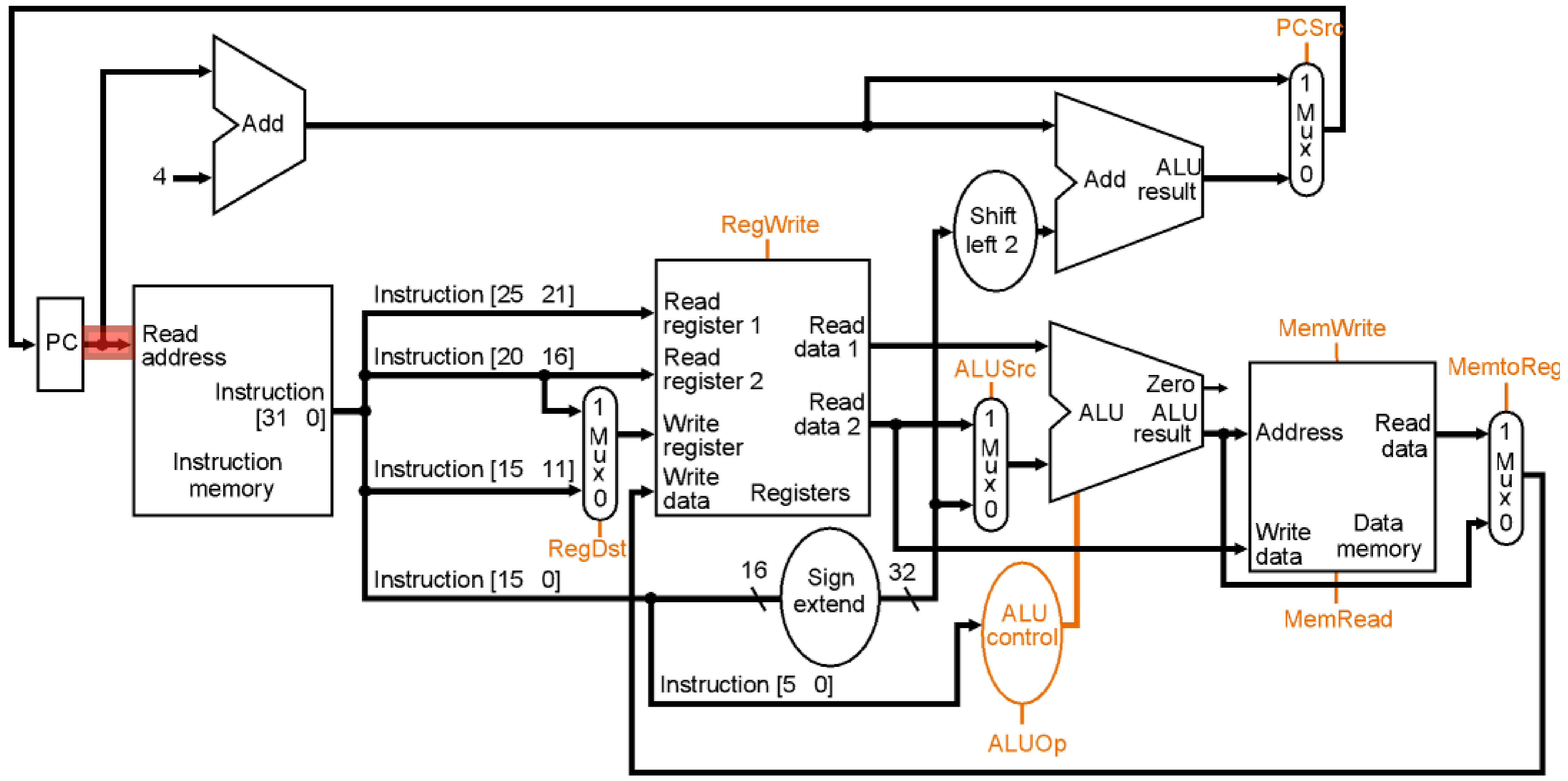

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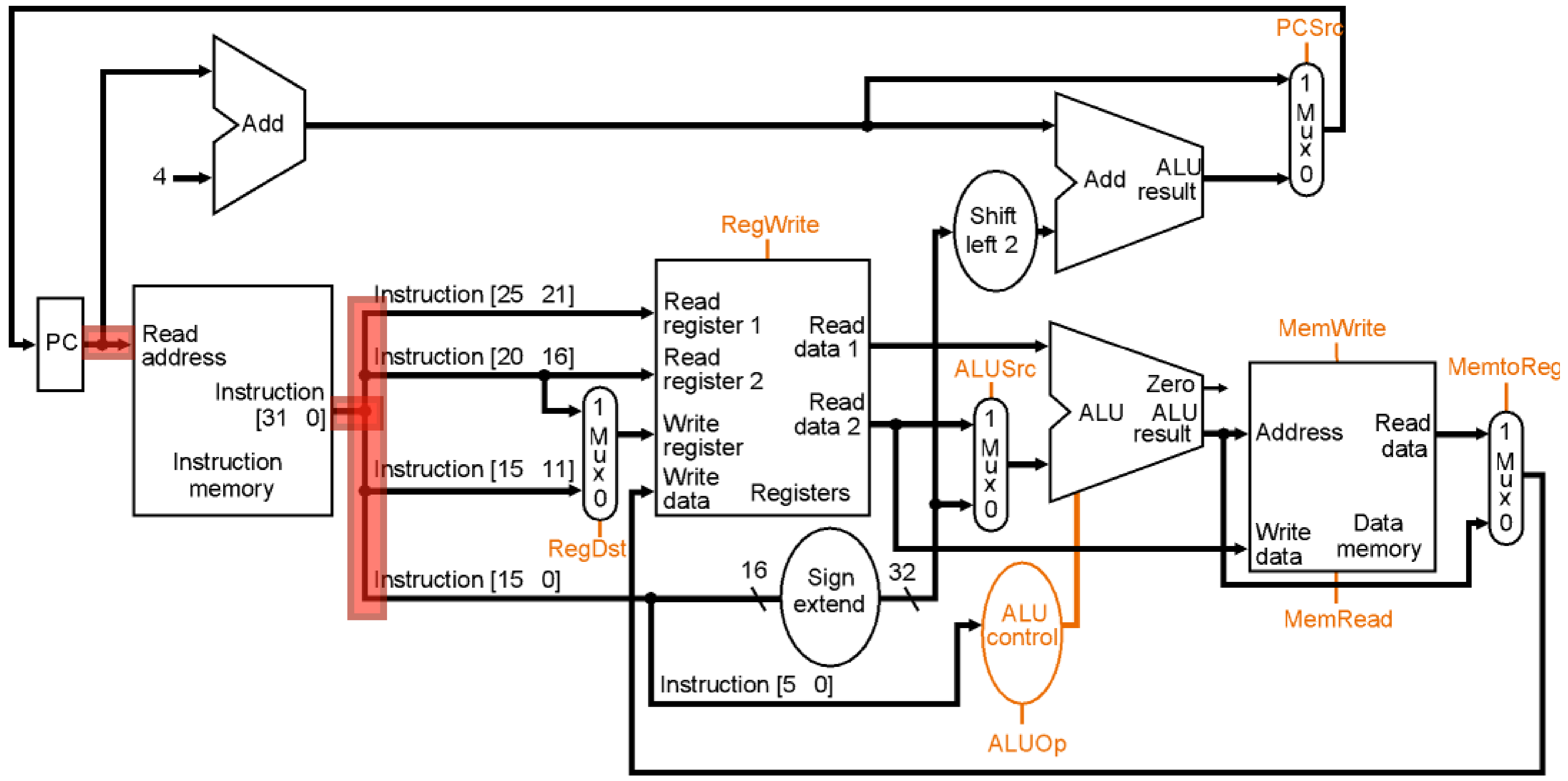

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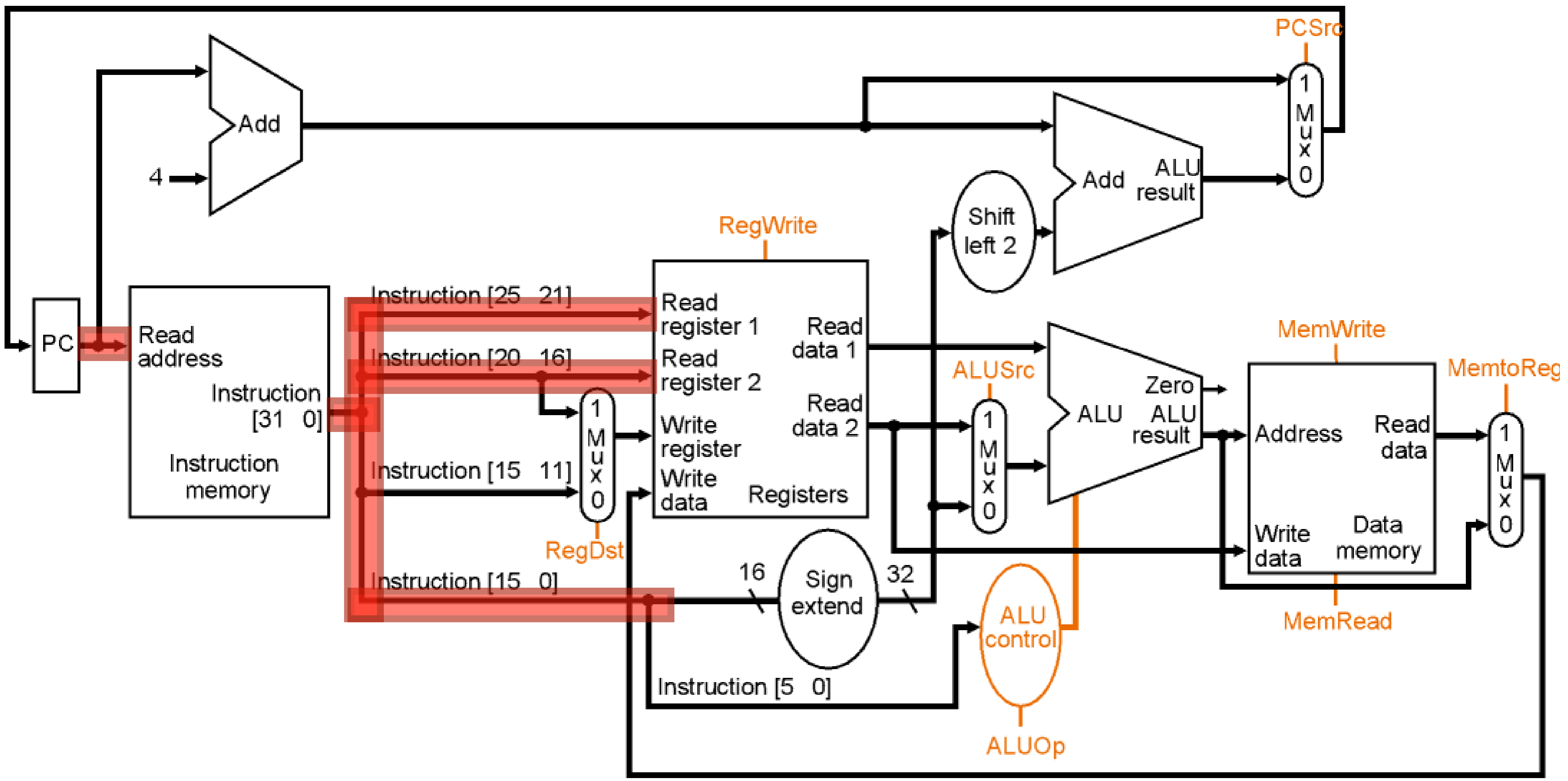

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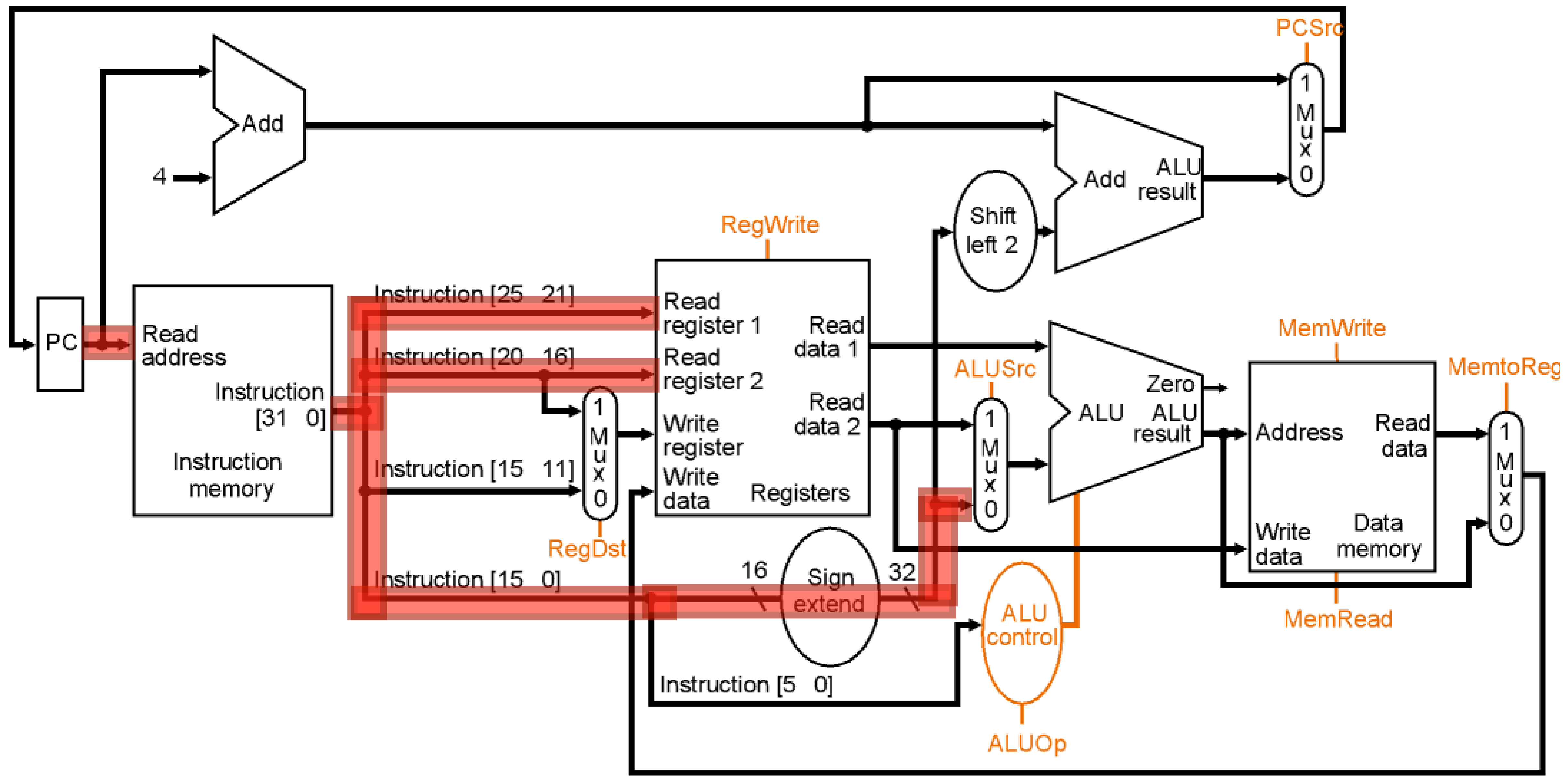

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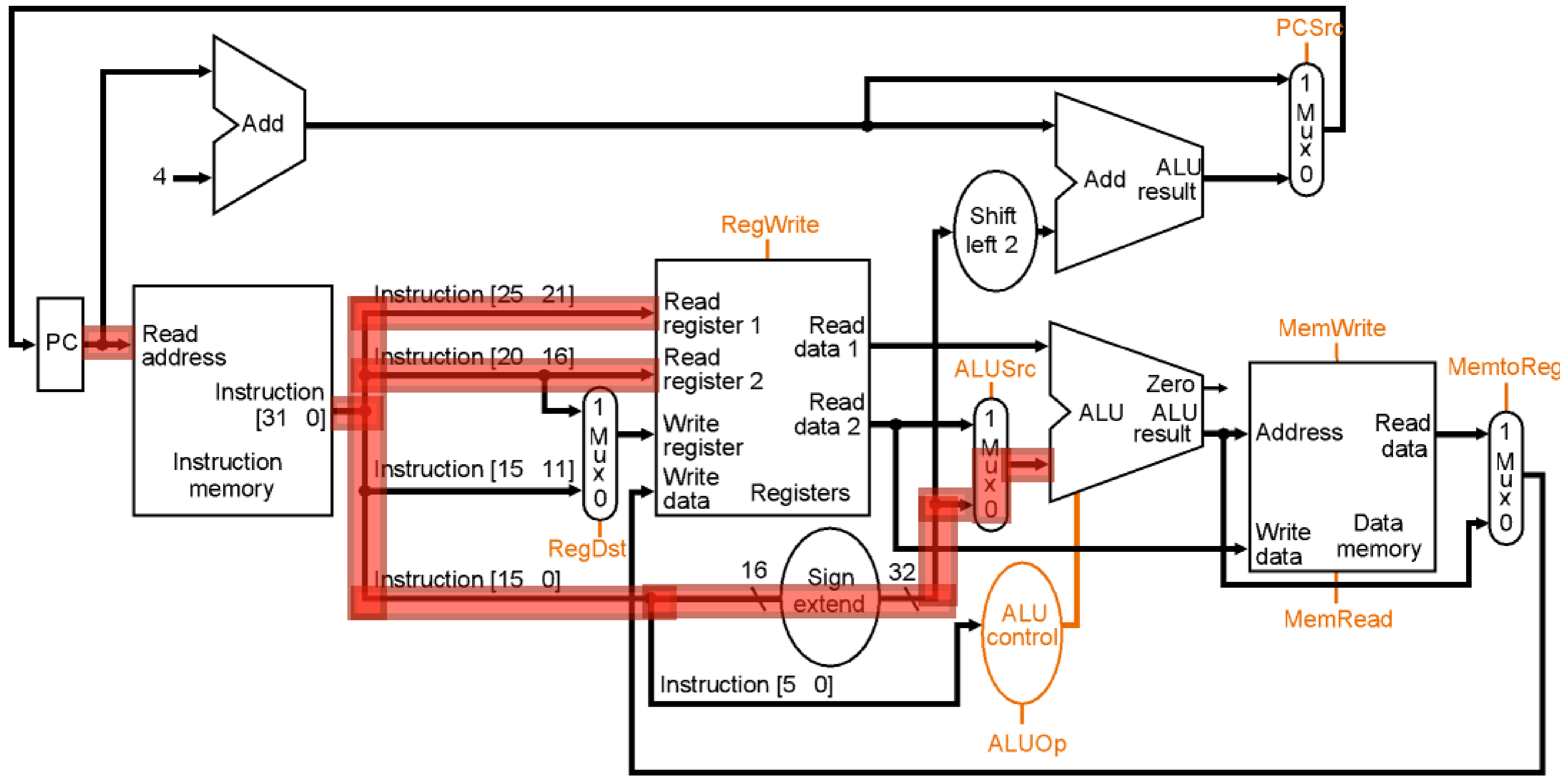

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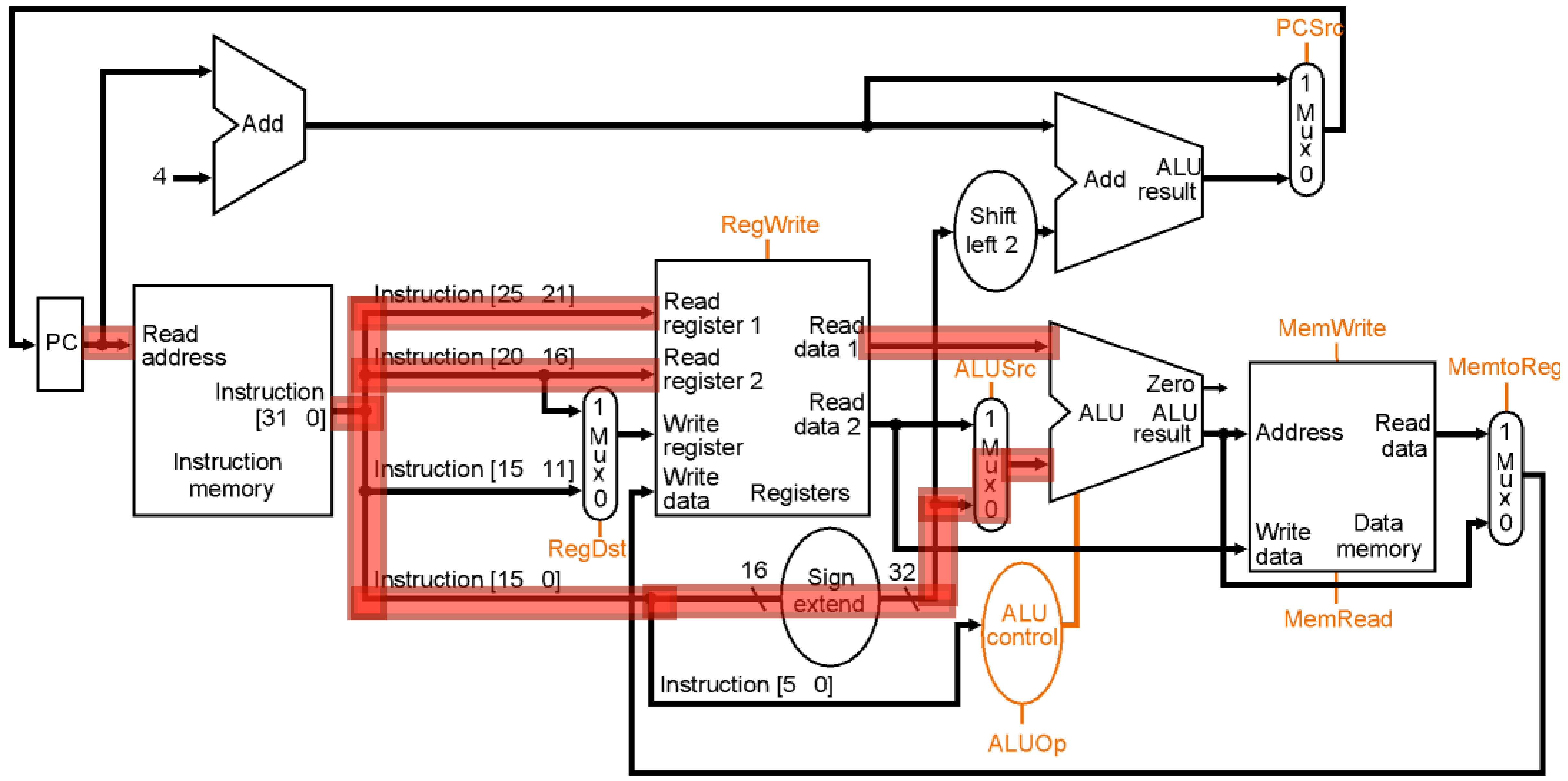

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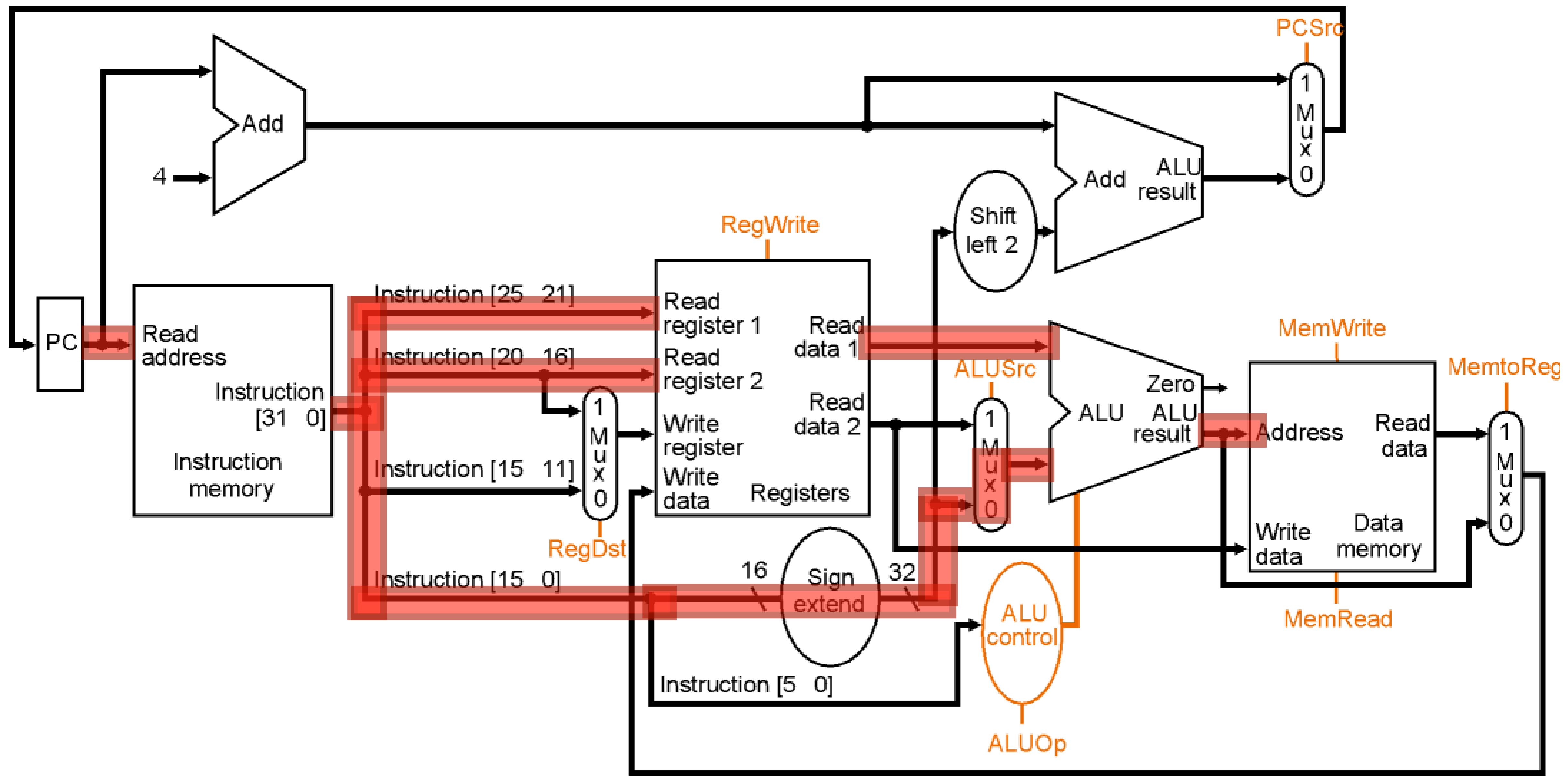

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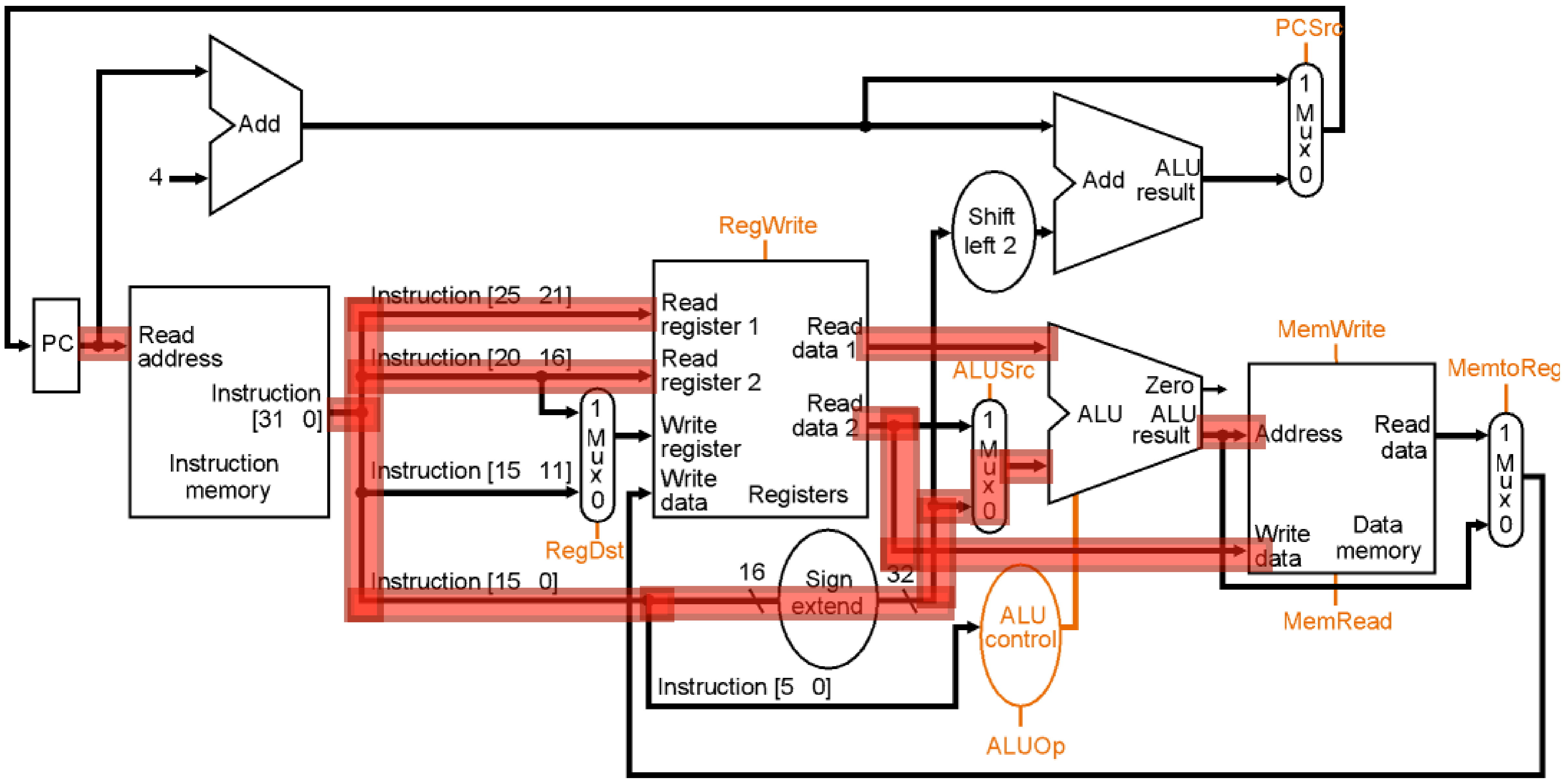
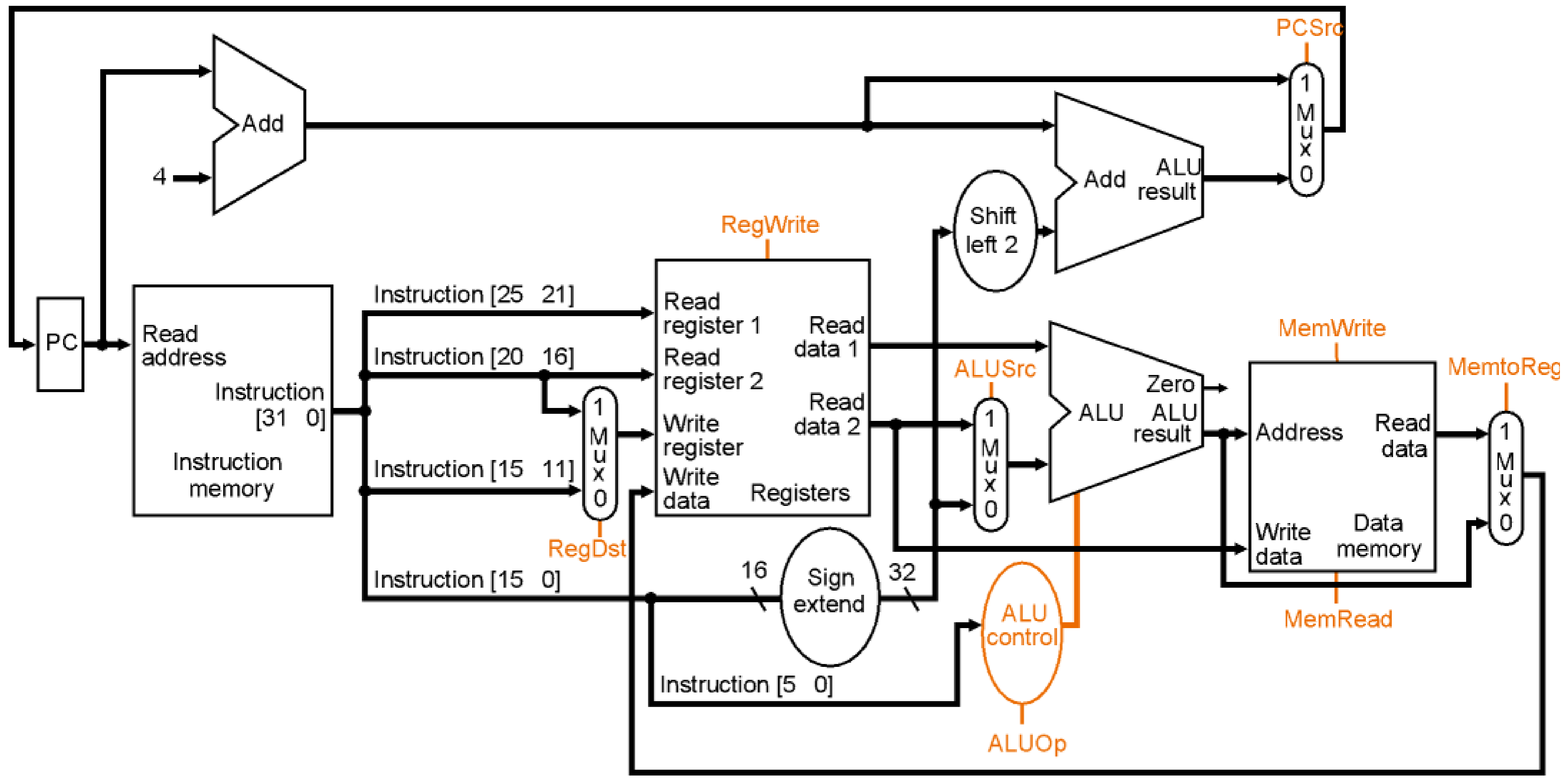


The Branch (beq) Datapath



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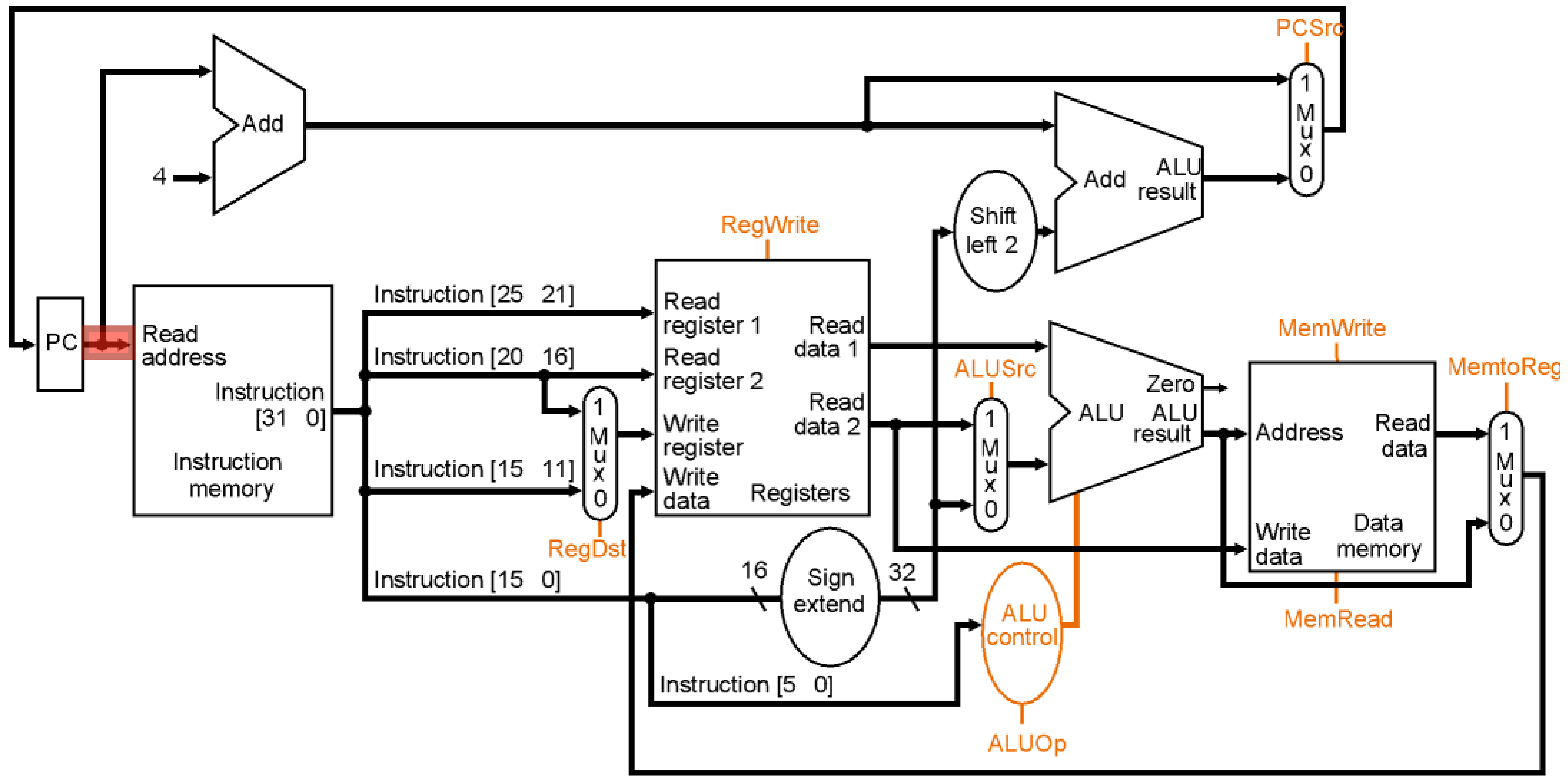

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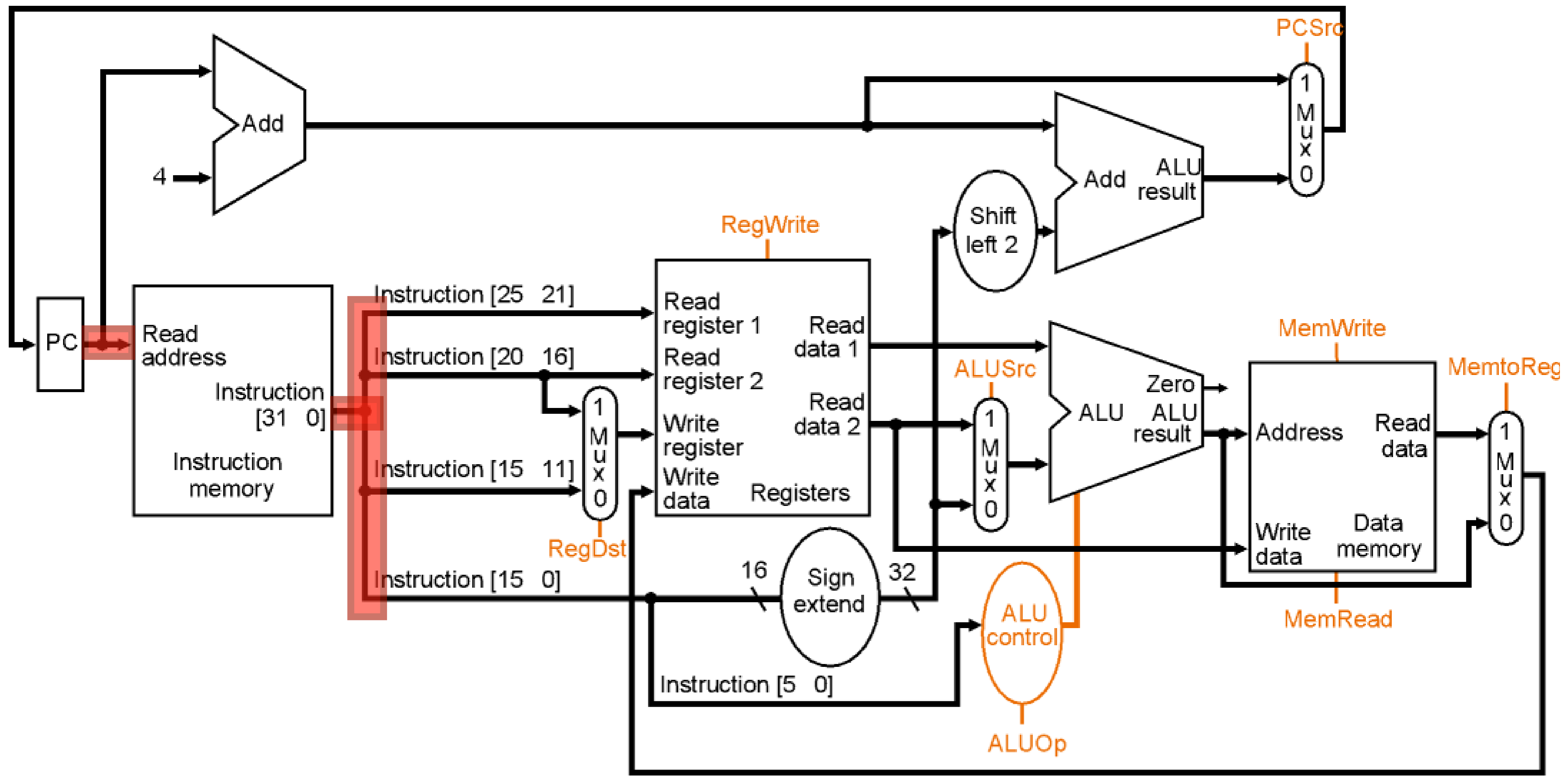

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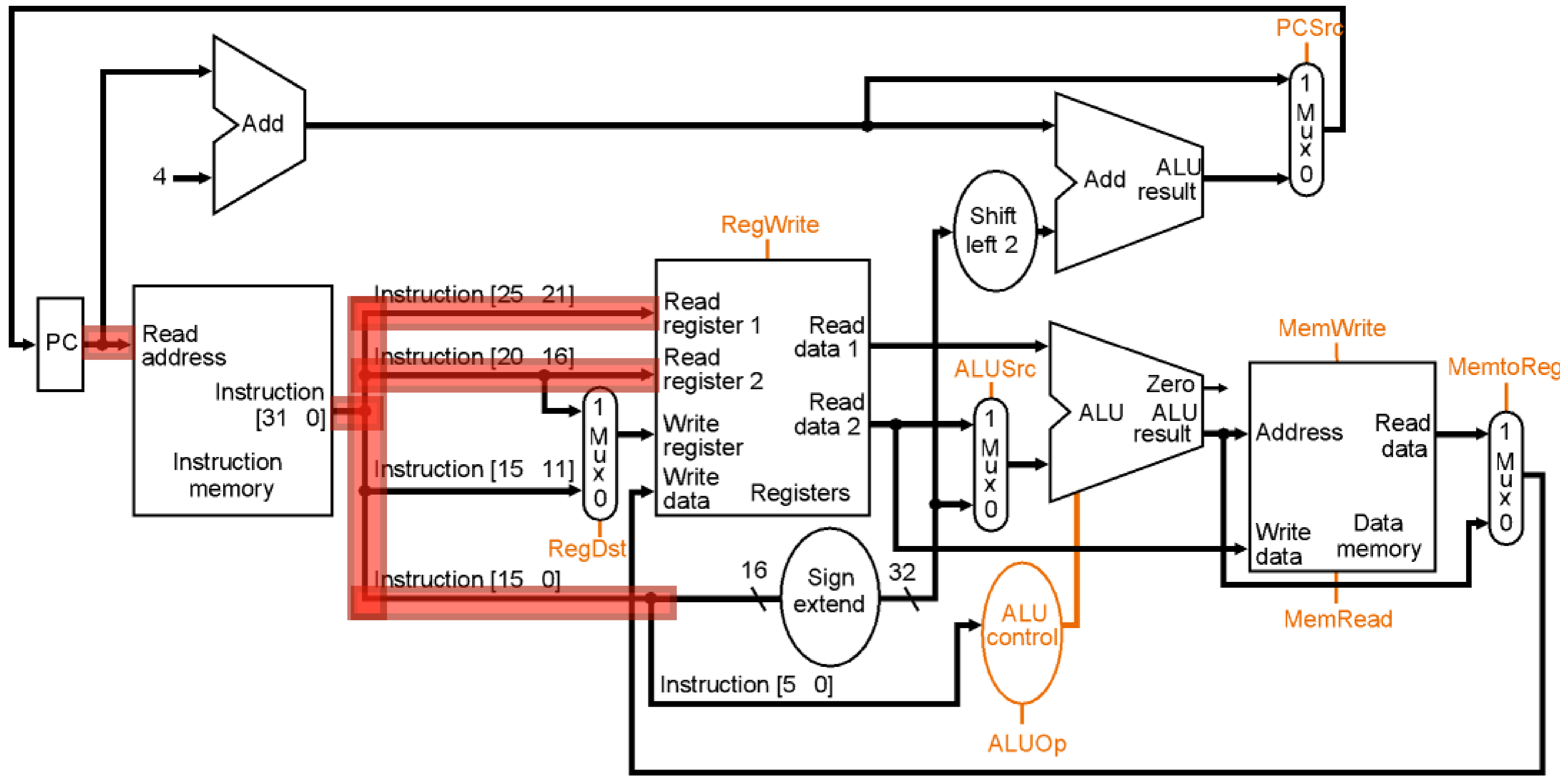

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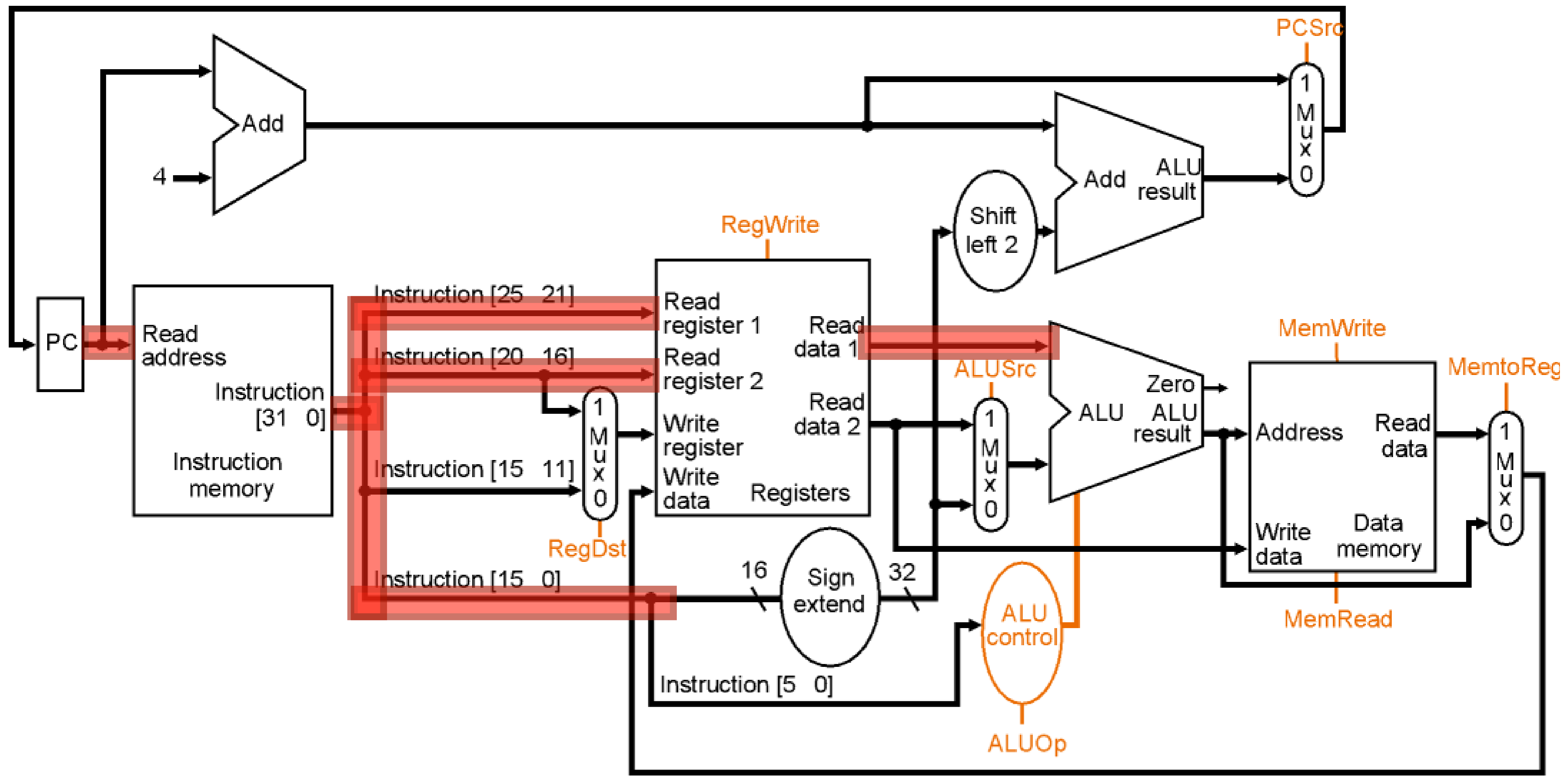

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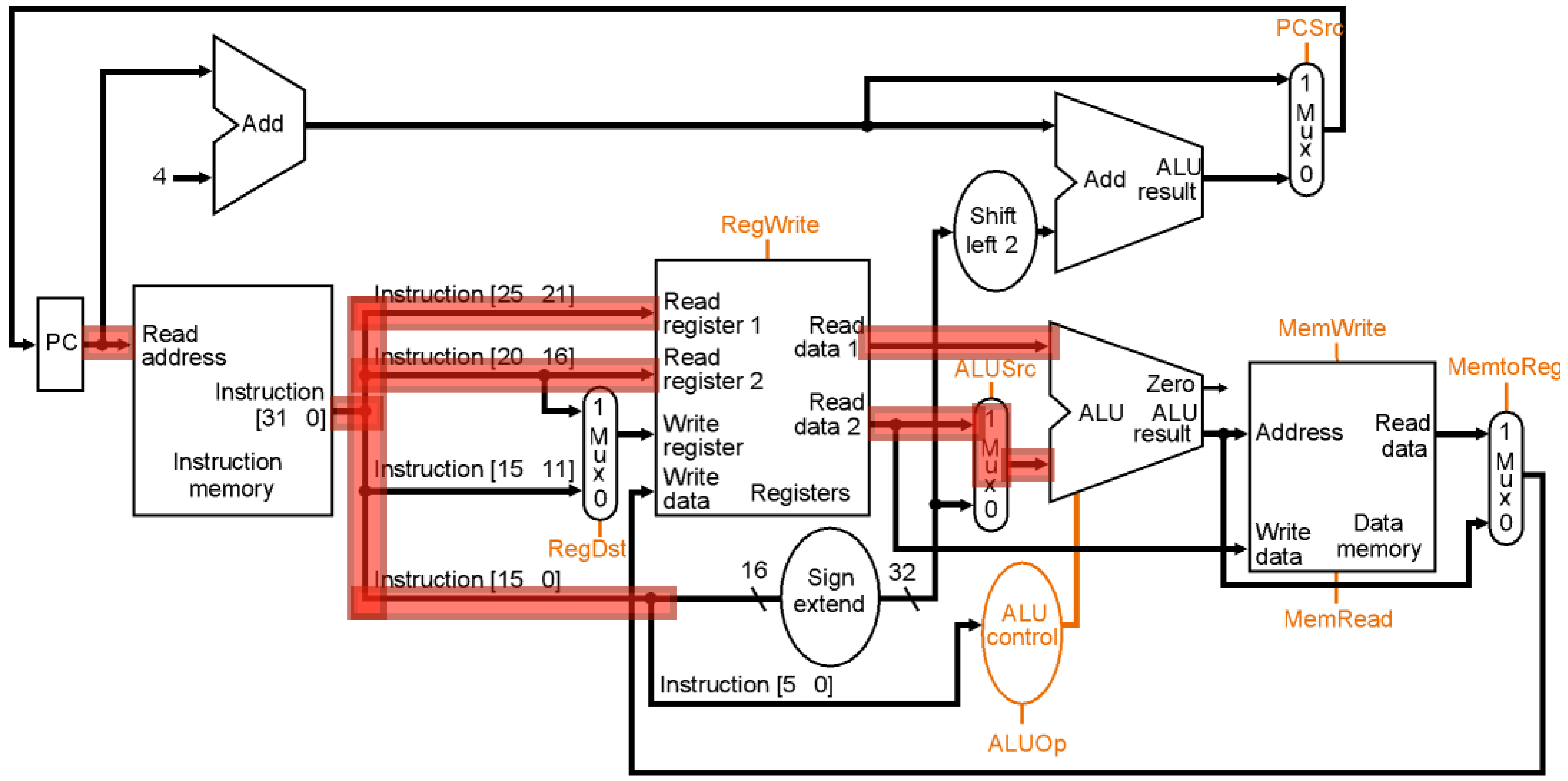

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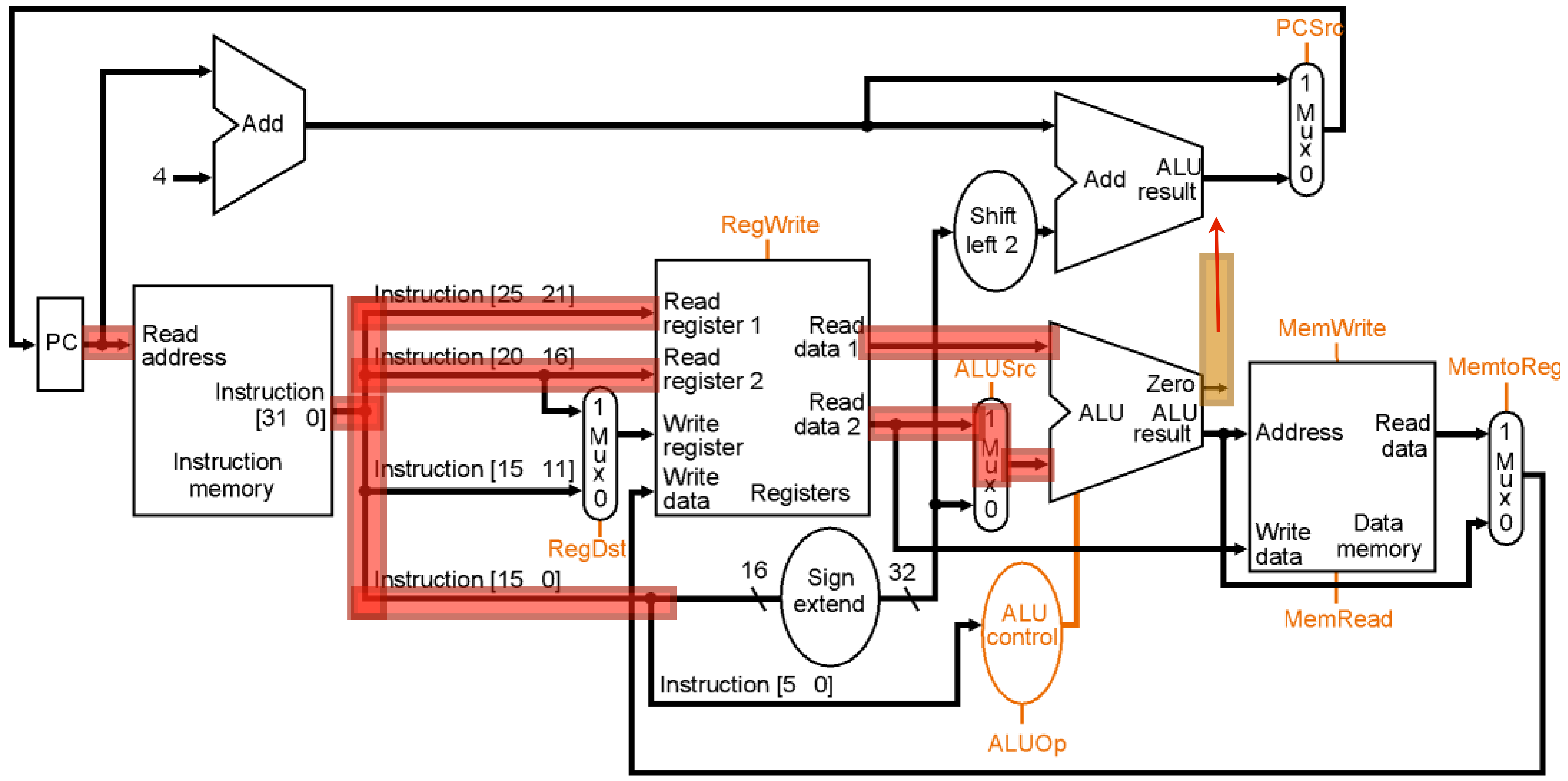

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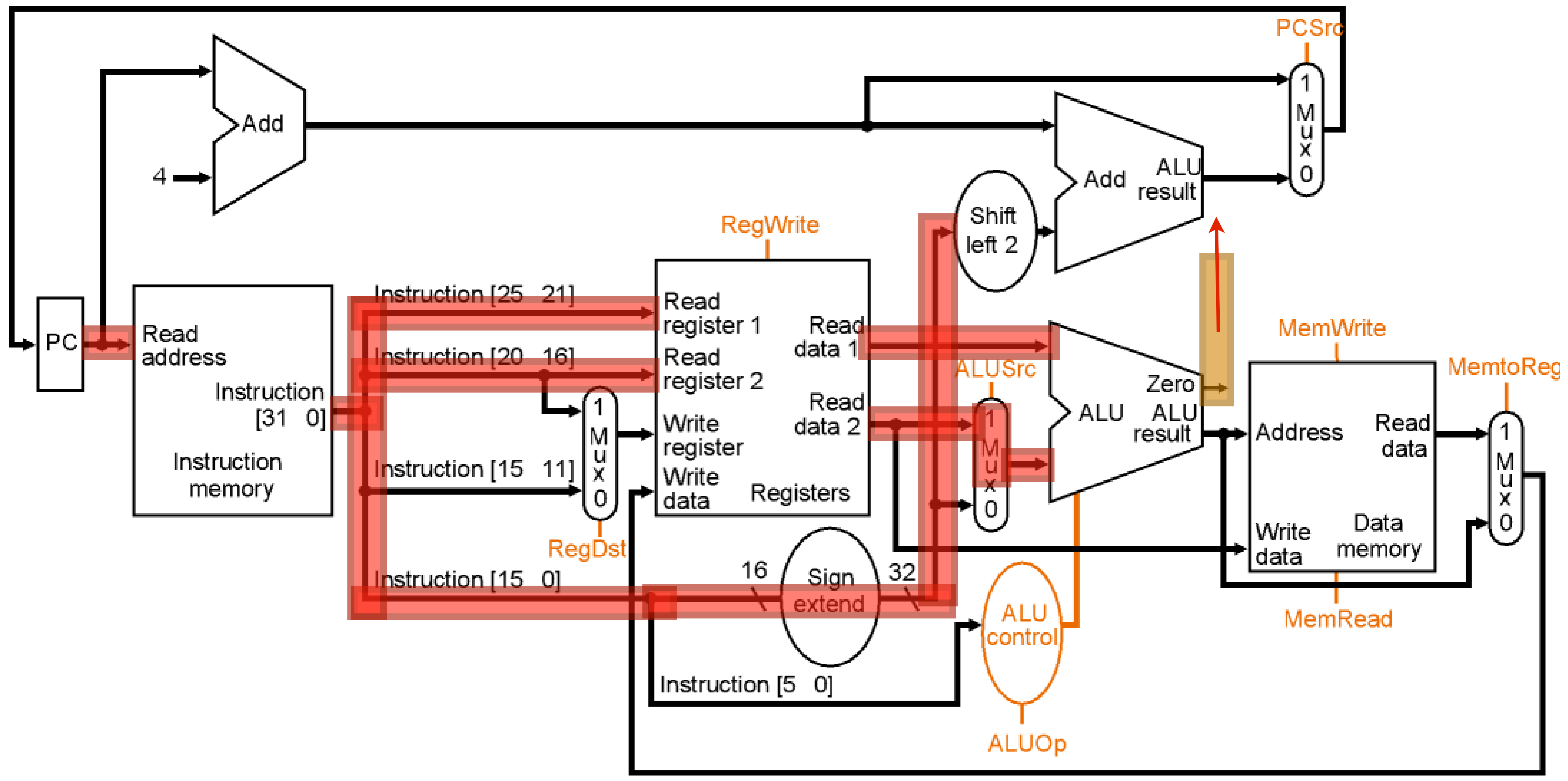

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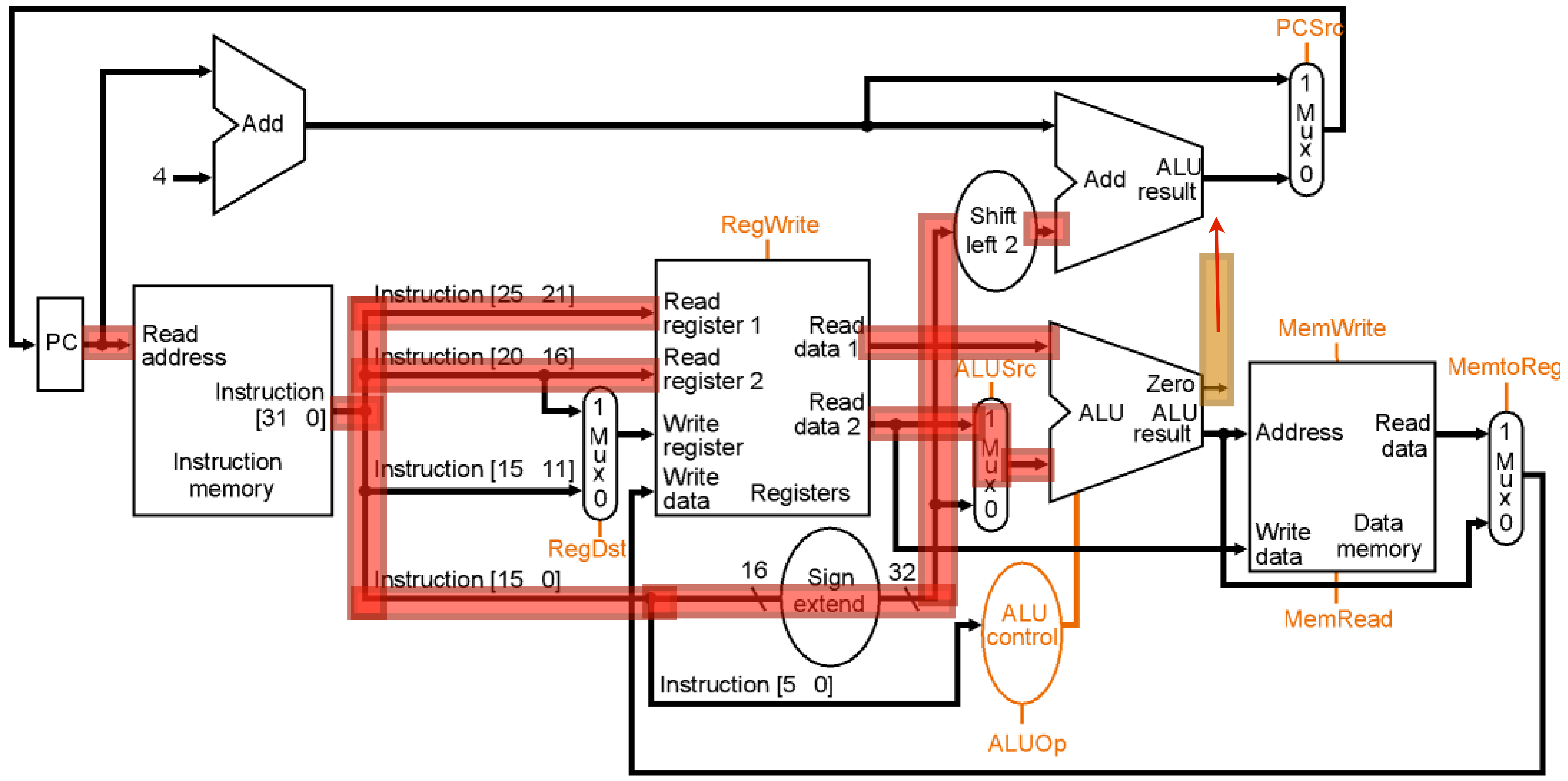

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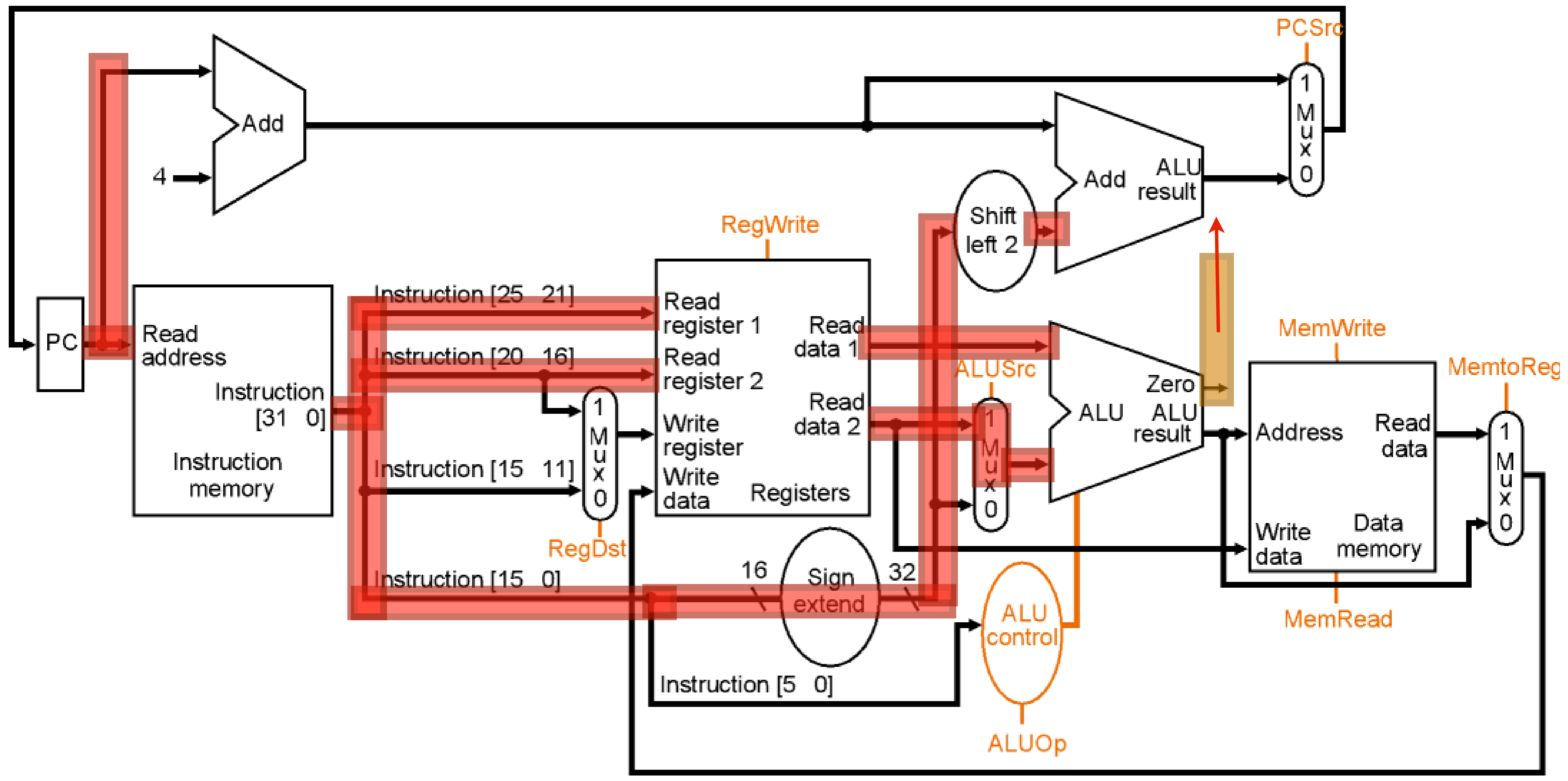

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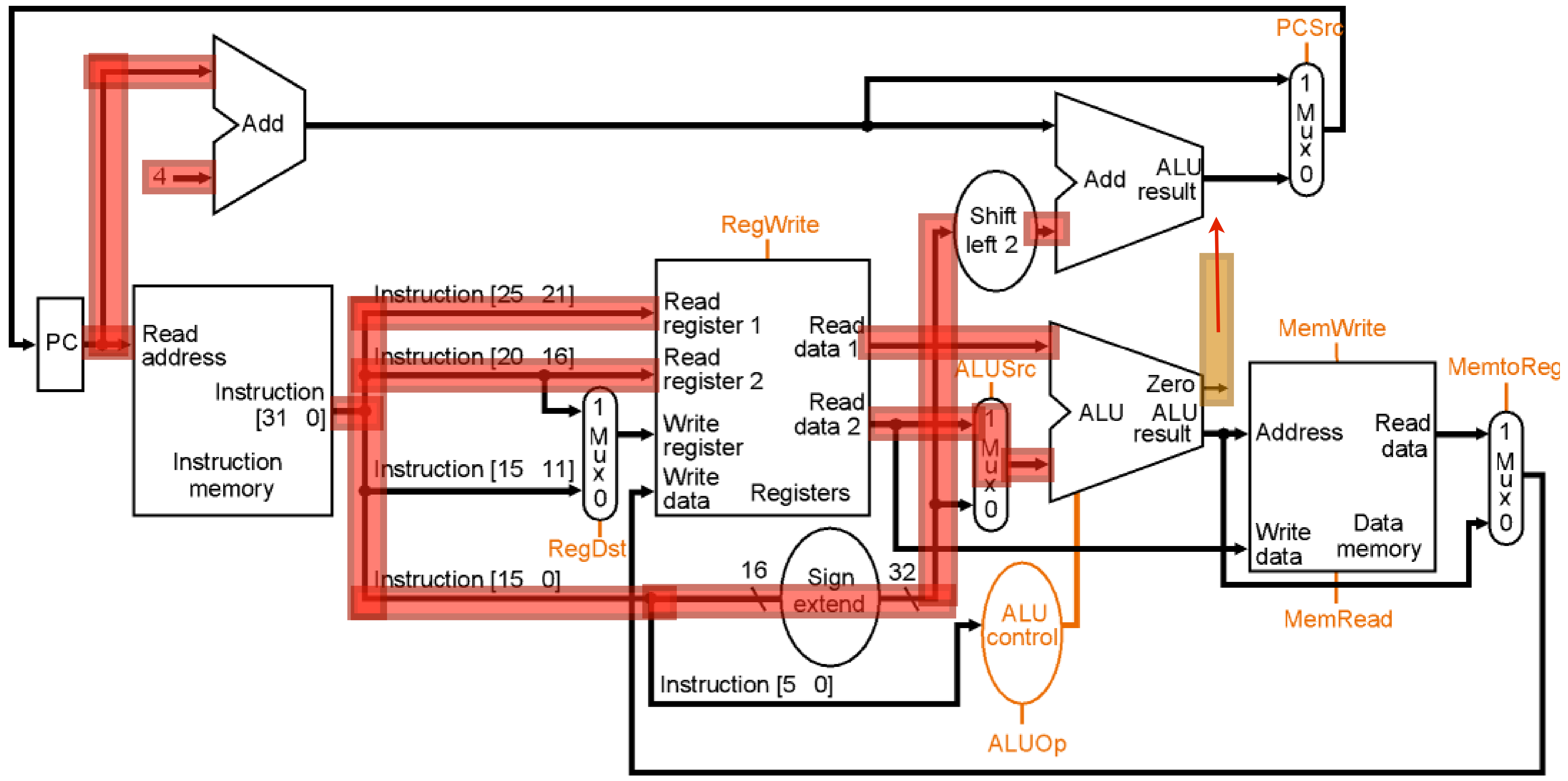

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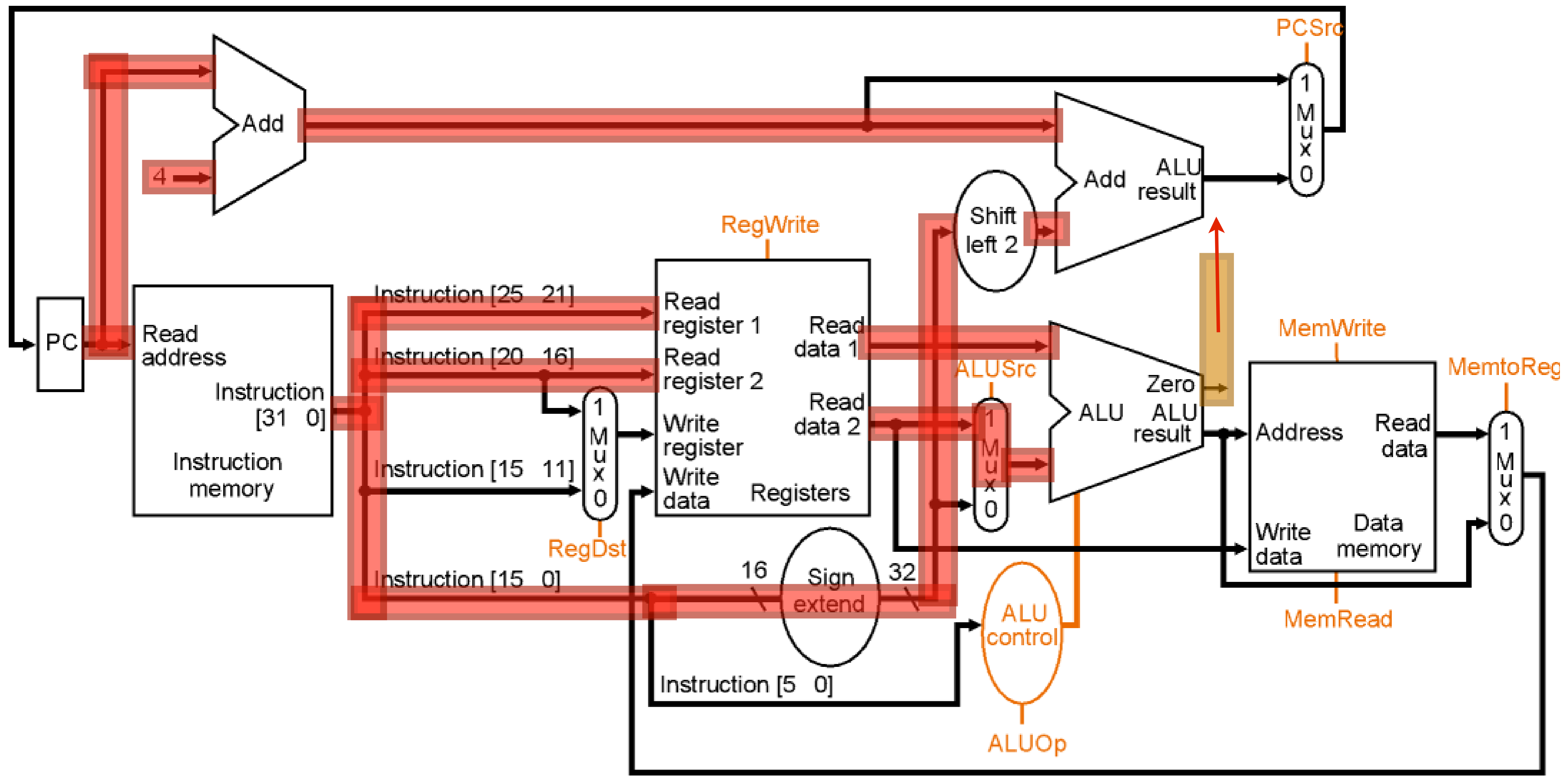

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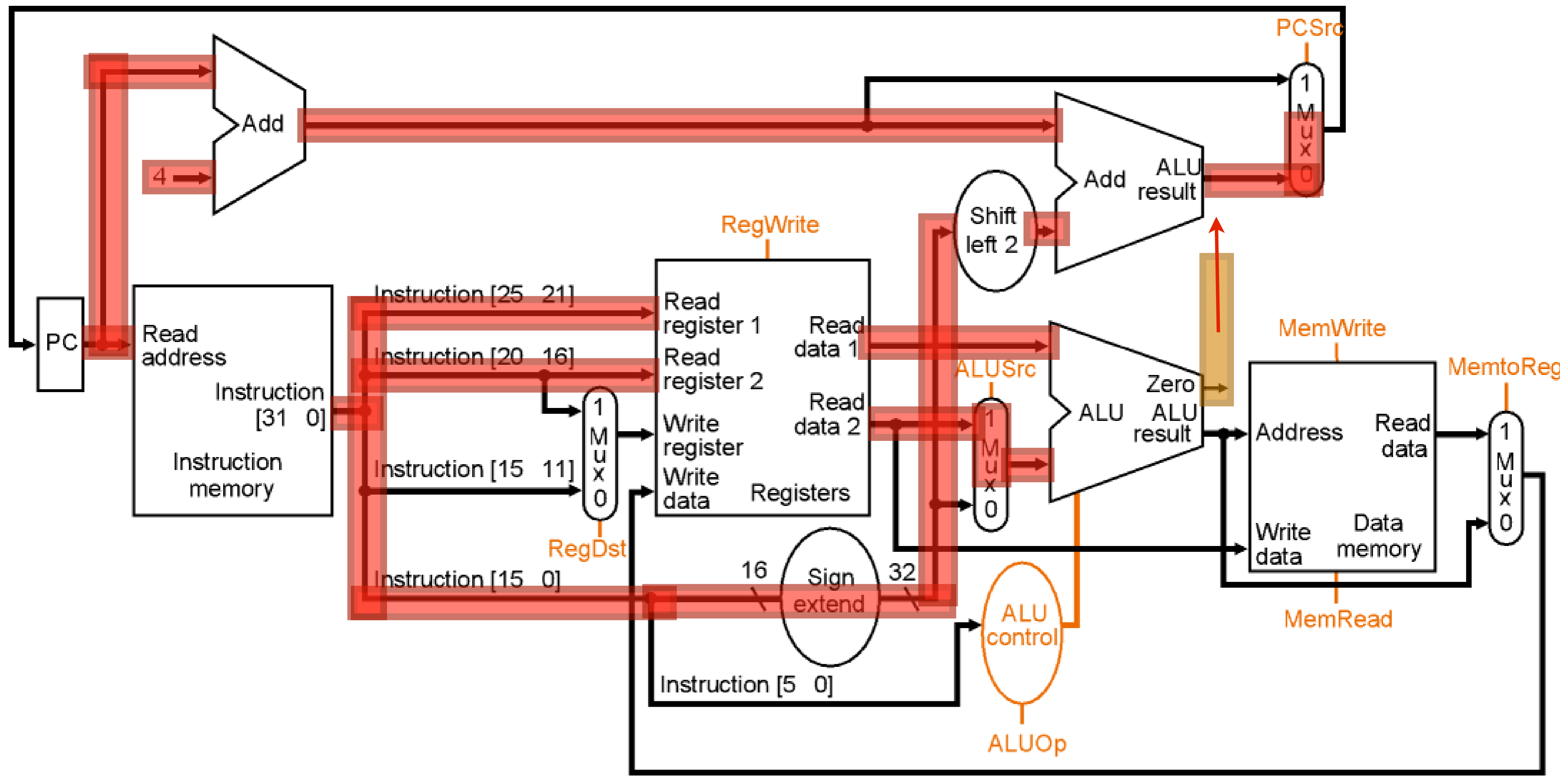

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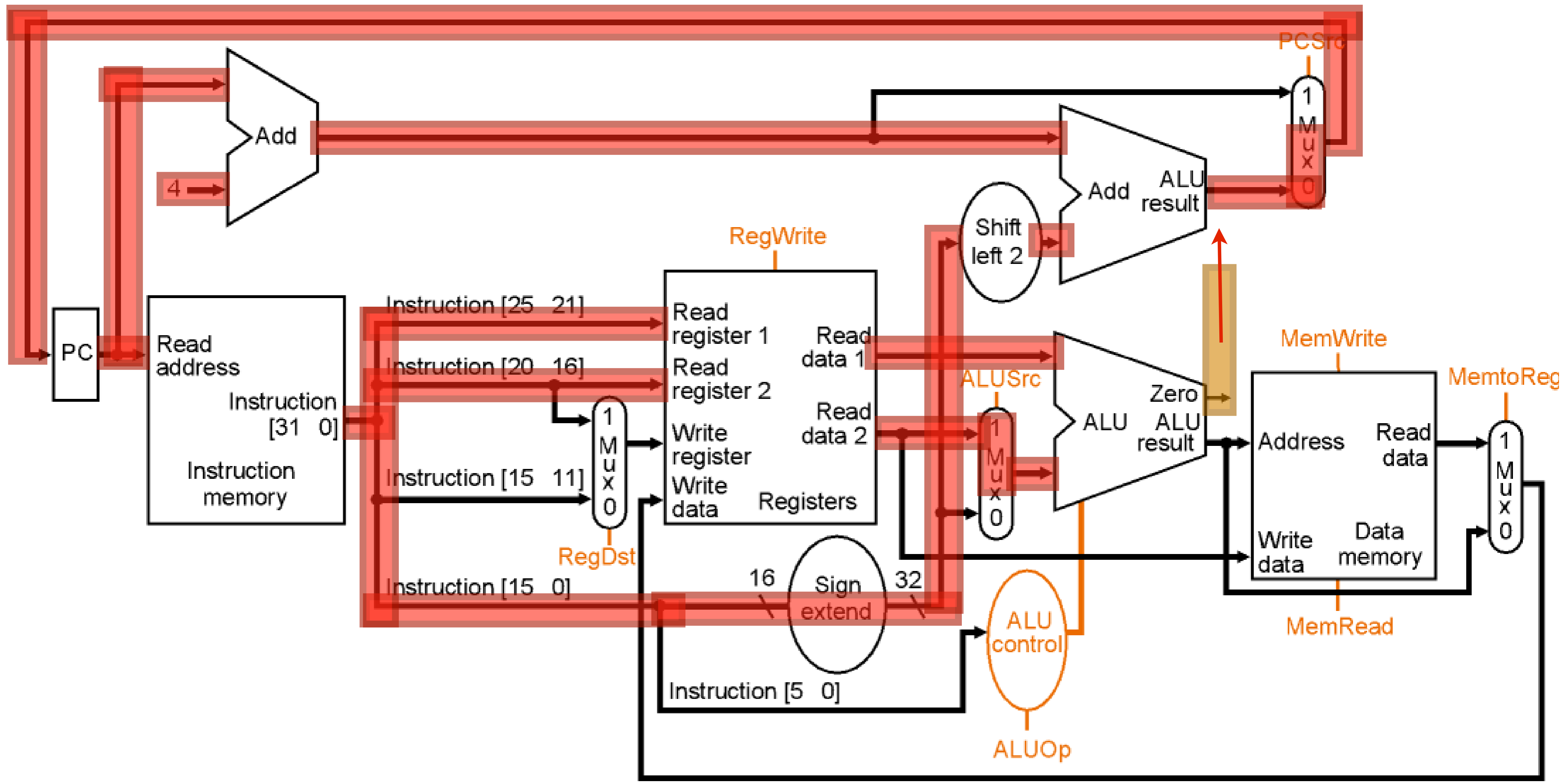

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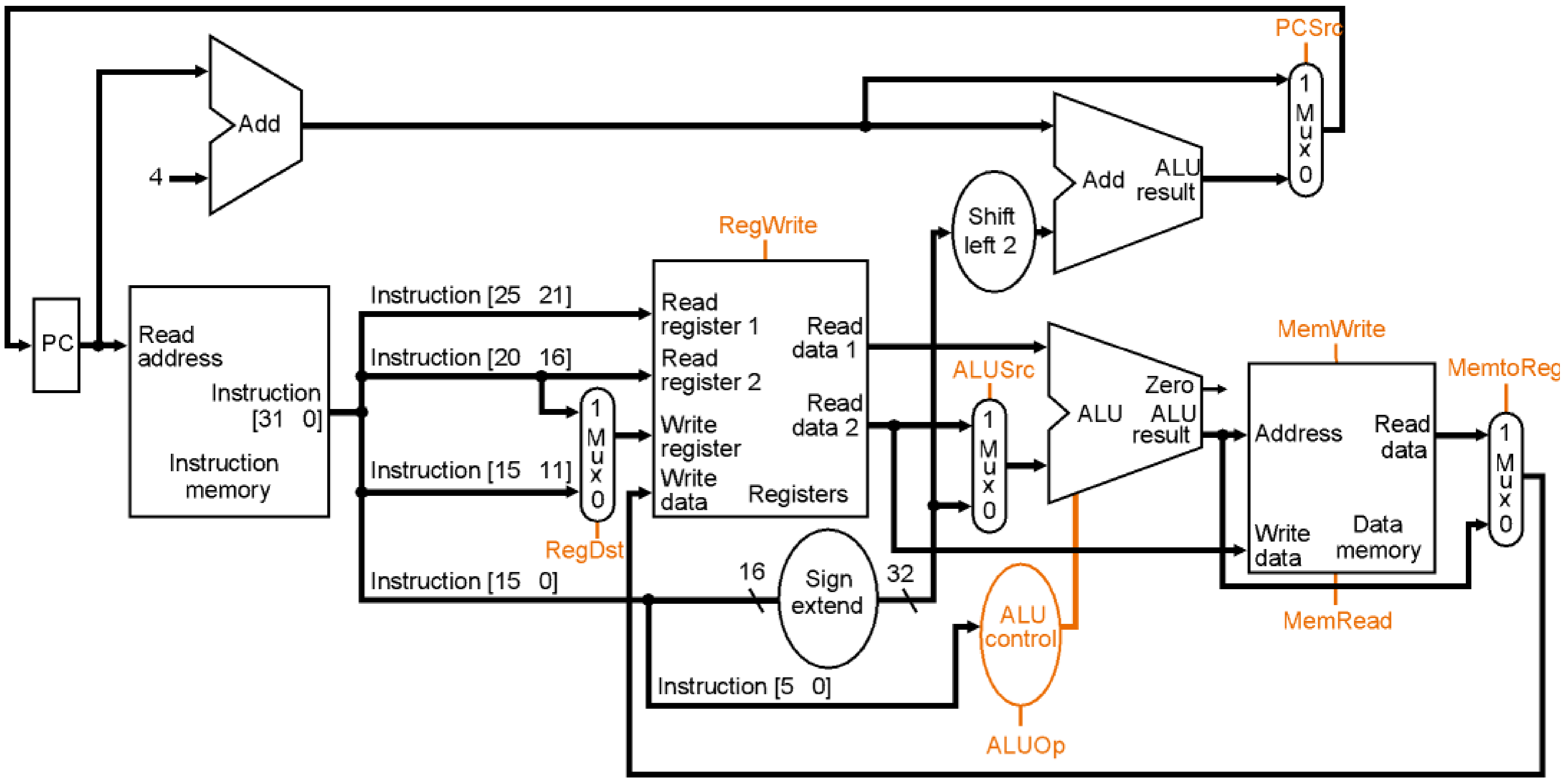

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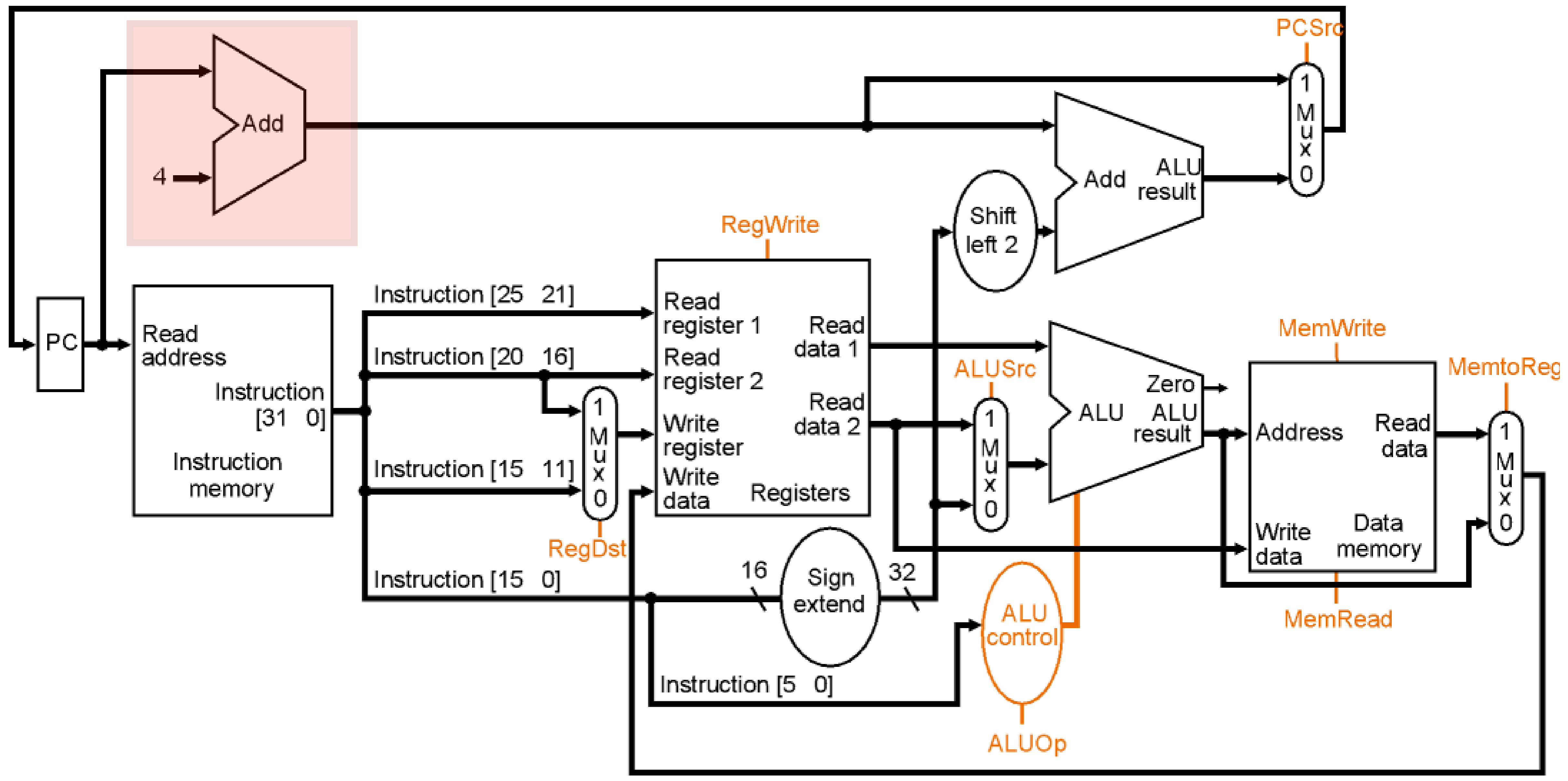

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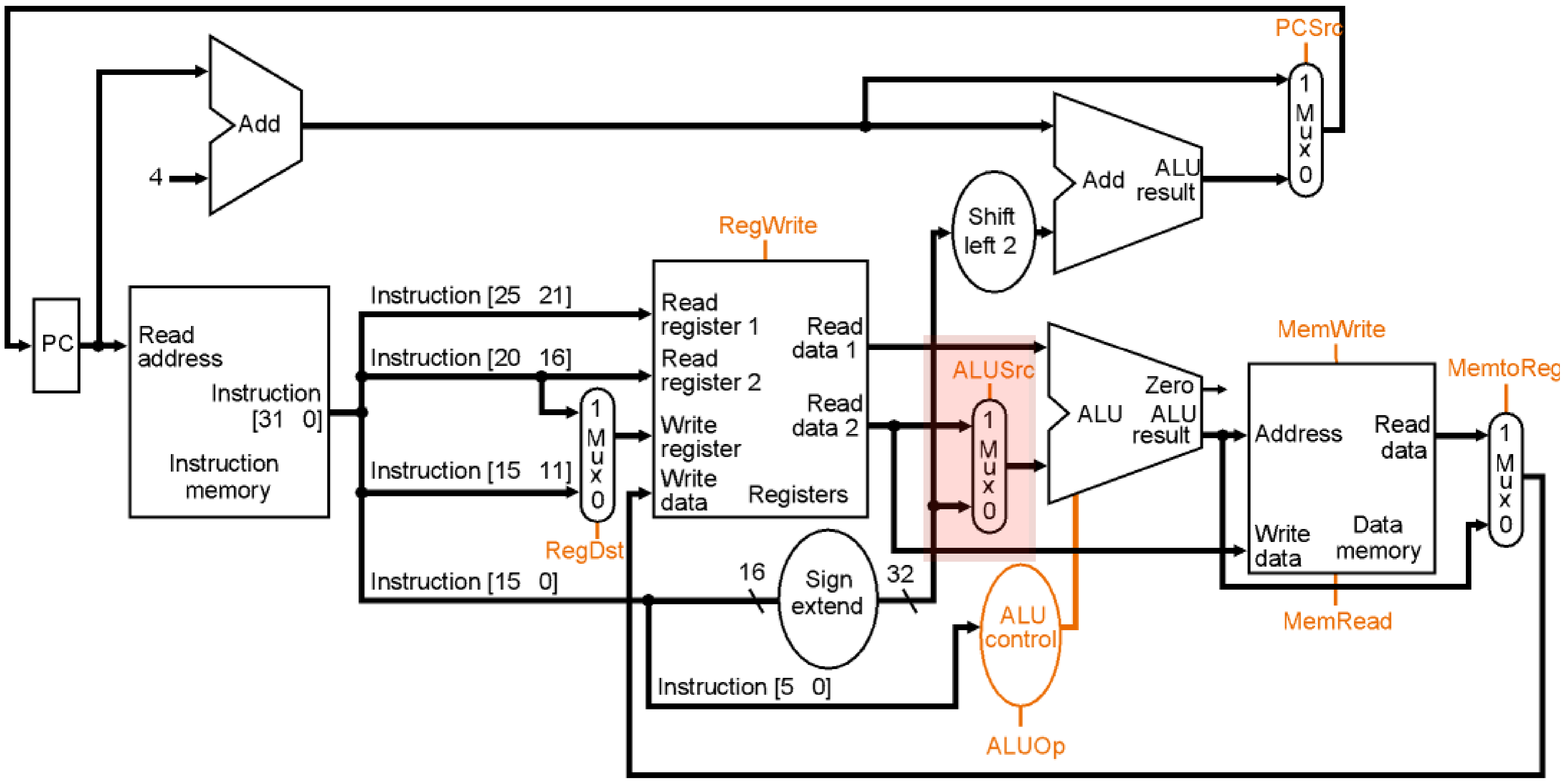

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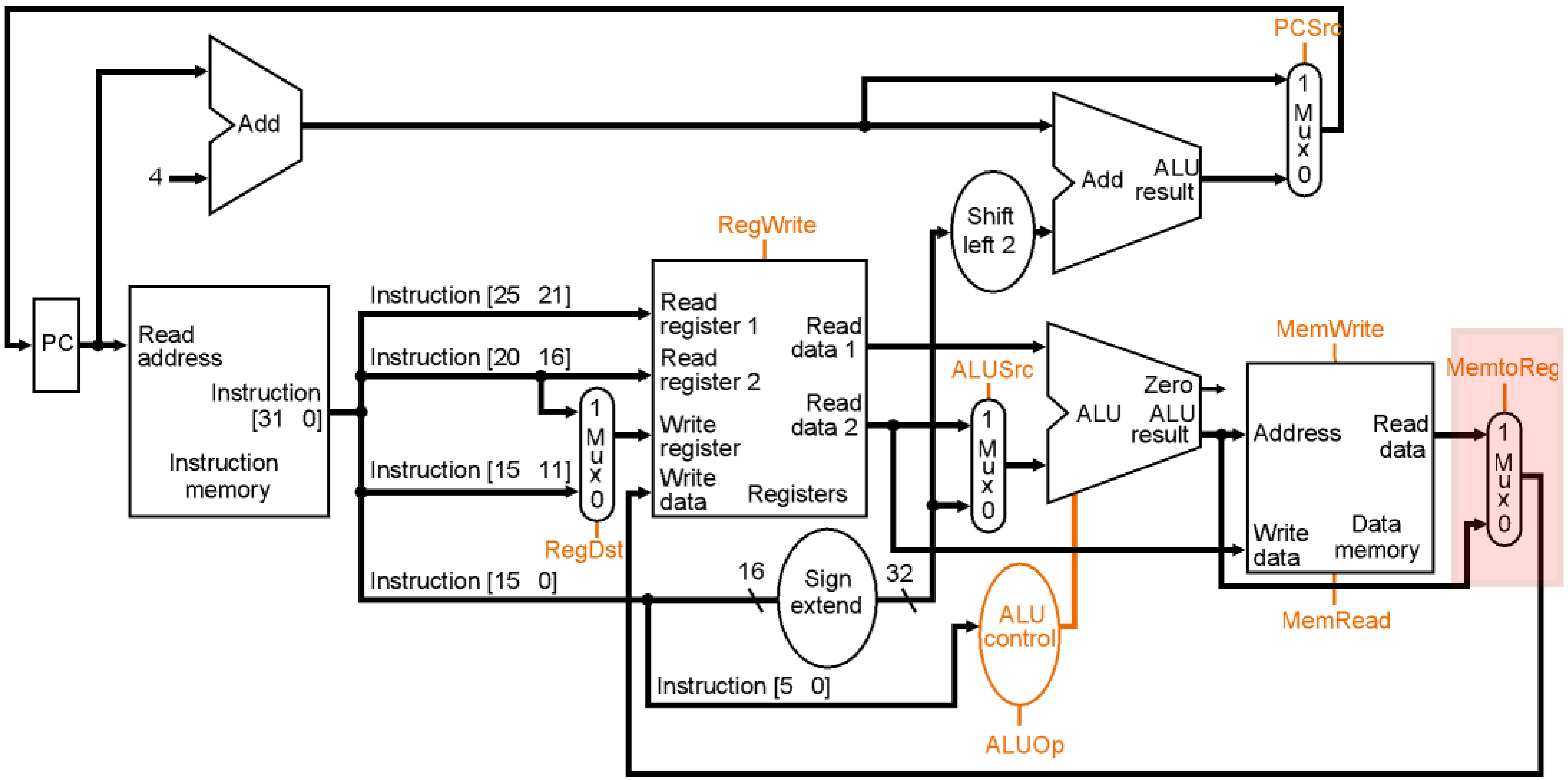

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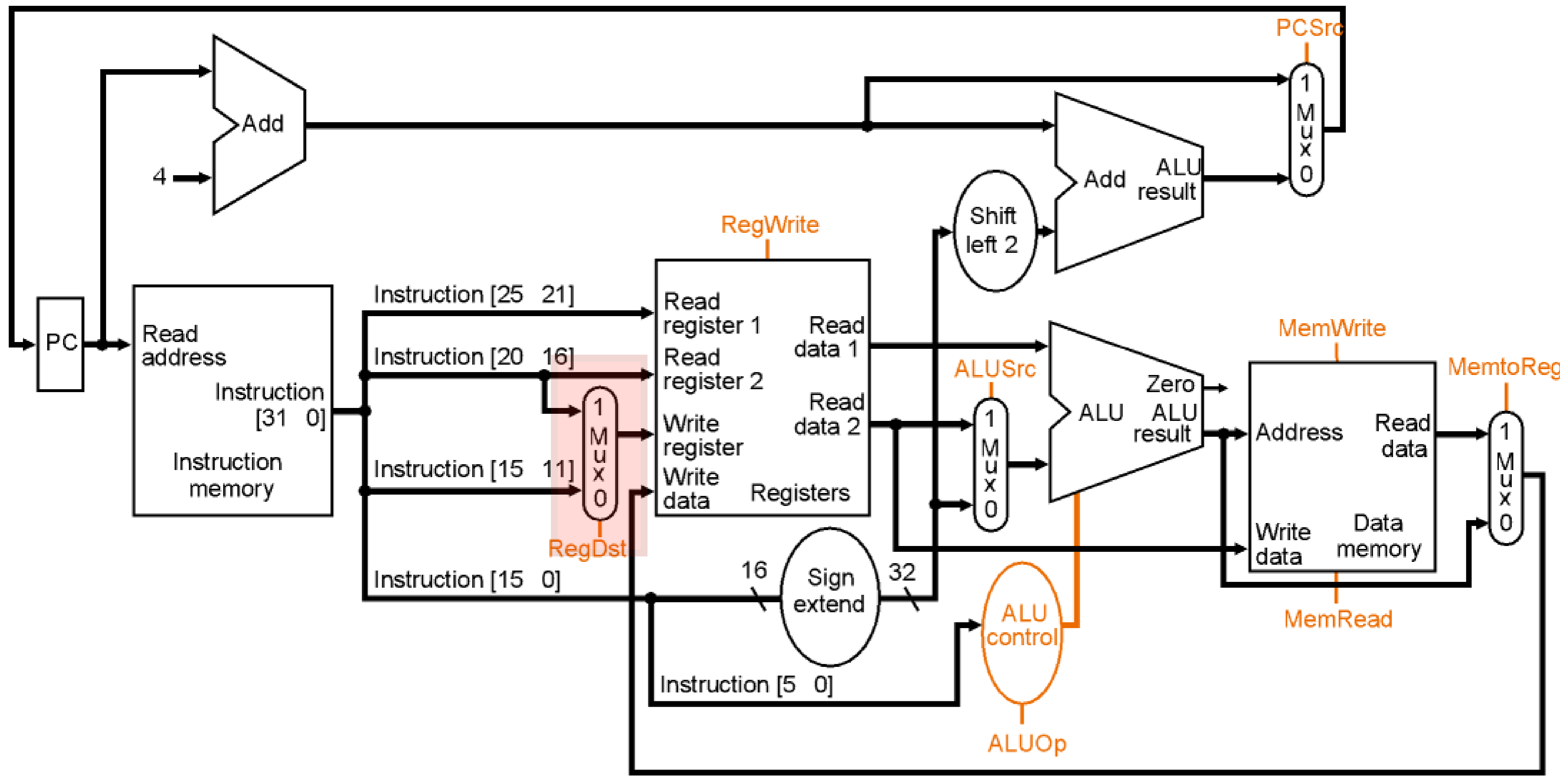

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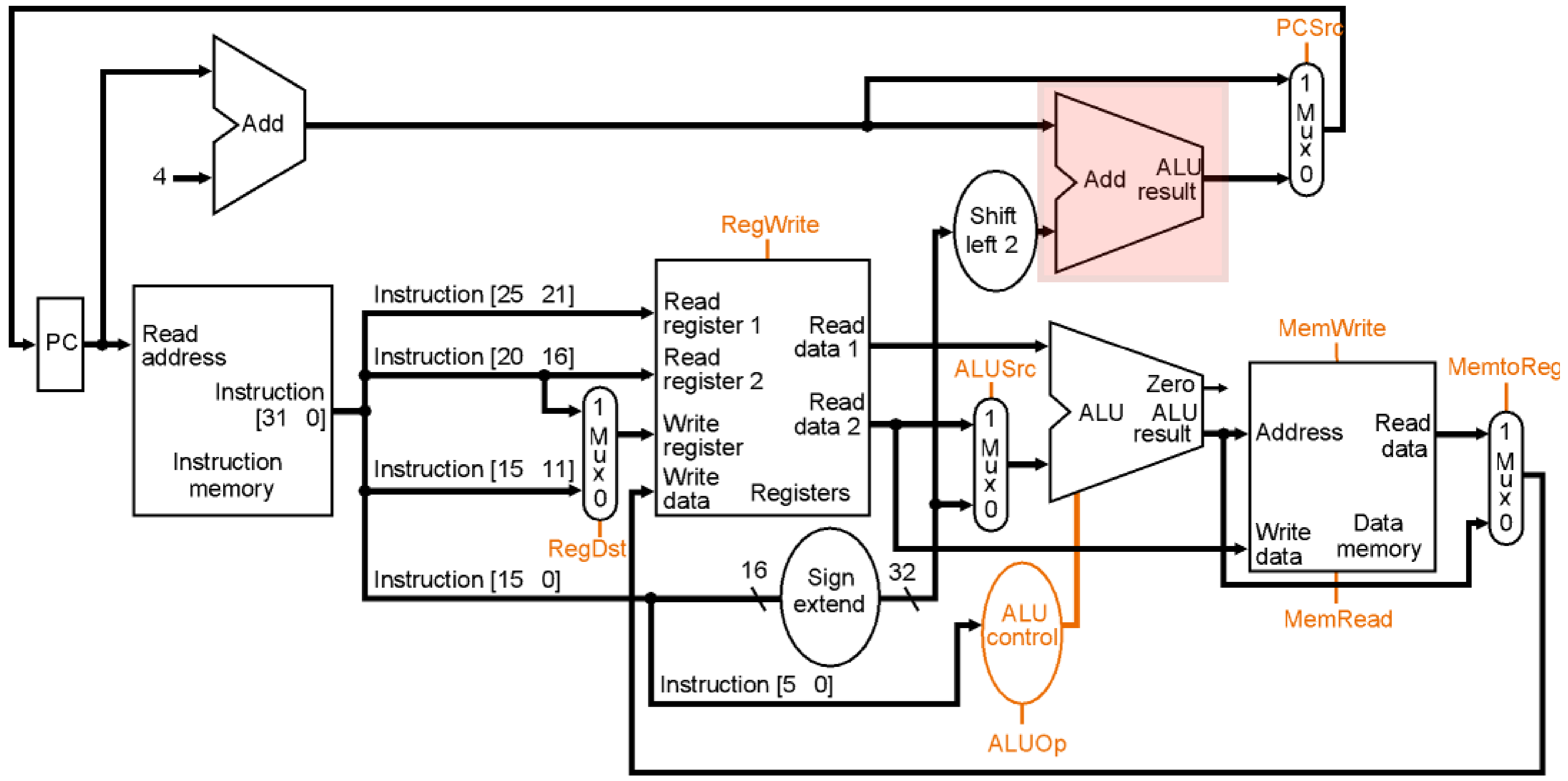

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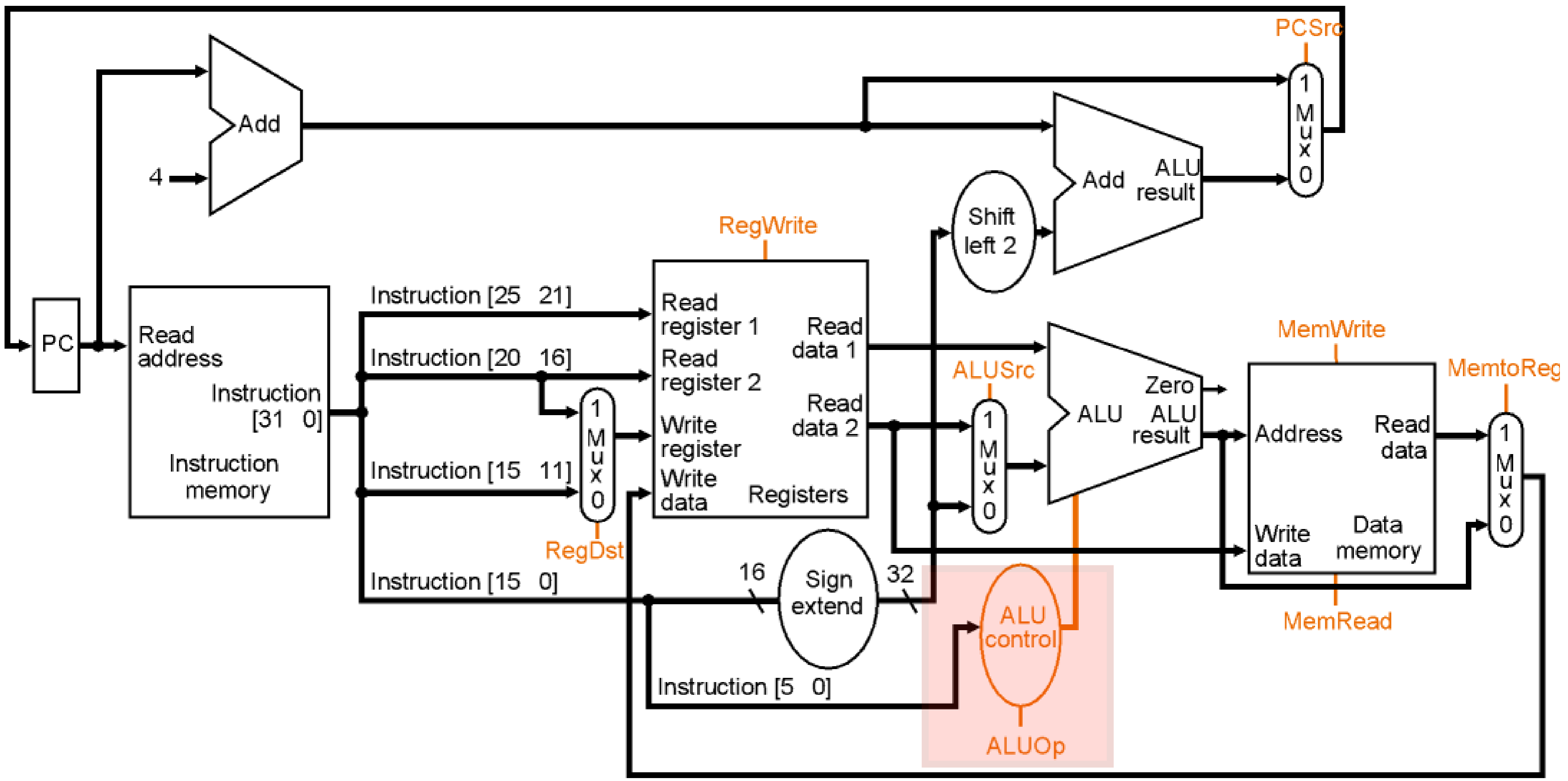

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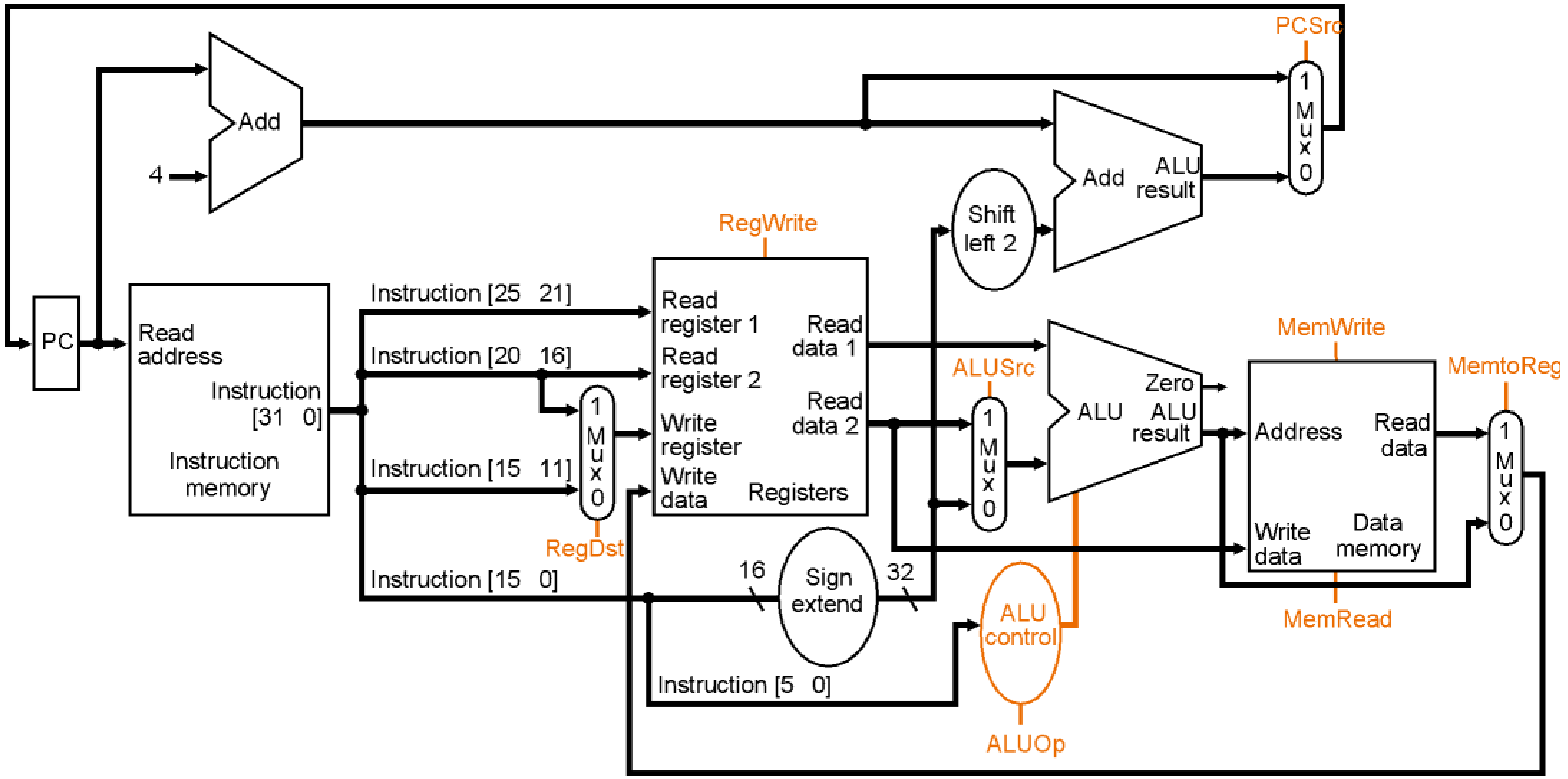

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- CPU is just a collection of state and combinational logic
- We just designed a very rich processor, at least in terms of functionality
- ET = IC * CPI * Cycle Time
    - where does the single-cycle machine fit in?

The Control Unit

Putting it All Together: A Single Cycle Datapath

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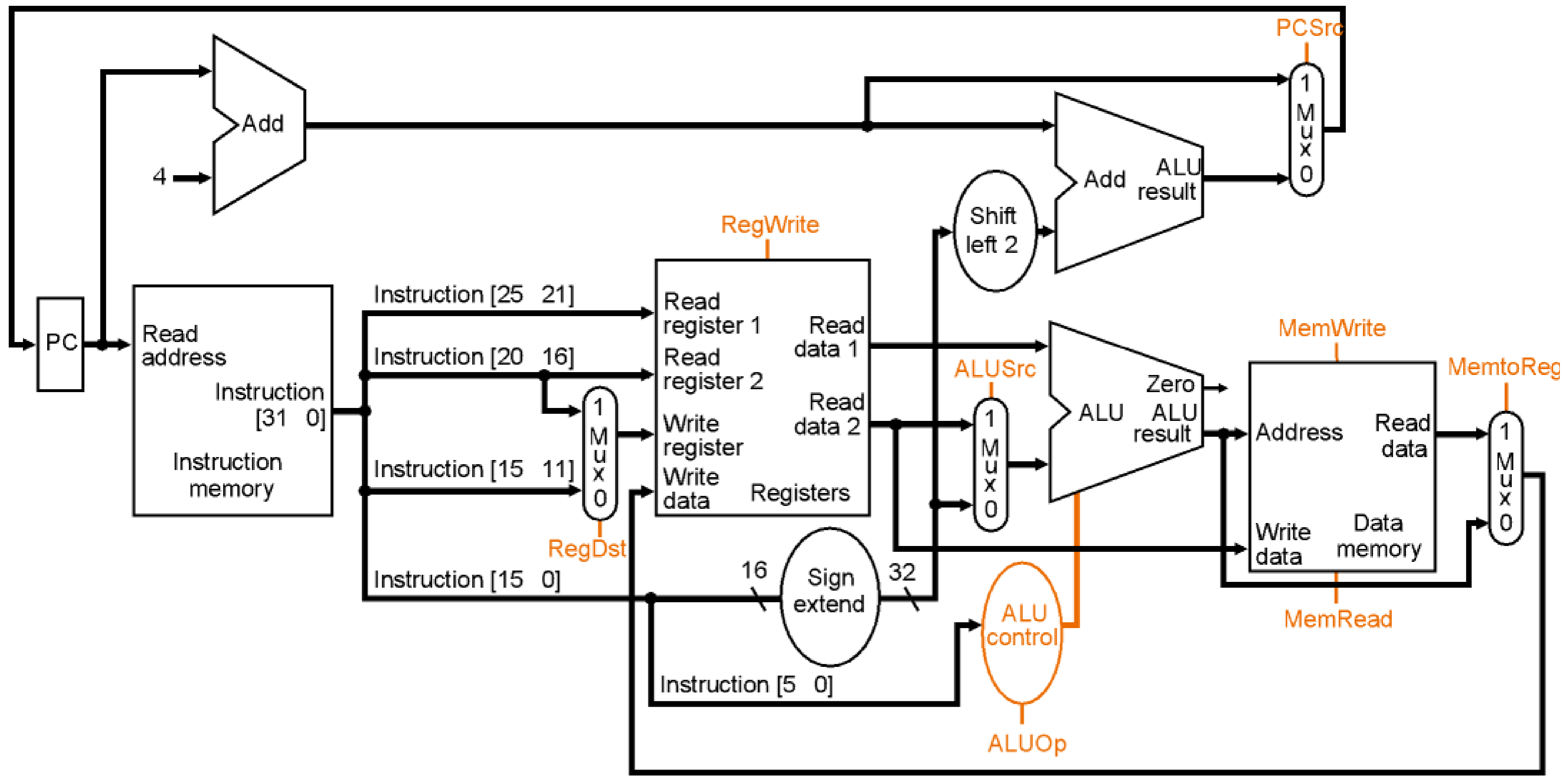

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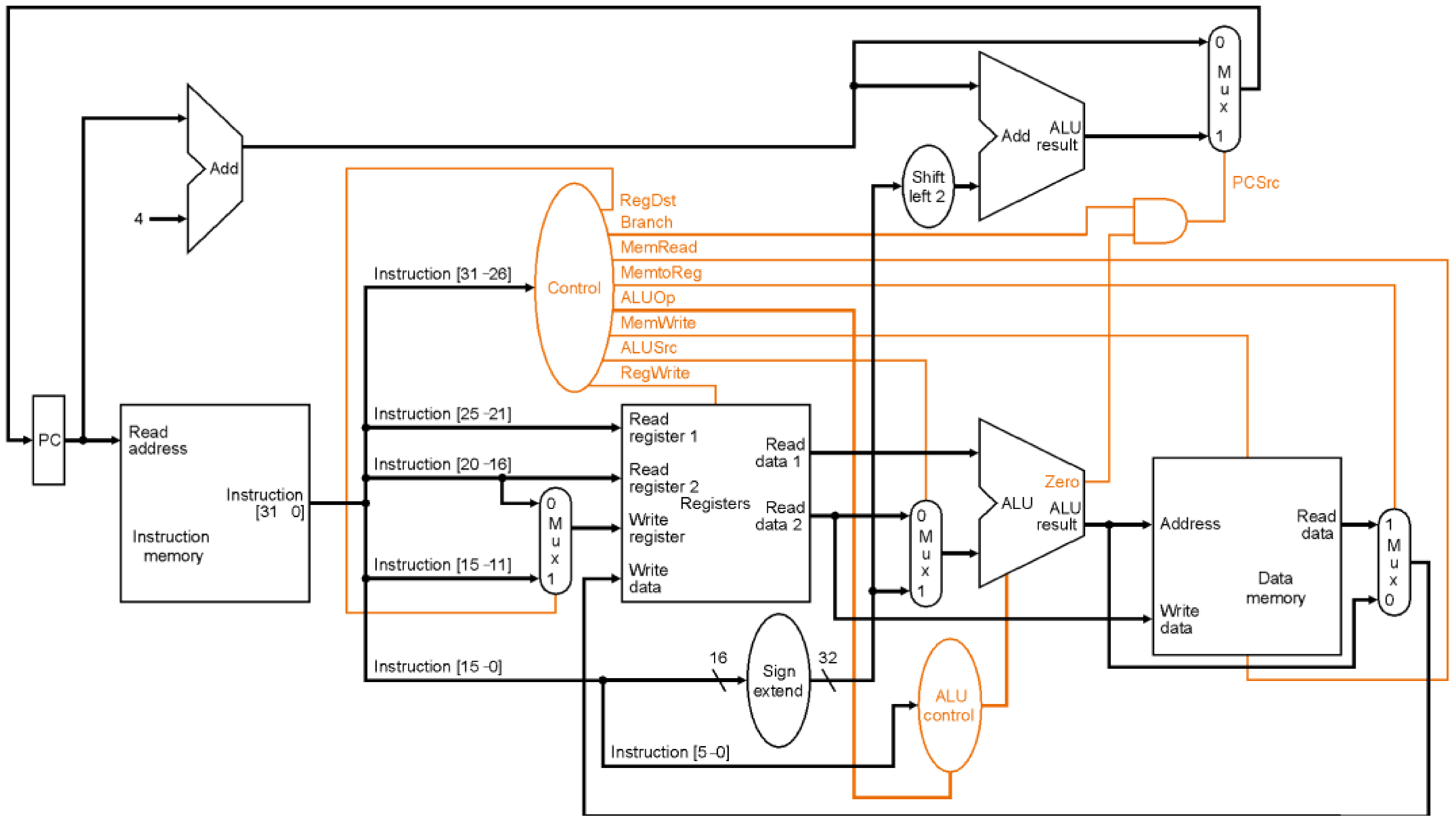

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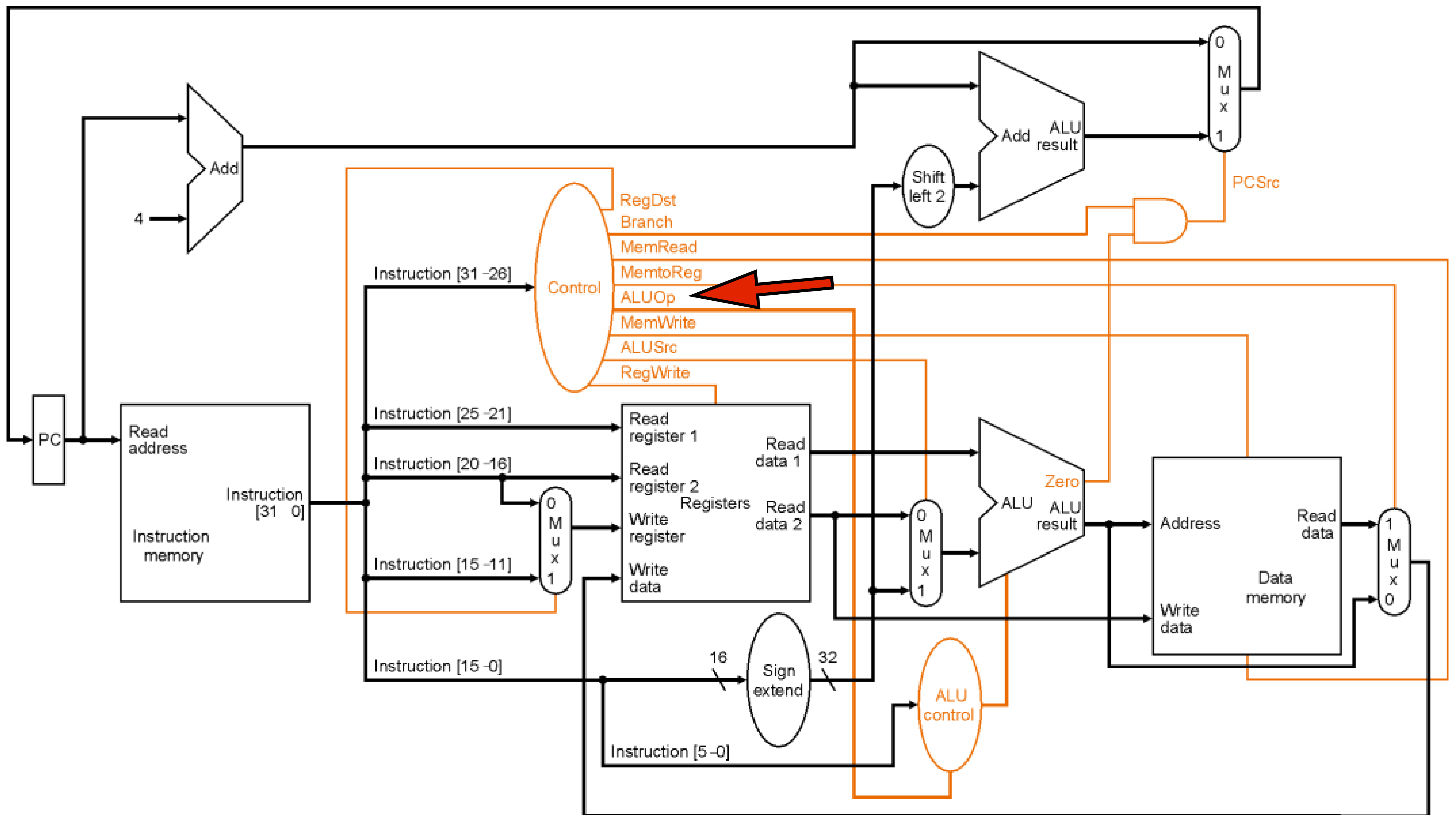

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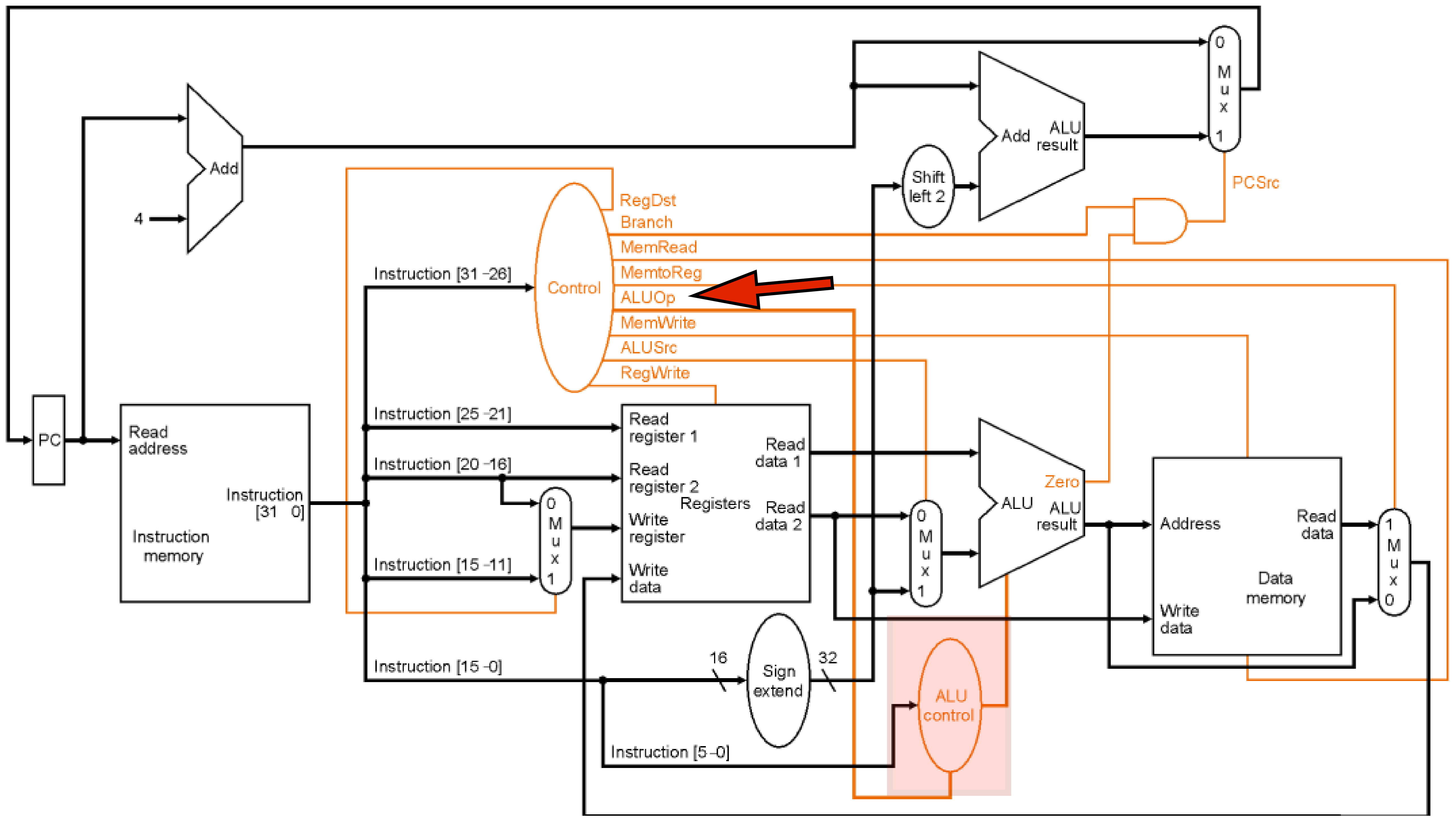


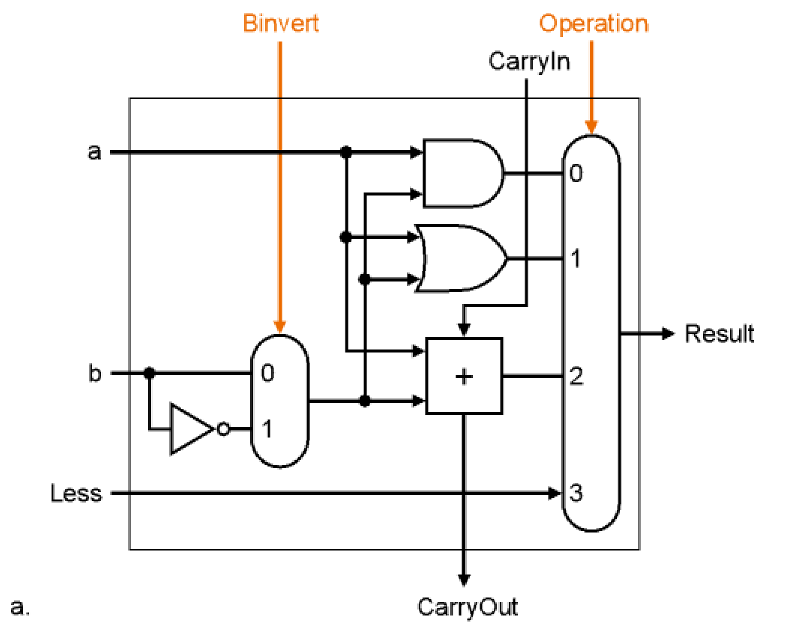
ALU Control Bits

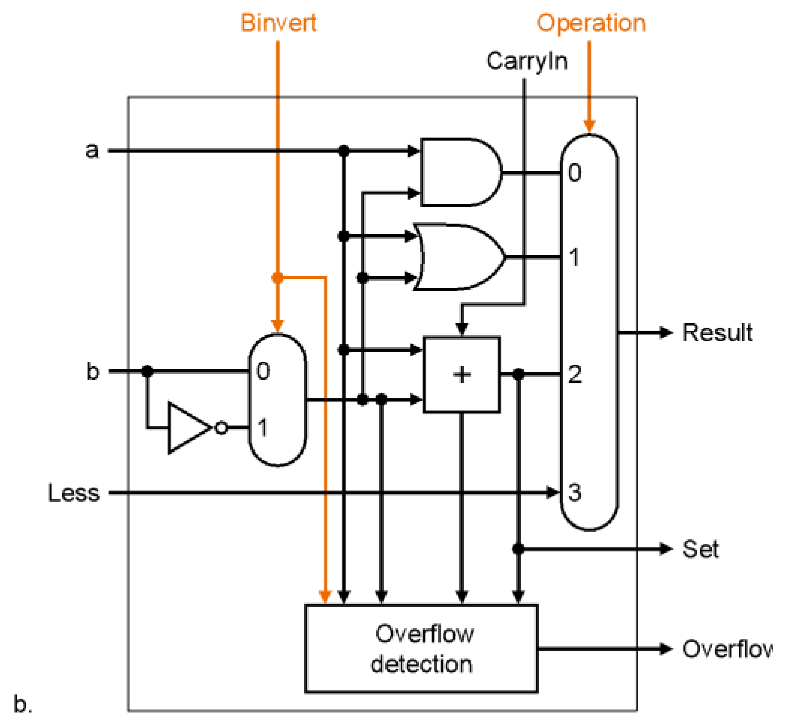
- 5-Function ALU

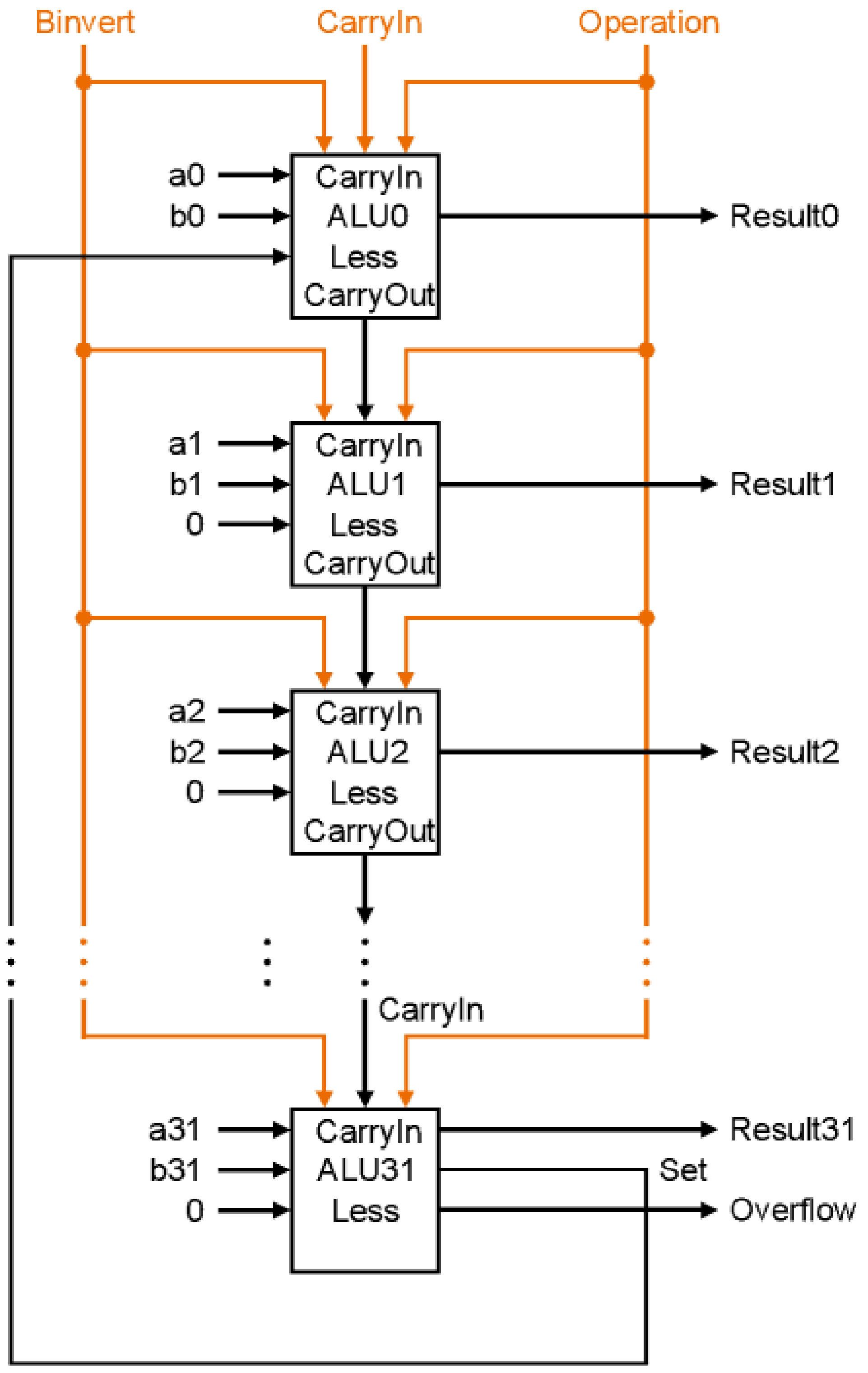
ALU control input	Function	Operations
000	And	and
001	Or	or
010	Add	add, lw, sw
110	Subtract	sub, beq
111	Slt	slt

- Note: book also has NOR, not used - and a forth bit, not used

Full ALU

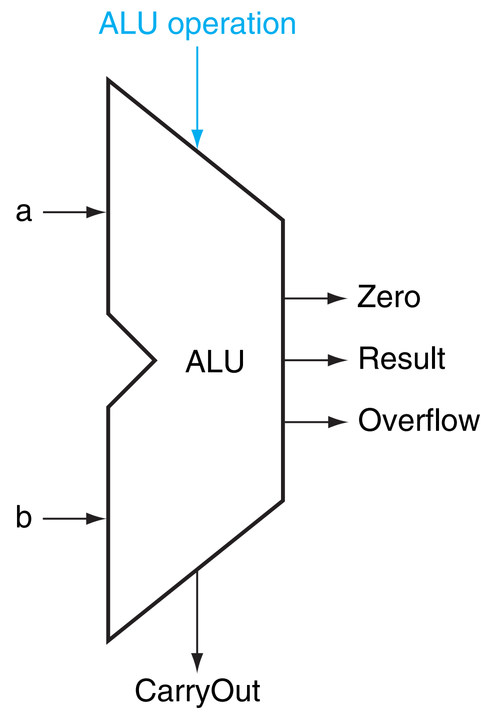






what signals accomplish:

	Binvert	CIn	Oper
add?			
sub?			
and?			
or?			
beq?			
slt?			



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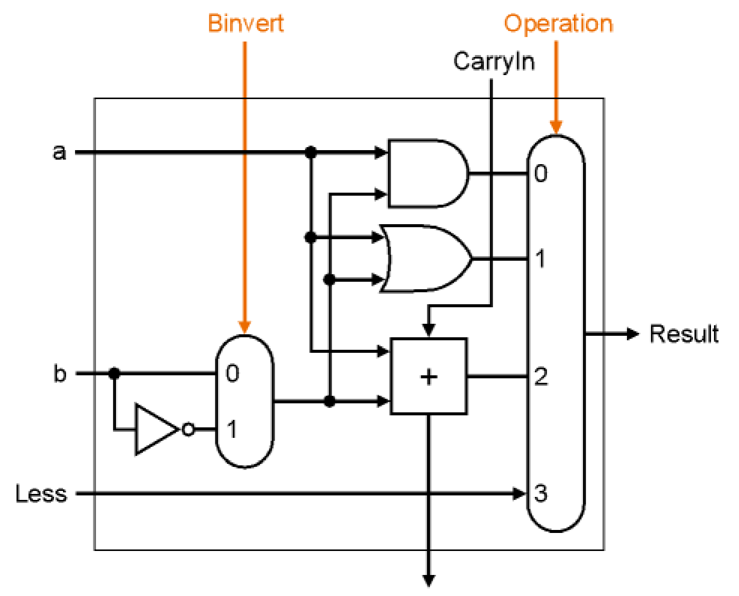

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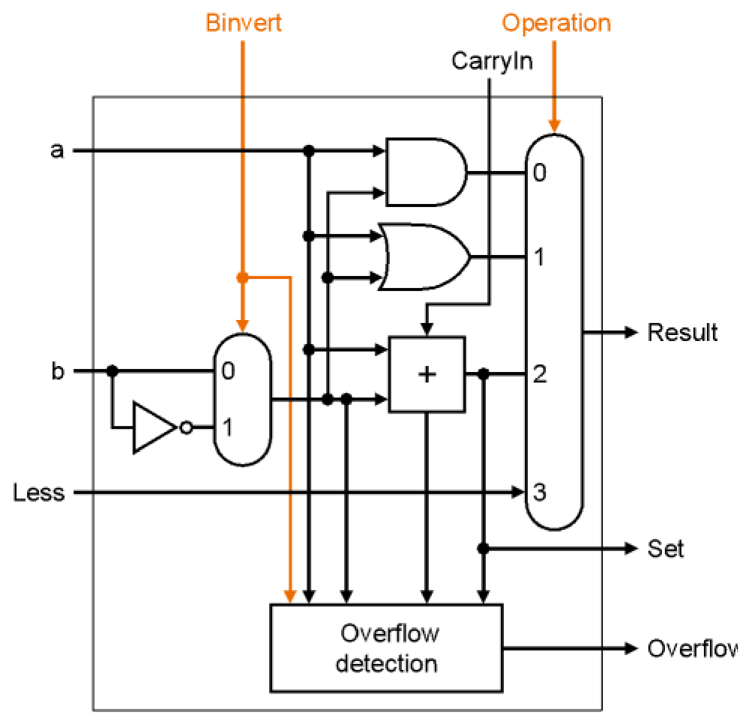

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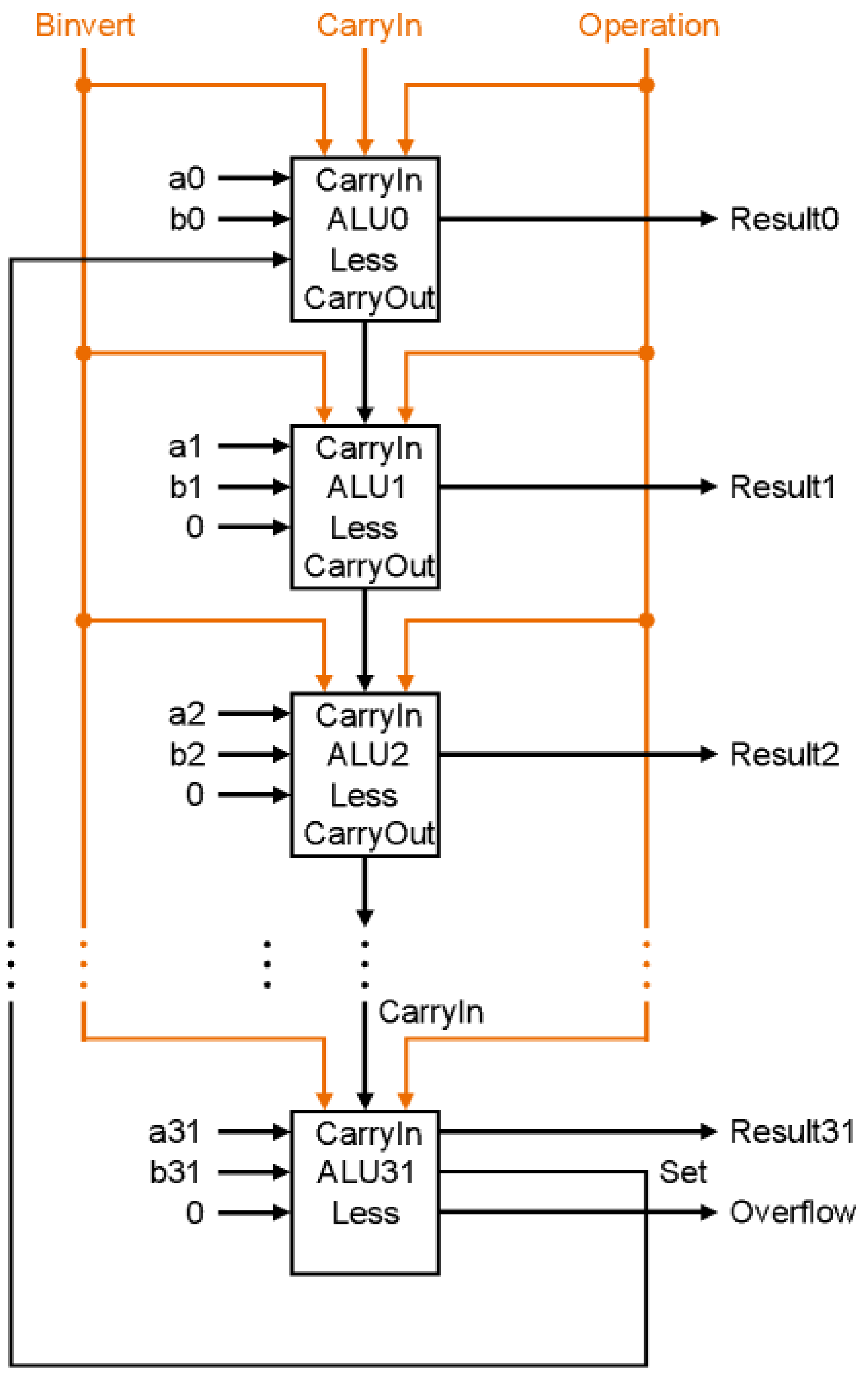
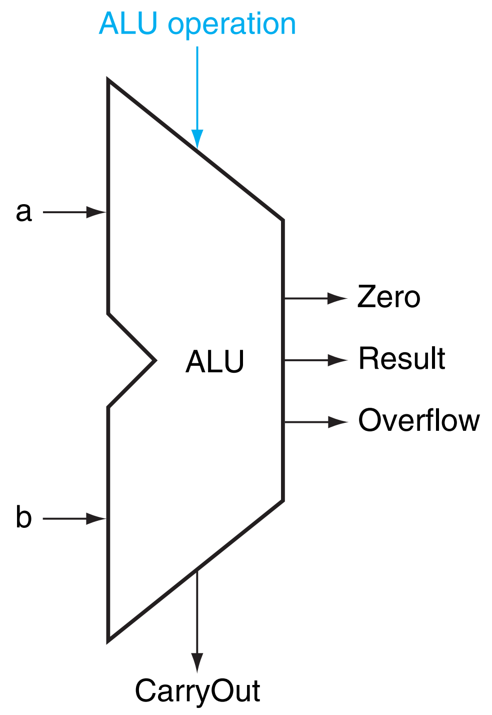
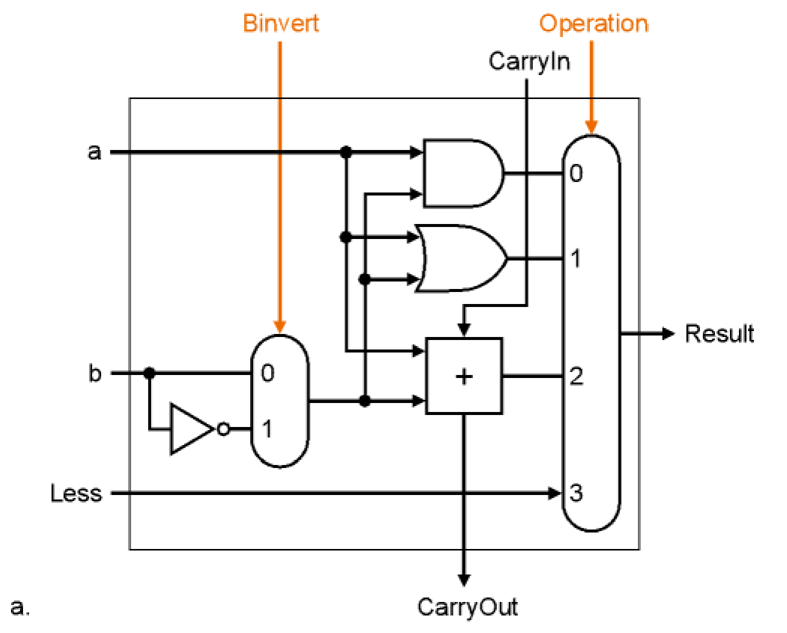


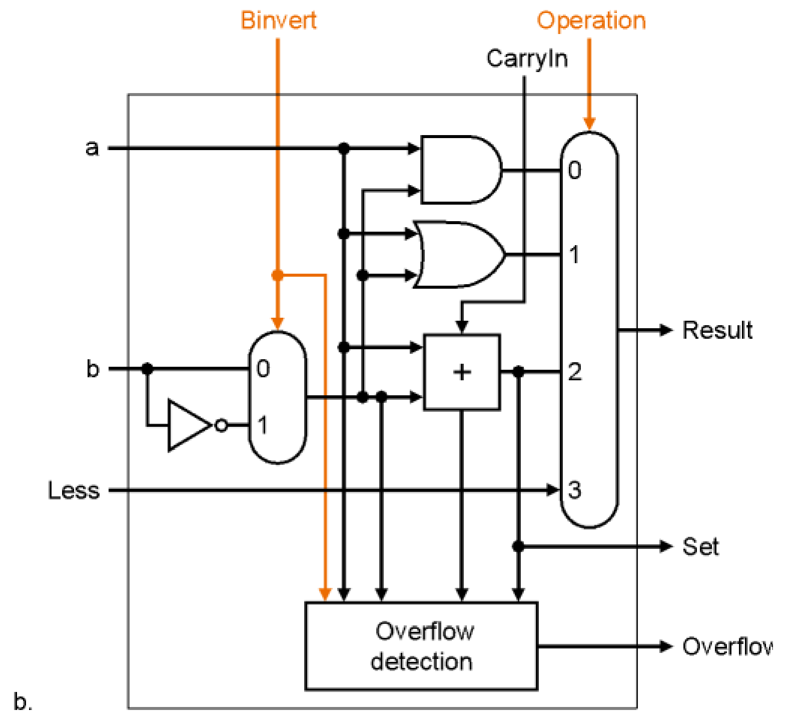
what signals accomplish:

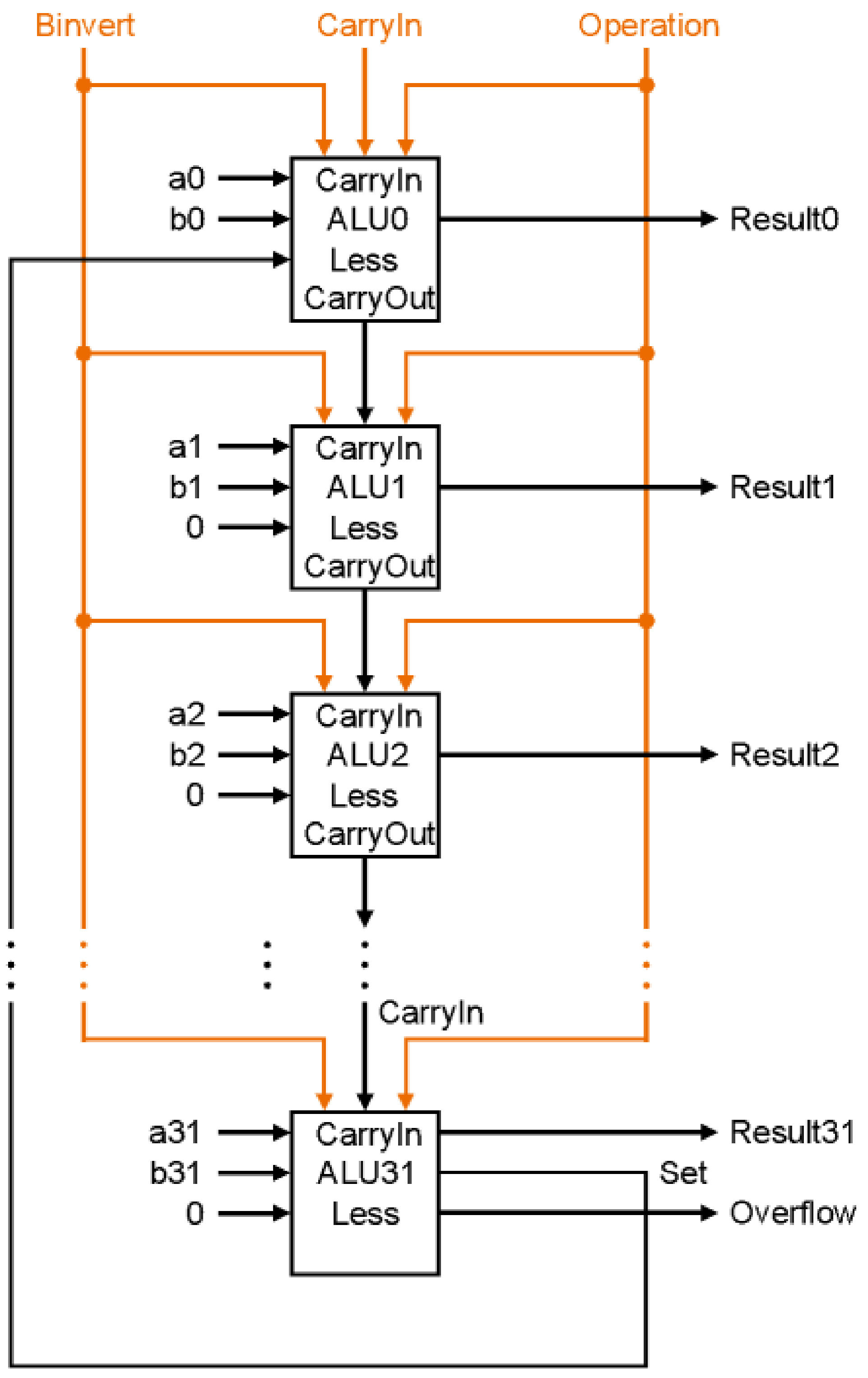
	Binvert	CIn	Oper
add?	0	0	10
sub?			
and?			
or?			
beq?			
slt?			



Full ALU

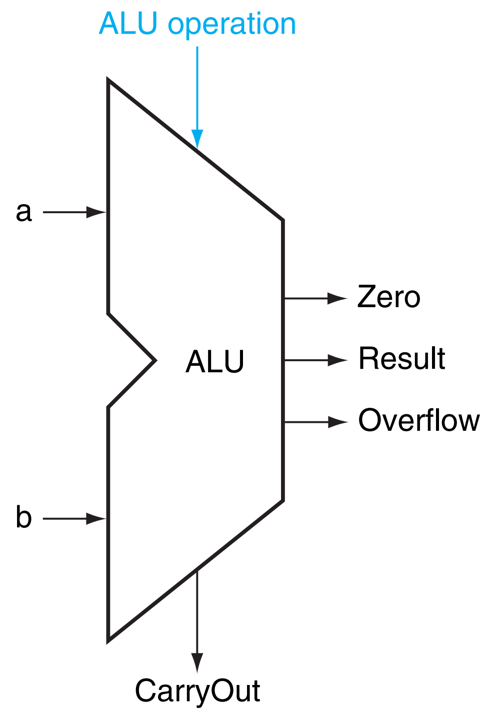




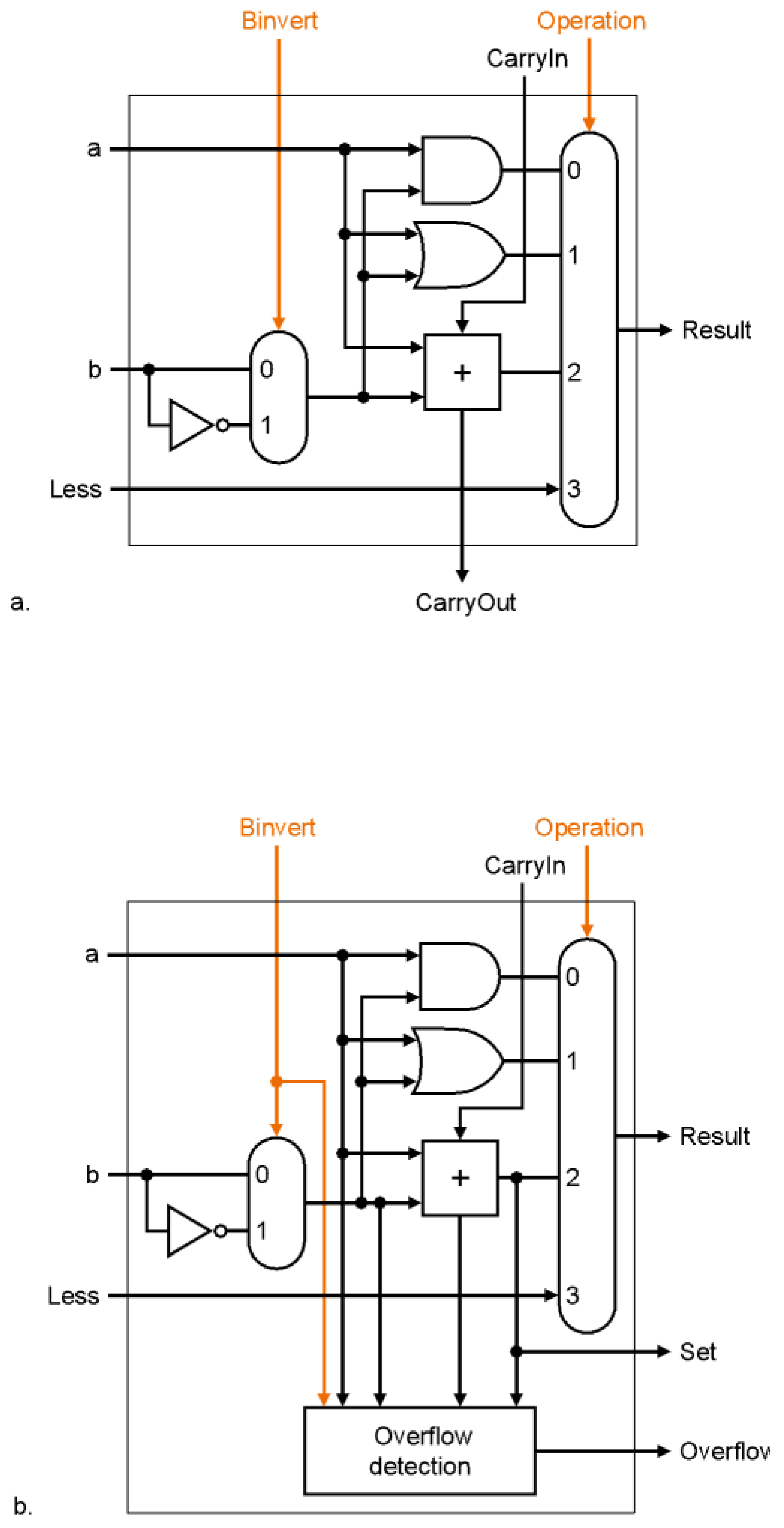


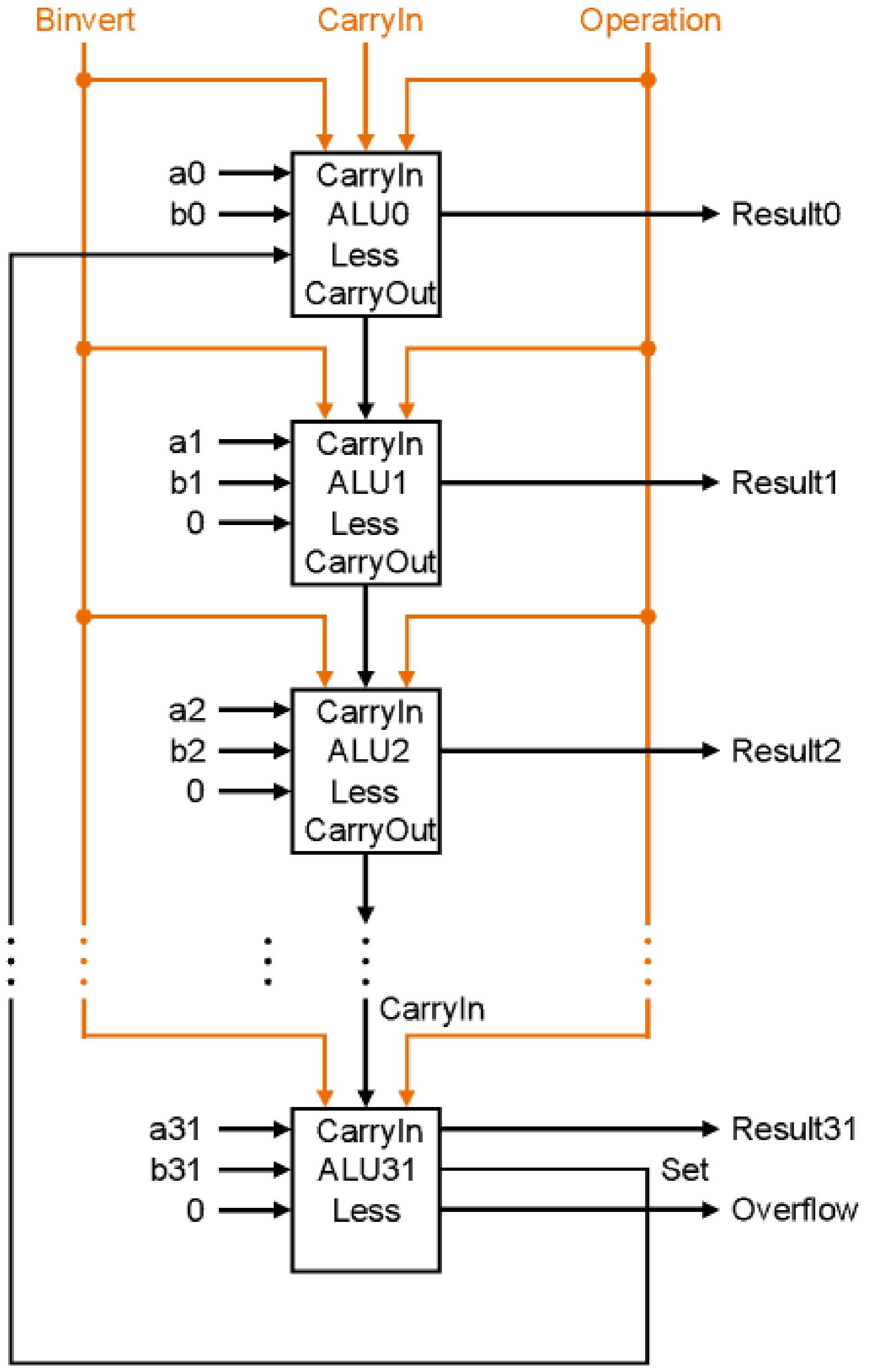
what signals accomplish:

	Binvert	CIn	Oper
add?	0	0	10
sub?	1	1	10
and?			
or?			
beq?			
slt?			



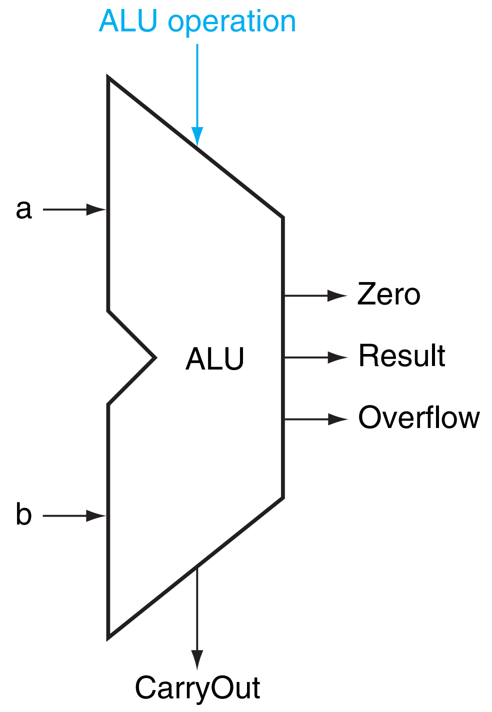
Full ALU



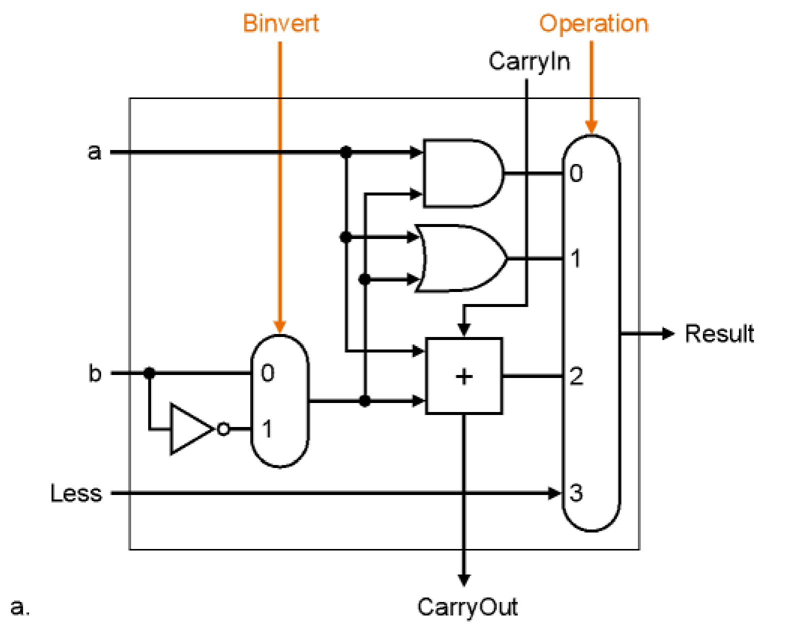


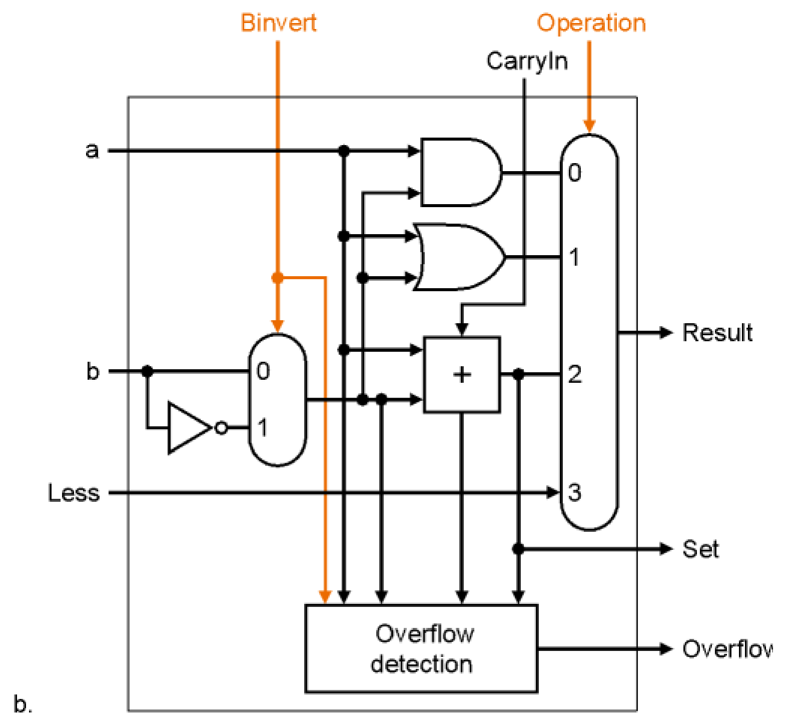
what signals accomplish:

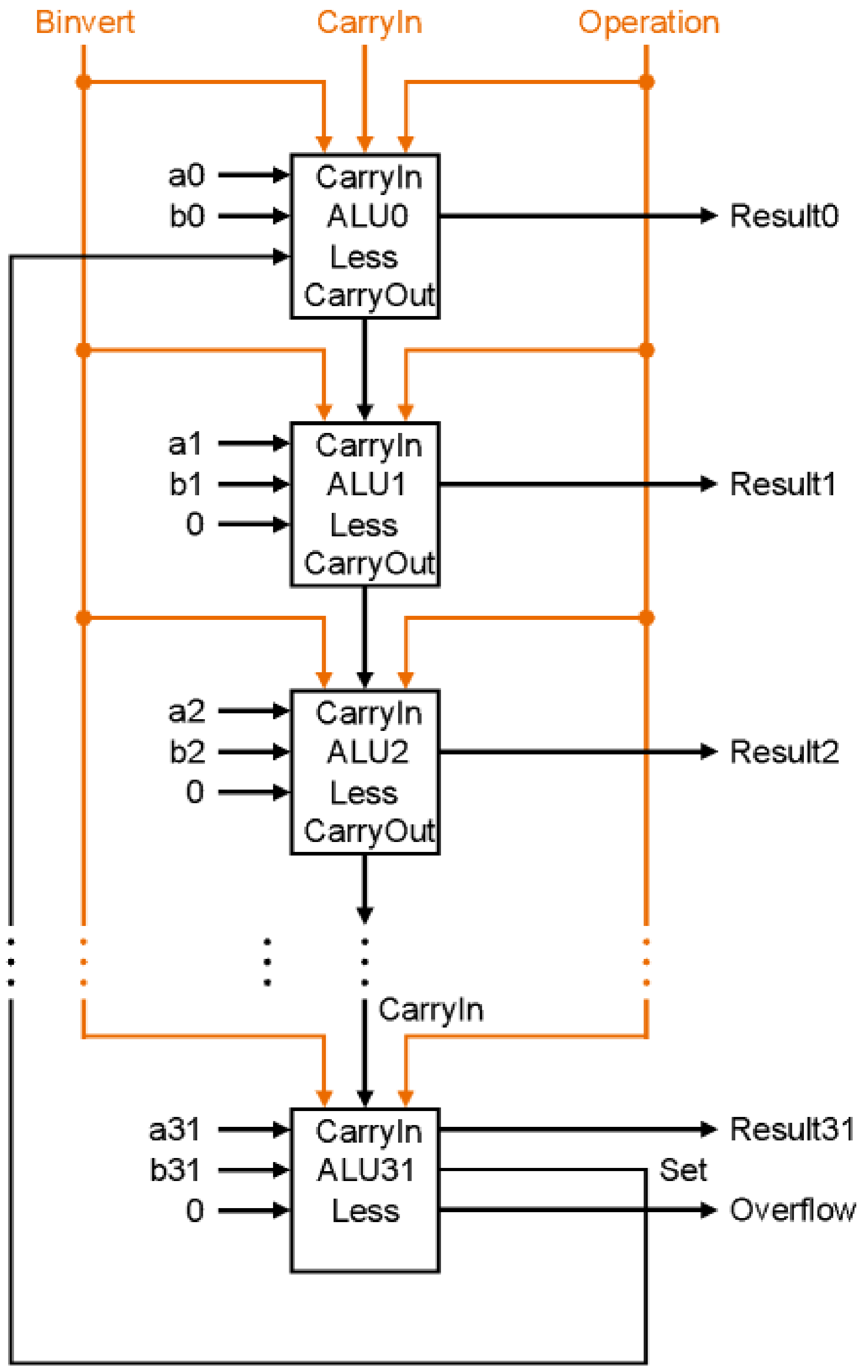
	Binvert	CIn	Oper
add?	0	0	10
sub?	1	1	10
and?	0	0	00
or?			
beq?			
slt?			



Full ALU

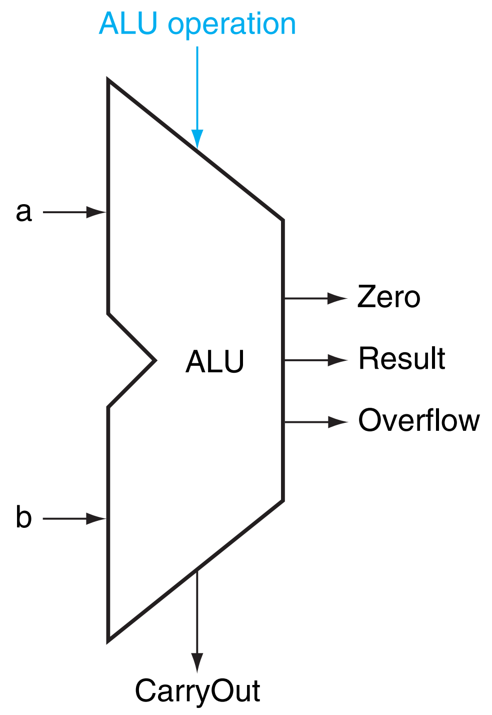




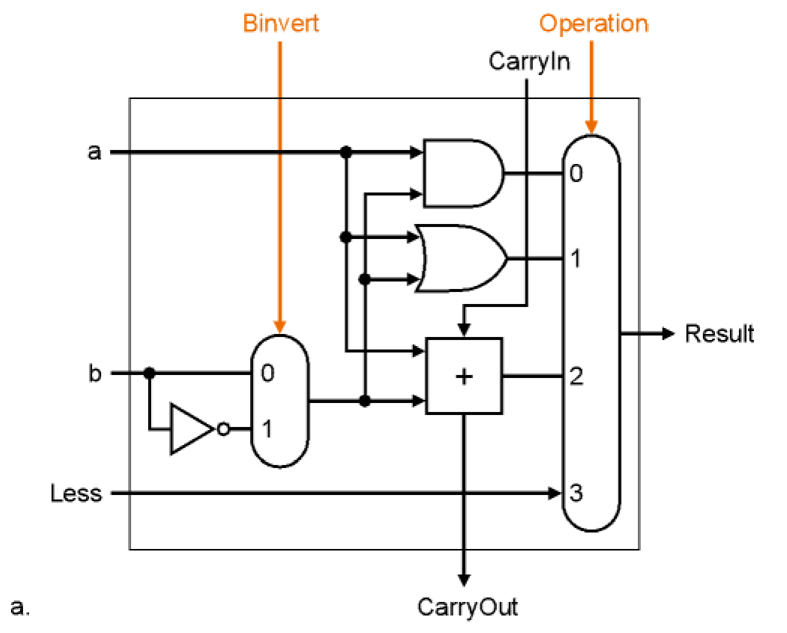


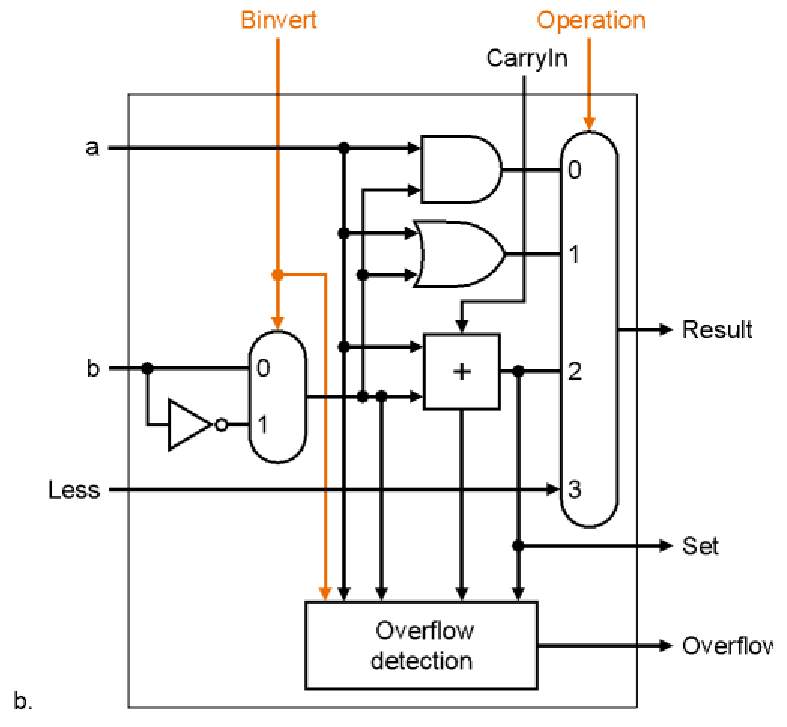
what signals accomplish:

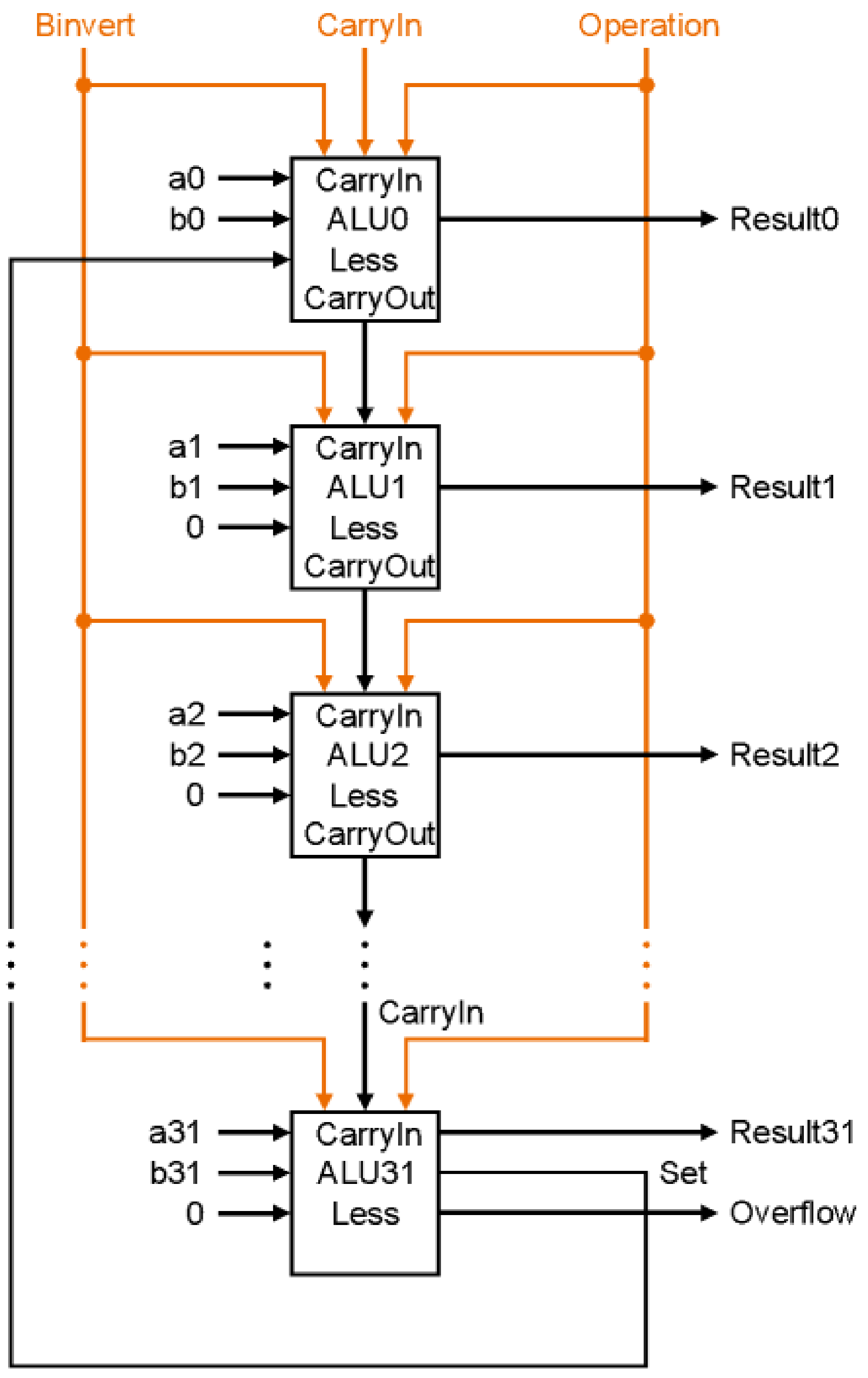
	Binvert	CIn	Oper
add?	0	0	10
sub?	1	1	10
and?	0	0	00
or?	0	0	01
beq?			
slt?			



Full ALU

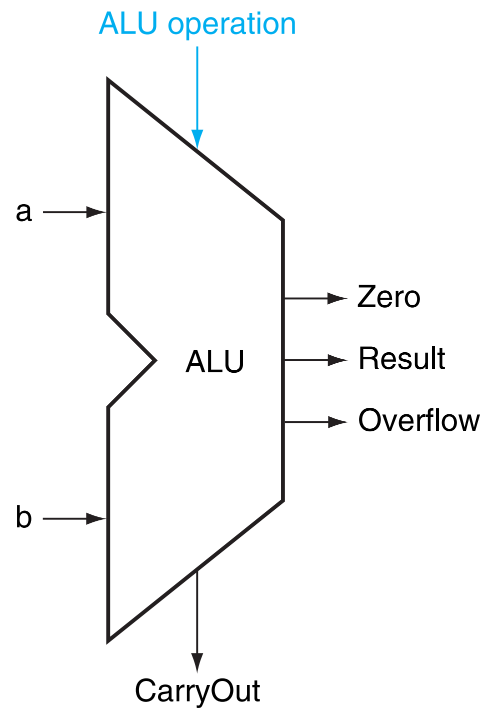




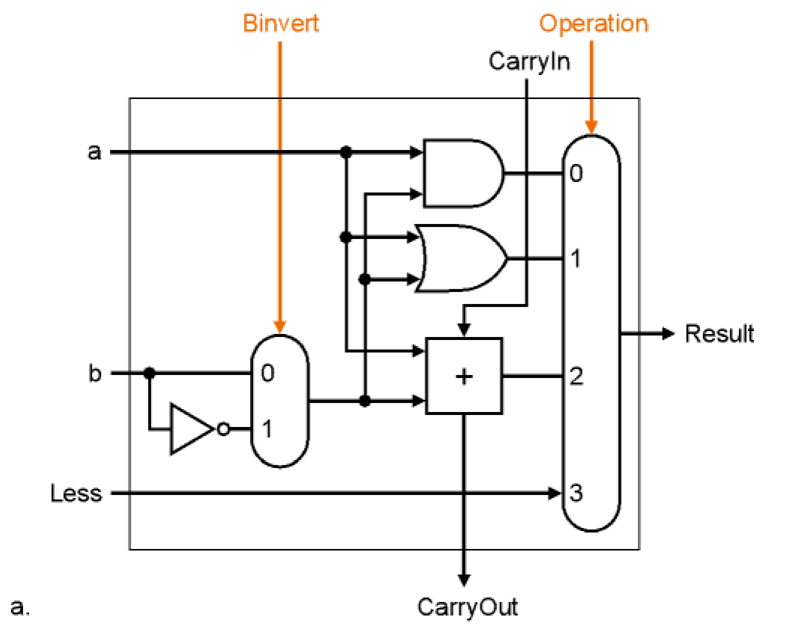


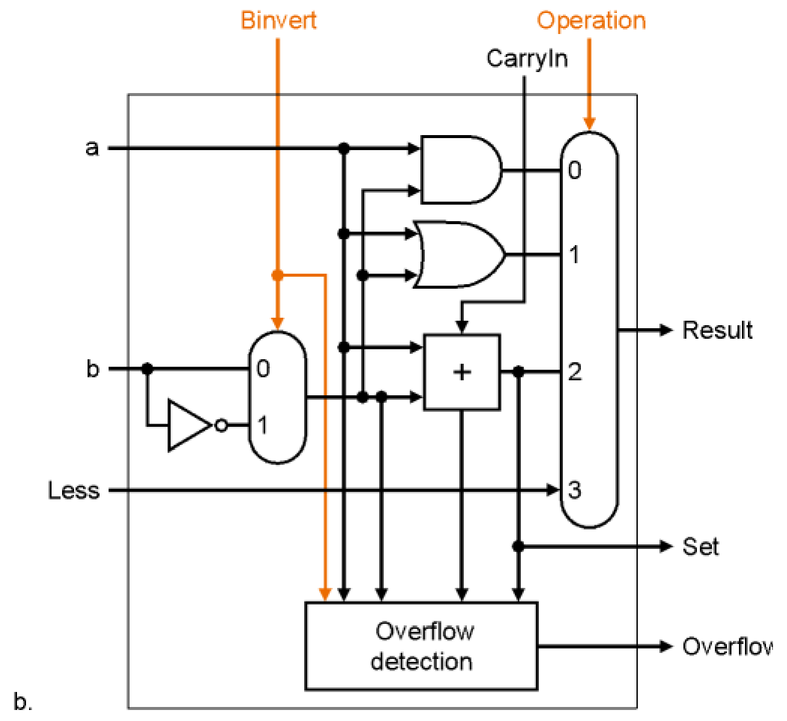
what signals accomplish:

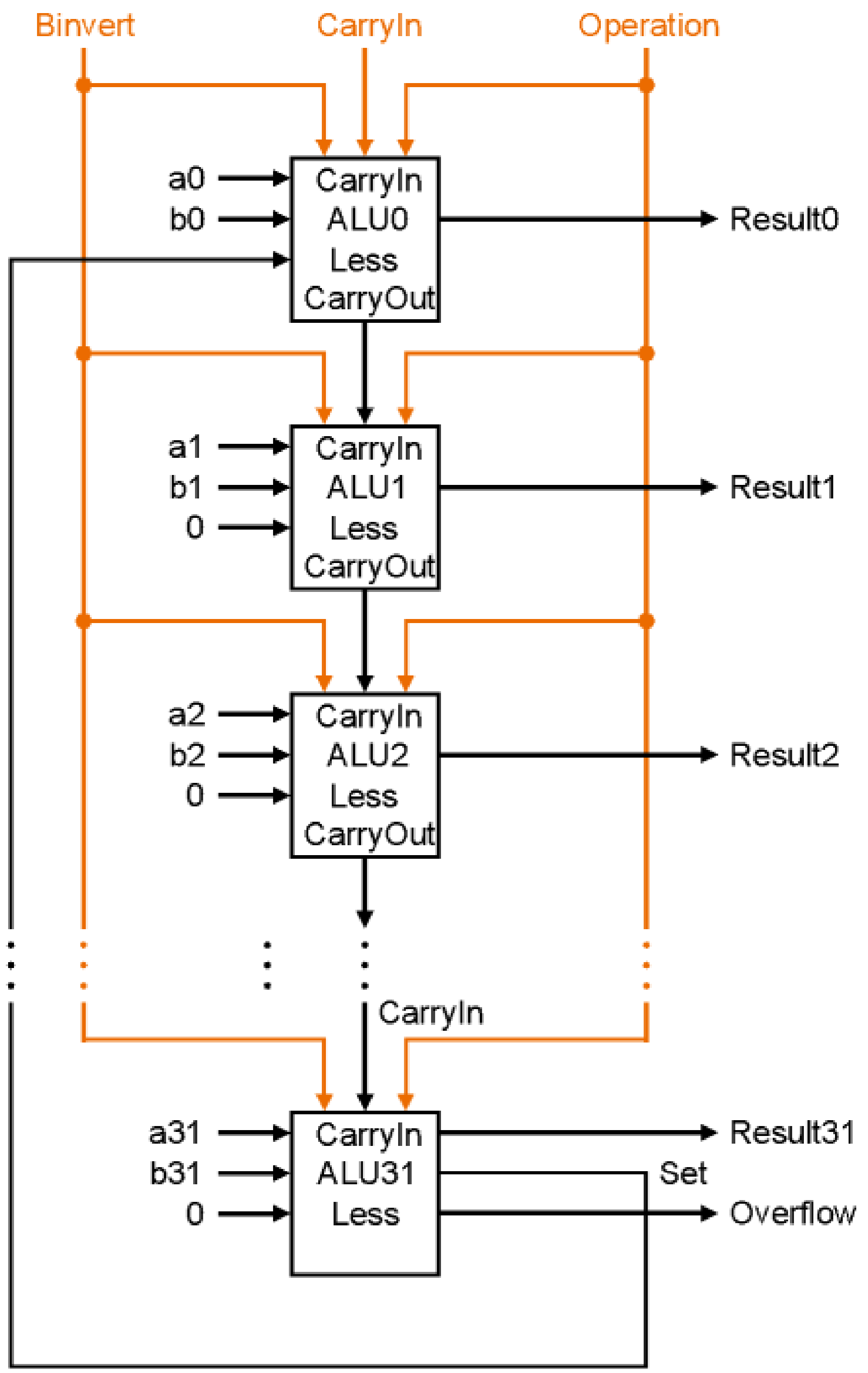
	Binvert	CIn	Oper
add?	0	0	10
sub?	1	1	10
and?	0	0	00
or?	0	0	01
beq?	1	1	10
slt?			



Full ALU

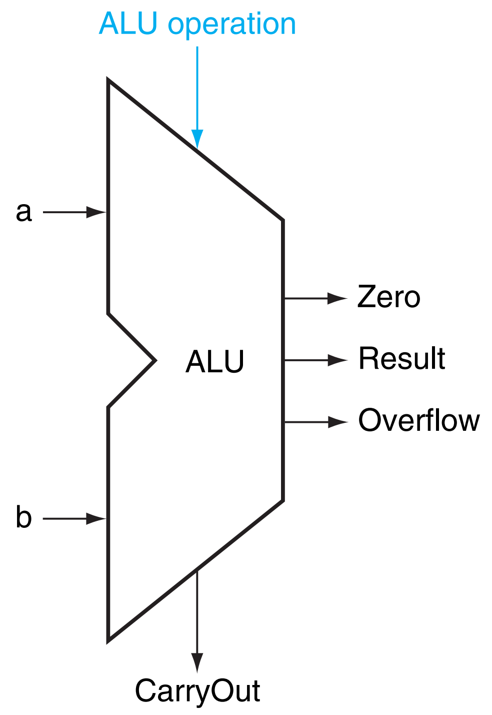






what signals accomplish:

	Binvert	CIn	Oper
add?	0	0	10
sub?	1	1	10
and?	0	0	00
or?	0	0	01
beq?	1	1	10
slt?	1	1	11



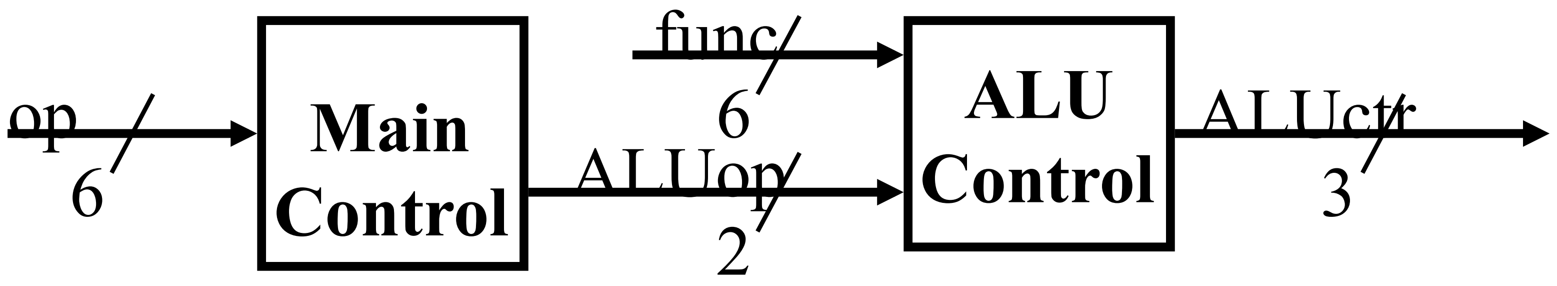
ALU Control Bits

- 5-Function ALU

ALU control input	Function	Operations
000	And	and
001	Or	or
010	Add	add, lw, sw
110	Subtract	sub, beq
111	Slt	slt

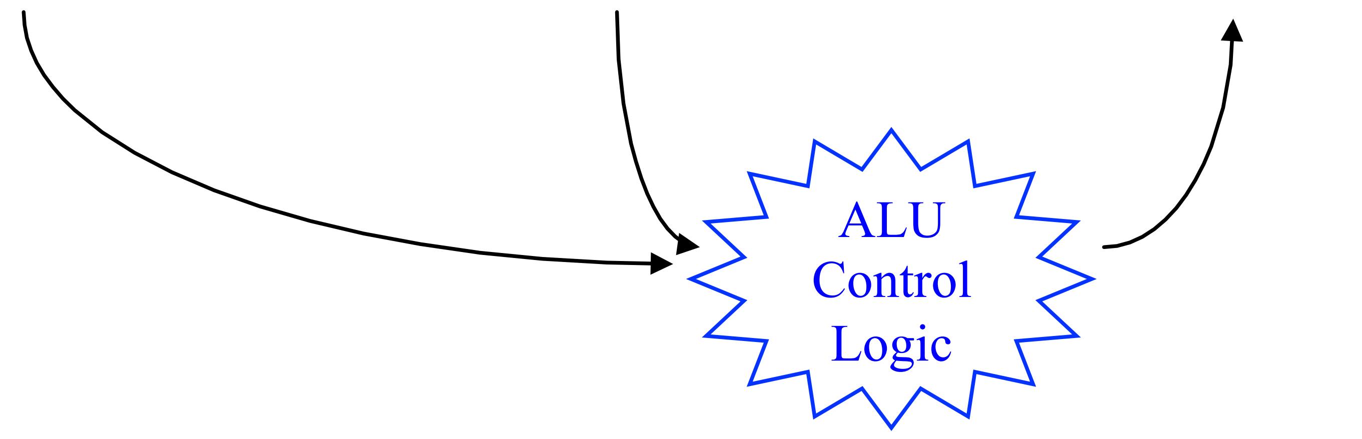
- Based on opcode (bits 31-26) and function code (bits 5-0) from instruction
- ALU doesn't need to know all opcodes--we will summarize opcode with ALUOp (2 bits):

00 - lw,sw   01 - beq   10 - R-format

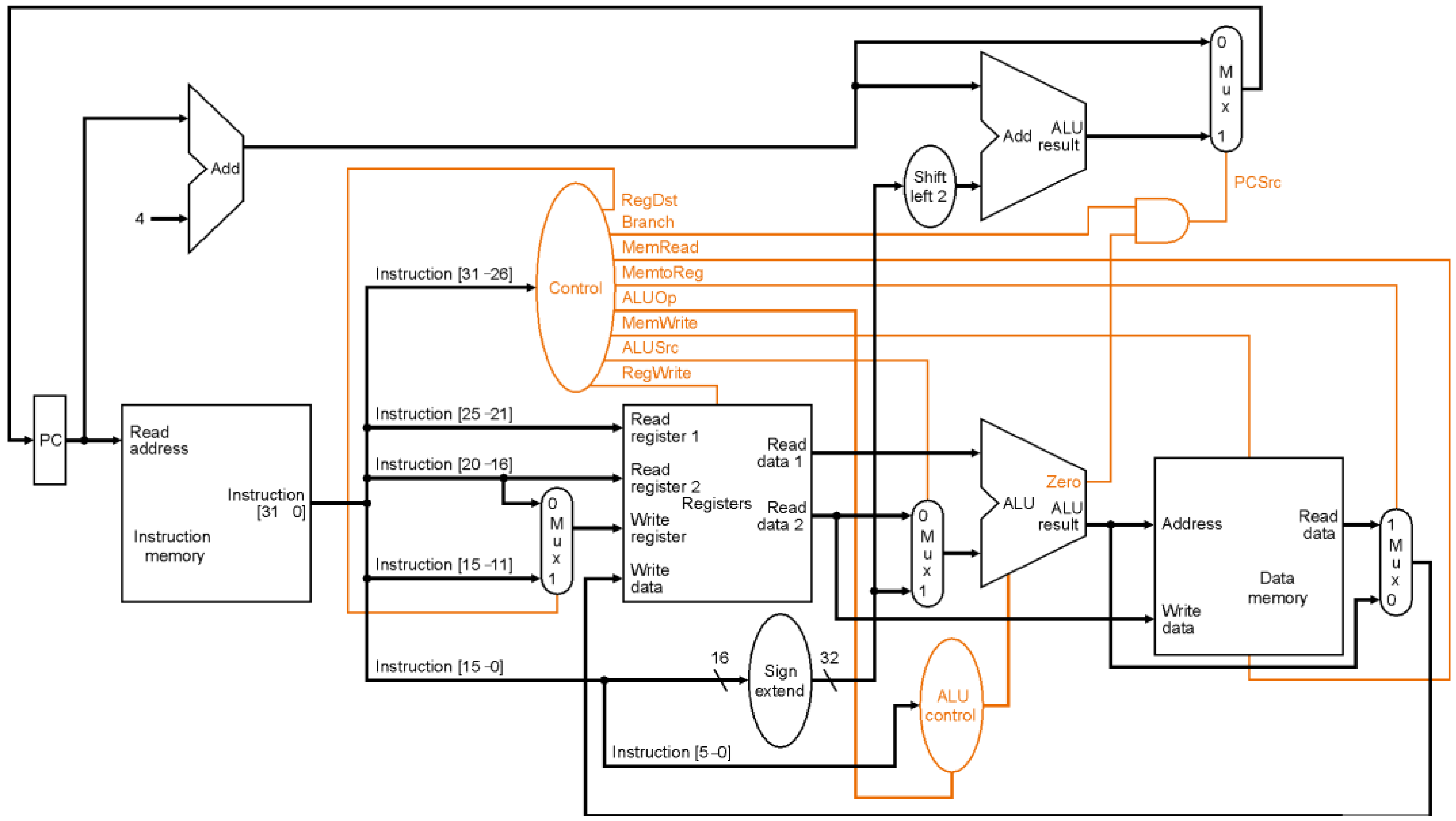


Generating ALU Control

Instruction opcode	ALUOp	Instruction operation	Function code	Desired ALU action	ALU control input
lw	00	load word	xxxxxx	add	010
sw	00	store word	xxxxxx	add	010
beq	01	branch eq	xxxxxx	subtract	110
R-type	10	add	100000	add	010
R-type	10	subtract	100010	subtract	110
R-type	10	AND	100100	and	000
R-type	10	OR	100101	or	001
R-type	10	slt	101010	slt	111

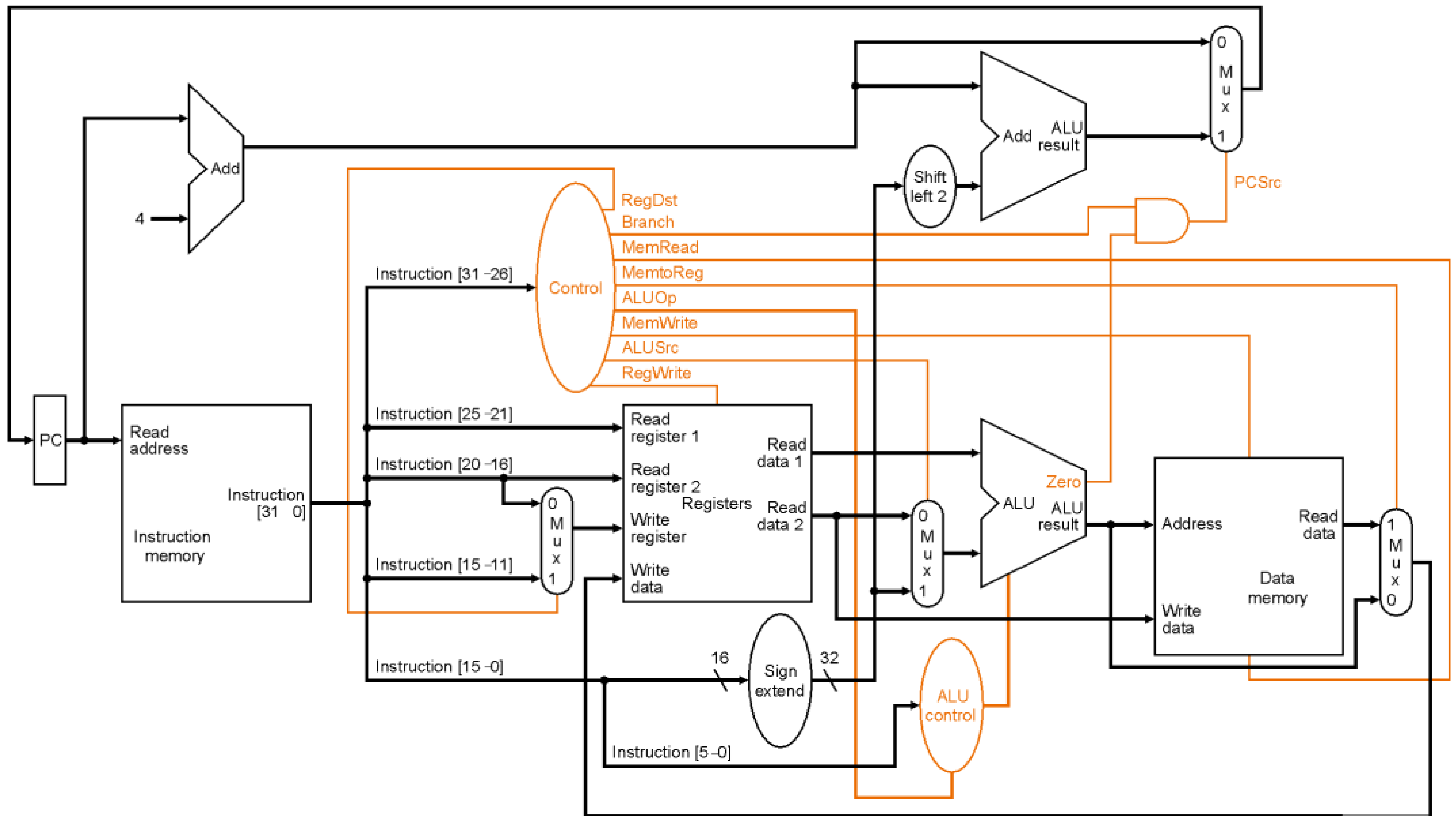


Controlling the CPU



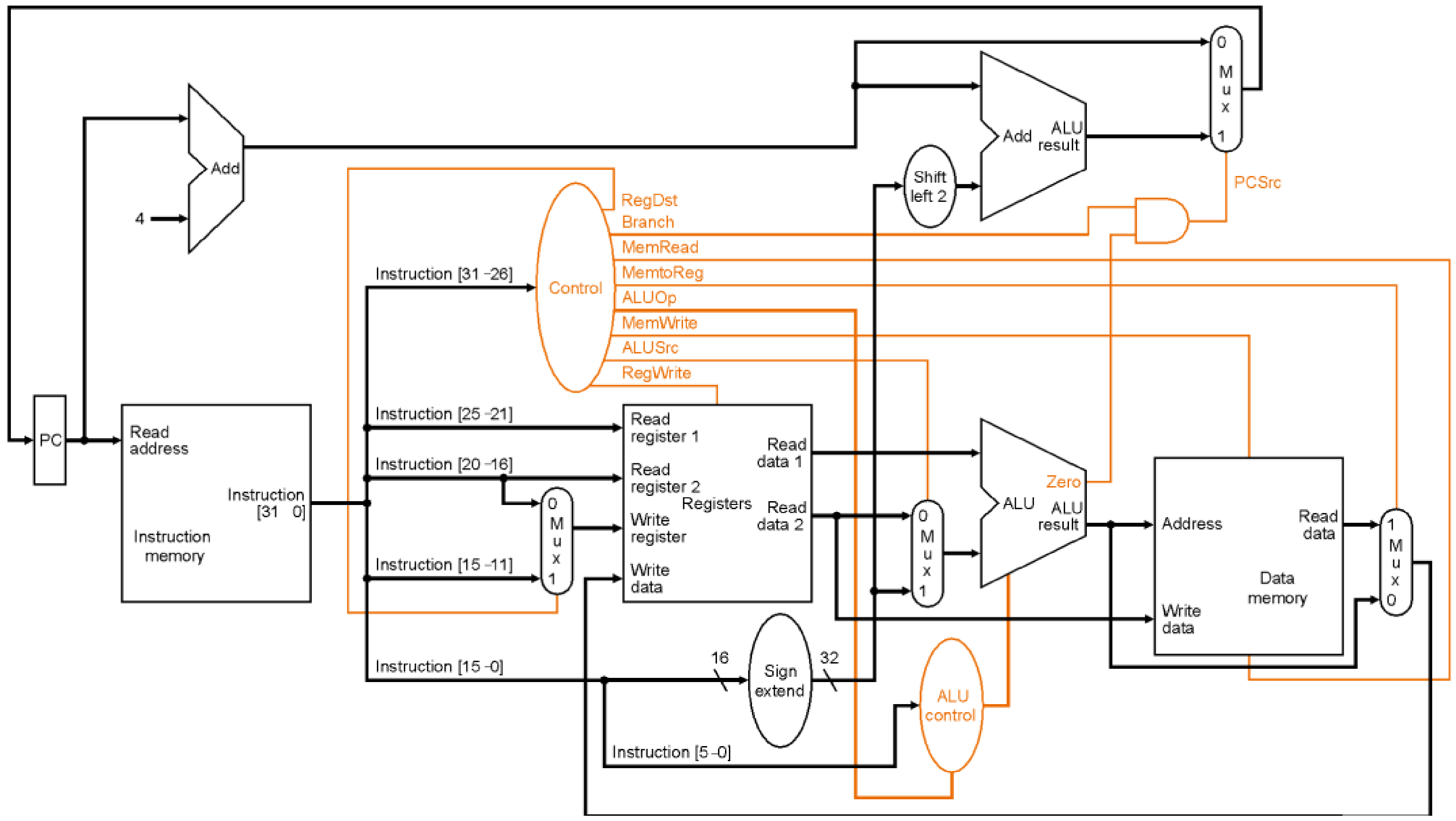
Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format								1	0
`lw`								0	0
`sw`								0	0
`beq`								0	1

Controlling the CPU



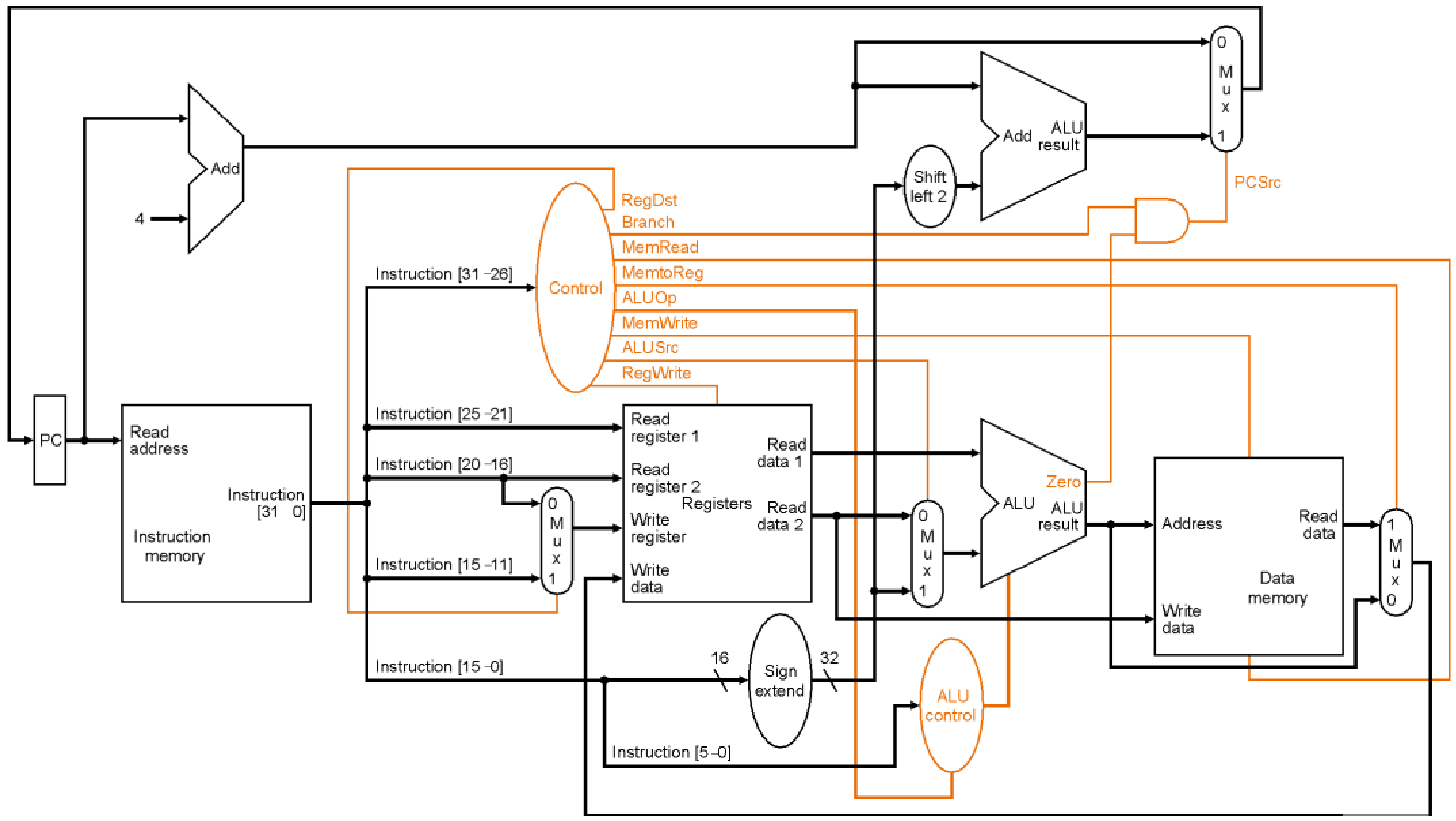
Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1							1	0
lw								0	0
sw								0	0
beq								0	1

Controlling the CPU



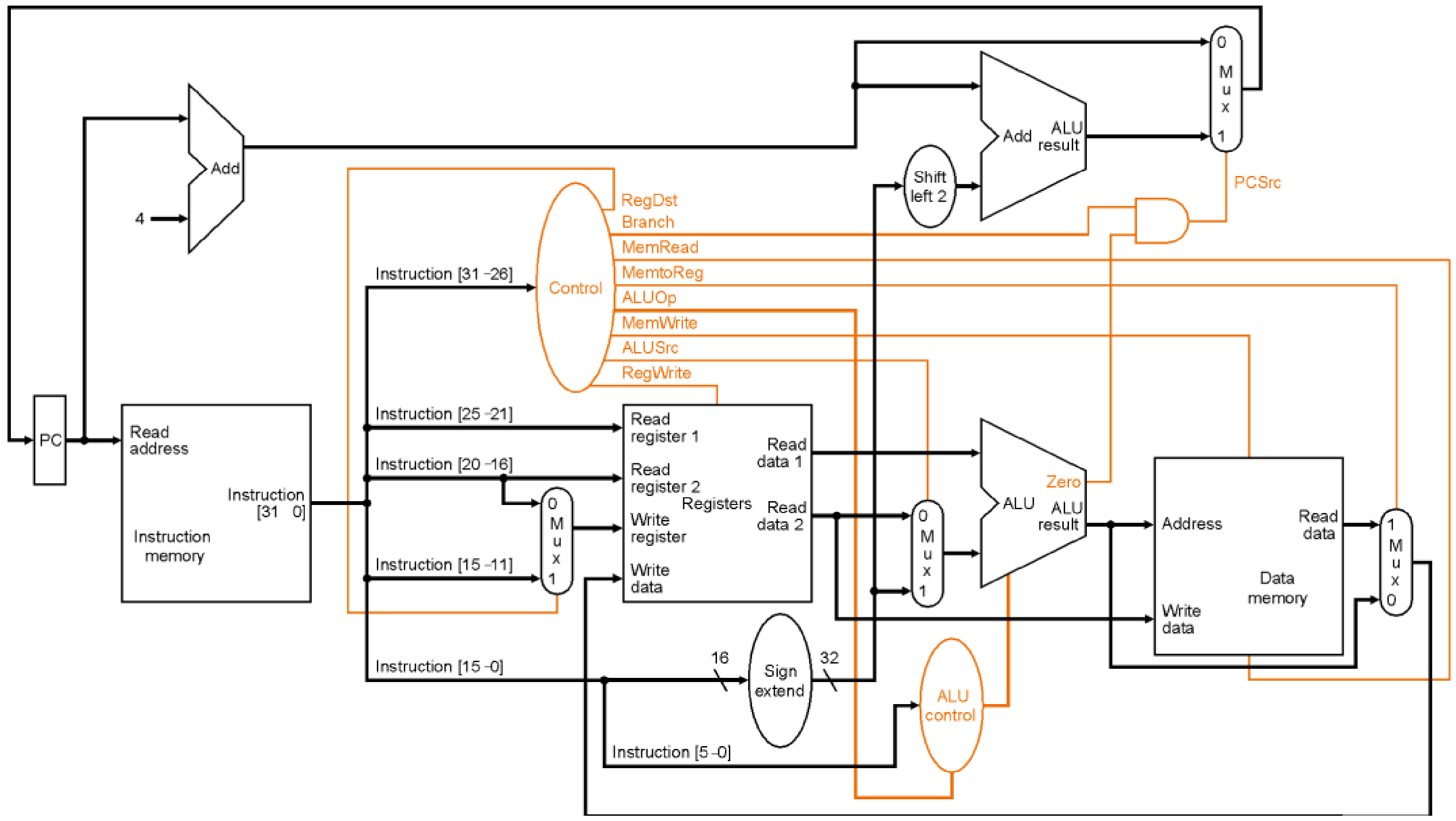
Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0						1	0
`lw`								0	0
`sw`								0	0
`beq`								0	1

Controlling the CPU



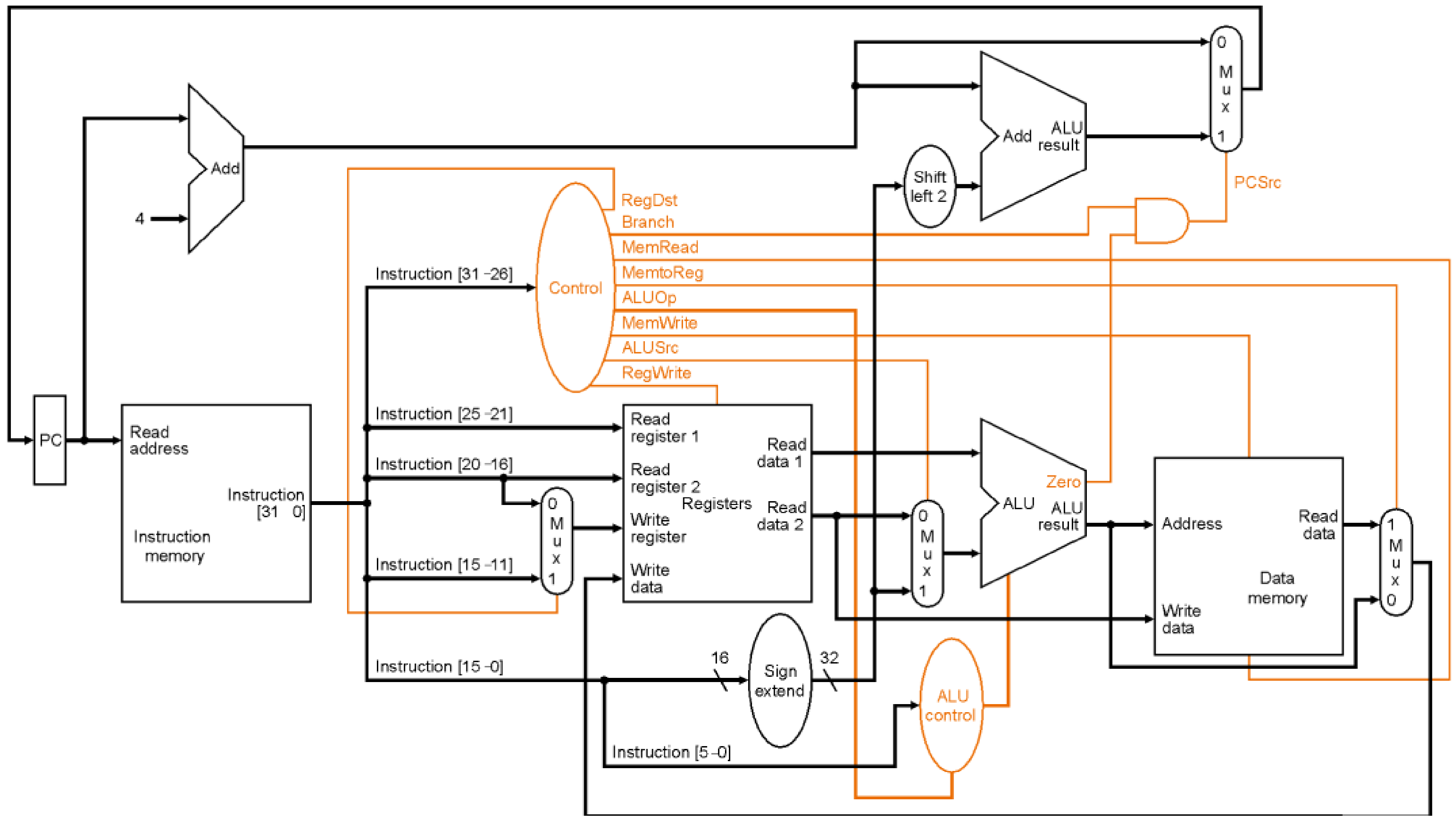
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0					1	0
lw								0	0
sw								0	0
beq								0	1

Controlling the CPU



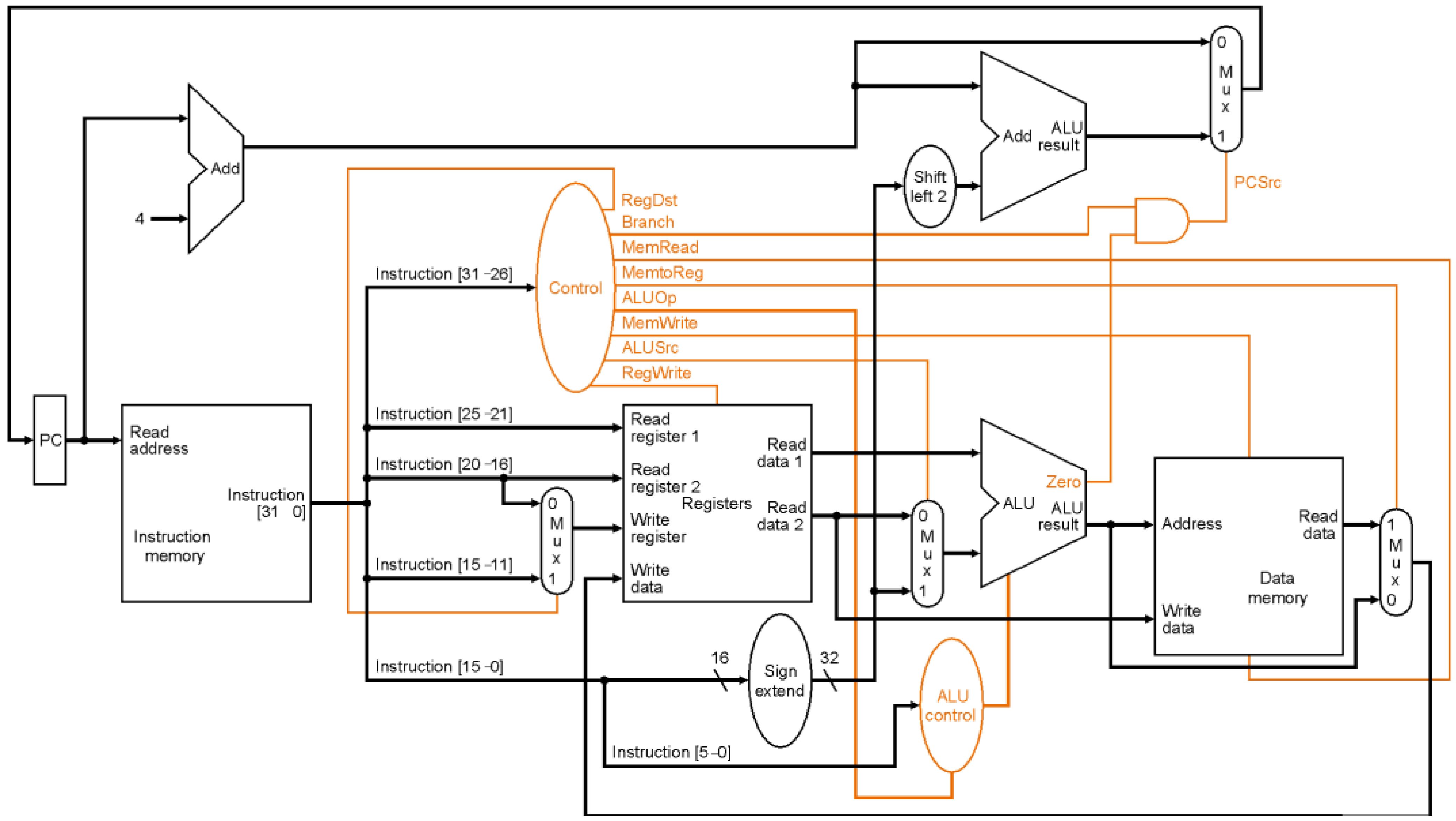
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1				1	0
lw								0	0
sw								0	0
beq								0	1

Controlling the CPU



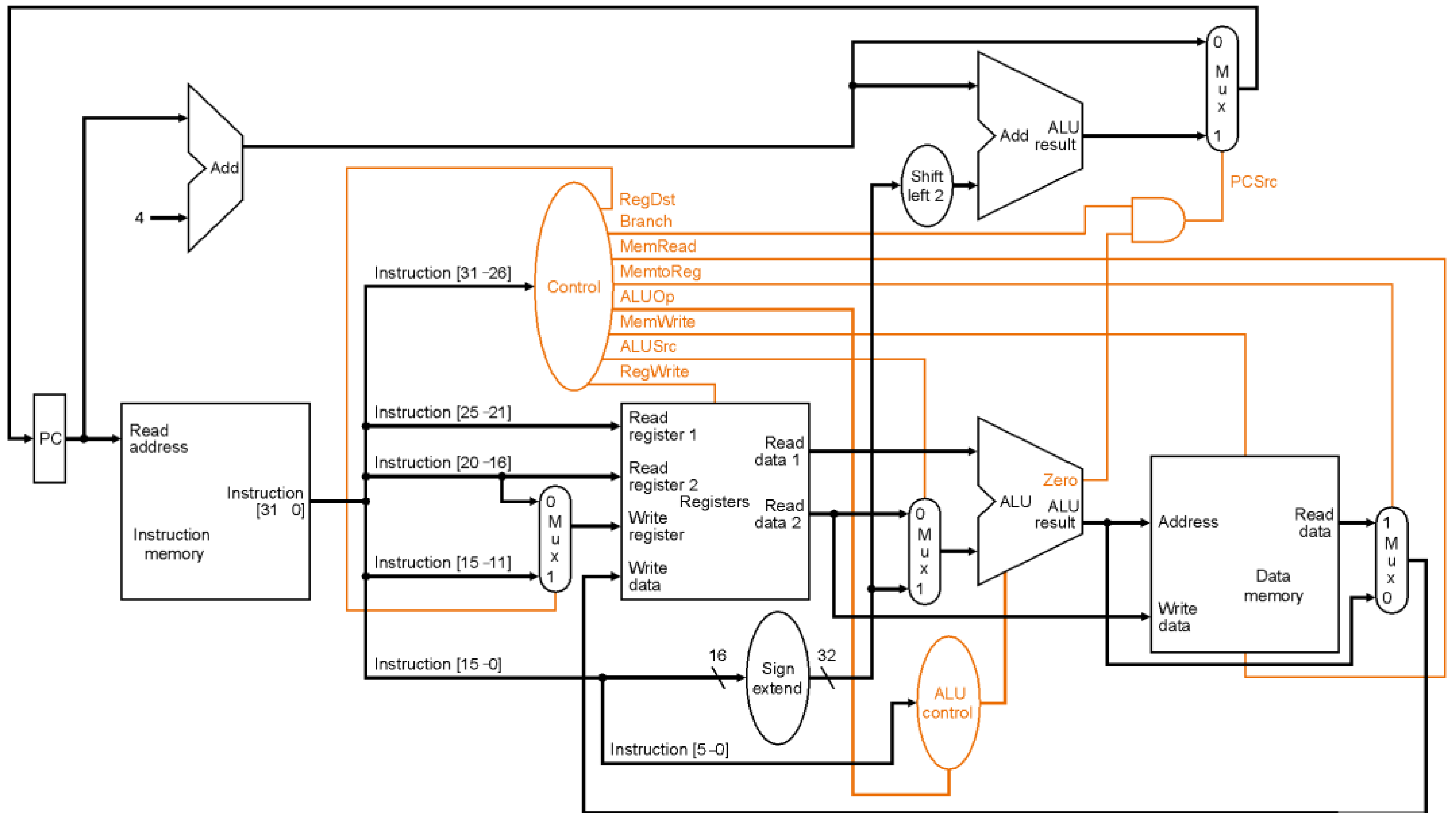
Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0			1	0
lw								0	0
sw								0	0
beq								0	1

Controlling the CPU



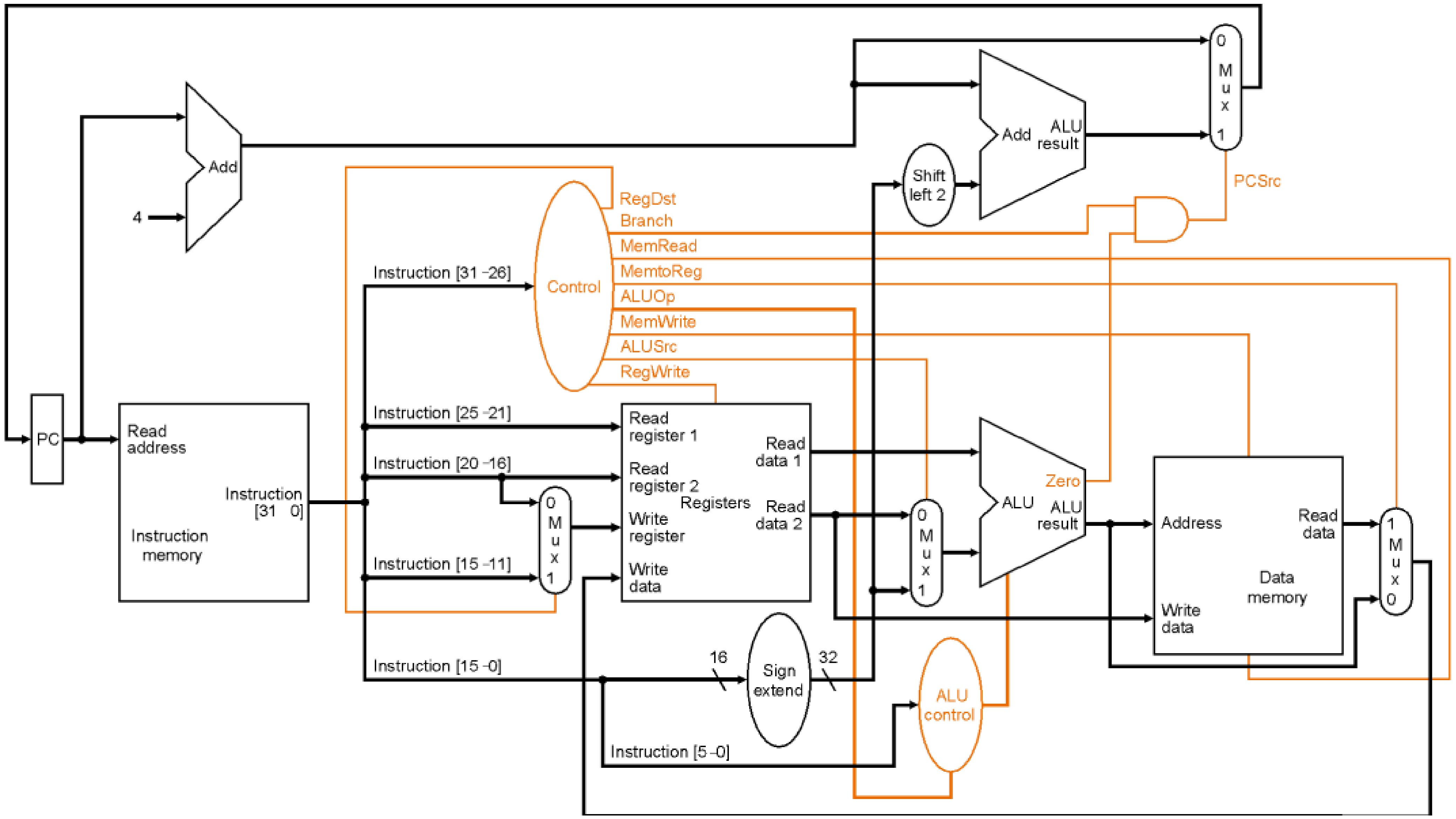
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0		1	0
lw								0	0
sw								0	0
beq								0	1

Controlling the CPU



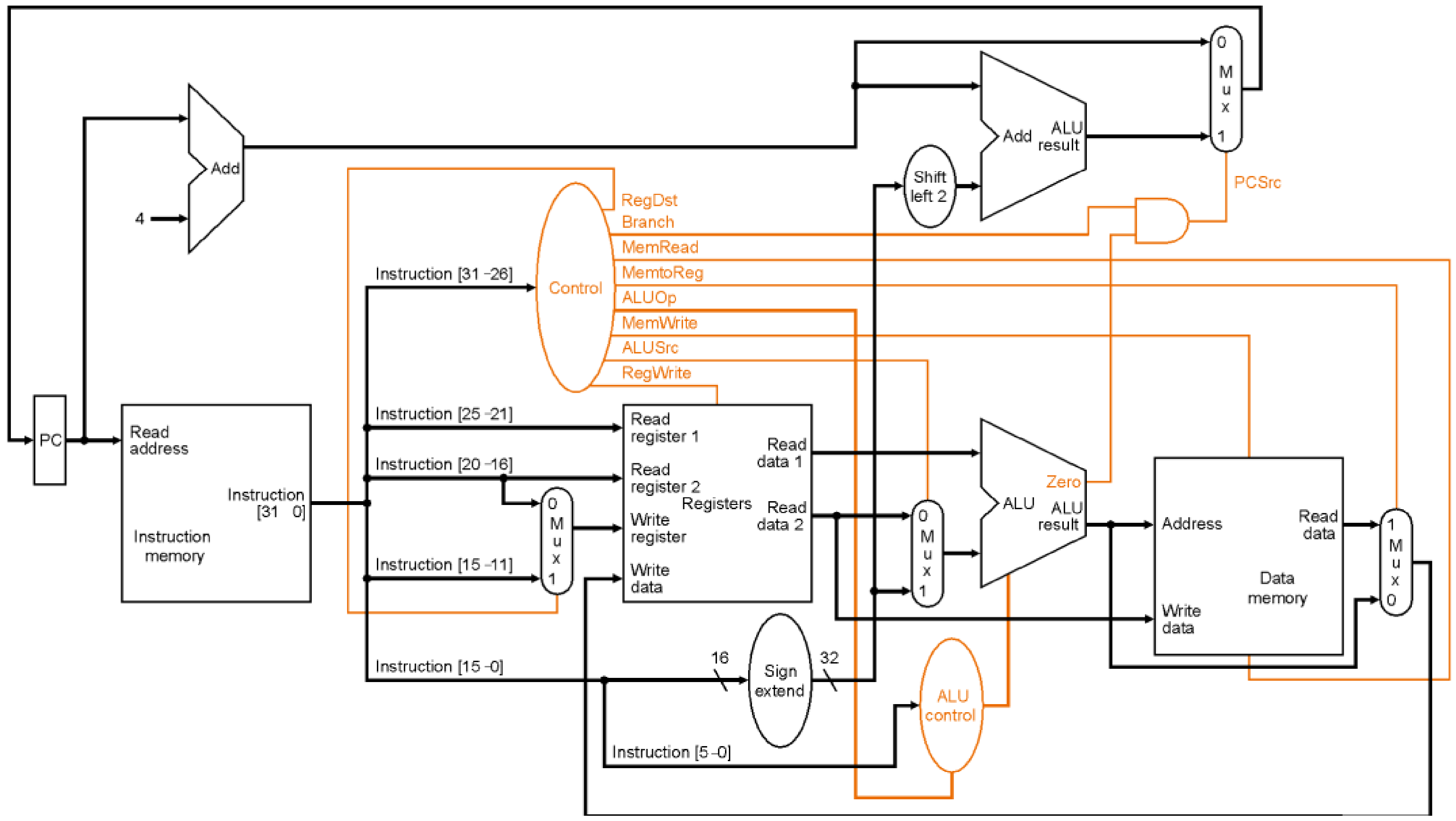
Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`								0	0
`sw`								0	0
`beq`								0	1

Controlling the CPU



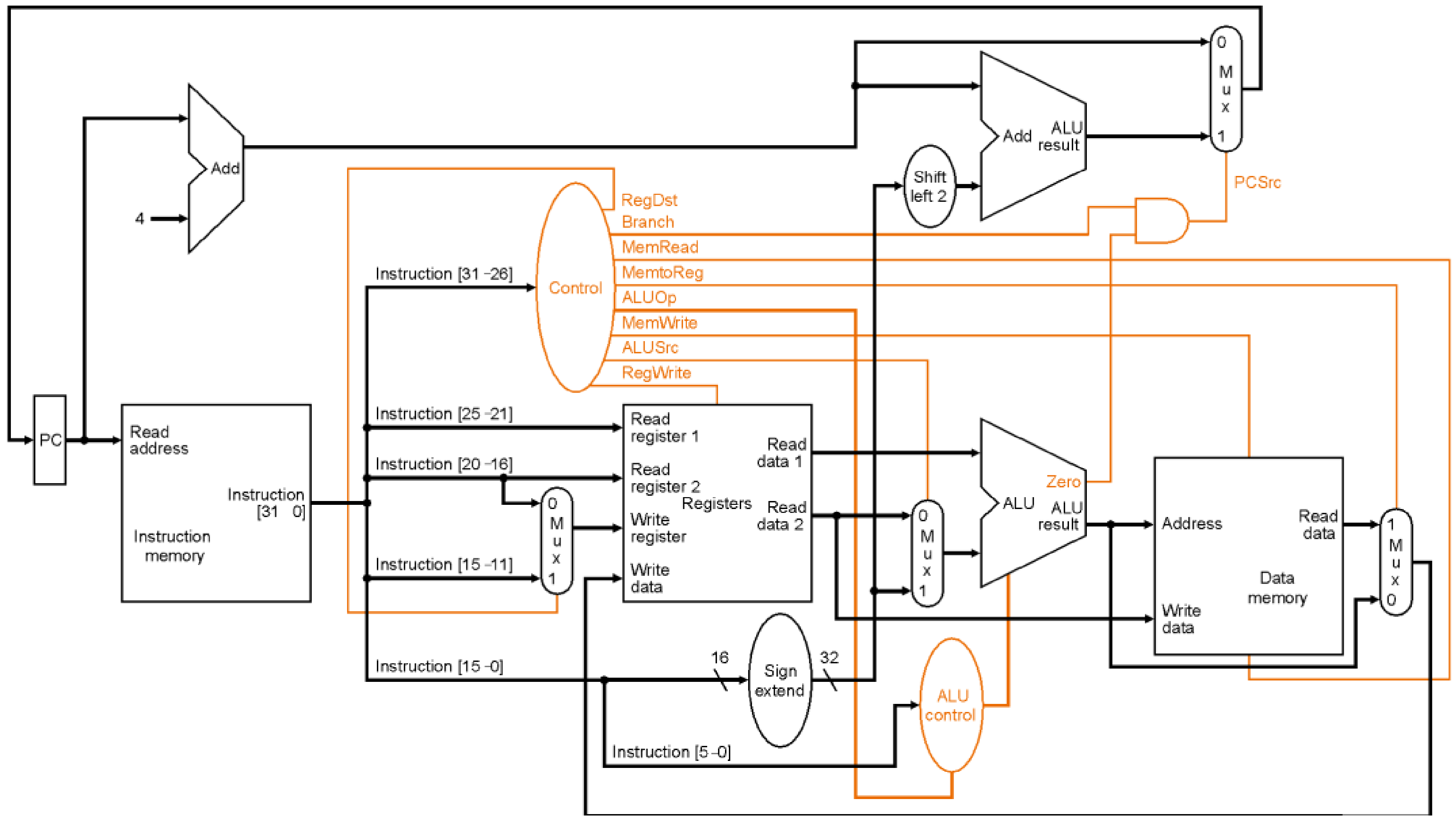
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0							0	0
sw								0	0
beq								0	1

Controlling the CPU



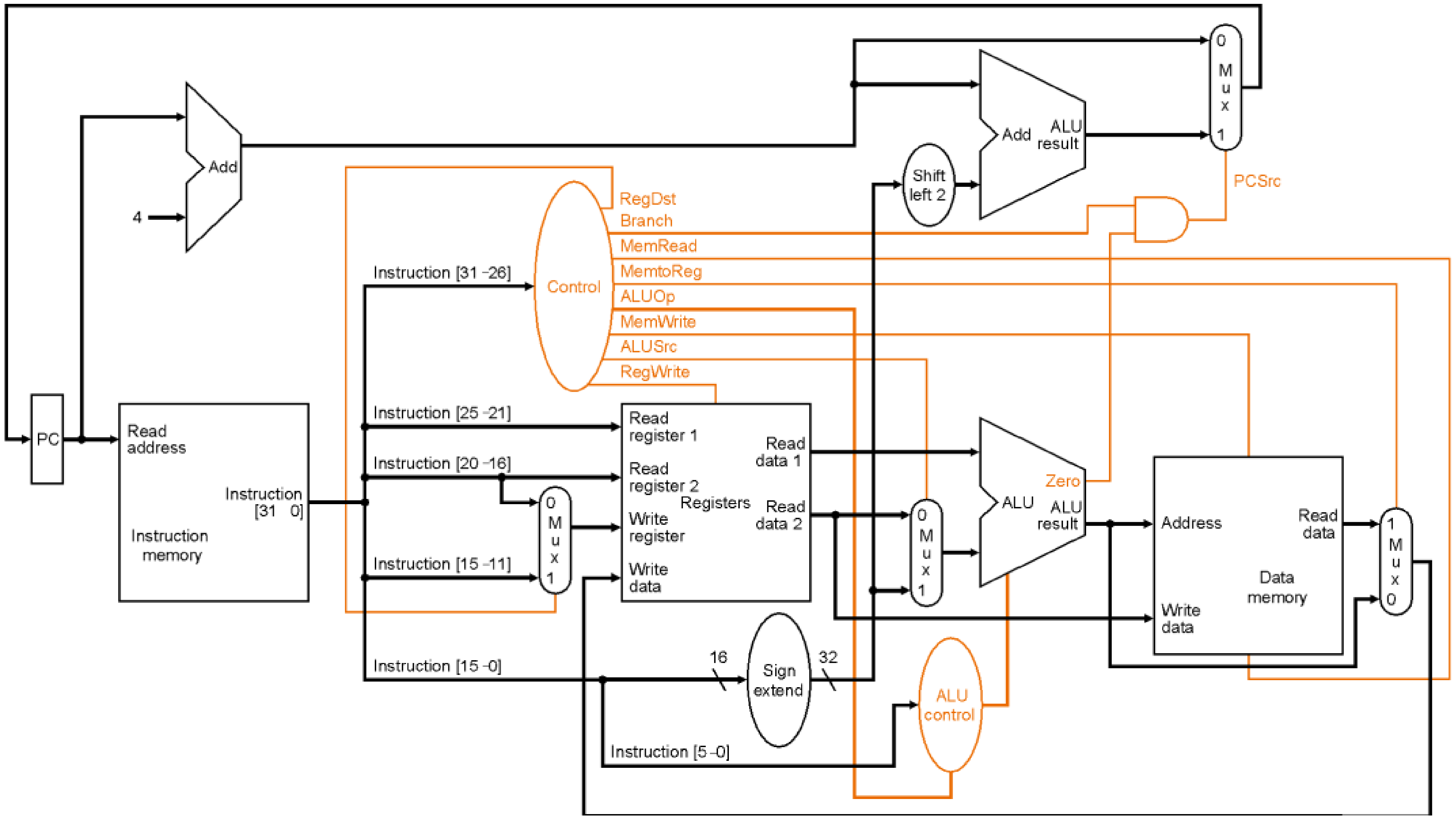
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1						0	0
sw								0	0
beq								0	1

Controlling the CPU



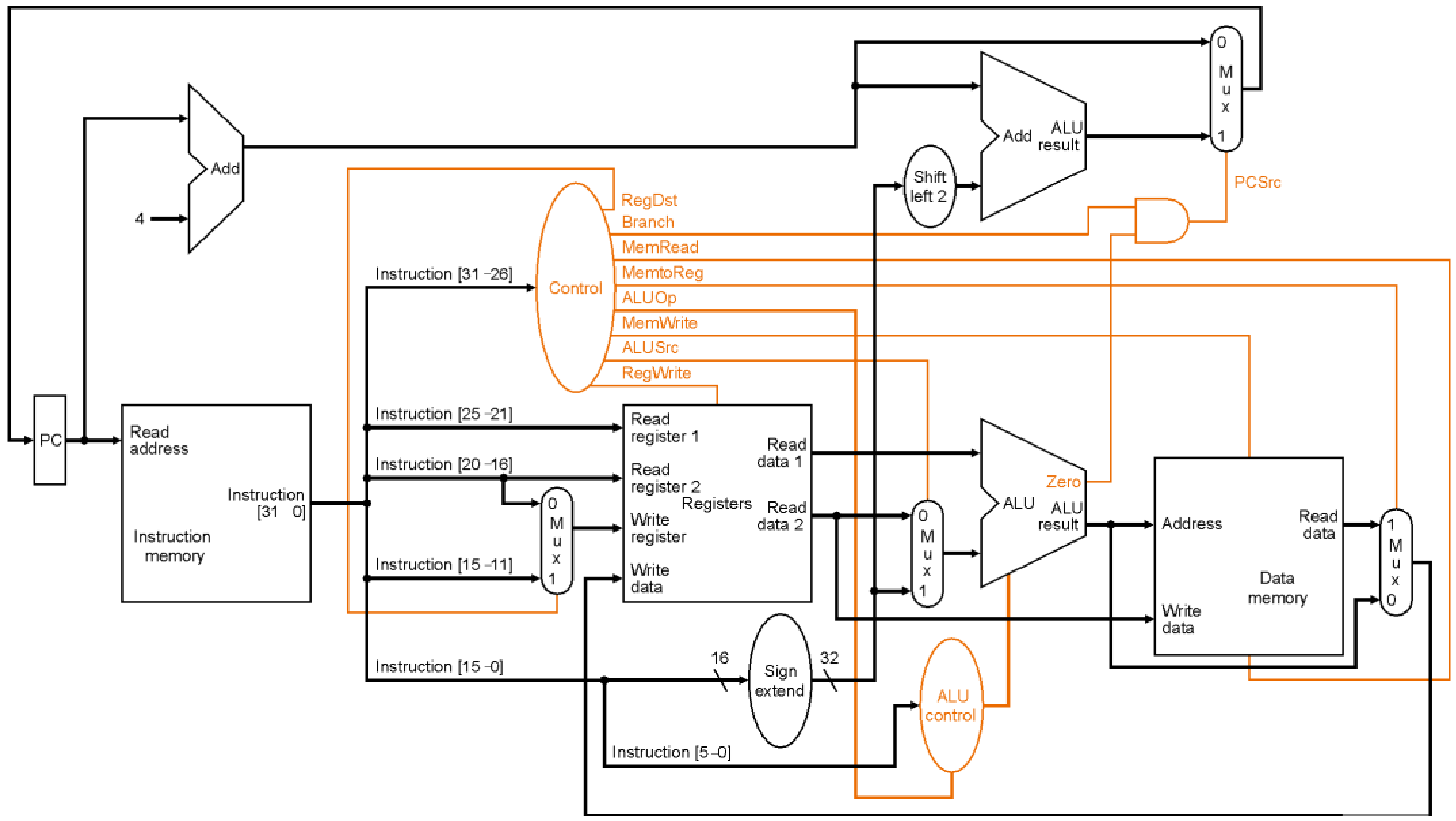
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1					0	0
`sw`								0	0
`beq`								0	1

Controlling the CPU



Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1				0	0
`sw`								0	0
`beq`								0	1

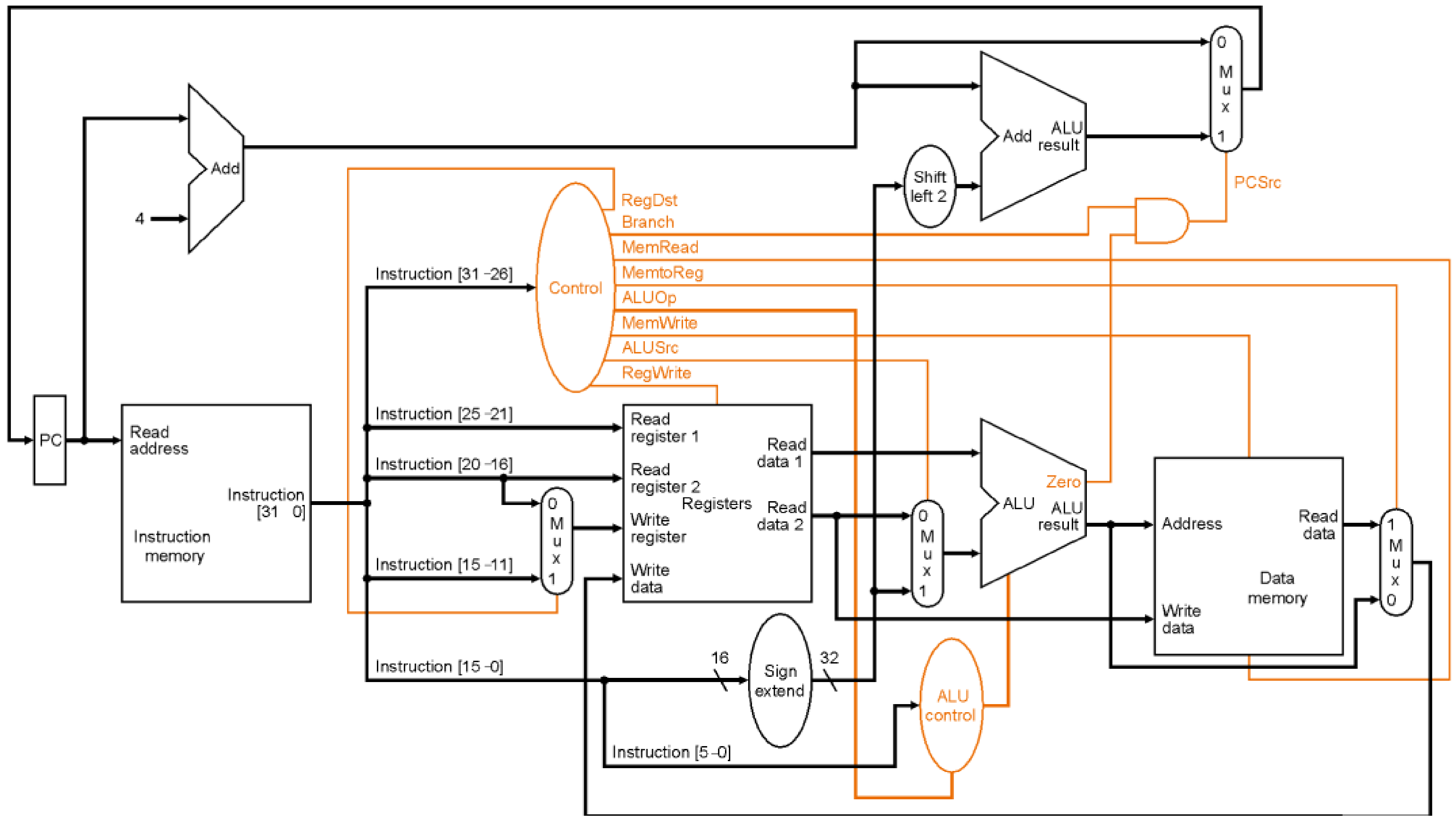
Controlling the CPU



Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1	1			0	0
`sw`								0	0
`beq`								0	1

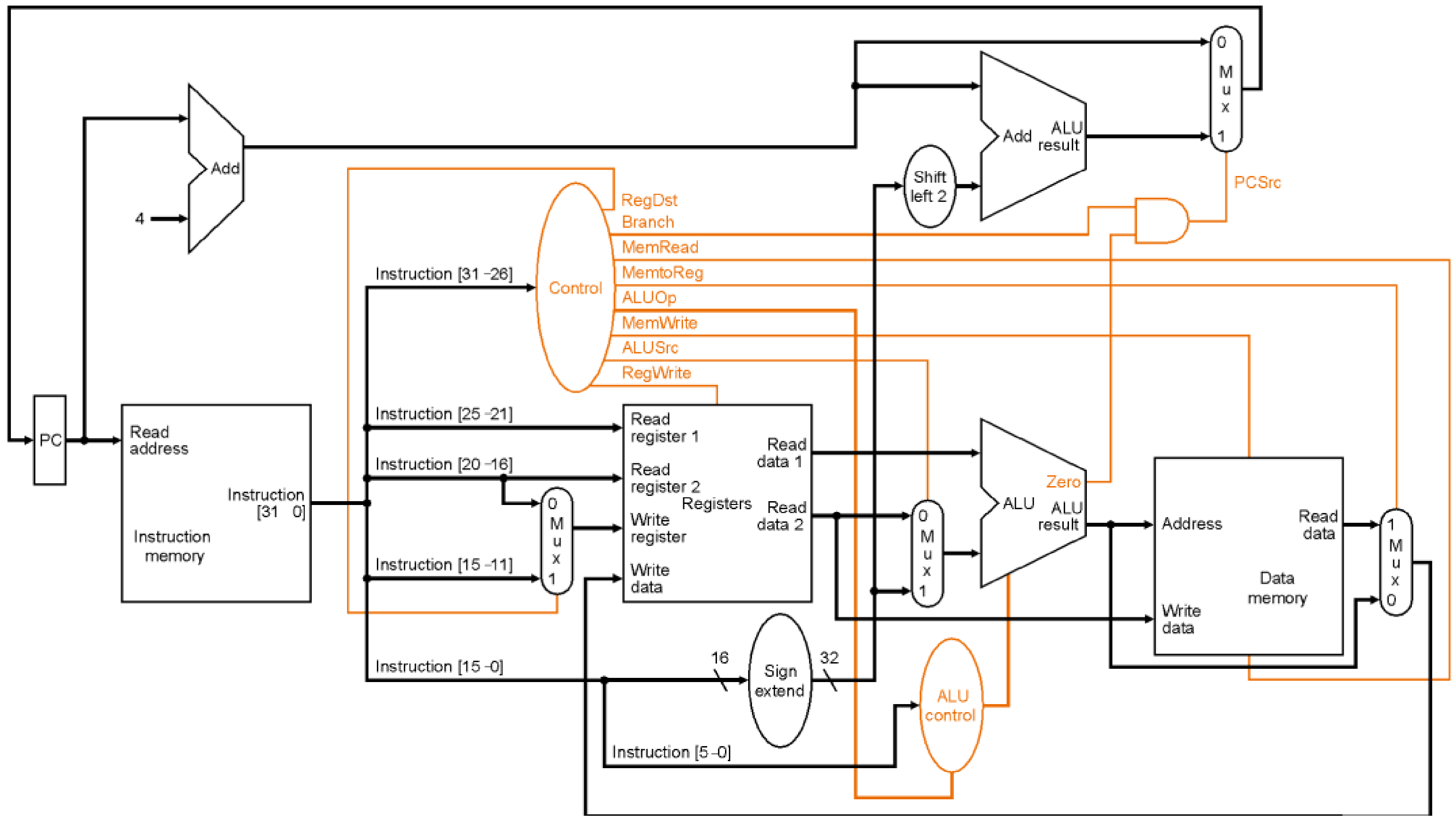
Tuesday, February 5, 13

Controlling the CPU



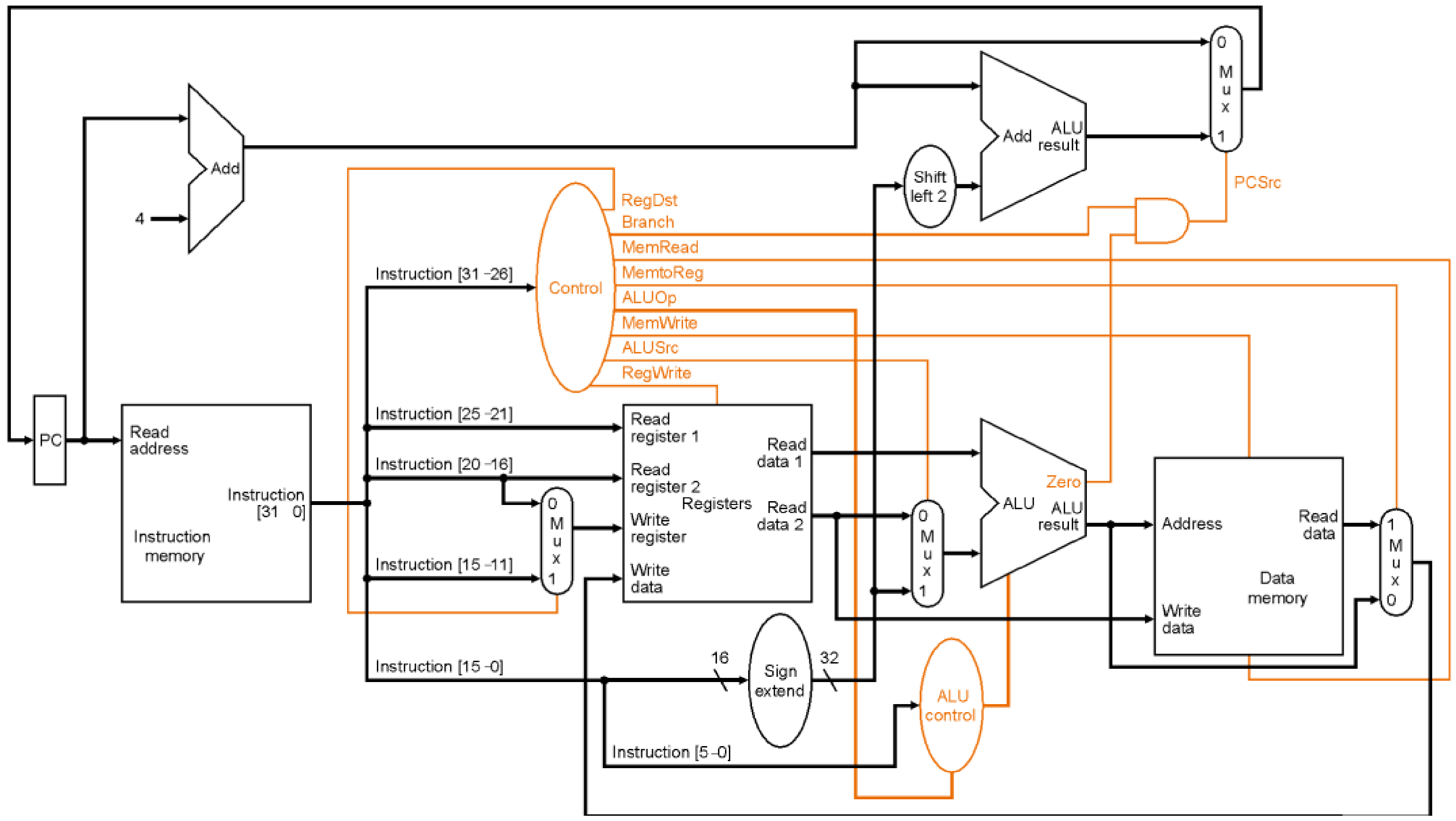
Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1	1	0		0	0
`sw`								0	0
`beq`								0	1

Controlling the CPU



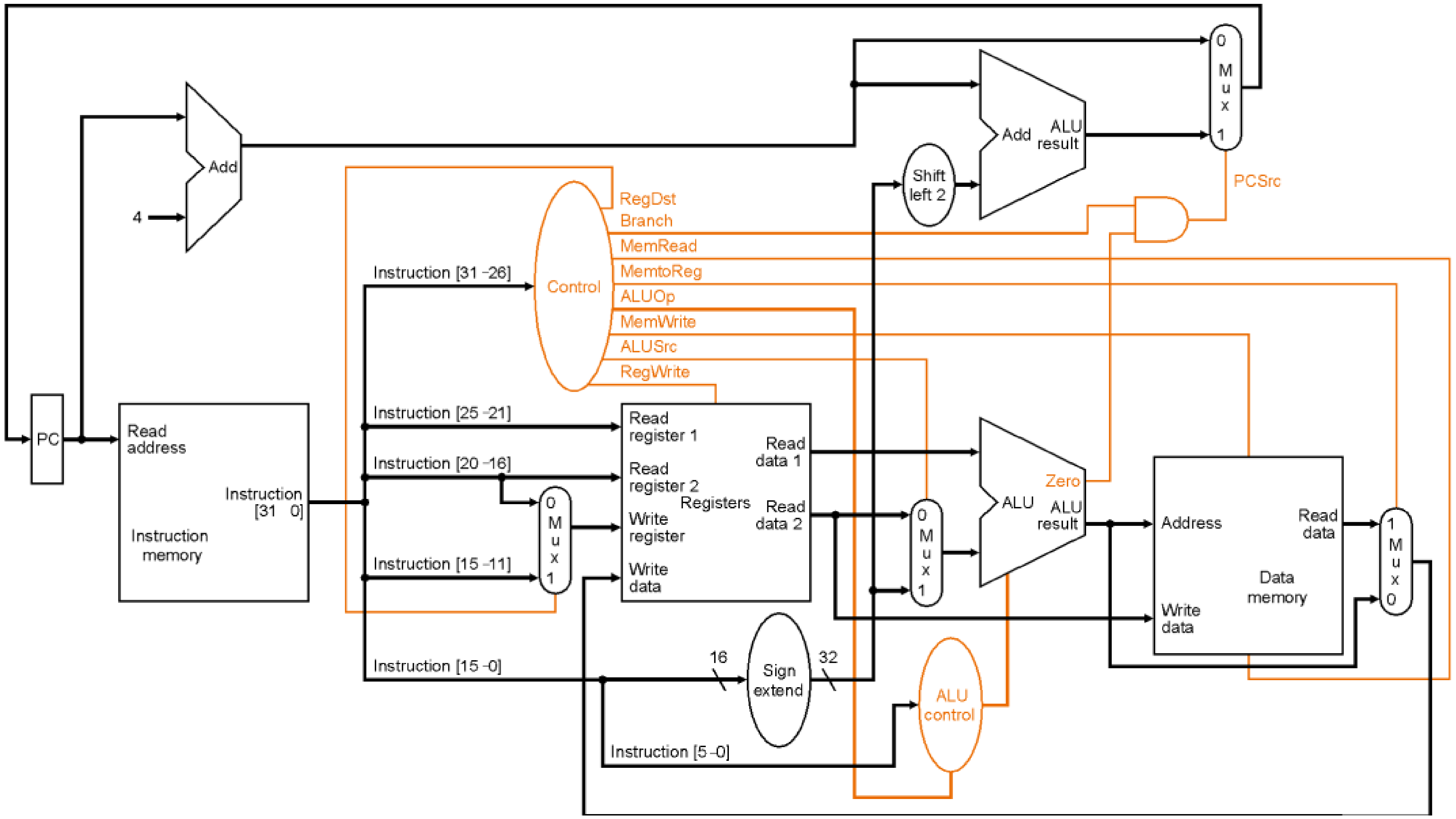
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1	1	0	0	0	0
`sw`								0	0
`beq`								0	1

Controlling the CPU



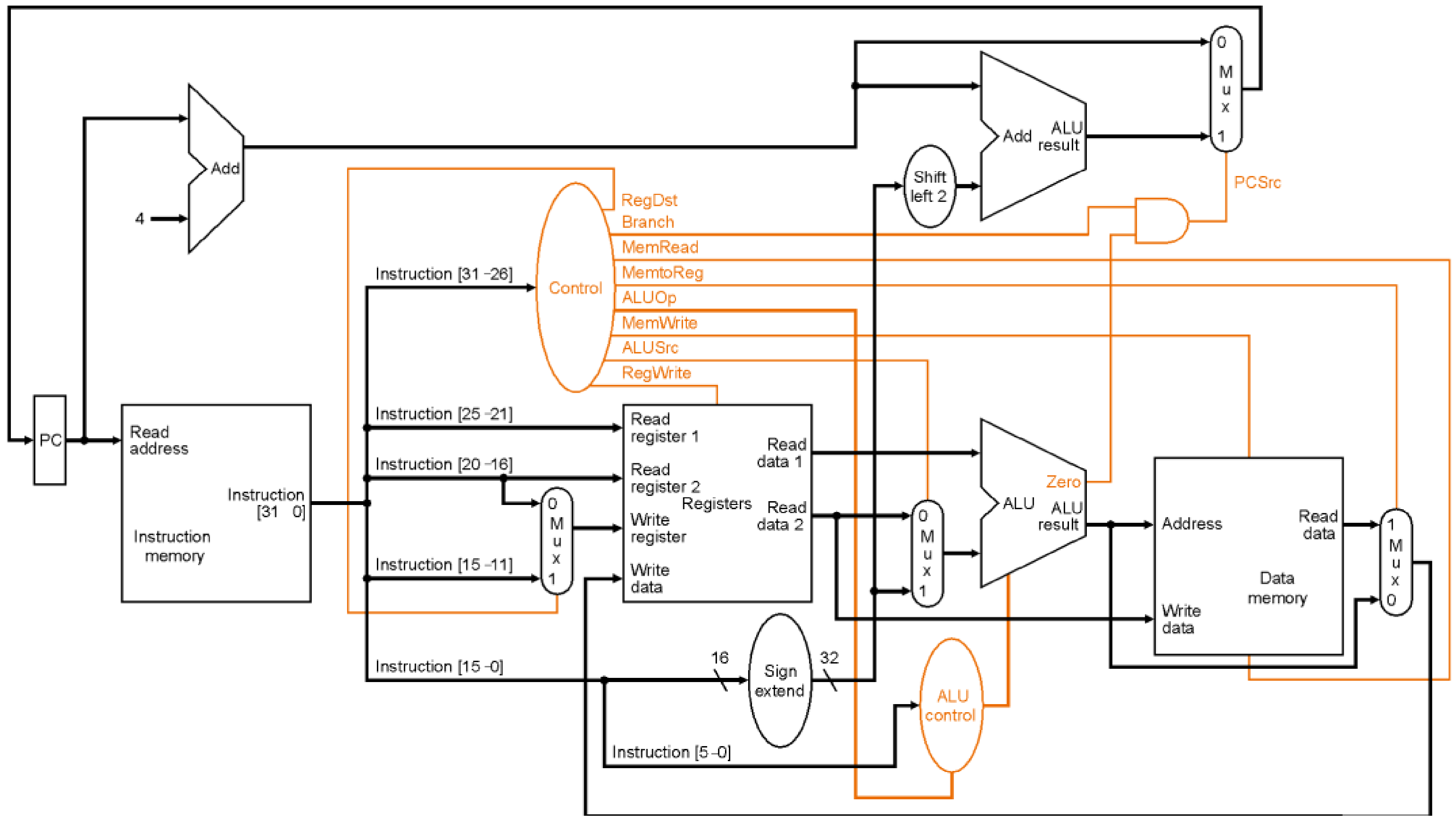
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X							0	0
beq								0	1

Controlling the CPU



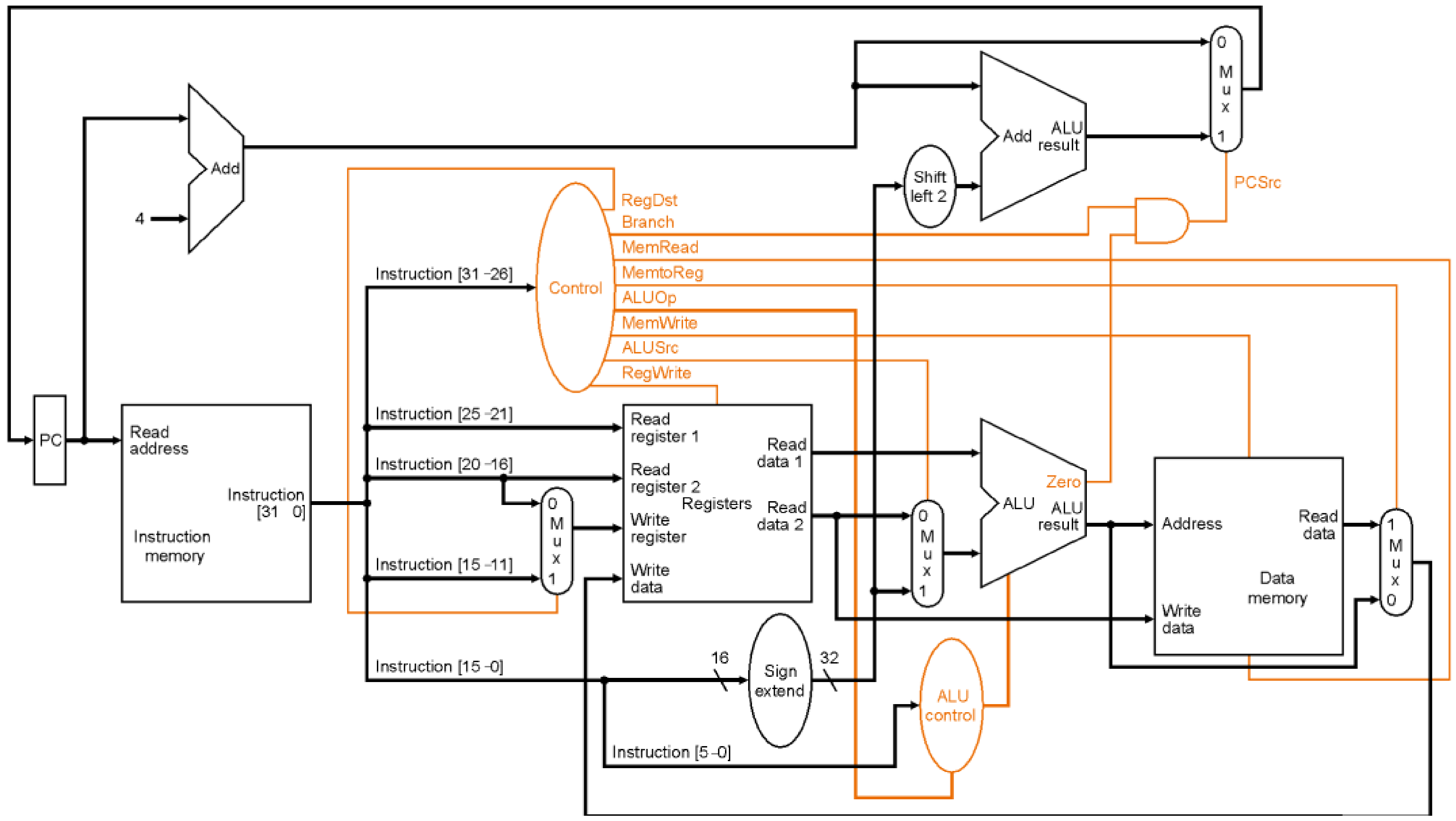
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1						0	0
beq								0	1

Controlling the CPU



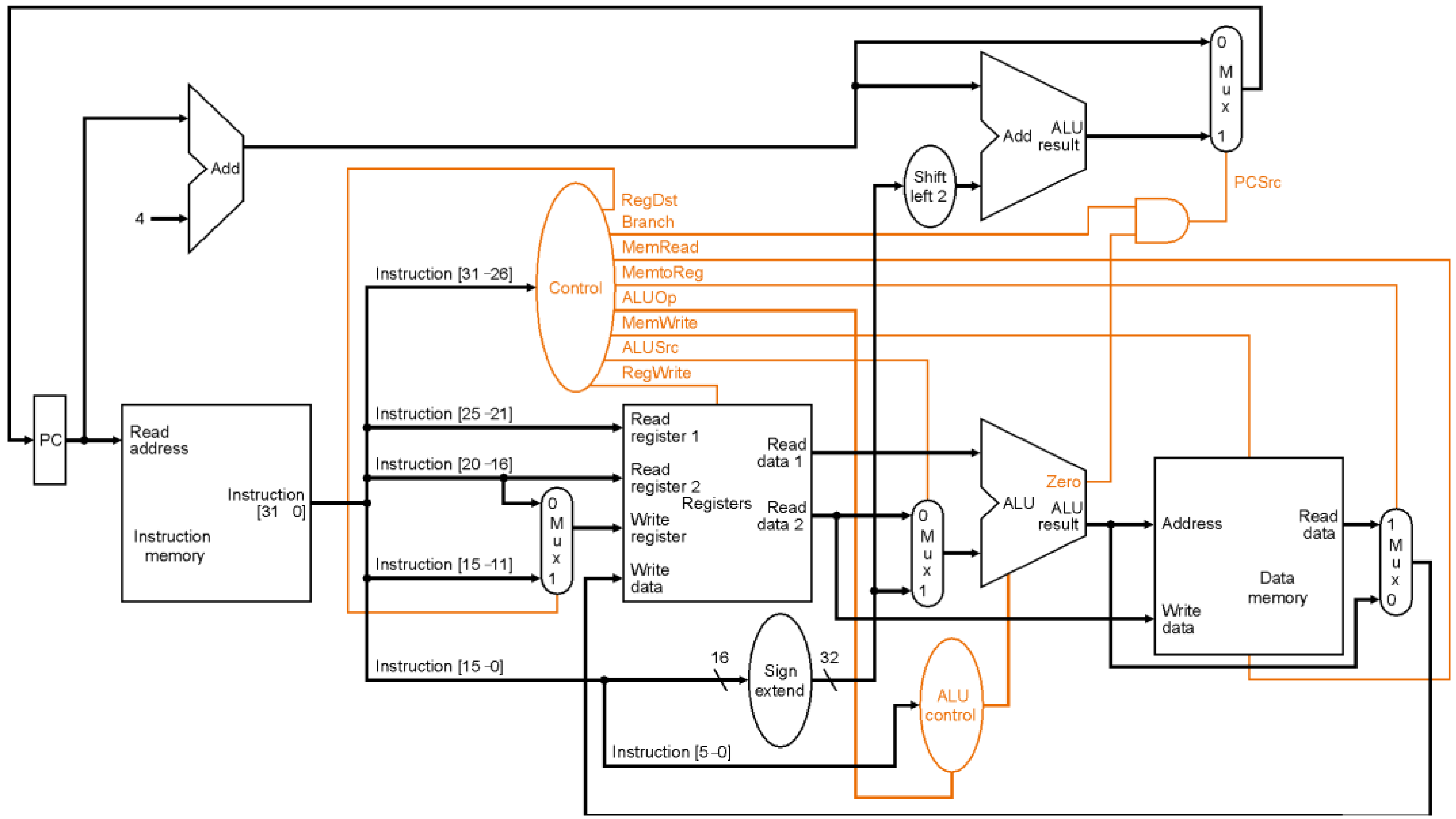
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1	1	0	0	0	0
`sw`	X	1	X					0	0
`beq`								0	1

Controlling the CPU



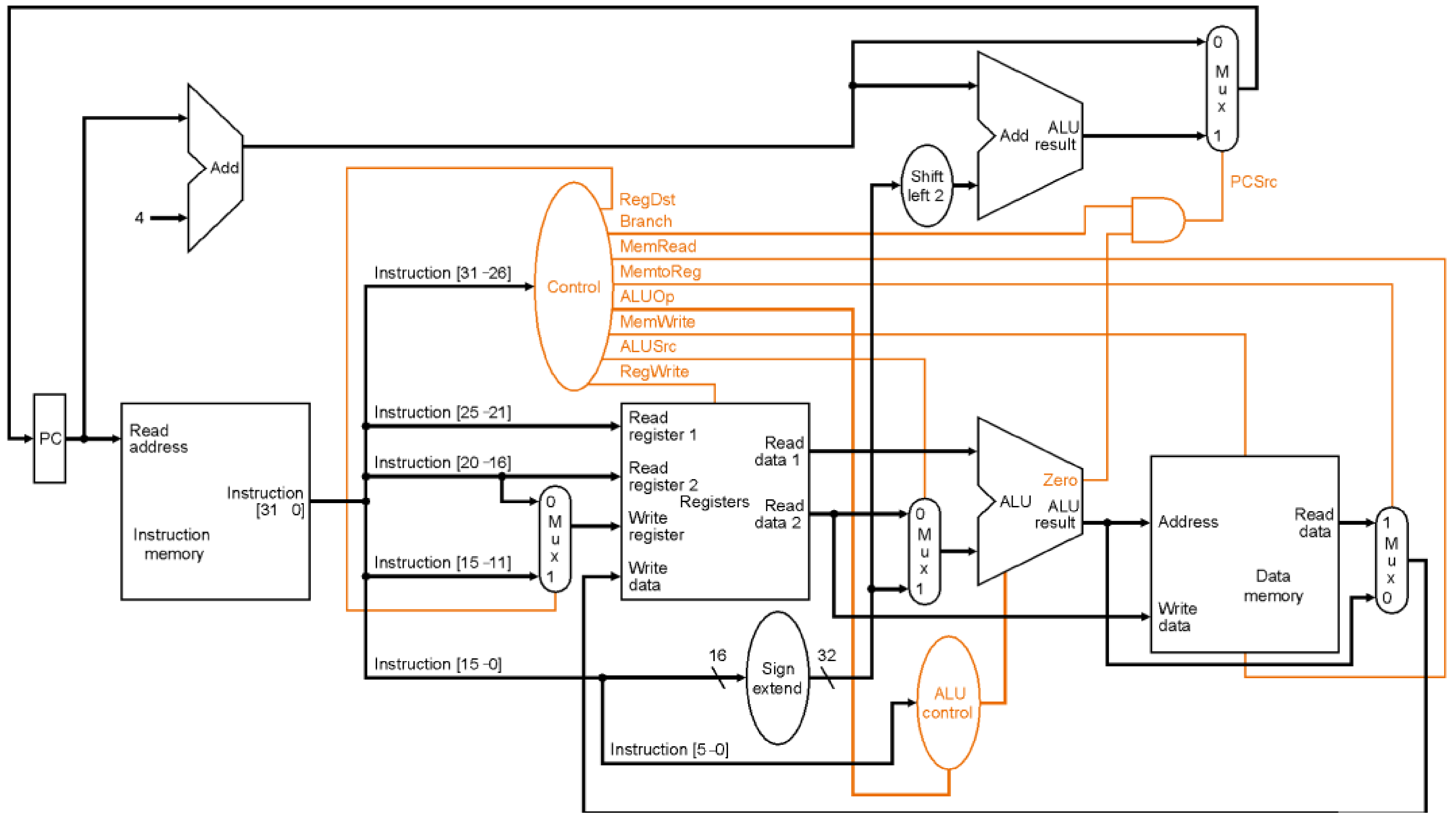
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0				0	0
beq								0	1

Controlling the CPU



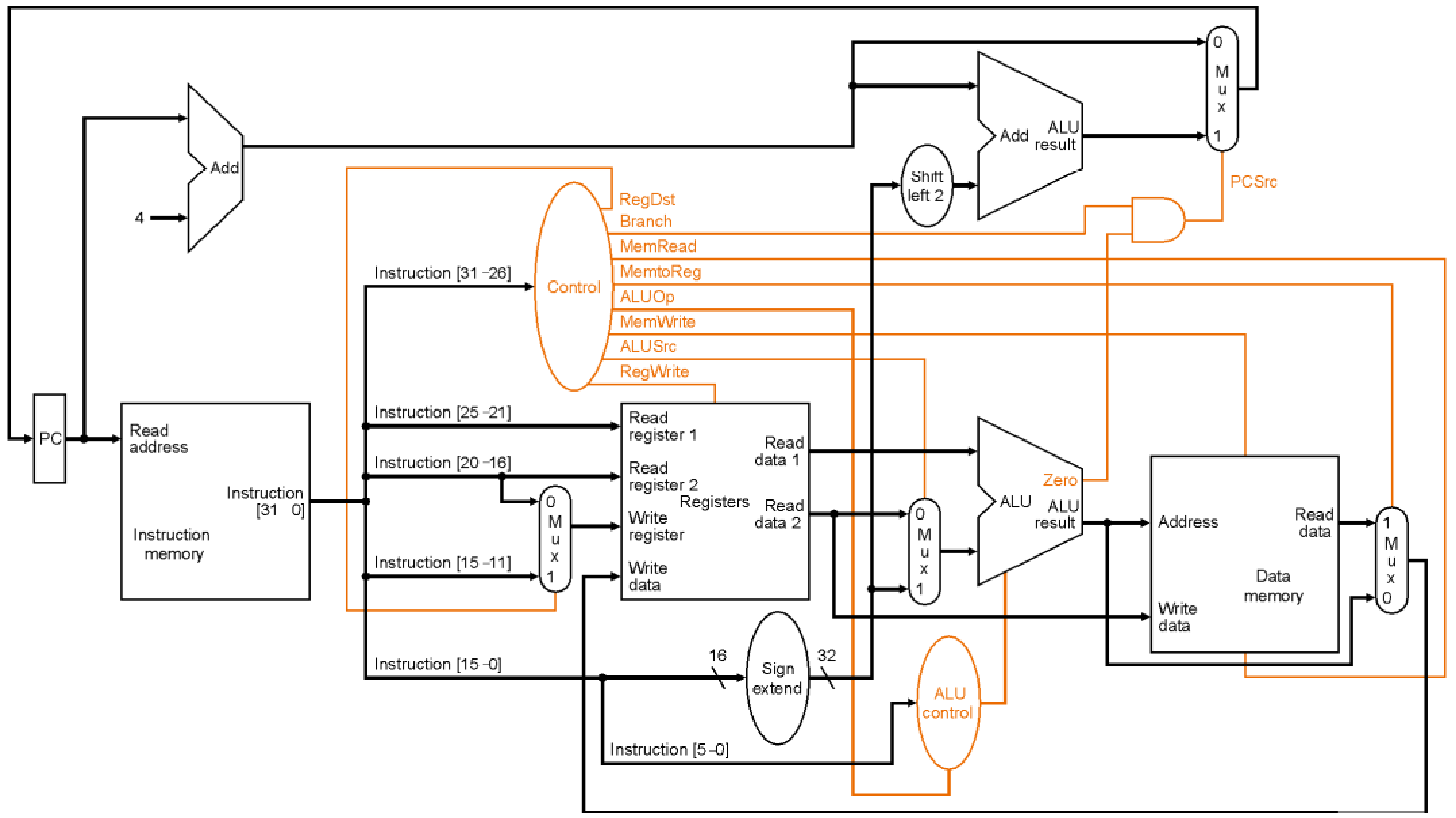
Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0			0	0
beq								0	1

Controlling the CPU



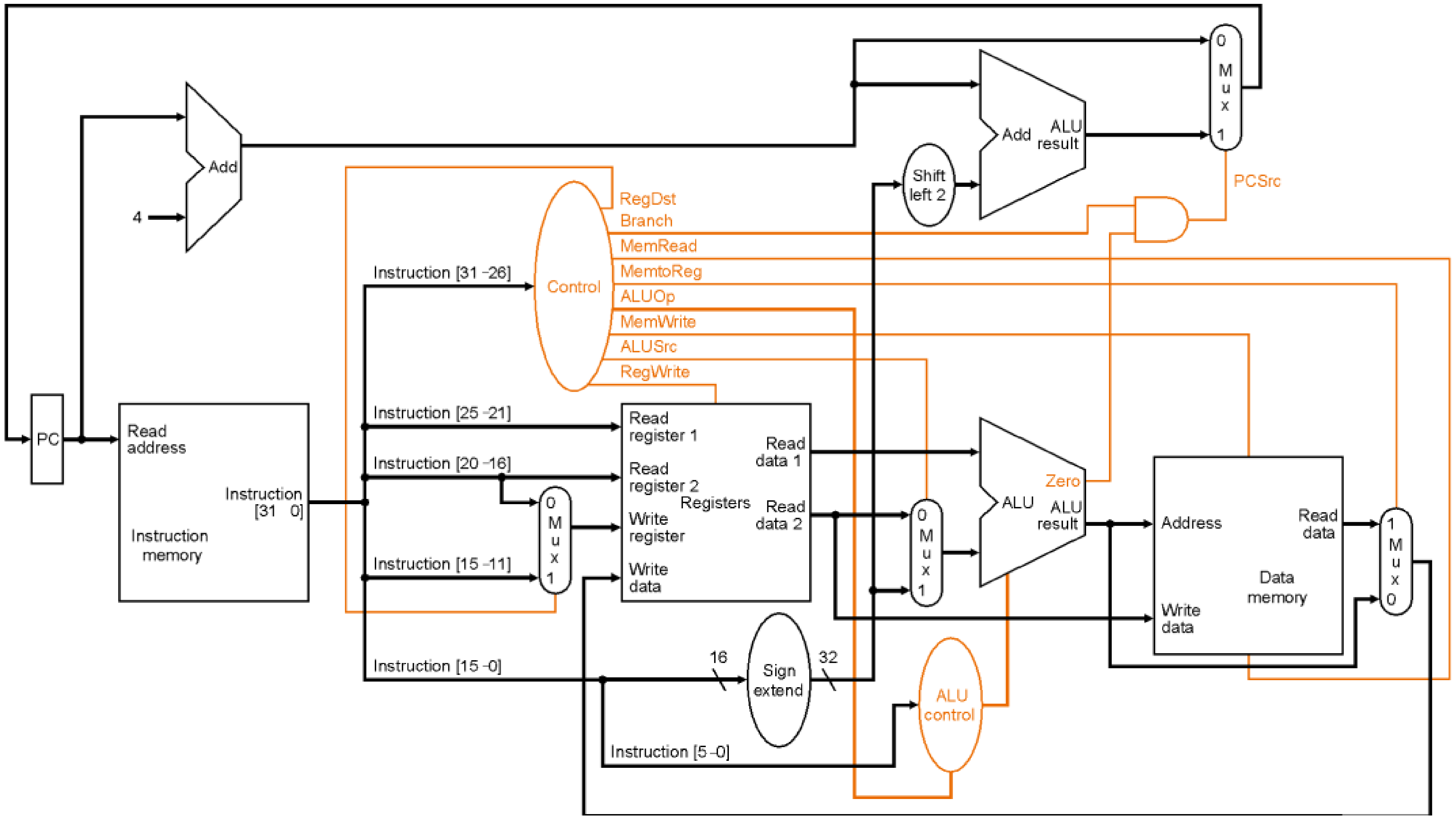
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1		0	0
beq								0	1

Controlling the CPU



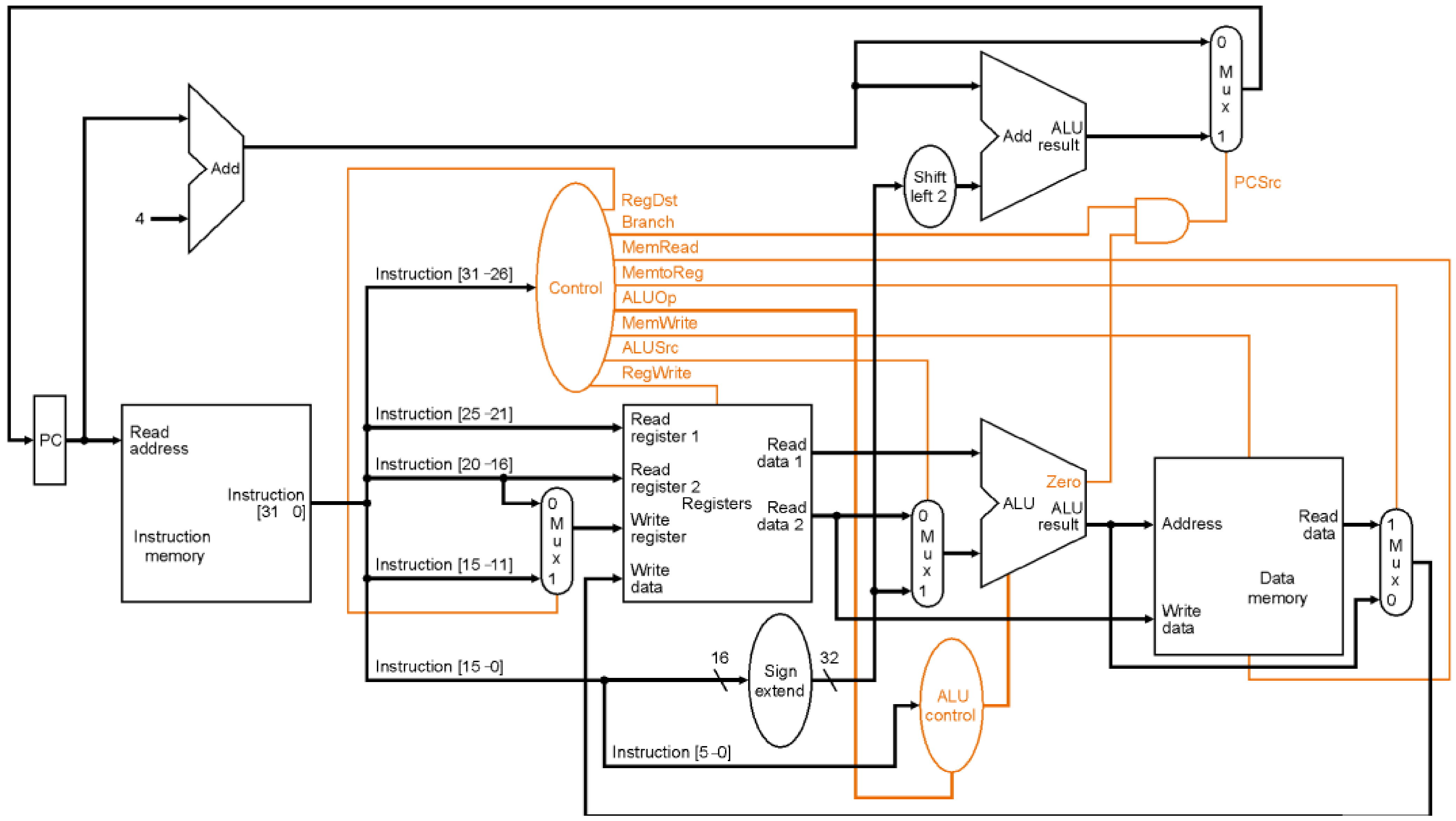
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1	1	0	0	0	0
`sw`	X	1	X	0	0	1	0	0	0
`beq`								0	1

Controlling the CPU



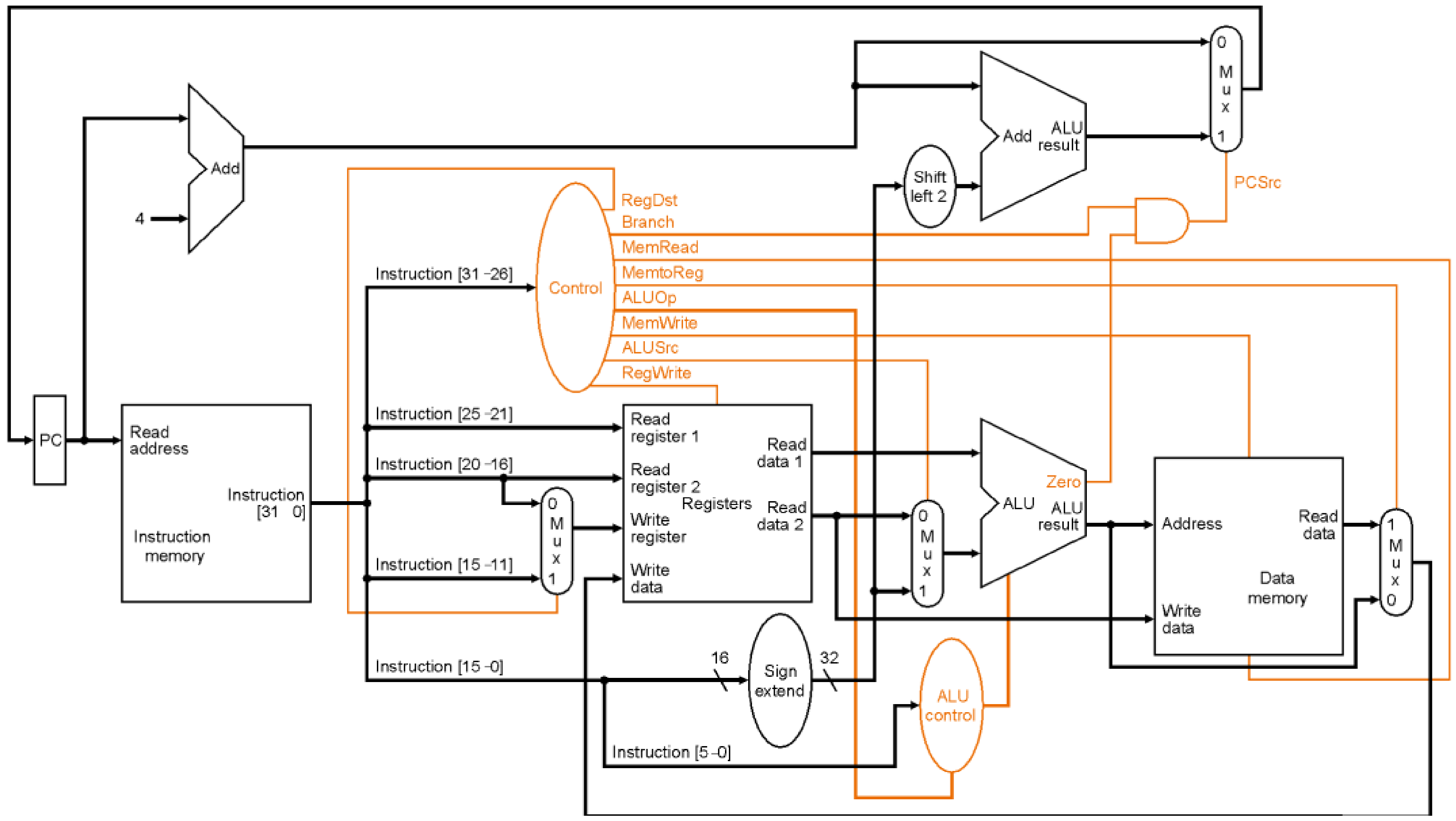
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X							0	1

Controlling the CPU



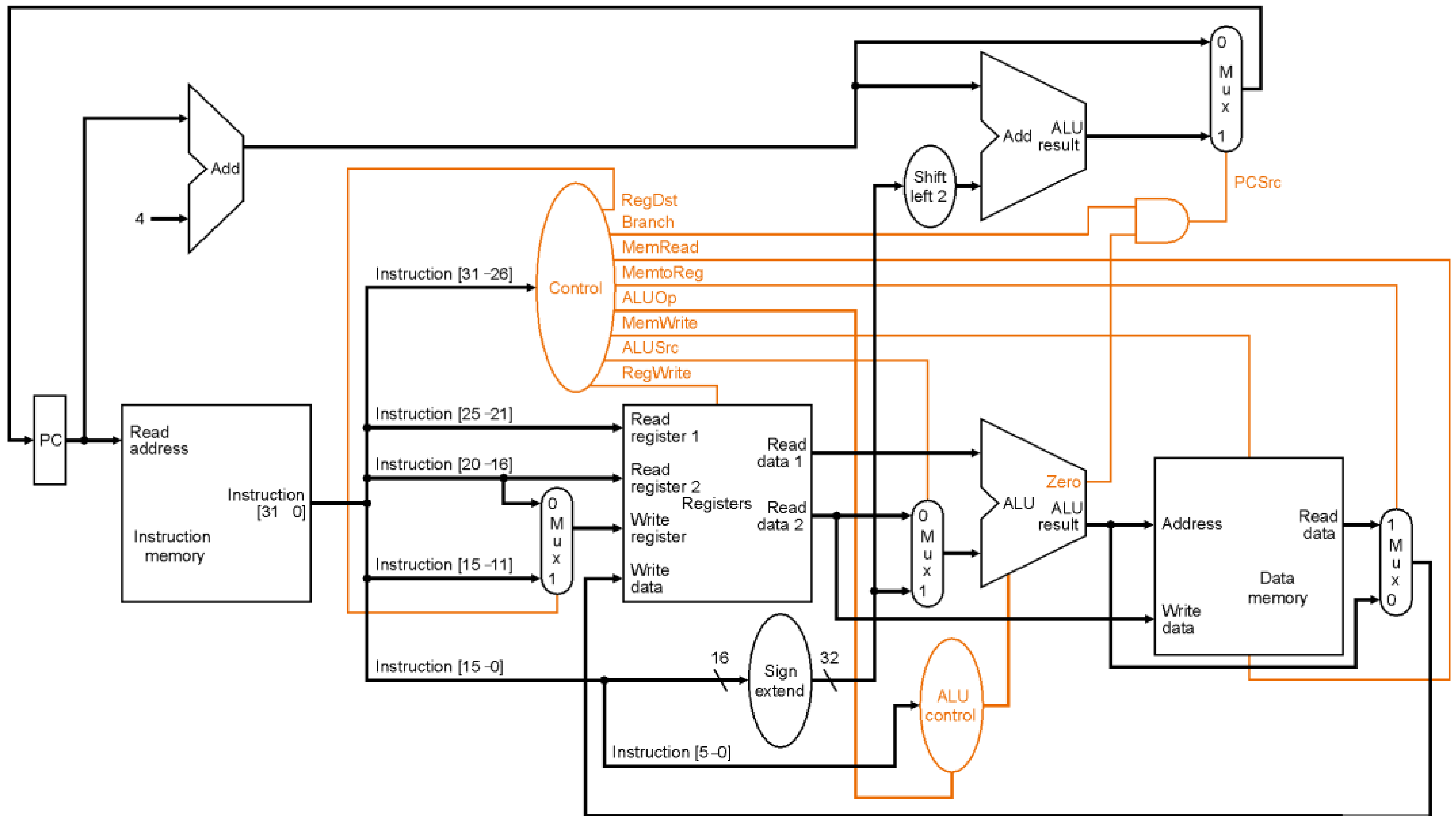
Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1	1	0	0	0	0
`sw`	X	1	X	0	0	1	0	0	0
`beq`	X	0						0	1

Controlling the CPU



Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X	0	X					0	1

Controlling the CPU



Instruction	RegDst	ALUSrc	Mem to-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1	1	0	0	0	0
`sw`	X	1	X	0	0	1	0	0	0
`beq`	X	0	X	0				0	1

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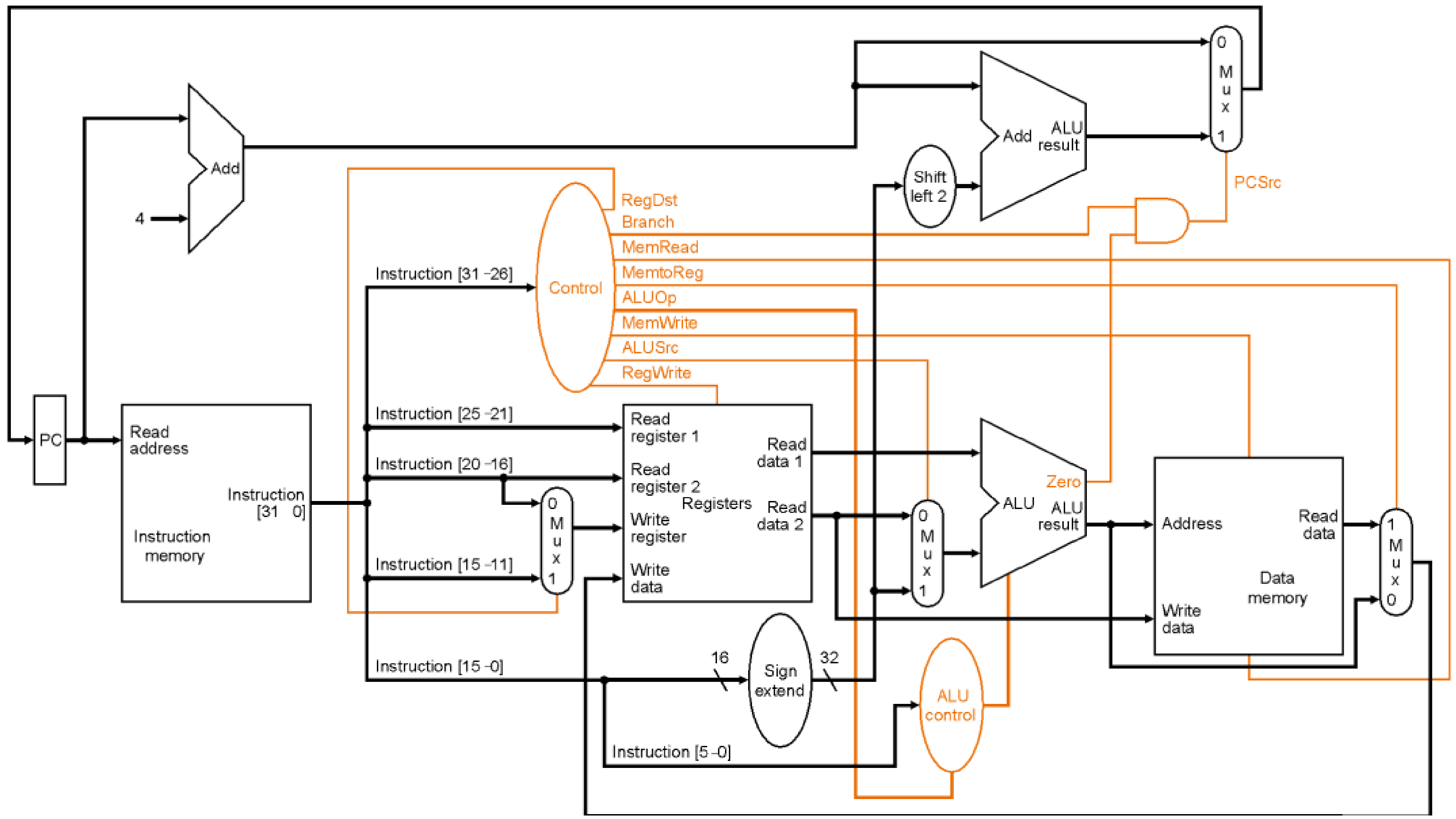

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`lw`	0	1	1	1	1	0	0	0	0
`sw`	X	1	X	0	0	1	0	0	0
`beq`	X	0	X	0	0			0	1

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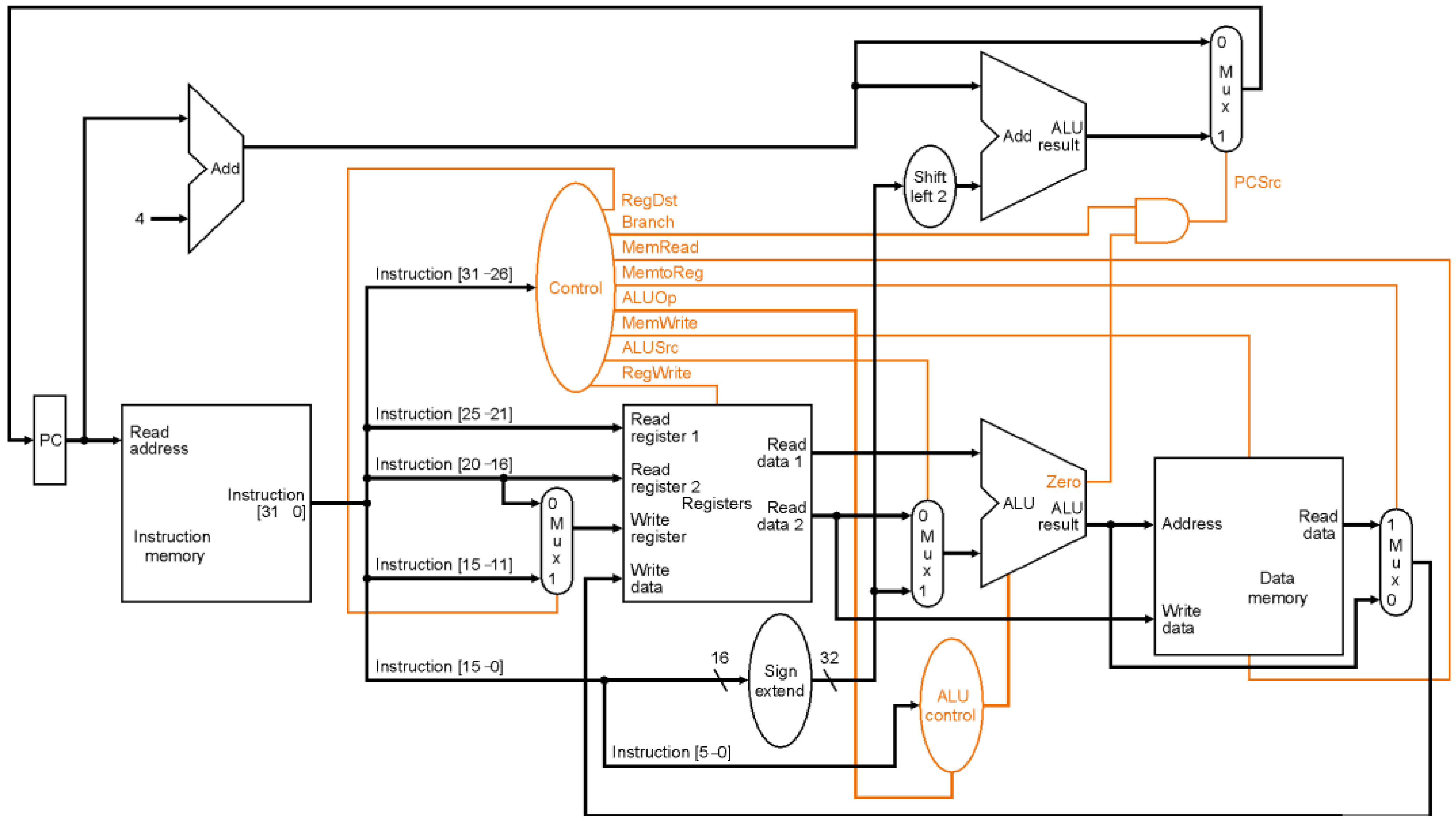

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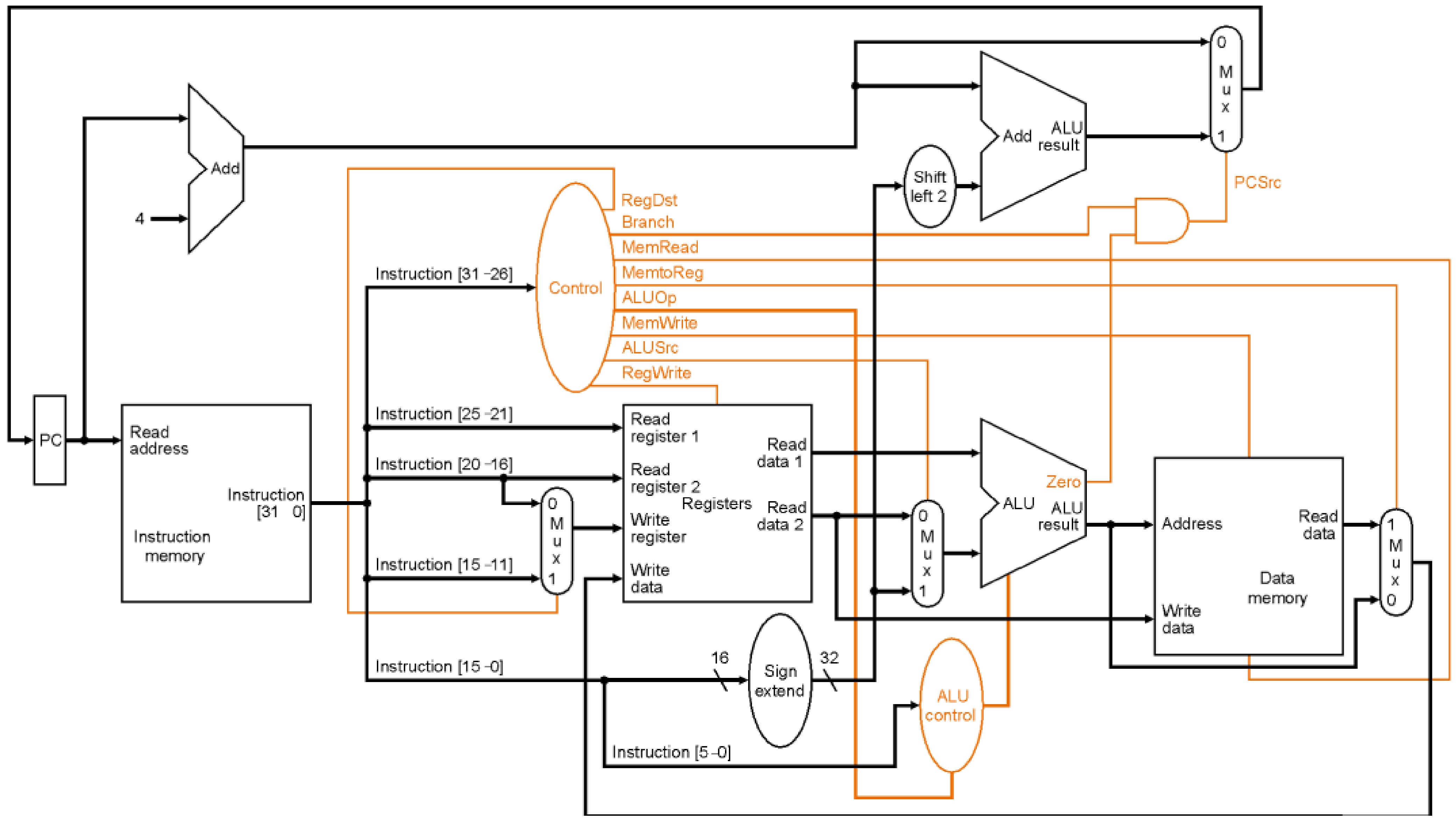
`sw`	X	1	X	0	0	1	0	0	0
`beq`	X	0	X	0	0	0		0	1

Controlling the CPU



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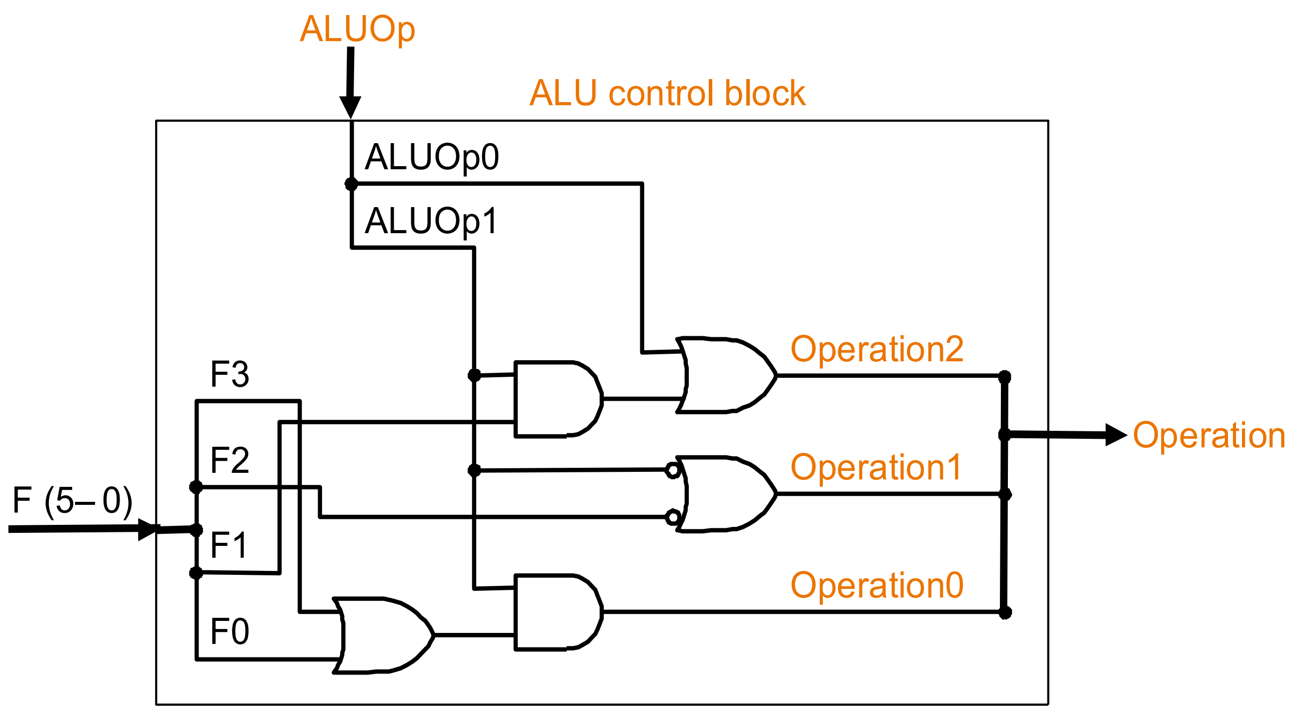
`beq`	X	0	X	0	0	0	1	0	1

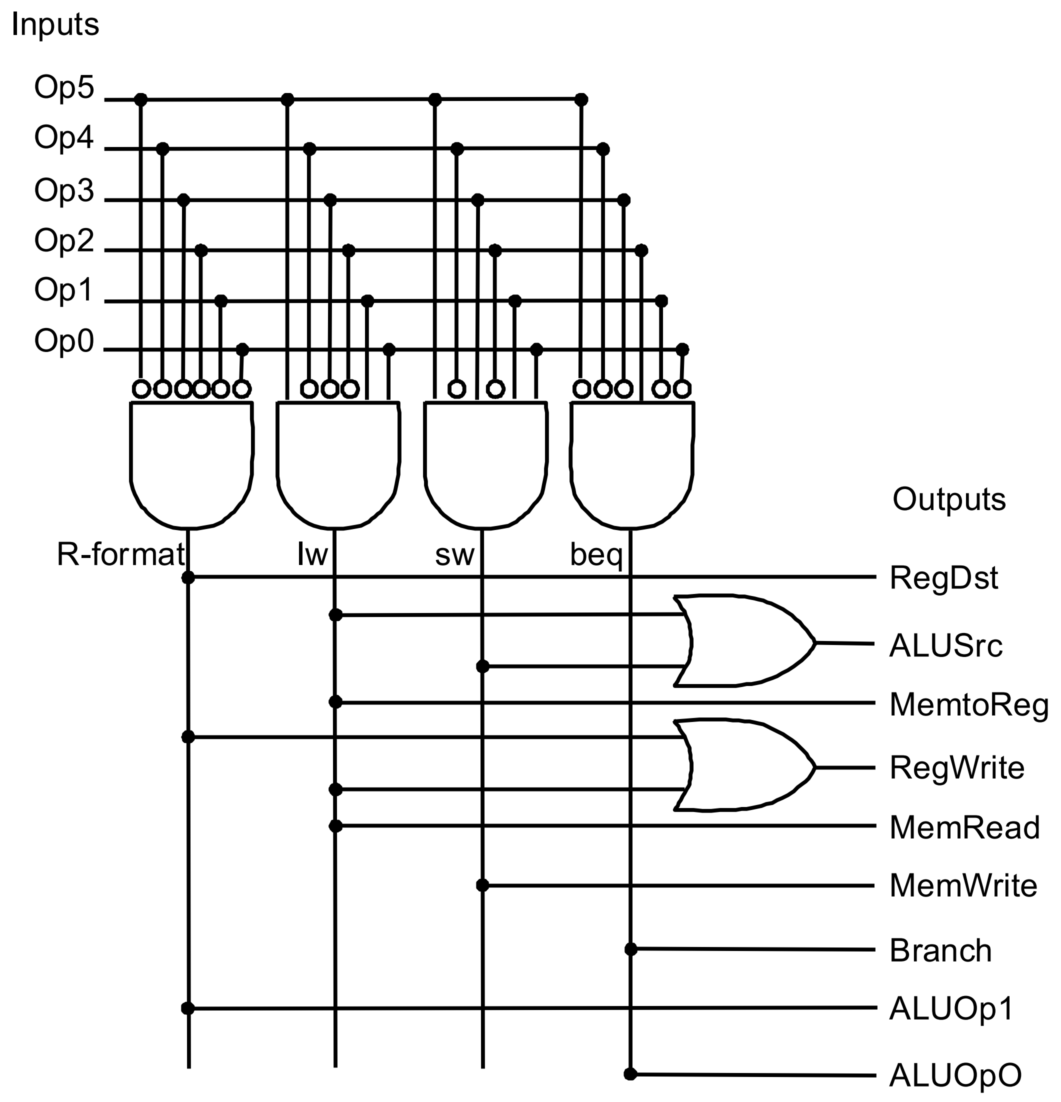
Control Truth Table

		R-format	**lw**	**sw**	**beq**
Opcode		000000	100011	101011	000100
Outputs	RegDst	1	0	x	x
	ALUSrc	0	1	1	0
	MemtoReg	0	1	x	x
	RegWrite	1	1	0	0
	MemRead	0	1	0	0
	MemWrite	0	0	1	0
	Branch	0	0	0	1
	ALUOp1	1	0	0	0
	ALUOp0	0	0	0	1

Control

- Simple Combinational Logic (truth tables)





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- Real machines have much more variable instruction latencies than this.