NanoFIP Frame Structure

Revision History			
Revision Number	*Date*	*Pages*	*Description*
v1.0	04/08/2009	ALL	First Draft
v1.1	05/08/2009	ALL	Minor mistake correction after review from E. van der Bij. Addition of hyperlinks to the referenced documents and made clear which bit is transmitted first for each field.
V1.2	07/07/2010	ALL	pg3: correction of CTRL field of ID_DAT and RP_DAT, according to IEC-61158-4-7 pg 34 Table 3.

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Introduction

The NanoFIP is an FPGA component implementing a minimal subset of the services offered by the WorldFIP protocol. NanoFIP is intended to be used as a station, producer or consumer of a variable and not as a bus arbiter. The station should be able to handle two types of frames: an *ID_DAT* and an *RP_DAT*.

An ID_DAT, the structure of which is shown in Figure 1, is broadcast by the bus arbiter to all the stations connected to the network segment to request for a specific variable. The station-producer of the variable will respond to this request by broadcasting to all the stations an RP_DAT frame shown in Figure 2, containing the variable requested. Finally the stations-consumers of this variable will consume the RP_DAT frame and the rest of the stations will simply ignore it.
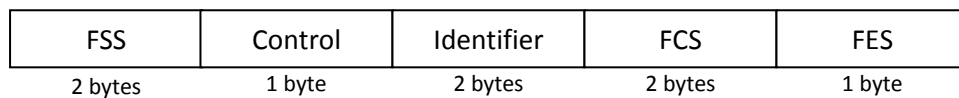
FSS	Control	Identifier	FCS	FES
2 bytes	1 byte	2 bytes	2 bytes	1 byte

Figure 1: *ID_DAT frame structure [IEC-61158-4-7 p32]*

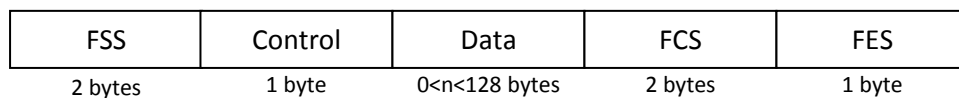| FSS	Control	Data	FCS	FES
2 bytes	1 byte	0<n<128 bytes	2 bytes	1 byte

Figure 2: *RP_DAT frame structure [IEC-61158-4-7 p32]*

The following sections describe the structure of each of the two frame types. Since most of the fields are the same between the two frames unless otherwise specified, what is described in the following sections is applicable to both. It is also important to note that in all fields described the leftmost bit (MSB) is transmitted first and the rightmost bit (LSB) is transmitted last.

Coding

Each data bit exchanged between the station is encoded before transmission using the Manchester 2 code. This code ensures that there is one transition for each bit. Therefore the signal carrying the data is self-clocking. This helps clock recovery. Additionally, since the average high time is equal to the low time, the code prevents DC built up. The coding scheme is described in Figure 3.
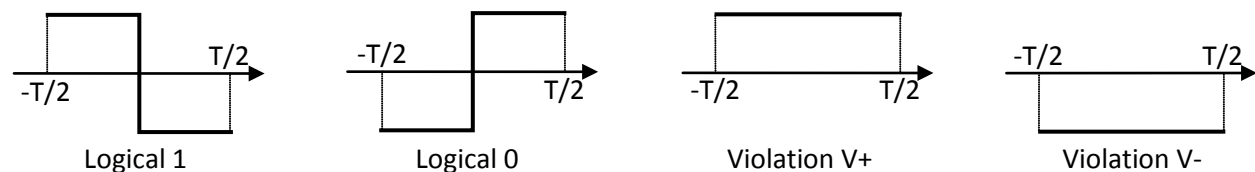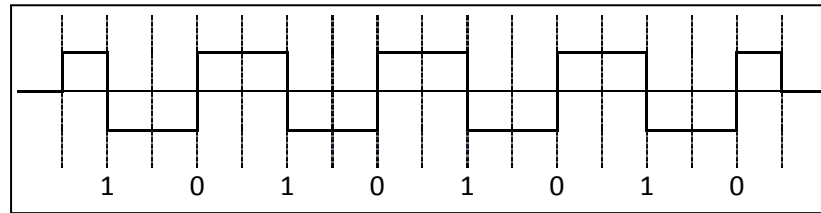

**Figure 3**: *Manchester 2 coding scheme*

Frame Start Sequence (FSS)

The *Frame Start Sequence (FSS)* consists of the *Preamble (PRE)* and the *Frame Start Delimiter (FSD)*.

The preamble is transmitted at the beginning of a frame in order to synchronise bit times and may contain from 8 bits down to as few as 4 bits [IEC-61158-2 p122]. The structure of the preamble field is shown in Figure 4.


Figure 4: *Preamble field*

The FSD immediately precedes the *control and data (CAD)* fields to delimit the start of frame. CAD are only accepted if the FSD is verified [IEC-61158-2 p122]. The structure of the FSD is shown in Figure 5.
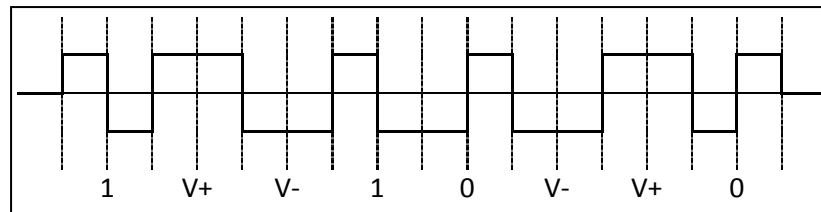
Figure 5: *Frame start delimiter field*

Frame End Sequence (FES)

The *Frame End Sequence (FES)* or *Frame End Delimiter (FED)* immediately follows the FCS field to indicate the end of frame. If a sequence of more than 300 bytes is received without receiving a FED then the frame is reported as too long. Additionally, if a frame is received with the FED not located at byte boundary, is also reported [IEC-61158-2 p122]. The structure of the FED is shown in Figure 6.
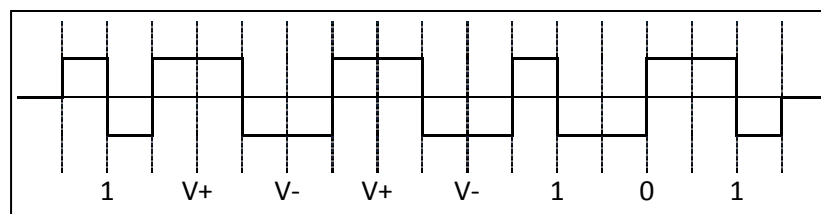

Figure 6: *Frame end delimiter field*

Control

The *Control (CTRL)* field specifies the type of frame being transmitted. For an ID_DAT frame CTRL(7:0) is "XX000011" and for an RP_DAT frame CTRL(7:0) is "XX000010". The 'X' indicates that the bit is ignored on reception but should be set to zero on transmission [IEC-61158-4-7 p33-34]. The structure of the control field for ID_DAT and RP_DAT is shown in Figure 7 and Figure 8 respectively.
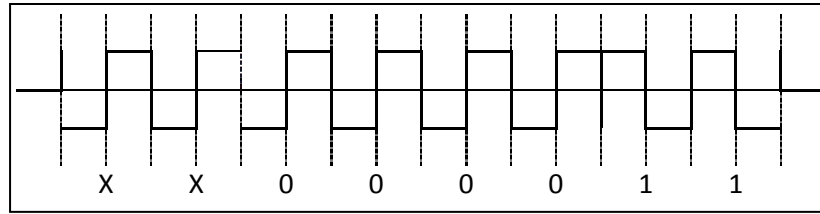
Figure 7: *ID_DAT control field*
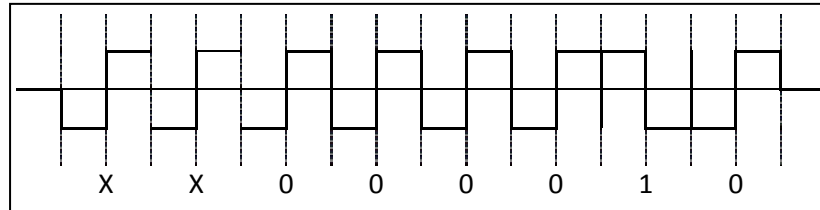
Figure 8: *RP_DAT control field*

Frame Check Sequence (FCS)

Error detection is provided by calculating and appending a *Frame Check Sequence (FCS)* after the Data/Identifier field. The FCS is evaluated on the Control and Data/Identifier fields using a *Cyclic Redundancy Check (CRC)* function [IEC-61158-4-7 p34-36]. An example of a CRC generator and syndrome check implementation is shown in [IEC-61158-4-7 p97]. The redundancy bits are evaluated by shifting the data bit by bit into the CRC generator (Data Select). When all the data enter the generator, the contents of the flip-flops contain the 16bit FCS which is obtained by shifting out the contents of the flip-flops (FCS Select). Similarly at the syndrome check, the received data are shifted in the validation block bit by bit. When all the data enter the verification block and if no error occurred during transmission, the contents of the flip-flops should be equal to: 1110 0011 1001 0100 (X15 to X0, respectively). It should be noted that the contents of the flip-flops in both the generator and verification blocks are initialised to all logical '1's before any data are shifted in the registers.

Data/Identifier

The *Identifier* field's contents are as specified in the NanoFIP specification document [NanoFIP Functional Specification p8-11] and the *Data* field contains the data requested by the identifier in the ID_DAT frame.

Timing

Silence Time is defined as the maximum time allowed without any activity after an ID_DAT has been received. The timer is initiated when an indication of absence of activity is received (SILENCE signal is asserted). It is terminated when an indication of activity is received due to the reception or transmission of the first frame symbol (BUSY signal is asserted). In the case of a consuming station the timer is named T4. Expiration of this timer causes the station to enter a status of waiting for the next ID_DAT frame (i.e. the current RP_DAT is considered lost and hence ignored) [IEC-61158-4-7 p39-43].

The reception or emission of the last frame symbol is signalled by a SILENCE indication. Likewise, the reception or emission of the first frame symbol is signalled by a BUSY indication. The time elapsed between these two signals within a single station defines the station's *Turnaround Time*, whether the station's function be that of a producer/consumer or bus arbitrator. The minimum turnaround time (response time) and the silence time at each data rate are specified in the NanoFIP specification document [NanoFIP Functional Specification p7].