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| BE/CO/HT  2009-06-26 | | | | | |
| Technical Note | | | | | |
| WORLDFIP INSOURCING PROJECT  NanoFIP WP3  NanoFIP  USER’S GUIDE | | | | | |
|  | | | | | |
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|  | | | | | |
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# RESET inputs

In order to reset the whole of the nanoFIP chip, the user has to activate both the **RSTIN** and the **RST\_I** signals. RSTIN resets all the logic in the user 40 MHz clock domain, whereas the RST\_I resets all the logic in the WISHBONE clock domain. The Power On Reset, **RSTPON** resets both “worlds”. If the operation is in stand-alone mode, RSTIN resets all the logic in use.

## RSTPON

Since in no Actel ProAsic3 documentation we could find a warrantee that all the flip-flops of the chip start at “0” right after power-up, we concluded that a Power On Reset is essential for nanoFIP. After a short survey summarized in [] we decided to use a R-C circuit that acts asynchronously and is removed synchronously.

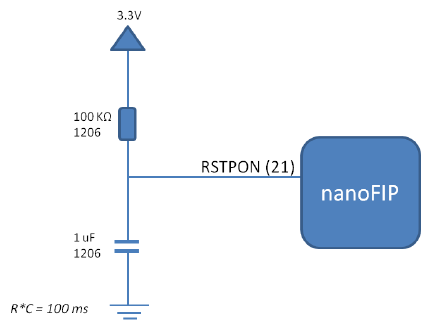


Figure : Power On Reset circuit

The RSTPON resets both the user and the WISHBONE logic, therefore the de-assertion synchronization is realised in both worlds. Two flip-flops are used for the synchronization, with the second used to remove any metastability that might be caused by the RSTPON being removed asynchronously and too close to the rising clock edge.

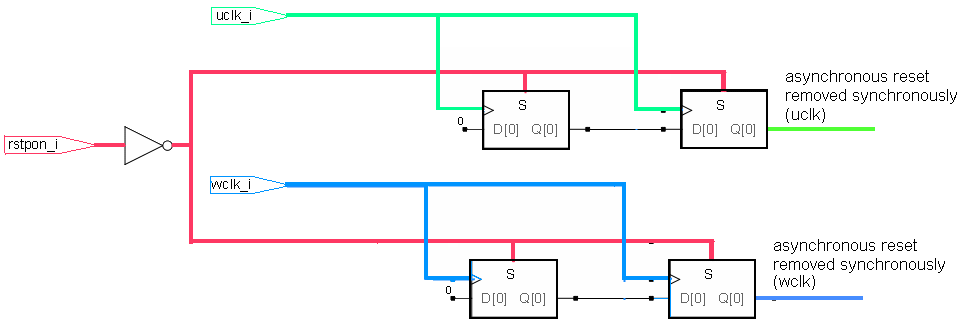


Figure : RSTPON synchronizers

*Note: The RSTPON does not activate nanoFIP’s RSTON output.*

## nanoFIP internal reset

nanoFIP logic running with the uclk is reset by:

* The RSTPON: the reset lasts for as long as the RSTPON is asserted plus 2 uclk cycles.
* The RSTIN: nanoFIP checks if RSTIN has stayed asserted for at least 8 uclk cycles and then asserts the nanoFIP internal reset for 1 uclk cycle.
* The reset variable (E0..h): nanoFIP is validating the consumed frame (in terms of Control, PDU\_TYPE, Length and FCS bytes and Manchester encoding) and checks if the first byte contains the station’s address; if so, it asserts nanoFIP’s internal reset for 1 uclk cycle.

## NANOFIP WISHBONE LOGIC RESET

nanoFIP WISHBONE logic running with the wclk is reset by:

* The RSTPON: the reset lasts for as long as the RSTPON is asserted, plus 2 wclk cycles.
* The RST\_I: following the WISHBONE rule 3.15 “all self-starting state machines and counters in WISHBONE interfaces MUST initialize themselves at the rising wclk edge following the assertion of RST\_I. They MUST stay in the initialized state until the rising wclk edge that follows the negation of RST\_I”.

# Reset outputs

## FD\_RST, FIELDRIVE RESET

nanoFIP asserts the output FD\_RST when:

* The RSTPON is asserted: the reset lasts for as long as the RSTPON is asserted plus 2 uclk cycles.
* The RSTIN is asserted: nanoFIP checks if RSTIN has stayed asserted for 8 uclk cycles and then asserts the FD\_RST for 4 FD\_TXCK cycles.
* A valid reset variable (E0..h) has been received with the first byte containing the station address: nanoFIP asserts FD\_RST for 4 FD\_TXCK cycles.

## rston, user reset

nanoFIP asserts the output RSTON only

* after the reception of a valid reset variable (E0..h) with the second byte containing the station address; the RSTON stays asserted for 8 uclk cycles.

# WISHBONE STB and ACK

When nanoFIP detects a rising edge on the STB\_I signal, it checks:

* If the CYC\_I signal is asserted and
* If the address provided ADR\_I belongs to the Produced memory block and the WE\_I is enabled or if the address provided belongs to the Consumed memory block and the WE\_I is disabled

If so, it asserts the ACK\_O for 1 wclk cycle.

Note: nanoFIP is synchronizing the WISHBONE control signals with triple buffers, therefore the ACK\_O signal appears 4 wclk cycles after the STB\_I rising edge.

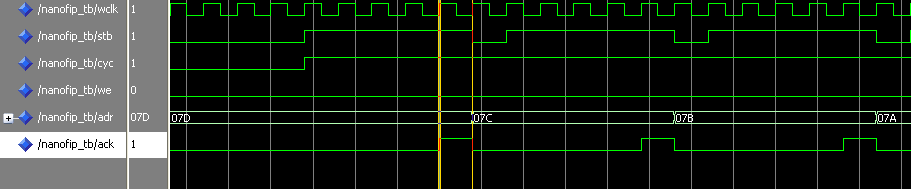


Figure : Read cycle WISHBONE control signals

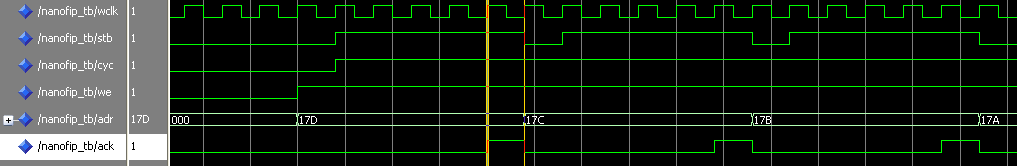


Figure : Write cycle WISHBONE contol signals

# VARx\_RDY signals

## VAR1\_RDY, VAR2\_RDY

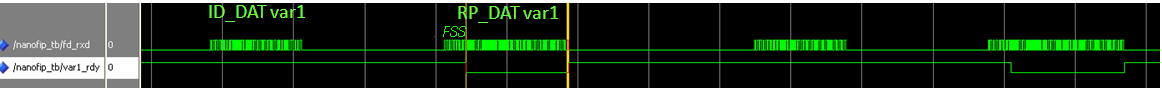
For the consumed variables var1 and var2, after the reception of a var1/ var2 ID\_DAT, nanoFIP de-asserts the signal VAR1/2\_RDY at the reception of the corresponding consumed RP\_DAT FSS. After the end of the reception and the validation of the RP\_DAT, nanoFIP re-asserts the VAR1/2\_RDY to signal the user for the new reception.

Figure : VAR1/2\_RDY handling

## VAR3\_RDY

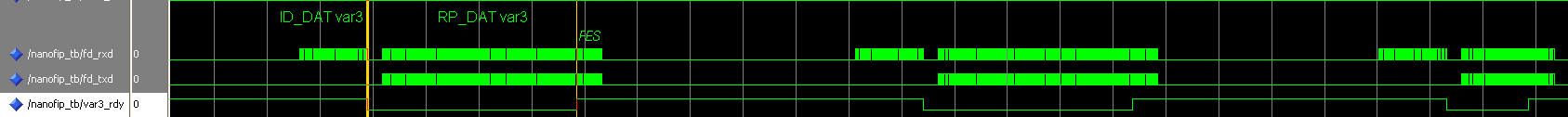
nanoFIP de-asserts the signal VAR3\_RDY after the reception of a valid var3 ID\_DAT. It re-asserts it at the FES delivery of the corresponding produced RP\_DAT frame.

Figure : VAR3\_RDY handling

# FD\_RXD and FD\_RXCDN

The FIELDRIVE does not provide echo cancellation, therefore in the input FD\_RXD appears also what nanoFIP is putting in the line through FD\_TXD.

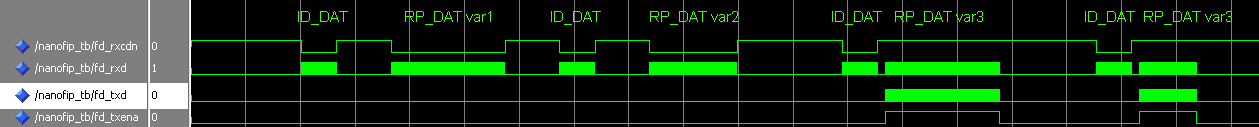


Figure : FD\_RXCDN & FD\_RXD nanoFIP inputs along with FD\_TXD & TX\_TXENA outputs

*NOTE: The reception activity signal FD\_RXCDN was decided not to be used in the design, in order to make nanoFIP compatible with other transceivers too.*

# WISHBONE interface & memories

The WISHBONE signals DAT\_I and ADR\_I are directly connected to the nanoFIP memories.

In the case of the Produced RAM, where the user is writing bytes to the memory, the write\_enable signal that is used is the ACK\_O (see paragraph 3).

# ConsRAM.pngProdRAM.png

Figure : nanoFIP Memories and WISHBONE interface signals

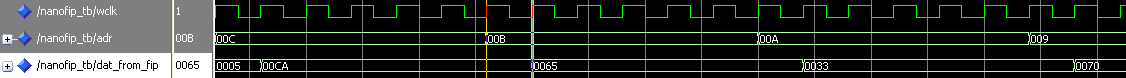
In the case of the Consumed RAM, the DAT\_O bus receives its value 1 wclk cycle after the setting of a new ADR\_I.

Figure : WISHBONE reading cycle ADR\_I and DAT\_O signals

# M\_ID and C\_id usage

Each one of the four pins of the M\_ID and C\_ID can be connected to either Vcc, Gnd, S\_ID1 or S\_ID0. After 2 uclk cycles each of the pins is translated to 2 bits (Table 1) and therefore the 8 bit words for the Model and the Constructor get defined. The signals S\_ID0 and S\_ID1 provide 2 opposite clocks (when one is ‘0’ the other is ‘1’ and vice-versa).

|  |  |
| --- | --- |
| **M\_ID, C\_ID pin connected to** | **Corresponding pair of bits** |
| **Gnd** | **00** |
| **S\_ID1** | **10** |
| **S\_ID0** | **01** |
| **Vcc** | **11** |

Table : Options for M\_ID/ C\_ID pins and corresponding bits translation

The following examples clearify the concept:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Model Word** | **M\_ID[3]** | **M\_ID[2]** | **M\_ID[1]** | **M\_ID[0]** |
| **00000000** | Gnd | Gnd | Gnd | Gnd |
| **00000001** | Gnd | Gnd | Gnd | S\_ID0 |
| **00000101** | Gnd | Gnd | S\_ID0 | S\_ID0 |
| **00001010** | Gnd | Gnd | S\_ID1 | S\_ID1 |
| **11010110** | Vcc | S\_ID0 | S\_ID0 | S\_ID1 |

Table : Examples of Model words with their M\_ID[] pins configuration

# ID\_DAT frames and the nanoFIP status byte

It is important to note that the bits 4 and 5 of the nanoFIP status byte refer only to consumed RP\_DAT frames. nanoFIP is not providing information of errors that may have been detected in ID\_DAT frames. Wrong ID\_DAT frames are just neglected.

# Turnaround and Silence times

Turnaround is the time that nanoFIP waits after the reception of a valid presence or identification or variable3 ID\_DAT before it starts delivering the corresponding RP\_DAT.

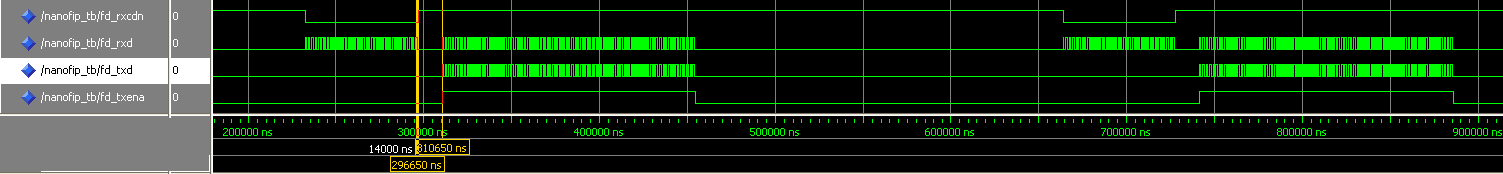
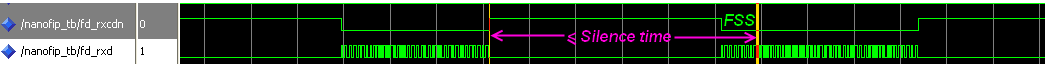


Figure : nanoFIP Turnaround time (1 MHz)

Silence time is the maximum time that nanoFIP waits for an RP\_DAT after the reception of a valid variable 1 or 2 or reset ID\_DAT. nanoFIP goes back to idle state if the silence time has expired and no FSS has arrived.

# nanofip device CHARACTERISTICS

Figure : nanoFIP Silence time (1 MHz)

nanoFIP is housed in an ACTEL ProASIC3 device with the following characteristics:

|  |  |
| --- | --- |
| **Family** | **ProASIC3** |
| **Die** | **A3P400** |
| **Packaging** | **208 PQFP** |
| **Speed** | **-2** |
| **Die Voltage** | **1.5** |
| **I/O Attributes** | **LVTTL** |
| **Junction Temperature** | **COM** |