CPEN 230L: Introduction to Digital Logic Laboratory
Lab #3: One Gate Type
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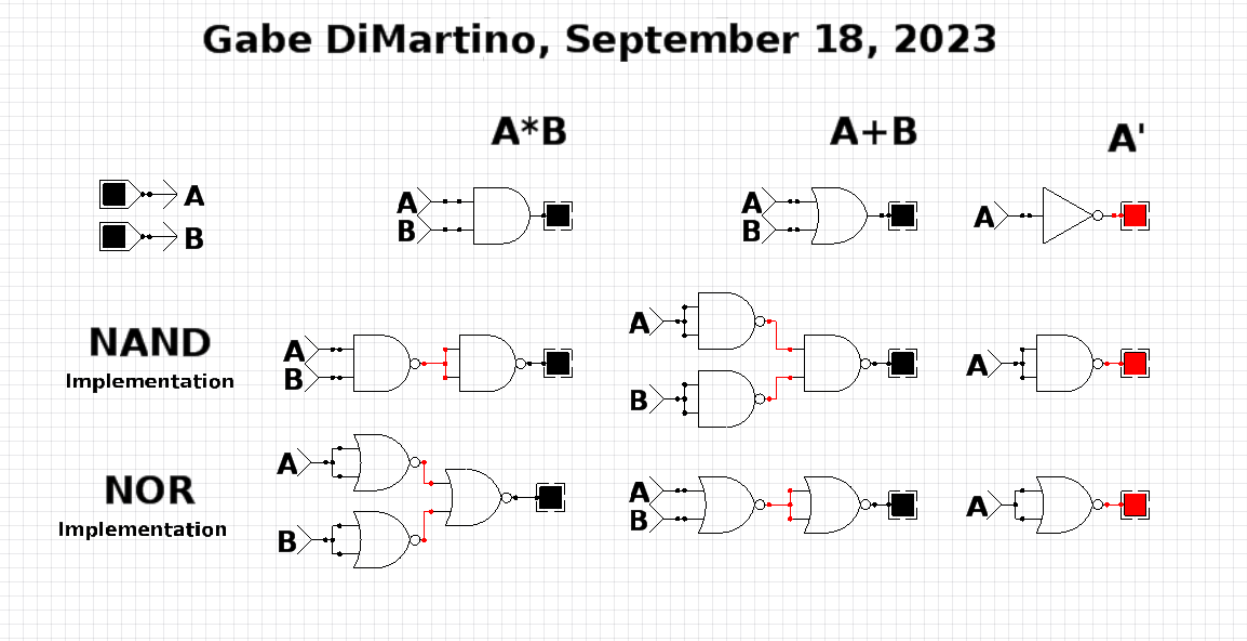
Part 1: Simple Logic using only NAND gates and NOR gates.

Prelab work: The prelab work for the operation of logical gates consisted of designing the Cedar file schematic for AND, OR, and NOT gates using only a single gate type. Specifically, the NAND and NOR gates.

Procedure: There were no procedure changes for this lab.

Part 1 Schematic



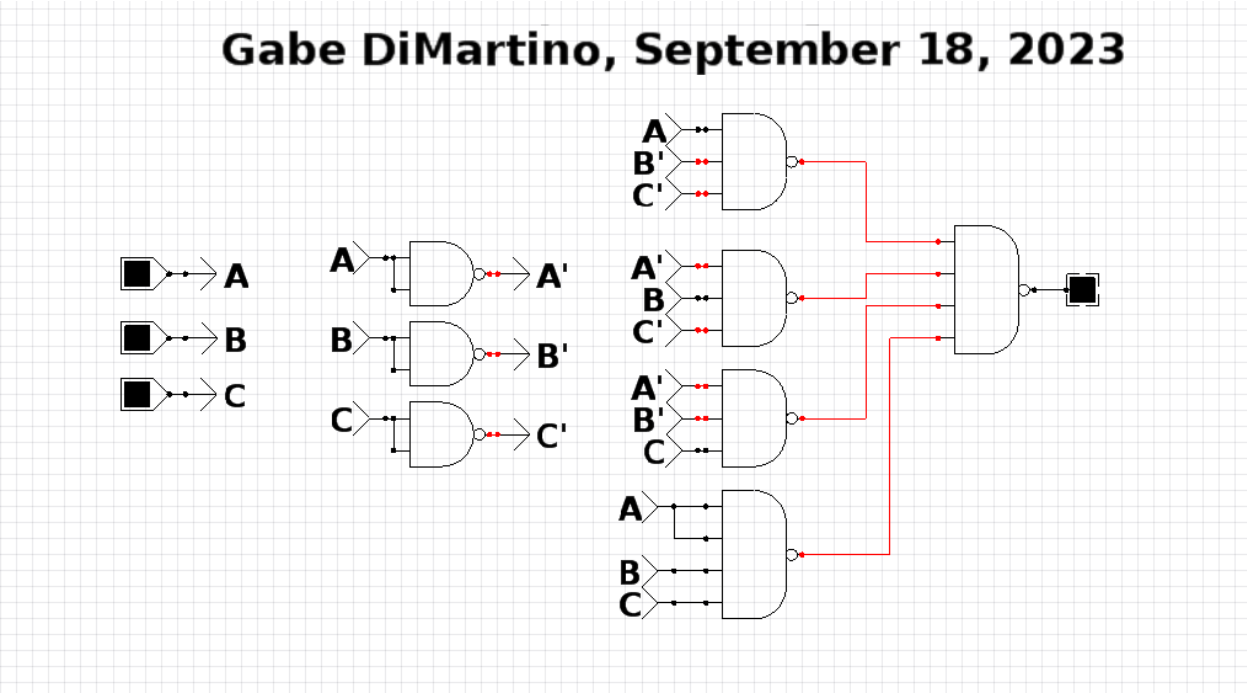
Discussion: Upon analyzing the gate types, it is possible to cut costs by using a single gate type instead of substituting multiple. For AND gates, the NAND is easier to replicate while the OR is easier to replicate with NOR gates.

Part 2: Complex Logic Using NAND Gates

Prelab work: The prelab work for the implementation of a three-way light switch using a single gate type. The Cedar Lab file demonstrates how it is possible to create a three-way light switch using a single gate, and by limiting the design to only 3 chips.

Procedure: There were no procedure changes for this lab.

Part 2 Schematic

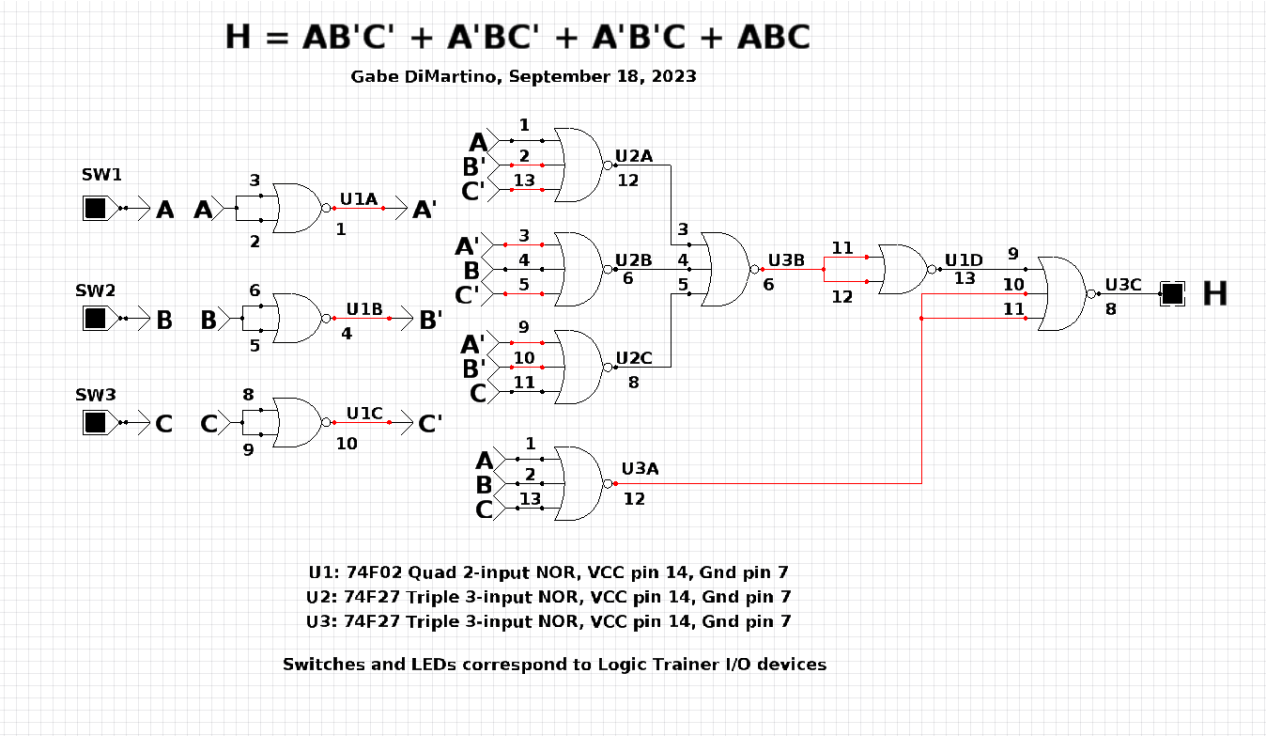


Discussion: Using only 3 chips added complexity to the three-way light switch design. On its own, using a single gate type would decrease cost and manufacturing complexity, however the design can be further optimized by limiting the amount of chips for the process. This is visualized above as the Cedar File utilizes several NAND gate types instead of a standard quad 2-input chip.

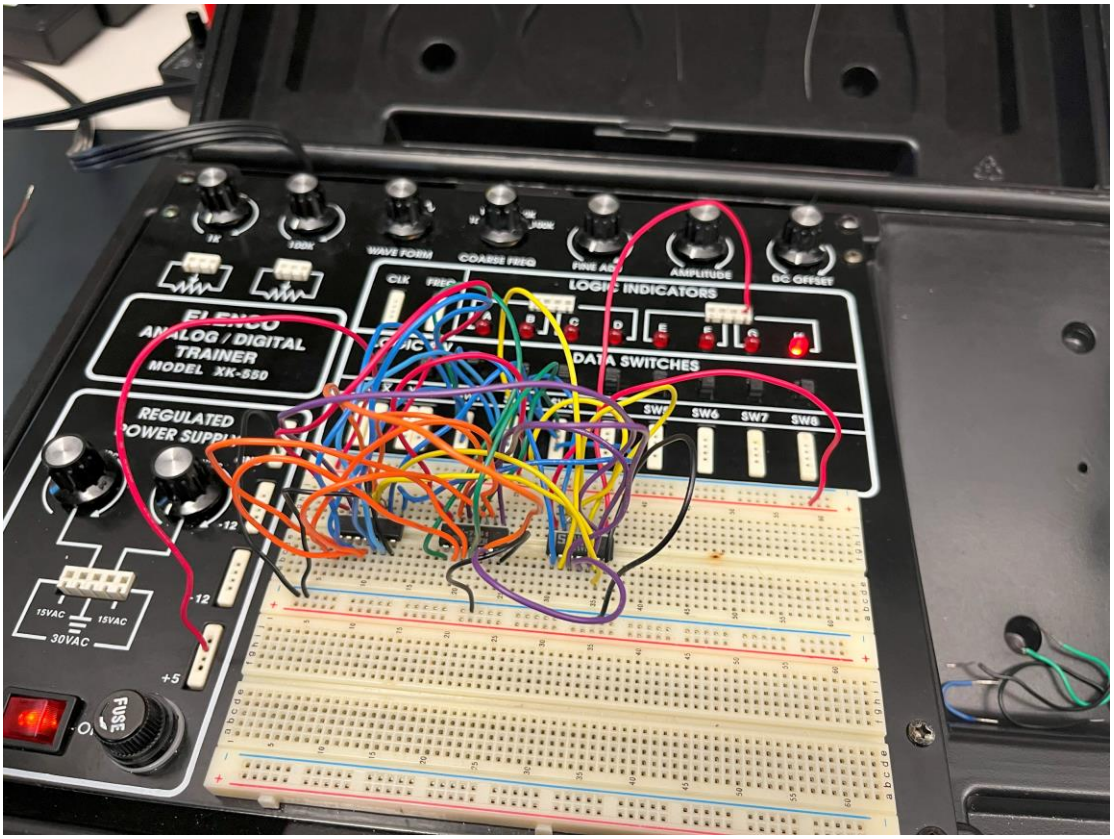
Part 3: Complex Logic Using NAND Gates

Prelab work: The prelab work for the implementation of a three-way light switch using a single gate type. The Cedar Lab file demonstrates how it is possible to create a three-way light switch using a single gate, and by limiting the design to only 3 chips.

Part 3 Schematic



Procedure: There were no procedure changes for this lab.



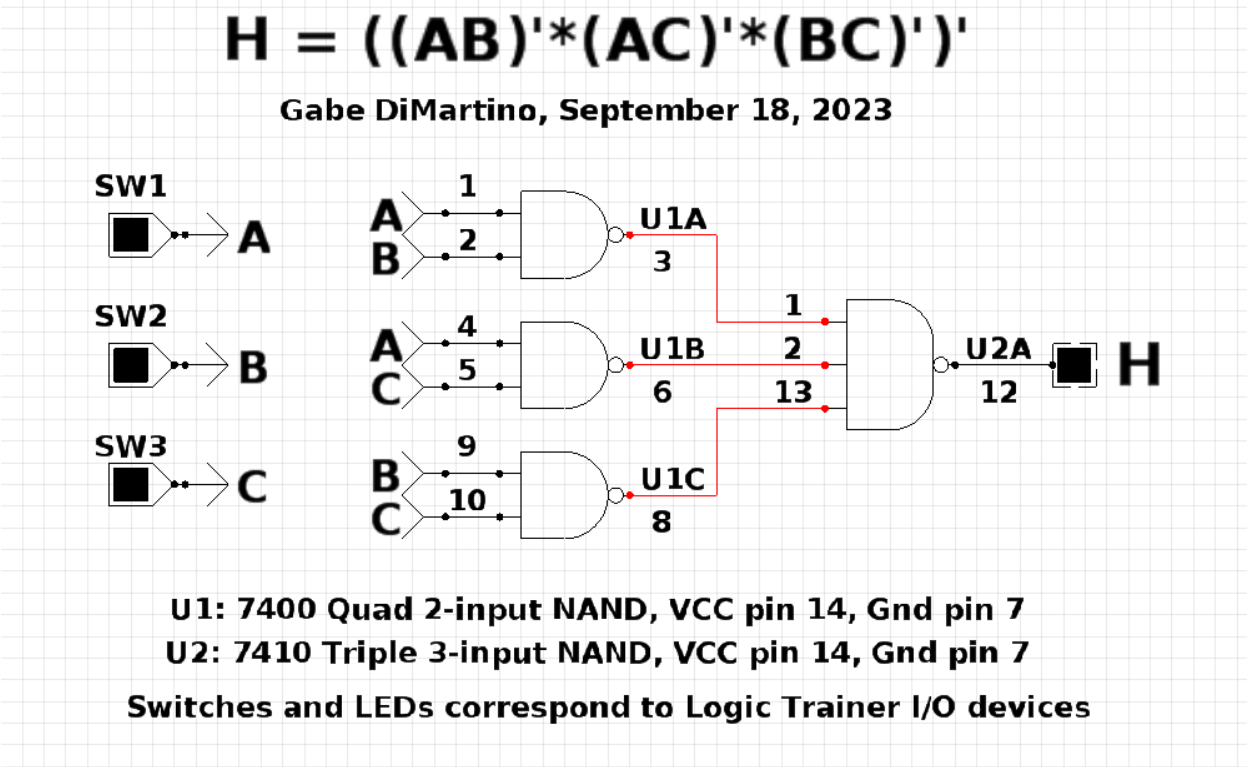
Results: Upon testing each of the chips, each gate outputs the predicted outcome. Following the configuration of the truth table in the prelab, each result was verified. We used the IC Tester and verified the ICs first before creating our circuit. The ICs used are the 7402 Quad 2-Input chips, and two 7427 Three 3-input chips. The image below shows the completed circuit with SW1: 1 SW2: 1 and SW3: 1. Under this configuration the predicted output is ON and that is confirmed by no activation on LED H

Discussion: Using only 3 chips added complexity to the three-way light switch design. On its own, using a single gate type would decrease cost and manufacturing complexity, however the design can be further optimized by limiting the amount of chips for the process. This is visualized above by the physical implementation and the Cedar File which utilizes both the 2-input and 3-input gate types.

Part 4: Majority Gate Using NAND

Prelab work: The prelab work for implementing a majority switch where the output LED would not illuminate unless most switches were activated. Adding complexity to the circuit, it could only be created using a single gate type NAND.

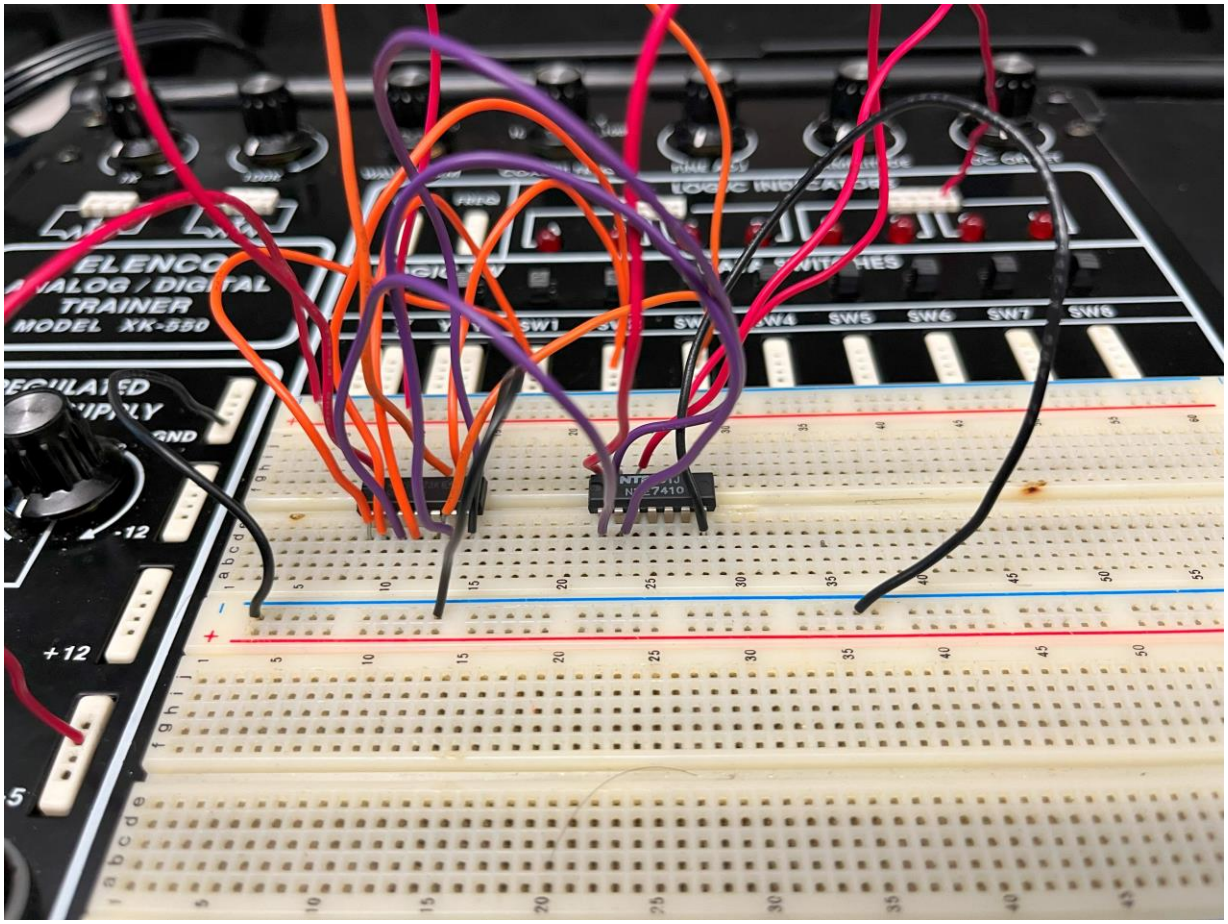
Part 4 Schematic



Part 4 Truth Table

SW1	SW2	SW3	H
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Procedure: There were no procedure changes for this lab.



Results: Upon testing each of the chips, each gate outputs the predicted outcome. Following the configuration of the truth table in the prelab, each result was verified. We used the IC Tester and verified the ICs first before creating our circuit. The ICs used are the 7400 Quad 2-Input chips, and two 7410 Three 3-input chips. The image below shows the completed circuit with SW1: 0 SW2: 0 and SW3: 0. Under this configuration the predicted output is OFF and that is confirmed by no activation on LED H

Discussion: This part gave another example of utilizing single gate type design for the creation of a circuit. Similarly, this helped with applying DeMorgan's theorem in a new situation.

Summary and Conclusion

This lab was extremely helpful for applying DeMorgan's theorem in several scenarios. Similarly, it was good practice for using single gate type design to minimize cost and manufacturing complexity. As I progress in lab, I will look back, and remember these core steps for making a circuit minimal, cost efficient, and simple to manufacture.