CPEN 230L: Introduction to Digital Logic Laboratory
Lab #1: Cedar Software & Logic Trainer
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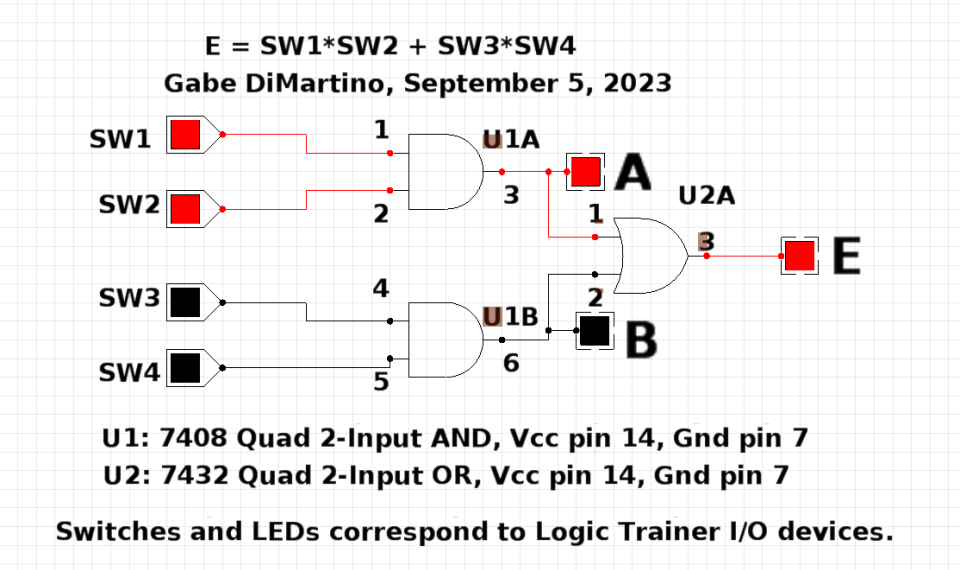
Part 1: Cedar Logic Test

Procedure Changes: During the lab, I found it easiest to modify the original AND/OR Ceder file instead of making the circuit from scratch. Similarly, the Microsoft snipping tool was easier to use compared to taking a full screenshot and re-sizing.

Results: The schematic diagram below visualizes the SOP circuit E=SW1.SW2+SW3.SW4. A and B respond to the AND gates activating, and the final E led responds when both an AND and an OR are activated.



The Ceder file was simple to create, using the template provided for the lab we were able to create a Sum of Products circuit with inputs SW1, SW2, SW3, and SW4. It was a little hard at first to add LEDs A and B to the circuit, but we figured it out by adding the connection from the AND gate to the OR gate then added the LED second. Designing this circuit in Ceder helped our process for the rest of the lab as we were able to easily translate this design into the Logic training in part two.

Part 2: Elenco Logic Trainer, IC Testers, and ICs.

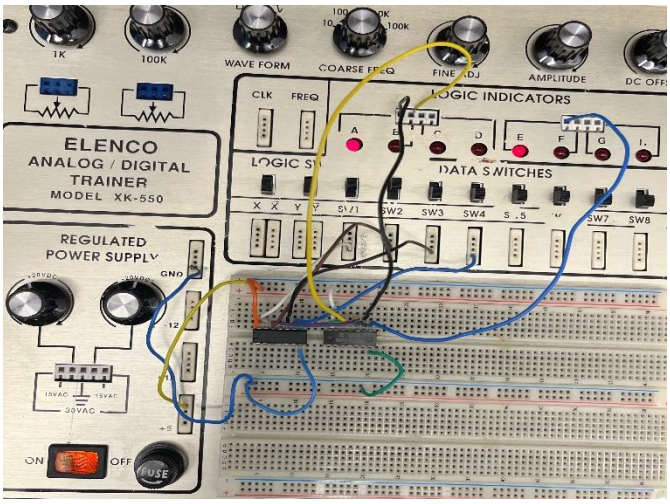
Procedure Changes: During the lab, we changed the inputs to the AND and Or Gates to 12-8. This was done for a more simplified design on our breadboard. Due to 2 people working on the breadboard at the same time, it was easier for us to work with the top row instead of the bottom.

Results: The truth table below visualizes the predicted outcome of the circuit and the tested outputs. Agreement on both demonstrates that our circuit works as intended with no failure.

SW1	SW2	SW3	SW4	A= SW1• SW2	B = SW3• SW4	E = (SW1• SW2) + (SW3• SW4)	✓
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	1	1	1
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	1	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	1	1
1	1	0	0	1	0	1	1
1	1	0	1	1	0	1	1
1	1	1	0	1	0	1	1
1	1	1	1	1	1	1	1

Creating the truth table first helped streamline the testing of our circuit as we were able to check our results to the configuration on the truth table.

The image below is the physical circuit created on the Logic Trainer to test the sum of products circuit. After testing the gate chips with the IC tester and providing power to the breadboard, all outcomes matched our predicted.



The image above visualizes our circuit used for the lab. We used the IC Tester and verified the ICs first before creating our circuit. The ICs used are the 7408 AND chip and the 7432 OR chip. Combined with the Logic Trainer to provide power and switches, the circuit demonstrated the properties of an AND and OR gate. In the image, SW1 and SW2 are activated showing that led A and led E are on as expected.

Summary and Conclusion

This lab was extremely helpful for demonstrating AND and OR gate chips as well as how to format and write a lab report. It was a great hands-on experience for the Ceder software and the Logic trainer to practice with simple circuits. Moving forward, I will look back on this lab for support as it has successfully laid the groundwork for future labs.