CPEN 230L: Introduction to Digital Logic Laboratory
Lab #4: System Design Review
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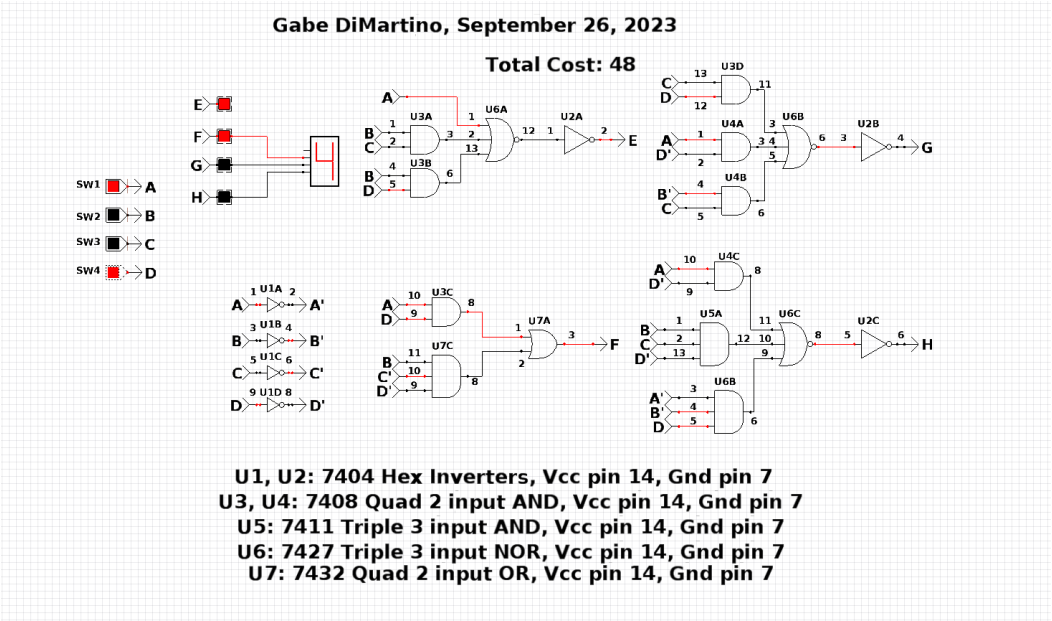
Part 1: BCD digit divided by 5.

Prelab work: The prelab work for the operation of logical circuit to divide an integer by 5. The schematic below only accounts for integers that represent 0-9 and throws out values that do not matter. Similarly, the equations used to create this circuit have been simplified to produce the minimal cost of 48.

SW1	SW2	SW3	SW4	E	F	G	H	✓
0	0	0	0	0	0	0	0	✓
0	0	0	1	0	0	0	1	✓
0	0	1	0	0	0	1	0	✓
0	0	1	1	0	0	1	1	✓
0	1	0	0	0	0	1	0	✓
0	1	0	1	1	0	0	0	✓
0	1	1	0	1	0	0	1	✓
0	1	1	1	1	0	1	0	✓
1	0	0	0	1	0	1	1	✓
1	0	0	1	1	1	0	0	✓



FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS11
Triple 3-Input AND Gate

General Description

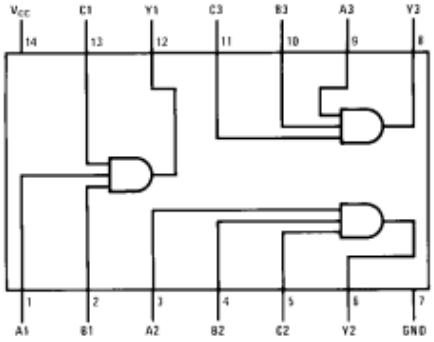
This device contains three independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS11M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS11N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



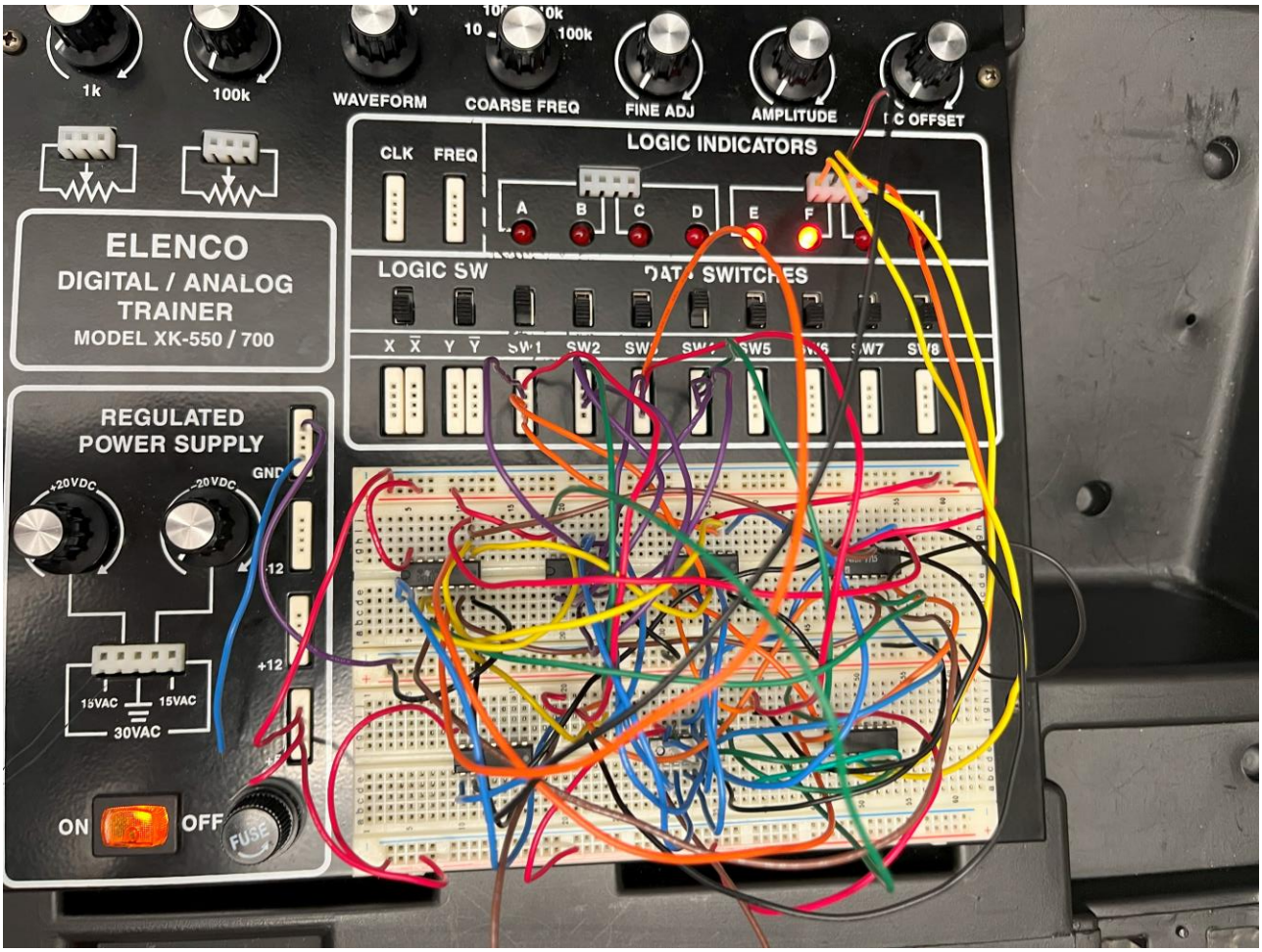
Function Table

Y = ABC

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level

Procedure: Initially, the schematic was created for a three way OR and AND gate. However, during the lab, the procedure was changed to account for the lack of a three way OR gate. Similarly, the specification sheet for the three way AND gate was acquired over the internet and used for the circuit.



Results: Upon testing each of the chips, each gate outputs the predicted outcome. Following the configuration of the truth table in the prelab, each result was verified. We used the IC Tester and verified the ICs first before creating our circuit. The ICs used are the 7404 Hex Inverters, 7408 Quad 2-Input AND Chips, 7411 Triple 3-Input chips, 7427 Triple 3-Input NOR chips, and finally a 7432 Quad 2-Input OR chip. Under this configuration the predicted output is a quotient of 1 with a remainder of 4 and that is confirmed by activation of the E and F LED.

Discussion: Balancing the cost of the circuit heavily influenced the complexity of the design. After revising the design twice during lab and assessing issues with the circuit prior to its completion, the logic circuit was finally completed with the expected outcomes. Similarly, despite its challenges, the cost maintained its minimal cost despite last-minute adjustments.

Summary and Conclusion

Upon analyzing this circuit, the balance between cost and chip effectiveness demonstrates a strong understanding of minimal cost design. Similarly, the complexity of the circuit allowed for

an opportunity to practice working on larger scale circuits, balancing cost, and producing only relevant outputs.