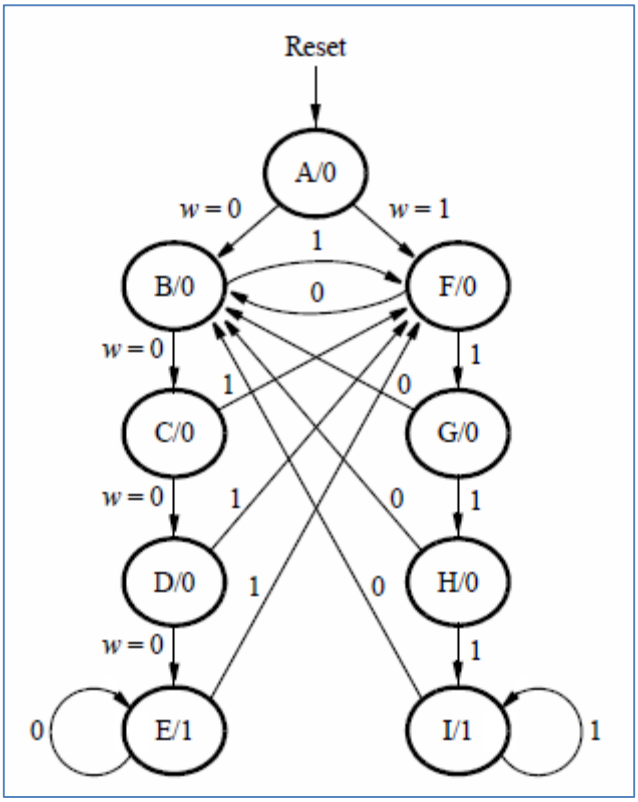
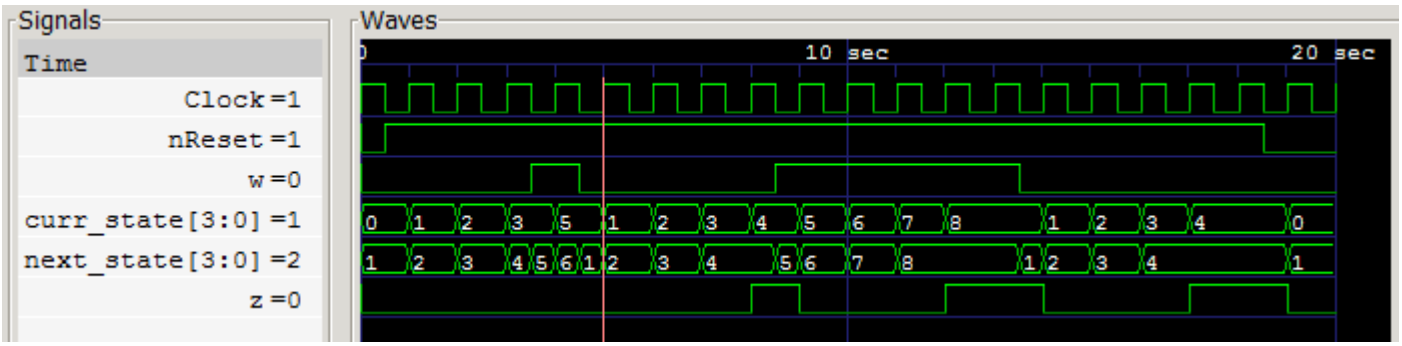
CPEN 230L: Introduction to Digital Logic Laboratory

Lab #11: Finite State Machines

Pre-Lab

- Background: Read the following textbook sections.
  - "Synchronous Sequential Circuits" and "Basic Design Steps", pages 331-333.
  - "State Diagram" and "State Table", pages 333-336, enough to understand Figures 6.3 and 6.4.
  - "Design of FSMs Using CAD Tools" and "Verilog Code for Moore-Type FSMs", pages 354-356. Understand in detail the Verilog code in **Figure 6.29 (page 356)** and the state machine it is implementing in **Figure 6.3 (page 335)**.
- You will implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z. When w = 1 or w = 0 for four consecutive positive clock edges the value of z is 1, otherwise z is 0. Overlapping sequences are allowed, so that if w = 1 for five consecutive positive clock edges the output z will be equal to 1 after both the fourth and fifth positive clock edges.





- The previous two images show the state diagram of the FSM and some test bench results. In the test bench, states A, B, C, D, E, F, G, H, I are represented by 0, 1, 2, 3, 4, 5, 6, 7, 8 respectively. Positive clock edges occur at t = 0, 1, 2, 3, 4… seconds. The marker is at t = 5.
    - At t = 4 what state transition occurs and why?
    - At t = 8 what state transition occurs and why?
    - At t = 12 what state transition occurs and why?
    - How can you tell from the waveforms that nReset is active-low and synchronous?
- Implement the FSM by completing provided file **seq4FSM.v**.
- **Simulate** the FSM by demonstrating that it behaves as shown in the waveform diagram above. Your ModelSim or GTKWave waveforms must be just as shown above -- 0 to 20 seconds, 1 clock per second, signals in the order shown, all signal transitions at the times shown, marker at 5 seconds.

During Lab

- **Synthesize** the FSM on the DE2-115 board using ~KEY0 as the Clock input, SW[1] as the w input, SW[0] as the active-low synchronous nReset input, LEDG0 as the z output, HEX1 to display current state (as A b C d E F 6 H I, not 0 through 8), and HEX0 to display next state. Debounce KEY0 with about 21 ms of debounce settling time before using it to clock the FSM.
- When your FSM is working on the DE2-115 board, demonstrate it to your instructor.