TEXAS INSTRUMENTS
UCC27624
SLUSE44A – APRIL 2020 – REVISED AUGUST 2021

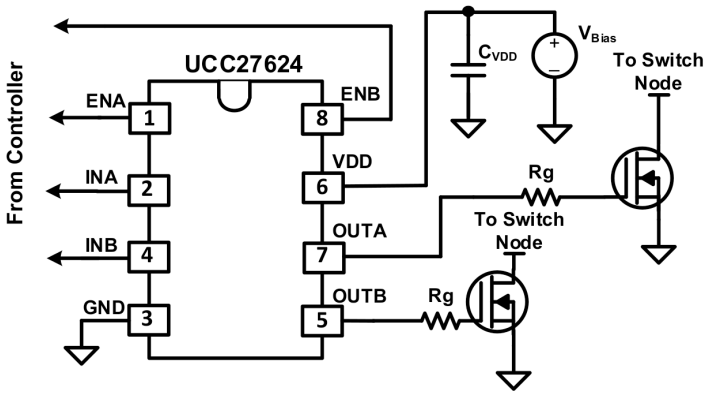
UCC27624 Dual Channel 30-V, 5-A High-Speed Low-Side Gate Driver

1 Features

- 30-V absolute maximum bias voltage
- Two independent gate-drive channels
- 5-A peak source and sink-drive current for each channel
- Independent-enable function for each output
- Hysteretic-logic thresholds for high noise immunity
- Input and enable pins capable of withstanding up to –10 V
- VDD independent input thresholds (TTL compatible)
- Wide VDD operating range from 4.5 V to 26 V
- Fast propagation delays (17-ns Typical)
- Fast rise and fall times (3.5-ns and 6-ns typical)
- 1-ns typical delay matching between 2-channels
- Two channels can be paralleled for higher drive current
- SOIC8 and VSSOP8 PowerPAD™ package options
- Operating junction temperature range of –40°C to 150°C

2 Applications

- Switch-mode power supplies
- Power factor correction (PFC) circuits
- Motor drives
- Solar power supplies
- Line drivers



Simplified Application Diagram

3 Description

The UCC27624 device family comprises dual-channel, high-speed, and low-side gate drivers that effectively drive MOSFET, IGBT, SiC, and GaN power switches. UCC27624 has a typical peak drive strength of 5 A, which helps reduce rise and fall time of the power switches. This results in low switching losses in the power train and therefore enables high efficiency. A small propagation delay of the UCC27624 helps reduce the dead-time and improve pulse width utilization. This further improves the power stage efficiency. Small propagation delay also helps improve control loop response time and may improve transient performance of the system.

UCC27624 can handle –10 V at its inputs. This negative input voltage capability helps to improve system robustness where moderate ground bouncing may exist in the system. The inputs are independent of supply voltage and can be connected to most controller outputs. This allows maximum control flexibility. An independent enable signal allows the power stage to be controlled independently of main control logic; that is, the gate driver can quickly shut-off the power stage in an event where there is a fault in the system that requires the power train to be turned-off immediately. Many high-frequency switching power supplies exhibit high-frequency noise at the gate of the power device, which can get injected into the output pin on the gate driver and can cause the driver to malfunction. Due to the UCC2762x transient reverse current and reverse voltage capability, the driver performs well in such conditions and systems.

The UCC27624 family of devices has an undervoltage lockout (UVLO) feature so that when there is not enough bias voltage to fully enhance the power device, the gate driver output is held low by the strong internal pull down MOSFET. This active pull-down feature further improves system robustness.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
UCC27624	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

DATE	REVISION	NOTES
August 2021	A	Advance Information

5 Pin Configuration and Functions

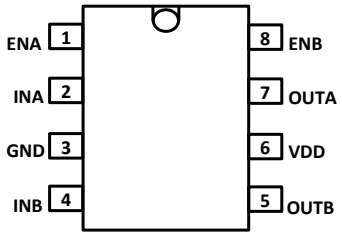

Figure 5-1. D Package 8-Pin SOIC Top View

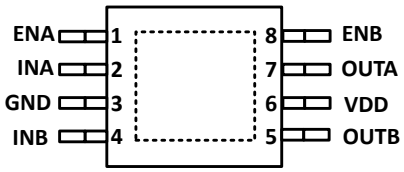

Figure 5-2. DGN Package 8-Pin VSSOP Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DGN	D		
ENA	1	1	I	Enable input for channel A. ENA is biased LOW to disable the channel A output regardless of the INA state. ENA is biased HIGH to enable the Channel A output. If ENA is left floating the channel is enabled; hence, the pin-to-pin compatibility with the UCC2732X N/C pin.
ENB	8	8	I	Enable input for Channel B. ENB is biased LOW to disable the Channel B output regardless of the INB state. ENB is biased HIGH to enable Channel B output. If ENB is left floating, then the output is enabled; hence, the pin-to-pin compatibility with the UCC2732x N/C pin.
GND	3	3	—	Ground: All signals are referenced to this pin.
INA	2	2	I	Input to Channel A. INA is the non-inverting input in the UCC27624 device. OUTA is held LOW if INA is unbiased or floating. Connect this pin to GND if unused.
INB	4	4	I	Input to Channel B. INB is the non-inverting input in the UCC27624 device. OUTB is held LOW if INB is unbiased or floating. Connect this pin to GND if unused.
OUTA	7	7	O	Channel A Output. Place the switching device such as MOSFET as close as possible to this pin and connect this pin to one end of the external gate resistor if needed.
OUTB	5	5	O	Channel B Output. Place the switching device such as MOSFET as close as possible to this pin and connect this pin to one end of the external gate resistor if needed.
VDD	6	6	I	Bias supply input. Connect positive node of voltage source to this pin through an impedance for high common mode noise rejection. Bypass this pin with ceramic capacitor, generally 1 µF, which is referenced to GND pin of this device. Also, place a 100-nF ceramic surface-mount capacitor in parallel with the bypass capacitor and close to the VDD and GND pins.
	Thermal Pad	—	—	Connect to GND through large copper plane.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
Supply voltage, VDD		–0.3	30	V
Output Voltage, OUTA, OUTB	DC	–0.3	VDD +0.3	V
	200ns Pulse	–3	VDD +3	V
Input Voltage INA, INB, ENA, ENB		–10	30	V
Operating junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See *Section 6.4* of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range. All voltages are with reference to GND (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5	12	26	V
Input voltage, INA, INB, ENA, ENB	–2(1)		26	V
Output Voltage, OUTA, OUTB	0		VDD	V
Operating junction temperature	–40		150	°C

(1) This value will be -10V in production release

6.4 Thermal Information

THERMAL METRIC		UCC27624		UNIT
		DGN	D	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	126.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.8	67.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.3	69.9	
ψ_{JT}	Junction-to-top characterization parameter	2.6	19.2	
ψ_{JB}	Junction-to-board characterization parameter	22.3	69.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	n/a	

6.5 Electrical Characteristics

Unless otherwise noted, VDD = 12 V, $T_A = T_J$ = –40°C to 150°C, 1-µF capacitor from VDD to GND, No load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{VDDq}	VDD quiescent supply current	V_{INx} = 3.3V, VDD = 3.4 V, ENx = VDD		300	450	µA
I_{VDD}	VDD static supply current	V_{INx} = 3.3V, ENx = VDD		0.6	1.2	mA
I_{VDD}	VDD static supply current	V_{INx} = 0 V, ENx = VDD		0.5	1.0	mA
I_{VDDO}	VDD operating current	f_{SW} = 1000 kHz, ENx = VDD, V_{INx} = 0 - 3.3 V PWM		3.2	3.8	mA
I_{DIS}	VDD disable current	V_{INx} = 3.3 V, ENx = 0 V		0.8	1.1	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{VDD_ON}	VDD UVLO Rising Threshold		3.8	4.1	4.4	V
V_{VDD_OFF}	VDD UVLO Falling Threshold		3.5	3.8	4.1	V
V_{VDD_HYS}	VDD UVLO Hysteresis			0.3		V
INPUT (INA, INB)						
V_{INx_H}	Input signal high threshold	Output High, ENx = HIGH	1.8	2	2.3	V
V_{INx_L}	Input signal low threshold	Output Low, ENx=HIGH	0.8	1	1.2	V
V_{INx_HYS}	Input signal hysteresis			1		V
R_{INx}	INx pin Pull down resistor	INx = 3.3V		120		kΩ
ENABLE (ENA, ENB)						
V_{ENx_H}	Enable signal high threshold	Output High, INx=HIGH	1.8	2	2.3	V
V_{ENx_L}	Enable signal low threshold	Output Low, INx=HIGH	0.8	1	1.2	V
V_{ENx_HYS}	Enable signal hysteresis			1		V
R_{ENx}	EN pin pull up resistance	ENx = 0 V		200		kΩ
OUTPUTS (OUTA, OUTB)						
I_{SRC} (1)	Peak output source current	VDD = 12V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		5		A
I_{SNK} (1)	Peak output sink current	VDD = 12V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		-5		A
R_{OH}	Pull-up resistance	I_{OUT} = –50 mA		5	8.5	Ω
R_{OL}	Pull-down resistance	I_{OUT} = 50 mA		0.6	1.1	Ω

(1) Not production tested.

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6.6 Switching Characteristics

Unless otherwise noted, VDD = V_{EN} = 12 V, T_A = T_J = –40°C to 150°C, 1-µF capacitor from VDD to GND, No load on the output. Typical condition specifications are at 25°C (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Rx}	Rise time	C_{LOAD} = 1.8 nF, 20% to 80%, Vin = 0 to 3.3V		3.5	6.5	ns
t_{Fx}	Fall time	C_{LOAD} = 1.8 nF, 90% to 10%, Vin = 0 to 3.3V		6	10	ns
t_{D1x}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, V_{INx_H} of the input rise to 10% of output rise, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle, T_J = 125°C		17	25	ns
t_{D2x}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, V_{INx_L} of the input fall to 90% of output fall, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle, T_J = 125°C		17	25	ns
t_{D3x}	Enable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_H} of the enable rise to 10% of output rise, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle, T_J = 125°C		17	25	ns
t_{D4x}	Disable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_L} of the enable fall to 90% of output fall, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle, T_J = 125°C		17	25	ns
t_M	Delay matching between 2 channels	C_{LOAD} = 1.8 nF, Vin=0 - 3.3V, Fsw=500kHz, 50% duty cycle, INA = INB, $\lvert t_{RA} - t_{RB} \rvert$, $\lvert t_{FA} - t_{FB} \rvert$			2	ns
t_{PWmin}	Minimum input pulse width	C_L = 1.8nF, Vin=0 - 3.3V, Fsw=500kHz, Vo > 1.5V		10	15	ns

(1) Switching parameters are not tested in production.

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6.7 Timing Diagrams

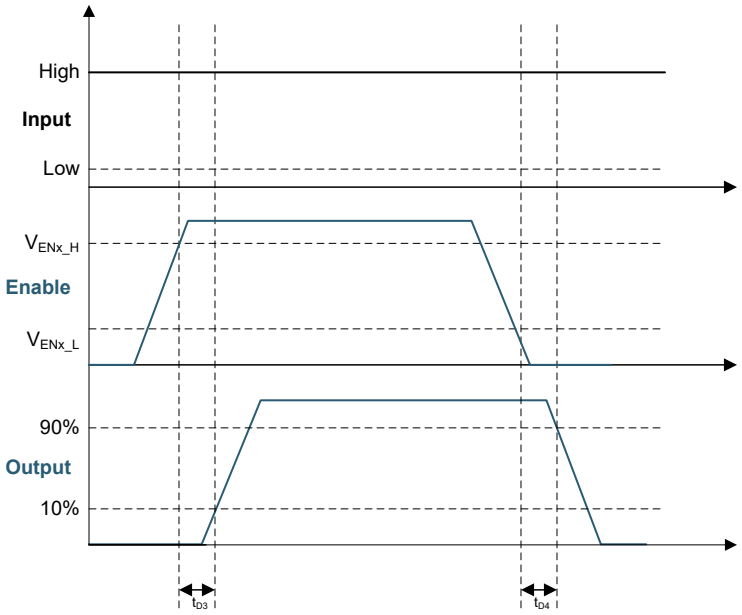

Figure 6-1. Enable Function

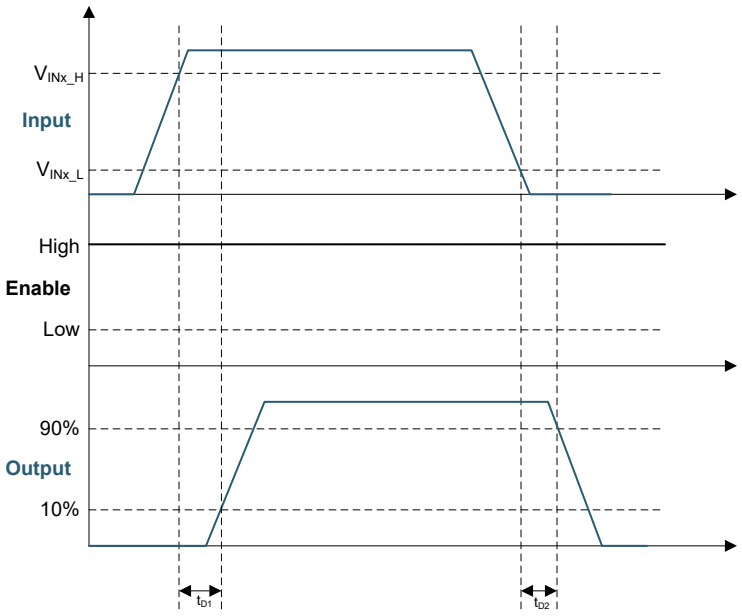

Figure 6-2. Input-Output Operation

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6.8 Typical Characteristics

Unless otherwise specified, VDD=12 V, INx=3.3 V, ENx=3.3 V, no load

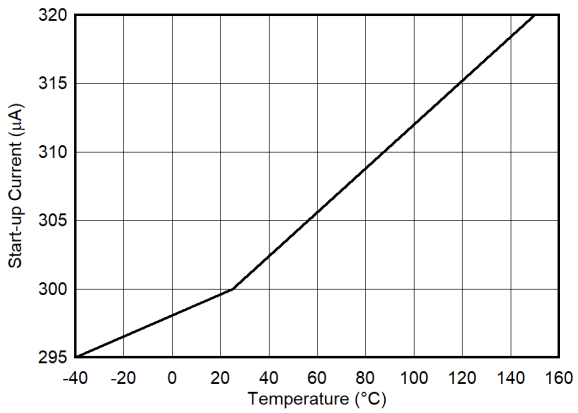


Figure 6-3. Start-Up/Quiescent Current

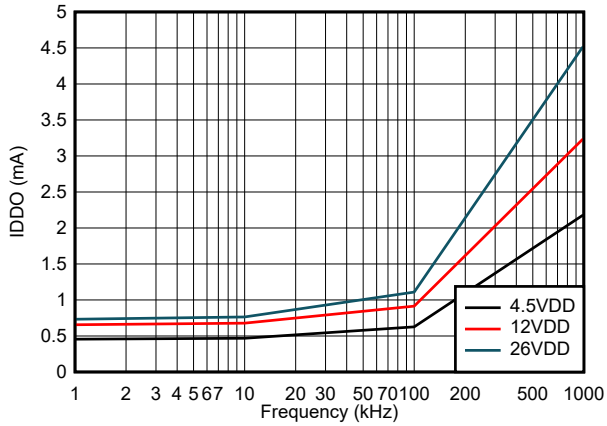


Figure 6-4. Operating Supply Current (Both Outputs Switching)

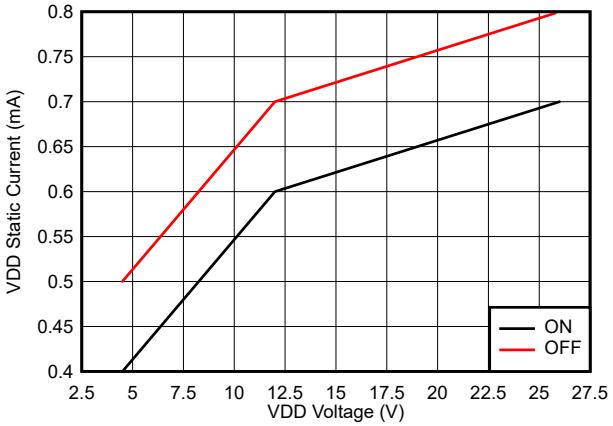


Figure 6-5. Static Supply Current (Outputs In DC On/Off Condition)

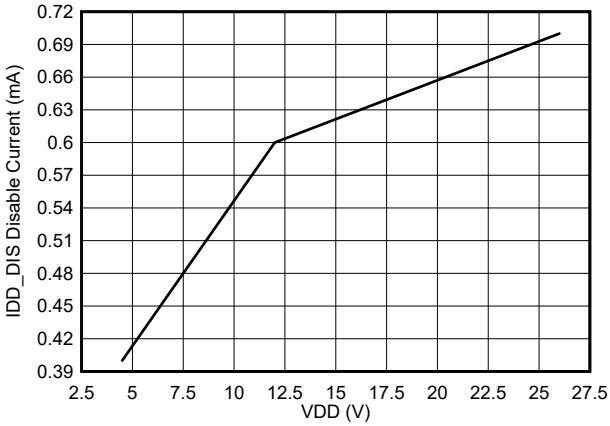


Figure 6-6. Disable Current (EN = 0V)

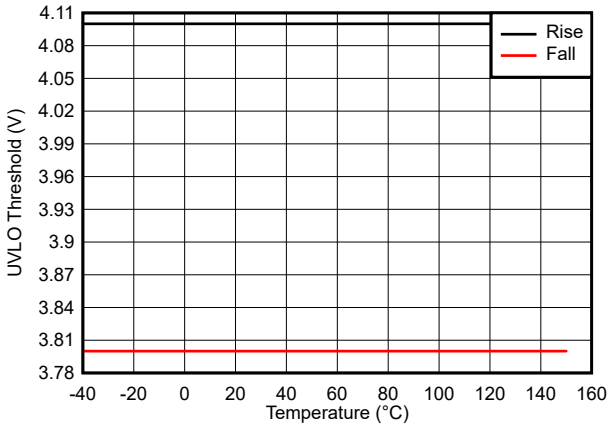


Figure 6-7. VDD UVLO Threshold

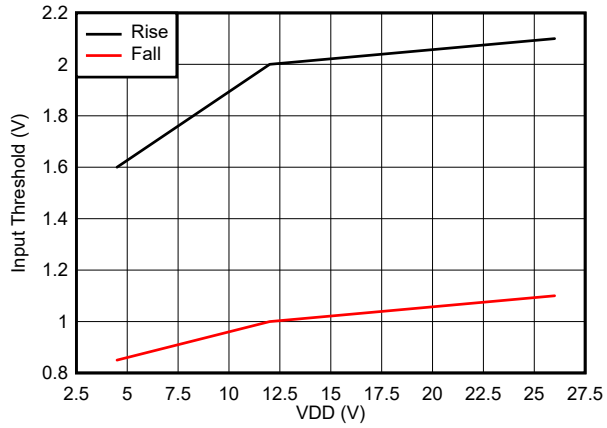


Figure 6-8. Input Thresholds

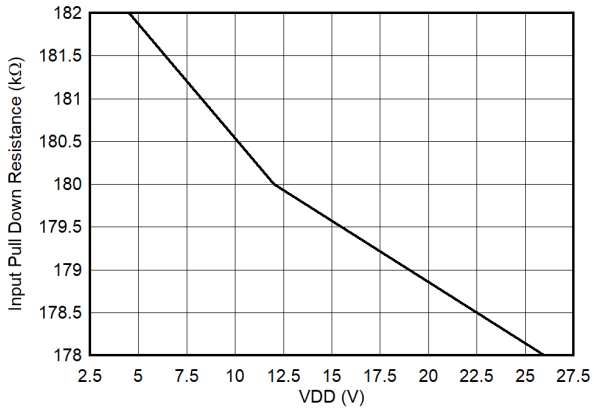


Figure 6-9. Input Pull-down Resistance

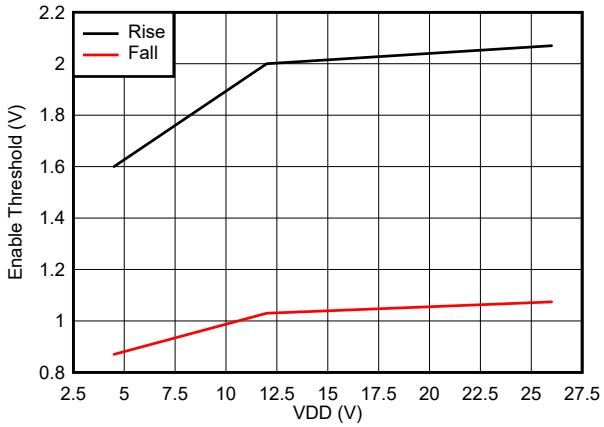


Figure 6-10. Enable Threshold

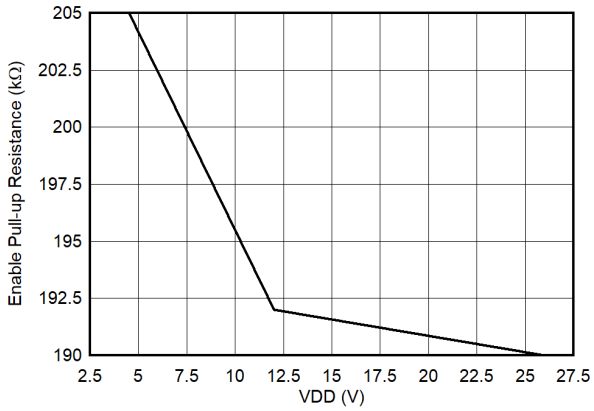


Figure 6-11. Enable Pull-up Resistance

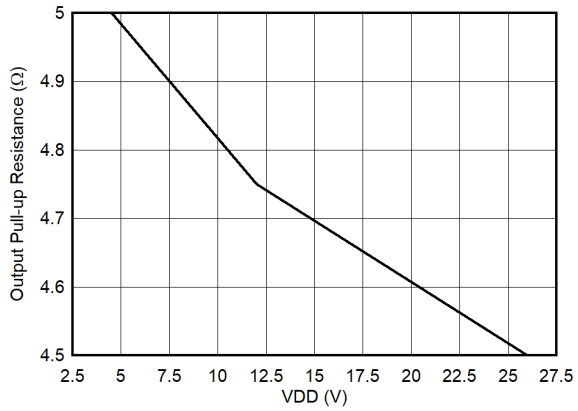


Figure 6-12. Output pull-up Resistance

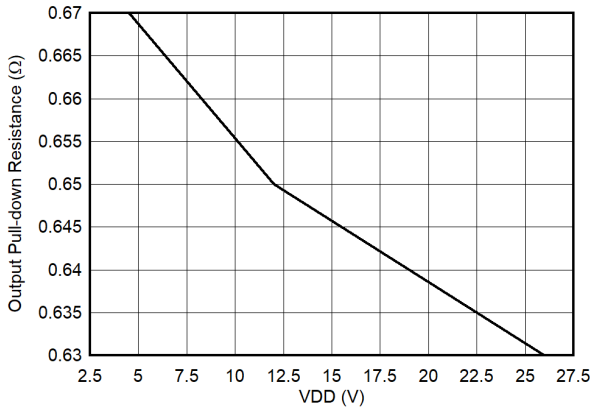
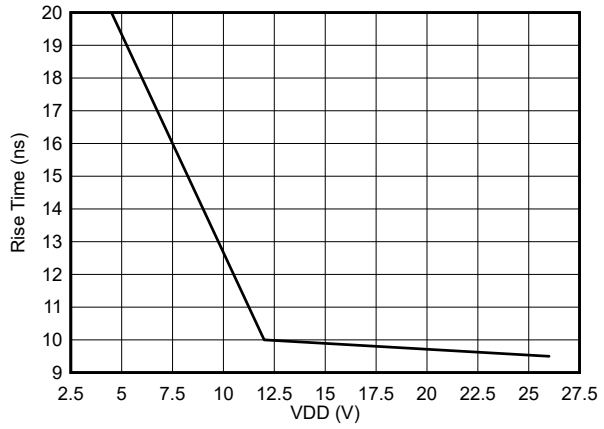


Figure 6-13. Output Pull-down Resistance



C_{LOAD} = 1.8 nF

Figure 6-14. Output Rise Time vs VDD

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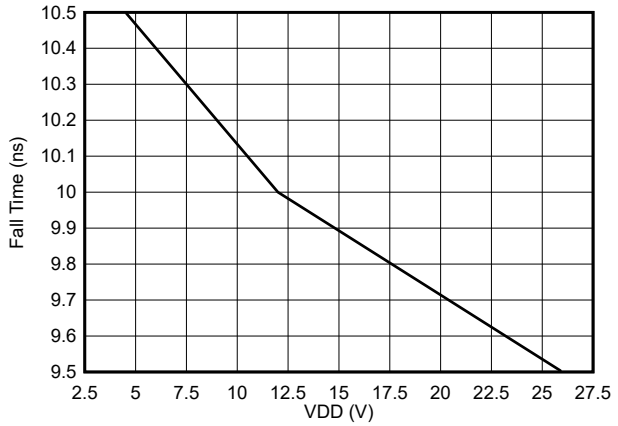
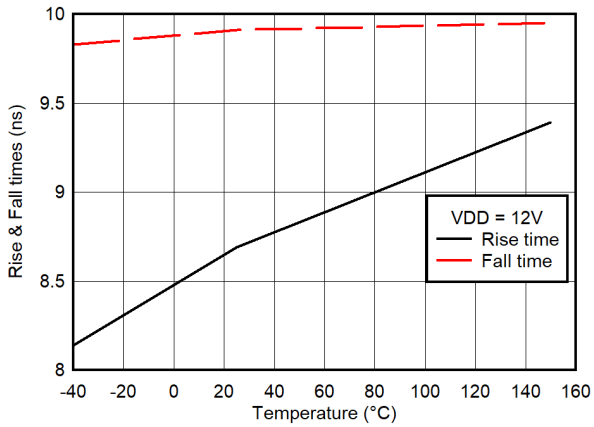


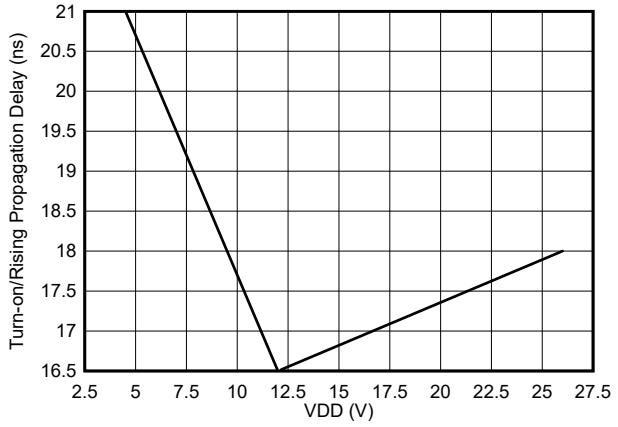
C_{LOAD} = 1.8 nF

Figure 6-15. Output Fall Time vs VDD



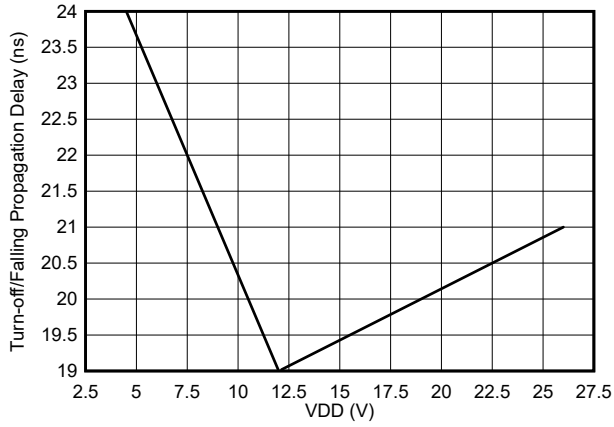
C_{LOAD} = 1.8 nF

Figure 6-16. Output Rise & Fall Time vs Temperature



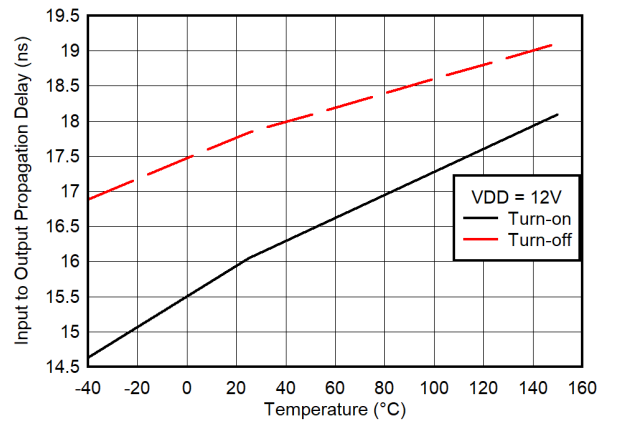
C_{LOAD} = 1.8 nF

Figure 6-17. Input to Output Rising (Turn-On) Propagation Delay vs VDD



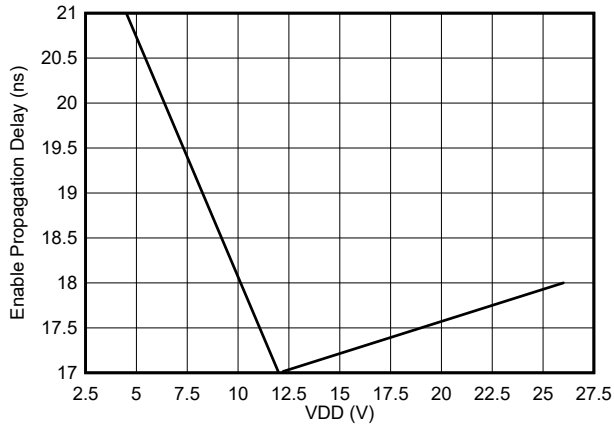
C_{LOAD} = 1.8 nF

Figure 6-18. Input to Output Falling (Turn-Off) Propagation Delay vs VDD



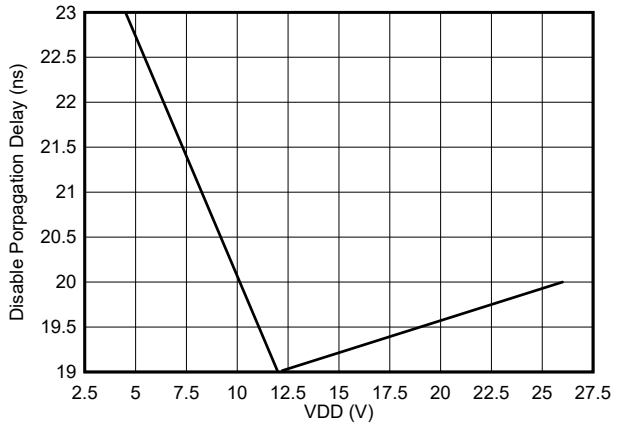
C_{LOAD} = 1.8 nF

Figure 6-19. Input Propagation Delay vs Temperature



C_{LOAD} = 1.8 nF

Figure 6-20. Enable to Output Rising Propagation Delay



C_{LOAD} = 1.8 nF

Figure 6-21. Enable to Output Falling Propagation Delay

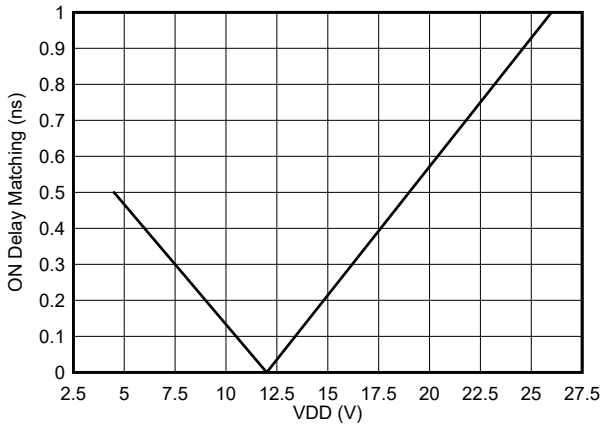


Figure 6-22. Turn-on/Rising Delay Matching

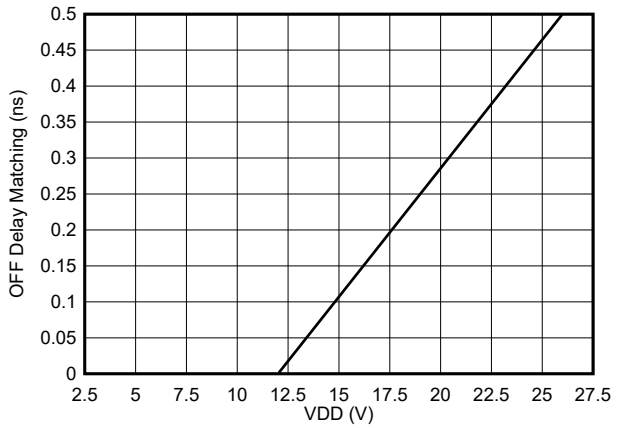


Figure 6-23. Turn-off/Falling Delay Matching

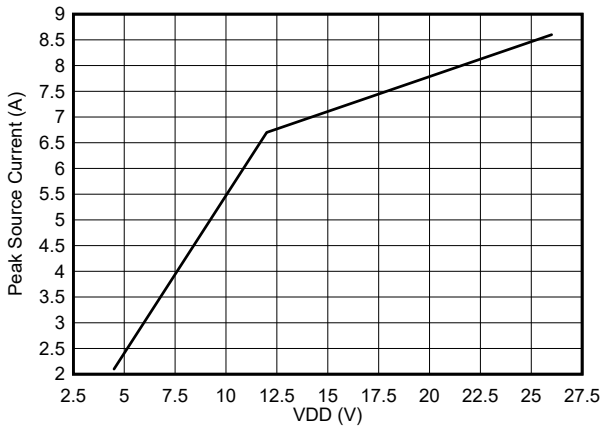


Figure 6-24. Peak Source Current vs VDD

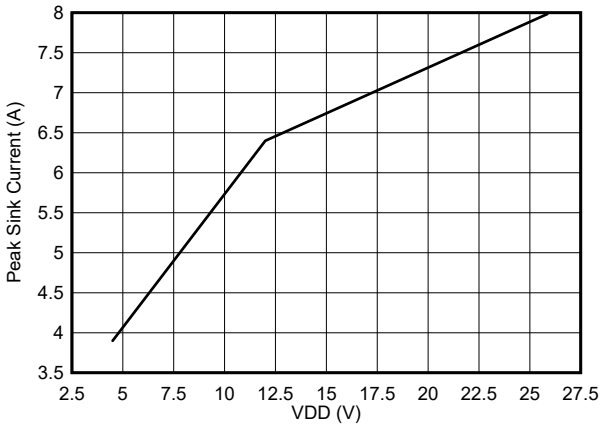


Figure 6-25. Peak Sink Current vs VDD

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7 Detailed Description

7.1 Overview

The UCC27624 device represents Texas Instruments latest generation of dual-channel, low-side, high-speed, gate-driver devices featuring a 5-A source and sink current capability, fast switching characteristics, and a host of other features listed in table below, all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 7-1. UCC27624 Features and Benefits

FEATURE	BENEFIT
17-ns (typ) propagation delay	Extremely low-pulse transmission distortion
1-ns (typ) delay matching between channels	Ease of paralleling outputs for higher (2 times) current capability, ease of driving parallel-power switches
Expanded VDD Operating range of 4.5 to 26 V	Flexibility in system design. Covers wide range of power switches
Expanded operating temperature range of –40 °C to +150 °C	Flexibility in system design. System robustness improvement
VDD UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down.
Outputs held Low when input pins (INx) in floating condition	Protection feature, especially useful in passing abnormal condition tests during safety certification
Outputs enable when enable pins (ENx) in floating condition	Pin-to-pin compatibility with the legacy devices from Texas Instruments in designs where Pin 1 and Pin 8 are in floating condition
Input and enable threshold with wide hysteresis	Enhanced noise immunity while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
Inputs independent of VDD	System simplification, especially related to auxiliary bias supply architecture
Ability to handle –10 V (max) at input pins	Increased robustness in noisy environments

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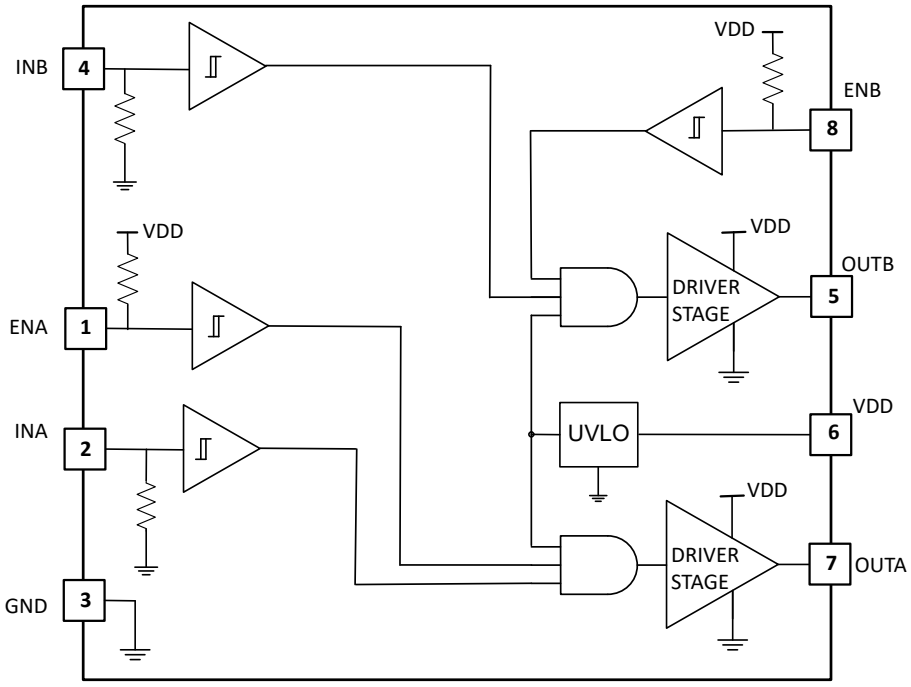
7.2 Functional Block Diagram



Typical

ENx pull-up resistance is 200 kΩ and INx pull-down resistance is 120 kΩ.

7.3 Feature Description

7.3.1 Operating Supply Current

The UCC27624 device features low quiescent I_{DD} currents. The typical operating-supply current in UVLO state and fully-on state (under static and switching conditions) are summarized in the Electrical Characteristics table. The I_{DD} current, when the device is fully on and outputs are in a static state (DC high or DC low), represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current because of switching, and any current related to pullup resistors on the enable pins. Knowing the operating switching frequency (f_{SW}) and the MOSFET gate charge (Q_G) at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

Typical Characteristics provides a complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages. The linear variation and close correlation with the theoretical value of the average I_{OUT} indicate a negligible shoot-through inside the gate-driver device, displaying its high-speed characteristics.

7.3.2 Input Stage

The input pins of the UCC27624 gate-driver device are based on a TTL compatible input-threshold logic that is independent of the VDD supply voltage. With a high threshold of 2 V and a low threshold of 1 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis (1 V typical) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. UCC27624 devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Typical Characteristics graphs). The very low input capacitance on these pins reduces loading and increases switching speed.

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The UCC27624 device features an important protection feature that holds the output of a channel low when the respective input pin is in a floating condition. This is achieved using pulldown resistors to the ground on all of the non-inverting input pins (INA, INB), as shown in the device block diagram.

The input pins can handle wide range of slew rate. In most power supply applications, the gate driver is either driven by the output of a digital controller or logic gates. Therefore, in most applications the input signal slew rate is fast and is no concern for the UCC27624 family of devices. While the wide hysteresis offered in UCC27624 definitely alleviates the concern of chattering compared to many other drivers that have very small hysteresis at the input. If limiting the rise or fall times to the power device is the primary goal, then an external gate resistor is highly recommended between the output of the driver and the gate of the switching power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself. Input pins of UCC27624 are capable of handling –10 V. This improves the system robustness in noisy (electrical) applications. This also allows the driver to directly connected to the output of the gate drive transformer without the use of rectifying diodes, which saves board space and BOM cost.

7.3.3 Enable Function

The enable function is an extremely beneficial feature in gate-driver devices, especially for certain applications such as synchronous rectification where the driver outputs are disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27624 device is equipped with independent enable pins (ENx) for exclusive control of each driver-channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus, when ENx pins are driven high, the drivers are enabled and when ENx pins are driven low, the driver outputs are disabled. Similar to the input pins, the enable pins are also based on a TTL compatible threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V or 5-V controllers. The UCC27624 devices also feature tight control of the enable-function threshold-voltage levels which eases system design considerations and ensures stable operation across temperature. The ENx pins are internally pulled up to VDD using pull-up resistors, as a result of which the outputs of the device are enabled in the default state. Hence even if the ENx pins are left floating the driver output is enabled. Essentially, this floating allows the UCC27624 device to be pin-to-pin compatible with TI's previous generation of drivers (UCC27324, UCC27424, UCC27524), where Pin 1 and Pin 8 are either ENx or N/C pins. If the channel A and channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB must be connected and driven together. The ENx pins of the UCC27624 are capable of handling -10 V, which improves system robustness in noisy (electrical) applications.

7.3.4 Output Stage

The UCC27624 device output stage features a unique architecture on the pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn-on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turn-on. This is accomplished by briefly turning-on the N-Channel MOSFET during a narrow instance when the output is changing state from Low to High.

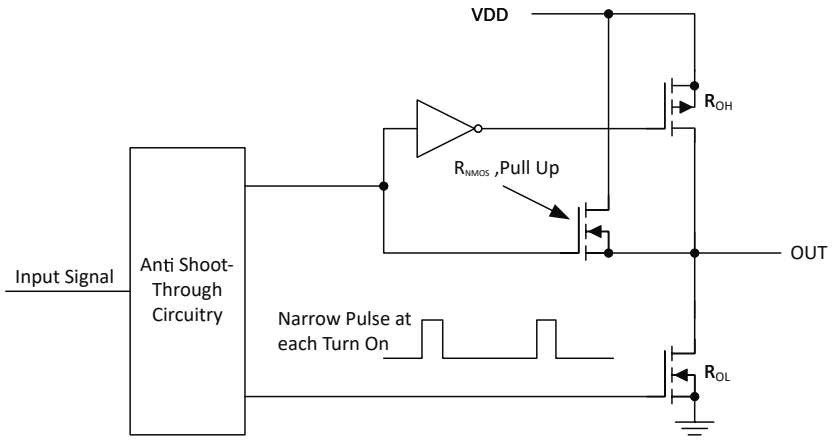

Figure 7-1. UCC27624 Gate Driver Output Structure

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Note that effective resistance of the UCC27624 pull-up stage during the turnon instance is much lower than what is represented by R_{OH} parameter.

The pulldown structure in the UCC27624 device is simply comprised of a N-Channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down stage in the device.

Each output stage in the UCC27624 device is capable of supplying 5-A peak source and 5-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to transient overshoots and undershoots. The outputs of these drivers are designed to withstand 5A of peak reverse current transients without damage to the device.

The UCC27624 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This is possible because of the extremely low dropout offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage. All of these allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure proper reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

7.3.5 Low Propagation Delays and Tightly Matched Outputs

The UCC27624 driver device features very small, 17-ns (typical) propagation delay between input and output, which offers the lowest level of pulse width distortion for high frequency switching applications. For example, in synchronous rectifier applications, the SR MOSFETs are driven with very low distortion when a single driver device is used to drive both the SR MOSFETs. Further, the driver devices also feature an extremely accurate, 1-ns (typical) matched internal-propagation delays between the two channels which is beneficial for applications requiring dual gate drives with critical timing. For example, in a PFC application, a pair of paralleled MOSFETs can be driven independently using each output channel, with the inputs of both channels are driven by a common control signal from the PFC controller. In this case the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion with the minimum of turn-on delay difference. Yet another benefit of the tight matching between the two channels is that the two channels can be connected together to effectively double the drive current capability. That is, A and B channels may be combined into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together. Then, a single signal controls the paralleled power devices.

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7.4 Device Functional Modes

Table 7-2. Device Logic Table

ENA	ENB	INA	INB	UCC27624	
				OUTA	OUTB
H	H	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H
L	L	Any	Any	L	L
Any	Any	x(1)	x(1)	L	L
x(1)	x(1)	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H

(1) Floating condition.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to achieve fast switching of power devices and reduce associated switching-power losses, a powerful gate-driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning ON a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn ON the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate-driver devices effectively combine both the level-shifting and buffer-drive functions. Gate-driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller.

Finally, emerging wide band-gap power-device technologies such as SiC MOSFETs and GaN switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include wide operating voltage range (5 V to 20 V), low propagation delays, good delay matching, and availability in compact, low-inductance packages with good thermal capability. In summary, gate-driver devices are an extremely important component in switching power combining benefits of high-performance, low-cost, low component-count, board-space reduction, and simplified system design.

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8.2 Typical Application

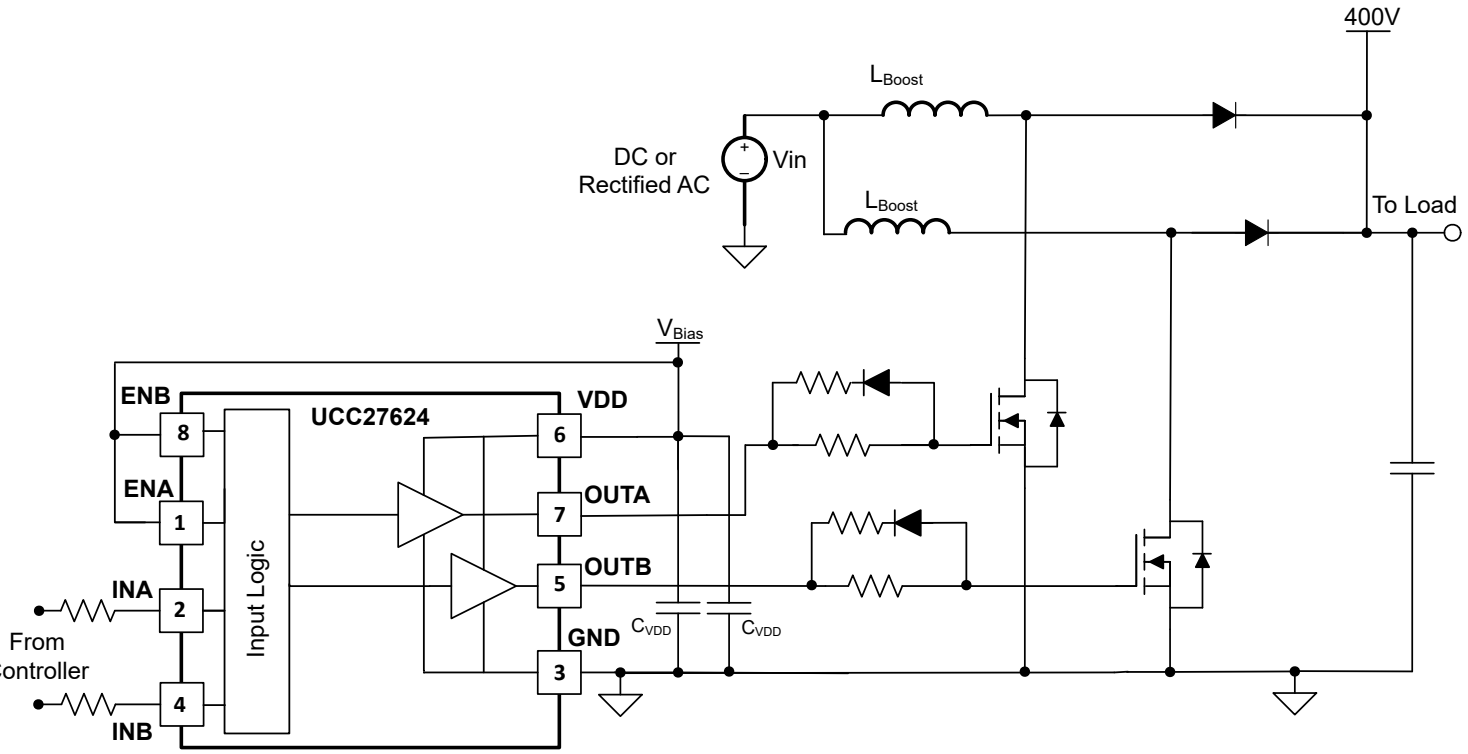

Figure 8-1. UCC27624 Typical Application Diagram

8.2.1 Design Requirements

When selecting and designing-in the gate driver device for an end application, some functional aspects must be considered and evaluated first, in order to make the most appropriate selection. Among these considerations are bias voltage, UVLO, drive current, and power dissipation.

8.2.2 Detailed Design Procedure

8.2.2.1 VDD and Undervoltage Lockout

The UCC27624 device has an internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low, regardless of the status of the inputs. The UVLO is typically 4 V with 300-mV typical hysteresis. This hysteresis prevents chatter when VDD supply voltages have noise, specifically at the lower end of the VDD operating range. UVLO hysteresis is also important to avoid any false tripping due to the bias noise generated because of fast switching transitions, where large peak currents are drawn from the bias supply bypass capacitors. The driver capability to operate at wide bias voltage range, along with good switching characteristics, is especially important in driving emerging power semiconductor devices, such as advanced low gate charge fast MOSFETs, GaN FETs, and SiC MOSFETs.

At power up, the UCC27624 driver device output remains low until the VDD voltage reaches the UVLO rising threshold irrespective of the state of any other input pins such as INx and ENx. Post UVLO rising threshold, the magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached.

Because the device draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor must be located as close as possible to the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1-µF), relatively low ESR type, must be connected in parallel (also as close to the driver IC as possible), in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

UCC27624 is a high current gate driver. If the gate driver is placed far from the switching power device such as MOSFET then that may create large inductive loop. Large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress exceeding device recommended rating. Therefore, it is recommended to place the gate driver as close to the switching power device as possible. It is also advisable to use an external gate resistor to damp any ringing due to the high switching currents and board parasitic elements.

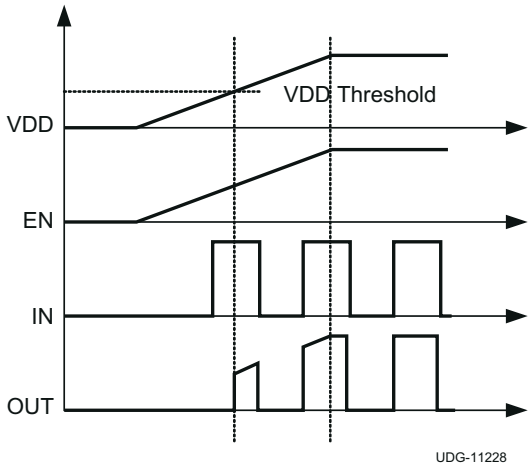

Figure 8-2. Power-Up sequence

8.2.2.2 Drive Current and Power Dissipation

The UCC27624 driver is capable of delivering 5-A of peak current to a switching power device gate (MOSFET, IGBT, SiC MOSFET, GaN FET) for a period of several-hundred nanoseconds at VDD = 12 V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground which repeats at the operating switching frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

Because UCC27624 features low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is very small compared to the losses due to switching of the power device.

When a driver device is tested with a discrete capacitive load, calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by equation below.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \quad (1)$$

where

- C_{LOAD} is the load capacitor
- V_{DD} is the bias voltage of the driver

There is an equal amount of energy dissipated when the capacitor is discharged. This leads to a total power loss given by the equation below.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \quad (2)$$

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where

- f_{SW} is the switching frequency

With V_{DD} = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz the switching power loss is calculated as equation below.

$$P_G = 10\,nF \times 12\,V^2 \times 300\,kHz = 0.432\,W \tag{3}$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor is determined which by using the equivalence $Q_g = C_{LOAD}V_{DD}$, which provides the equation beow.

$$P_G = C_{LOAD}V_{DD}{}^2 f_{SW} = Q_g V_{DD} f_{SW} \tag{4}$$

Assuming that the UCC27624 device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at V_{DD} = 12 V) on each output, the gate charge related power loss is calculated using the equation below.

$$P_G = 2 \times 60\,nC \times 12\,V \times 300\,kHz = 0.432\,W \tag{5}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as following.

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \tag{6}$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure)

Above equation comes into play when the external gate resistor is large enough to reduce the peak current of the driver. In addition to the above gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pull-up and pulldown resistors), enable, and UVLO sections. As shown in Electrical Characteristics table, the quiescent current is less than 1 mA. The power loss due to DC current consumption of the driver internal circuit can be calculated as below.

$$P_Q = I_{DD} V_{DD} \tag{7}$$

Assuming total internal current consumption to be 0.6 mA (typical) at bias voltage of 12 V, the DC power loss in the driver is:

$$P_Q = 0.6\,mA \times 12\,V = 7.2\,mW \tag{8}$$

Clearly, this power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ W}{12\ V} = 0.036\ A \quad (9)$$

If the gate driver is used with inductive load then special attention should be paid to the ringing on each pin of the gate driver device. The ringing should not exceed the recommended operating rating of the pin.

8.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC27624 device used in high-voltage boost converter application. In this application, the UCC27624 is driving the IGBT switch that has a gate charge of 110 nC.

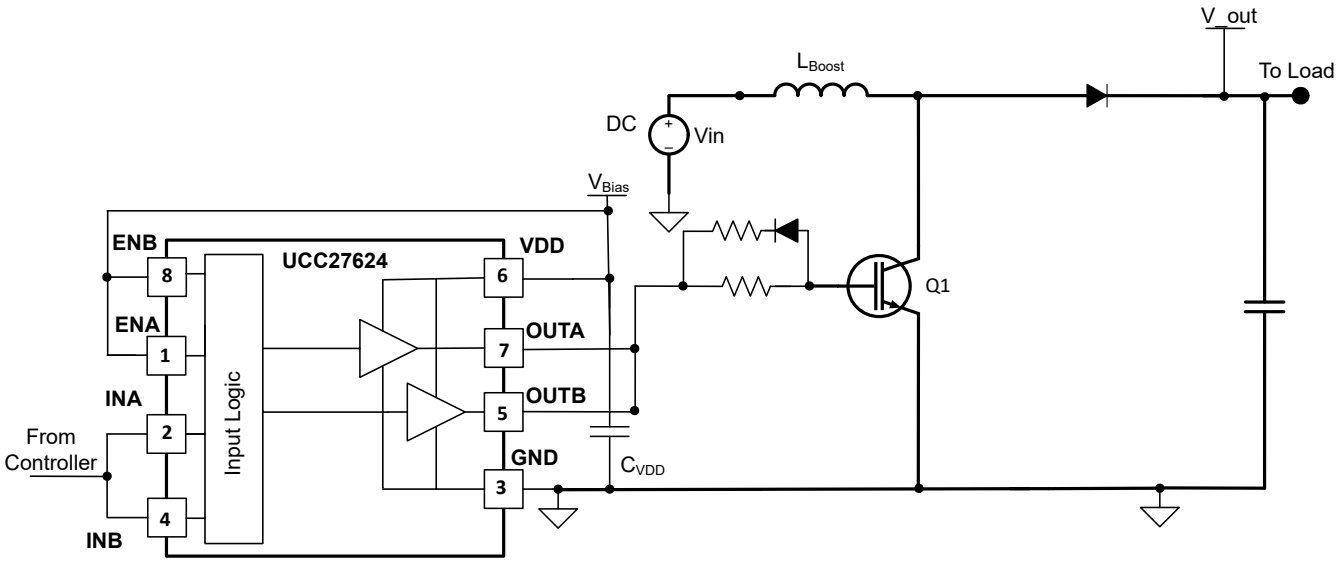
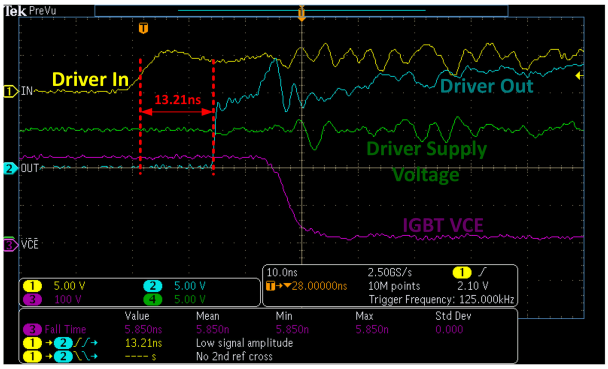
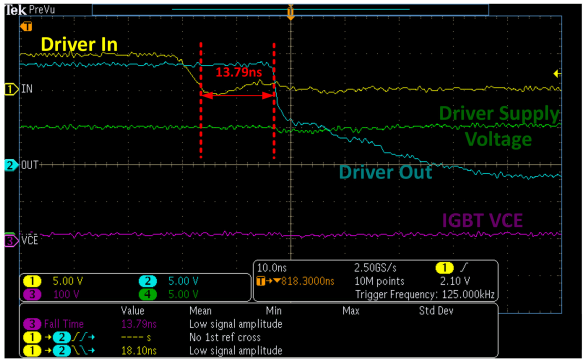


Figure 8-3. UCC27624D Used to Drive IGBT in the Boost Converter



Vin = 210 V, Vout = 235 V, Iout = 1.14 A, Fsw = 125 kHz,
Driver supply voltage=15 V, Gate resistor= 0 Ω

Figure 8-4. Turn-on Propagation Delay Waveform



Vin = 210 V, Vout= 235 V, Iout = 1.14 A, Fsw = 100 kHz,
Driver supply voltage = 15 V, Gate resistor= 0 Ω

Figure 8-5. Turn-off Propagation Delay Waveform

9 Power Supply Recommendations

The bias supply voltage range for which the UCC27624 device is rated to operate is from 4.5 V to 26 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the VDD UVLO turn-on (rising) threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 30-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). It is necessary to have sufficient margin from the absolute maximum rating of the device to realize full operating life of the device. Therefore, the upper limit of recommended voltage of the VDD pin is 26 V.

The UVLO protection feature also involves a hysteresis function. This means, when the VDD pin bias voltage has exceeded the threshold voltage and the device begins to operate, if the bias voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification. Therefore, while operating at or near the 4.5-V, design engineer should ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device. Otherwise the device output may turn-off. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD turn-off (falling) threshold, which must be accounted for while evaluating system shutdown timing or sequencing requirements. At system startup, the device does not begin operation until the VDD pin voltage has exceeded VDD turn-on (rising) threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same VDD pin capacitor, is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus, ensure that the local bypass capacitors are provided between the VDD and GND pins and locate them as close to the device pins as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is a must. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor which can be placed very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

UCC27624 is a high current gate driver. If the gate driver is placed far from the switching power device such as MOSFET then that may create large inductive loop. Large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress exceeding device recommended rating. Therefore, it is recommended to place the gate driver as close to the switching power device as possible. It is also advisable to use an external gate resistor to damp any ringing due to the high switching currents and board parasitic elements.

10 Layout

10.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27624 gate driver incorporates small propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate very quick voltage transitions. Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver IC as close as possible to the power device in order to minimize the length of high-current traces between the driver IC output pins and the gate of the switching power device.
- Place the VDD bypass capacitors between VDD and GND as close as possible to the driver IC with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD pin, during turn-on of power MOSFET. The use of low inductance surface-mounted-device (SMD) components such as 50V rated X7R chip capacitors are highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances, namely during turn-on and turn-off transients, which induces significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin of the driver IC may corrupt the input signals of the driver IC. The ground plane must not be a conduction path for any high current (power stage) loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- External gate resistor and parallel diode-resistor combination may come in handy when replacing any gate driver IC with UCC27624 device in existing or new designs, specifically if they do not have the same drive strength.

10.2 Layout Example

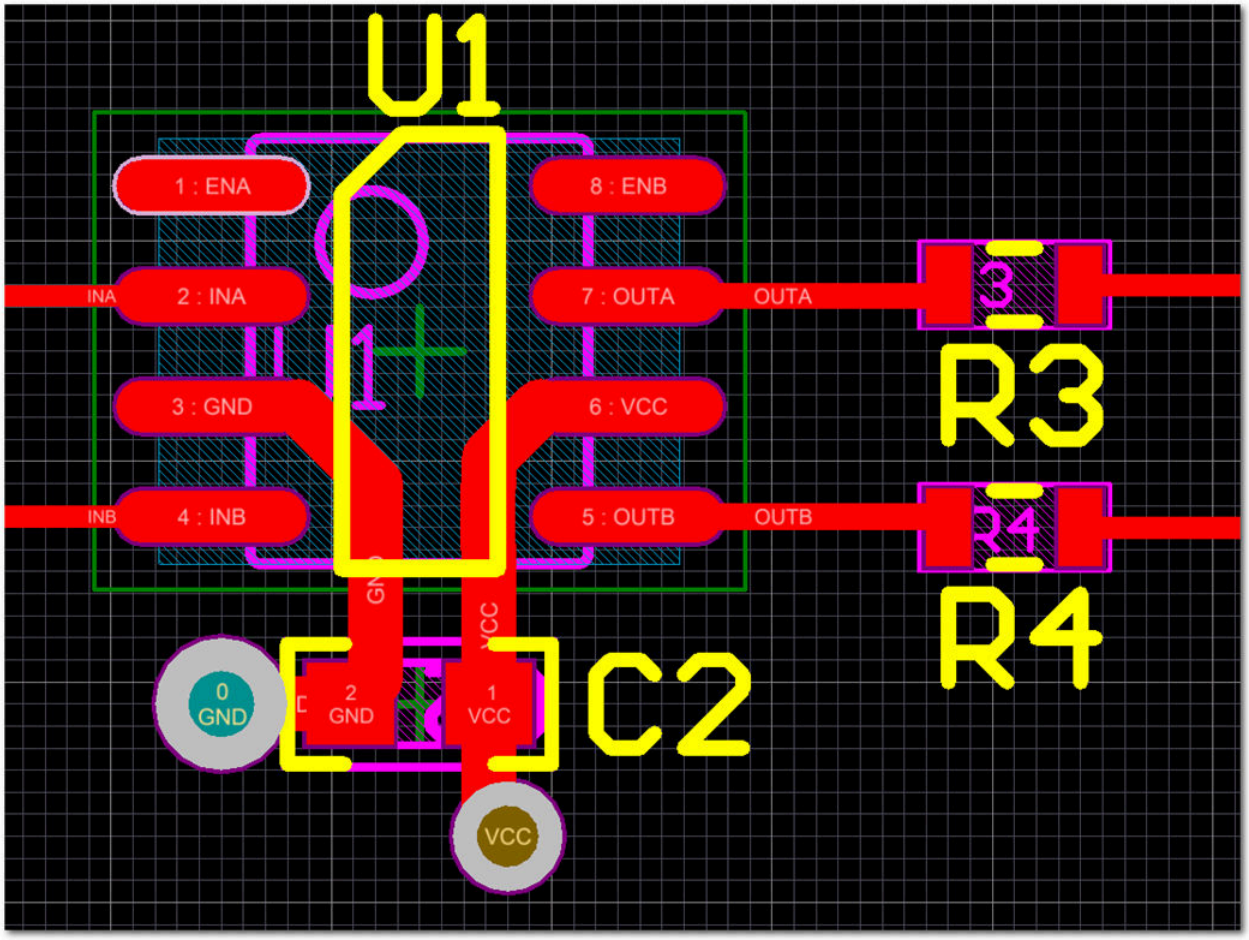


Figure 10-1. UCC27624 Layout Example

10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced, while keeping the junction temperature within the specified limit. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled, *Semiconductor and IC Package Thermal Metrics* (SPRA953).

Among the different package options available for the UCC27624 device, power dissipation capability of the DGN package is of particular mention. The VSSOP-8 (DGN) package offers thermal pad for removing the heat from the semiconductor junction through the bottom of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the VSSOP-8 package are not directly connected to any leads of the package, however, the PowerPAD is thermally connected to the substrate of the device. TI recommends to externally connect the exposed pads to GND pin of the driver IC in PCB layout.

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC27624DR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

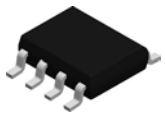
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

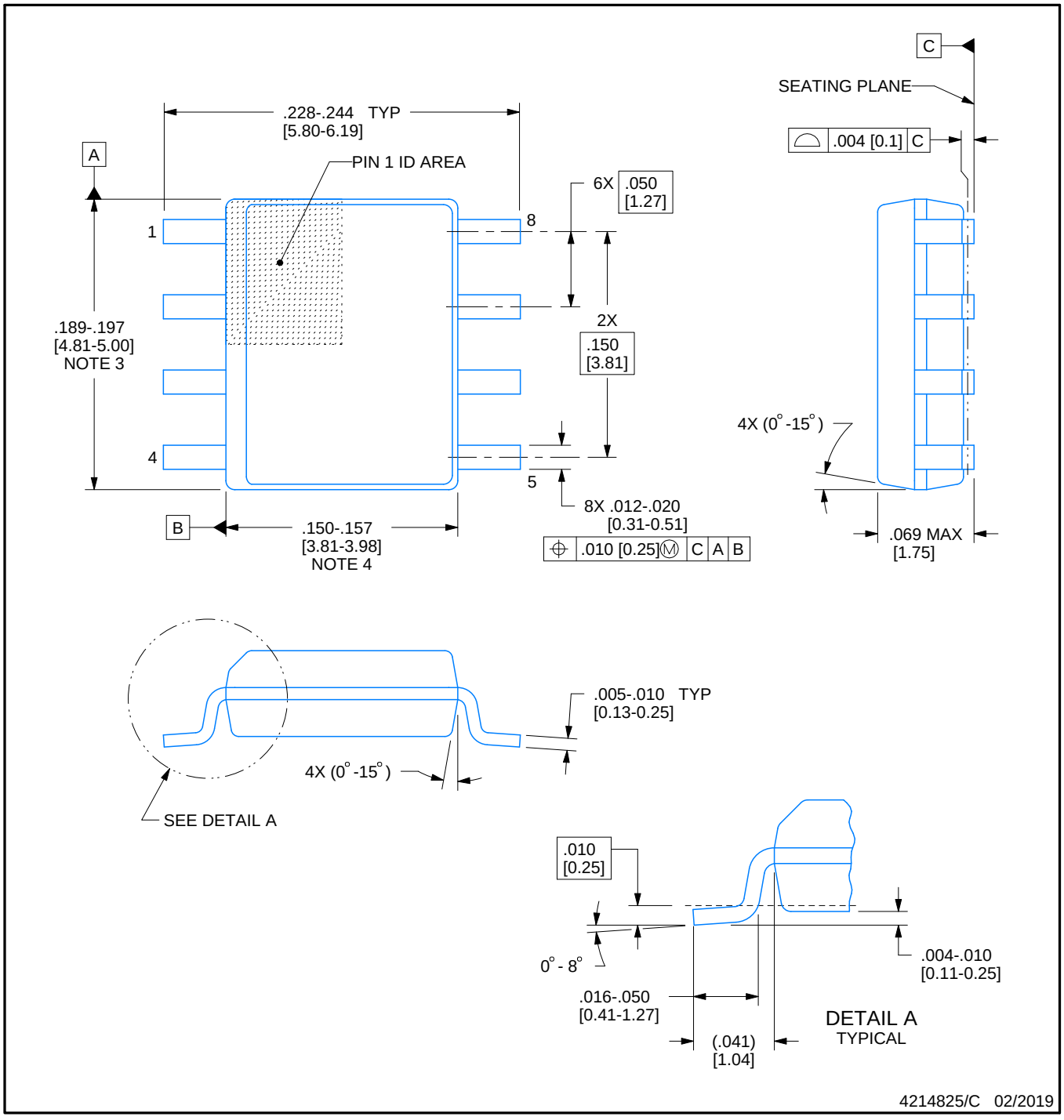


PACKAGE OUTLINE

D0008A

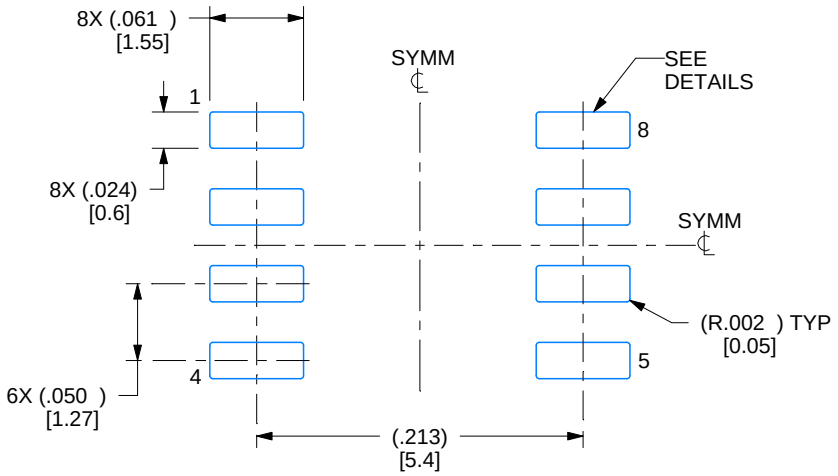
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

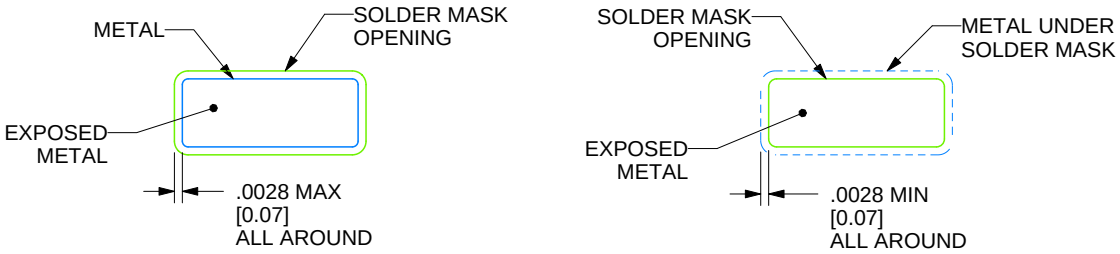


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

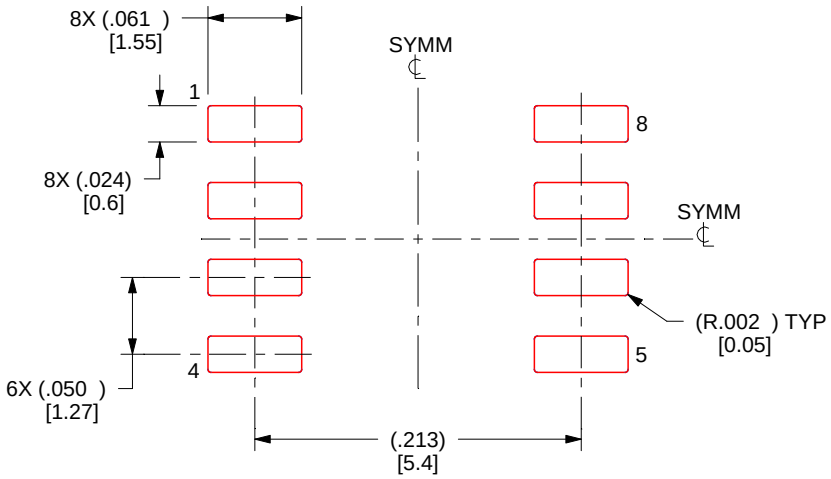
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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