Implementation of Automatic Test Pattern Generator | Self Project

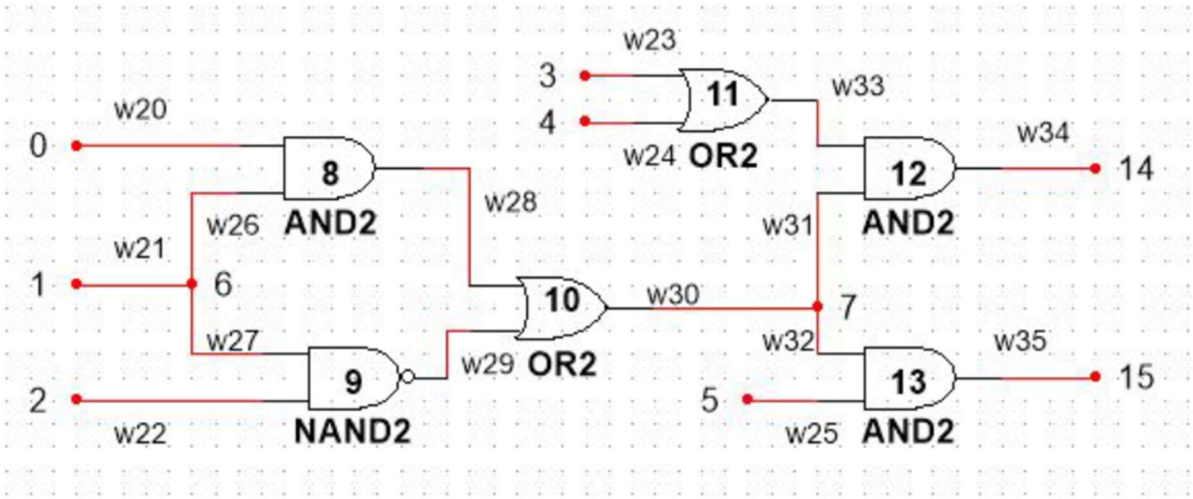
GUNANJAN REDDY K

23M1148 EE7

ELECTRICAL ENGINEERING

IIT BOMBAY

Automatic Test Pattern Generation (ATPG) is a crucial process in the design and verification of digital circuits, particularly in the context of VLSI (Very Large Scale Integration) design. ATPG is used to generate test patterns that can be applied to a digital circuit to identify faults or defects, such as manufacturing defects, that may have occurred during the fabrication process.



1. Setting Up the Environment

To begin, install the necessary dependencies using the following command:

```bash sudo apt install qt5-default qt5-qmake libqt5charts5-dev qtmultimedia5-dev
```

Then, build the project using QTCreator or the terminal:

For debugging, use the following commands:

```bash

qmake

CONFIG+=debug

make
```

```

## 2. Running ATPG Algorithms

To demonstrate the ATPG capabilities, run the tool on different circuits for stuck-at-0 and stuck-at-1 faults.

Example test cases:

1. dcirc1 N30 stuck-at-0
    - PIs: N5[1] N4[x] N3[x] N2[0] N1[1] N0[x]
    - POs: N15[D] N14[x]
2. c17 N11 stuck-at-1
    - PIs: N7[1] N2[1] N6[1] N3[1] N1[x]
    - POs: N23[E] N22[x]

## 3. Delay Timing Analysis

The tool allows you to perform delay timing analysis and critical path calculation. It also supports path sensitization and delay fault detection. Here's an example of a sensitized path:

Path: N3 NAND2_2 N11 NAND2_4 N19 NAND2_6 N23, Delay: X ns

## 4. False Path Detection

False path detection is crucial for accurate timing analysis. The Verilog-ATPG tool can identify these paths and help ensure the reliability of the circuit timing.
```

5. Generating Reports

Results can be compiled into a report using LaTeX or any other report generation tool. Below is an example LaTeX code snippet to create a simple report:

```latex
\documentclass{article}
\title{ATPG Report}
\begin{document}
\maketitle
\section*{Stuck-at Faults}
\begin{itemize}
\item dcirc1 N30 stuck-at-0: PIs: N5[1] N4[x] N3[x] N2[0] N1[1] N0[x], POs: N15[D] N14[x]
\item c17 N11 stuck-at-1: PIs: N7[1] N2[1] N6[1] N3[1] N1[x], POs: N23[E] N22[x]
\end{itemize}
\section*{Delay Timing Analysis}
\begin{itemize}
\item Path: N3 NAND2_2 N11 NAND2_4 N19 NAND2_6 N23, Delay: X ns
\end{itemize}
\end{document}
```

Compile the LaTeX file to generate the PDF report.

6. Conclusion

This guide provides a comprehensive walkthrough of using the Verilog-ATPG tool, from setup to report generation. Following these steps will allow you to create a clear and informative demo video.