# Chapter 2

# Combinational Logic Design

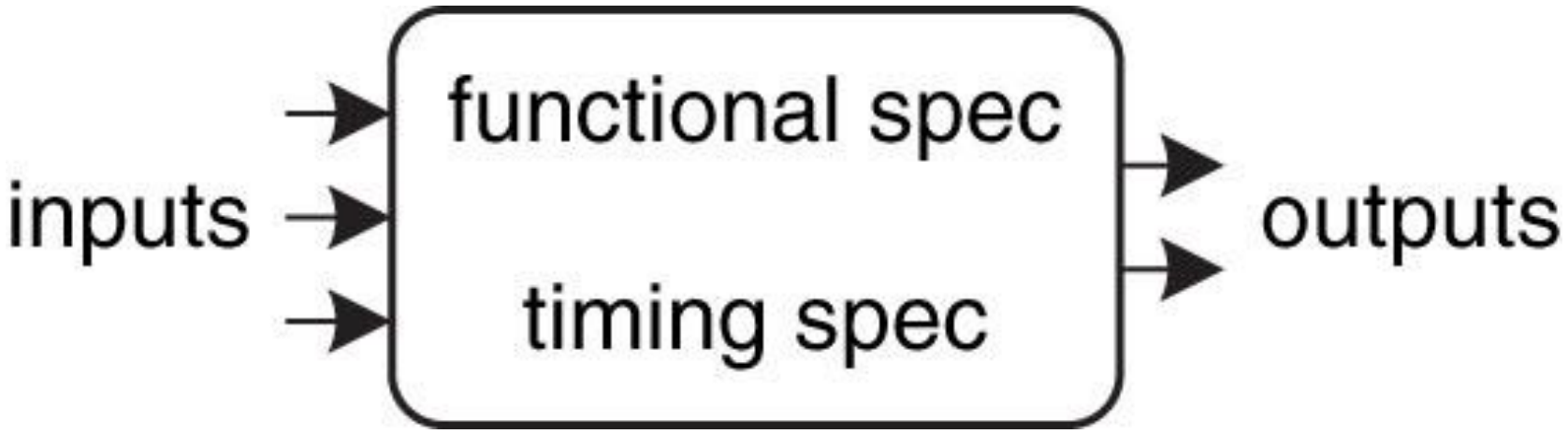



**Figure 2.1 Circuit as a black box with inputs, outputs, and specifications**

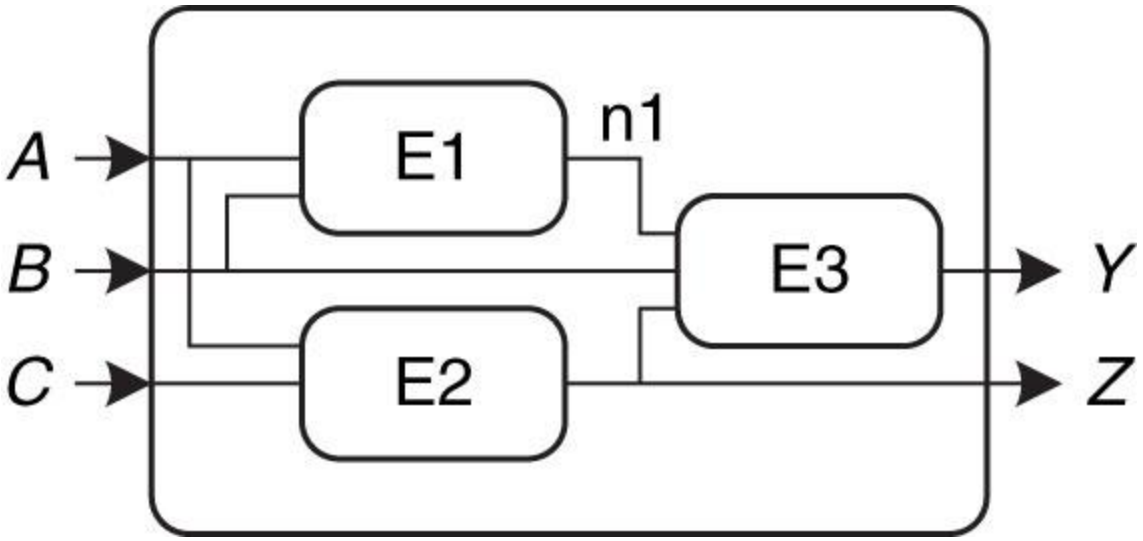
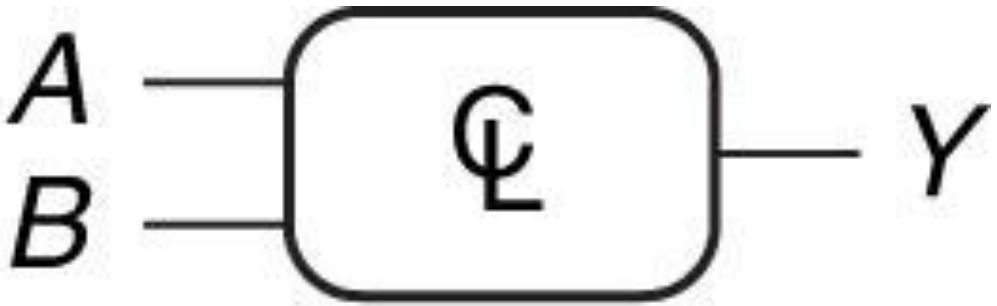



**Figure 2.2 Elements and nodes**




$$Y = F(A, B) = A + B$$

**Figure 2.3 Combinational logic circuit**

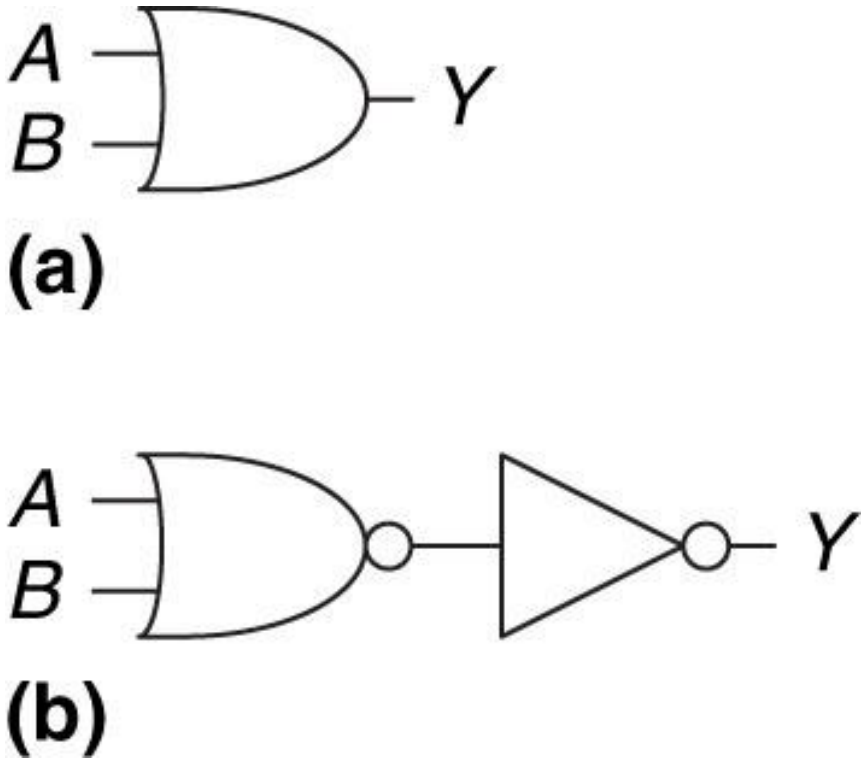
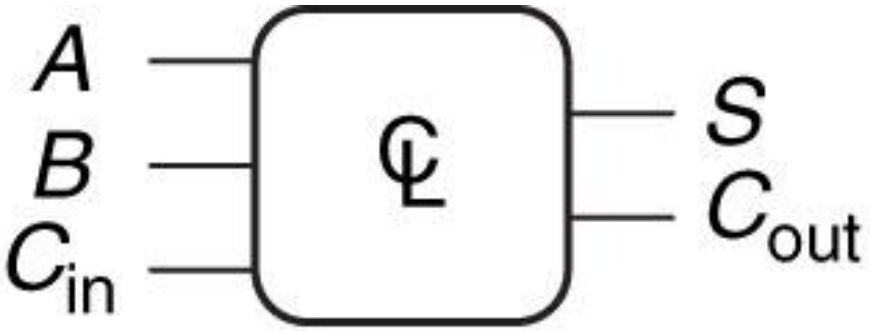



**Figure 2.4 Two OR implementations**




$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + AC_{in} + BC_{in}$$

**Figure 2.5 Multiple-output combinational circuit**

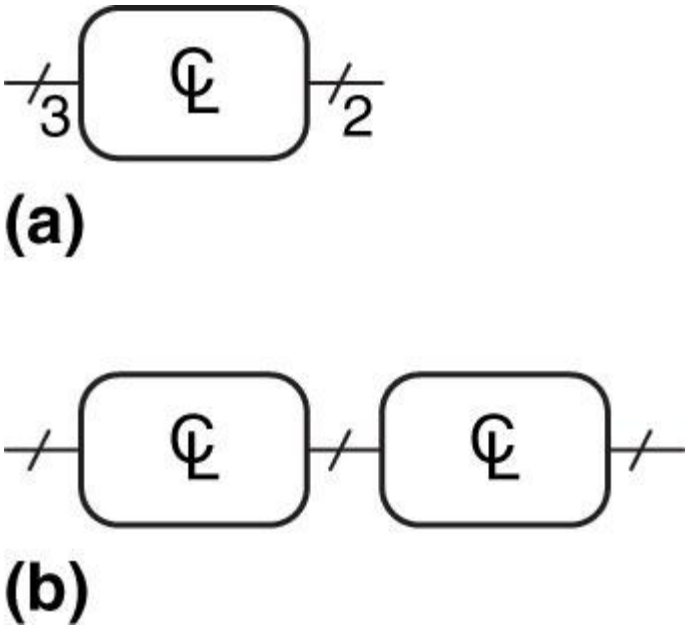



**Figure 2.6 Slash notation for multiple signals**

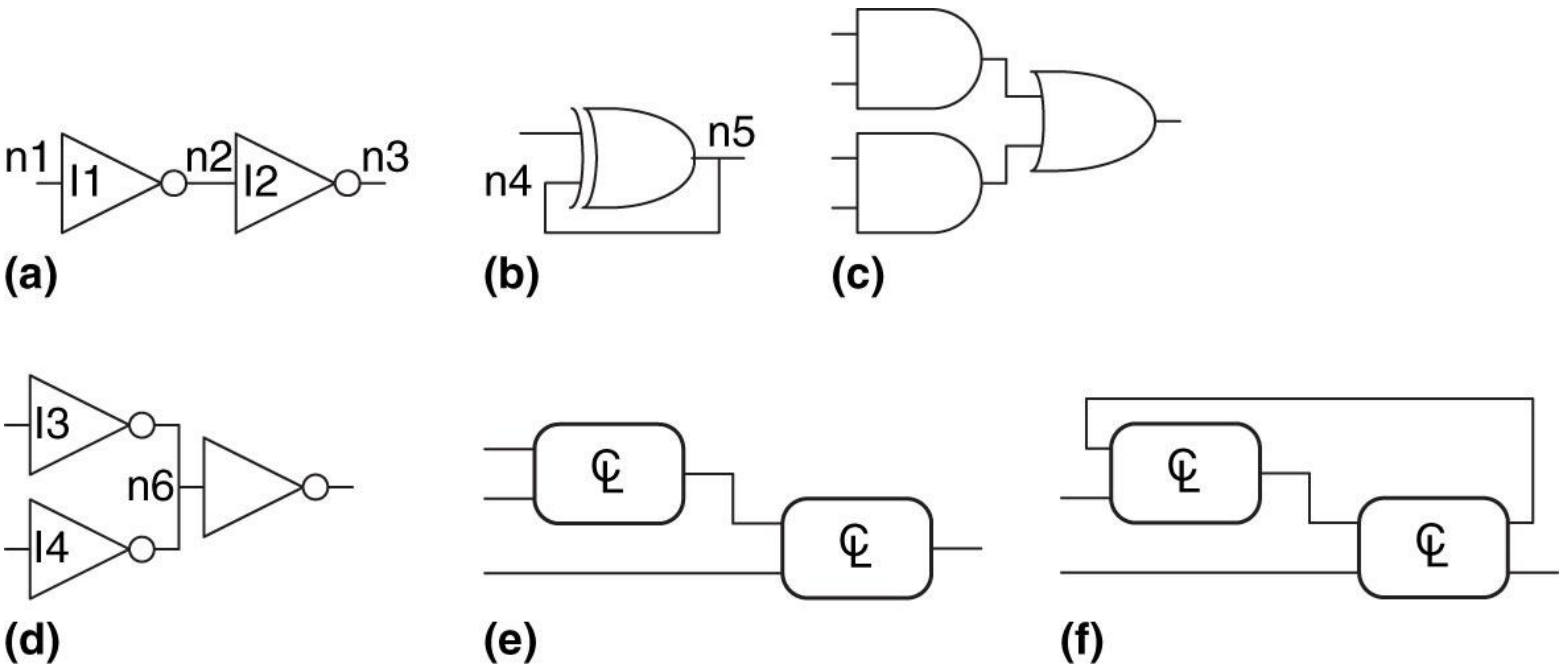
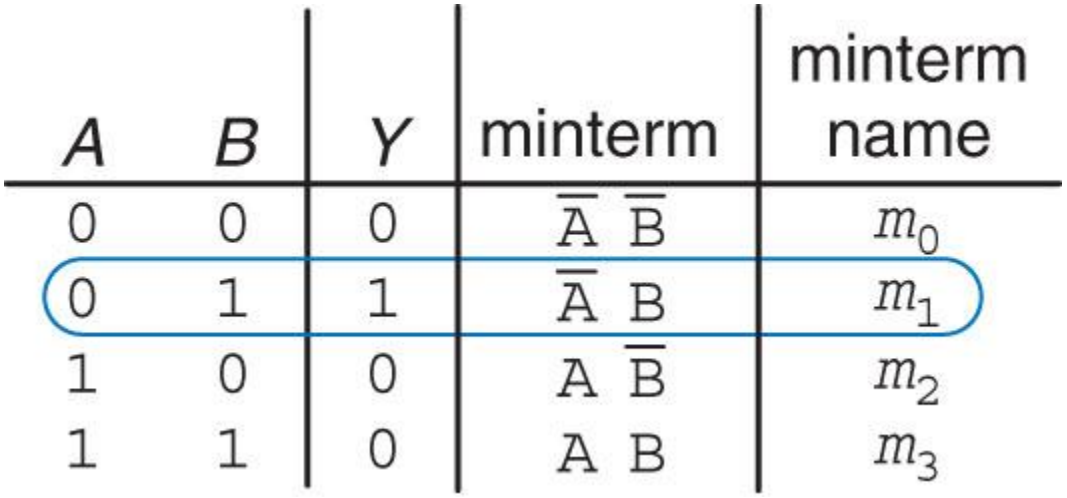



**Figure 2.7 Example circuits**



| A | B | Y | minterm | minterm name |
|---|---|---|---|---|
| 0 | 0 | 0 | $\overline{A}\ \overline{B}$ | $m_0$ |
| 0 | 1 | 1 | $\overline{A}\ B$ | $m_1$ |
| 1 | 0 | 0 | $A\ \overline{B}$ | $m_2$ |
| 1 | 1 | 0 | $A\ B$ | $m_3$ |

**Figure 2.8 Truth table and minterms**

| A | B | Y | minterm | minterm name |
|---|---|---|---|---|
| 0 | 0 | 0 | $\overline{A}\ \overline{B}$ | $m_0$ |
| 0 | 1 | 1 | $\overline{A}\ B$ | $m_1$ |
| 1 | 0 | 0 | $A\ \overline{B}$ | $m_2$ |
| 1 | 1 | 1 | $A\ B$ | $m_3$ |

**Figure 2.9 Truth table with multiple TRUE minterms**

| A | R | E |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Figure 2.10 Ben's truth table**

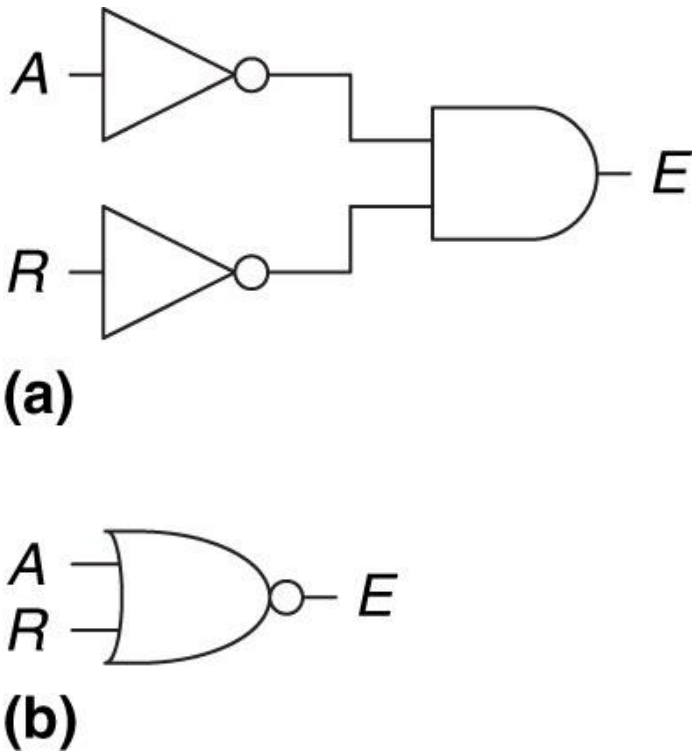



**Figure 2.11 Ben's circuit**

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Figure 2.12 Random three-input truth table**

| A | B | Y | maxterm | maxterm name |
|---|---|---|---|---|
| 0 | 0 | 0 | $A + B$ | $M_0$ |
| 0 | 1 | 1 | $A + \overline{B}$ | $M_1$ |
| 1 | 0 | 0 | $\overline{A} + B$ | $M_2$ |
| 1 | 1 | 1 | $\overline{A} + \overline{B}$ | $M_3$ |

**Figure 2.13 Truth table with multiple FALSE maxterms**

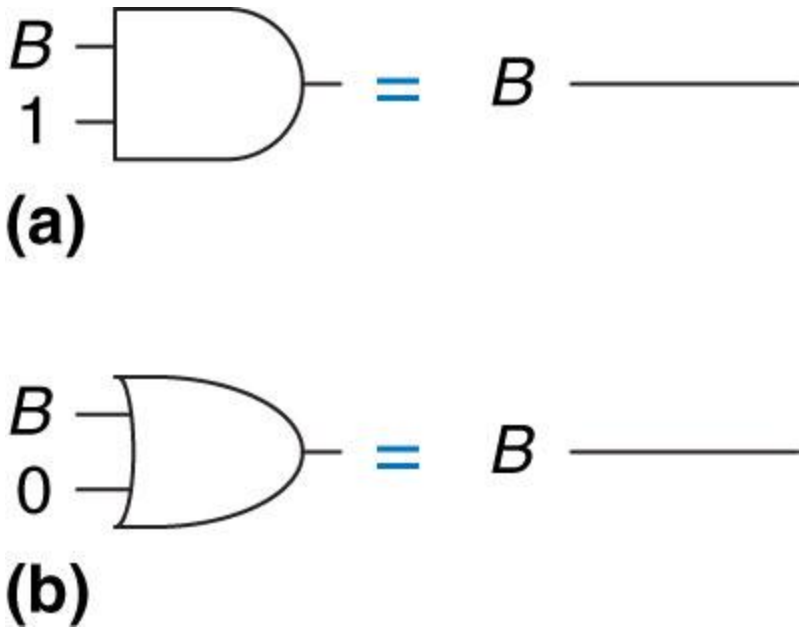



**Figure 2.14 Identity theorem in hardware: (a) T1, (b) T1′**

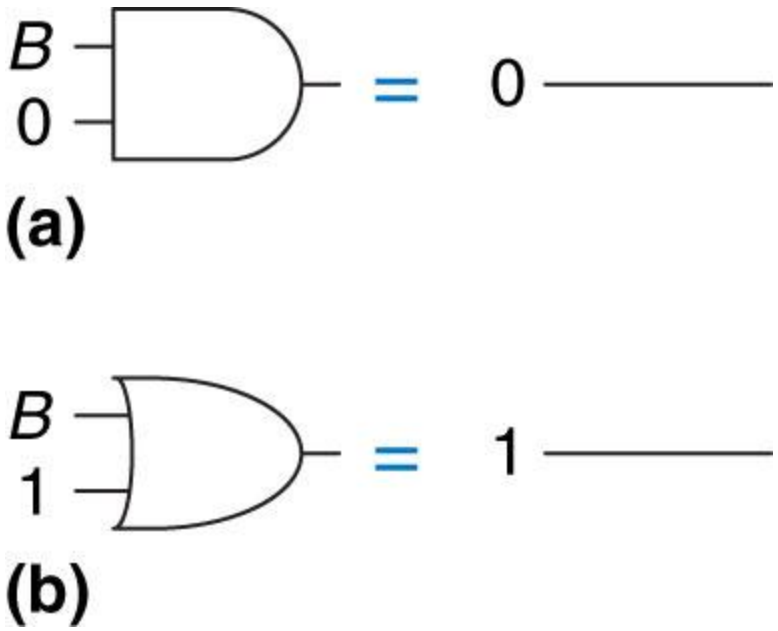



**Figure 2.15 Null element theorem in hardware: (a) T2, (b) T2′**

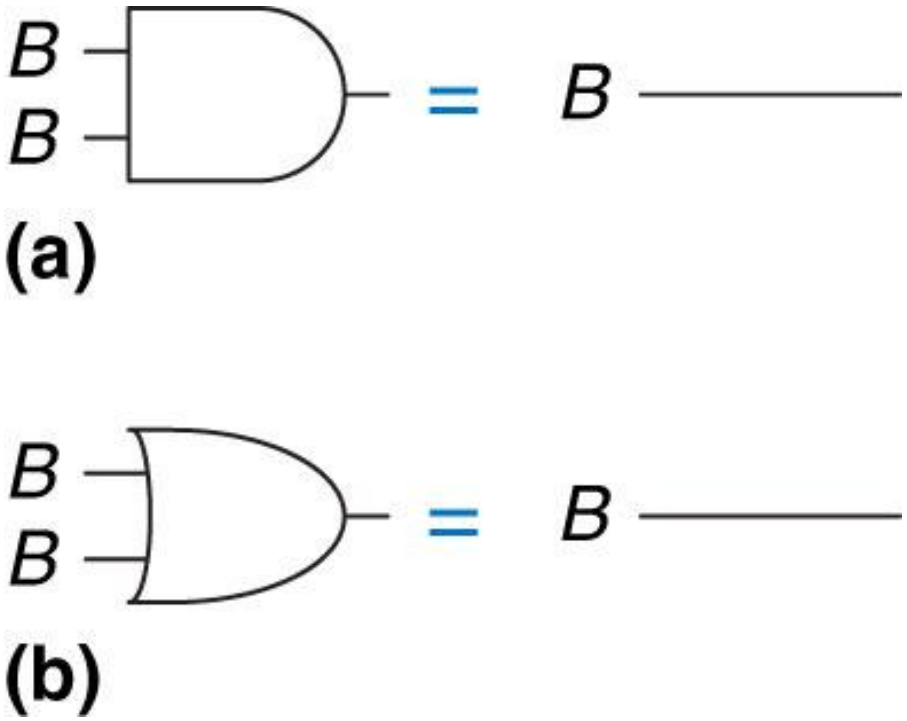



**Figure 2.16 Idempotency theorem in hardware: (a) T3, (b) T3′**

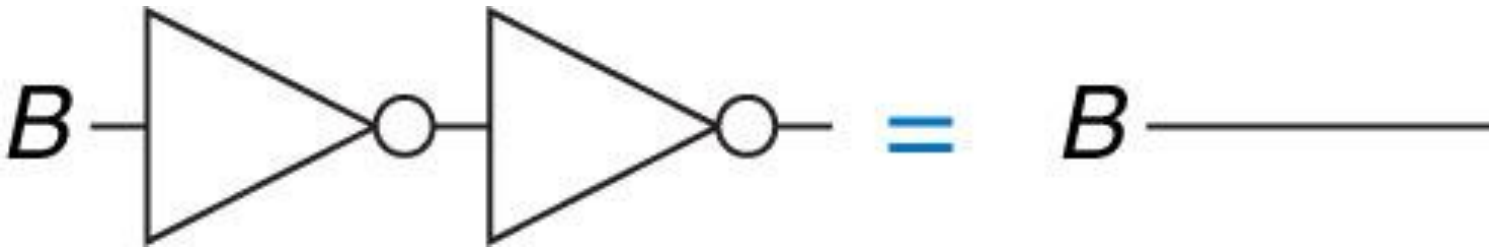



**Figure 2.17 Involution theorem in hardware: T4**

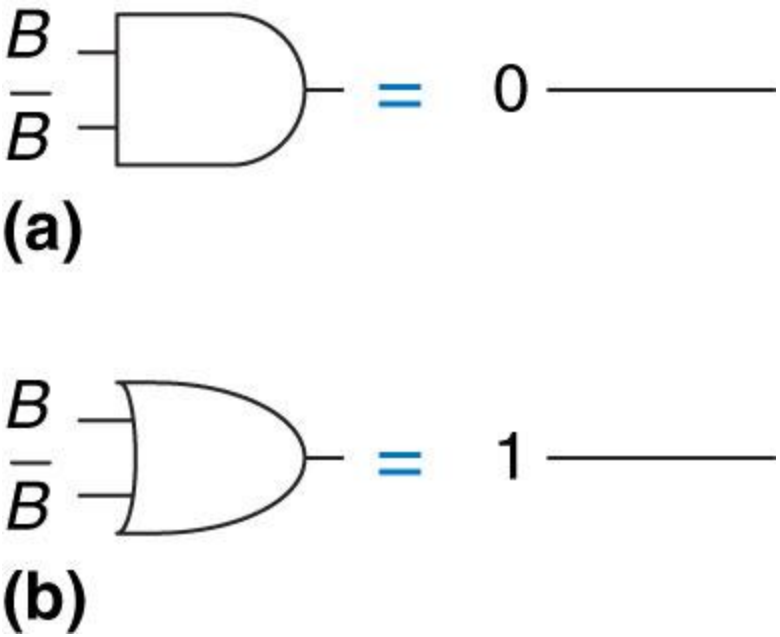
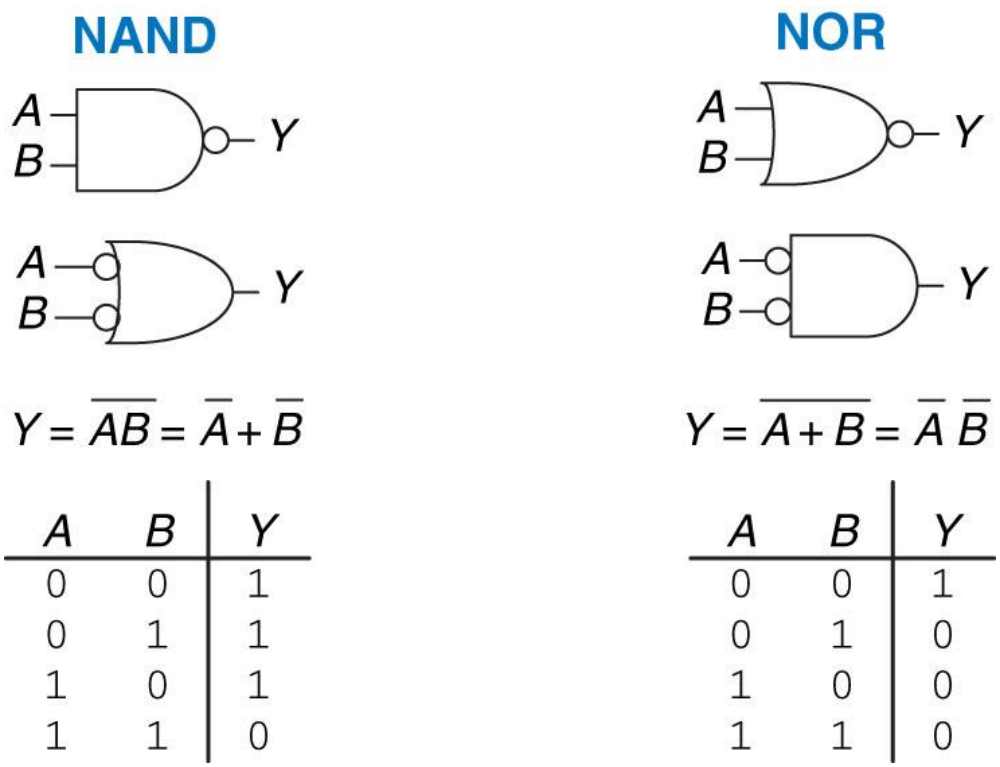



**Figure 2.18 Complement theorem in hardware: (a) T5, (b) T5′**



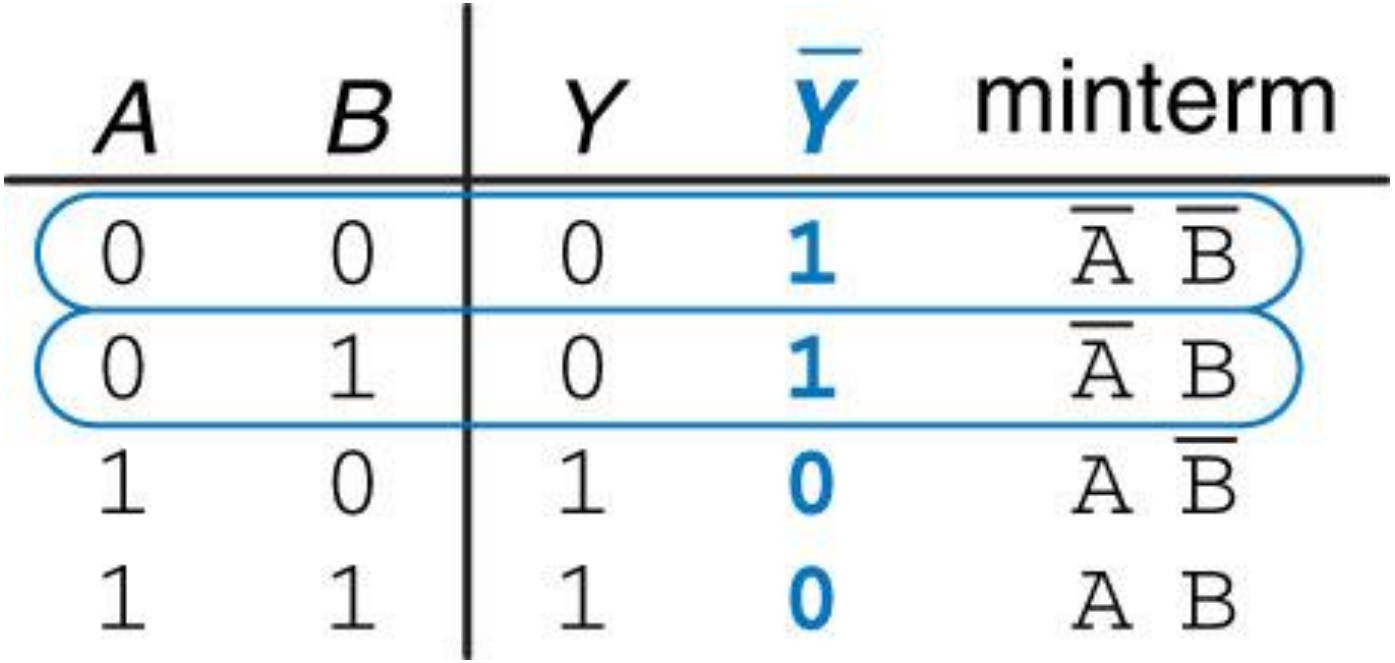

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Figure 2.19 De Morgan equivalent gates**

| $A$ | $B$ | $Y$ | $\overline{Y}$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

**Figure 2.20 Truth table showing *Y* and $\overline{Y}$**



| A | B | Y | $\overline{Y}$ | minterm |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | $\overline{A}\,\overline{B}$ |
| 0 | 1 | 0 | 1 | $\overline{A}\,B$ |
| 1 | 0 | 1 | 0 | $A\,\overline{B}$ |
| 1 | 1 | 1 | 0 | $A\,B$ |

**Figure 2.21 Truth table showing minterms for $\overline{Y}$**

| $B$ | $C$ | $D$ | $BC + \overline{B}D + CD$ | $BC + \overline{B}D$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Figure 2.22 Truth table proving T11**

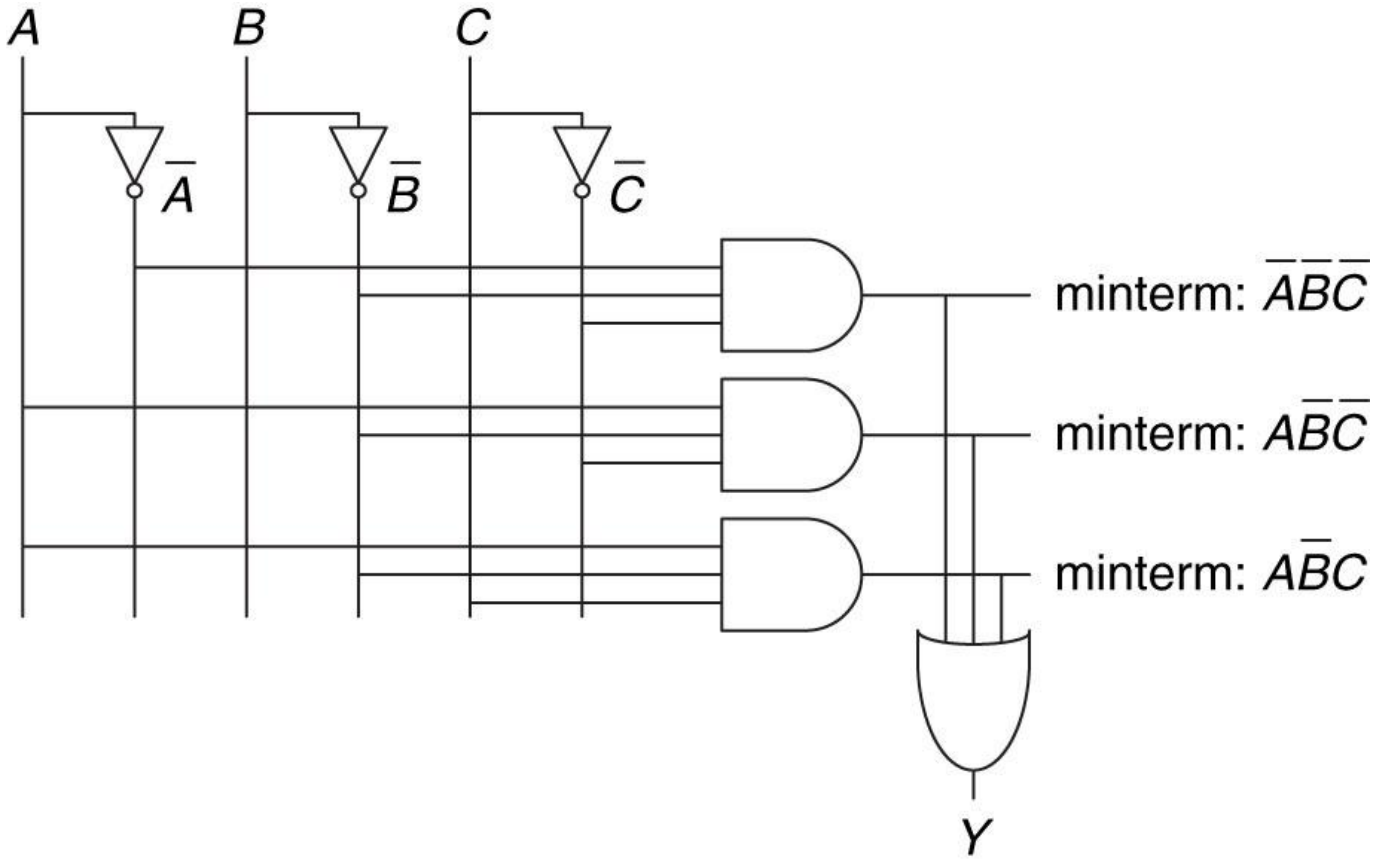



**Figure 2.23 Schematic of** $Y = \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C$

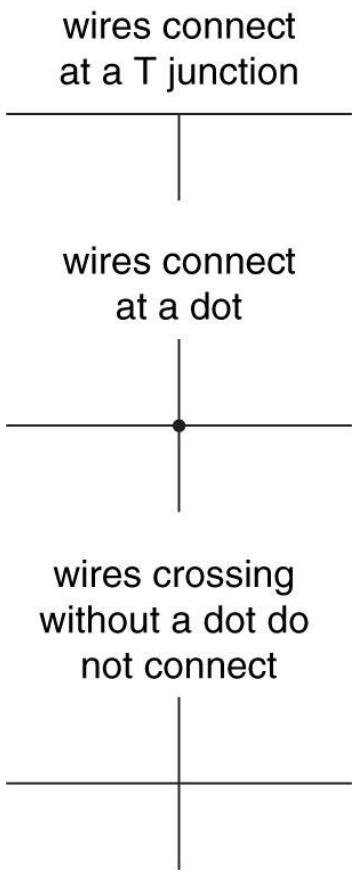



**Figure 2.24 Wire connections**

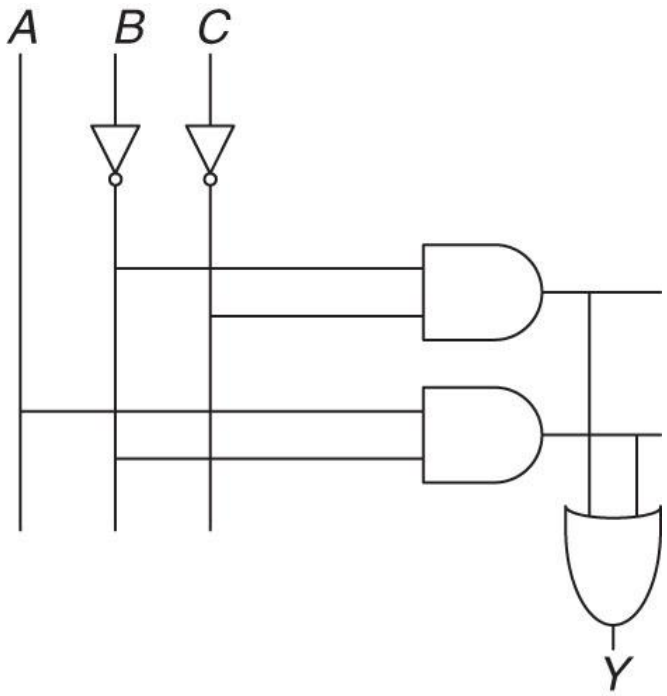



**Figure 2.25 Schematic of** $Y = \overline{B}\,\overline{C} + A\overline{B}$

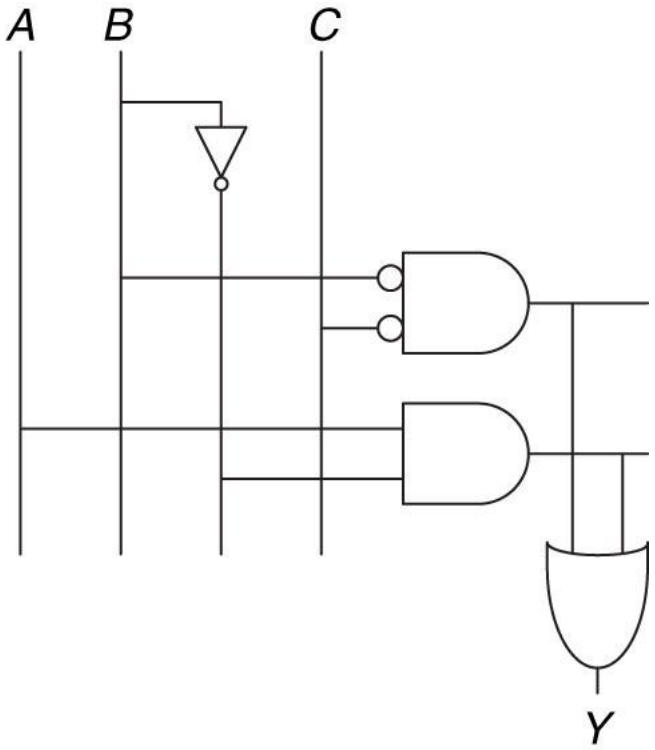
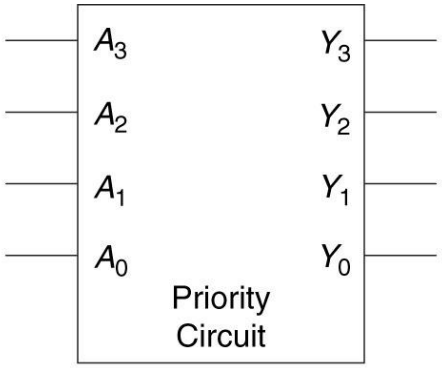



**Figure 2.26 Schematic using fewer gates**




| $A_3$ | $A_2$ | $A_1$ | $A_0$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

**Figure 2.27 Priority circuit**

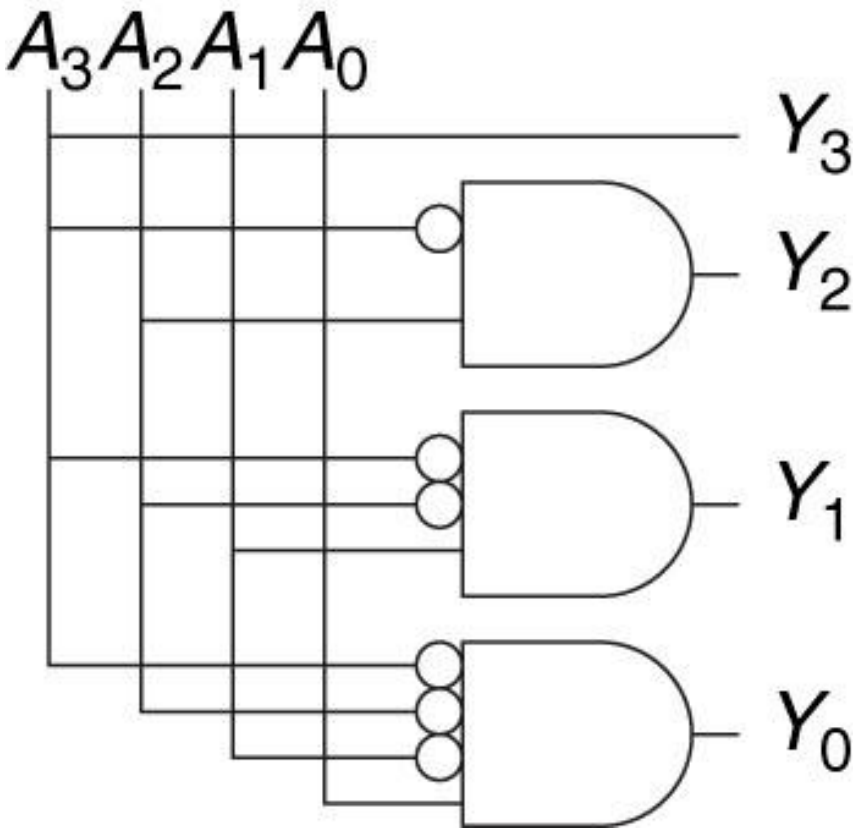



**Figure 2.28 Priority circuit schematic**

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | X | 0 | 0 | 1 | 0 |
| 0 | 1 | X | X | 0 | 1 | 0 | 0 |
| 1 | X | X | X | 1 | 0 | 0 | 0 |

**Figure 2.29 Priority circuit truth table with don't cares (X's)**

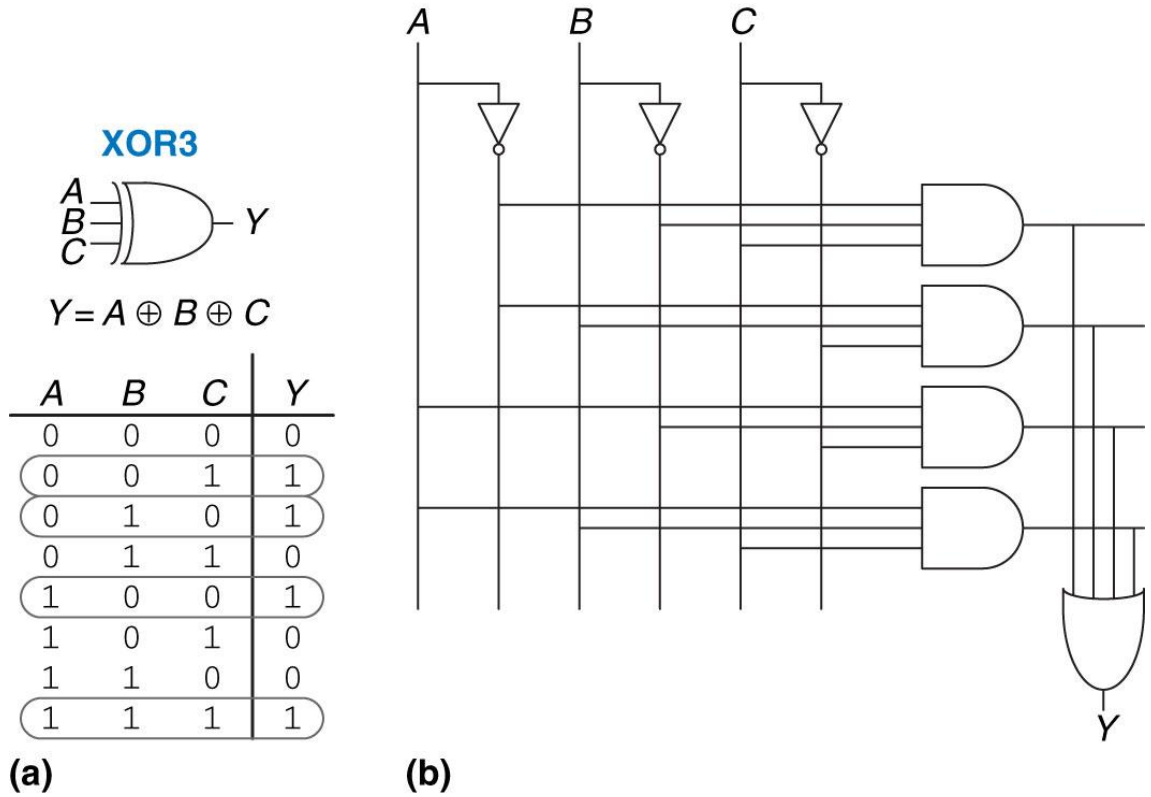



**Figure 2.30 Three-input XOR: (a) functional specification and (b) two-level logic implementation**

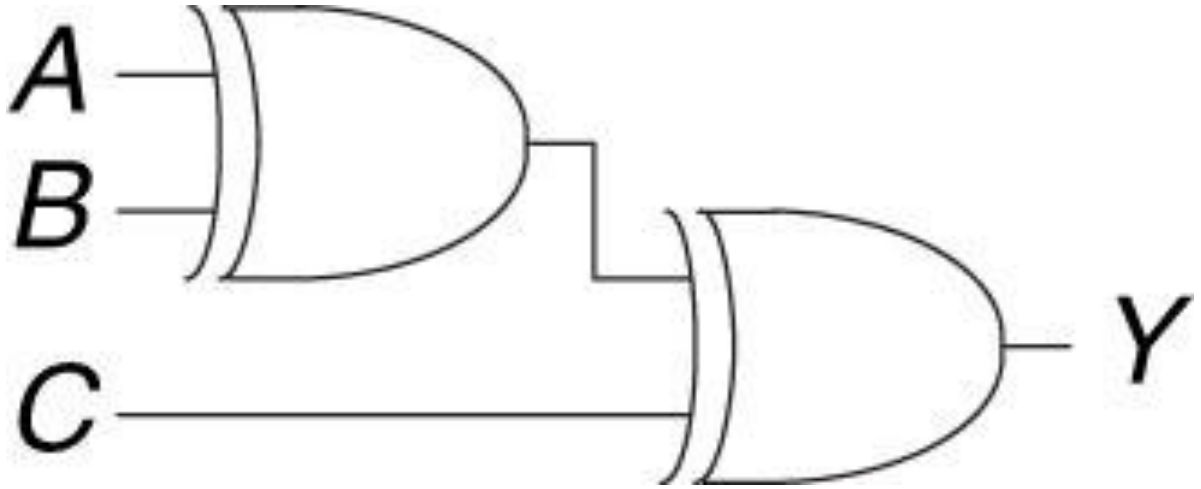



**Figure 2.31 Three-input XOR using two-input XORs**

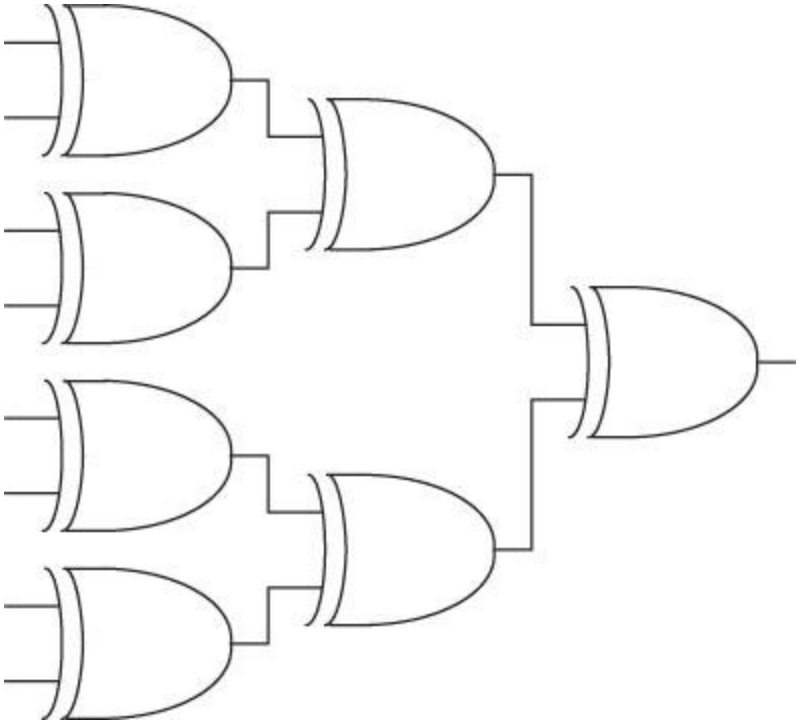


**Figure 2.32 Eight-input XOR using seven two-input XORs**

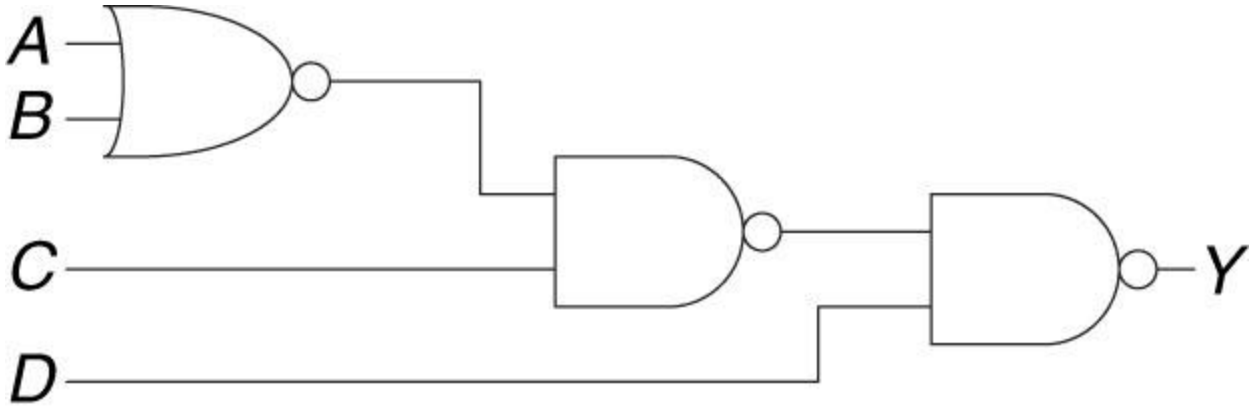



**Figure 2.33 Multilevel circuit using NANDs and NORs**

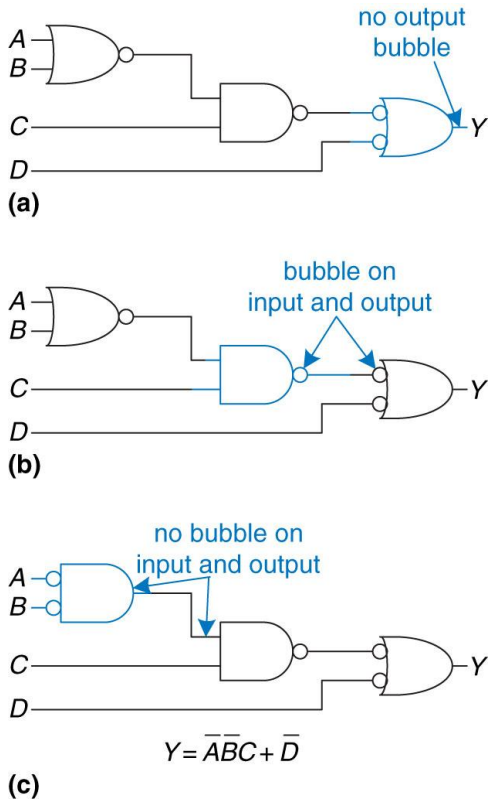



**Figure 2.34 Bubble-pushed circuit**

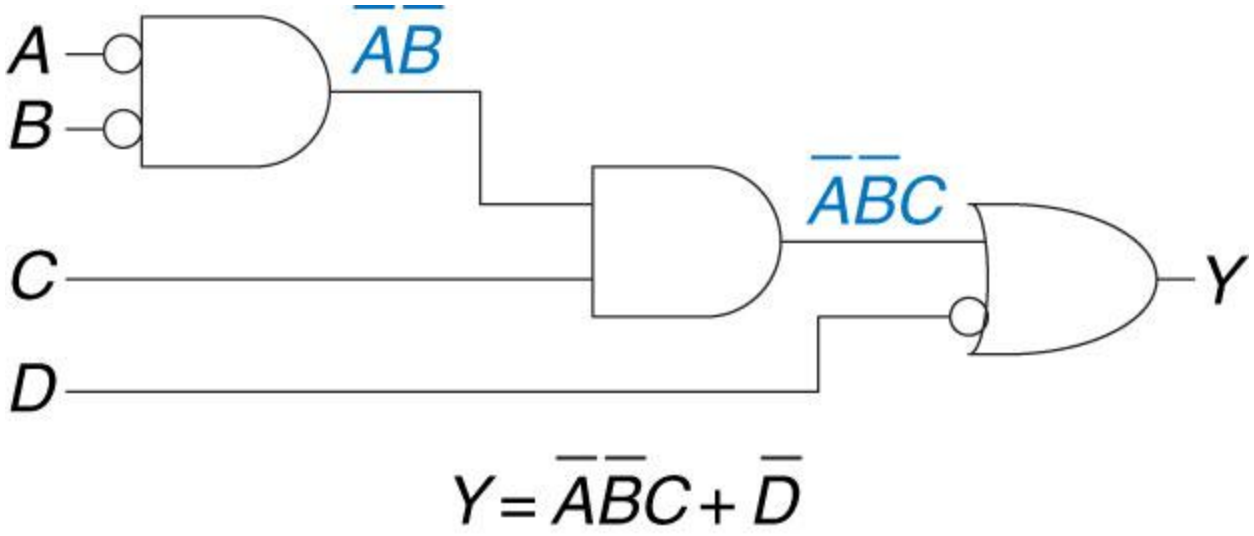



**Figure 2.35 Logically equivalent bubble-pushed circuit**

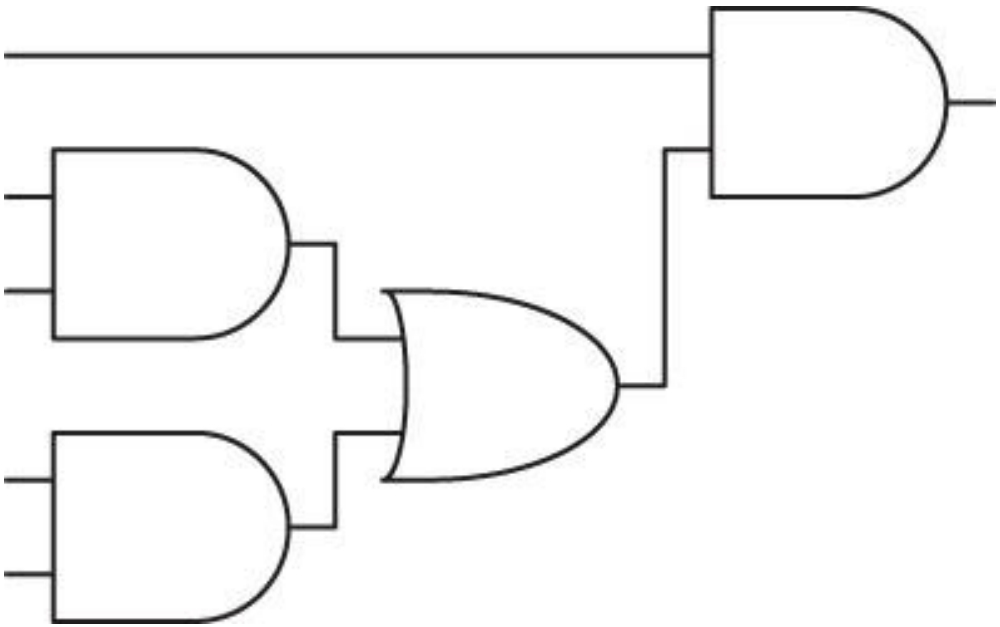


**Figure 2.36 Circuit using ANDs and ORs**

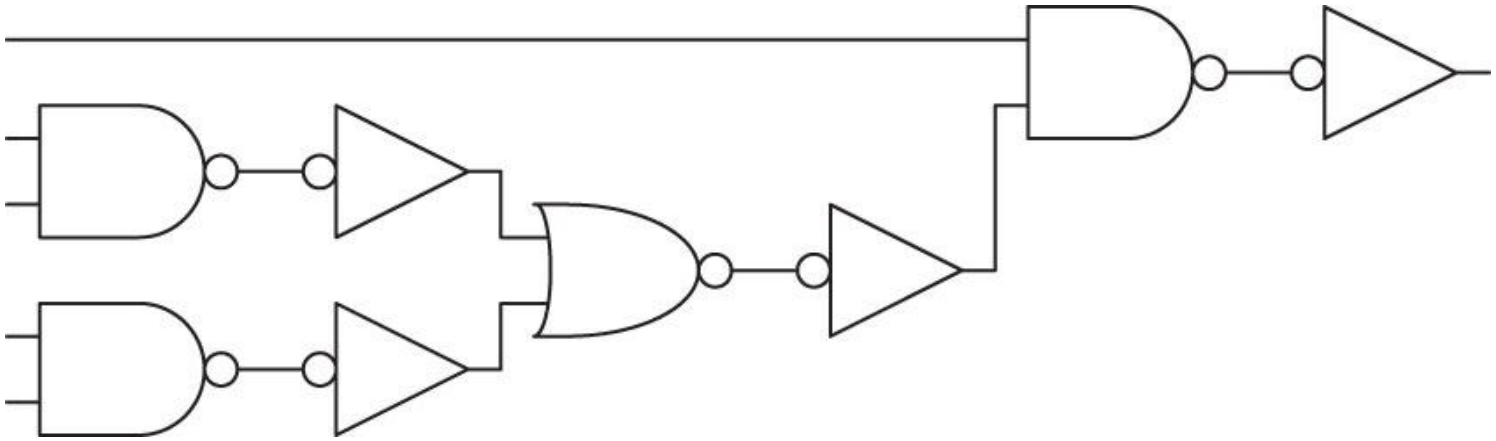


**Figure 2.37 Poor circuit using NANDs and NORs**

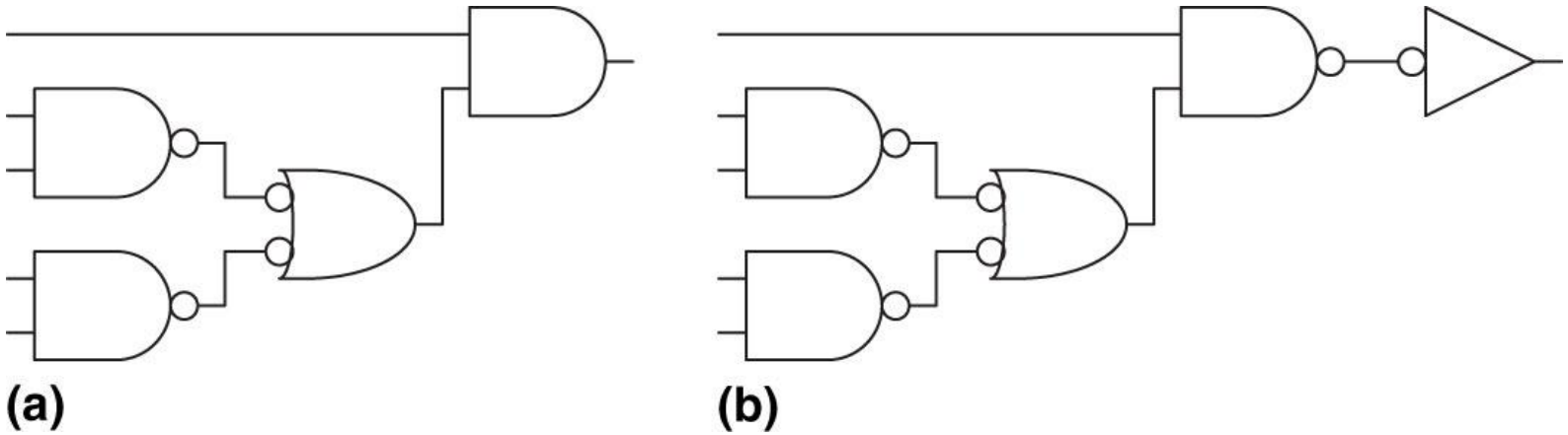



**Figure 2.38 Better circuit using NANDs and NORs**

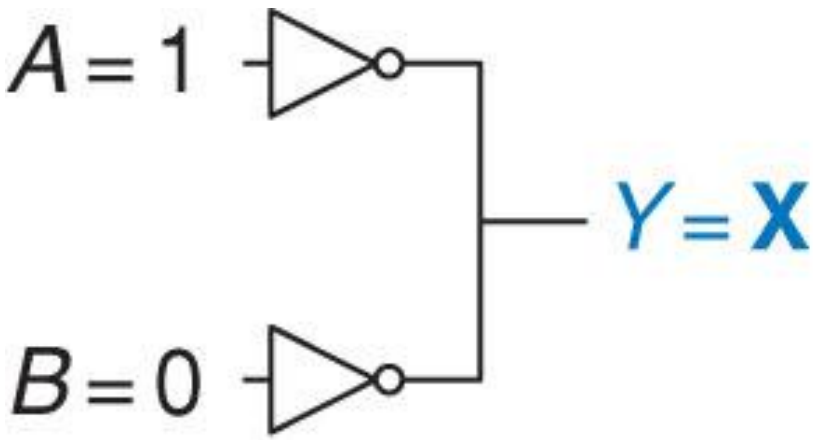
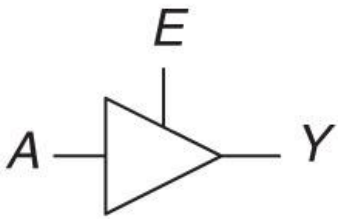


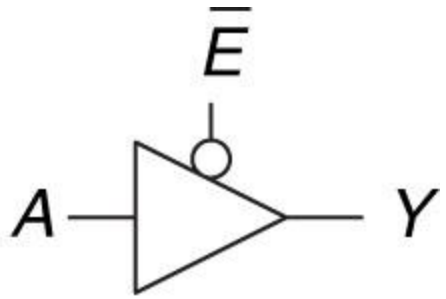

**Figure 2.39 Circuit with contention**

## Tristate Buffer




| E | A | Y |
|---|---|---|
| 0 | 0 | Z |
| 0 | 1 | Z |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Figure 2.40 Tristate buffer**




| $\overline{E}$ | A | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | Z |
| 1 | 1 | Z |

**Figure 2.41 Tristate buffer with active low enable**

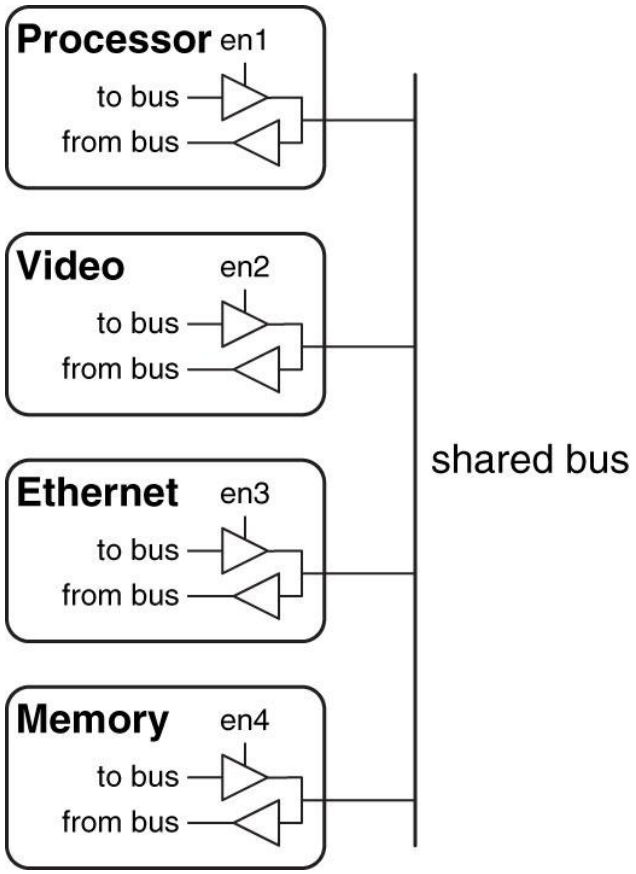
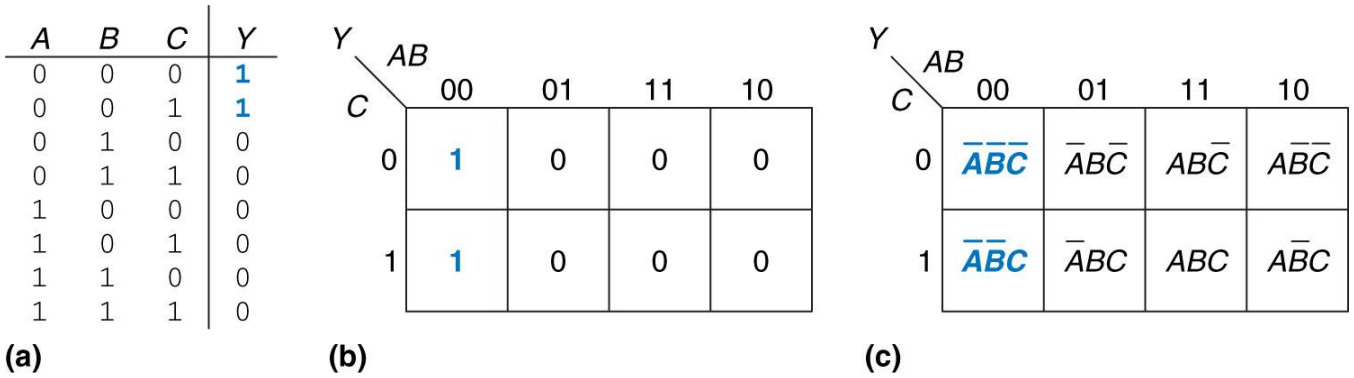



**Figure 2.42 Tristate bus connecting multiple chips**



| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

(a)

| Y, C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |

(b)

| Y, C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | $\bar{A}\bar{B}\bar{C}$ | $\bar{A}B\bar{C}$ | $AB\bar{C}$ | $A\bar{B}\bar{C}$ |
| 1 | $\bar{A}\bar{B}C$ | $\bar{A}BC$ | $ABC$ | $A\bar{B}C$ |

(c)

**Figure 2.43 Three-input function: (a) truth table, (b) K-map, (c) K-map showing minterms**

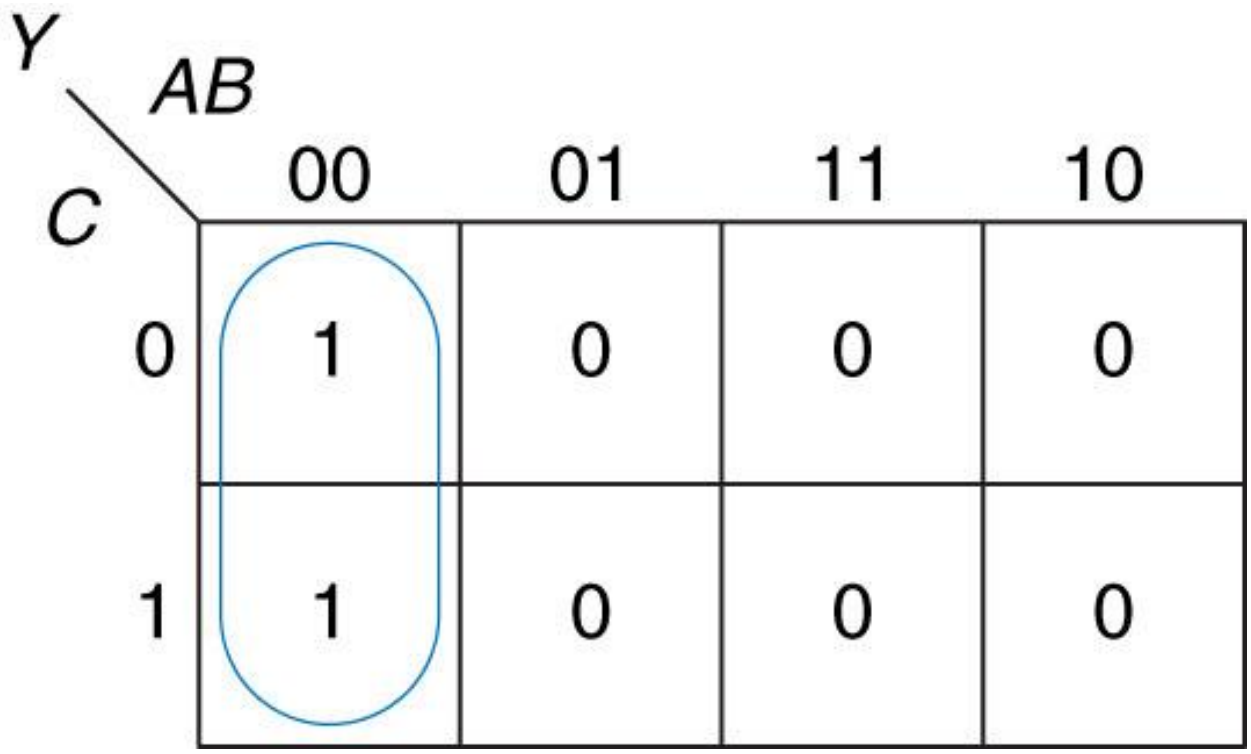



**Figure 2.44 K-map minimization**

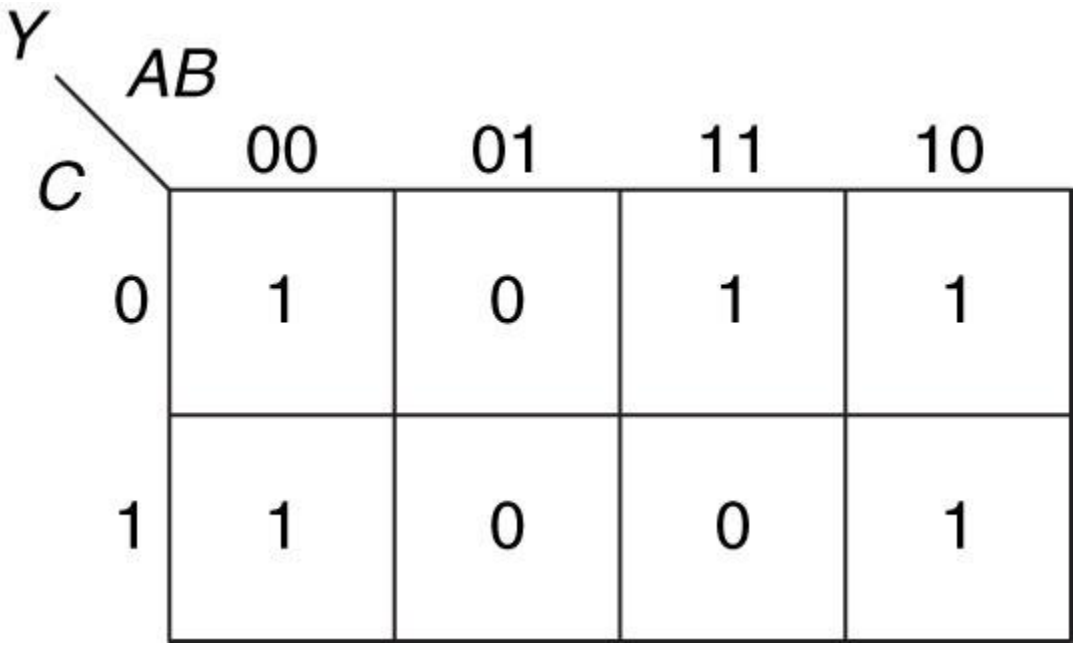



**Figure 2.45 K-map for Example 2.9**

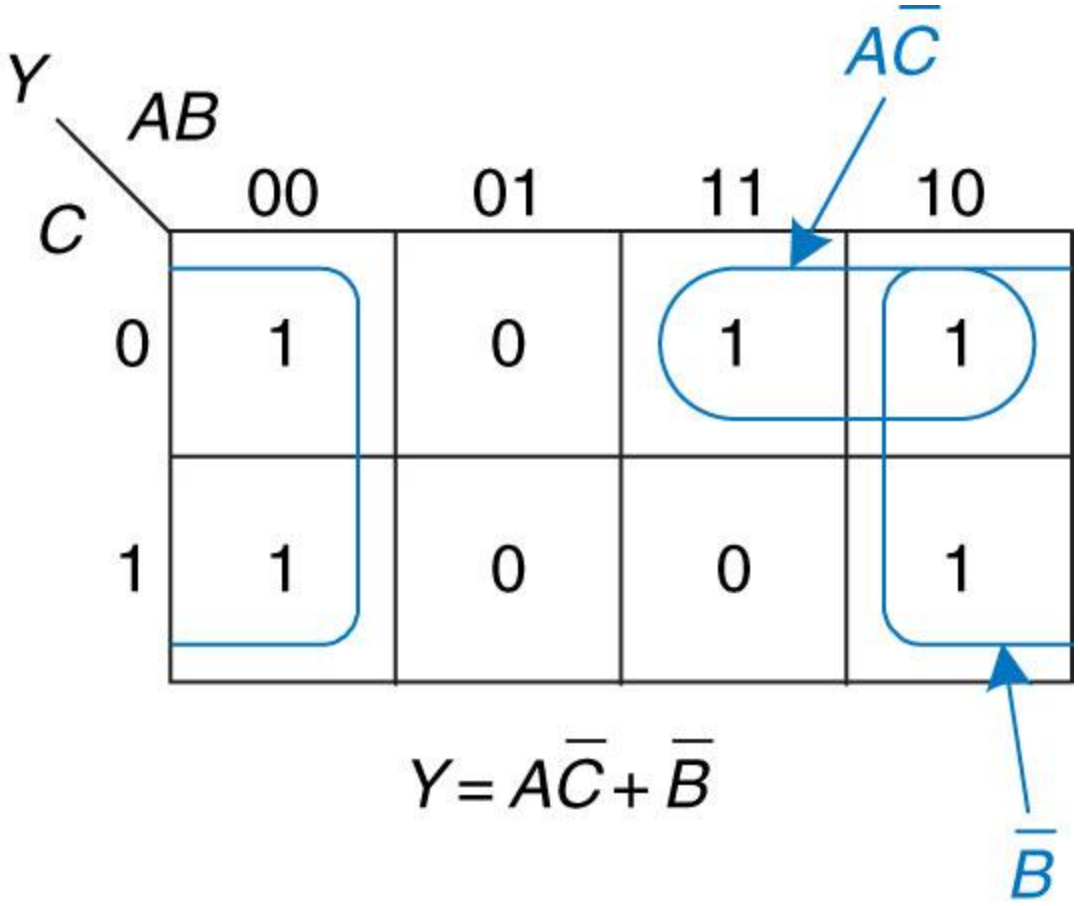



**Figure 2.46 Solution for Example 2.9**

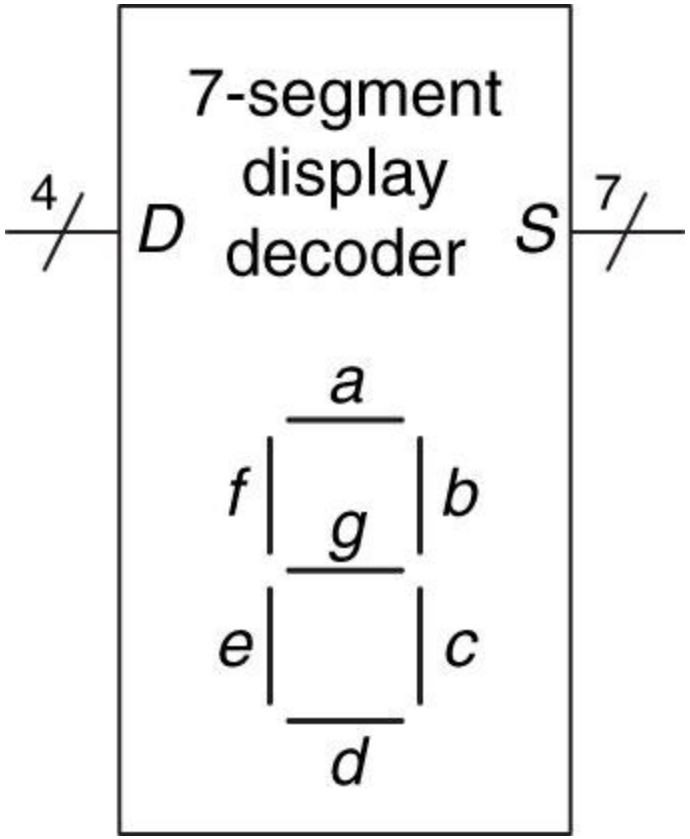



**Figure 2.47 Seven-segment display decoder icon**

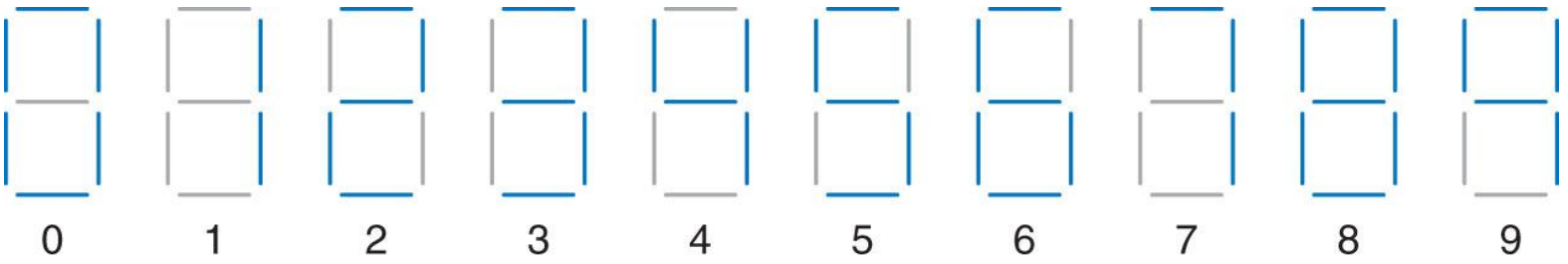



**Figure 2.48 Seven-segment display digits**

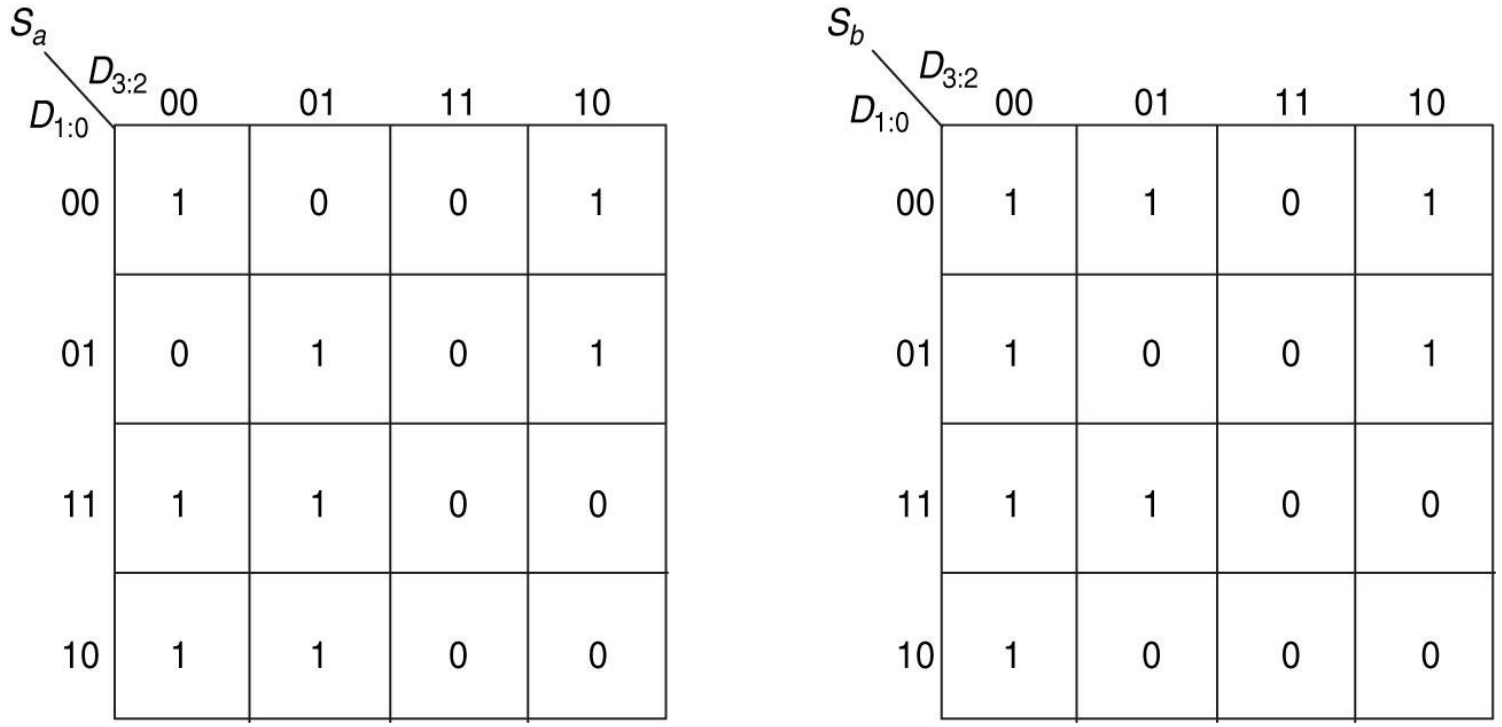



**Figure 2.49 Karnaugh maps for $S_a$ and $S_b$**

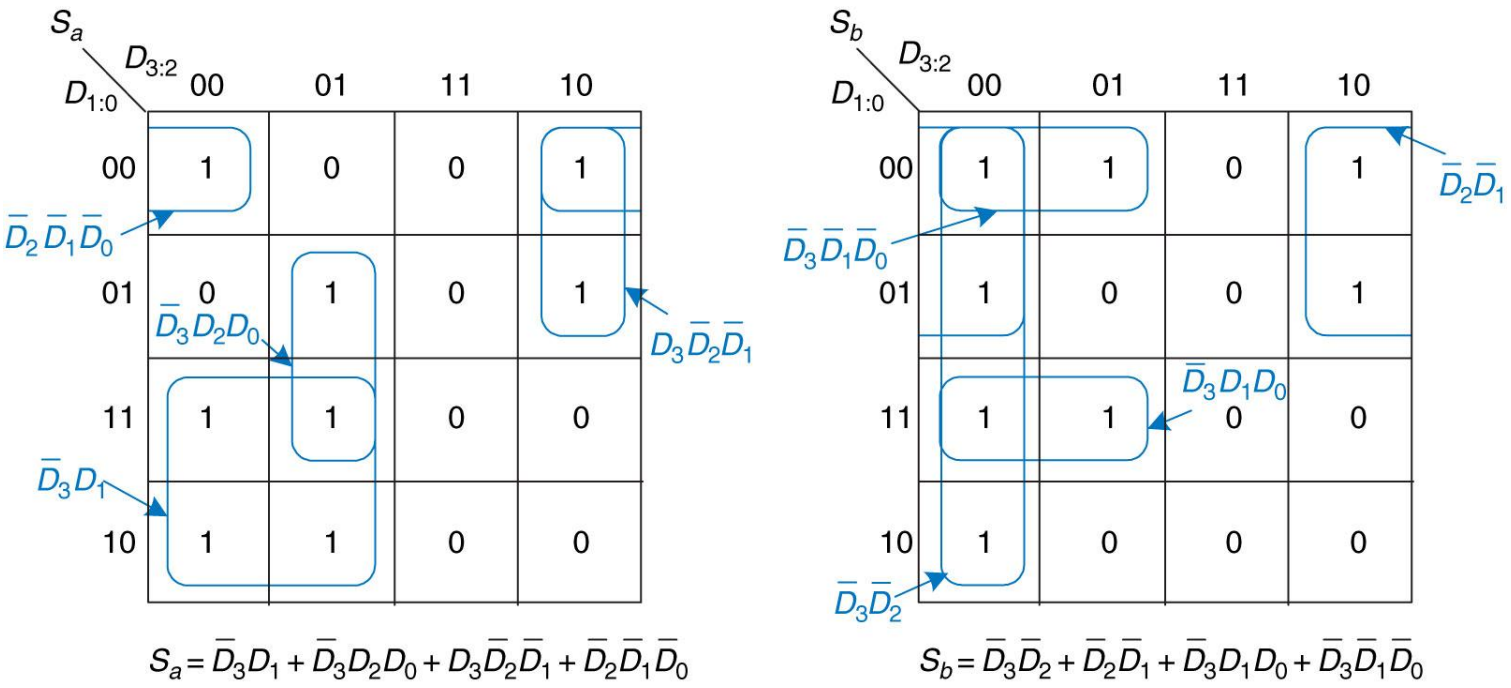



**Figure 2.50 K-map solution for Example 2.10**

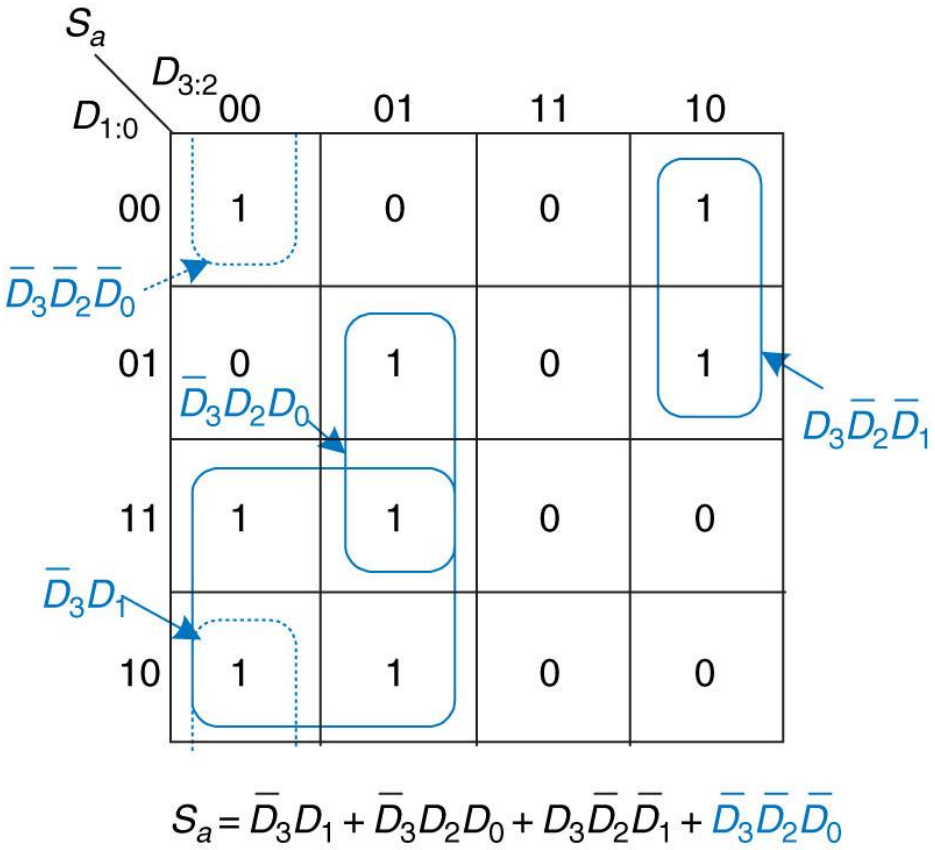



**Figure 2.51 Alternative K-map for $S_a$ showing different set of prime implicants**

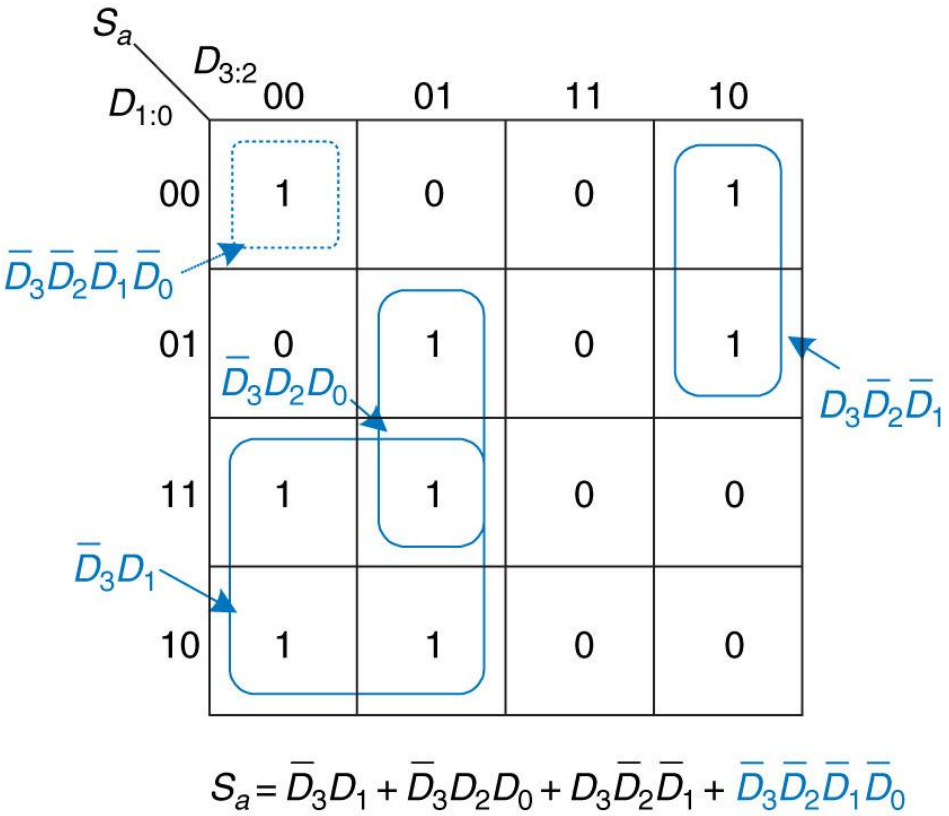



**Figure 2.52 Alternative K-map for $S_a$ showing incorrect nonprime implicant**

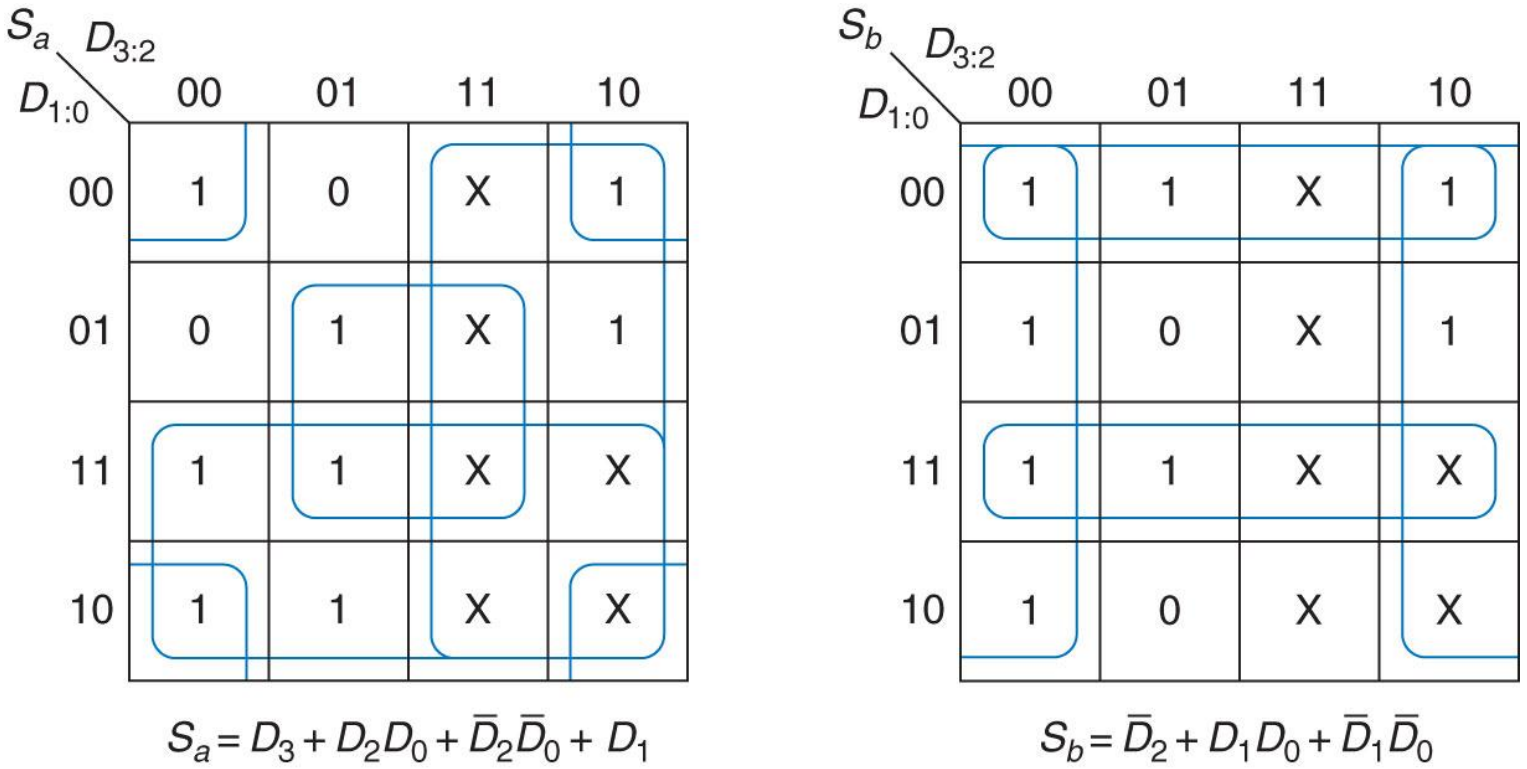
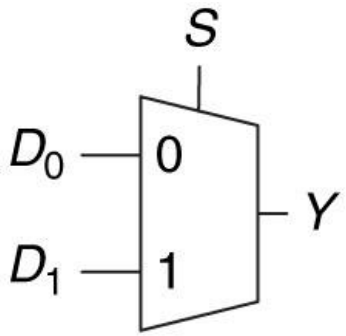
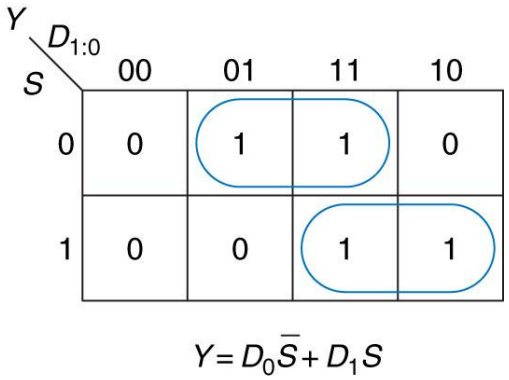



**Figure 2.53 K-map solution with don't cares**




| $S$ | $D_1$ | $D_0$ | $Y$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**Figure 2.54 2:1 multiplexer symbol and truth table**



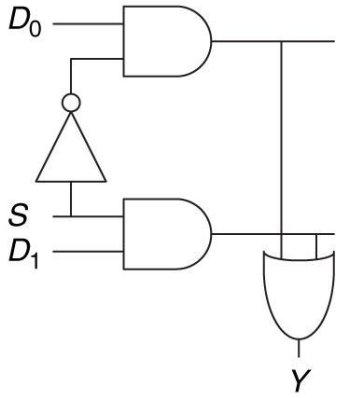




**Figure 2.55 2:1 multiplexer implementation using two-level logic**

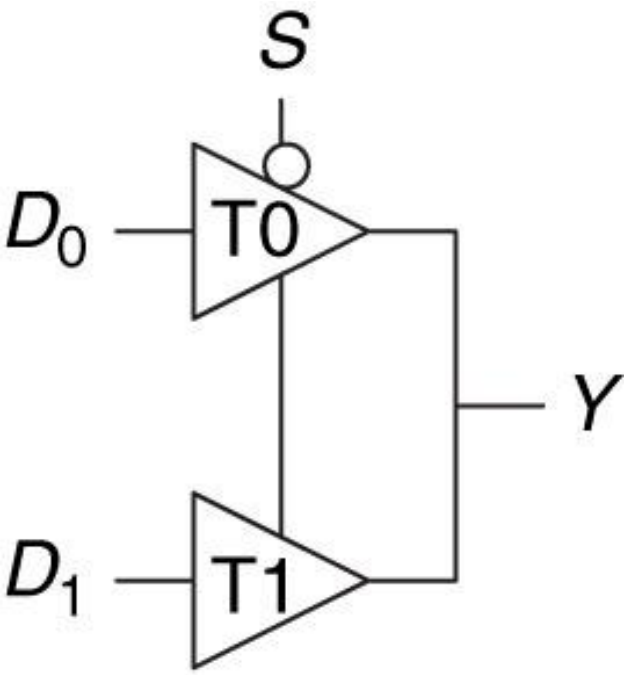



**Figure 2.56 Multiplexer using tristate buffers**

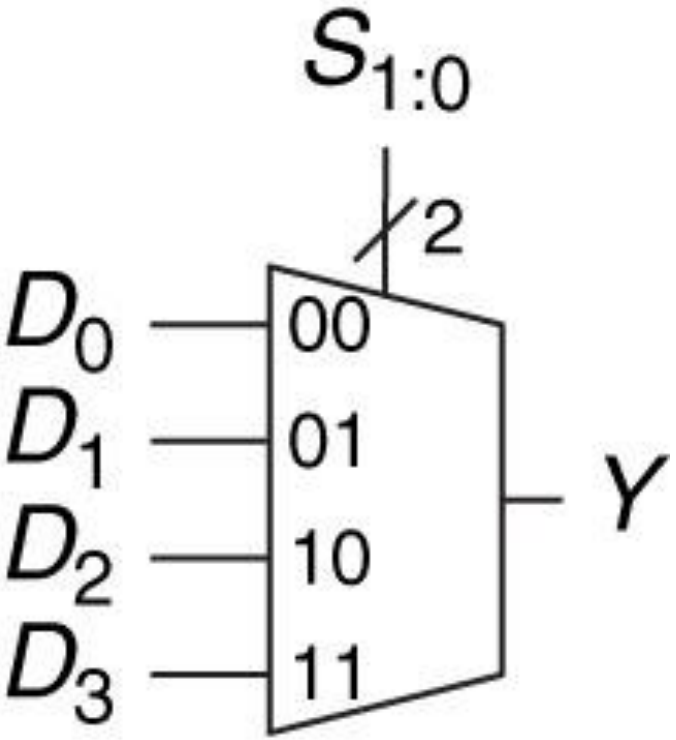



**Figure 2.57 4:1 multiplexer**

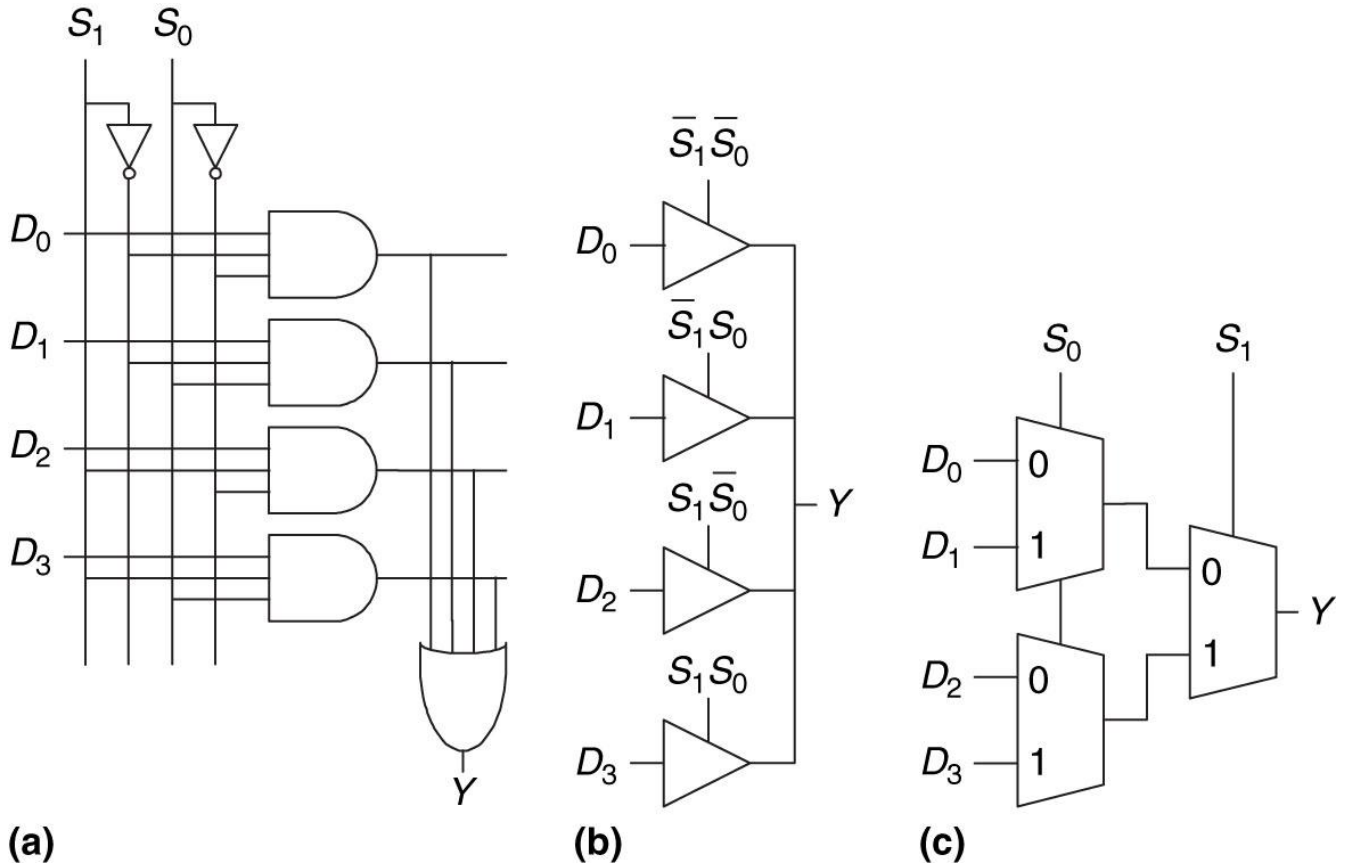



**Figure 2.58 4:1 multiplexer implementations: (a) two-level logic, (b) tristates, (c) hierarchical**

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

$Y = AB$

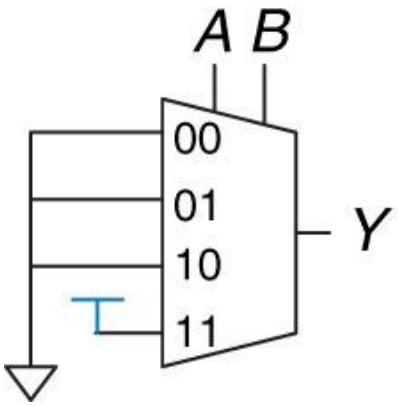



**Figure 2.59 4:1 multiplexer implementation of two-input AND function**

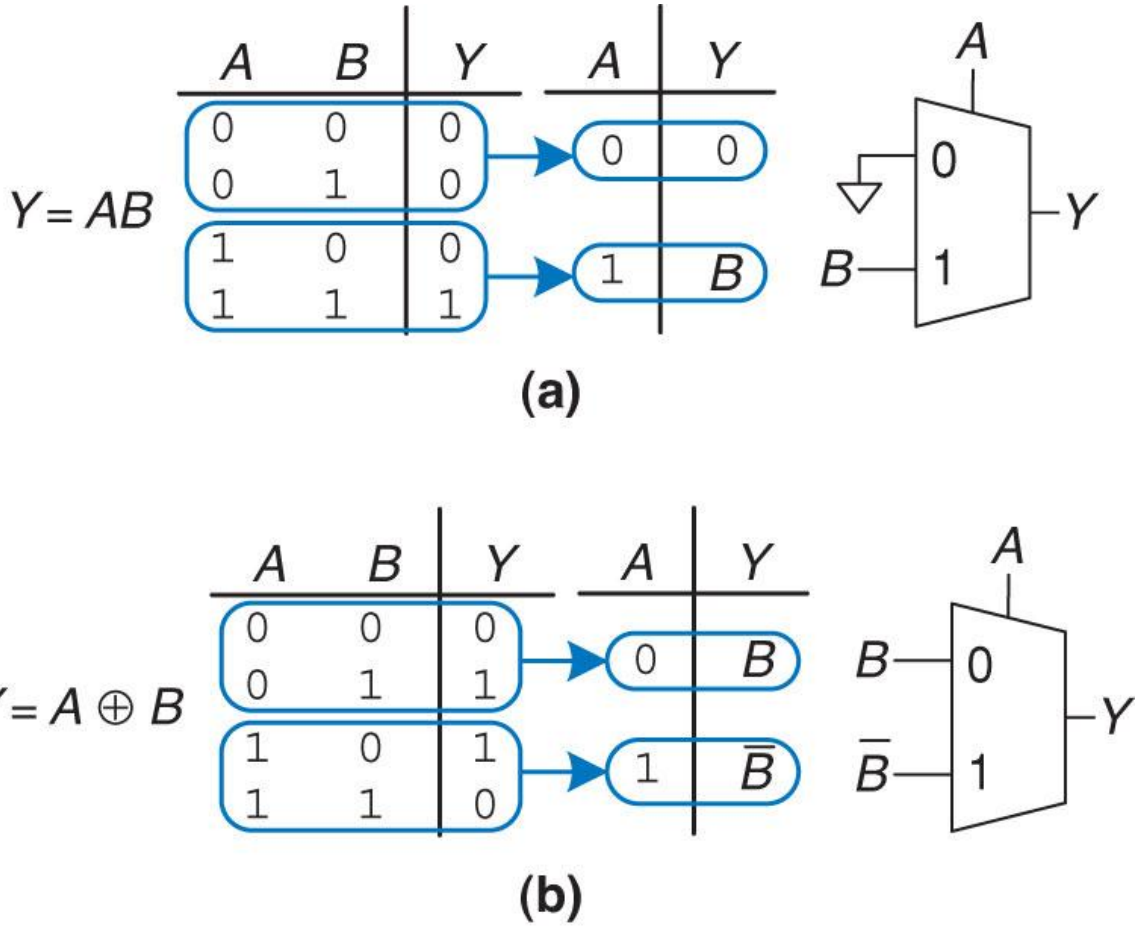



**Figure 2.60 Multiplexer logic using variable inputs**

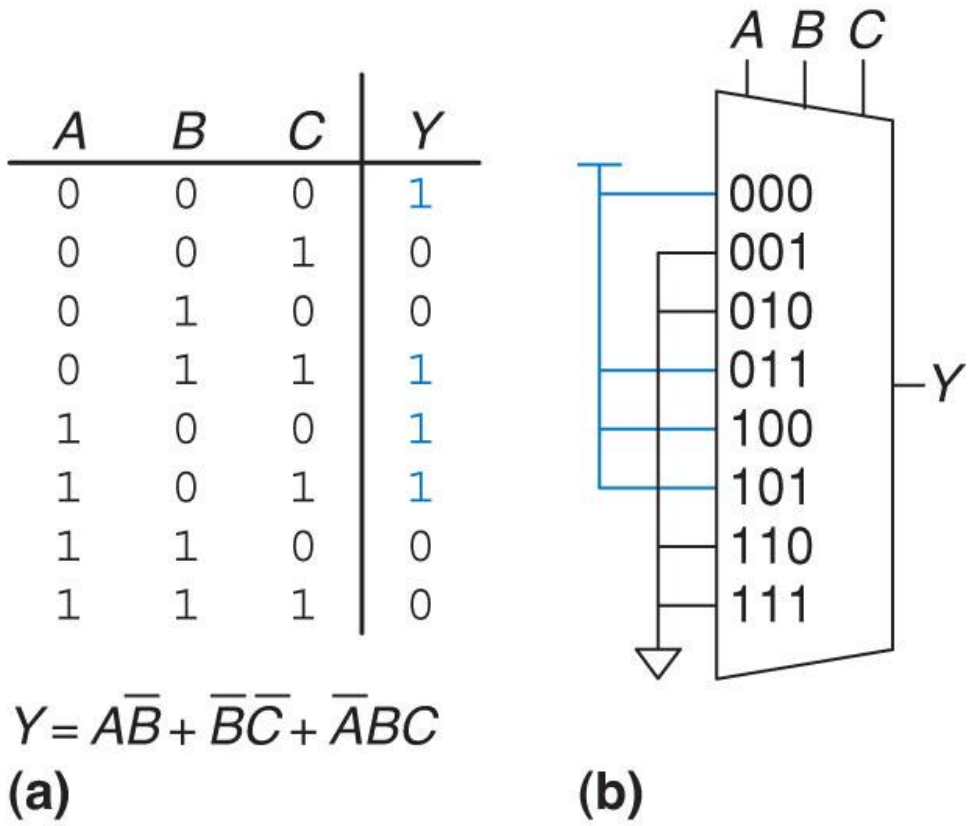



**Figure 2.61 Alyssa's circuit: (a) truth table, (b) 8:1 multiplexer implementation**

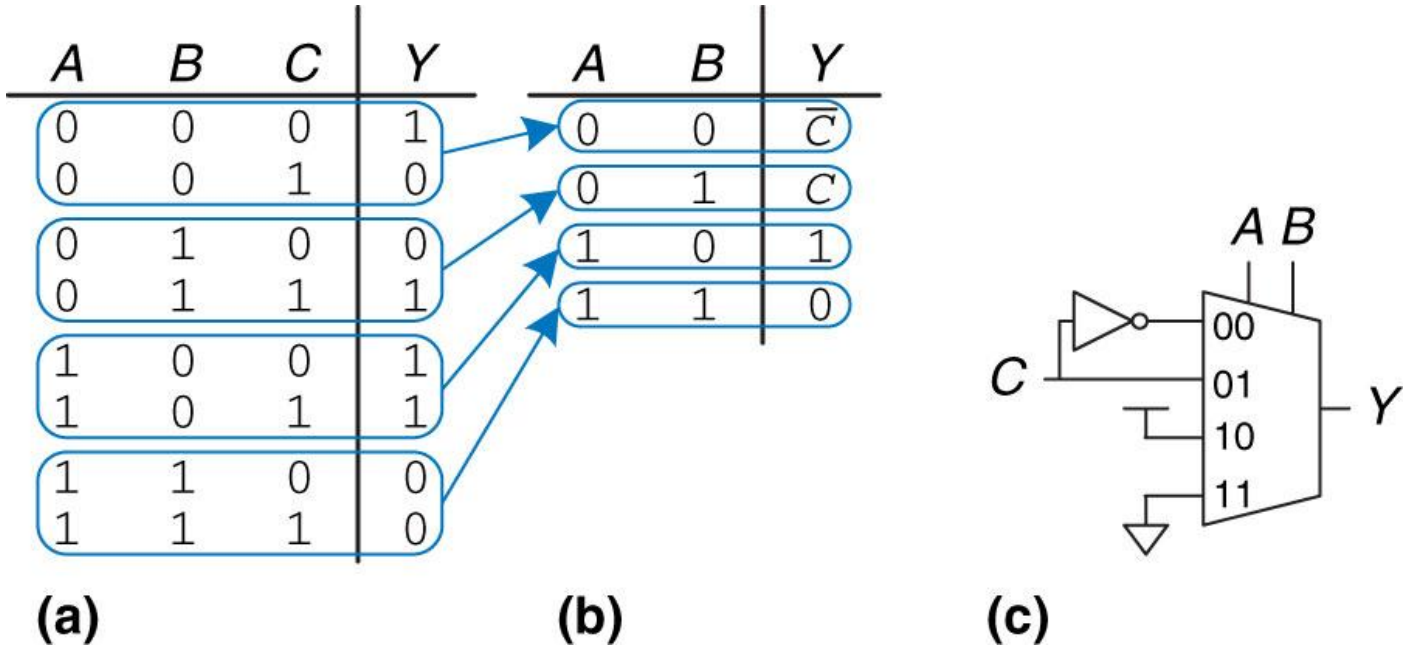
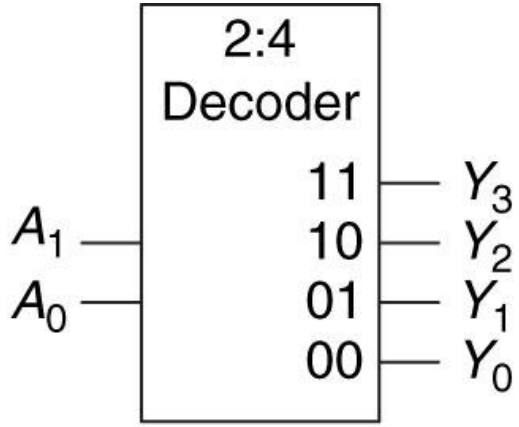



**Figure 2.62 Alyssa's new circuit**




| $A_1$ | $A_0$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |

**Figure 2.63 2:4 decoder**

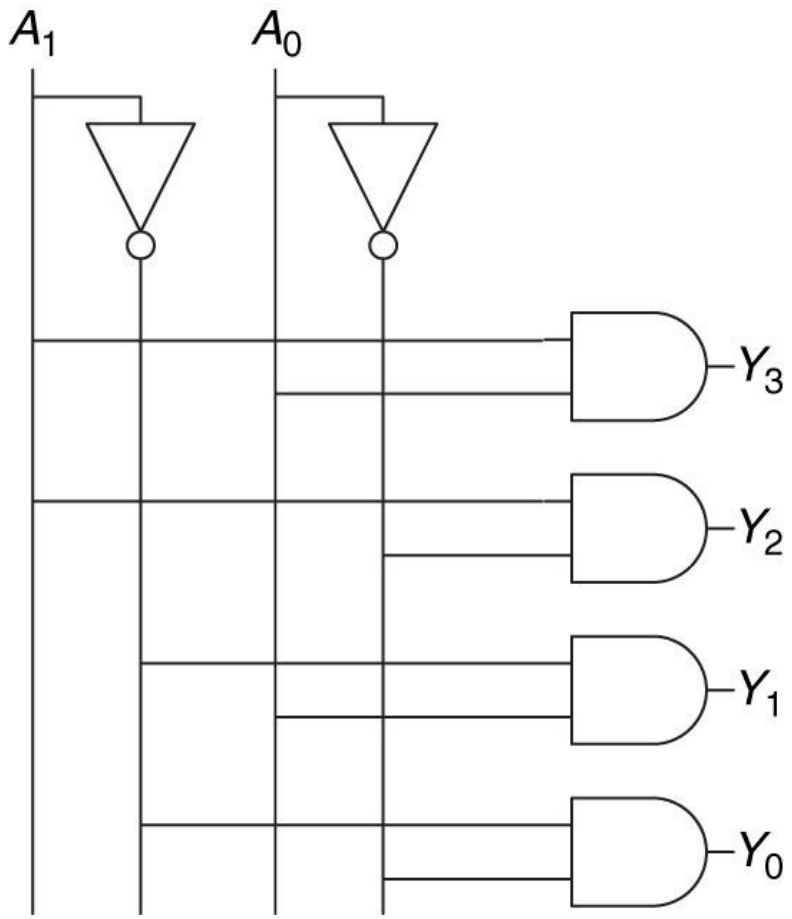



**Figure 2.64 2:4 decoder implementation**

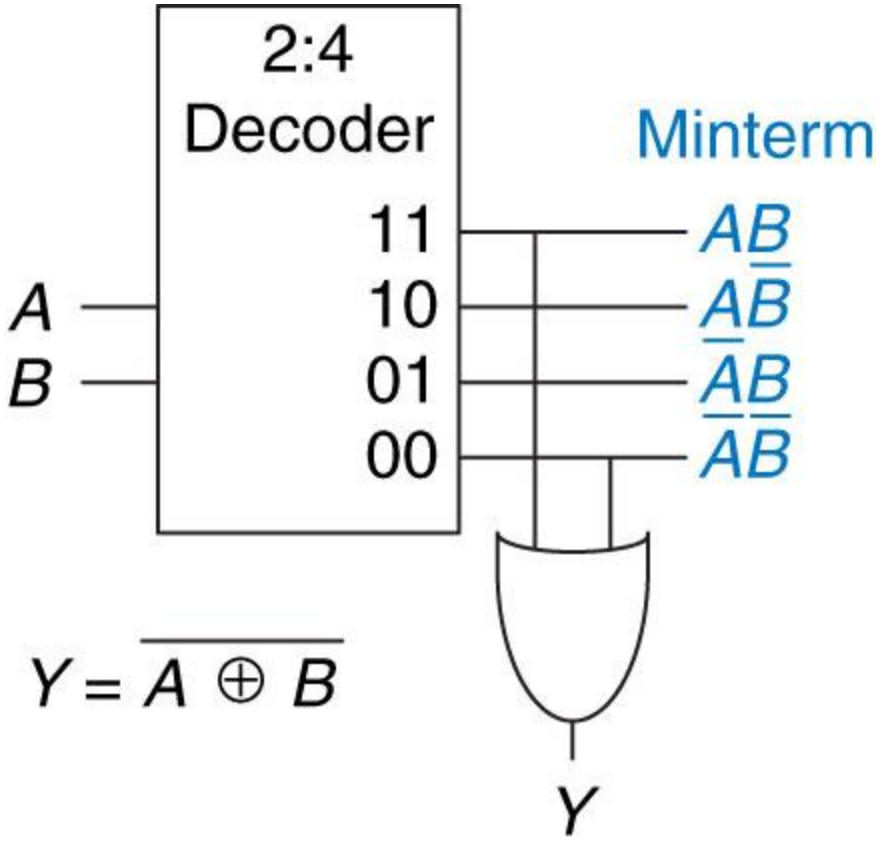



**Figure 2.65 Logic function using decoder**

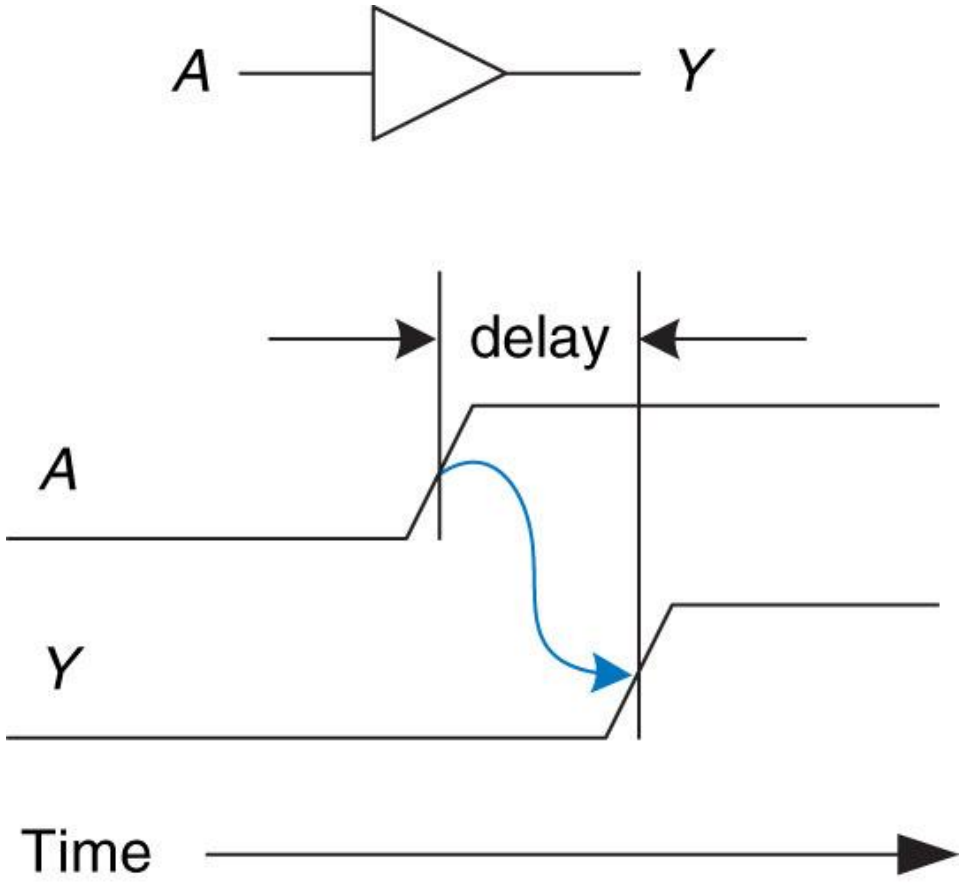



**Figure 2.66 Circuit delay**

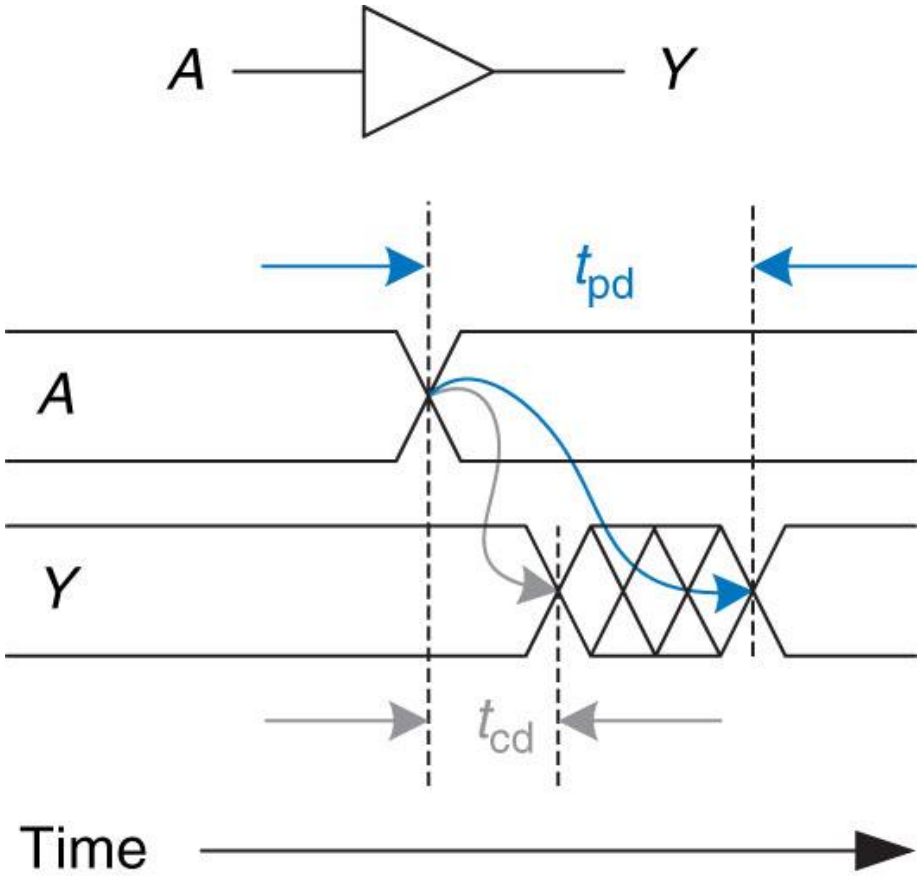



**Figure 2.67 Propagation and contamination delay**

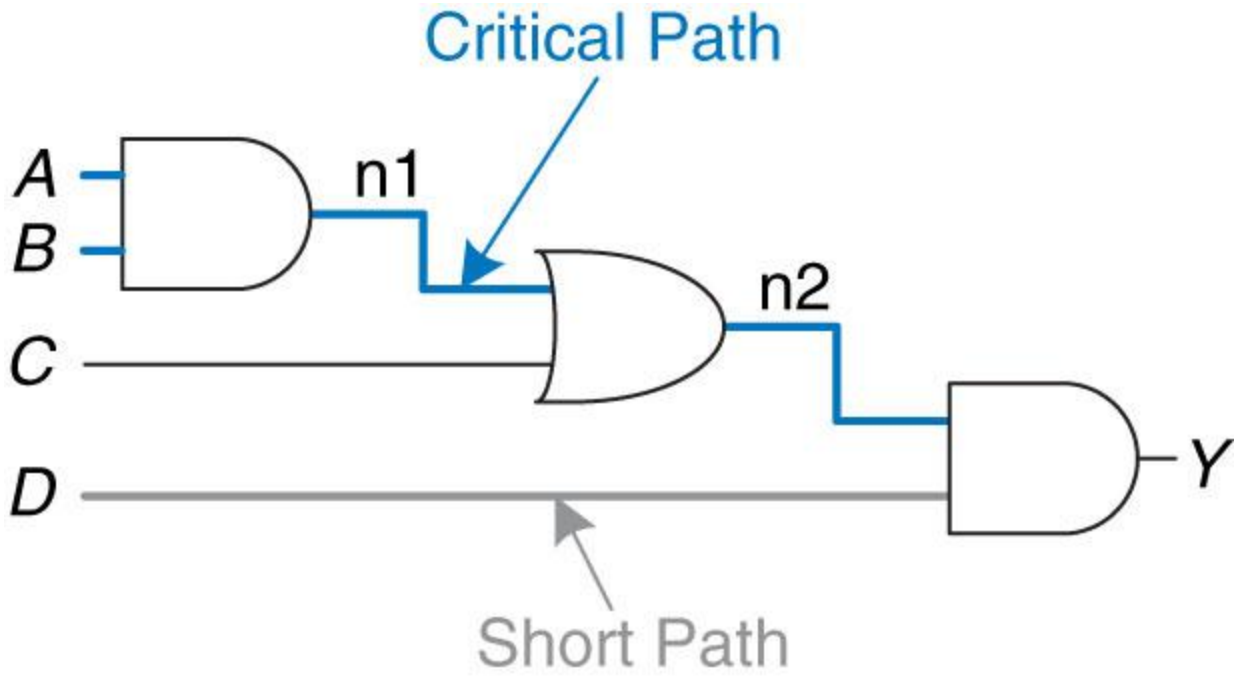



**Figure 2.68 Short path and critical path**

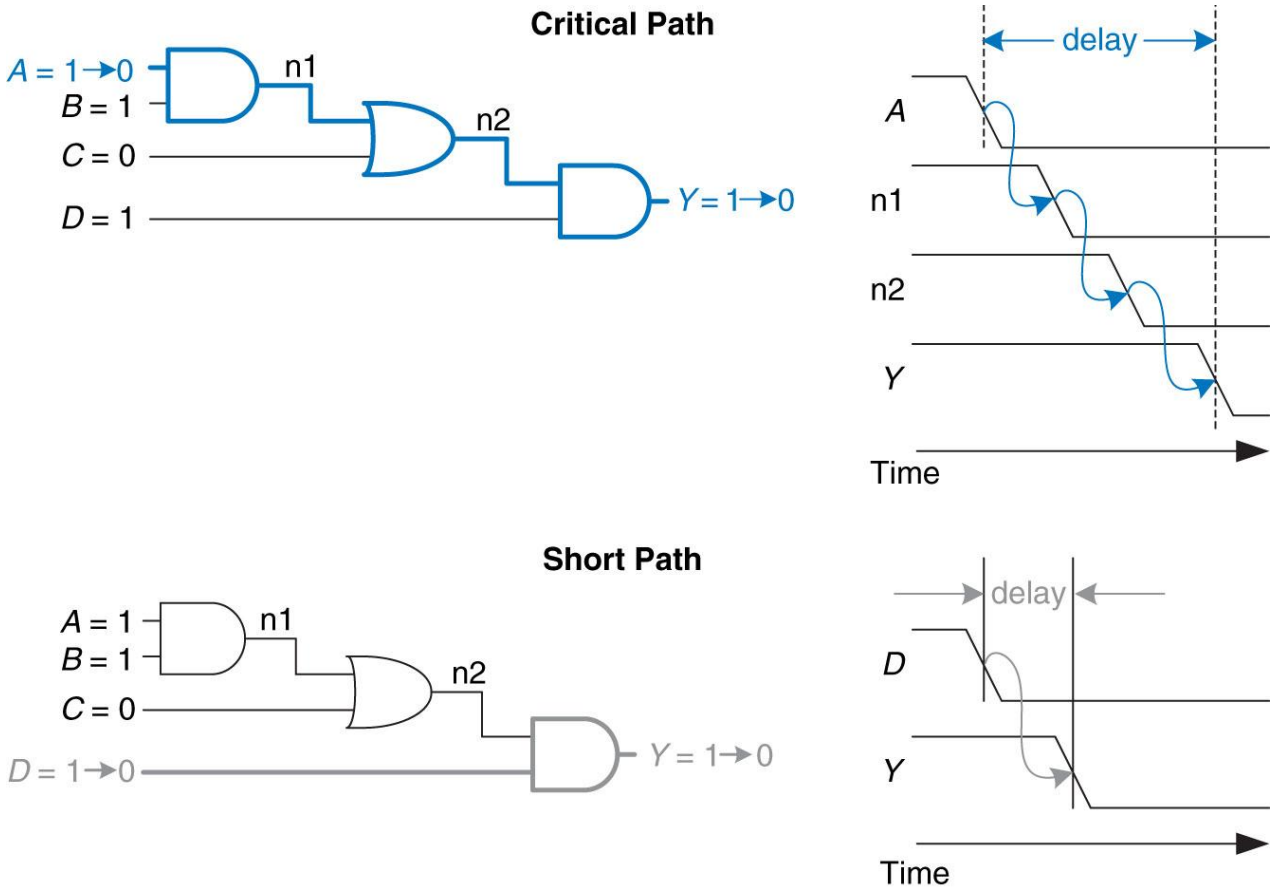



**Figure 2.69 Critical and short path waveforms**

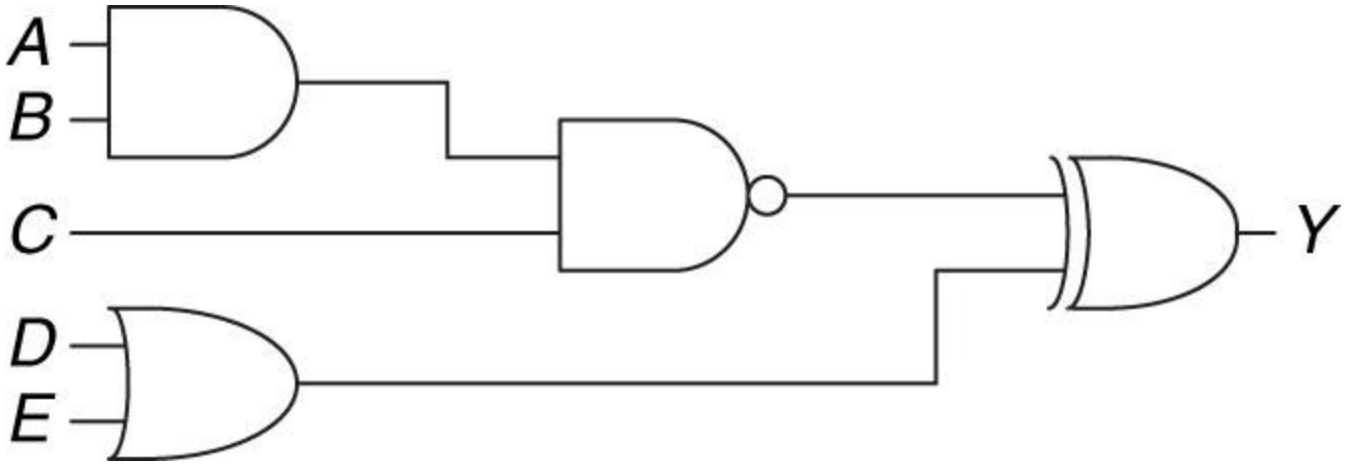



**Figure 2.70 Ben's circuit**

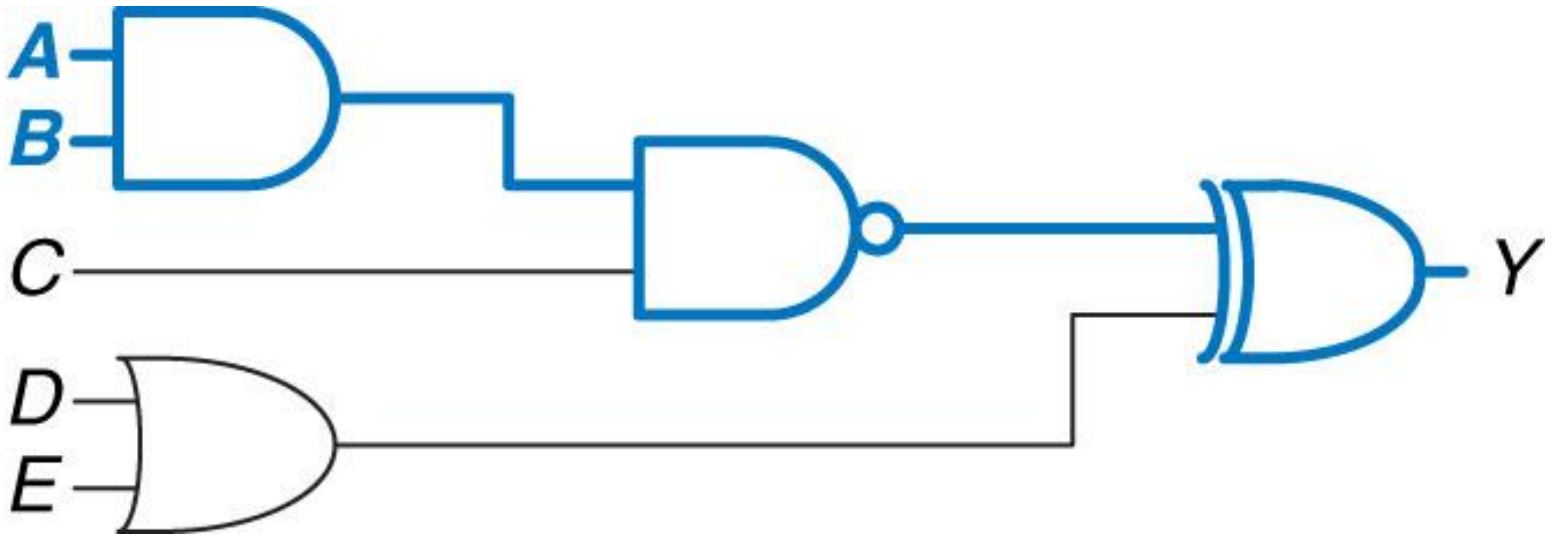



**Figure 2.71 Ben's critical path**

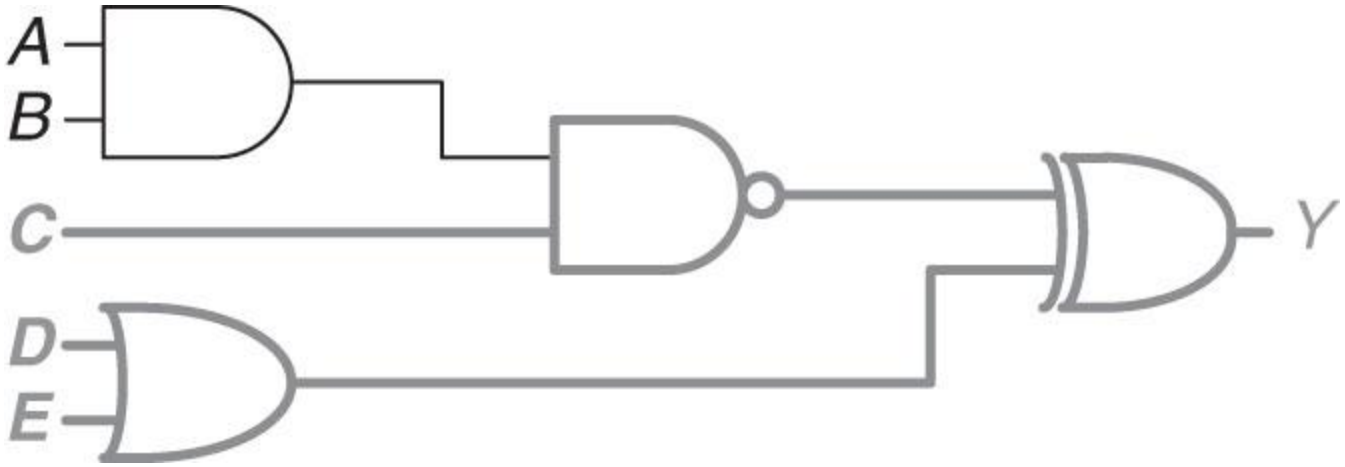



**Figure 2.72 Ben's shortest path**

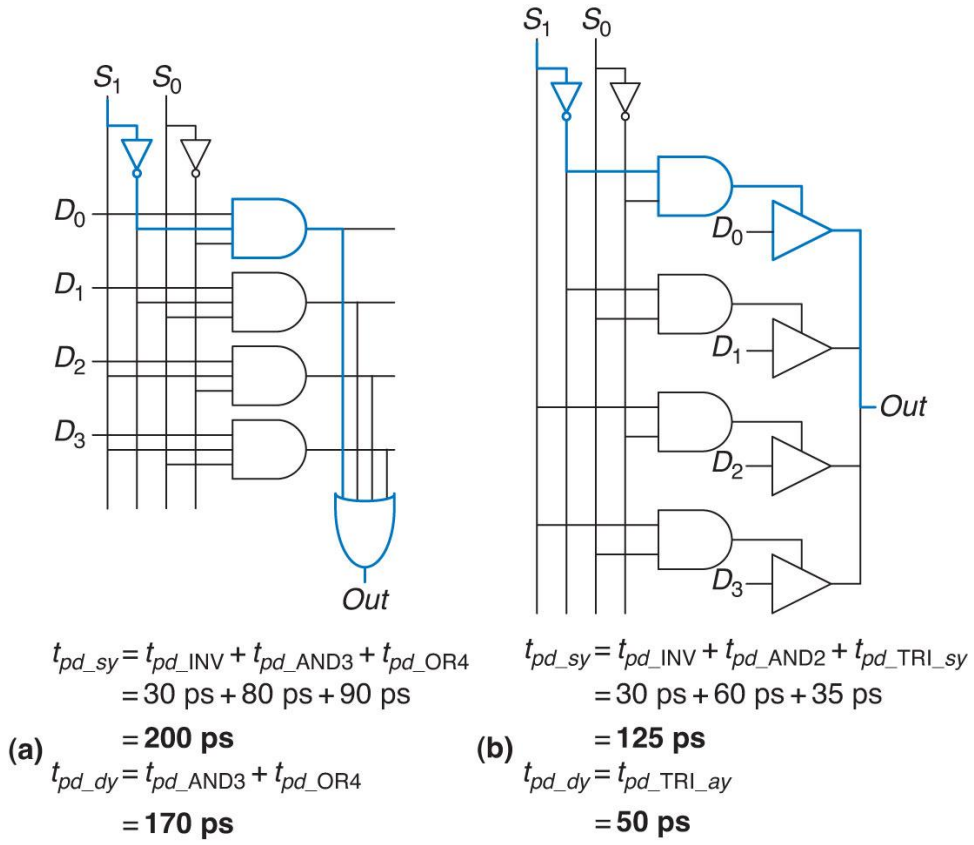
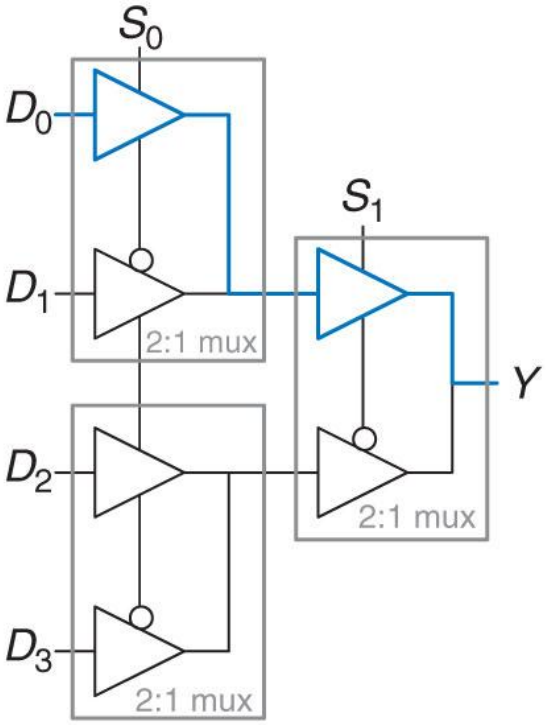



**Figure 2.73 4:1 multiplexer propagation delays: (a) two-level logic, (b) tristate**




$$t_{pd\_s0y} = t_{pd\_TRLSY} + t_{pd\_TRI\_AY} = \mathbf{85\ ns}$$

$$t_{pd\_dy} = 2\ t_{pd\_TRI\_AY} = \mathbf{100\ ns}$$

**Figure 2.74 4:1 multiplexer propagation delays: hierarchical using 2:1 multiplexers**

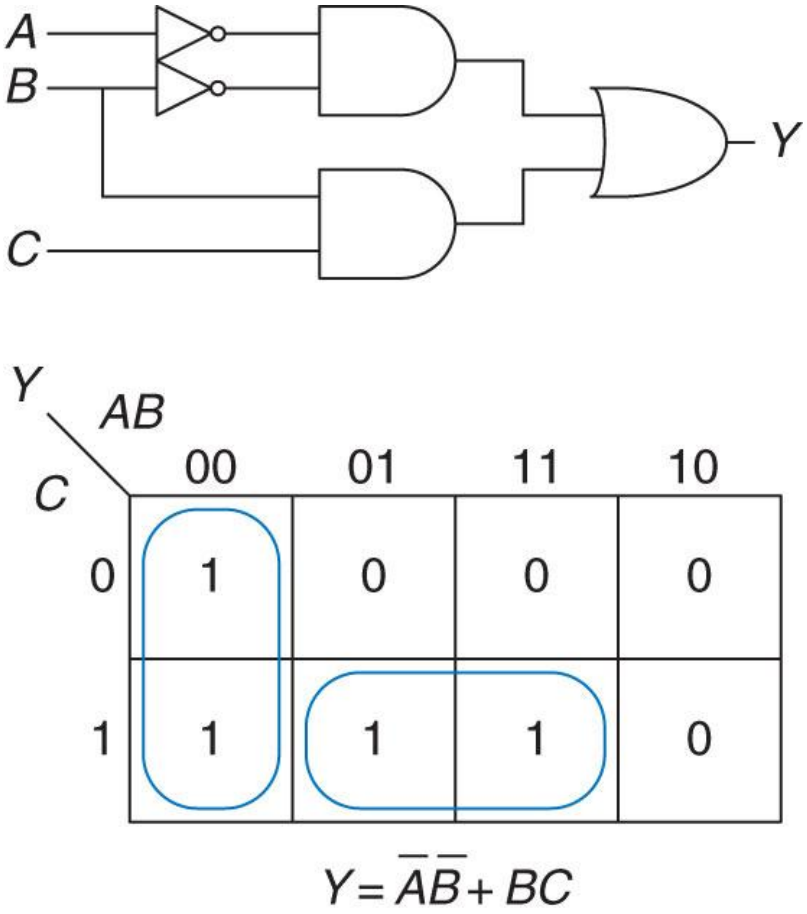



**Figure 2.75 Circuit with a glitch**

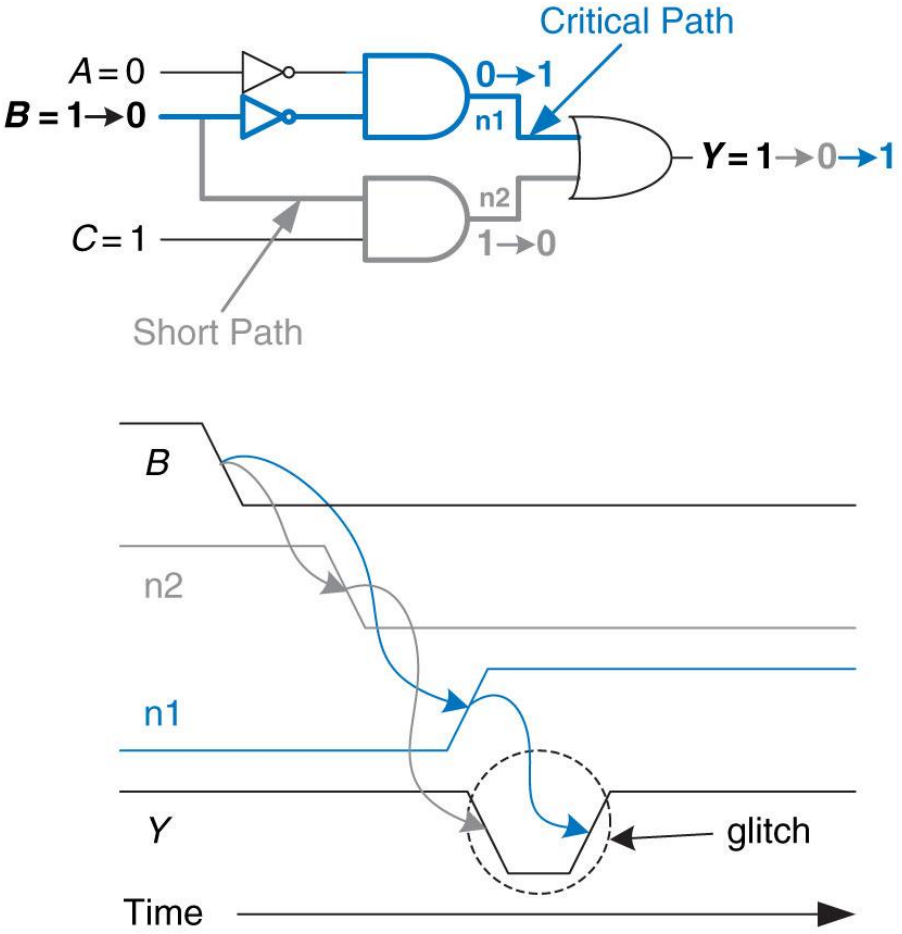



**Figure 2.76 Timing of a glitch**

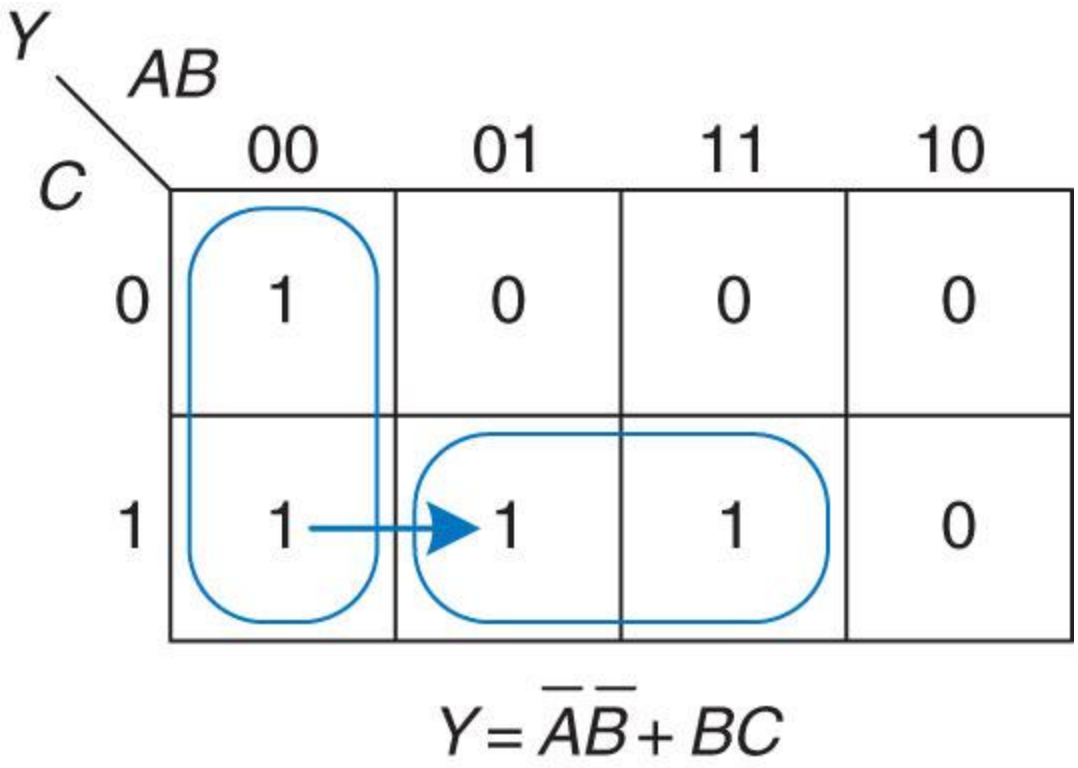



**Figure 2.77 Input change crosses implicant boundary**

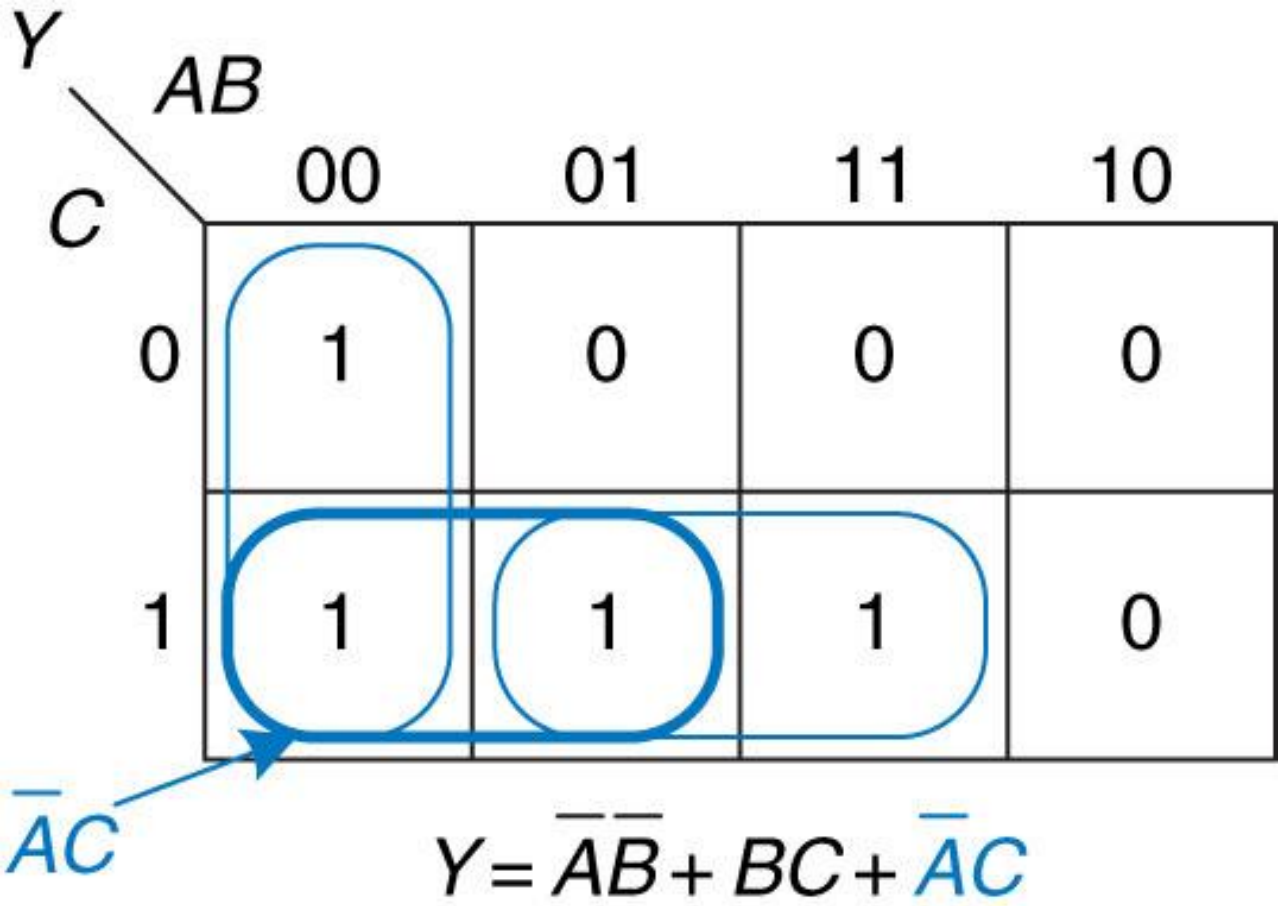



**Figure 2.78 K-map without glitch**

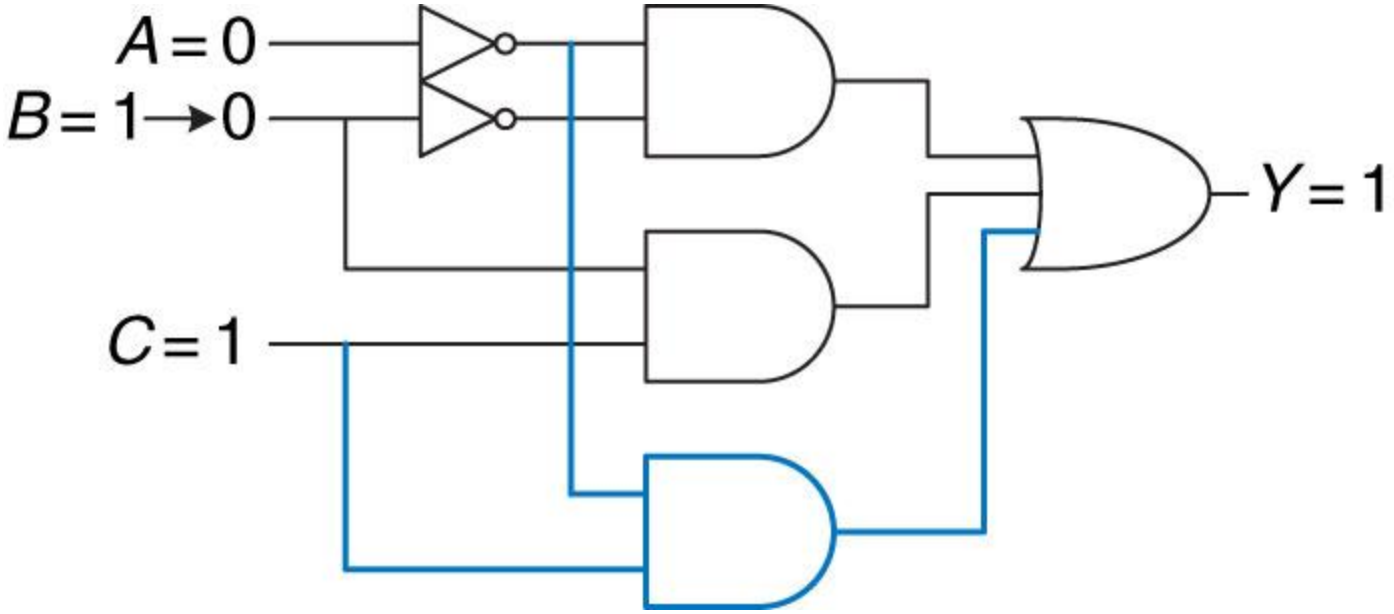



**Figure 2.79 Circuit without glitch**

**(a)**

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**(b)**

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**(c)**

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**(d)**

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

**(e)**

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Figure 2.80 Truth tables for Exercises 2.1 and 2.3**

**(a)**

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**(b)**

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**(c)**

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**(d)**

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**(e)**

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Figure 2.81 Truth tables for Exercises 2.2 and 2.4**

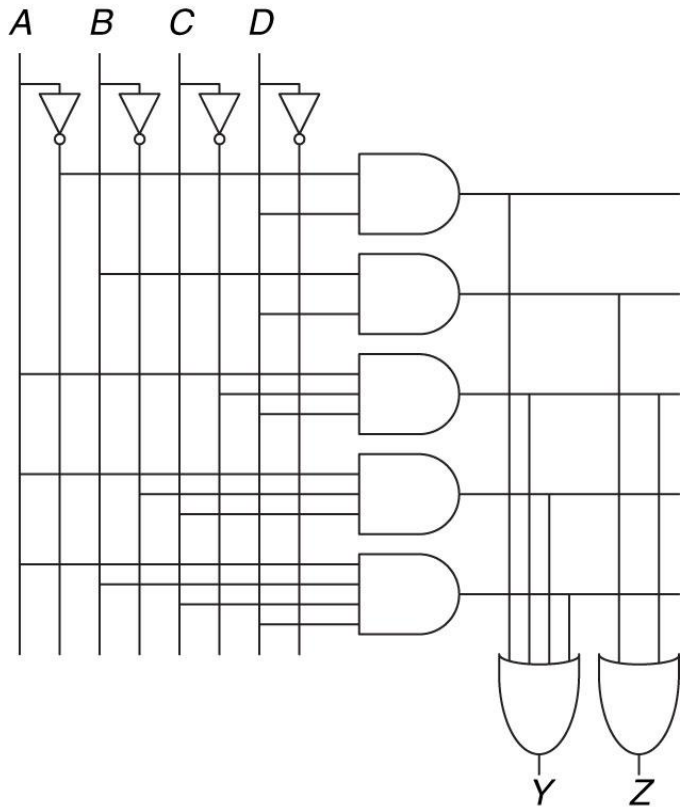



**Figure 2.82 Circuit schematic**

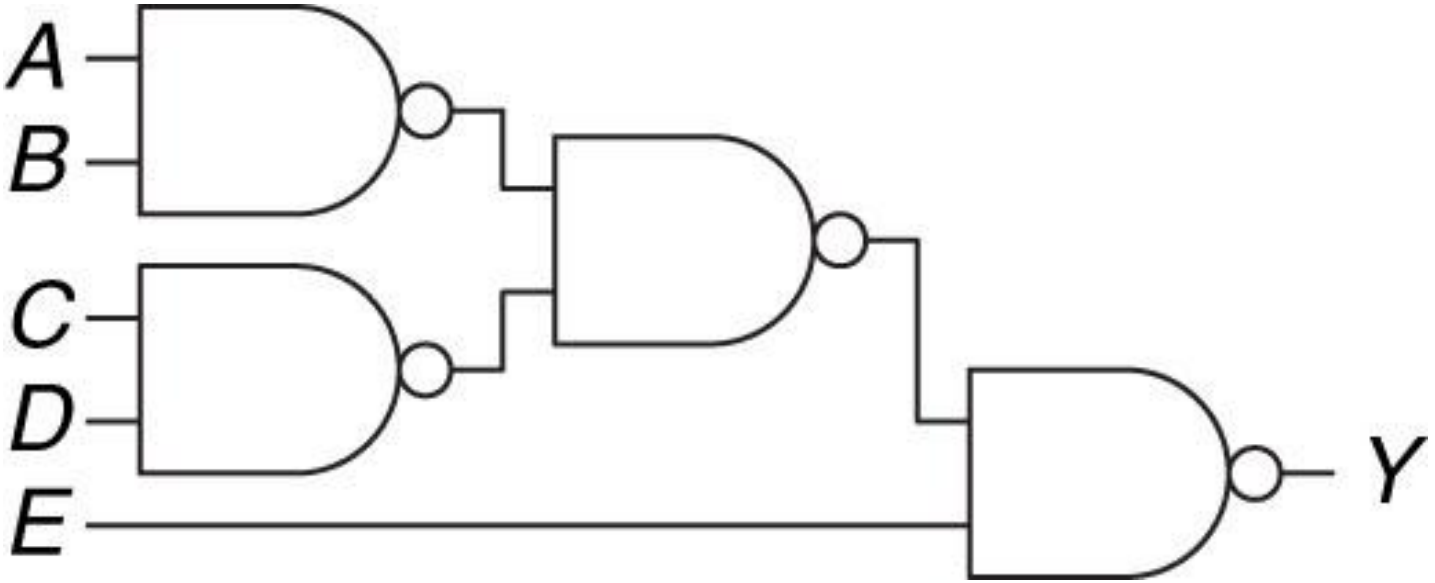



**Figure 2.83 Circuit schematic**

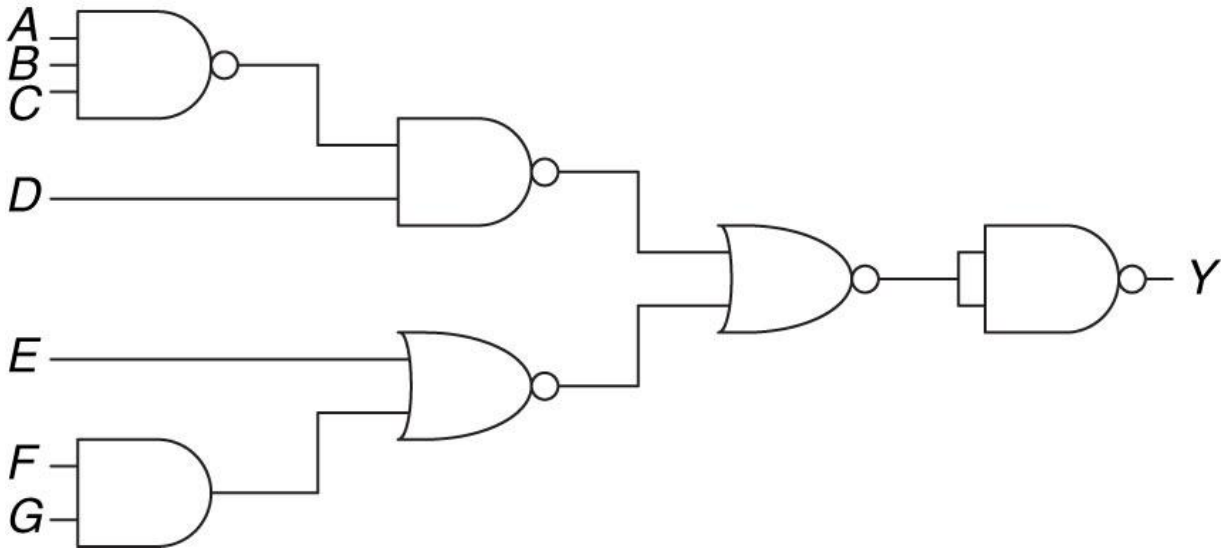



**Figure 2.84 Circuit schematic**

| *A* | *B* | *C* | *D* | *Y* |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X |
| 0 | 0 | 0 | 1 | X |
| 0 | 0 | 1 | 0 | X |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | X |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | X |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | X |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | X |
| 1 | 1 | 1 | 1 | 1 |

**Figure 2.85 Truth table for Exercise 2.28**

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | X |
| 0 | 0 | 1 | 1 | X |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | X |
| 0 | 1 | 1 | 0 | X |
| 0 | 1 | 1 | 1 | X |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | X |
| 1 | 1 | 1 | 1 | 1 |

**Figure 2.86 Truth table for Exercise 2.31**

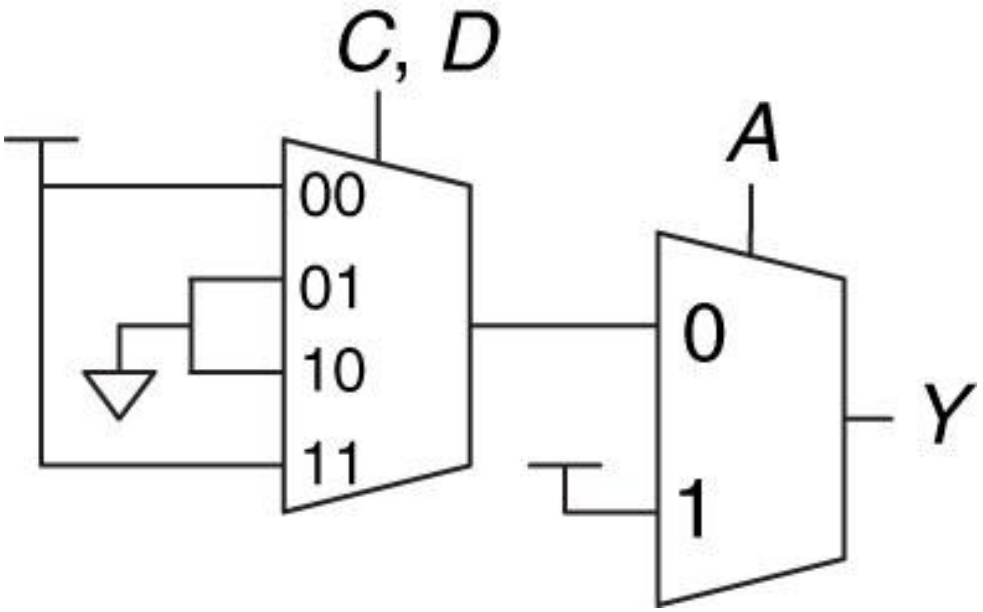



**Figure 2.87 Multiplexer circuit**

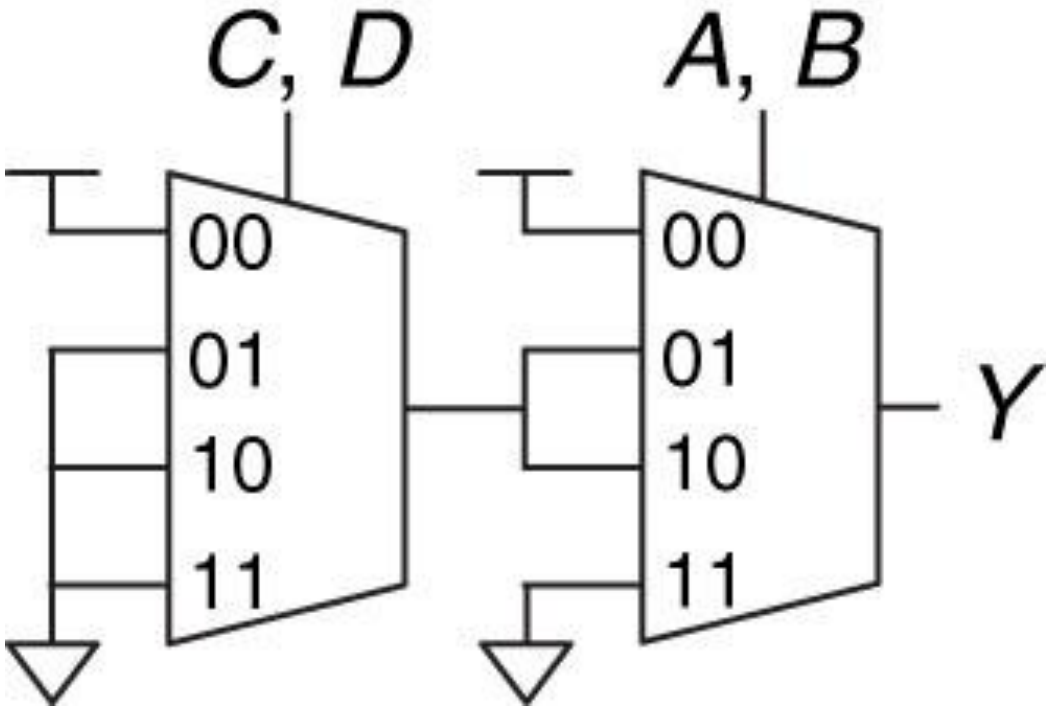



**Figure 2.88 Multiplexer circuit**

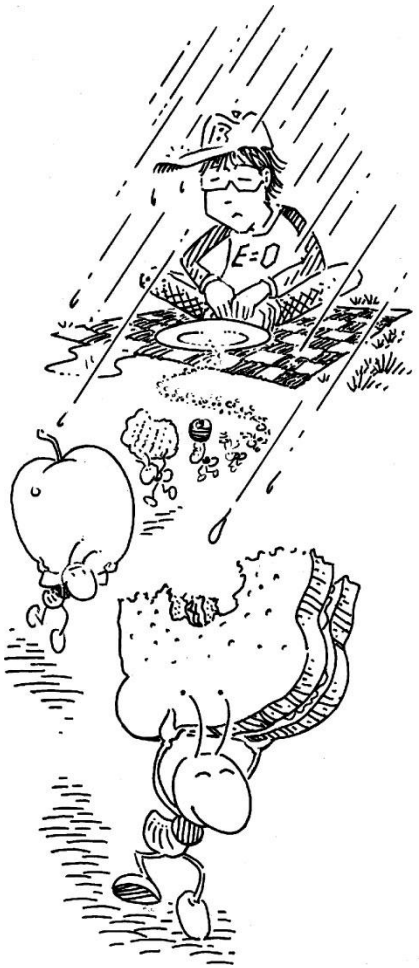
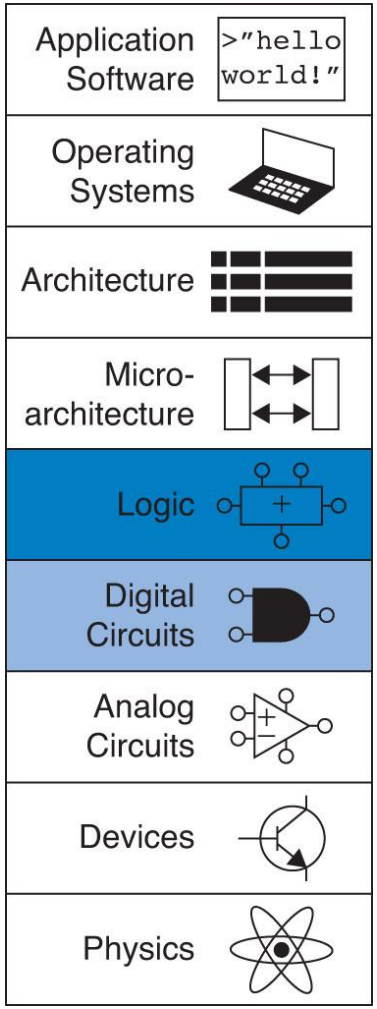



**Figure M 01**

**Figure M 02**




**UNN Figure 1**