Chapter 3

Sequential Logic Design

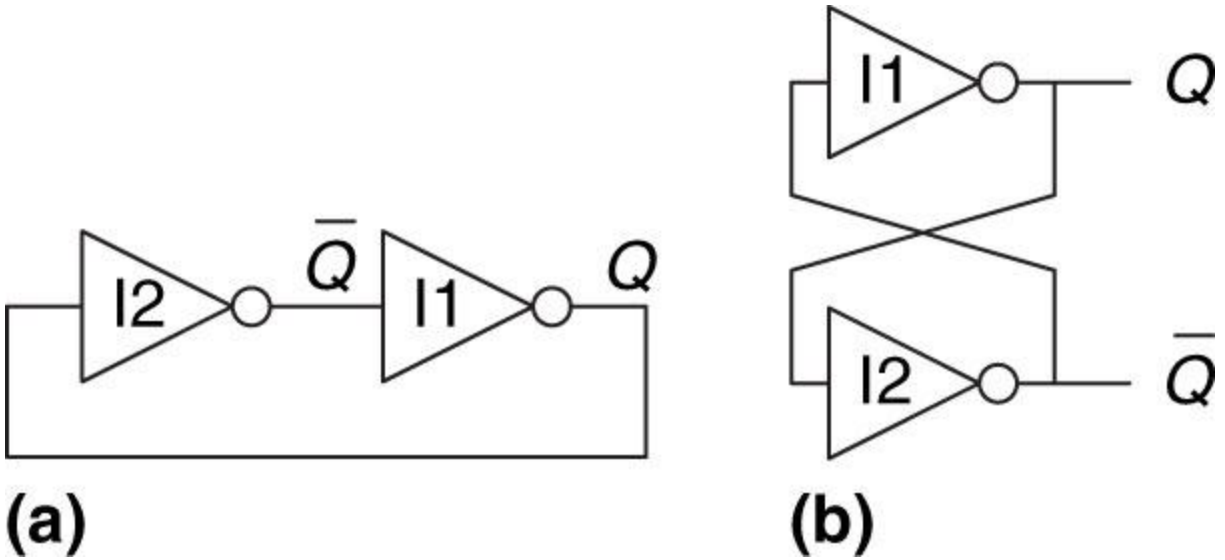


Figure 3.1 Cross-coupled inverter pair

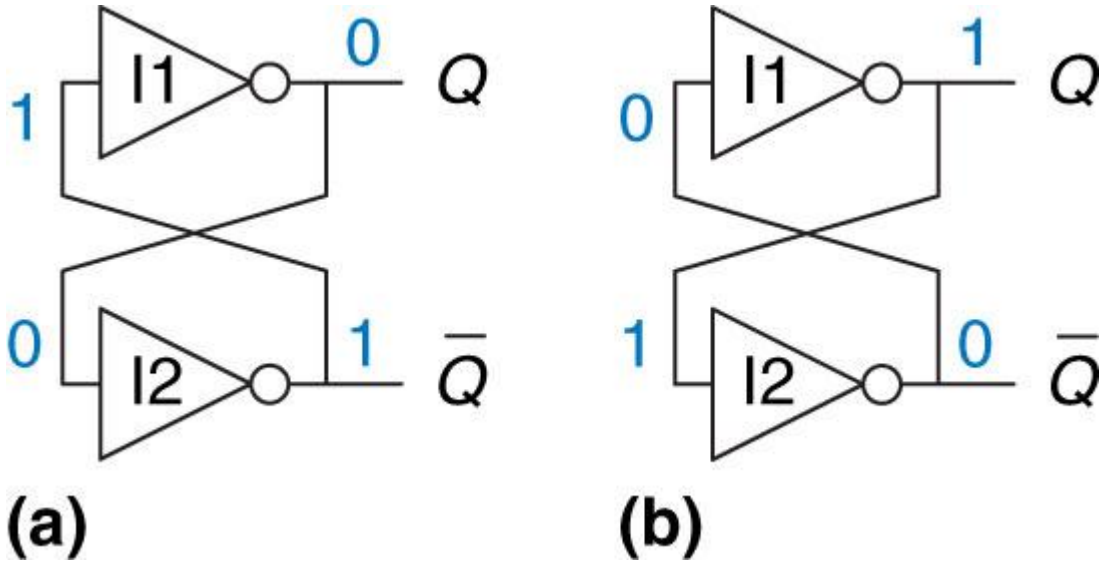


Figure 3.2 Bistable operation of cross-coupled inverters

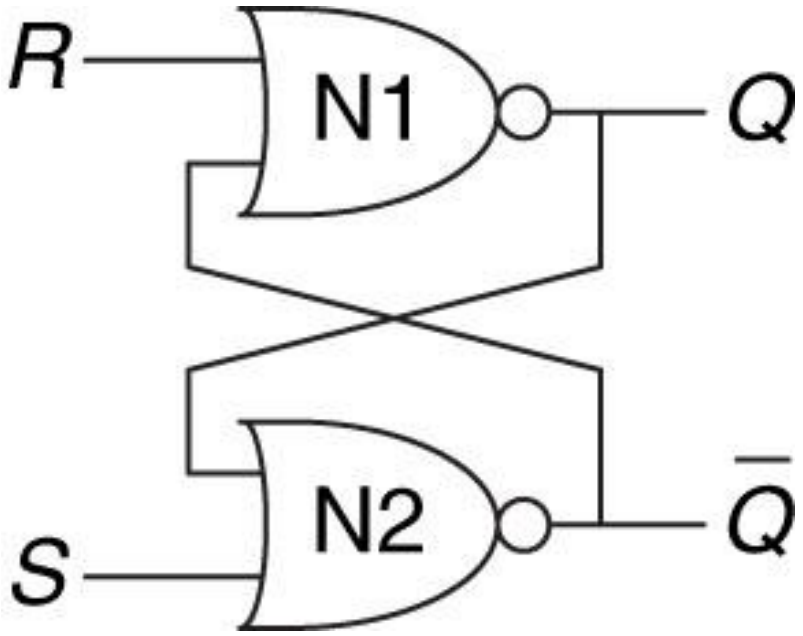


Figure 3.3 SR latch schematic

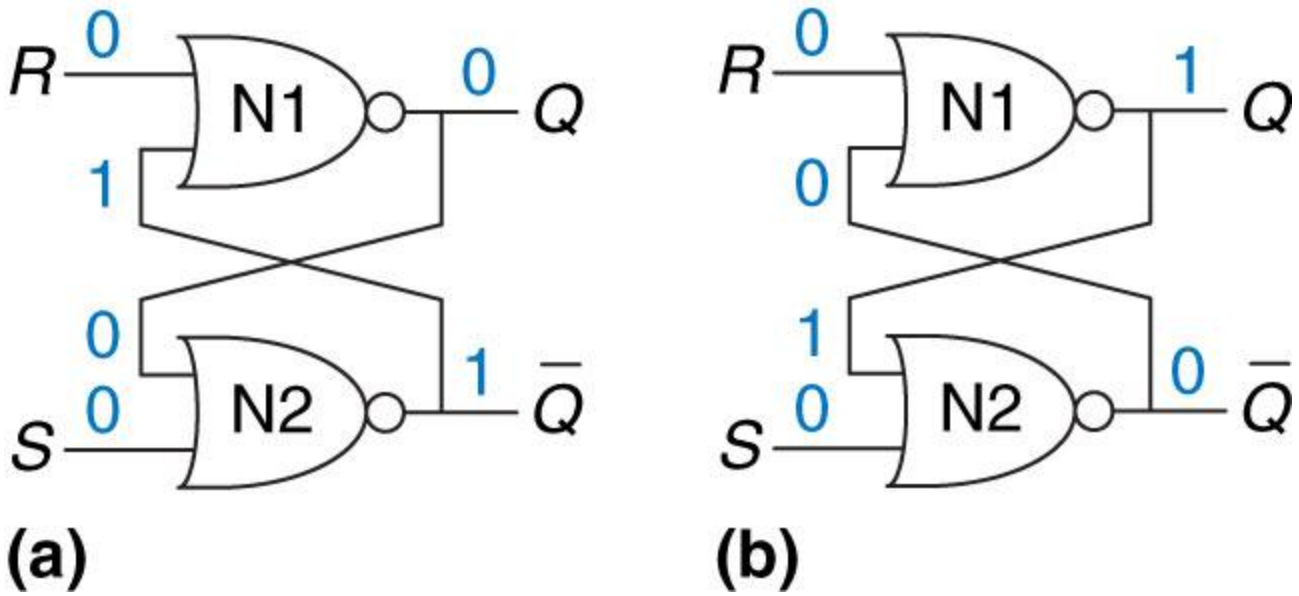


Figure 3.4 Bistable states of SR latch

Case	S	R	Q	$\overline{Q}$
IV	0	0	Q_{prev}	$\overline{Q}_{prev}$
I	0	1	0	1
II	1	0	1	0
III	1	1	0	0

Figure 3.5 SR latch truth table

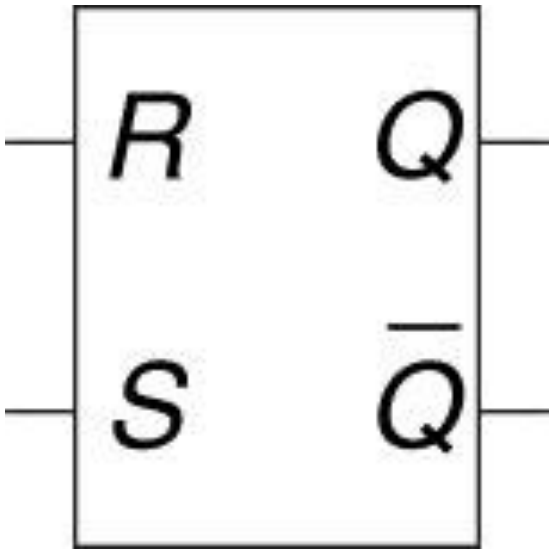


Figure 3.6 SR latch symbol

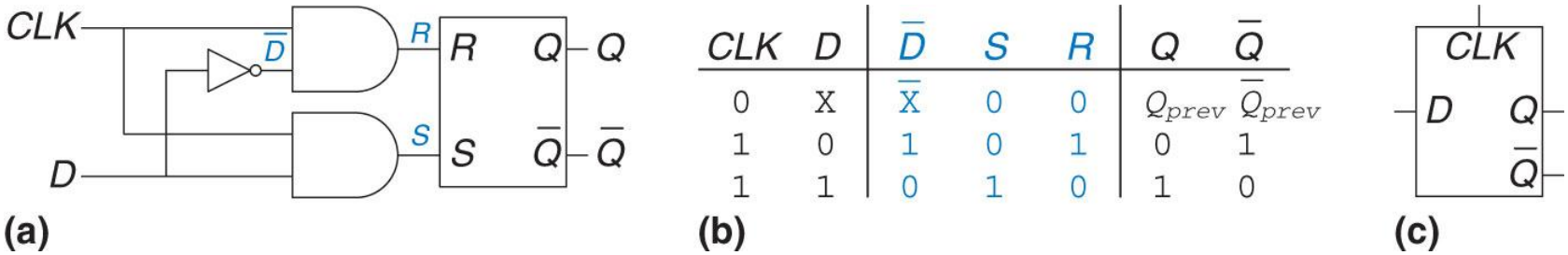


Figure 3.7 D latch: (a) schematic, (b) truth table, (c) symbol

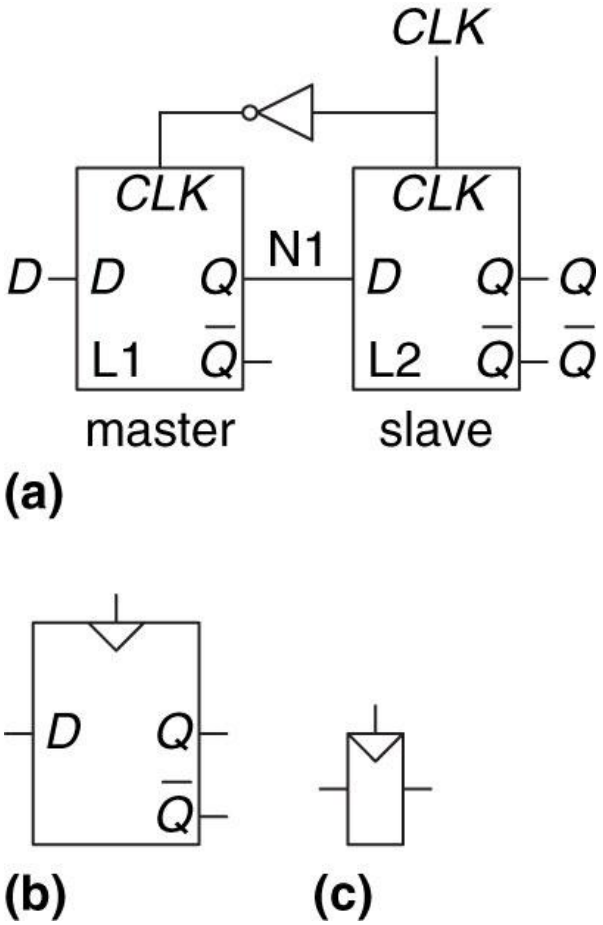


Figure 3.8 D flip-flop: (a) schematic, (b) symbol, (c) condensed symbol

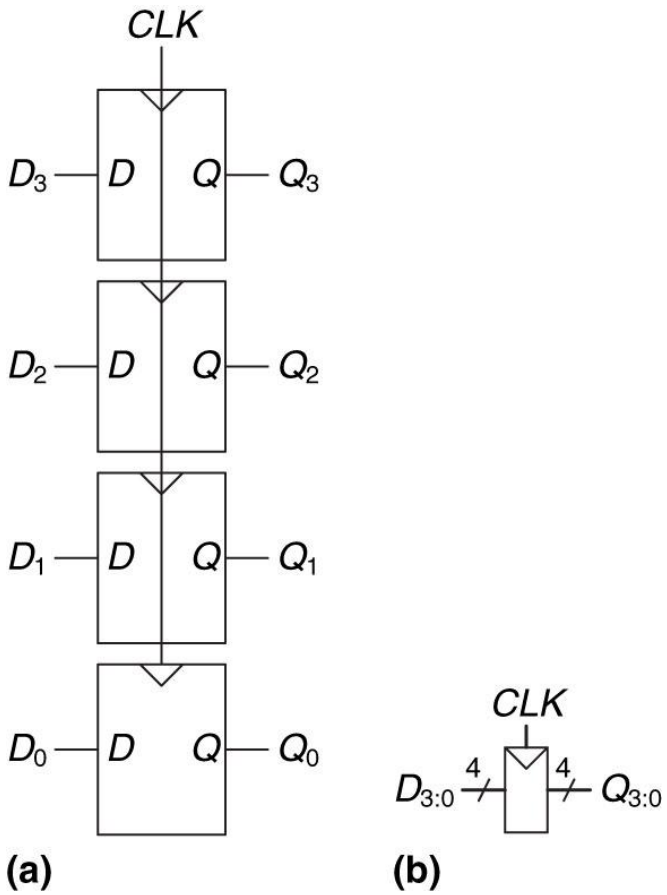


Figure 3.9 A 4-bit register: (a) schematic and (b) symbol

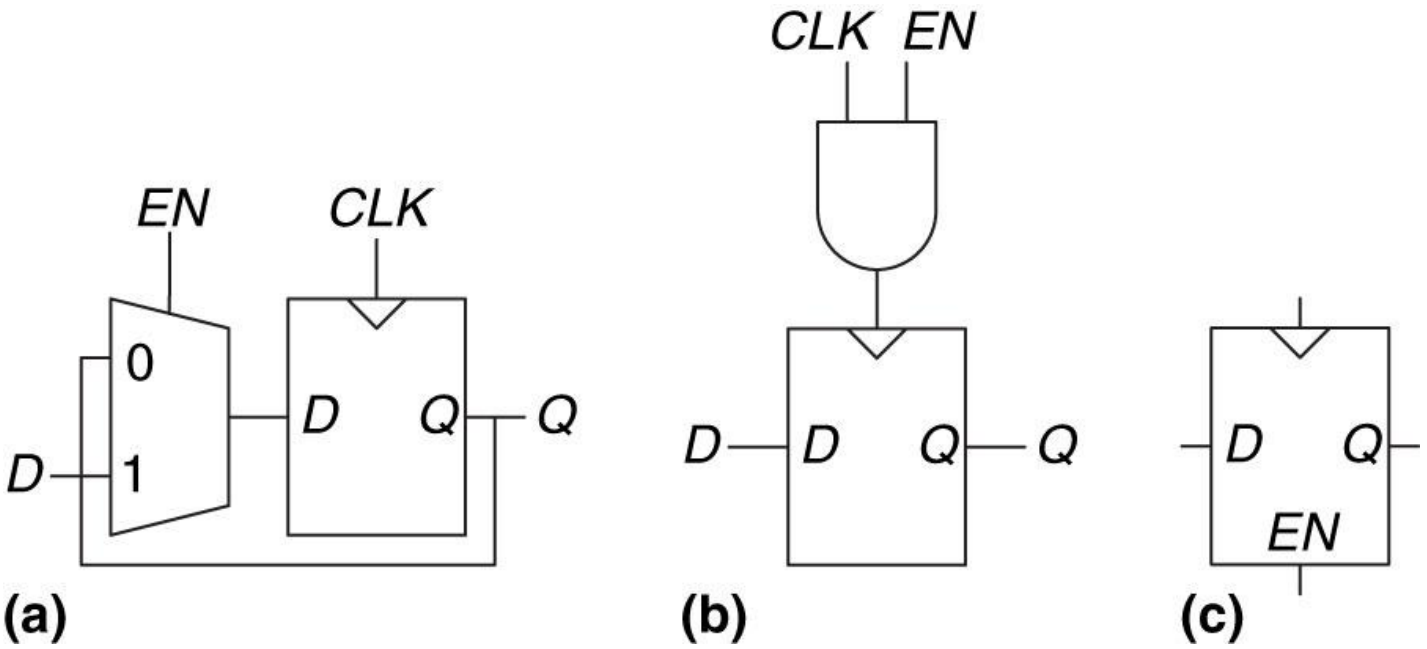


Figure 3.10 Enabled flip-flop: (a, b) schematics, (c) symbol

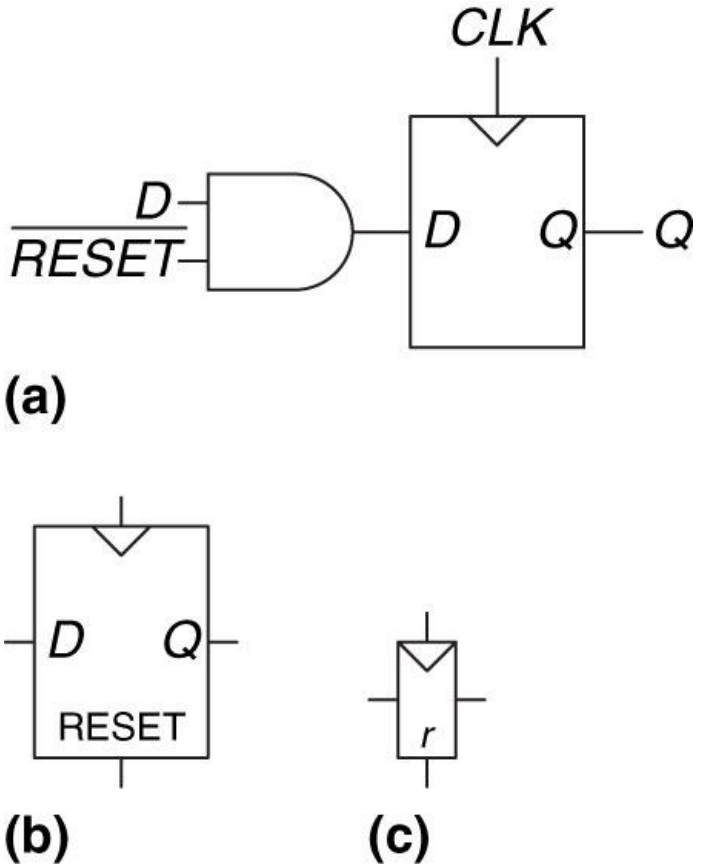


Figure 3.11 Synchronously resettable flip-flop: (a) schematic, (b, c) symbols

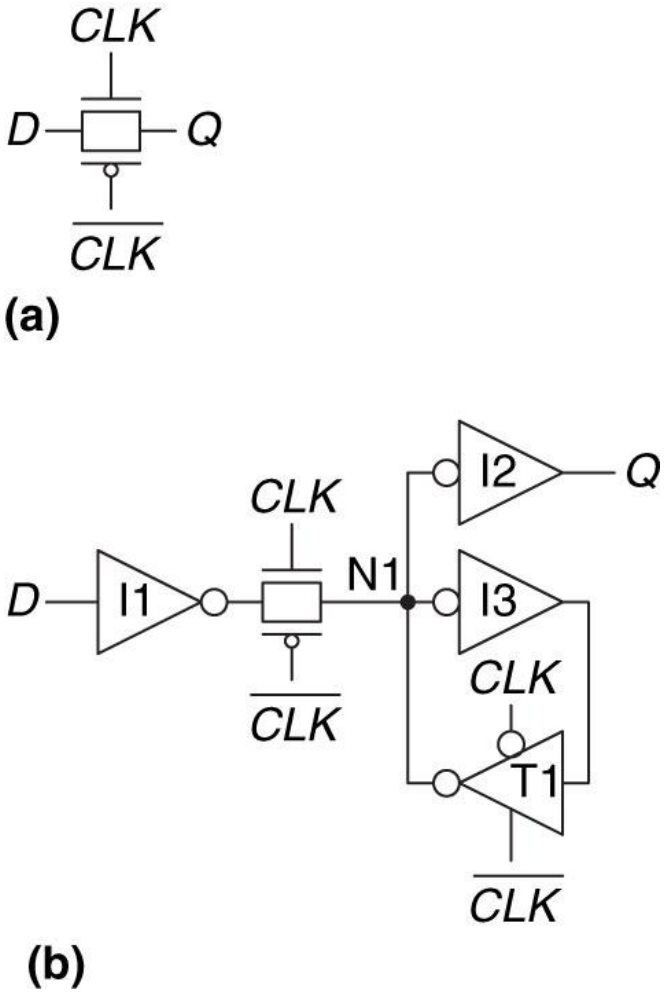


Figure 3.12 D latch schematic

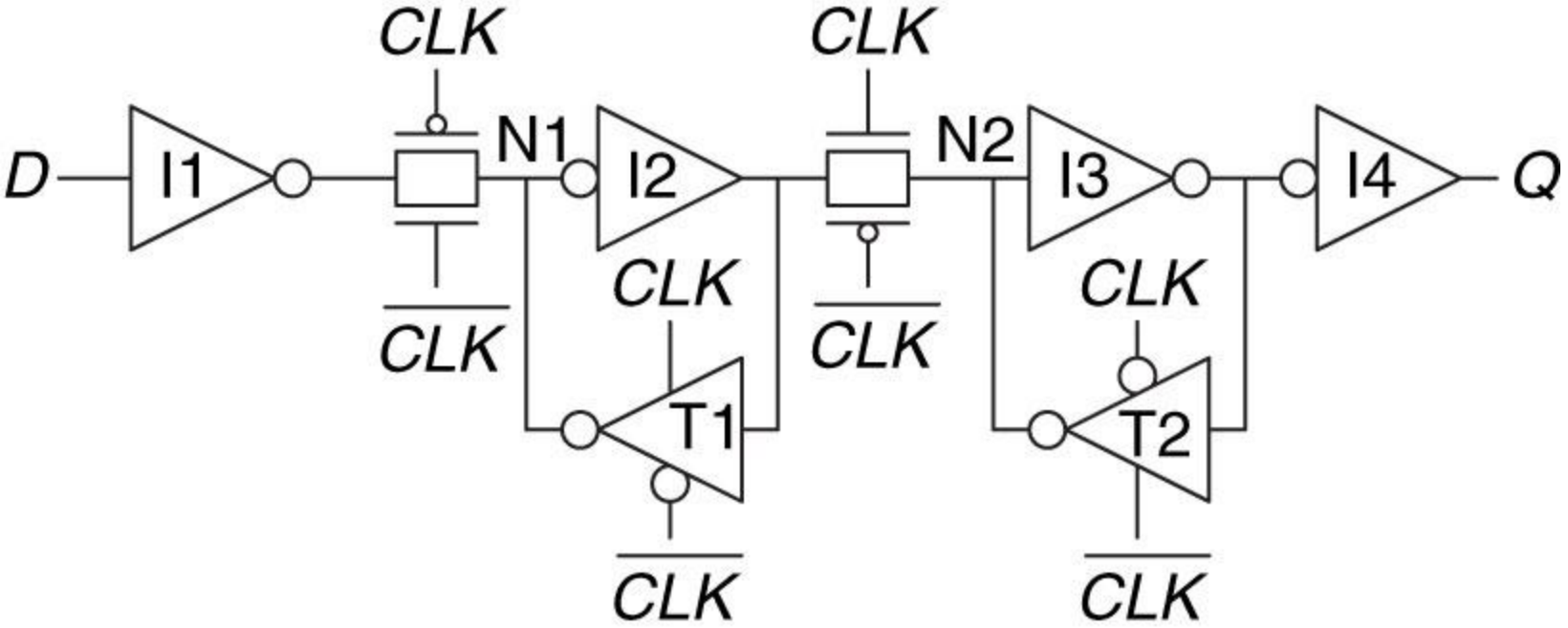


Figure 3.13 D flip-flop schematic

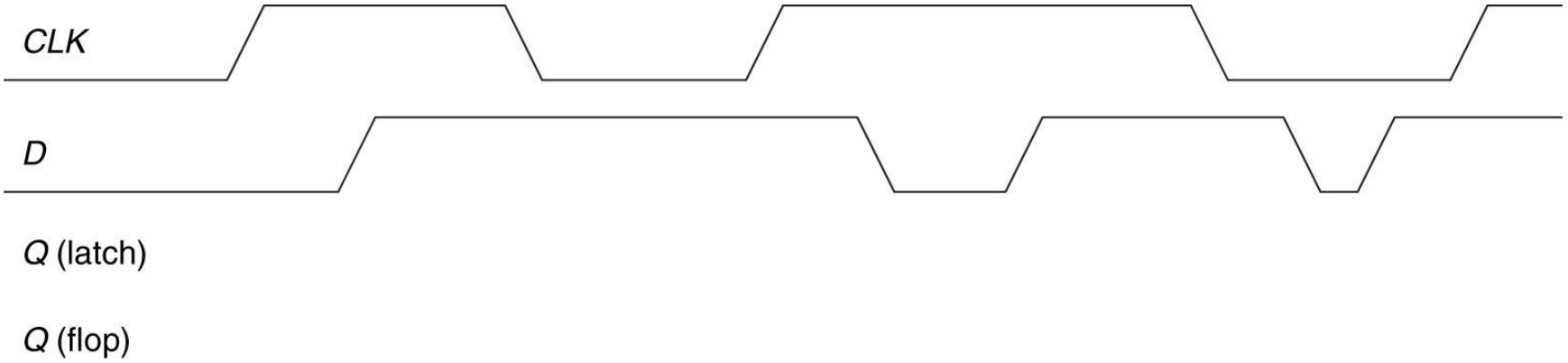


Figure 3.14 Example waveforms

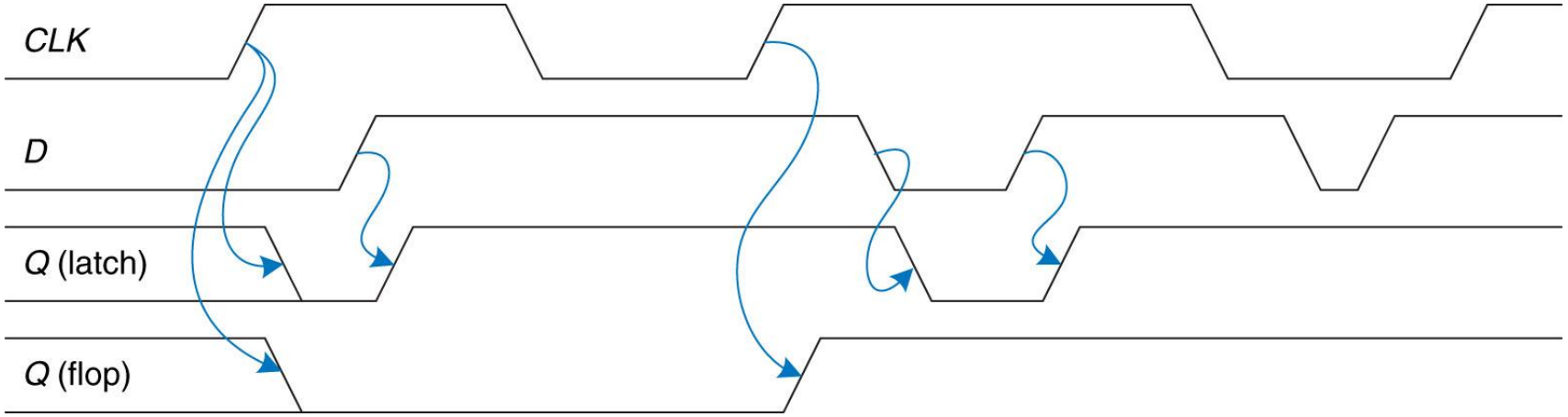


Figure 3.15 Solution waveforms

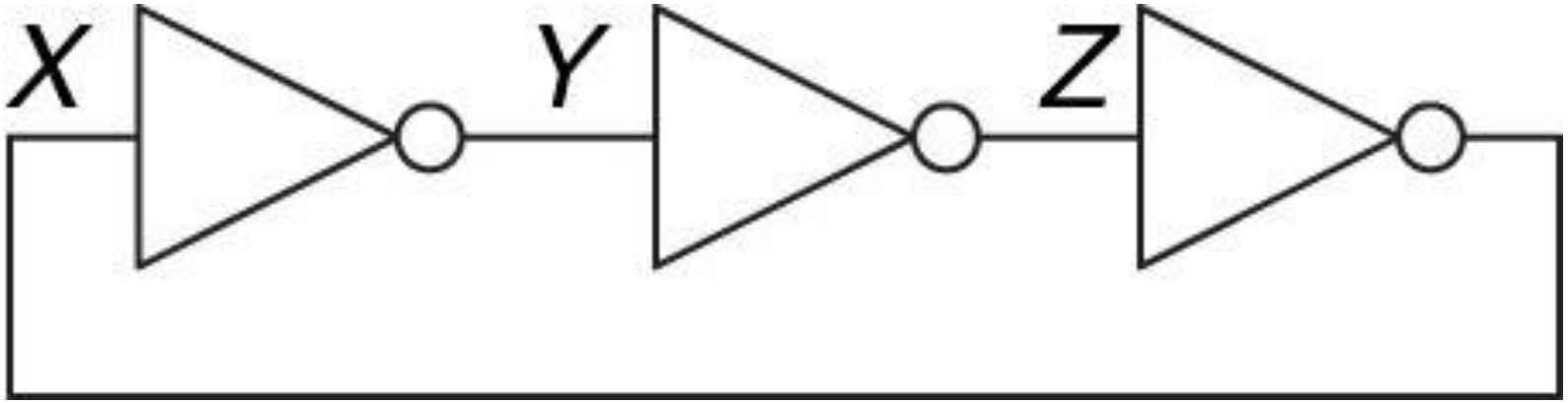


Figure 3.16 Three-inverter loop

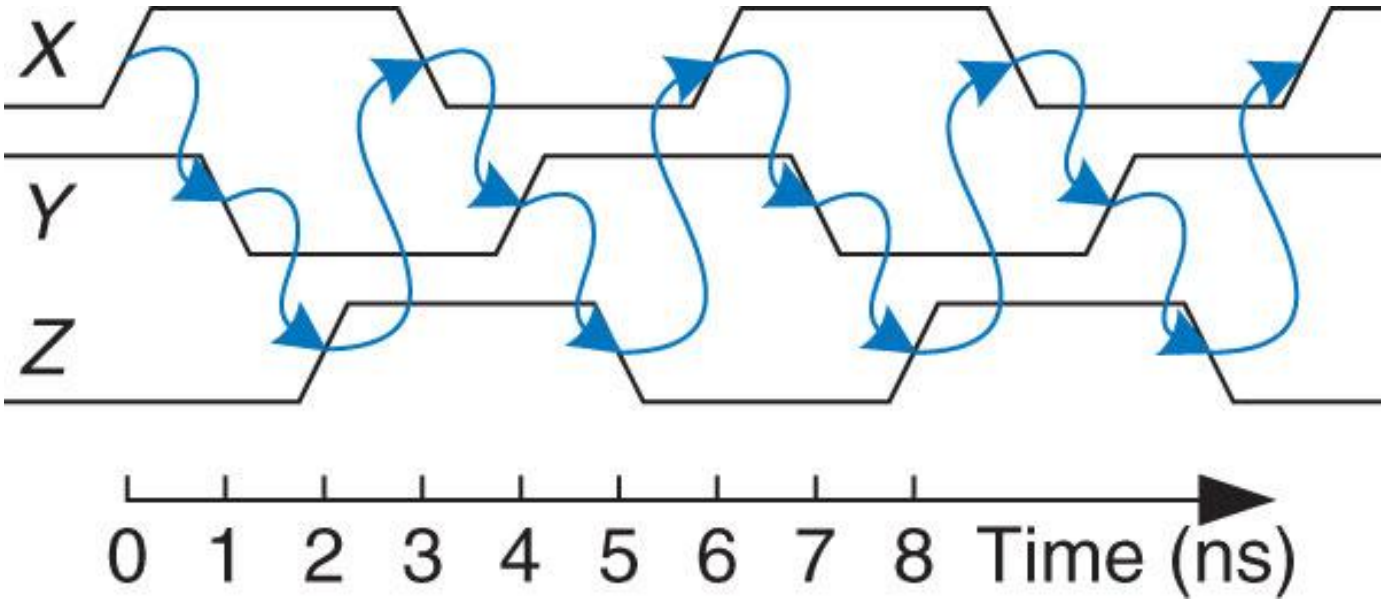


Figure 3.17 Ring oscillator waveforms

CLK	D	Q_{prev}	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$$Q = CLK \cdot D + \overline{CLK} \cdot Q_{prev}$$

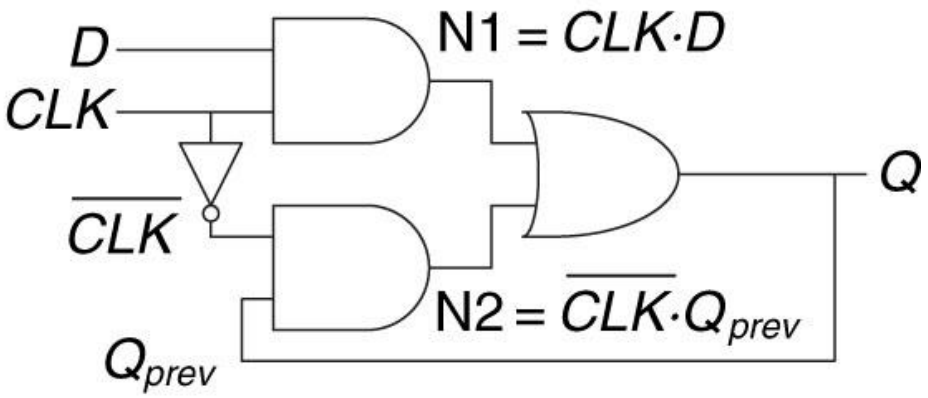


Figure 3.18 An improved (?) D latch

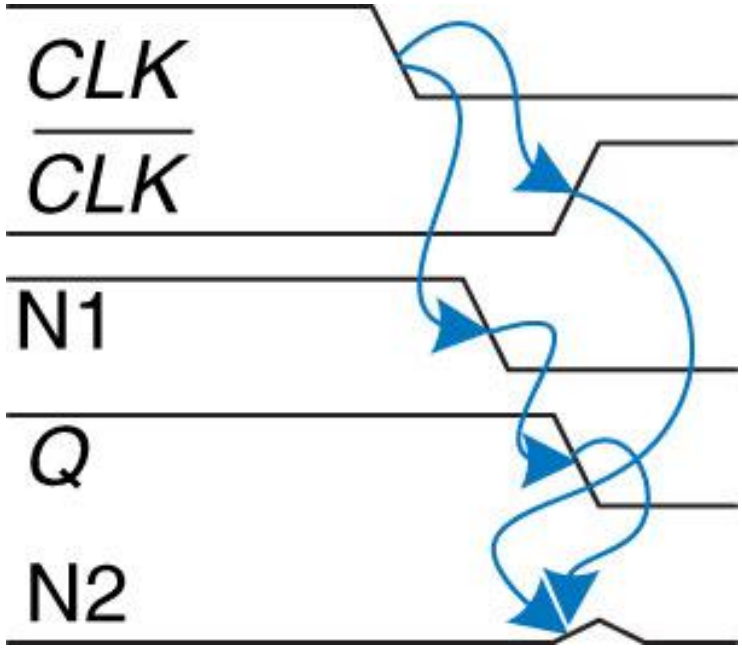


Figure 3.19 Latch waveforms illustrating race condition

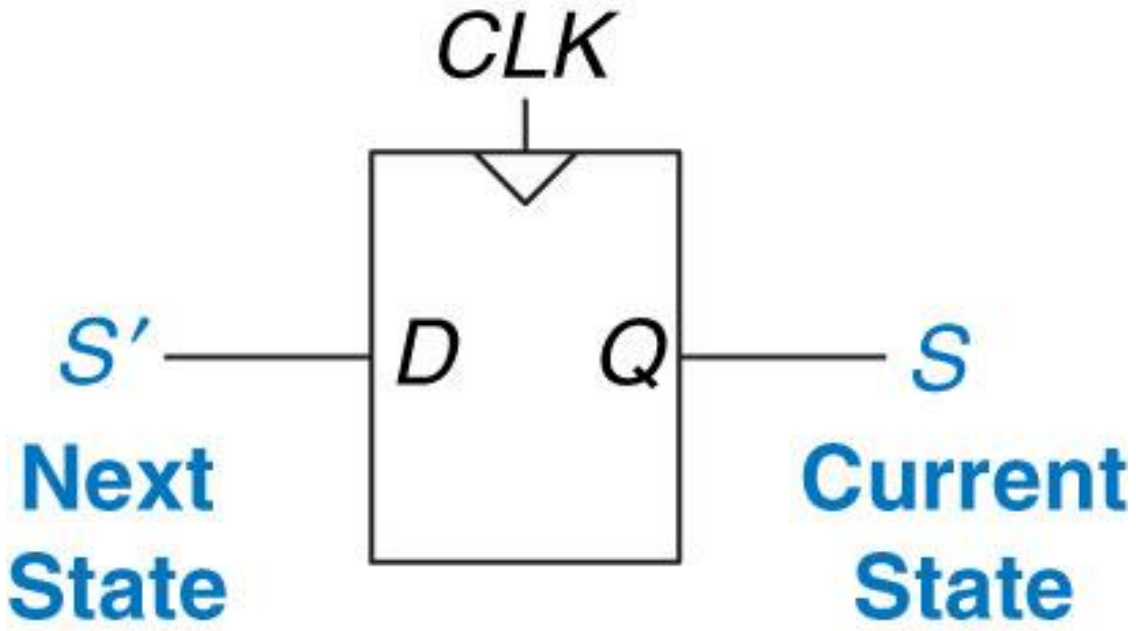


Figure 3.20 Flip-flop current state and next state

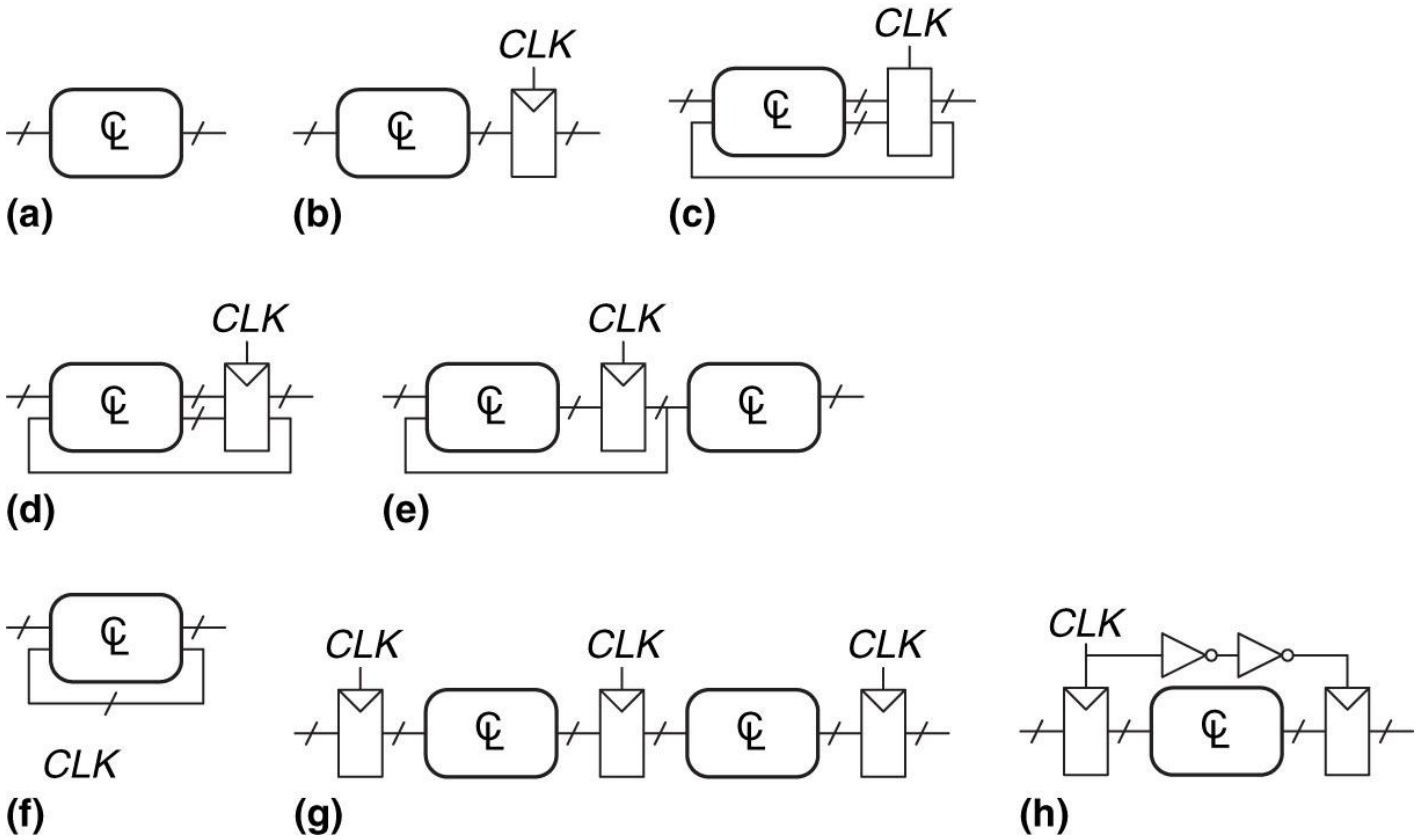


Figure 3.21 Example circuits

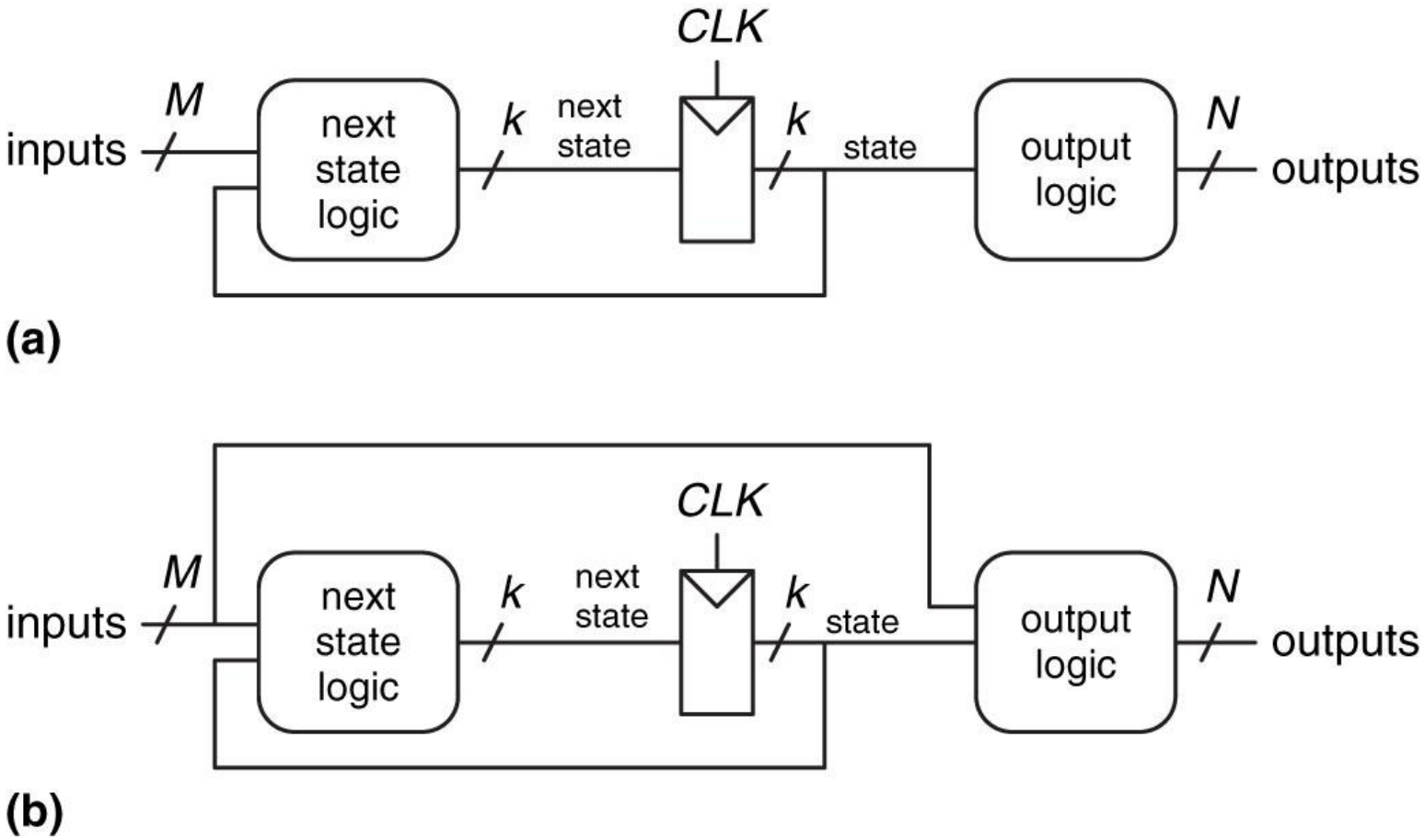


Figure 3.22 Finite state machines: (a) Moore machine, (b) Mealy machine

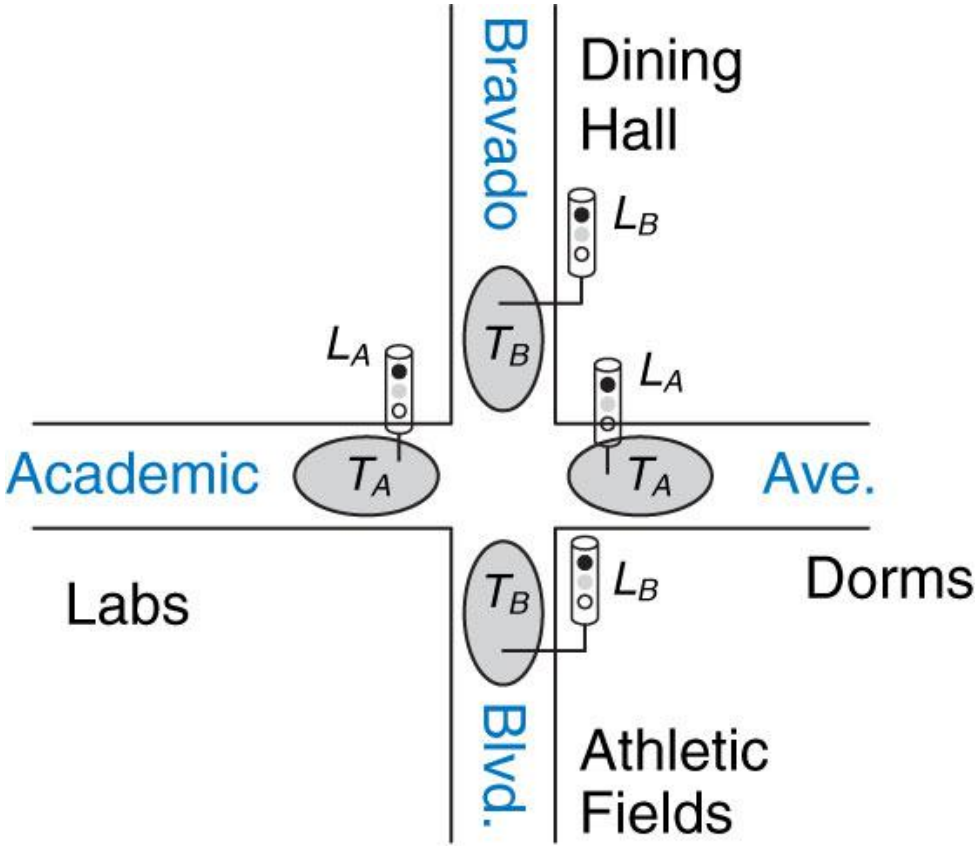


Figure 3.23 Campus map

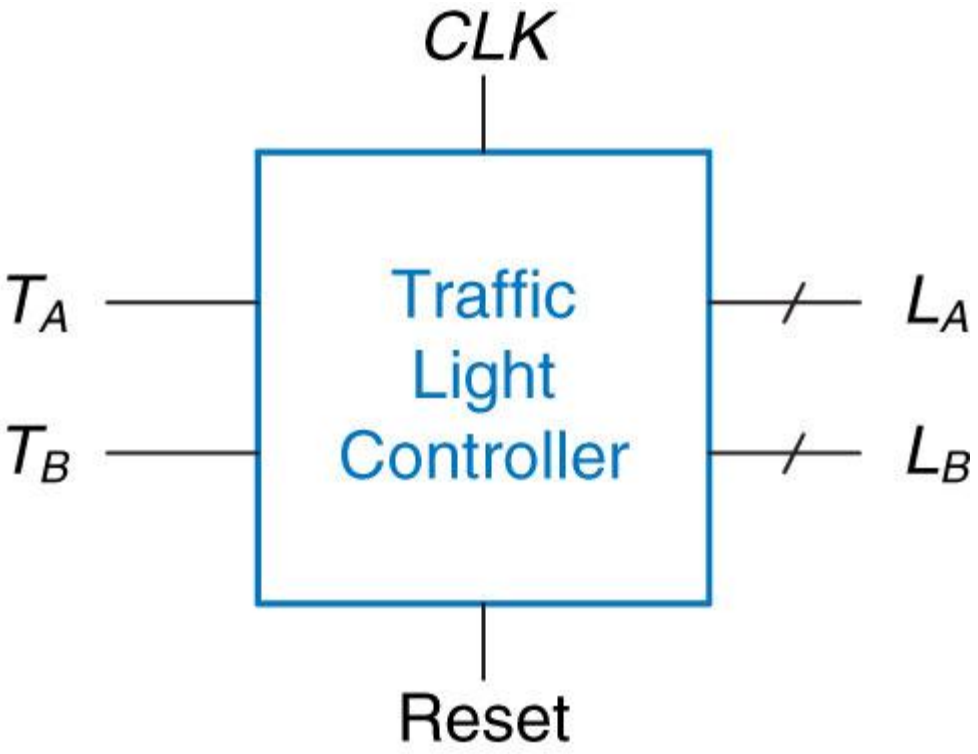


Figure 3.24 Black box view of finite state machine

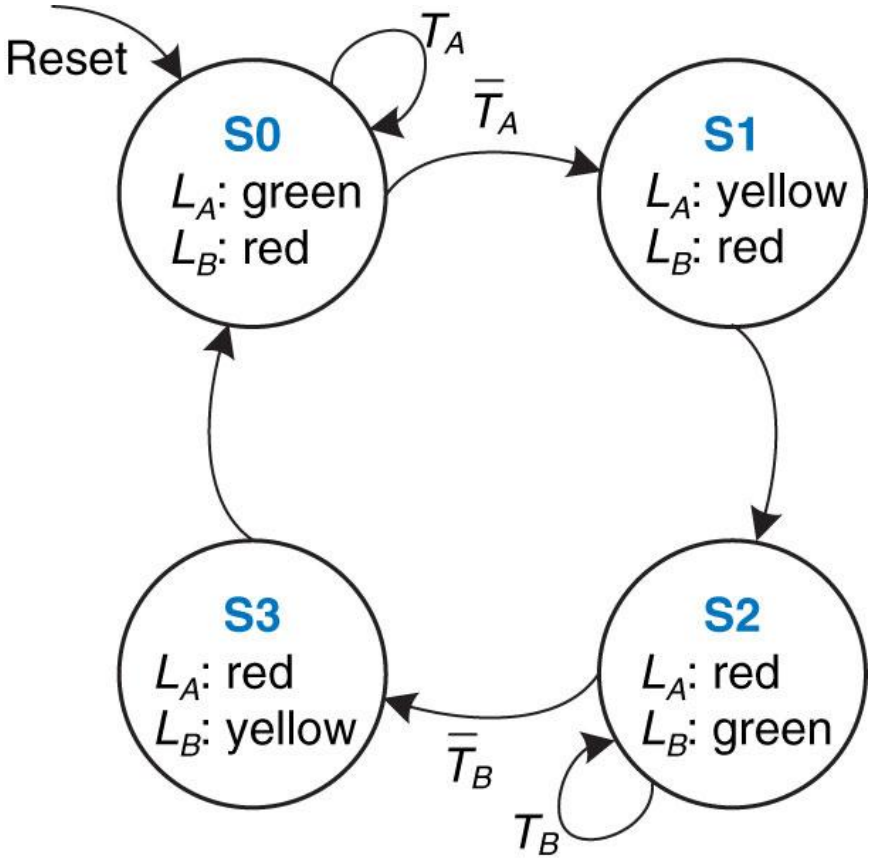


Figure 3.25 State transition diagram

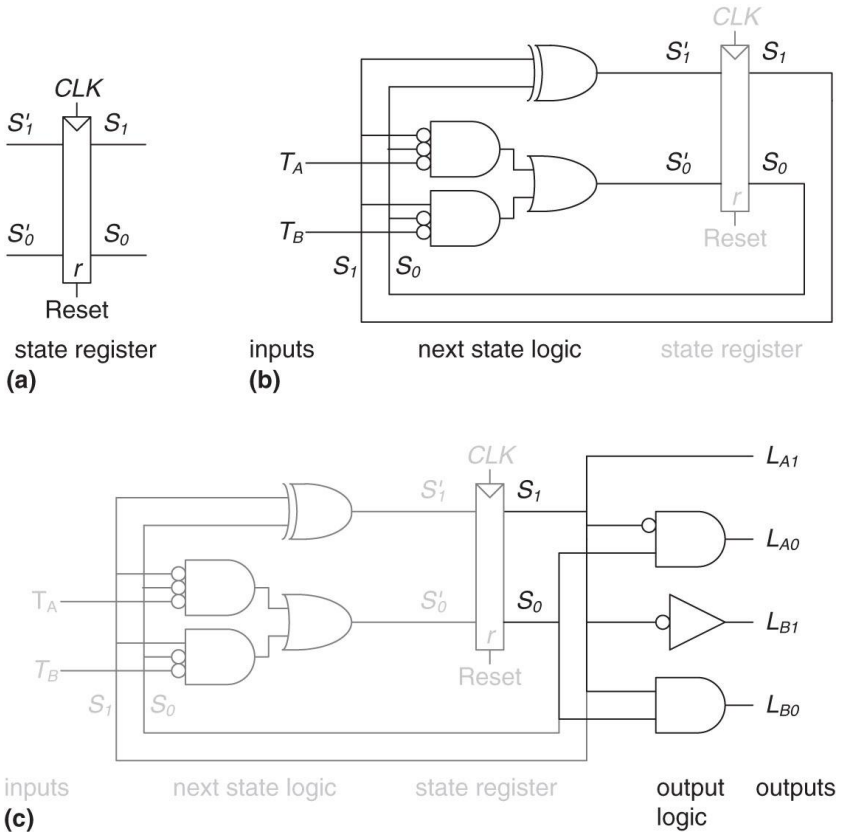


Figure 3.26 State machine circuit for traffic light controller

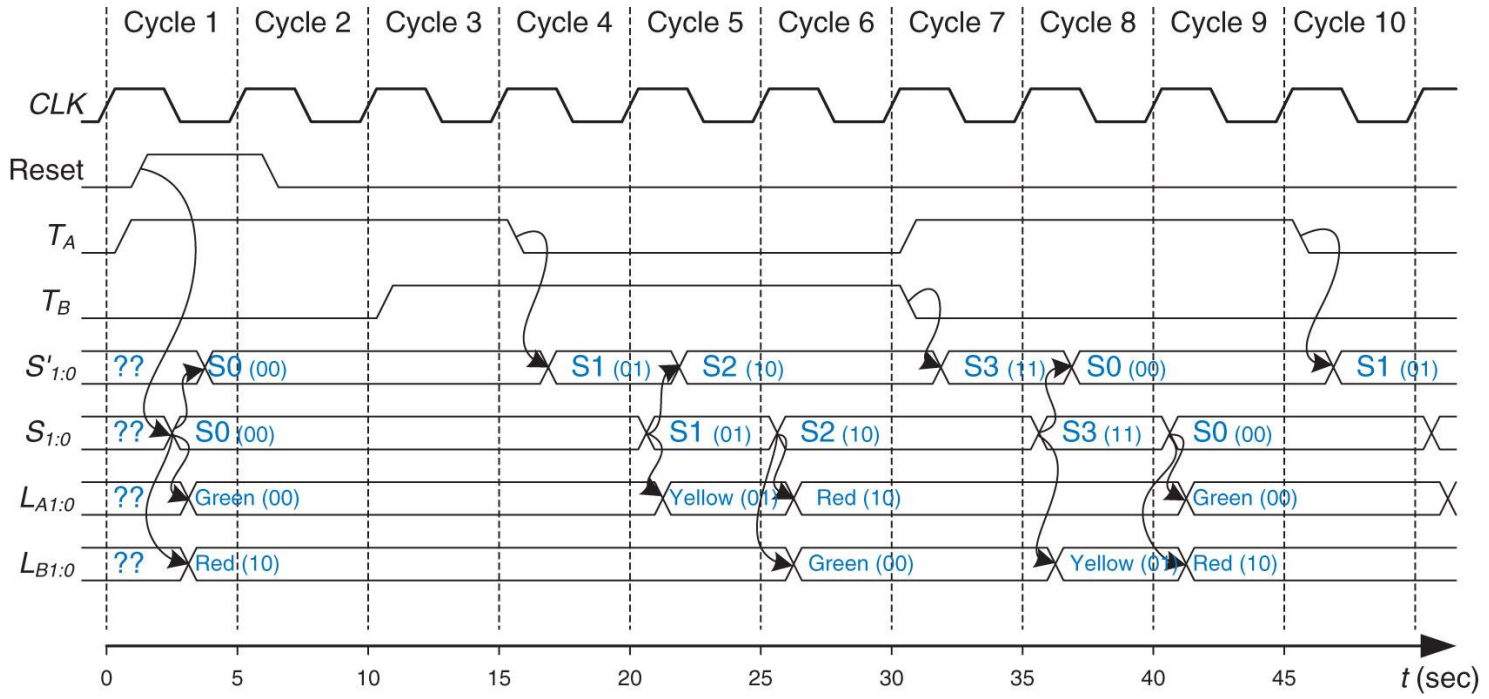


Figure 3.27 Timing diagram for traffic light controller

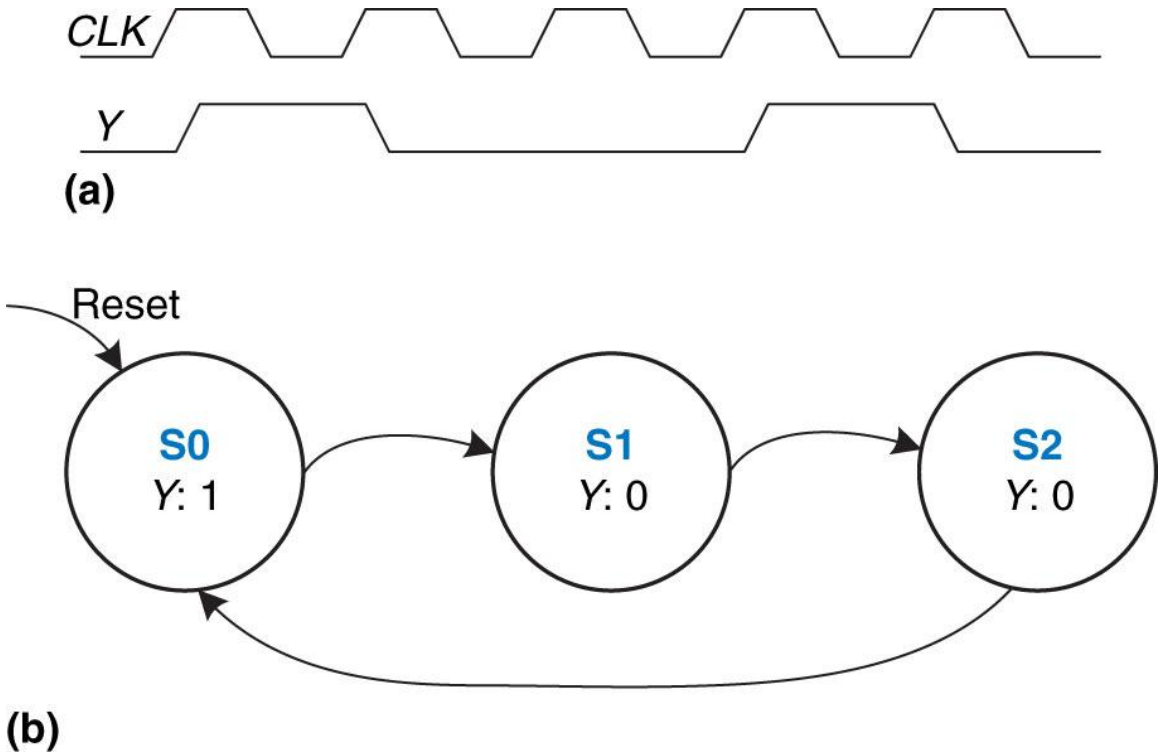


Figure 3.28 Divide-by-3 counter (a) waveform and (b) state transition diagram

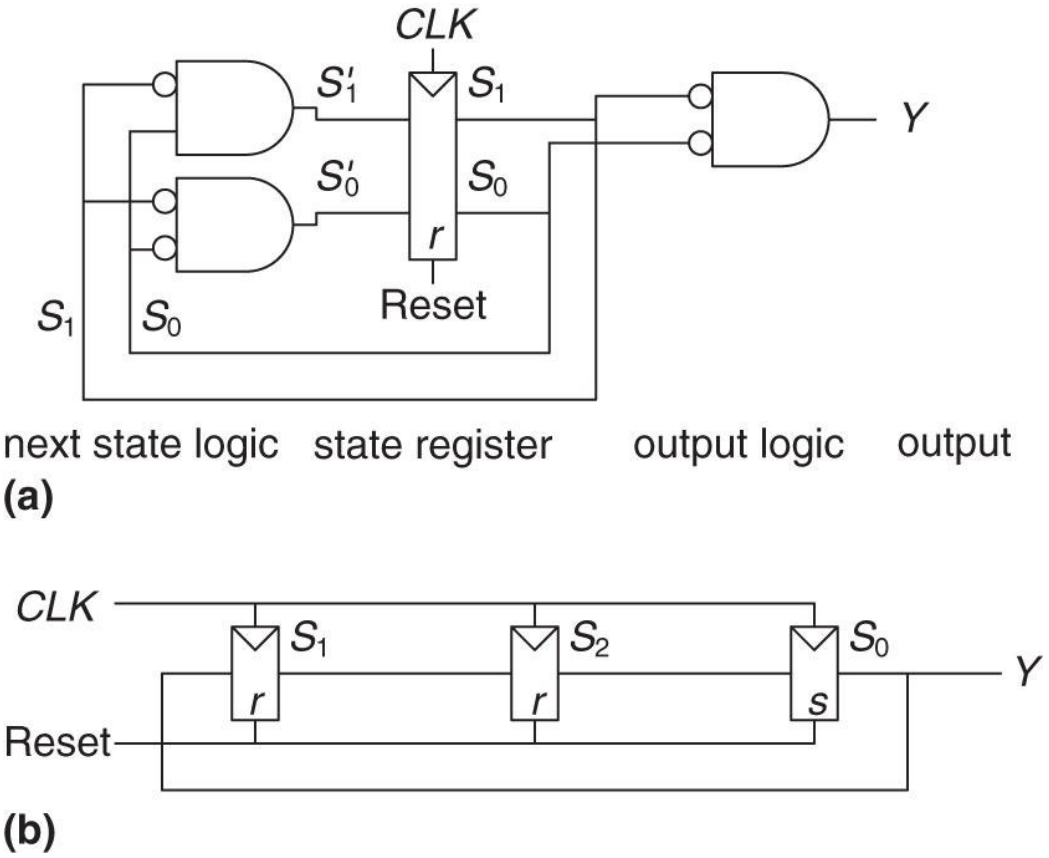


Figure 3.29 Divide-by-3 circuits for (a) binary and (b) one-hot encodings

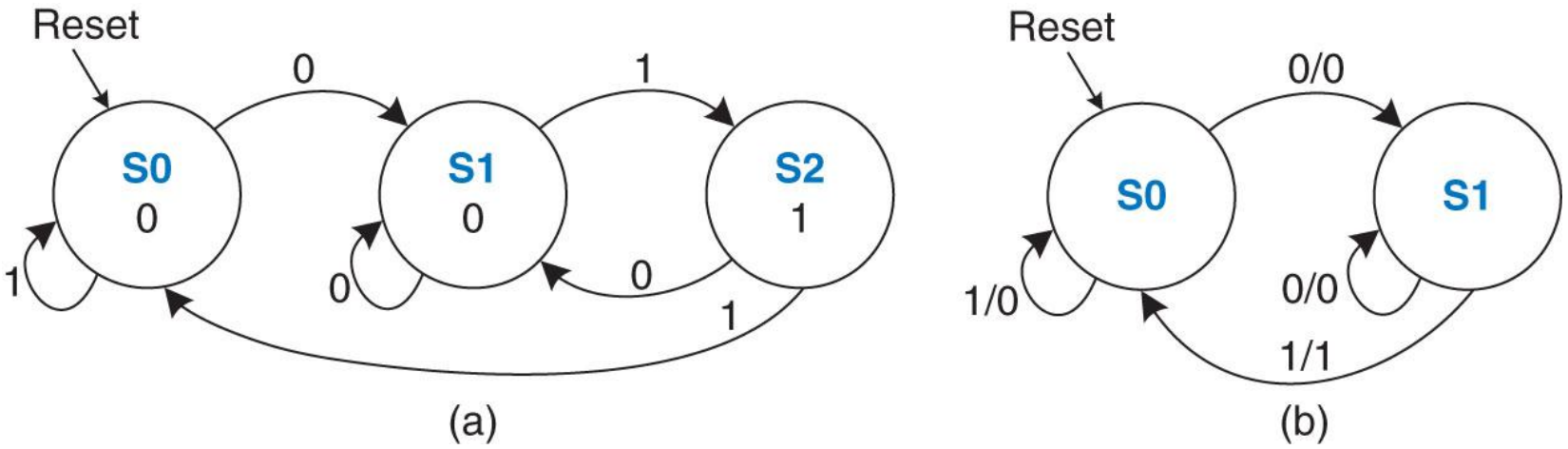


Figure 3.30 FSM state transition diagrams: (a) Moore machine, (b) Mealy machine

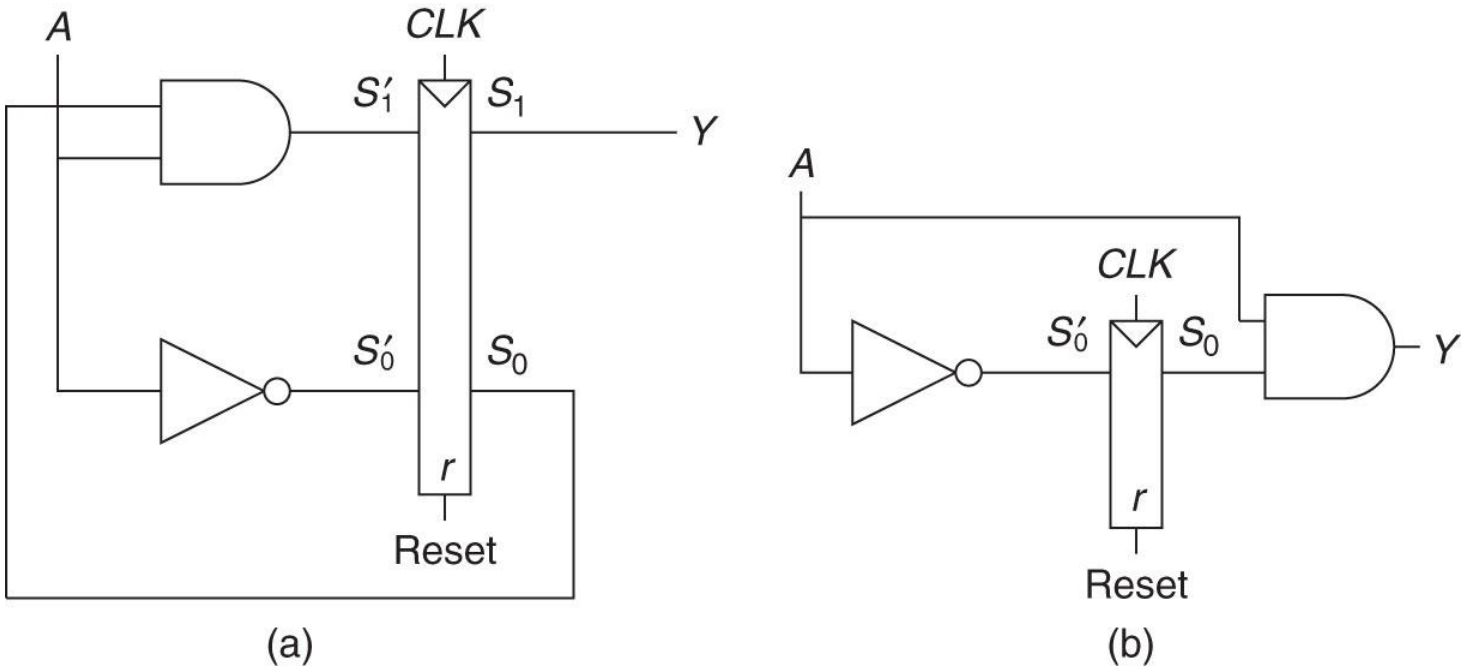


Figure 3.31 FSM schematics for (a) Moore and (b) Mealy machines

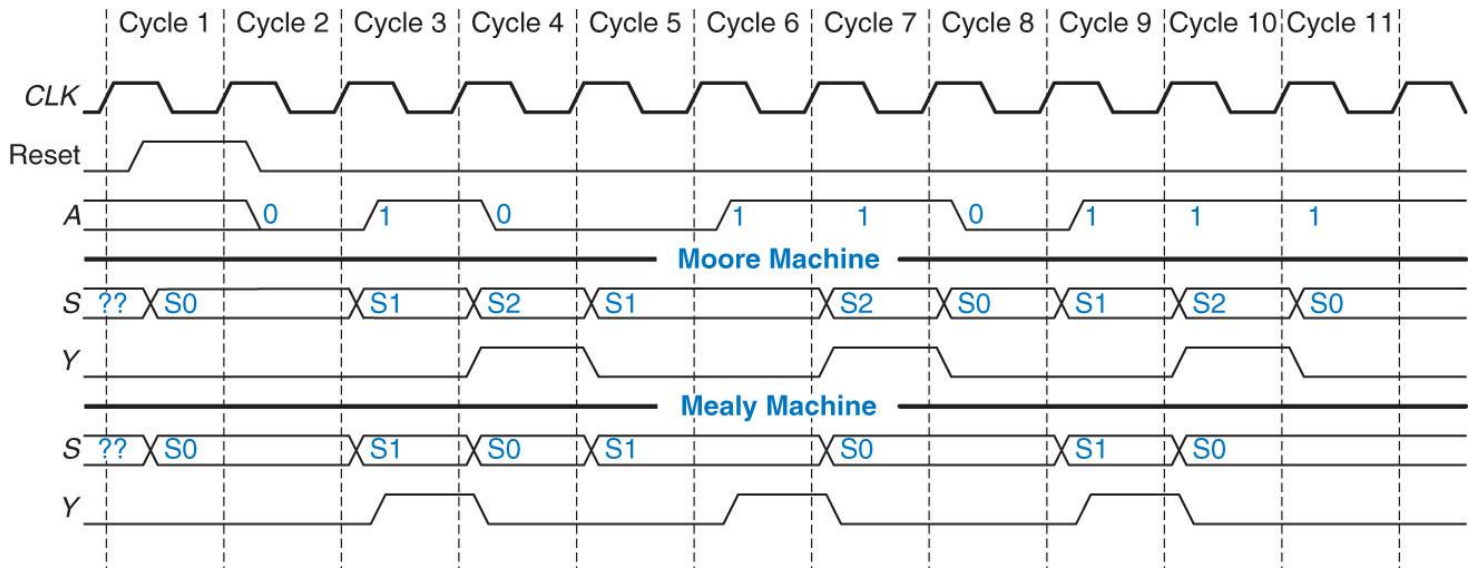


Figure 3.32 Timing diagrams for Moore and Mealy machines

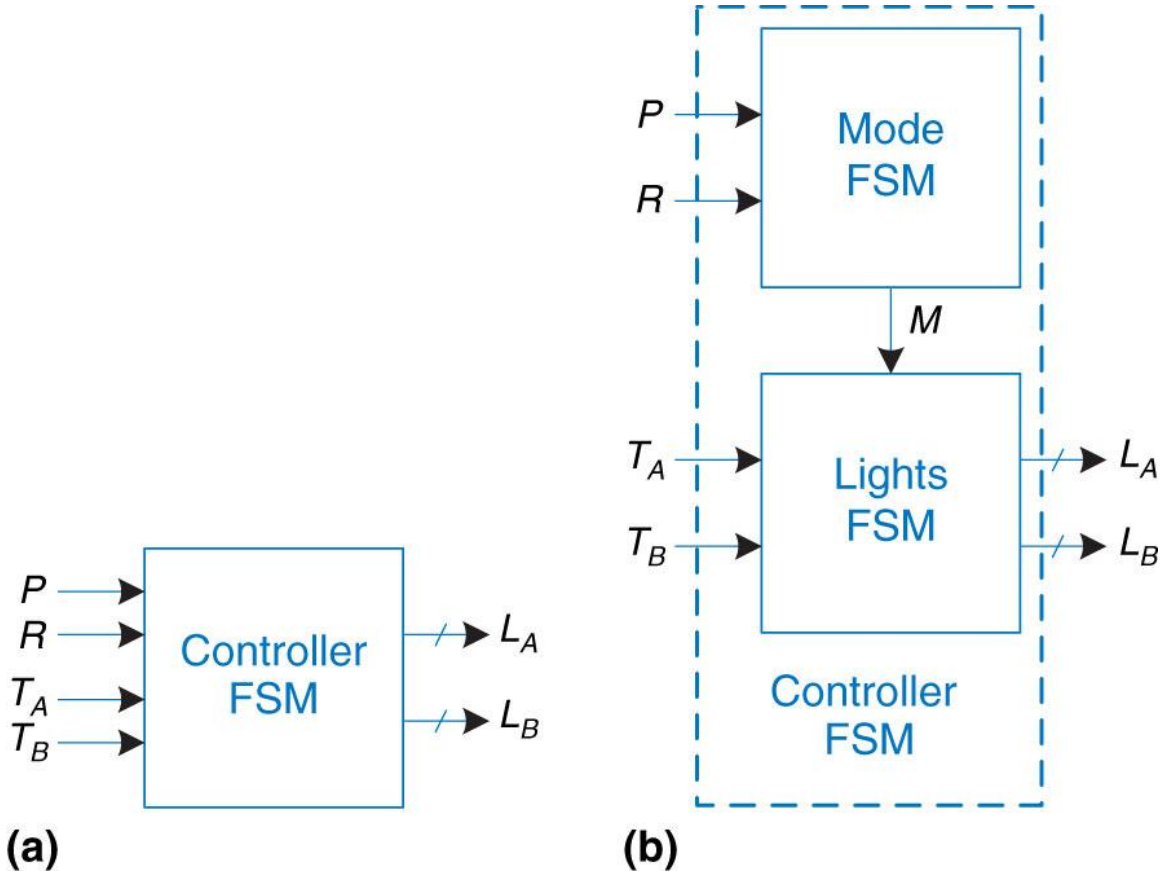


Figure 3.33 (a) single and (b) factored designs for modified traffic light controller FSM

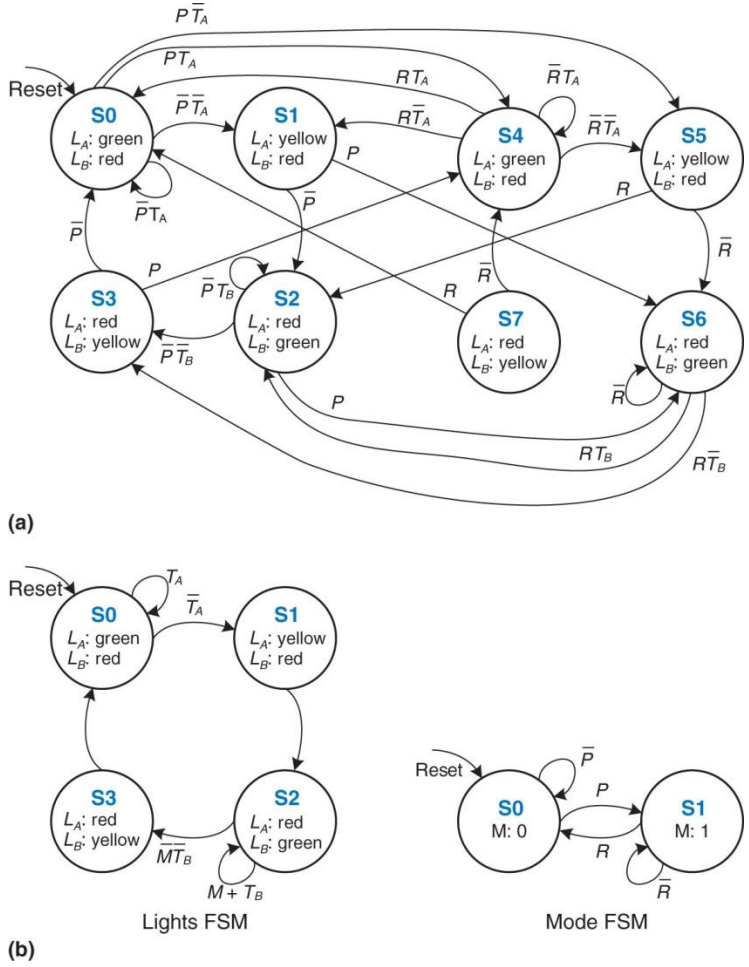


Figure 3.34 State transition diagrams: (a) unfactored, (b) factored

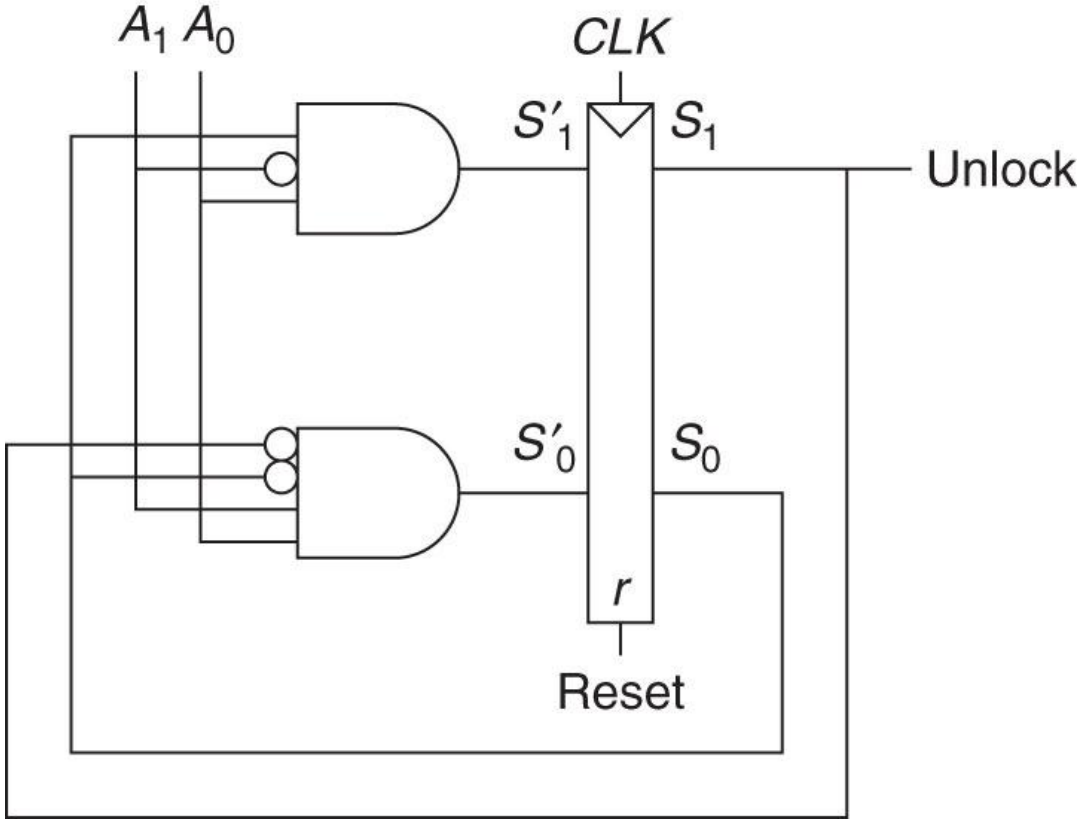


Figure 3.35 Circuit of found FSM for Example 3.9

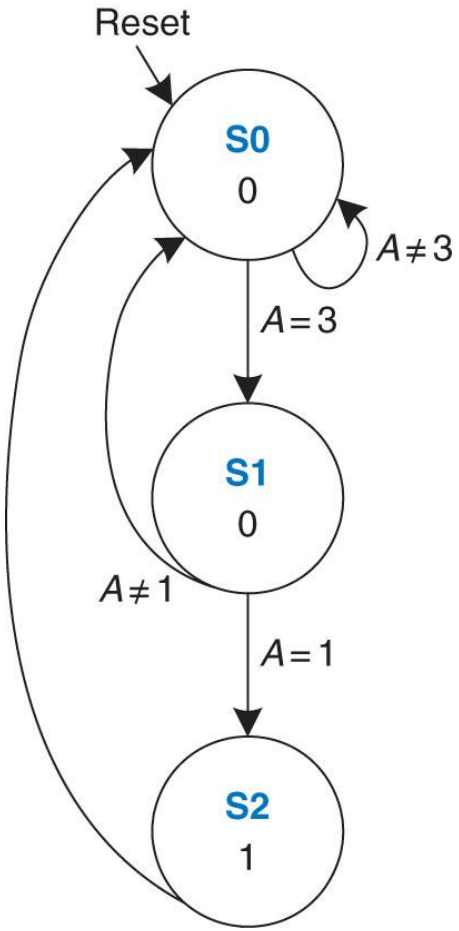


Figure 3.36 State transition diagram of found FSM from Example 3.9

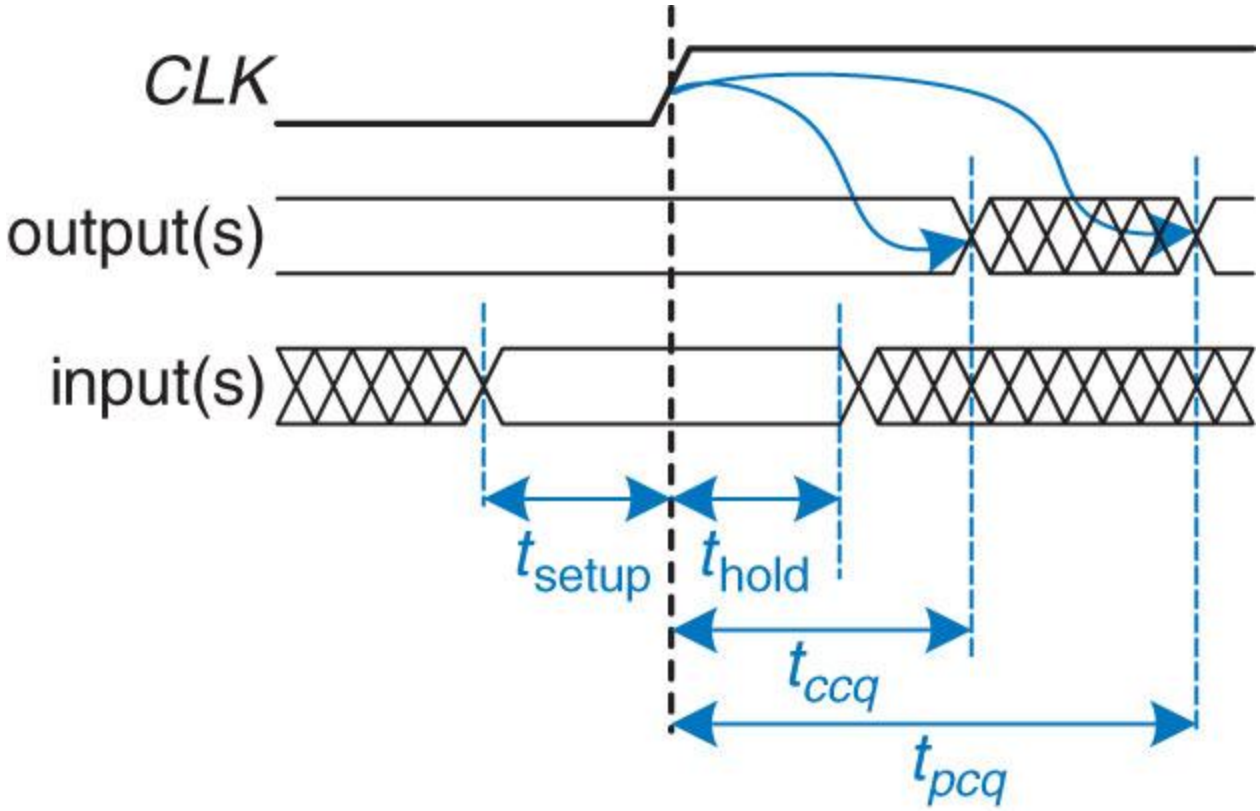


Figure 3.37 Timing specification for synchronous sequential circuit

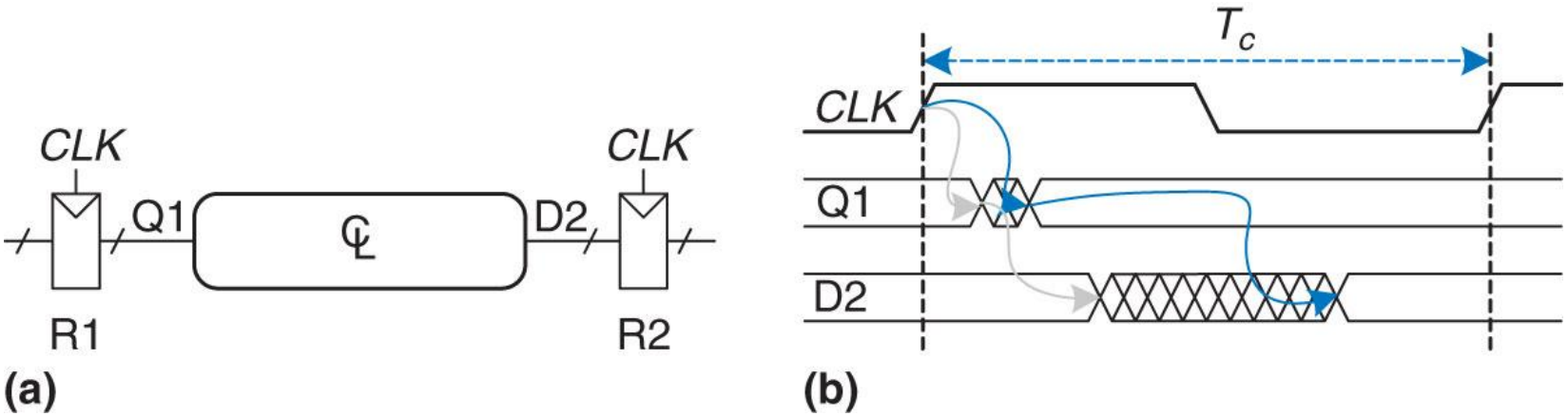


Figure 3.38 Path between registers and timing diagram

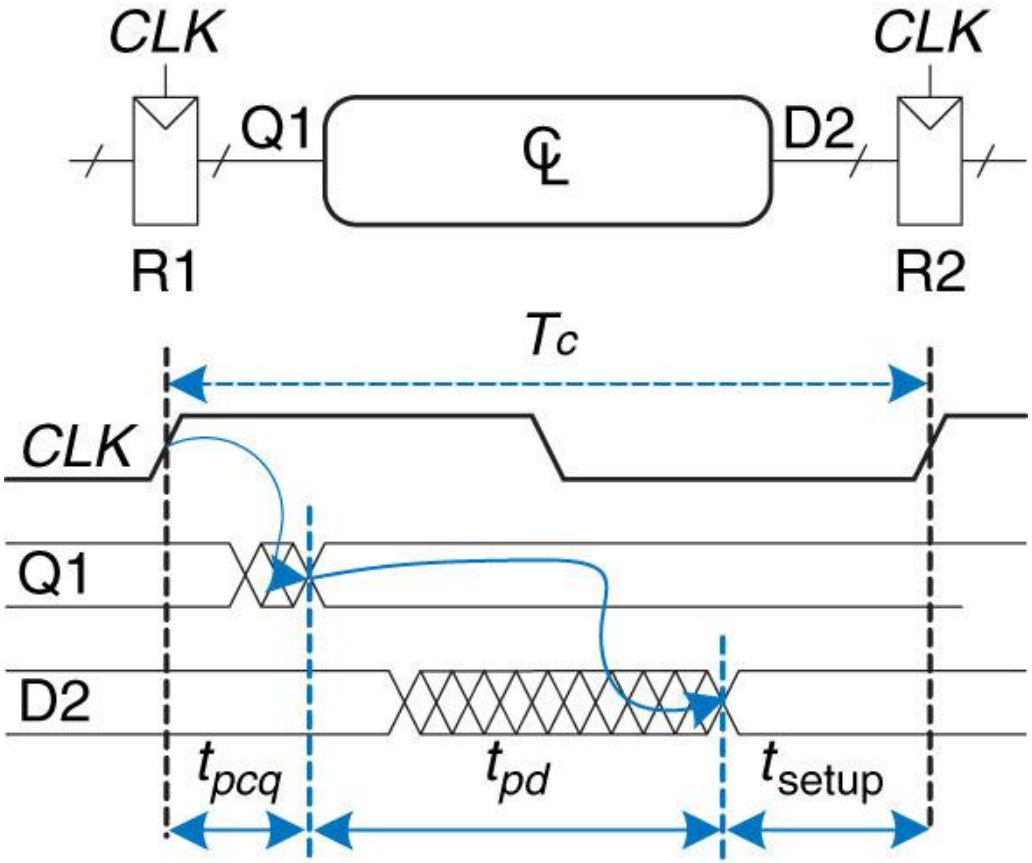


Figure 3.39 Maximum delay for setup time constraint

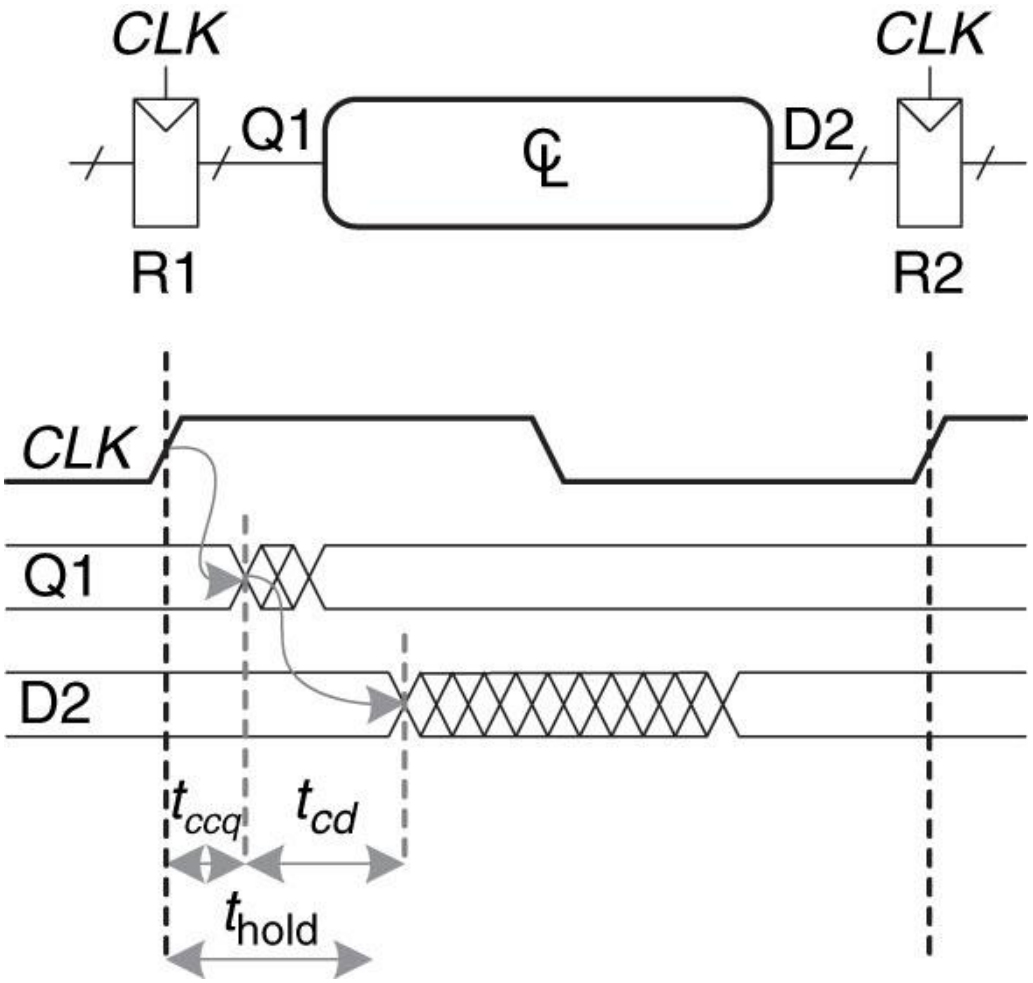


Figure 3.40 Minimum delay for hold time constraint

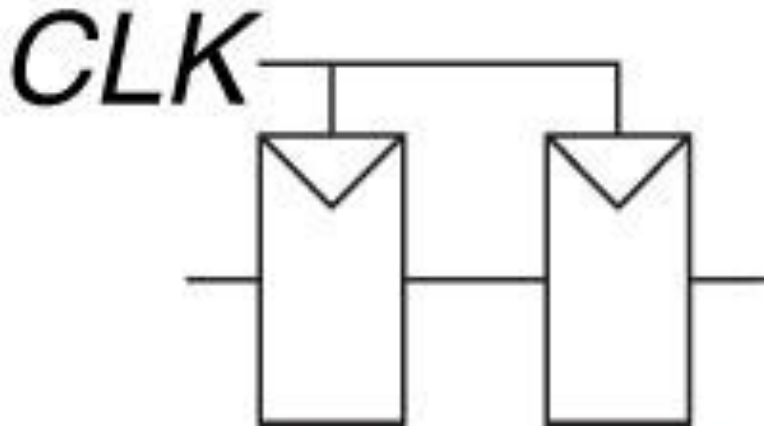


Figure 3.41 Back-to-back flip-flops

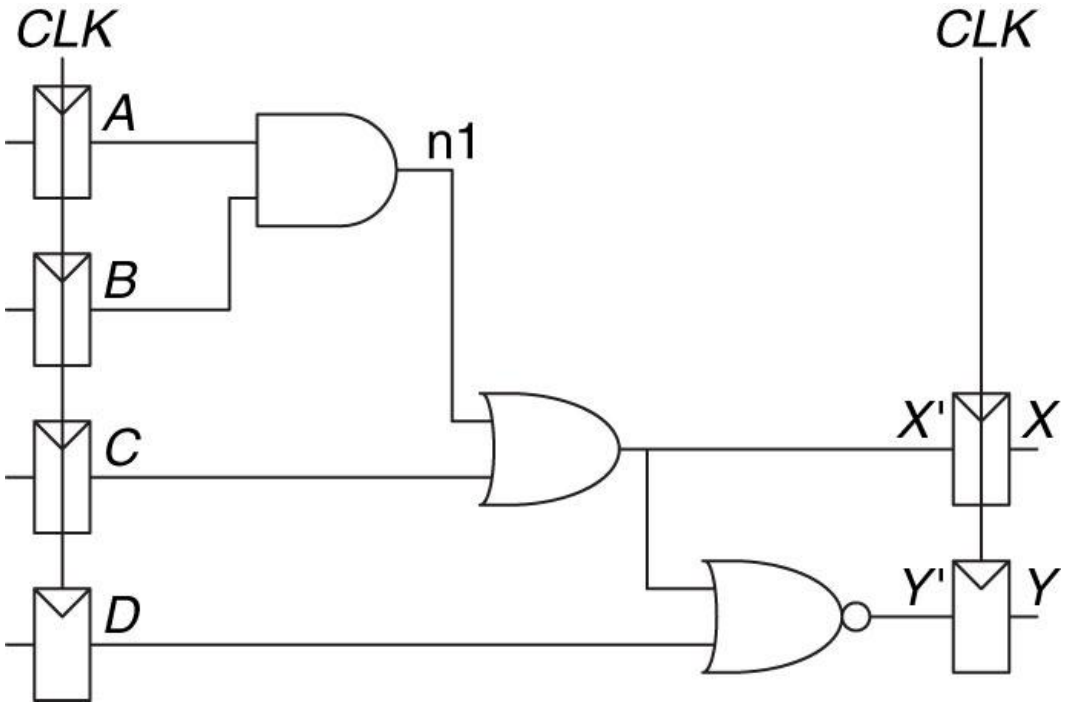


Figure 3.42 Sample circuit for timing analysis

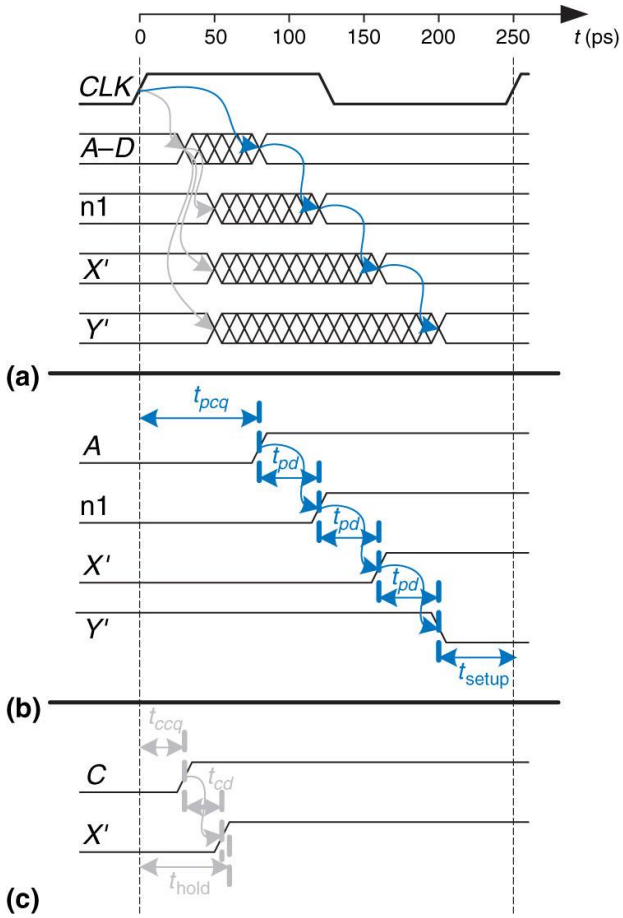


Figure 3.43 Timing diagram: (a) general case, (b) critical path, (c) short path

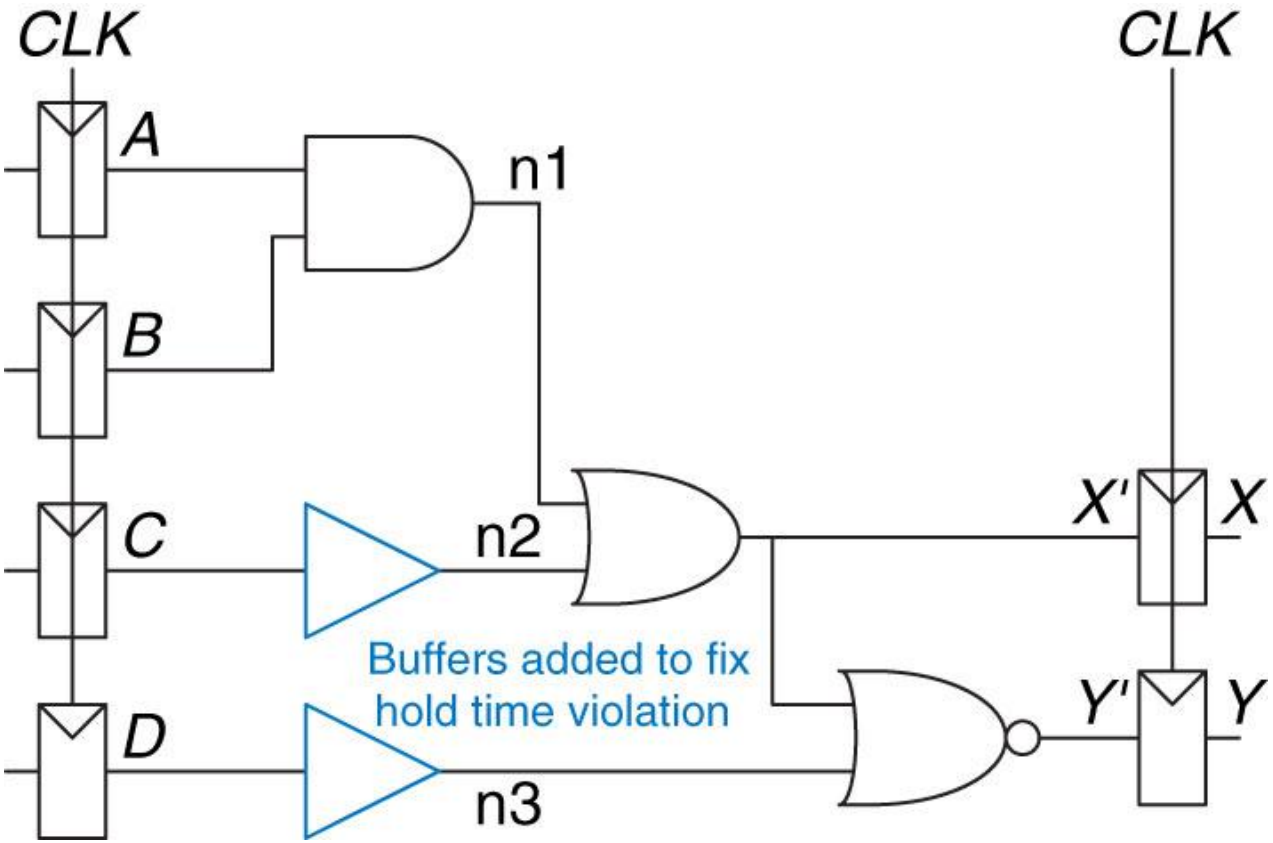


Figure 3.44 Corrected circuit to fix hold time problem

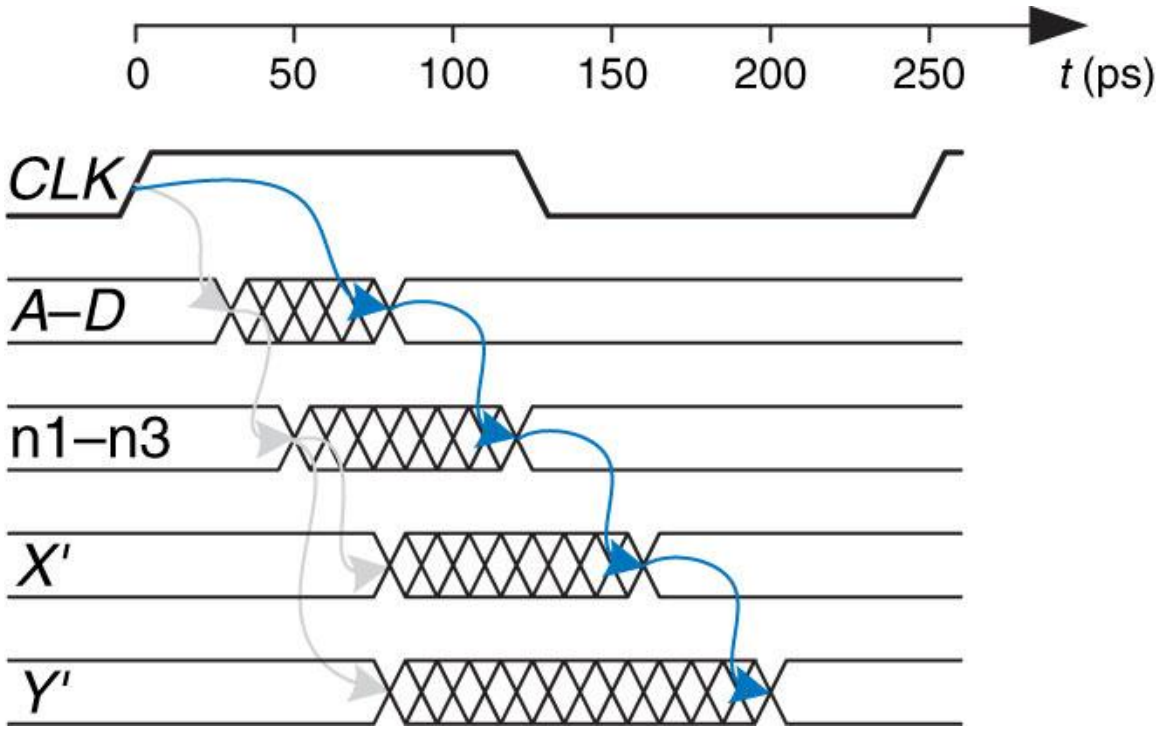


Figure 3.45 Timing diagram with buffers to fix hold time problem

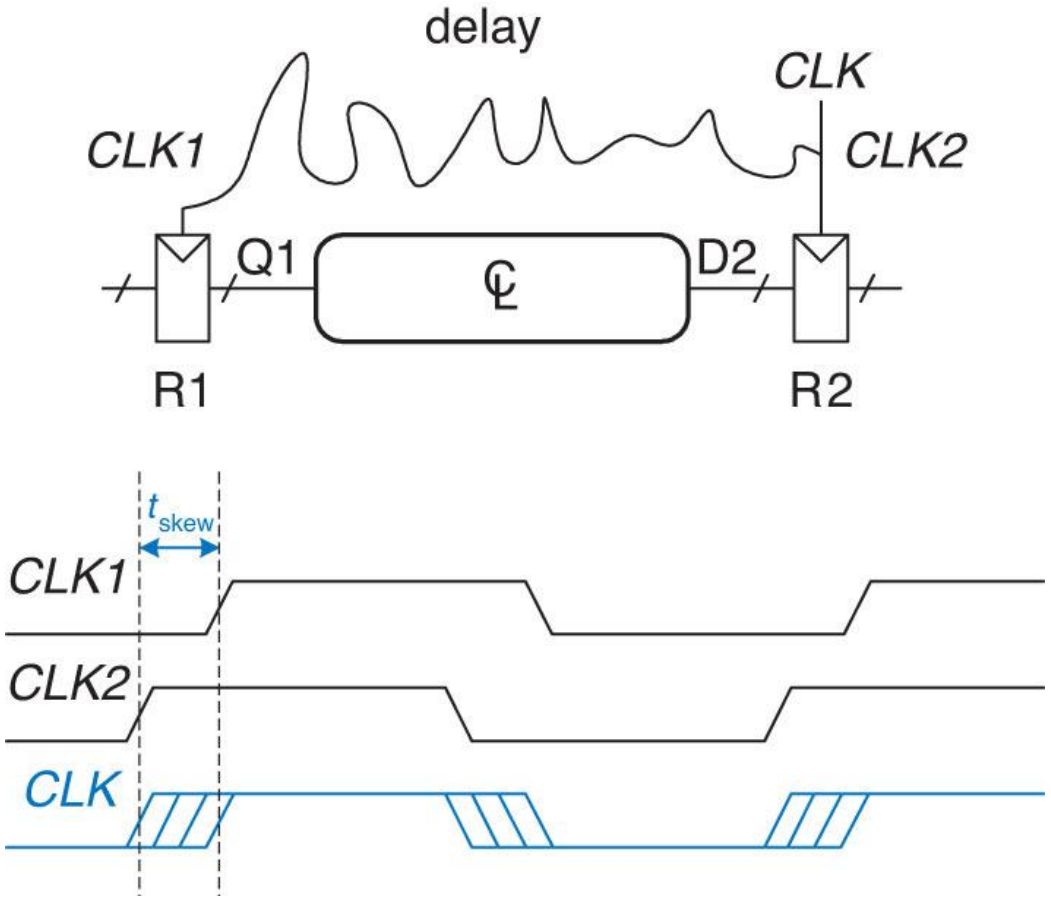


Figure 3.46 Clock skew caused by wire delay

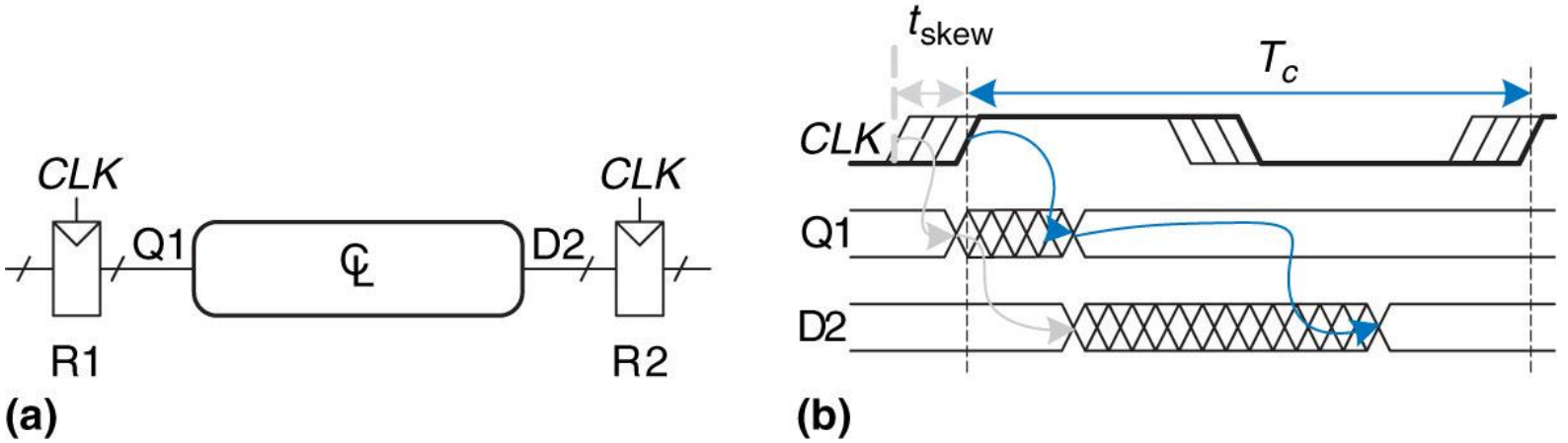


Figure 3.47 Timing diagram with clock skew

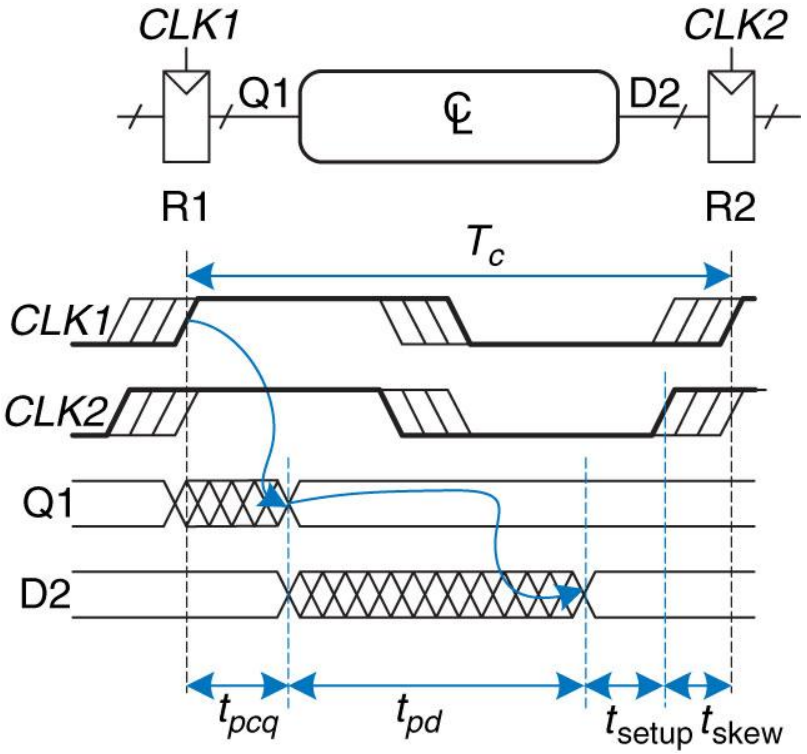


Figure 3.48 Setup time constraint with clock skew

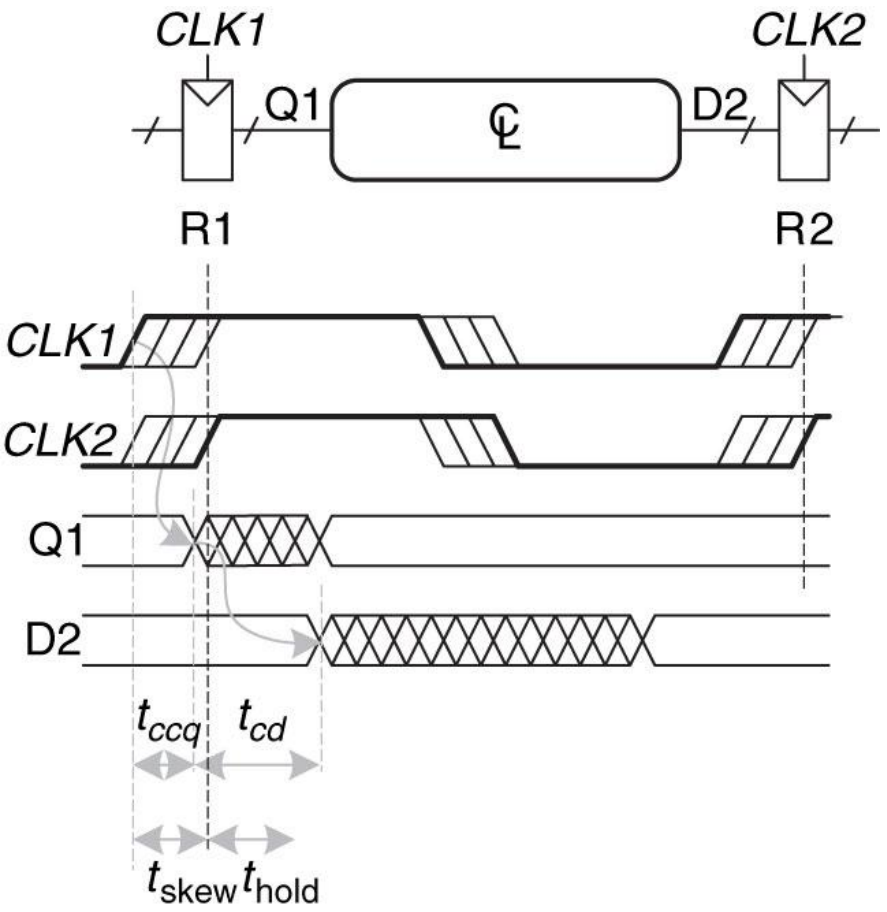


Figure 3.49 Hold time constraint with clock skew

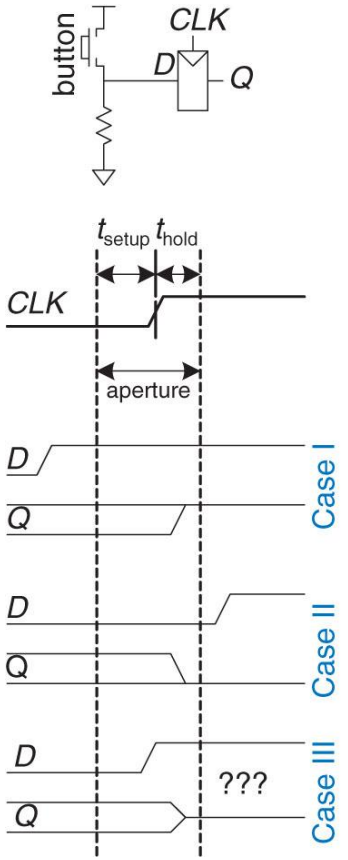


Figure 3.50 Input changing before, after, or during aperture

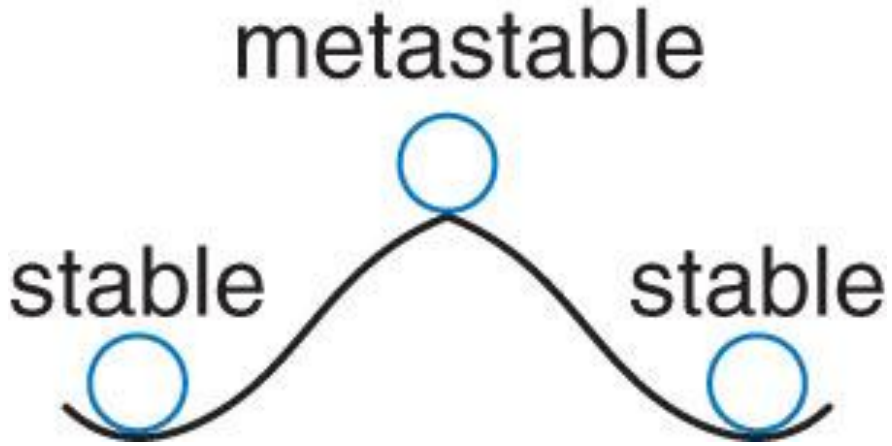


Figure 3.51 Stable and metastable states

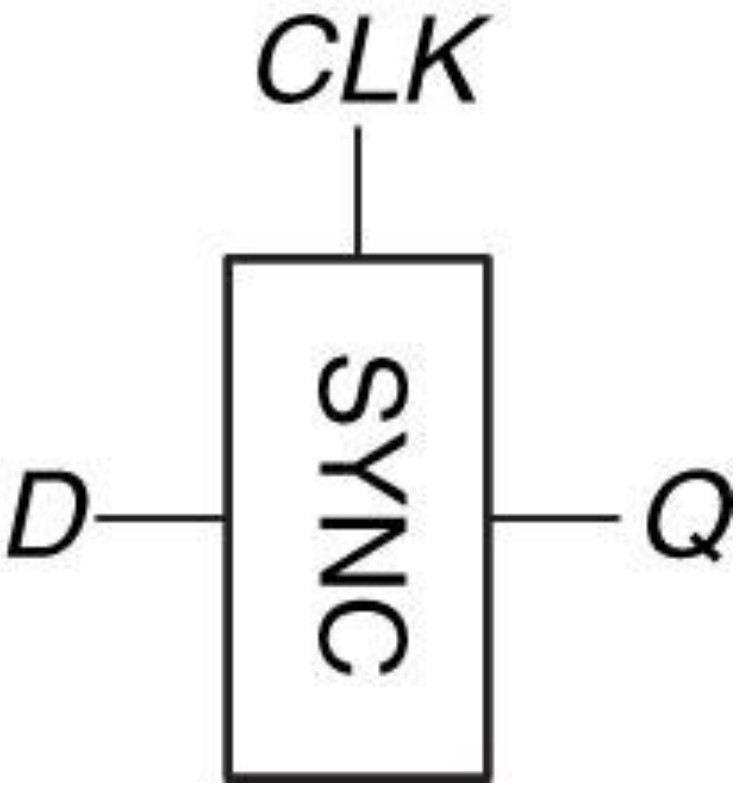


Figure 3.52 Synchronizer symbol

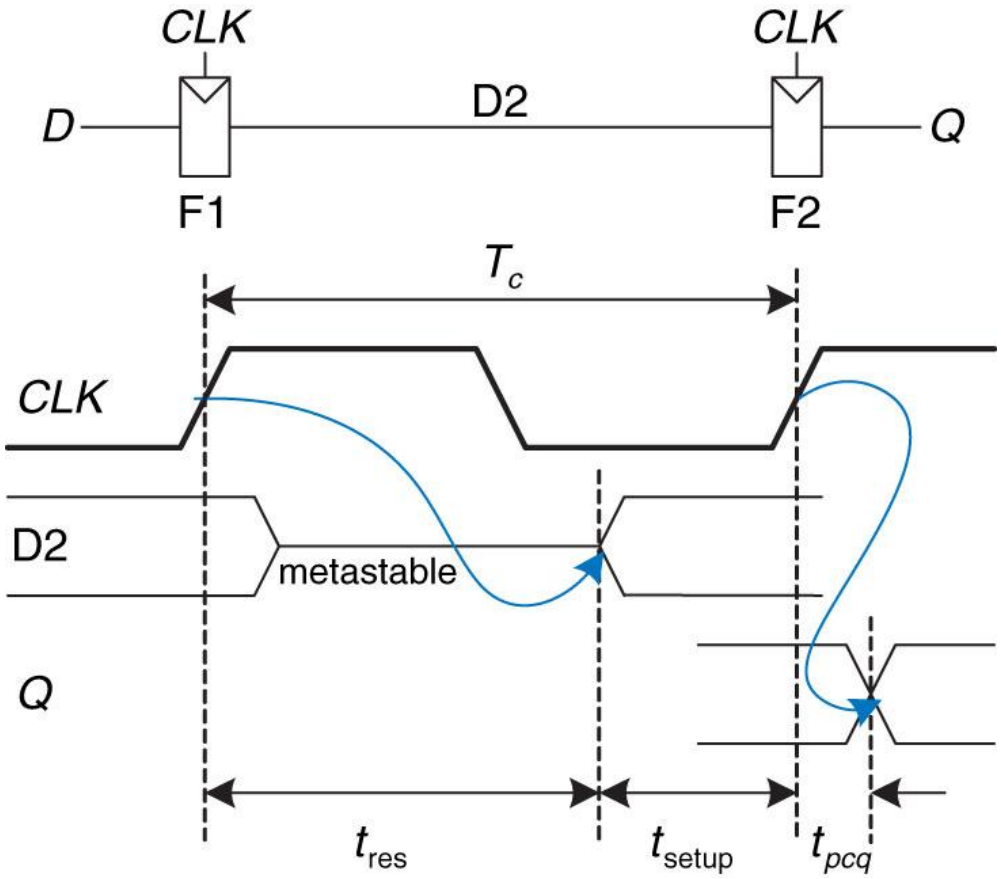


Figure 3.53 Simple synchronizer

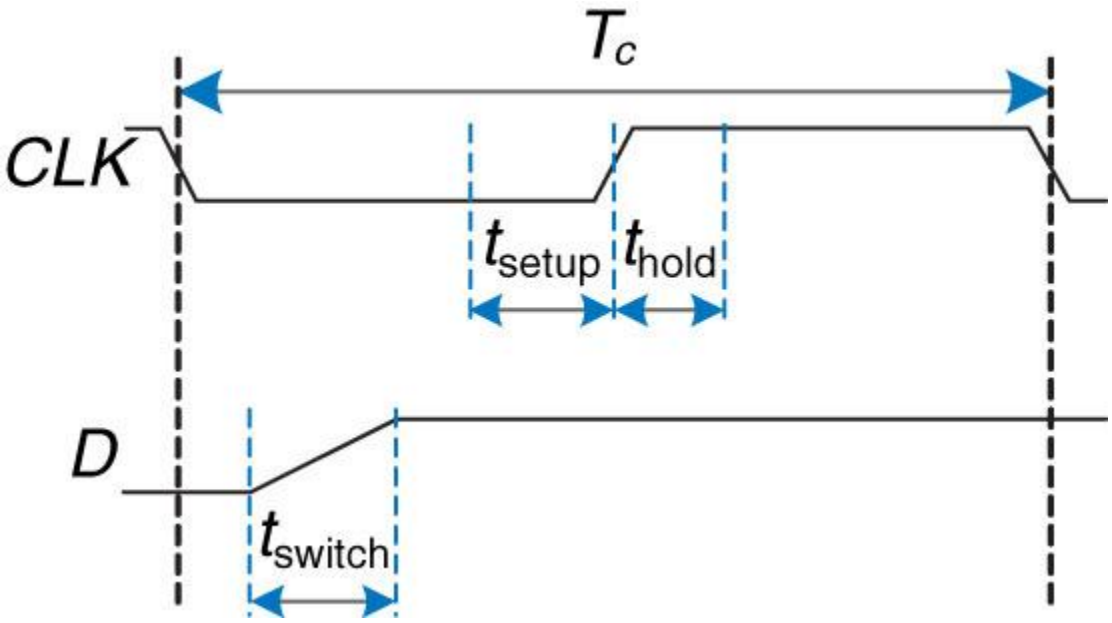


Figure 3.54 Input timing

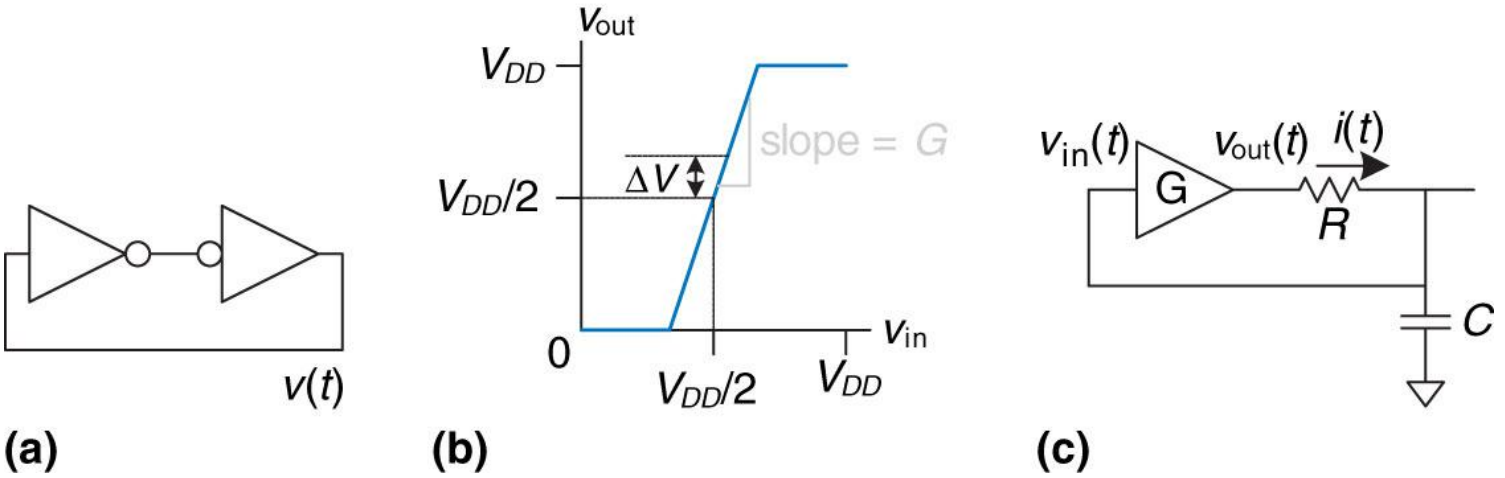


Figure 3.55 Circuit model of bistable device

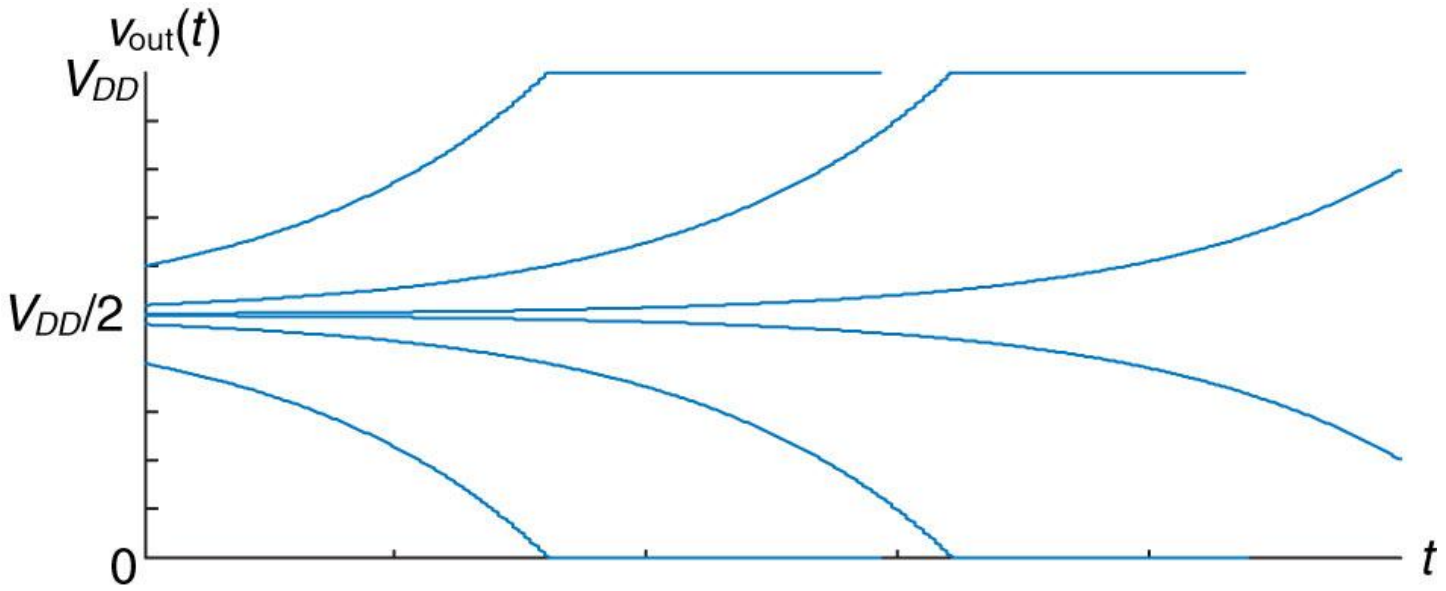


Figure 3.56 Resolution trajectories

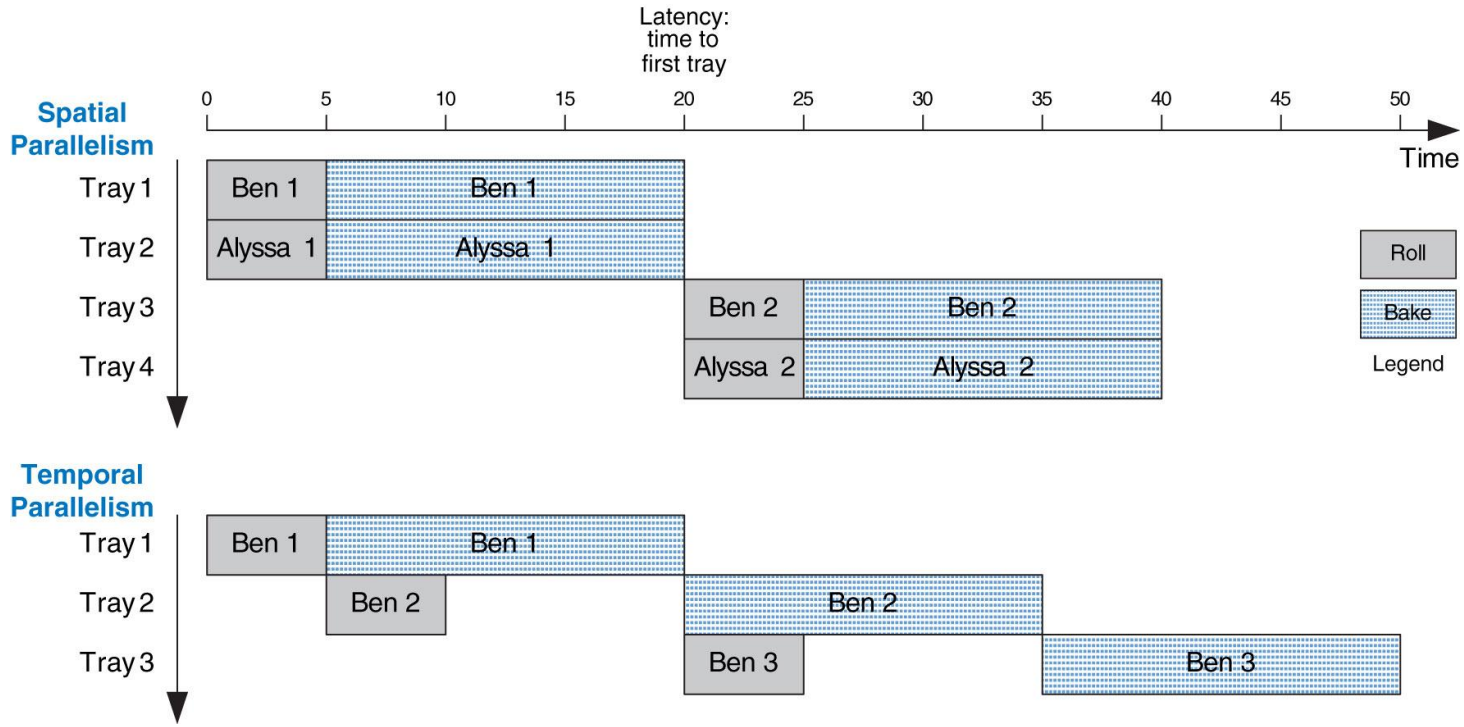


Figure 3.57 Spatial and temporal parallelism in the cookie kitchen

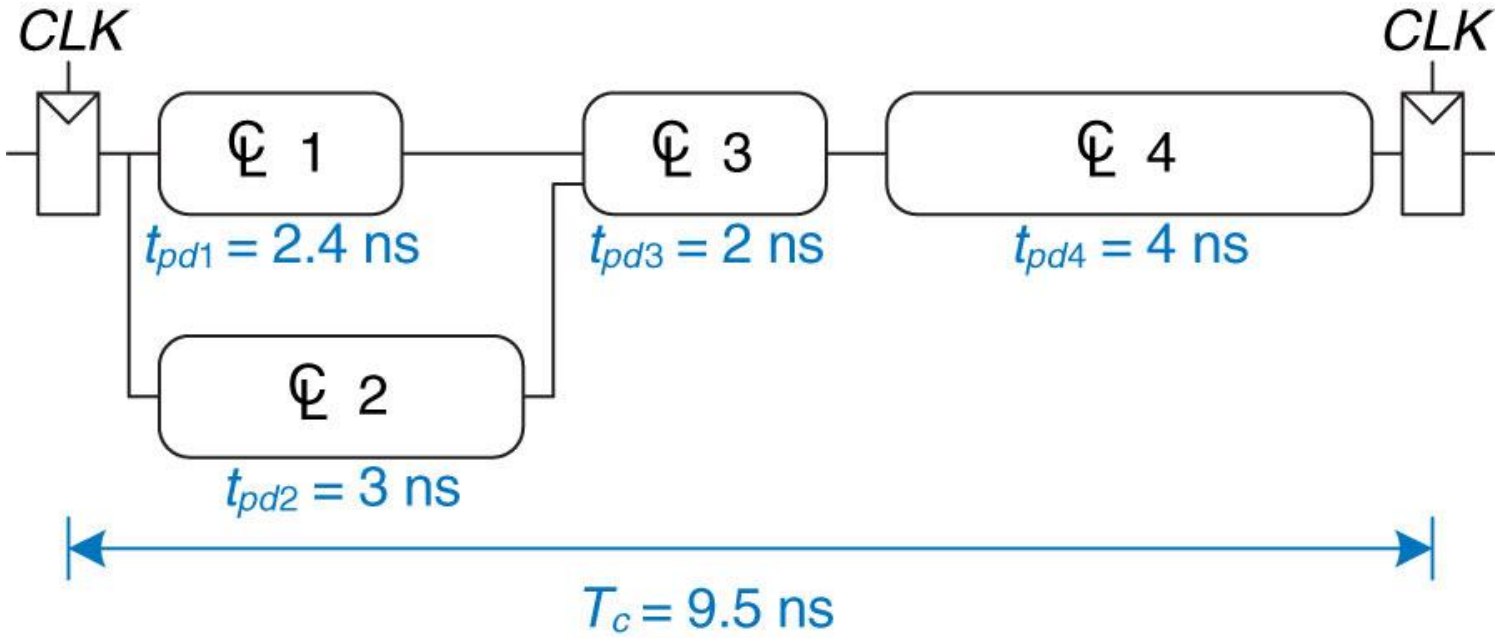


Figure 3.58 Circuit with no pipelining

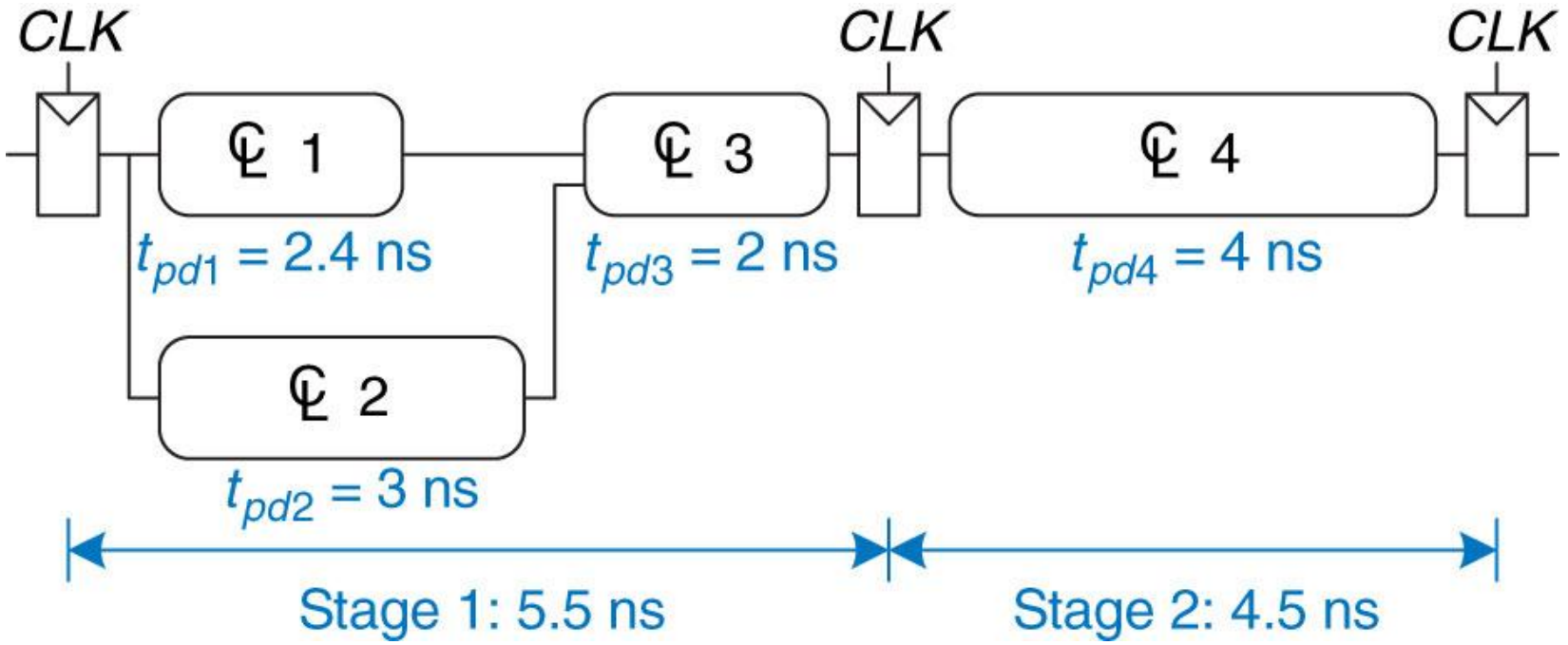


Figure 3.59 Circuit with two-stage pipeline

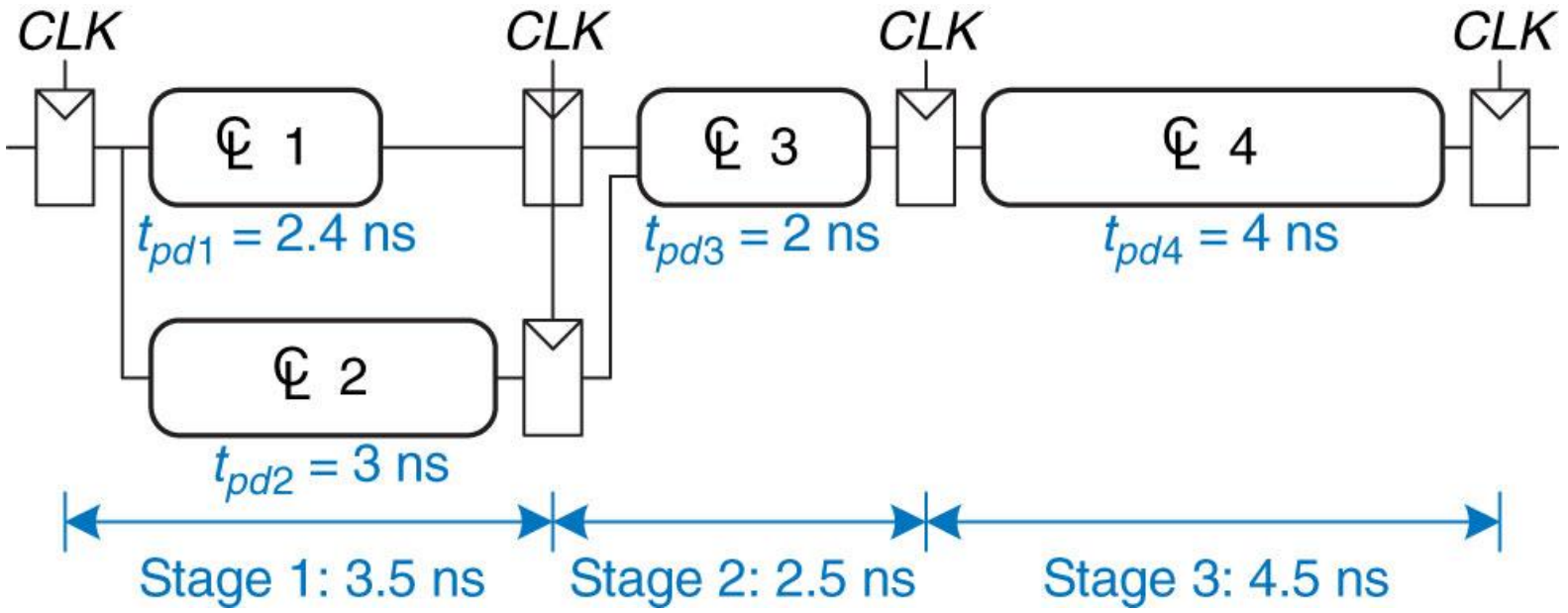


Figure 3.60 Circuit with three-stage pipeline

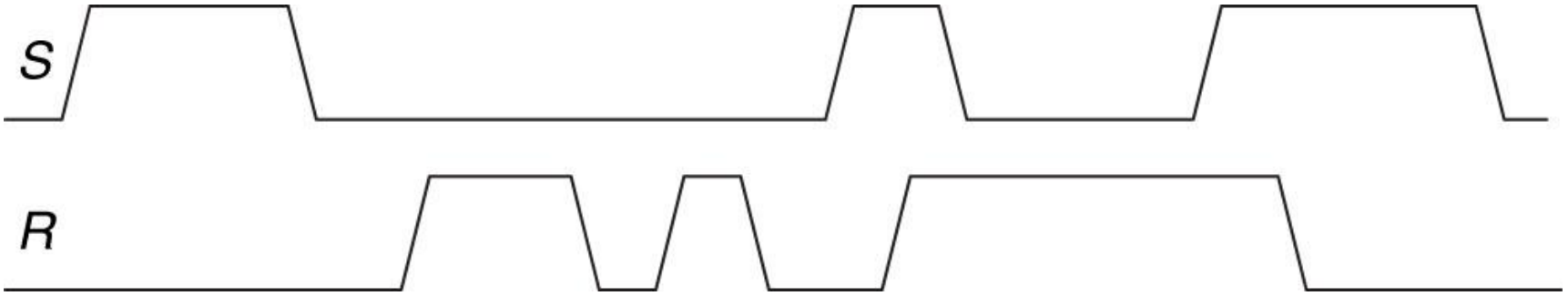


Figure 3.61 Input waveforms of SR latch for Exercise 3.1

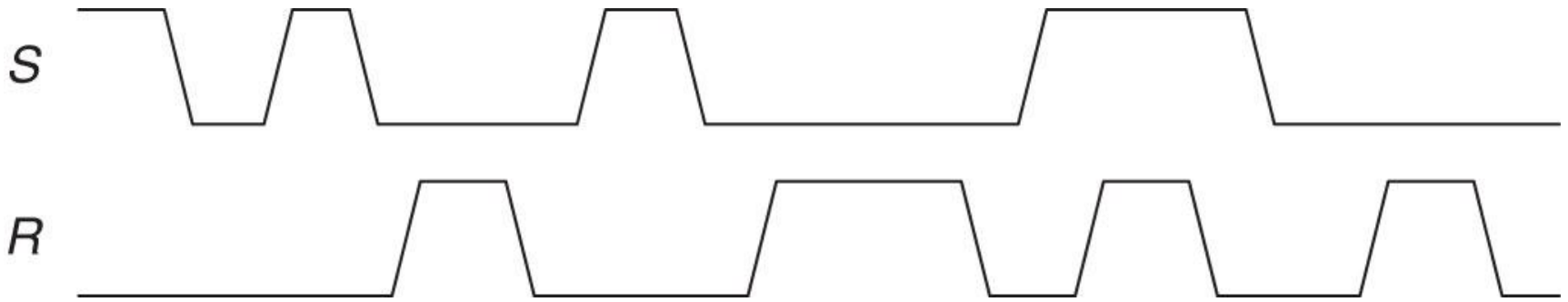


Figure 3.62 Input waveforms of SR latch for Exercise 3.2

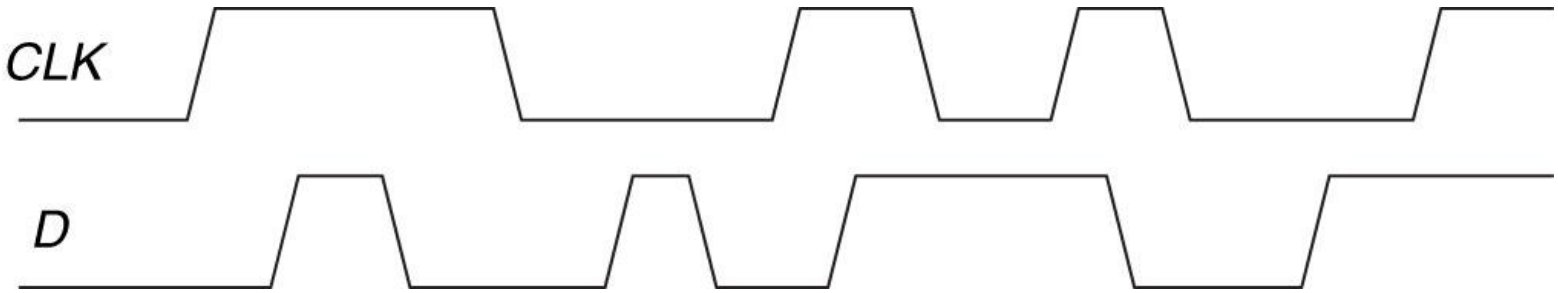


Figure 3.63 Input waveforms of D latch or flip-flop for Exercises 3.3 and 3.5

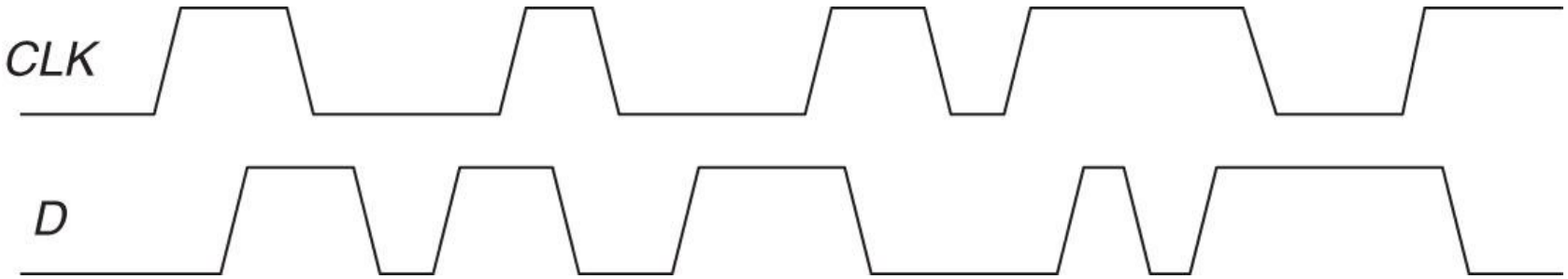


Figure 3.64 Input waveforms of D latch or flip-flop for Exercises 3.4 and 3.6

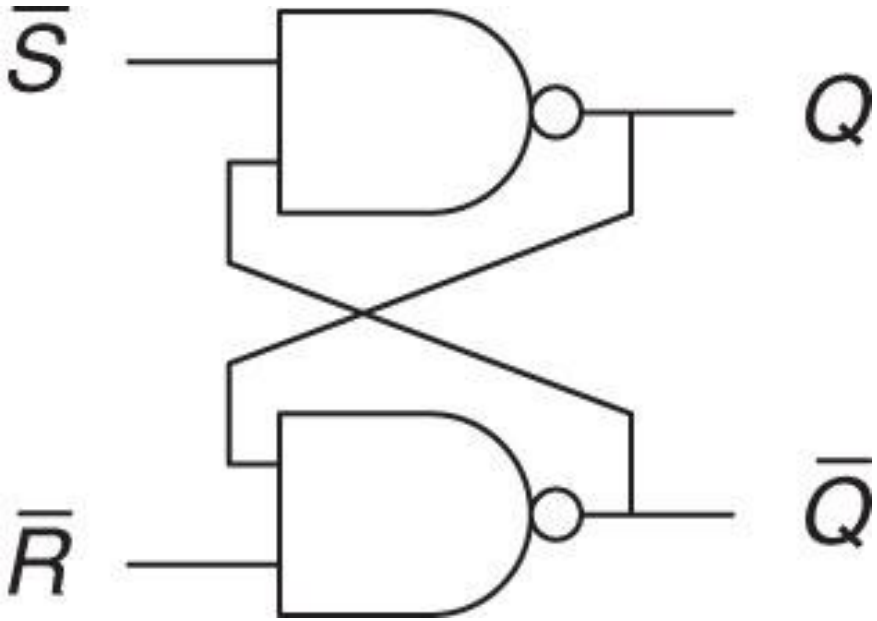


Figure 3.65 Mystery circuit

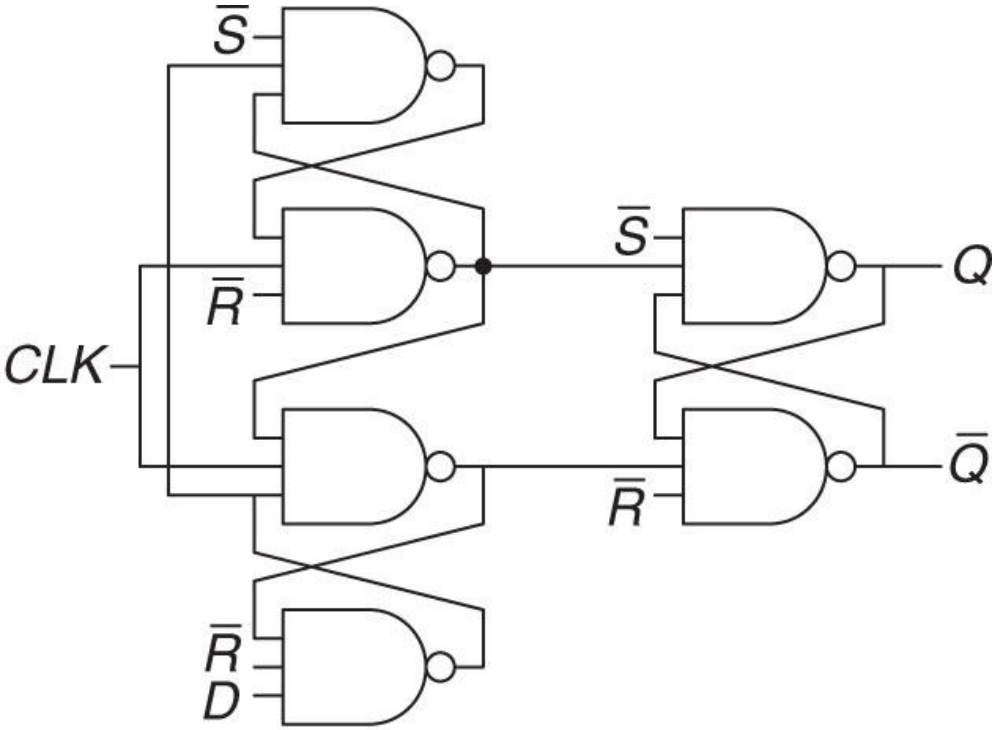


Figure 3.66 Mystery circuit

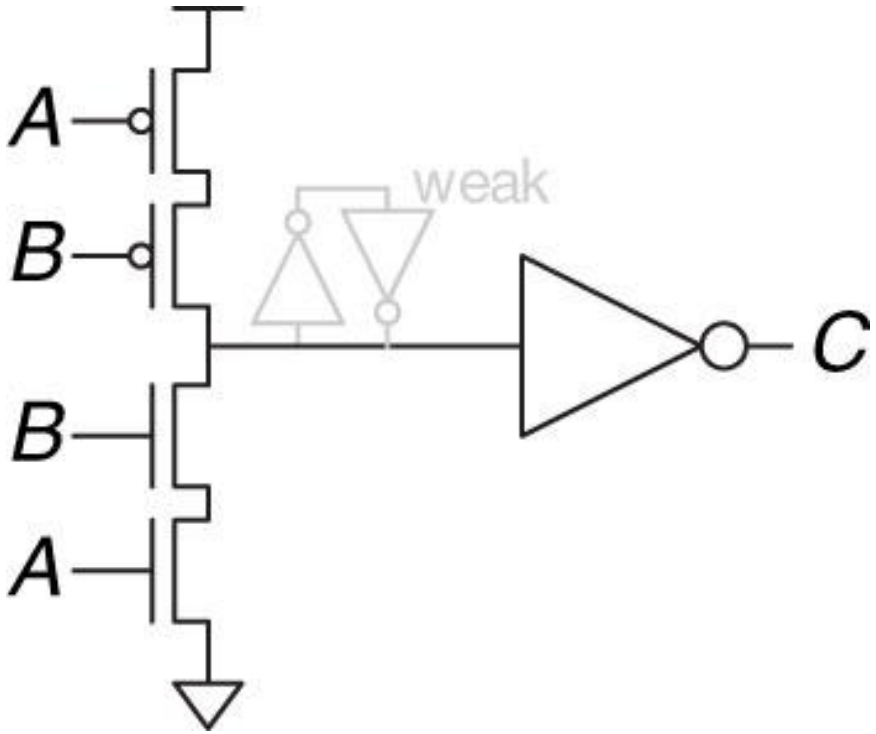


Figure 3.67 Muller C-element

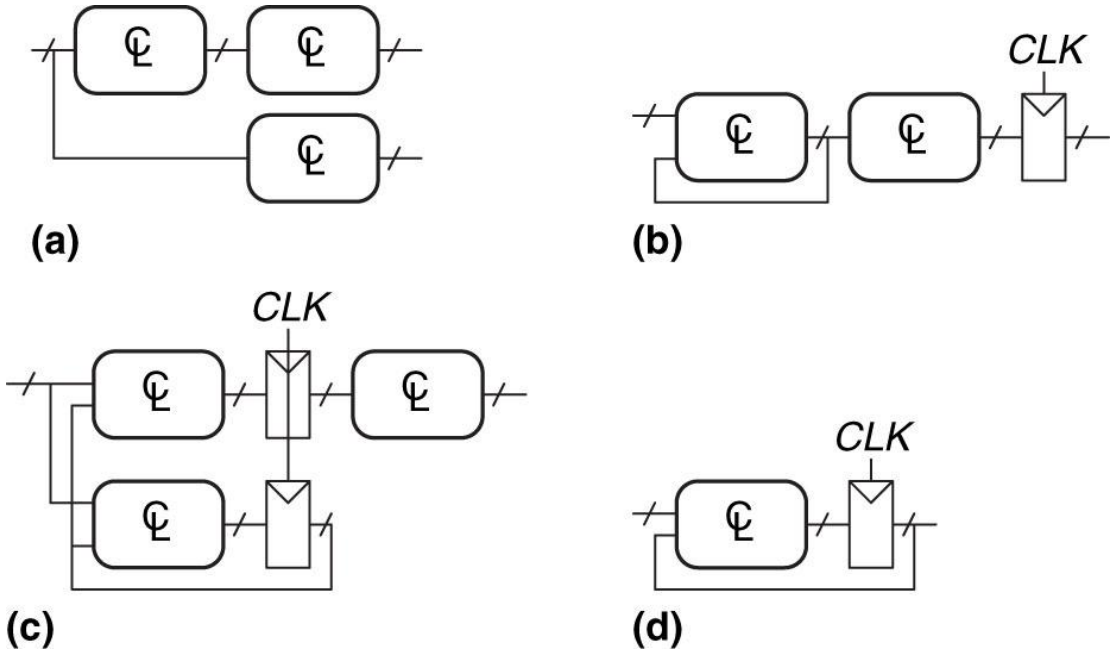


Figure 3.68 Circuits

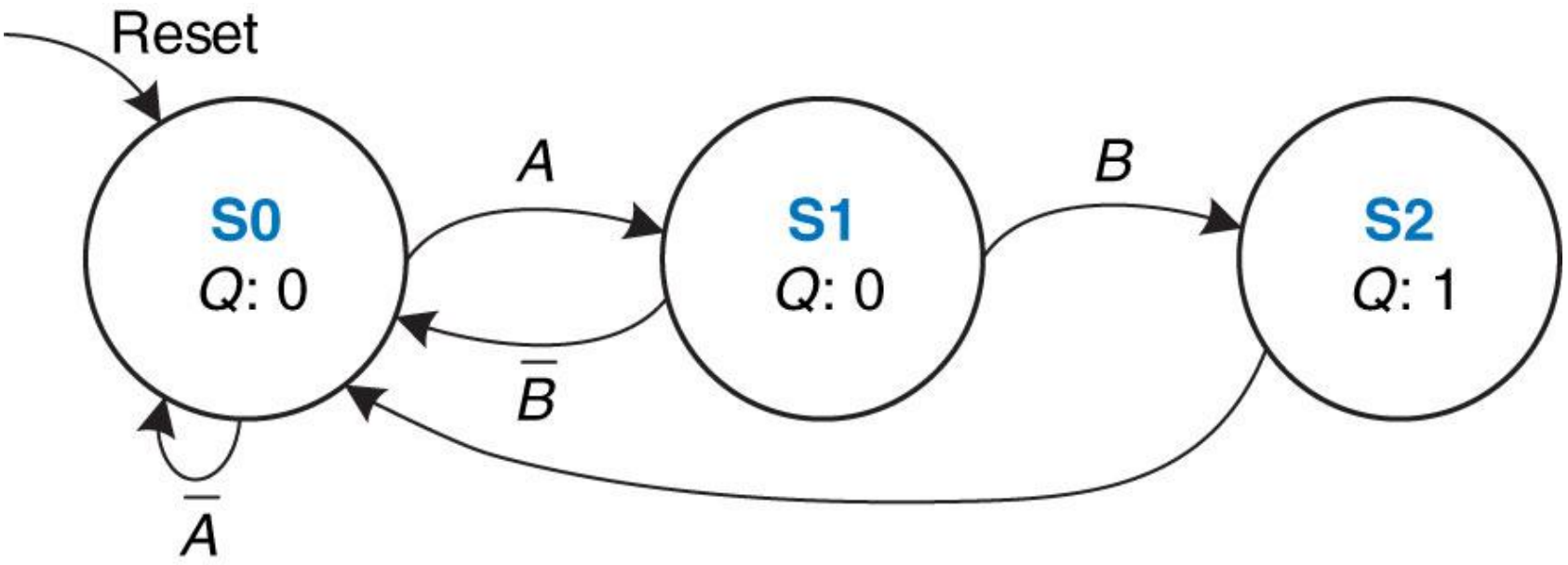


Figure 3.69 State transition diagram

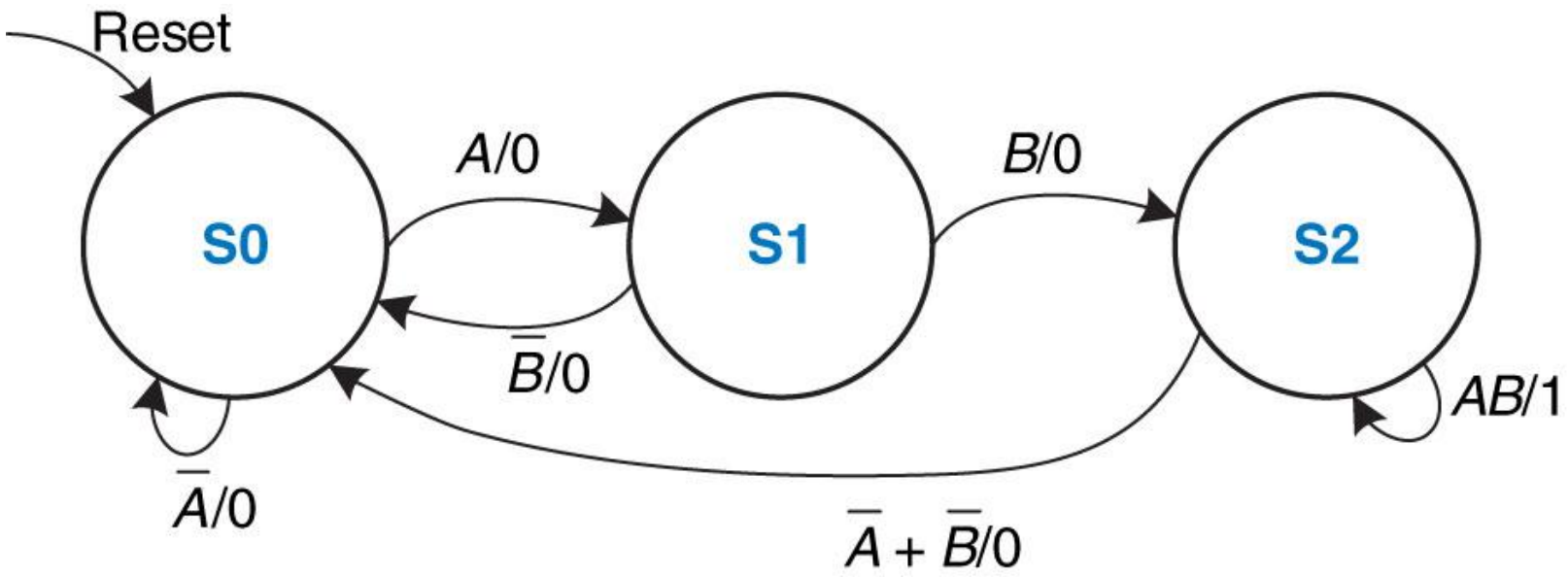


Figure 3.70 State transition diagram

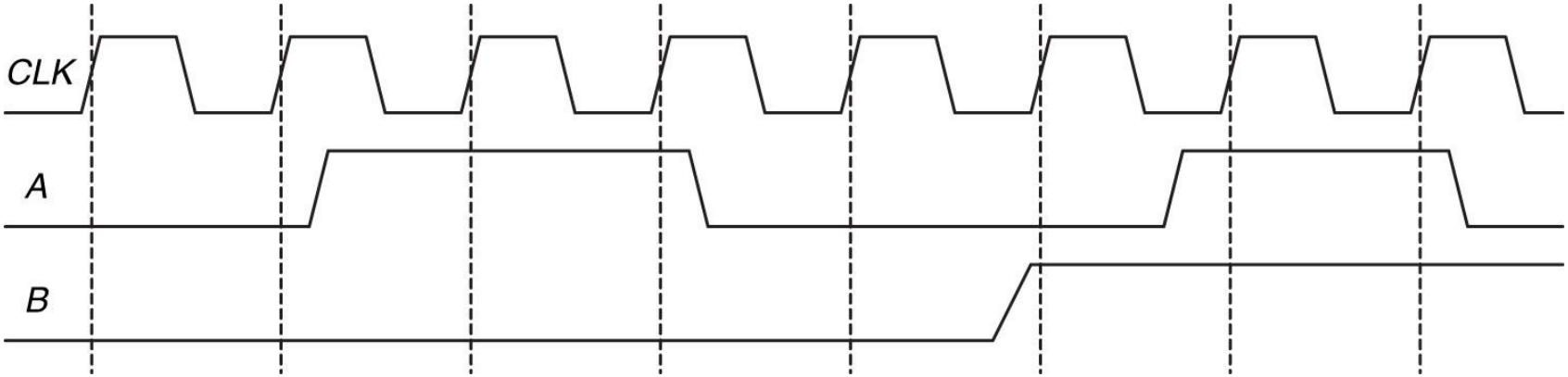


Figure 3.71 FSM input waveforms

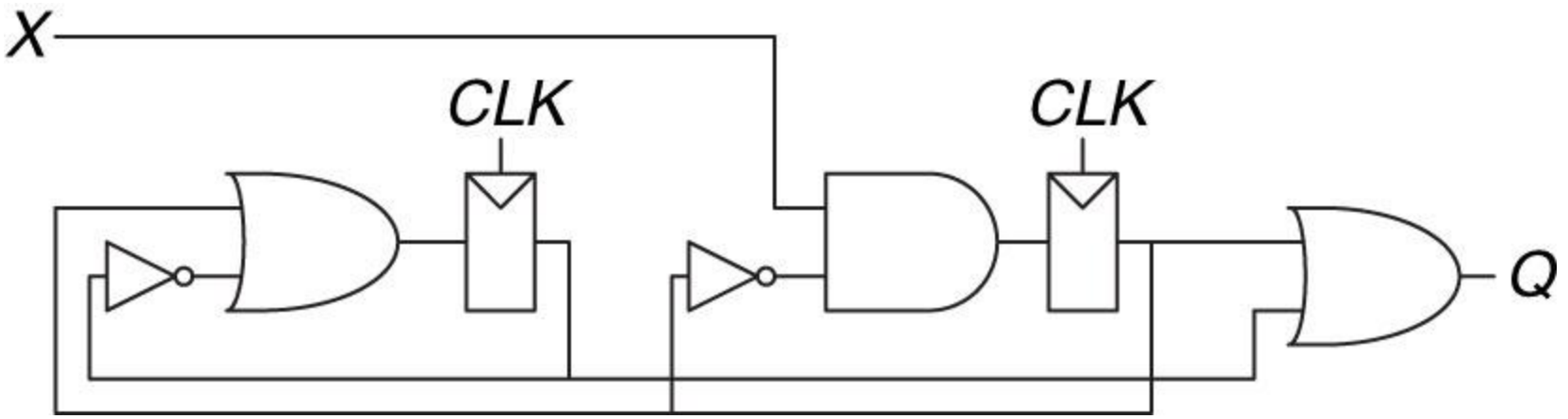


Figure 3.72 FSM schematic

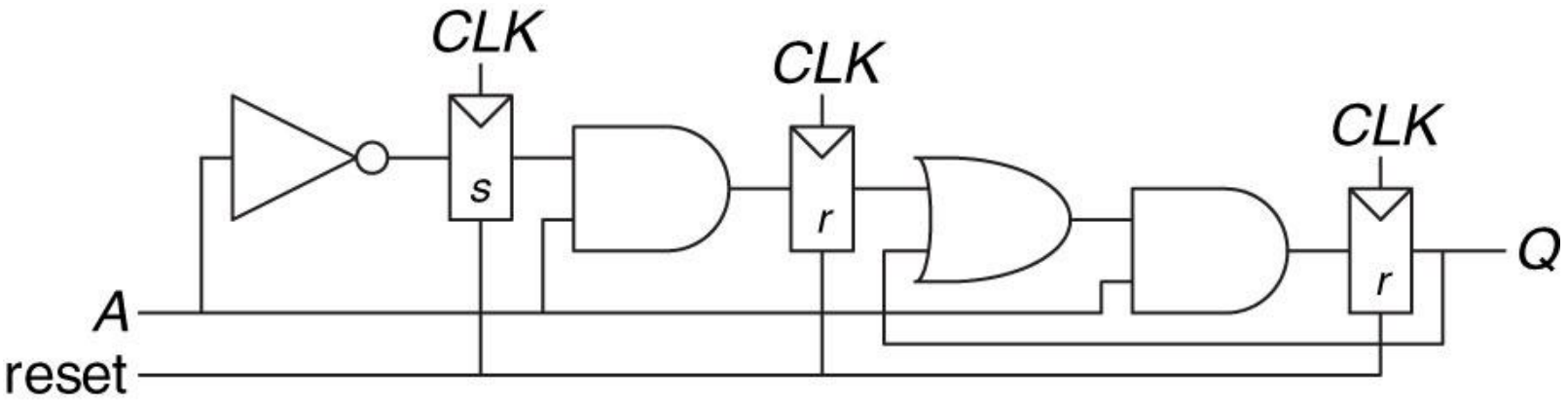


Figure 3.73 FSM schematic

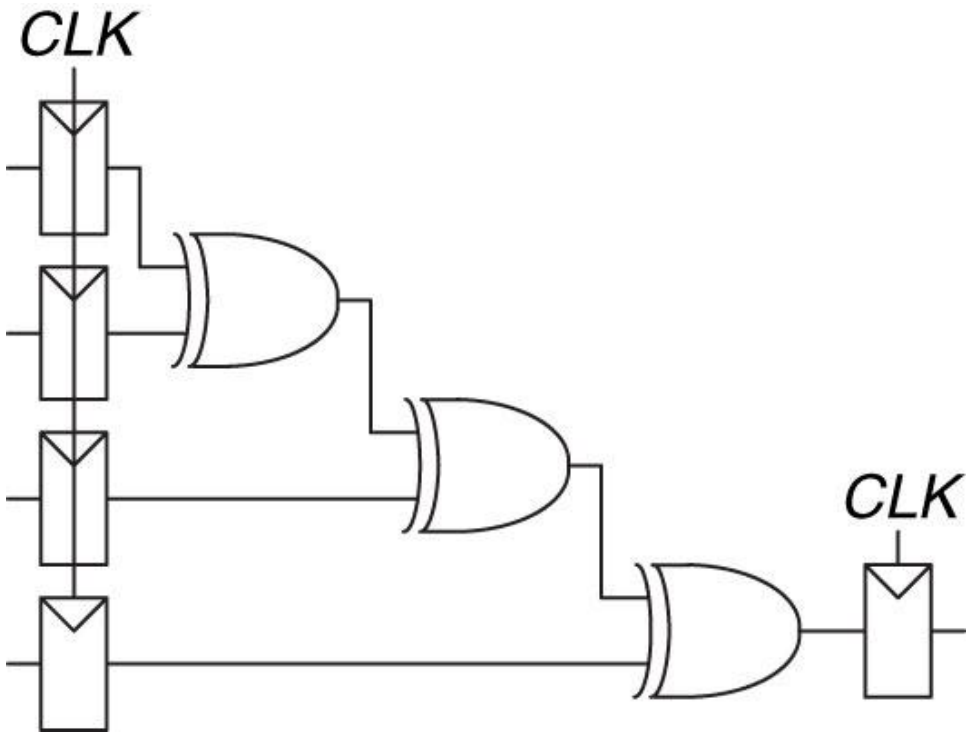


Figure 3.74 Registered four-input XOR circuit

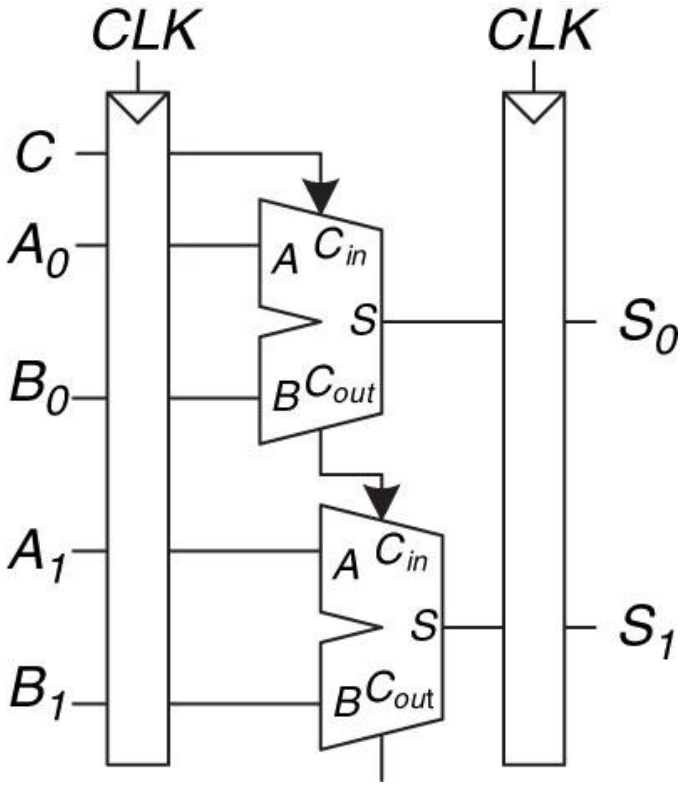


Figure 3.75 2-bit adder schematic

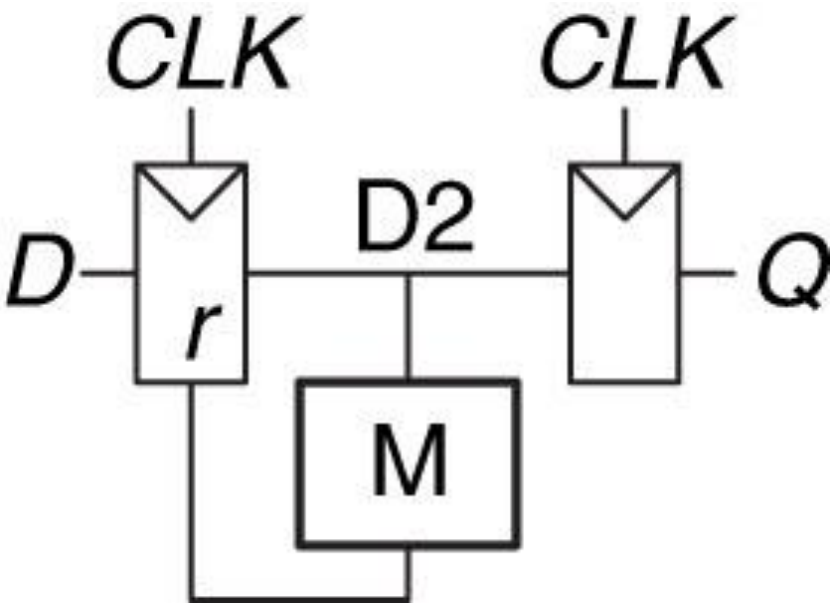


Figure 3.76 · New and improved · synchronizer

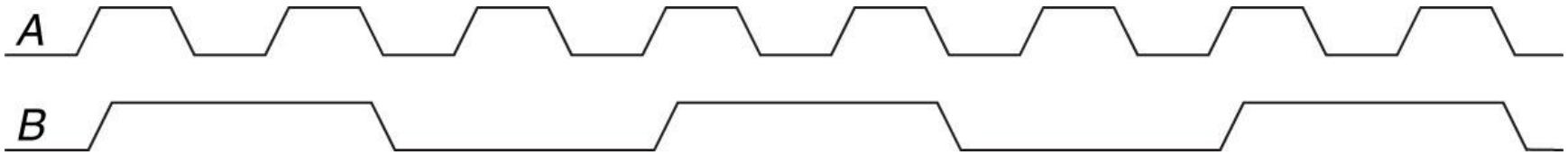


Figure 3.77 Signal waveforms

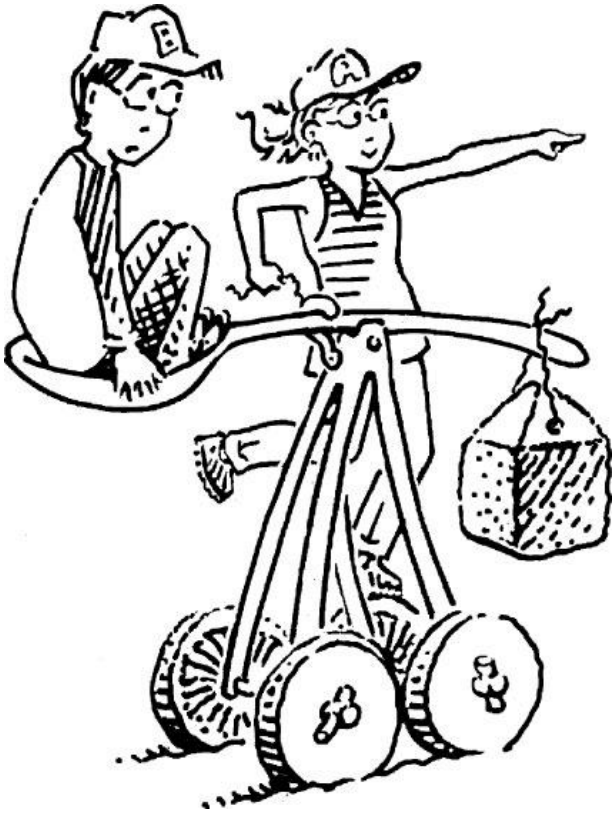


Figure M 01

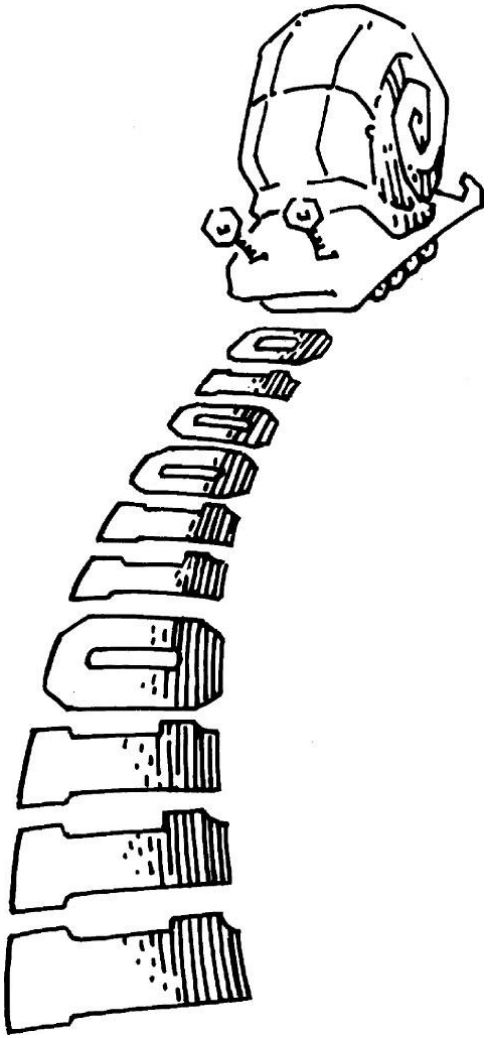
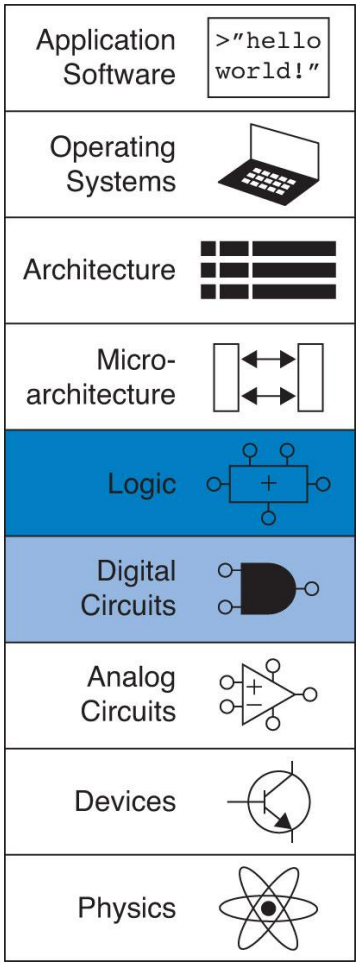


Figure M 02

Figure M 03

Figure M 04

Figure M 05



UNN Figure 1