Chapter 4

Hardware Description Languages

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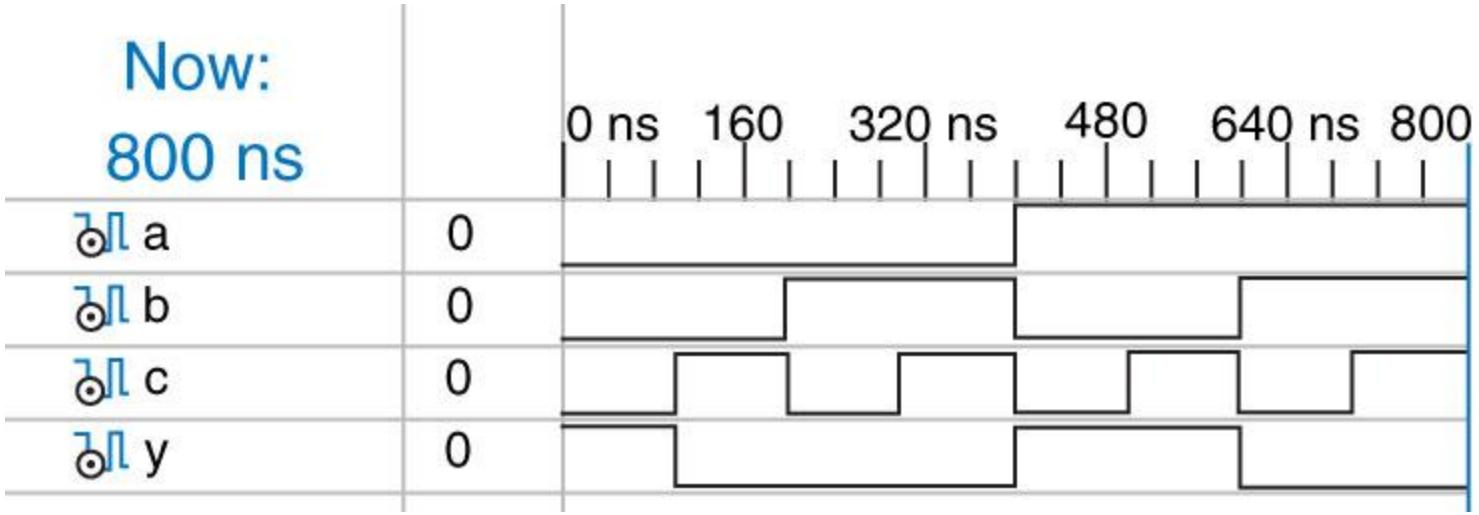

Figure 4.1 Simulation waveforms

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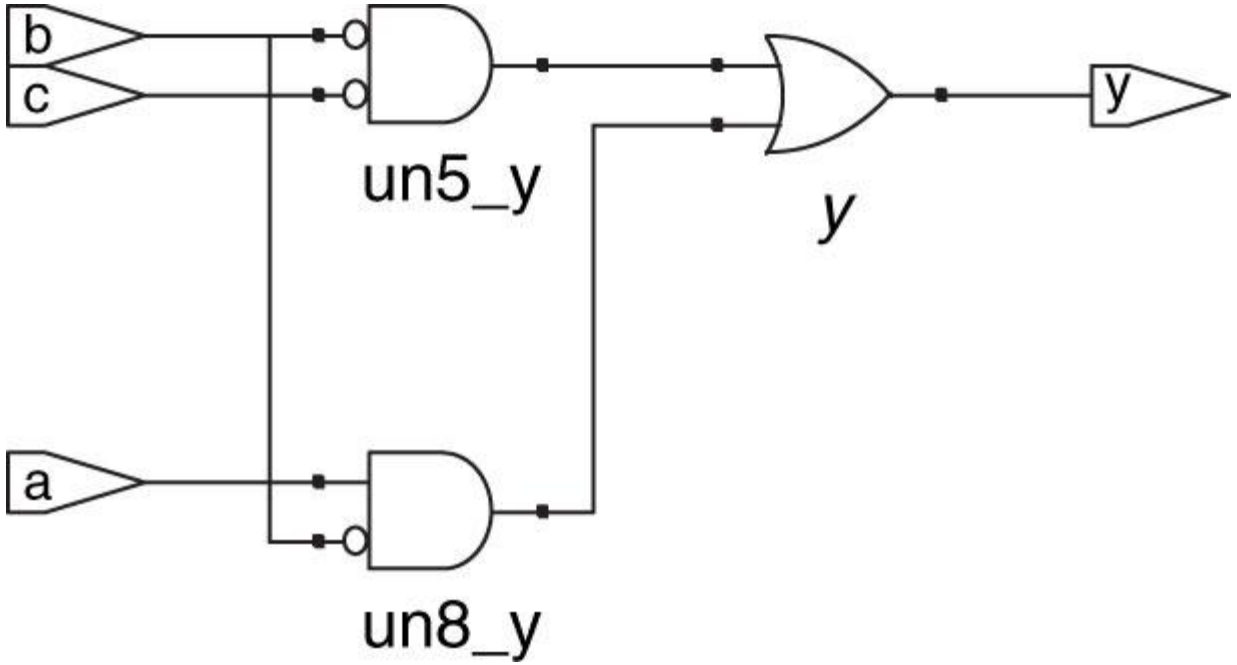

Figure 4.2 Synthesized circuit

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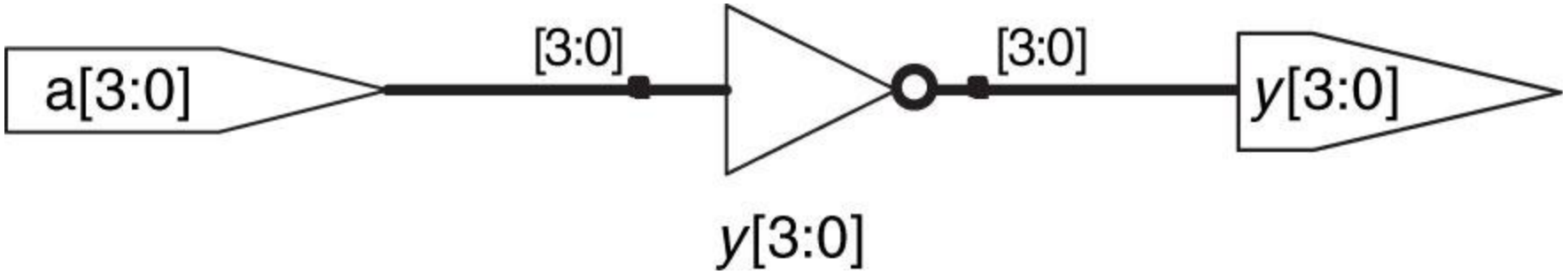

Figure 4.3 inv synthesized circuit

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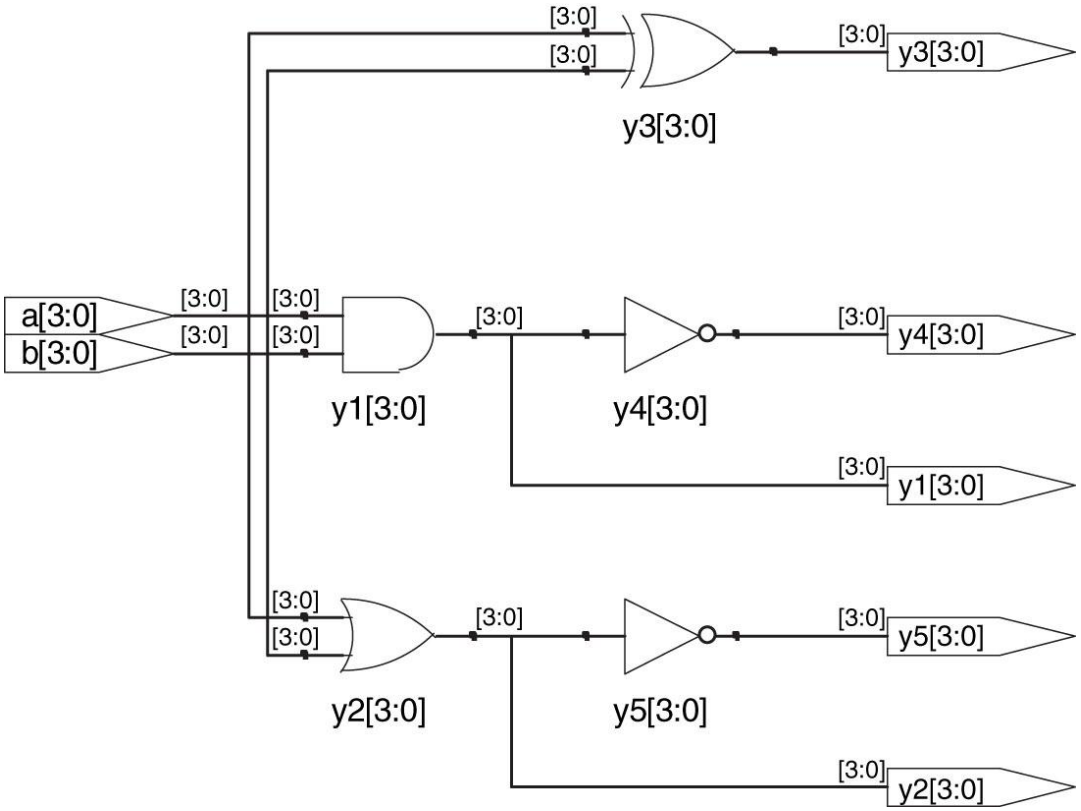

Figure 4.4 gates synthesized circuit

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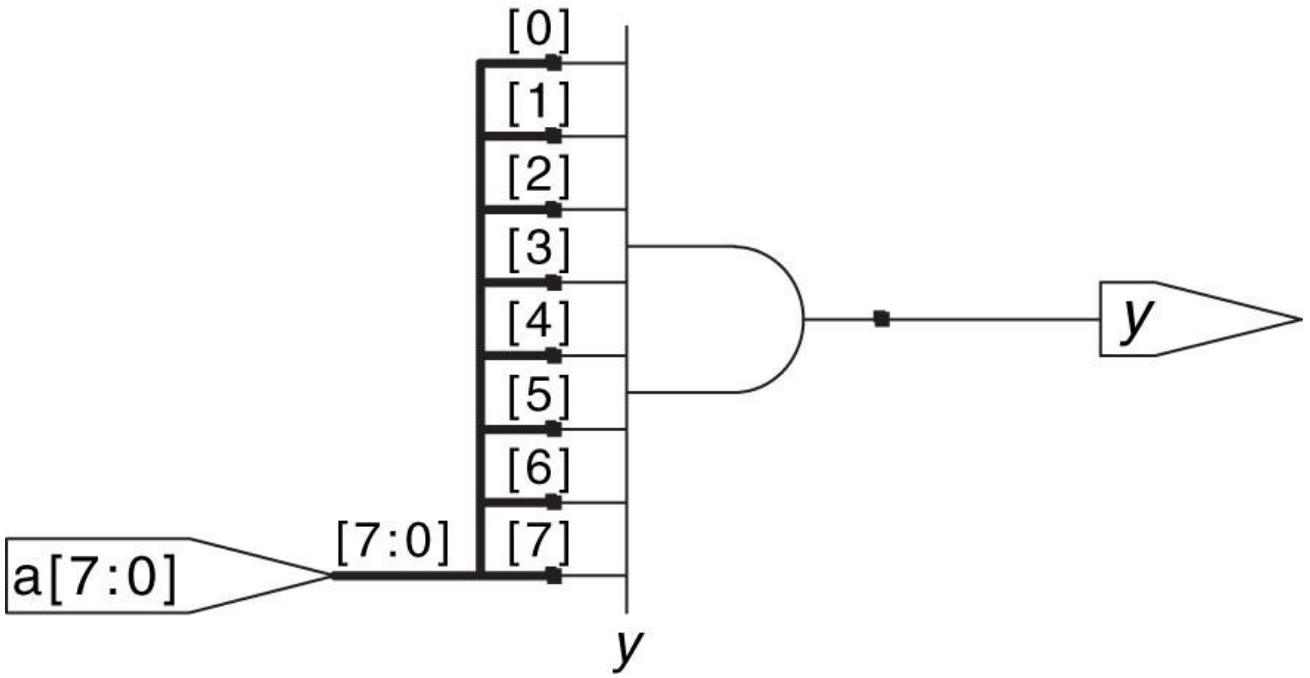

Figure 4.5 and8 synthesized circuit

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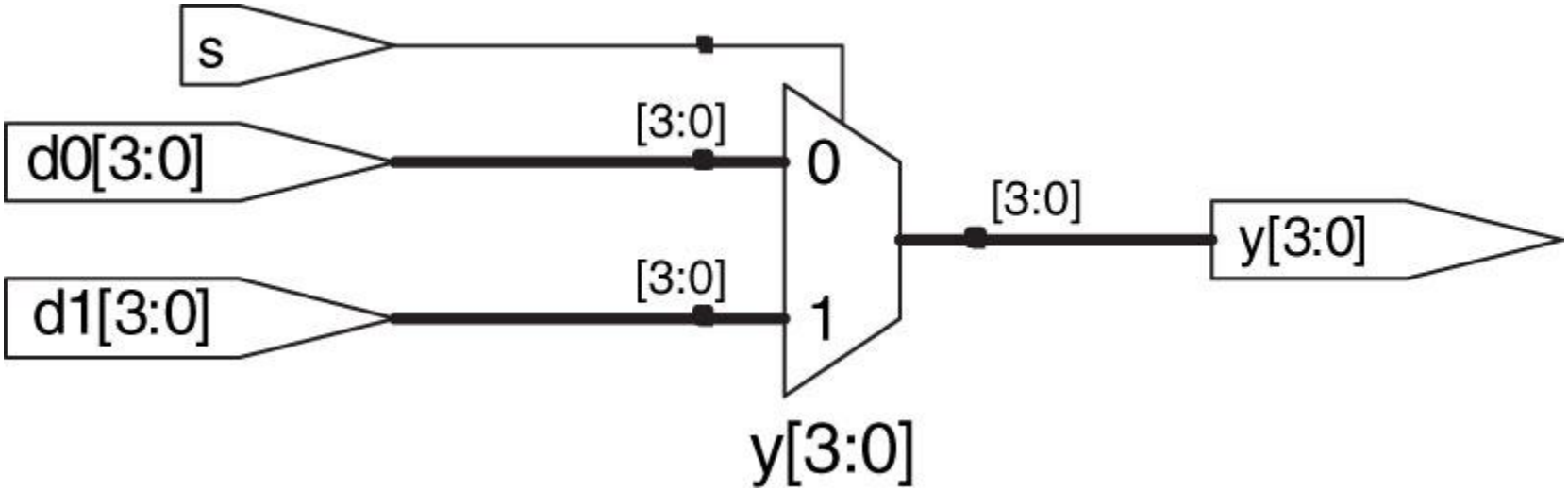

Figure 4.6 mux2 synthesized circuit

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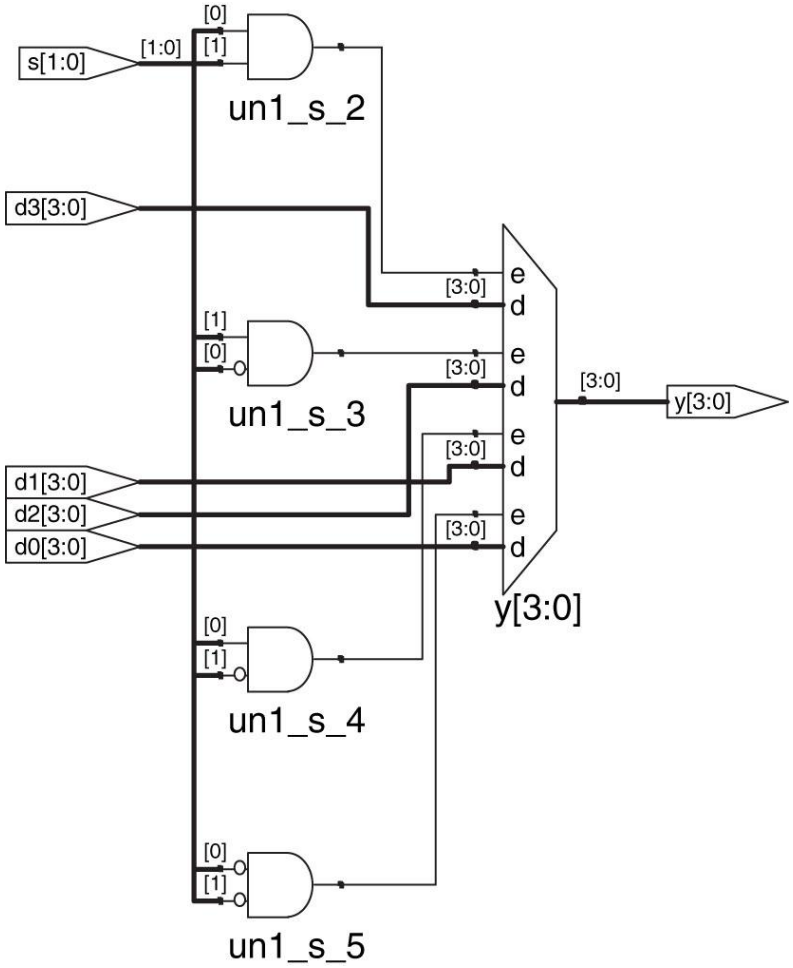

Figure 4.7 mux4 synthesized circuit

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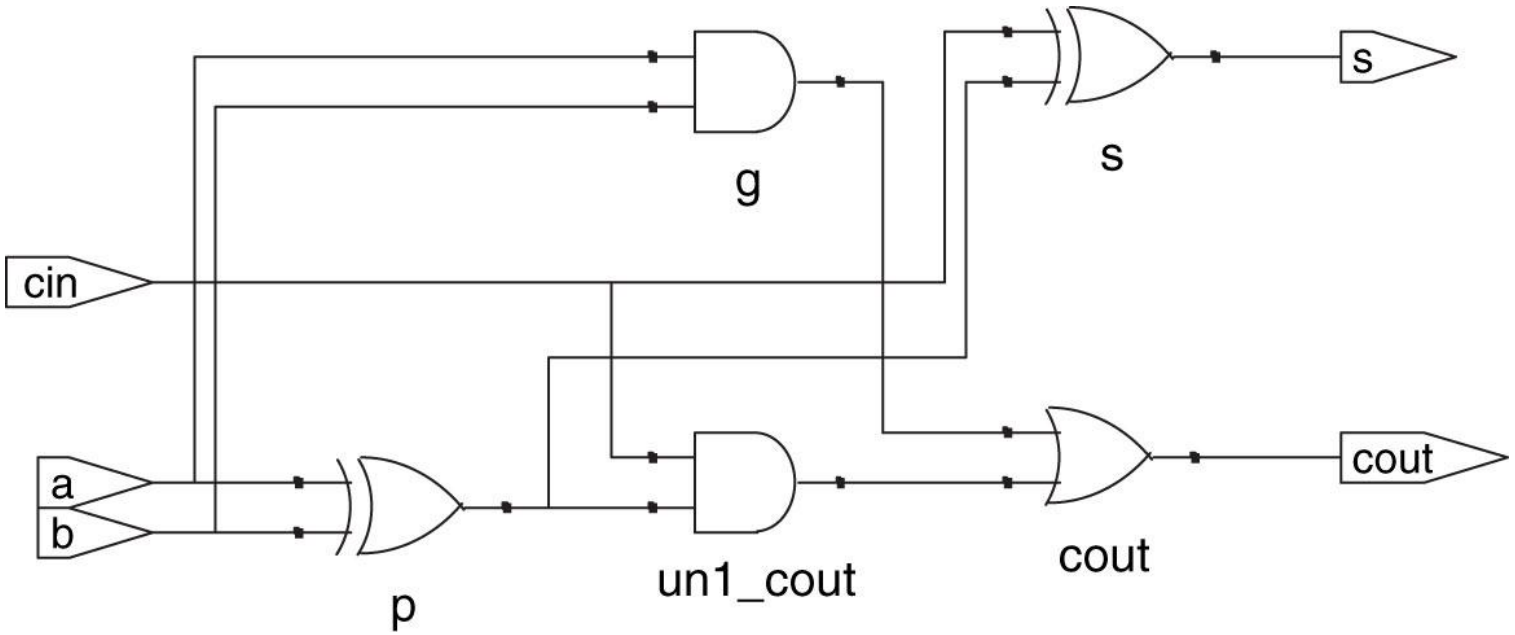

Figure 4.8 fulladder synthesized circuit

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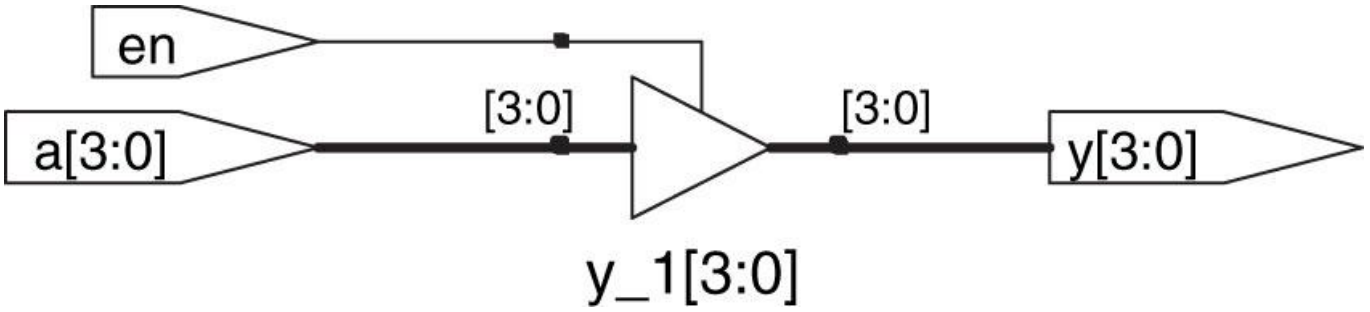

Figure 4.9 tristate synthesized circuit

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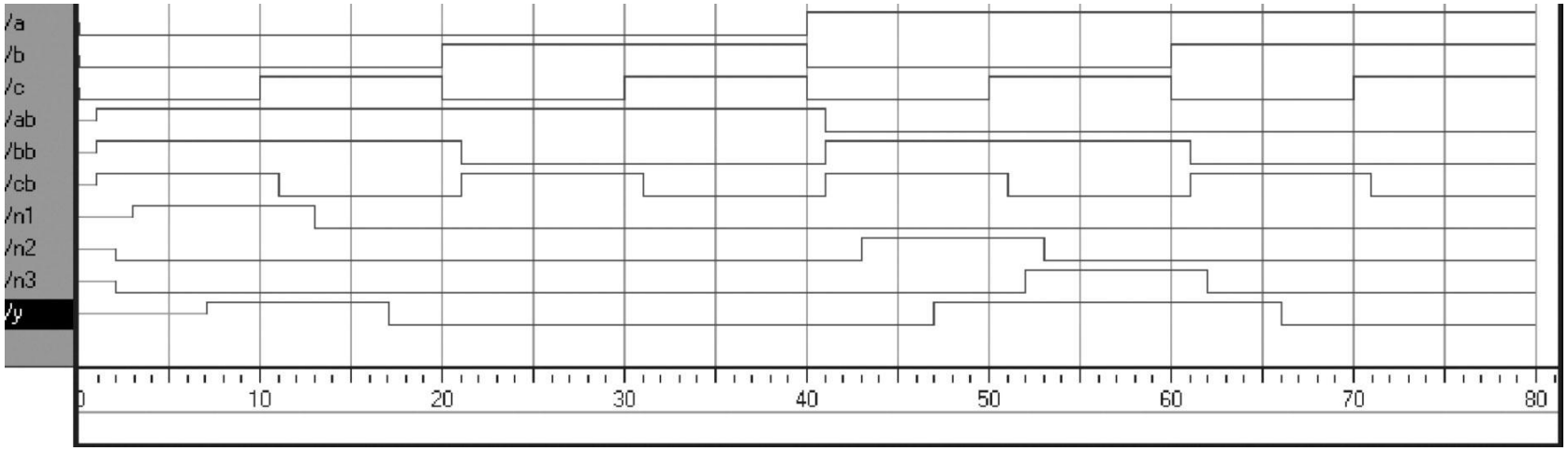

Figure 4.10 Example simulation waveforms with delays (from the ModelSim simulator)

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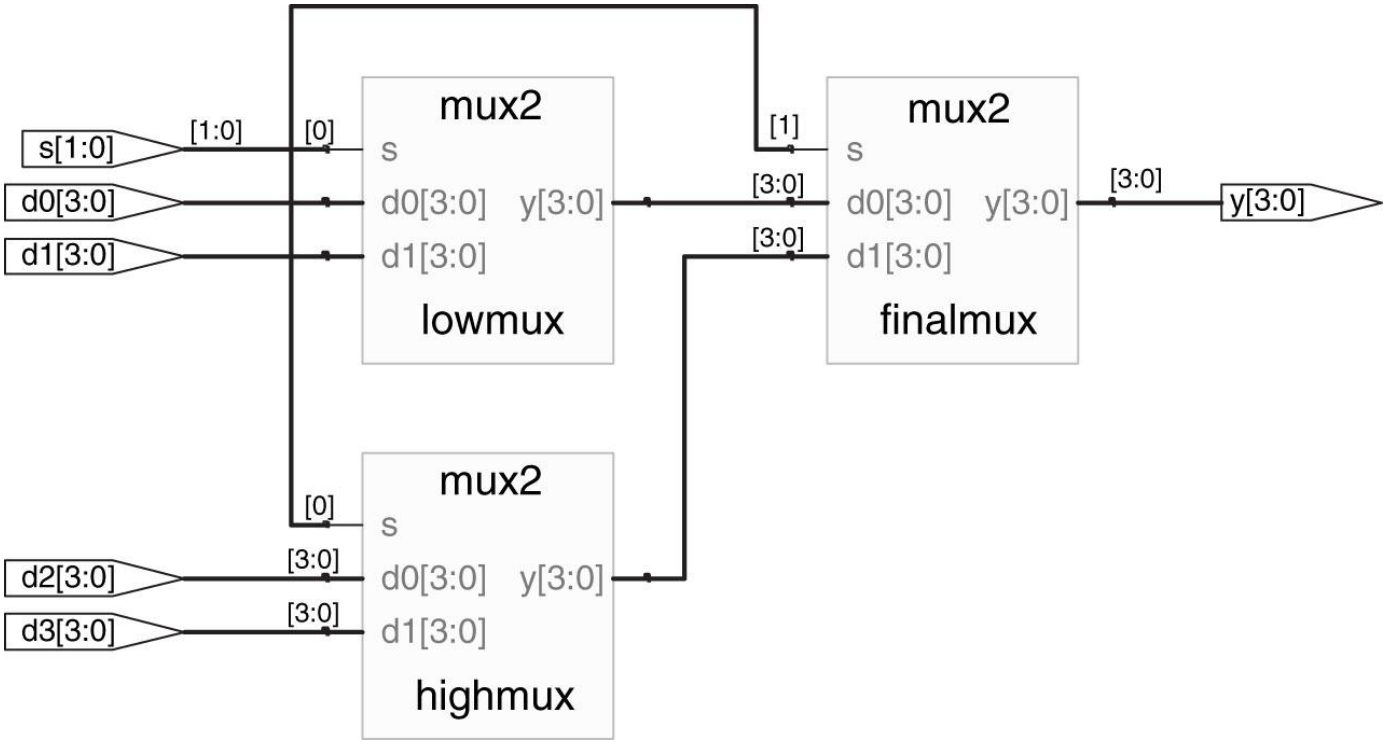

Figure 4.11 mux4 synthesized circuit

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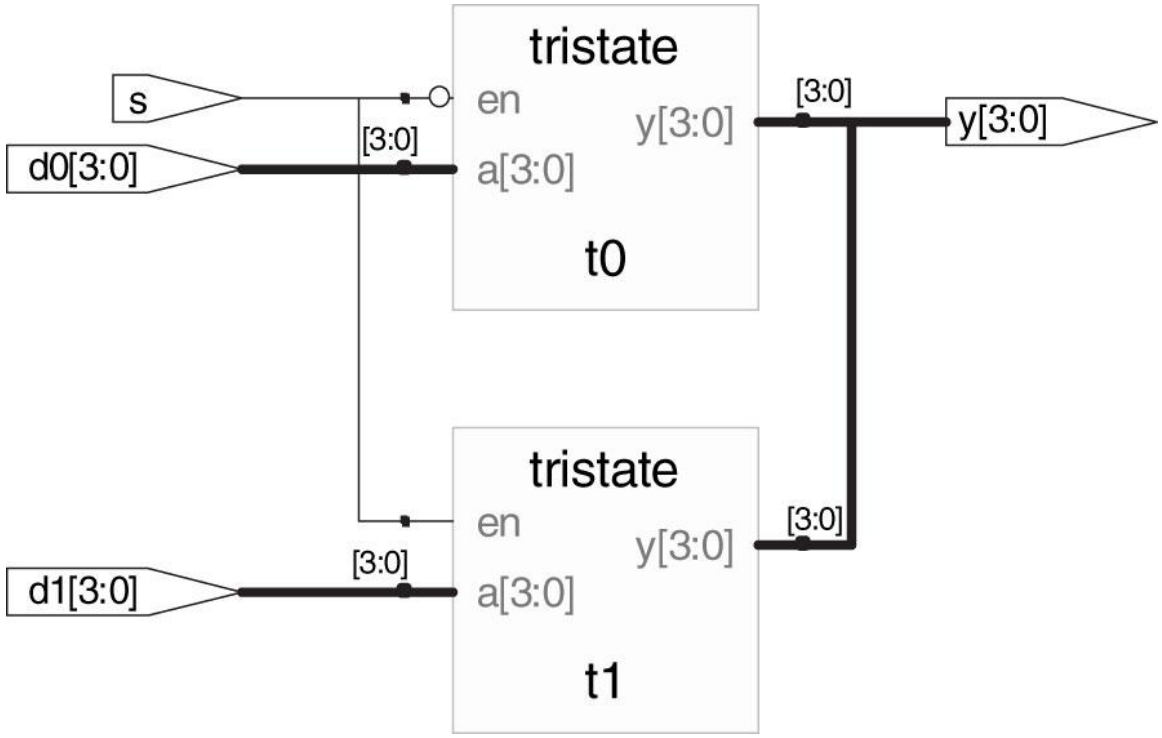

Figure 4.12 mux2 synthesized circuit

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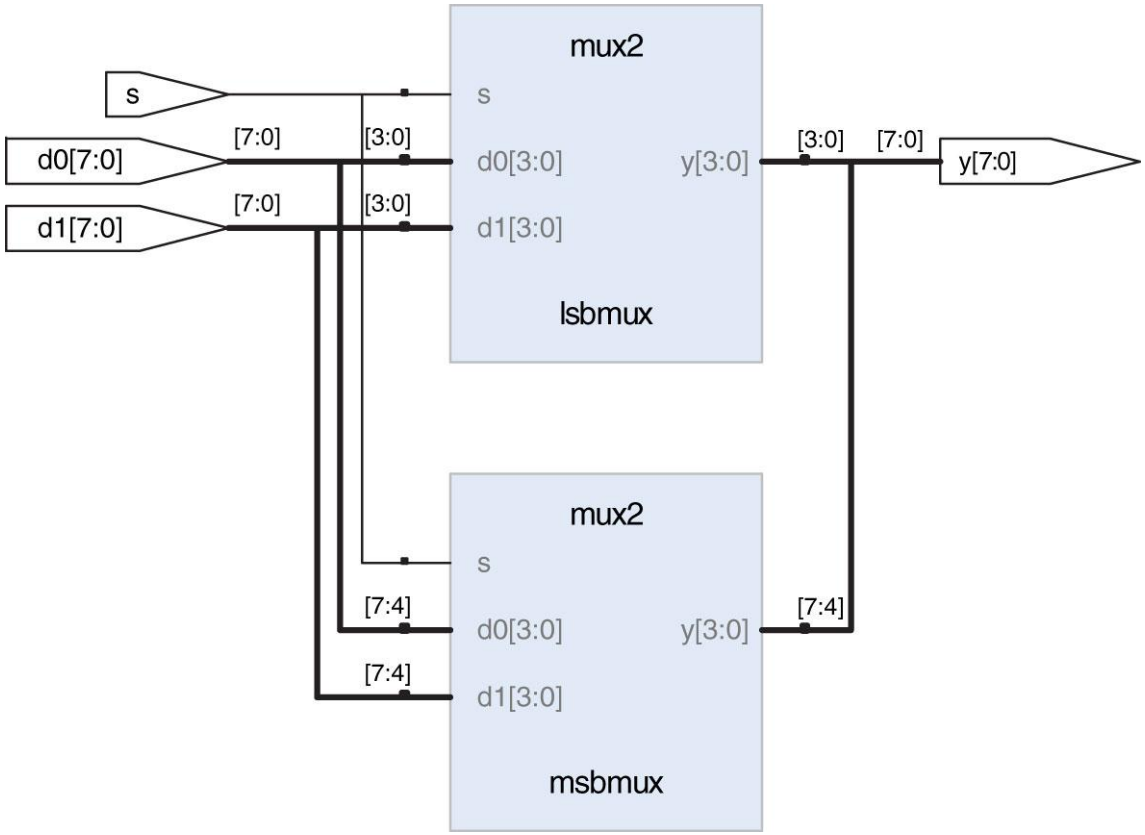

Figure 4.13 mux2_8 synthesized circuit

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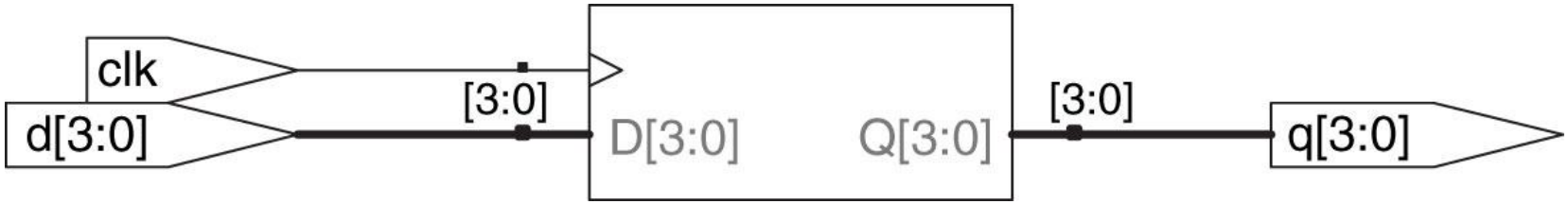

Figure 4.14 flop synthesized circuit

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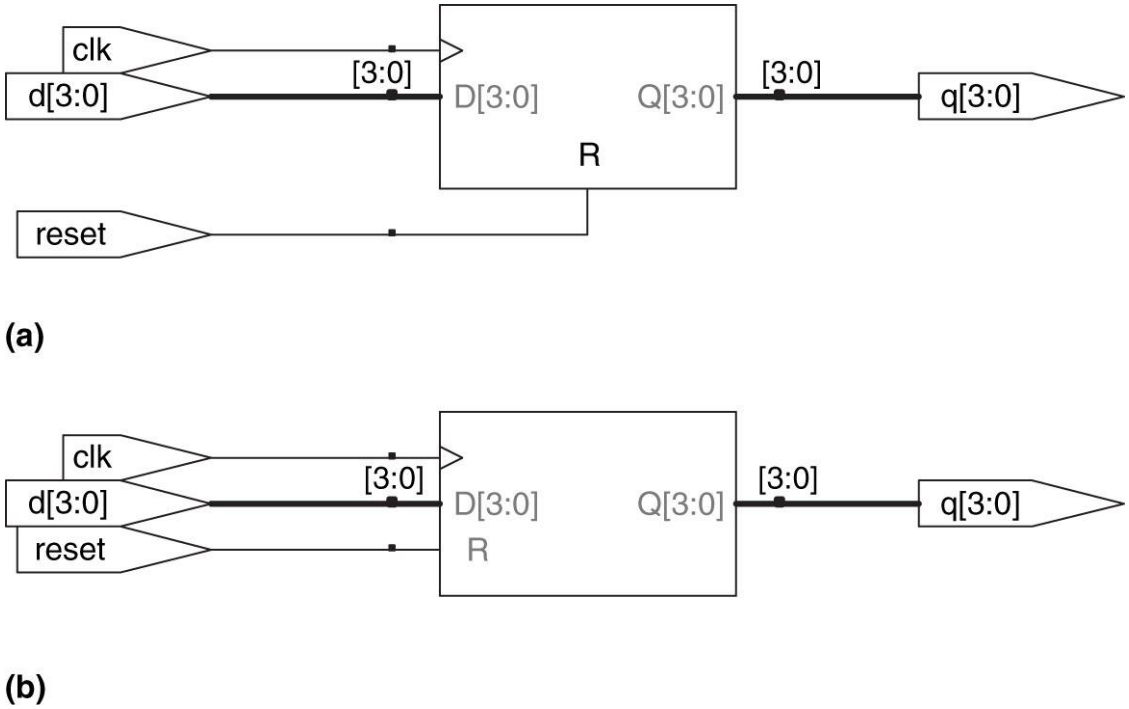

Figure 4.15 flopr synthesized circuit (a) asynchronous reset, (b) synchronous reset

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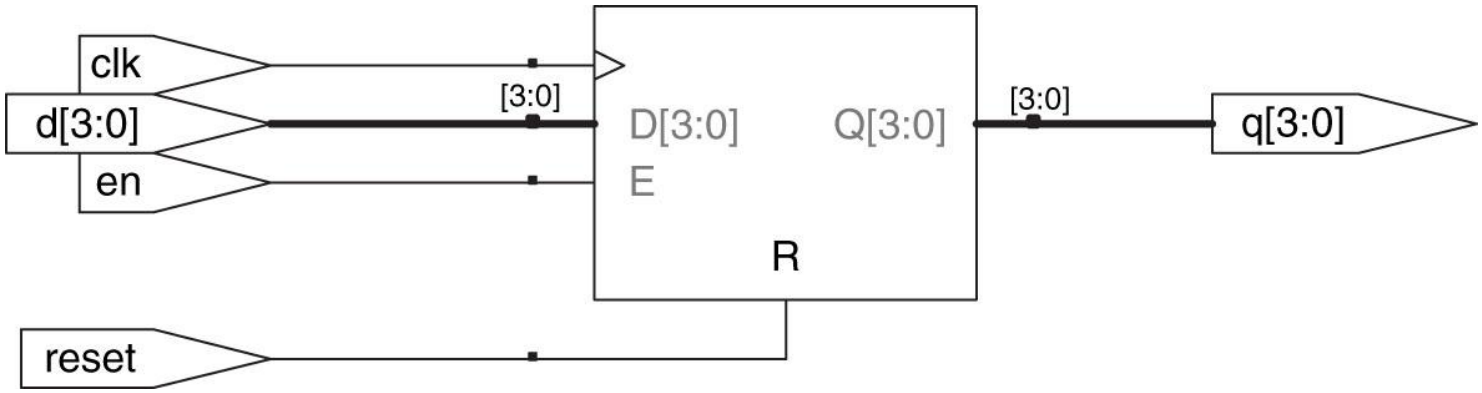

Figure 4.16 flopenr synthesized circuit

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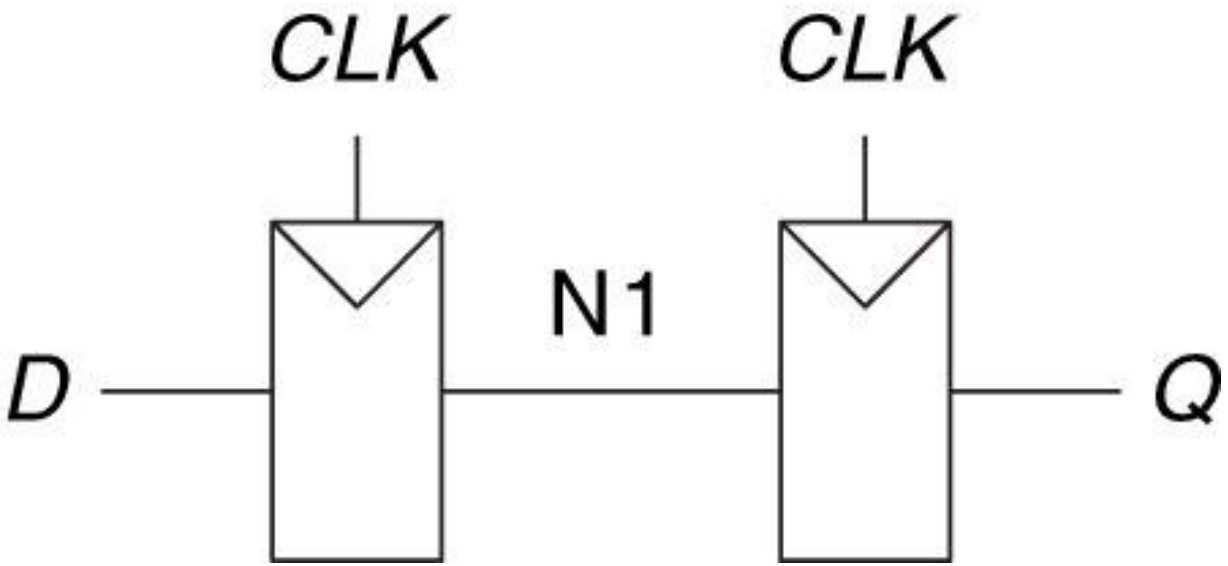

Figure 4.17 Synchronizer circuit

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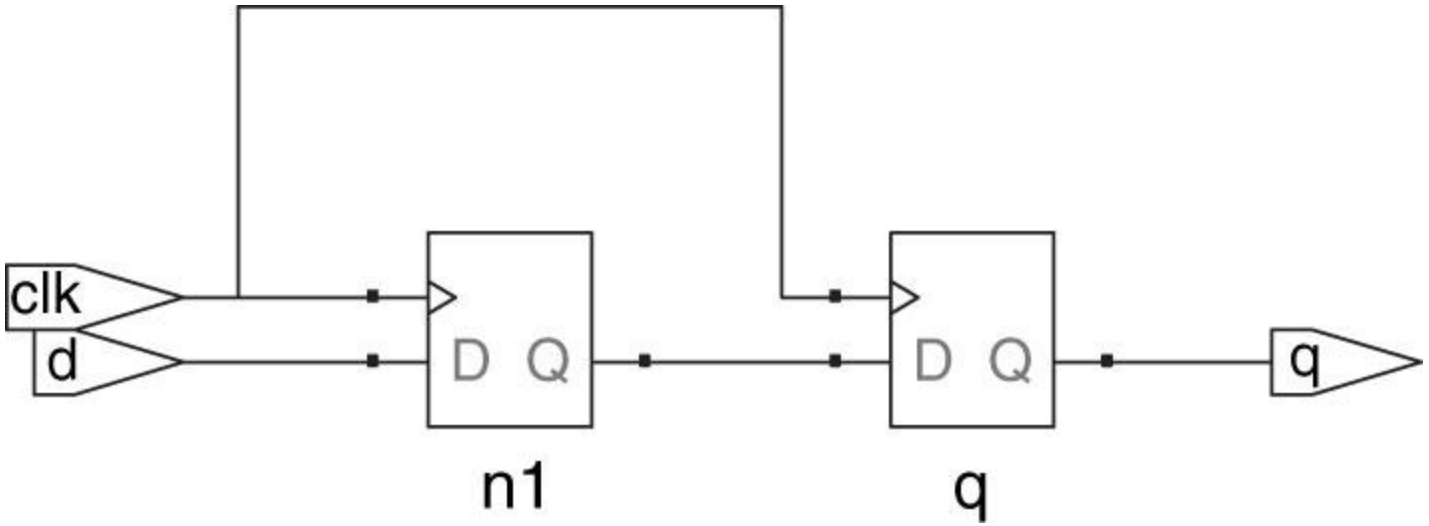

Figure 4.18 sync synthesized circuit

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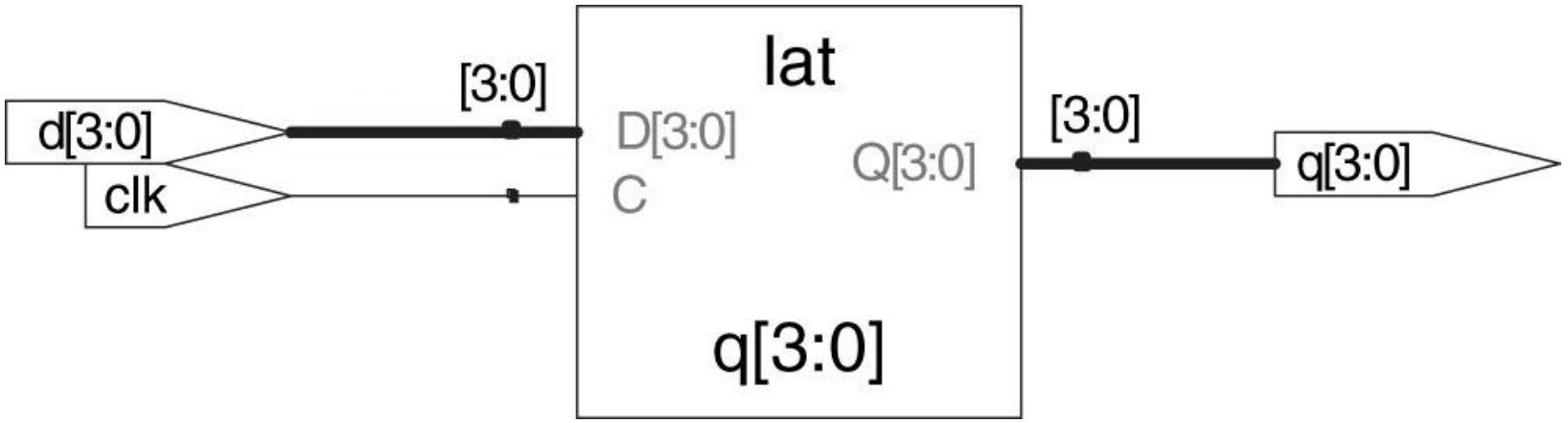

Figure 4.19 latch synthesized circuit

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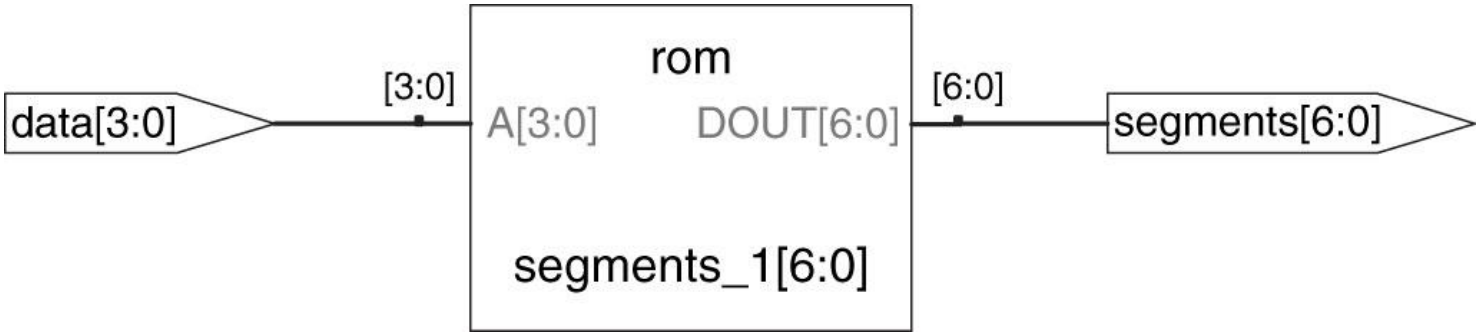

Figure 4.20 sevenseg synthesized circuit

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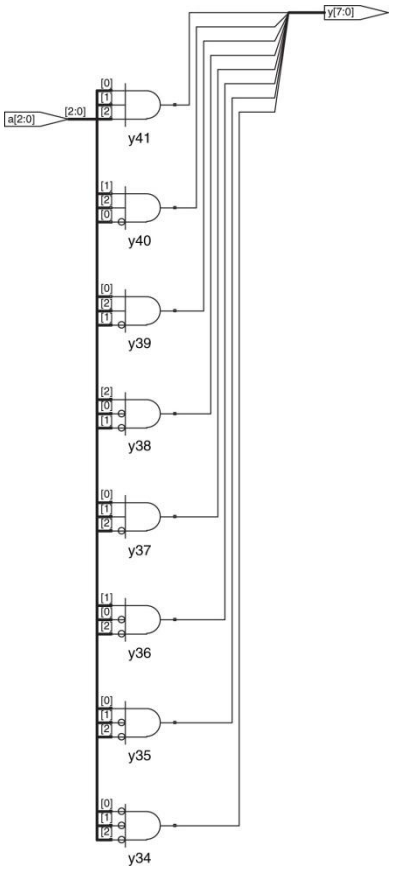

Figure 4.21 decoder3_8 synthesized circuit

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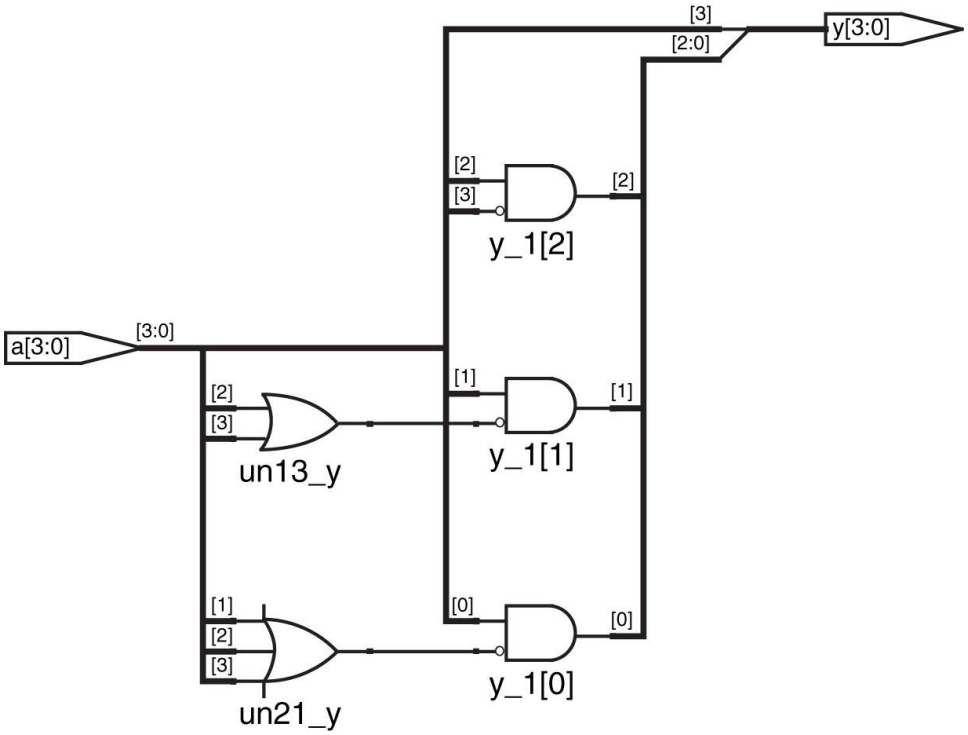

Figure 4.22 priorityckt synthesized circuit

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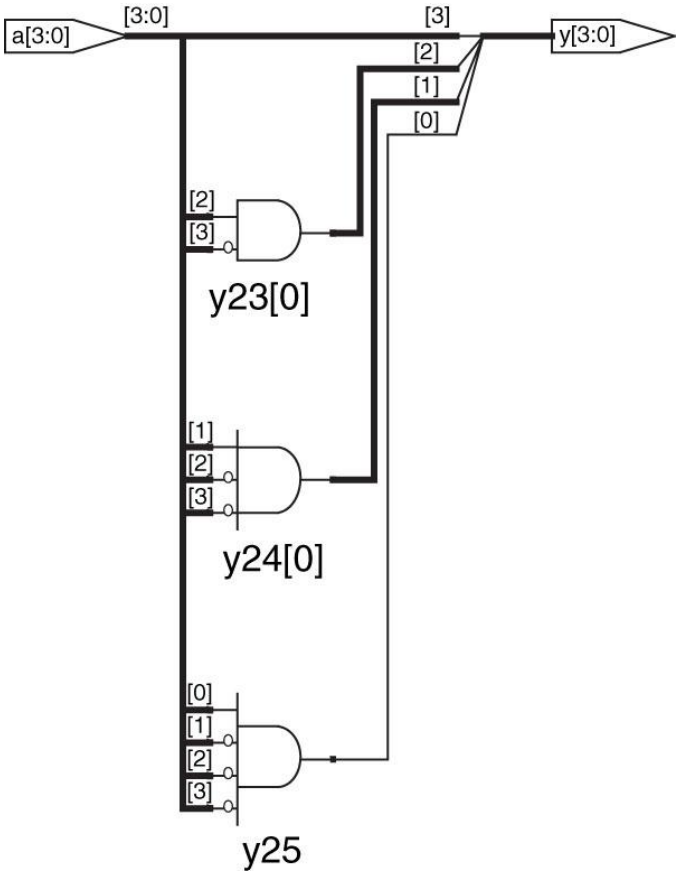

Figure 4.23 priority_casez synthesized circuit

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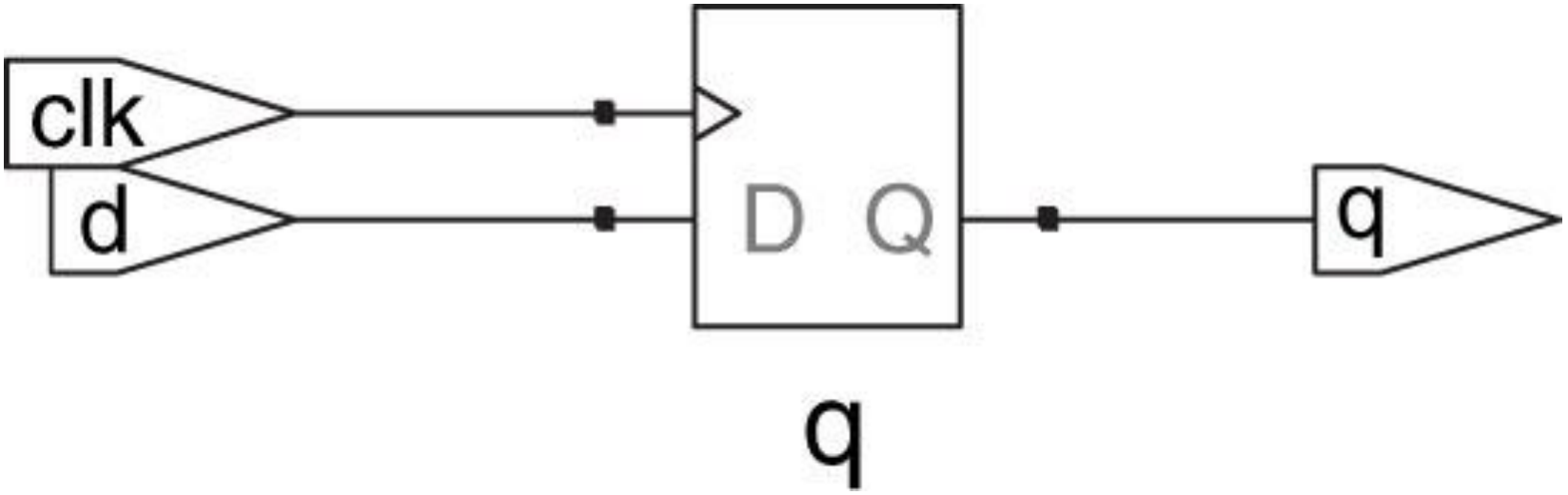

Figure 4.24 syncbad synthesized circuit

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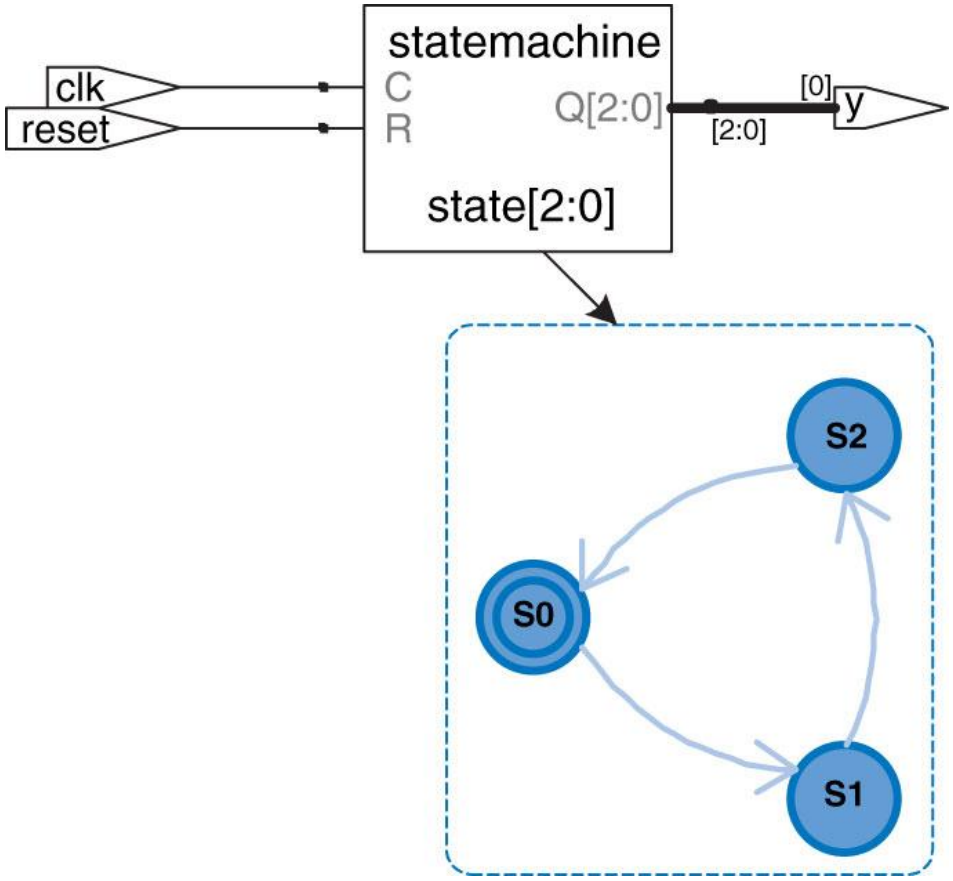

Figure 4.25 priority_casez synthesized circuit

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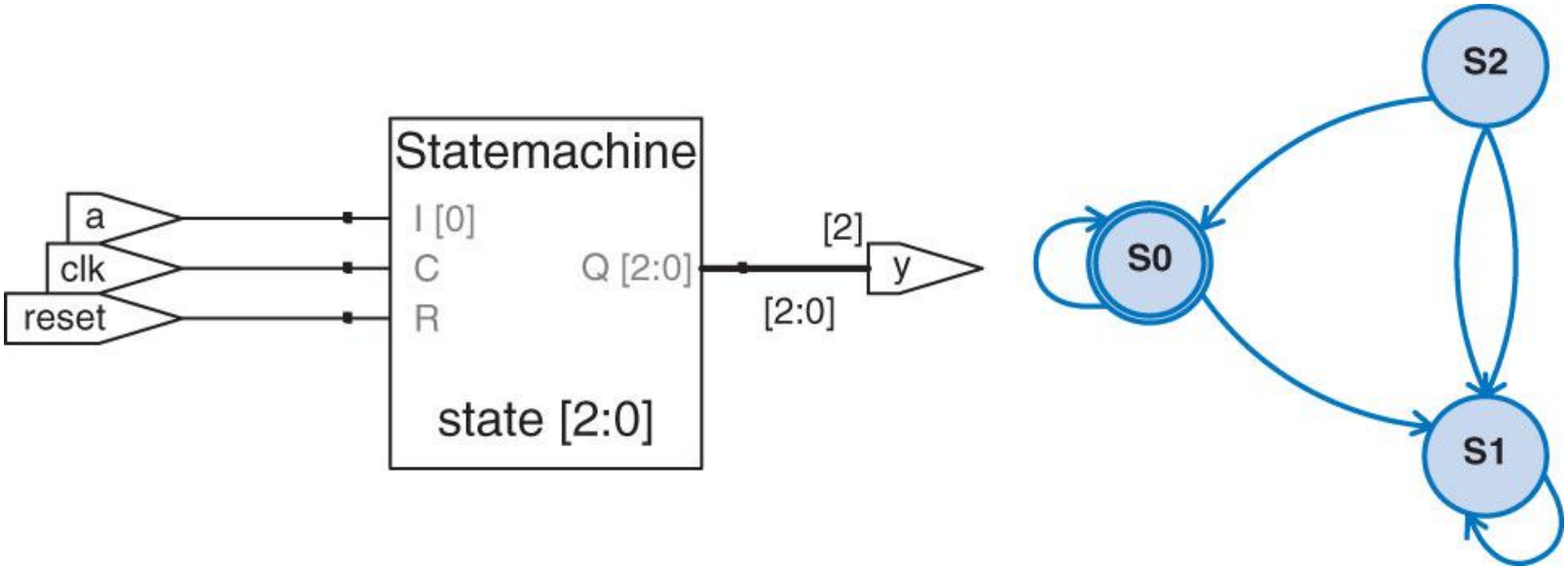

Figure 4.26 patternMoore synthesized circuit

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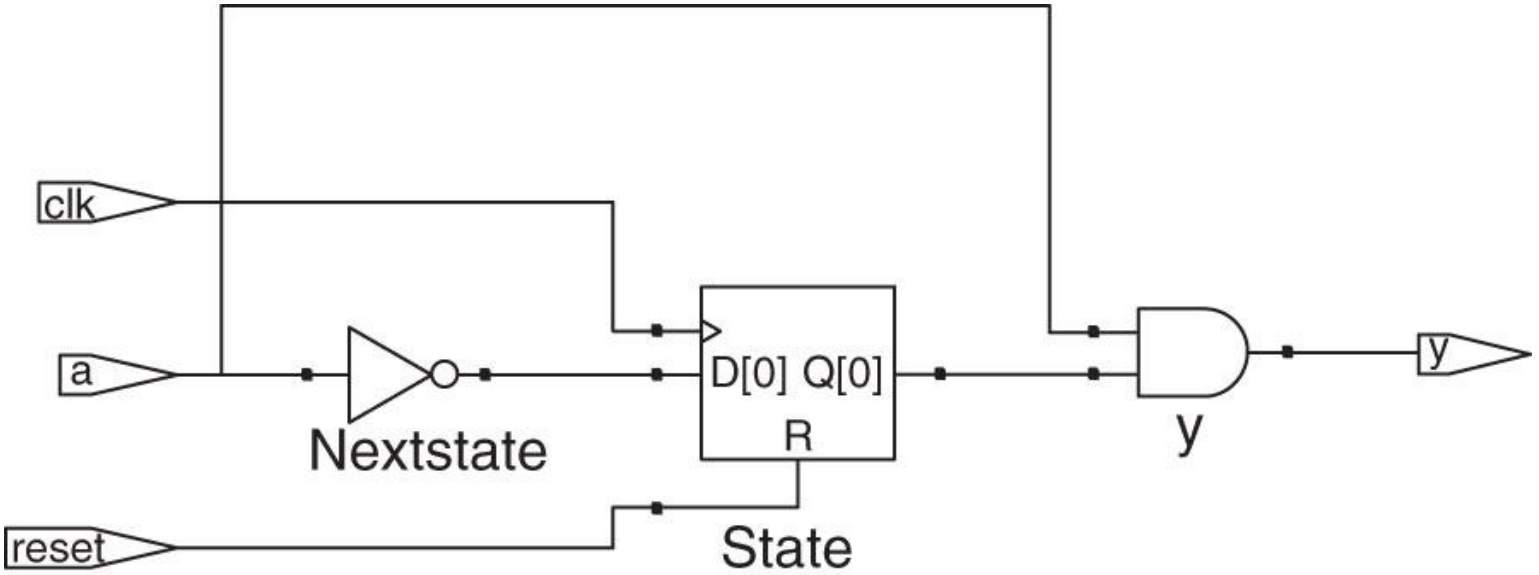

Figure 4.27 patternMealy synthesized circuit

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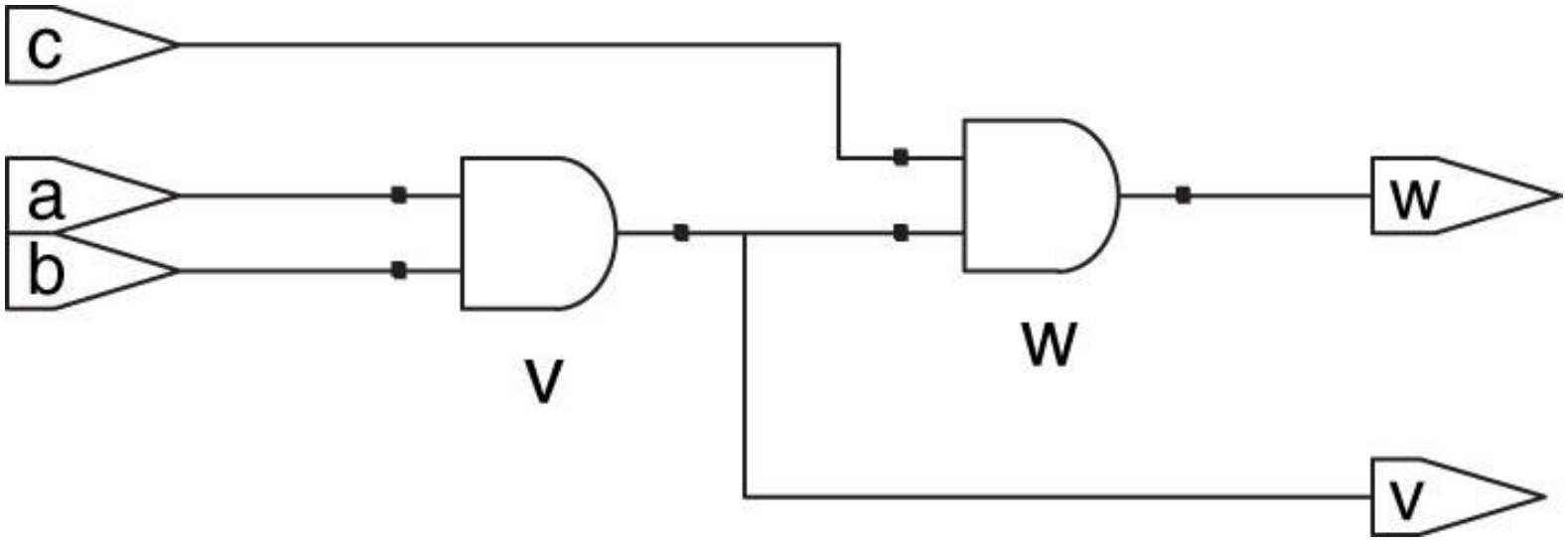

Figure 4.28 and23 synthesized circuit

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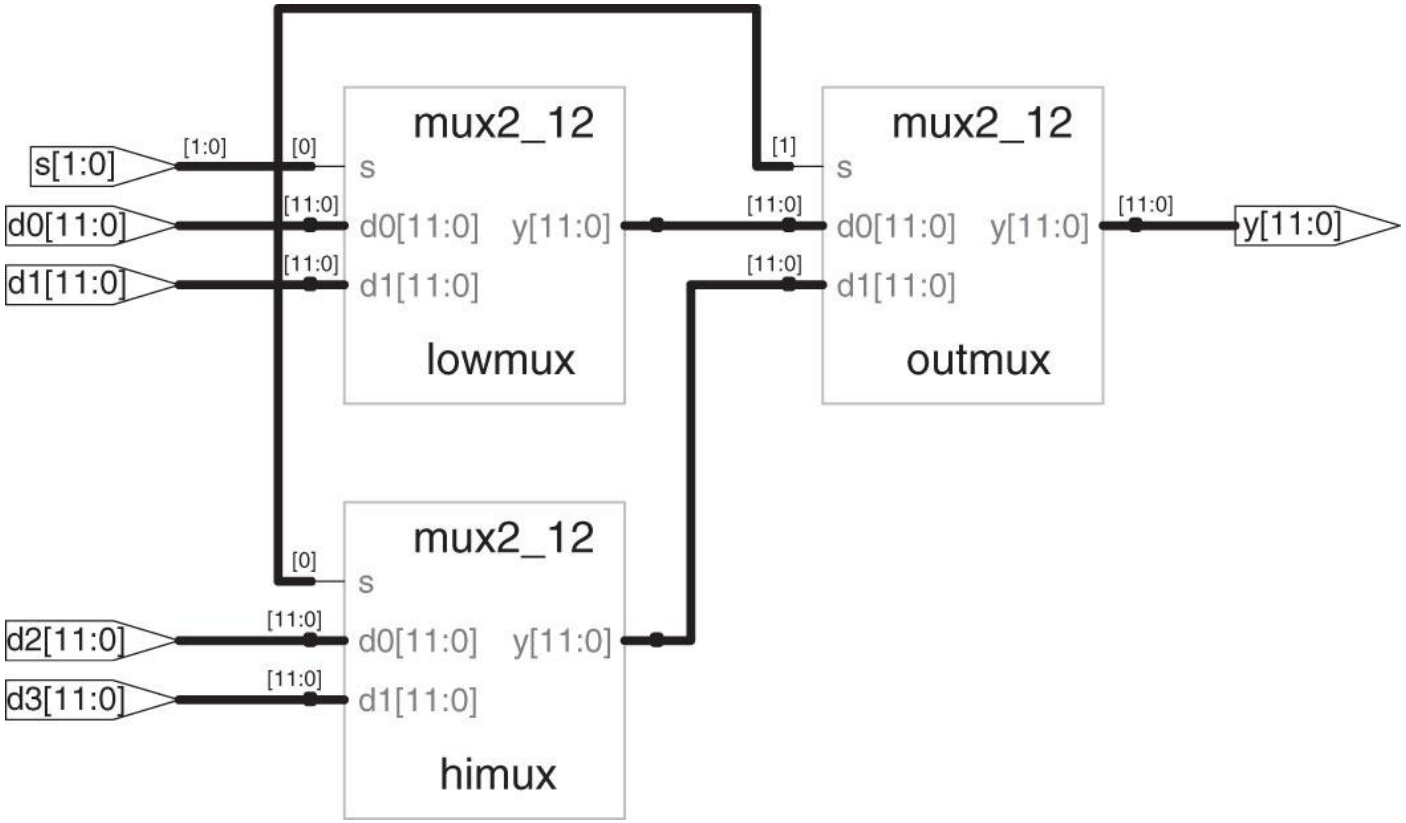

Figure 4.29 mux4_12 synthesized circuit

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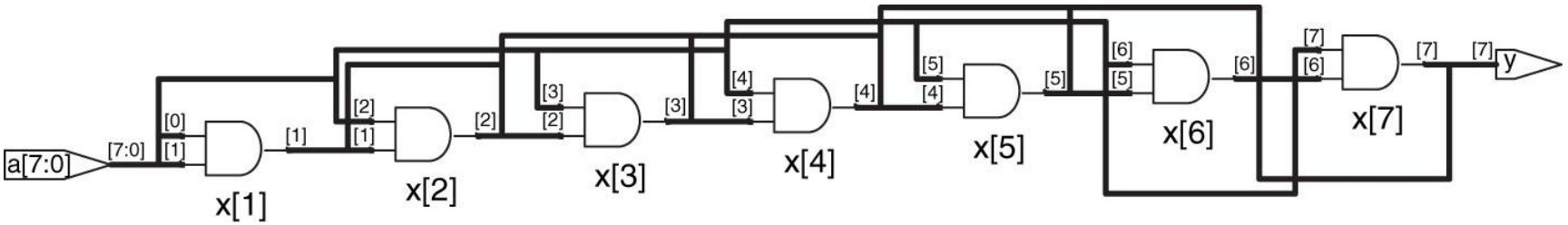

Figure 4.30 andN synthesized circuit

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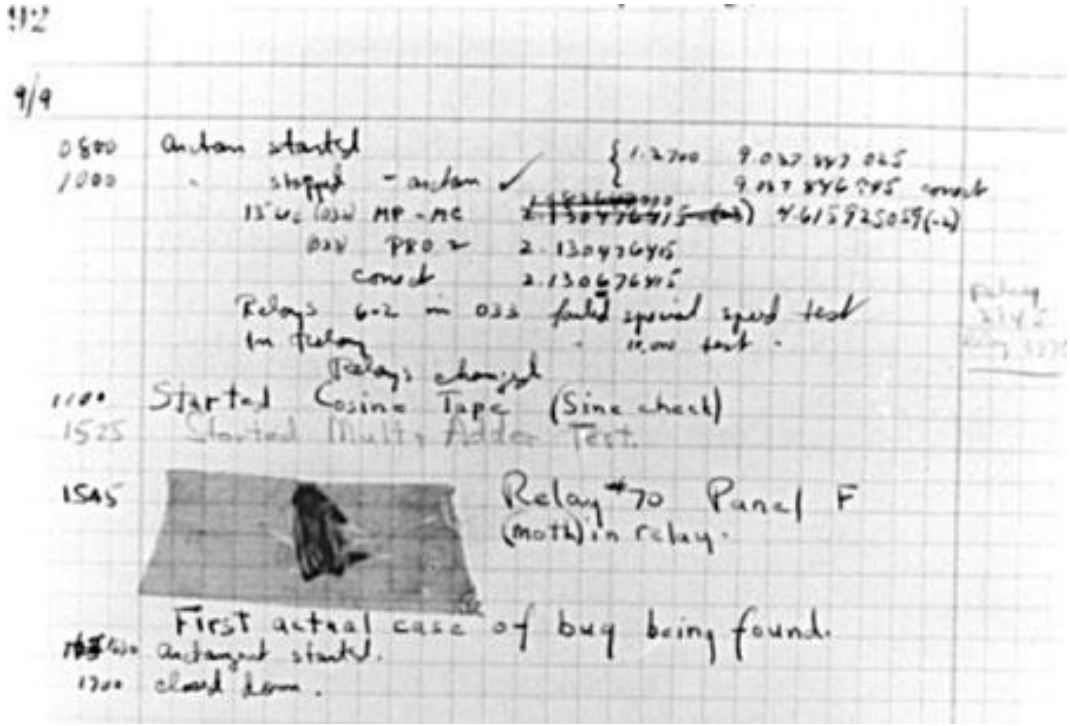

Figure M 01

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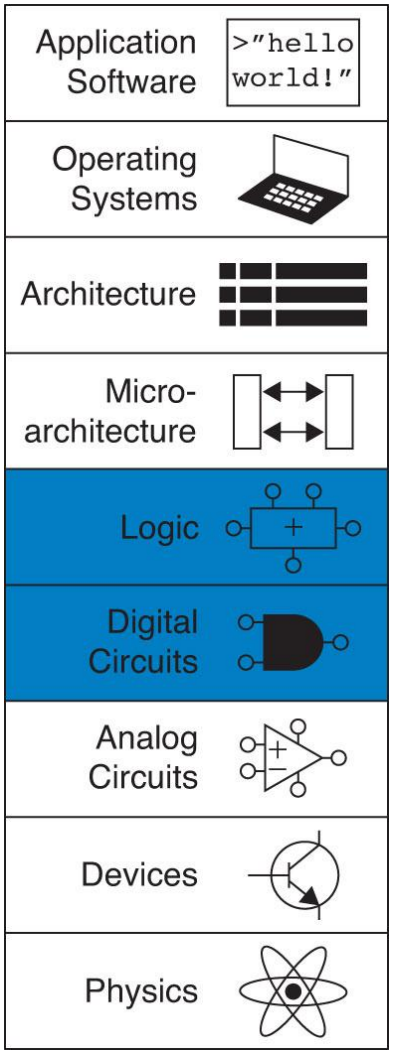

UNN Figure 1

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