

Chapter 4

Hardware Description Languages

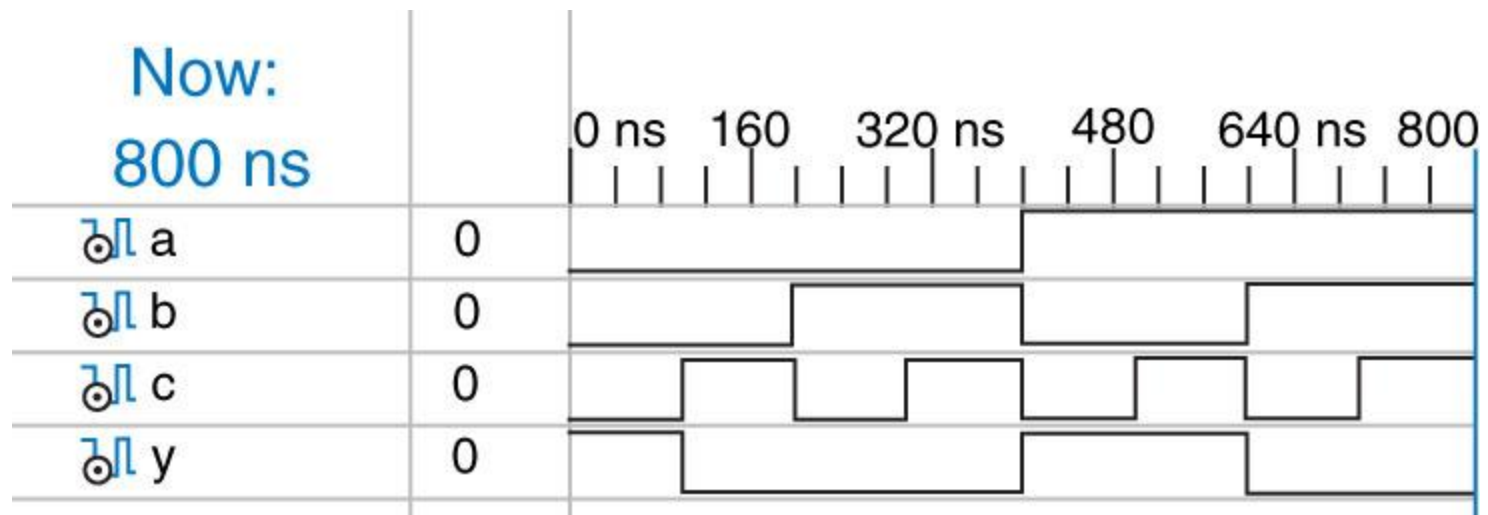


Figure 4.1 Simulation waveforms

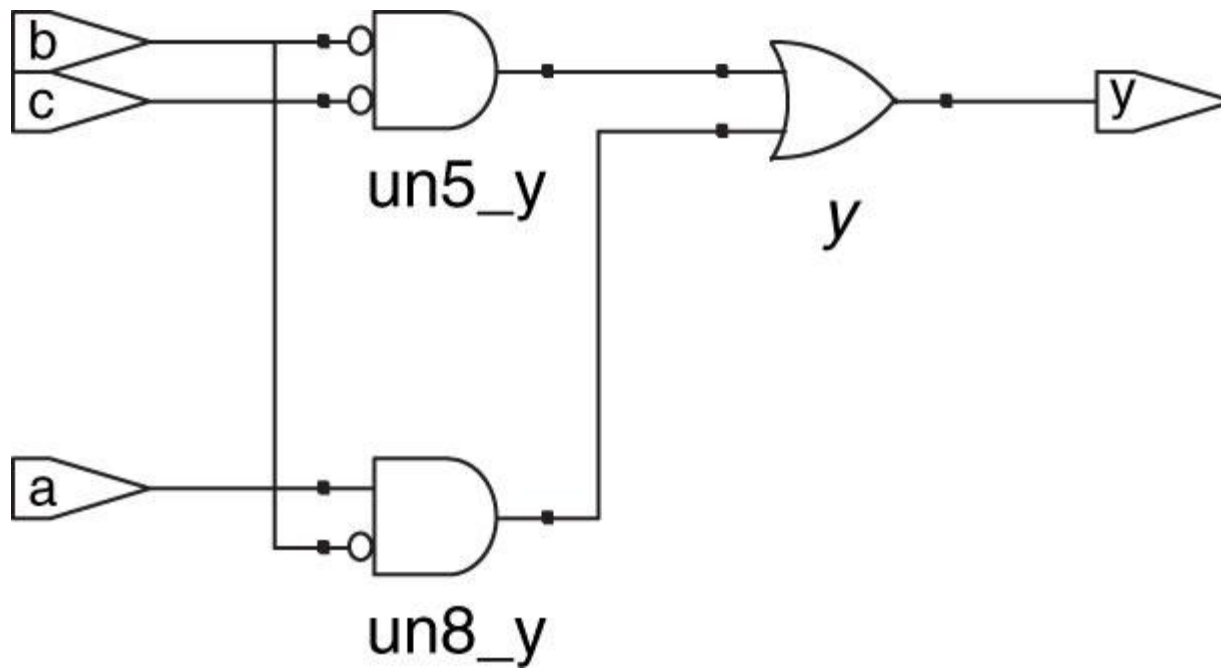


Figure 4.2 Synthesized circuit

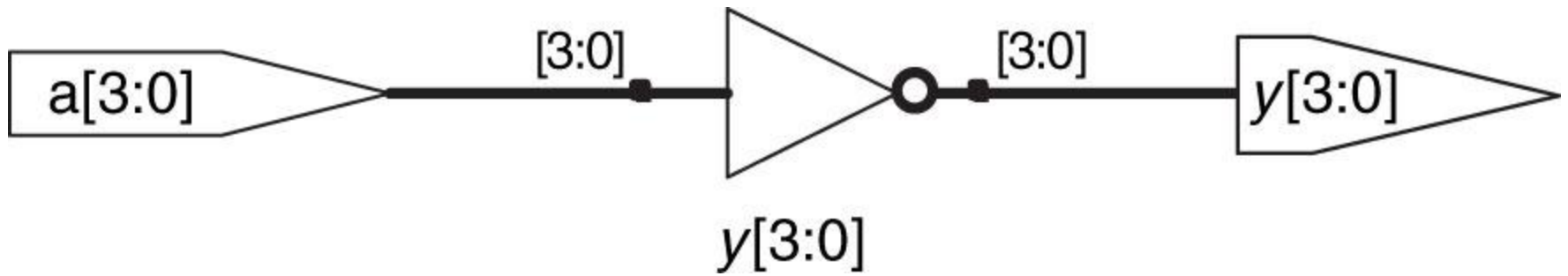


Figure 4.3 inv synthesized circuit

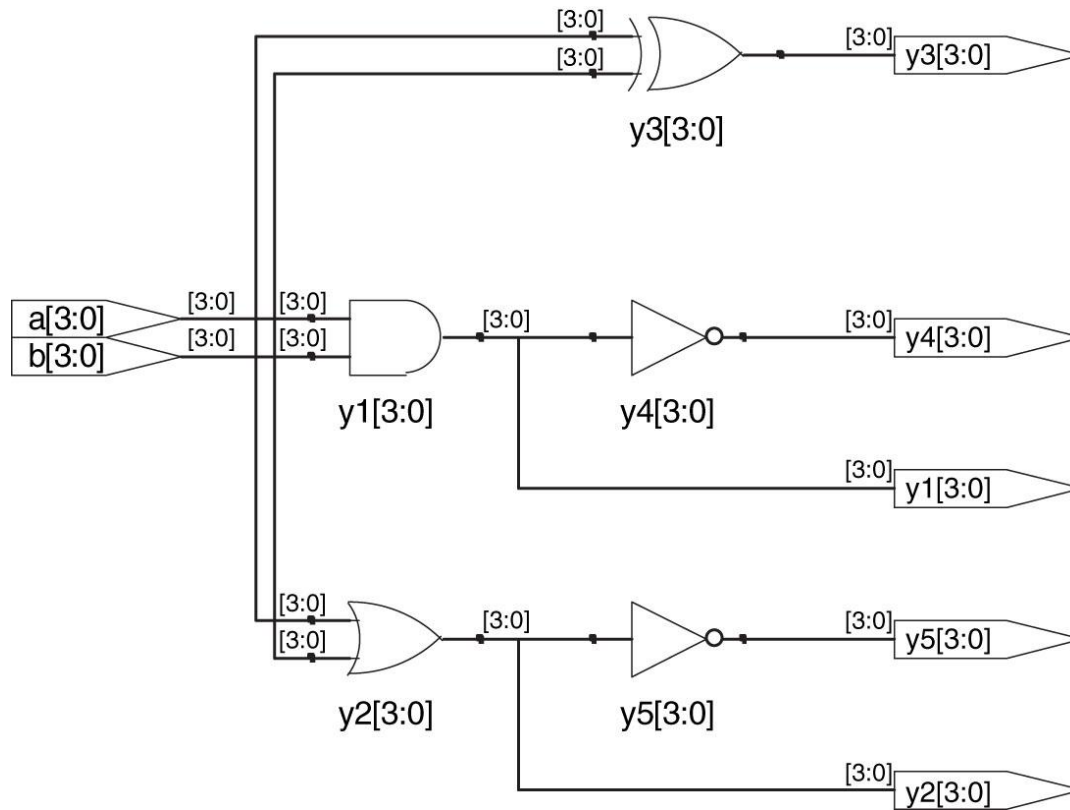


Figure 4.4 gates synthesized circuit

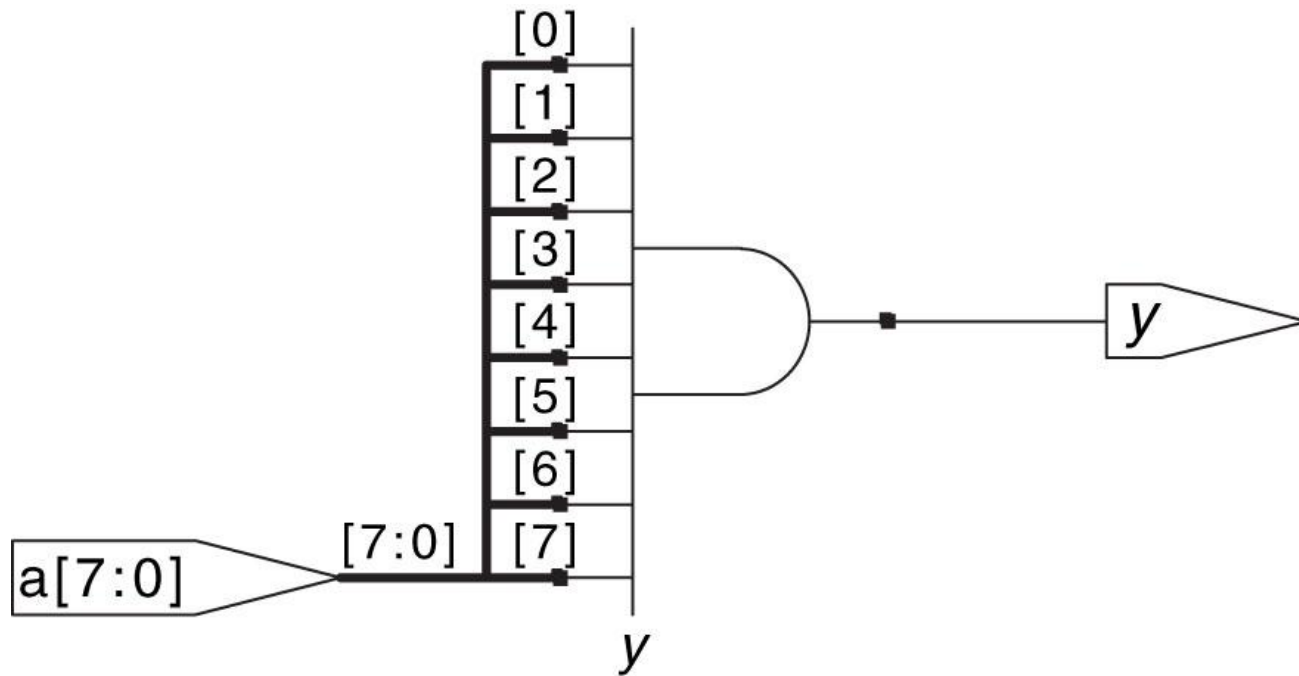


Figure 4.5 and8 synthesized circuit

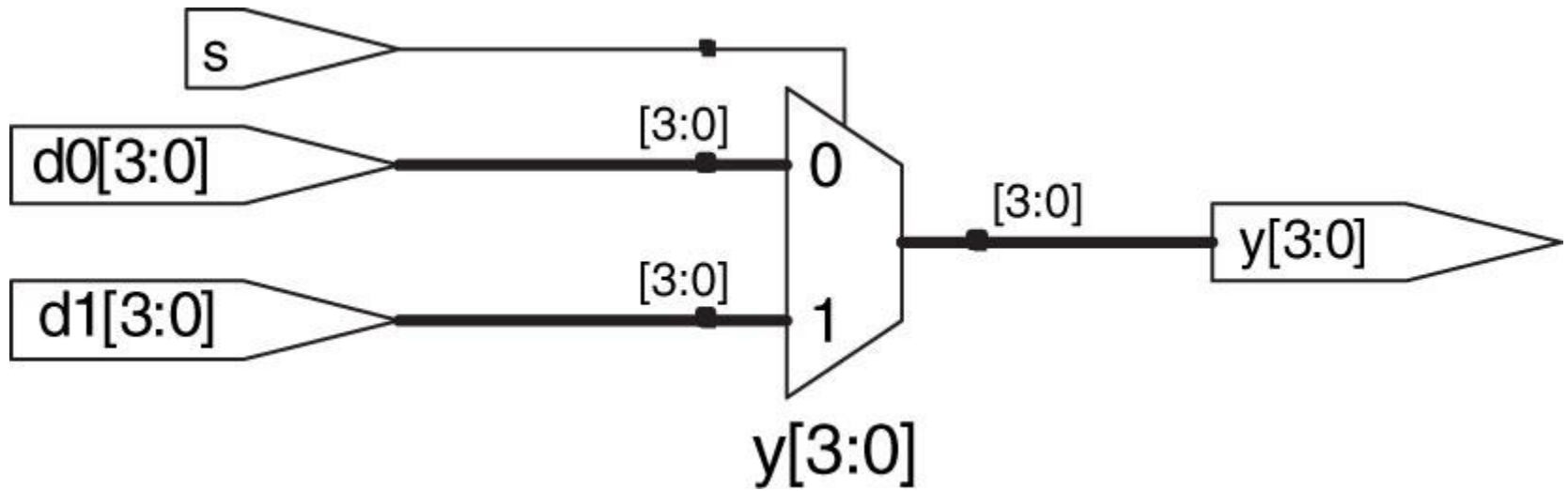


Figure 4.6 mux2 synthesized circuit

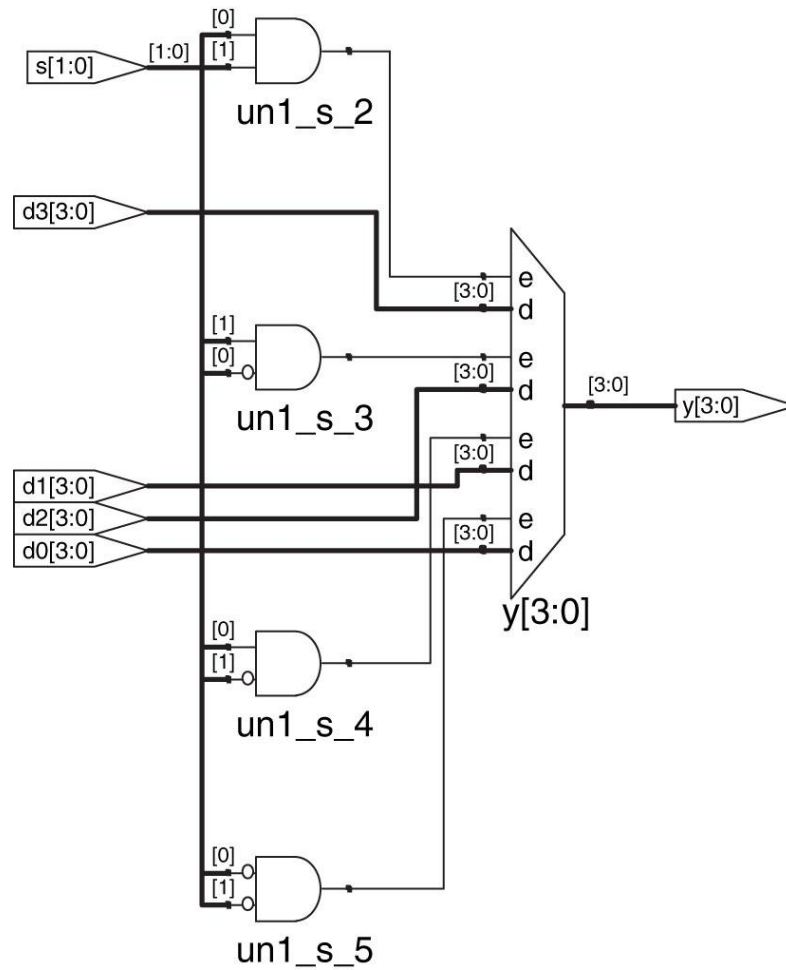


Figure 4.7 mux4 synthesized circuit

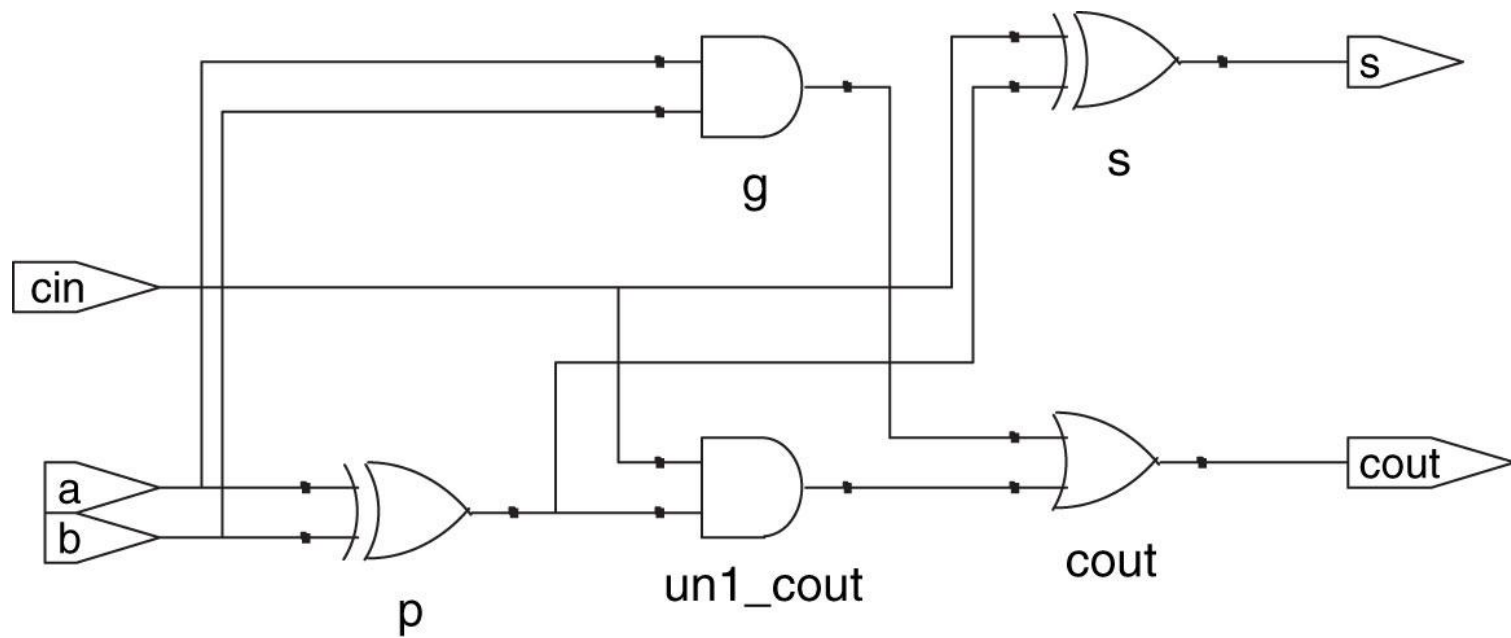


Figure 4.8 fulladder synthesized circuit

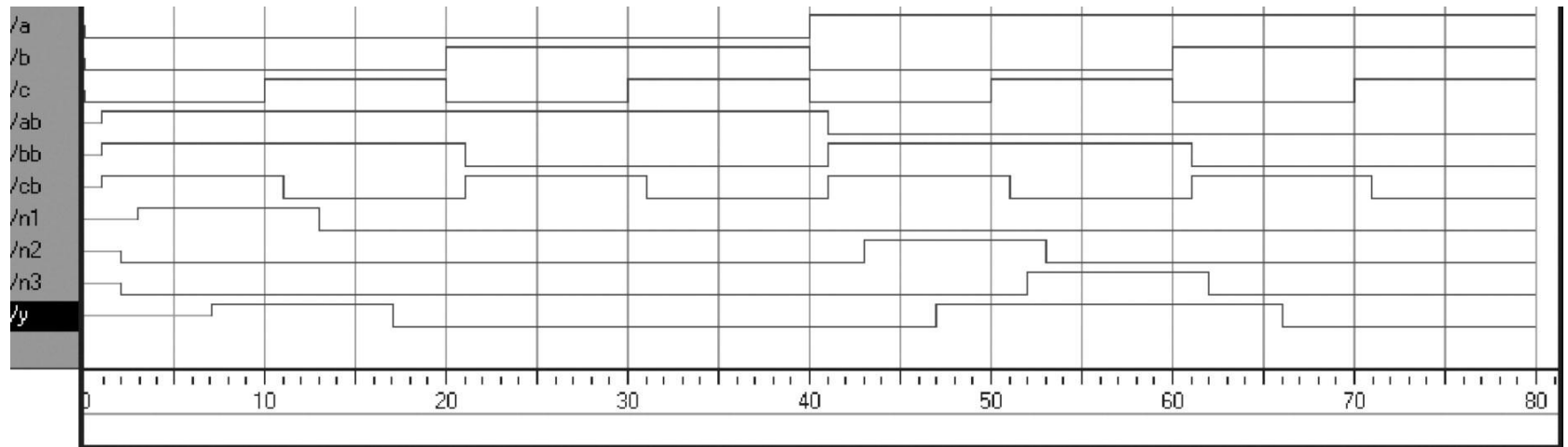


Figure 4.10 Example simulation waveforms with delays (from the ModelSim simulator)

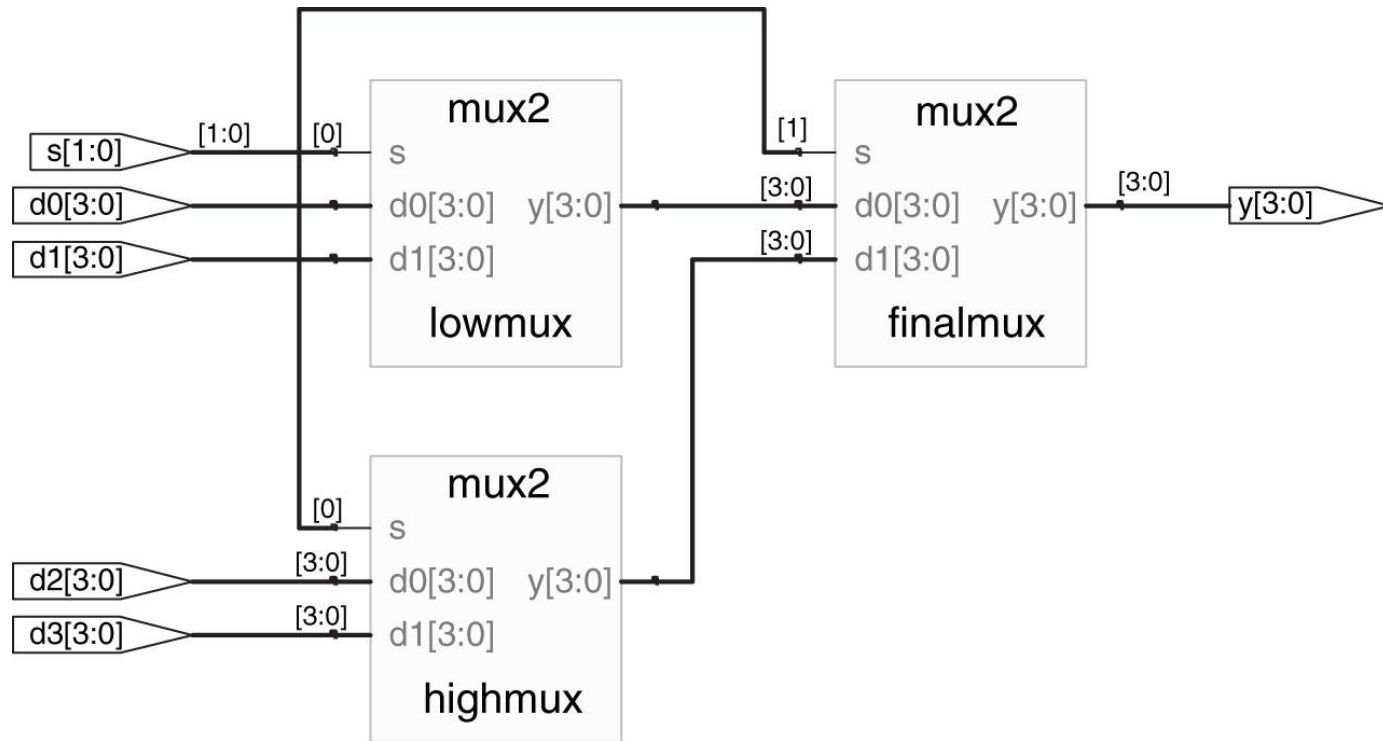


Figure 4.11 mux4 synthesized circuit

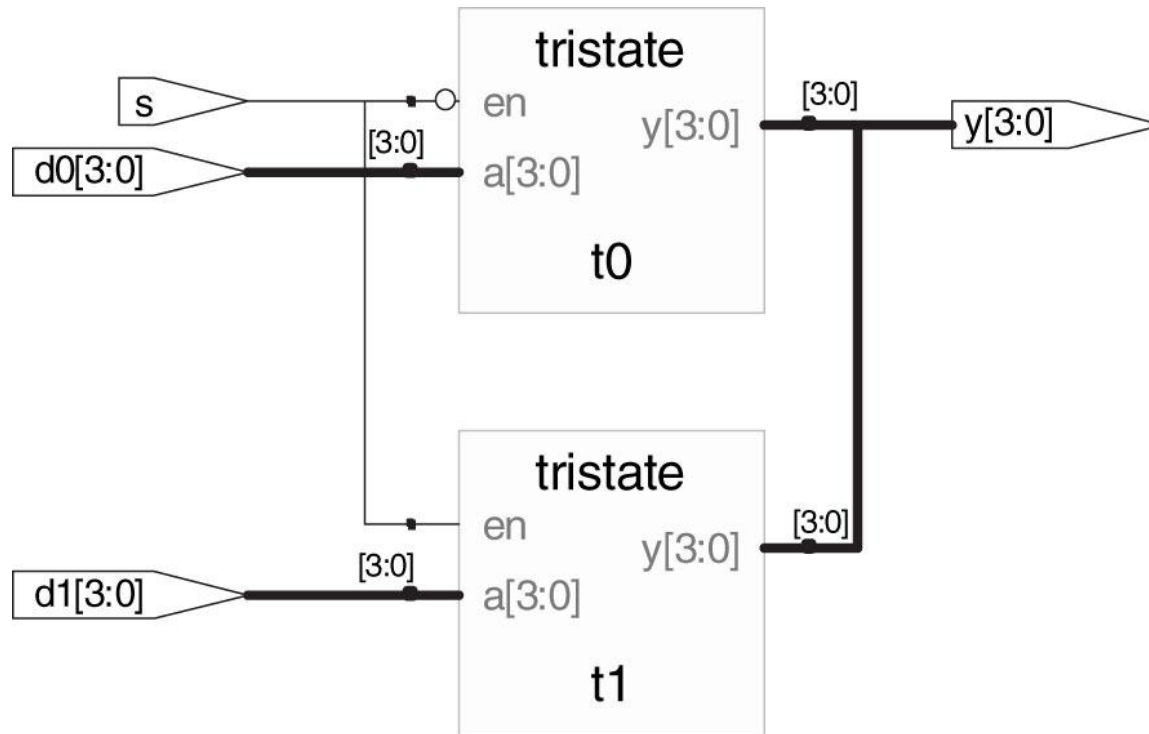


Figure 4.12 mux2 synthesized circuit

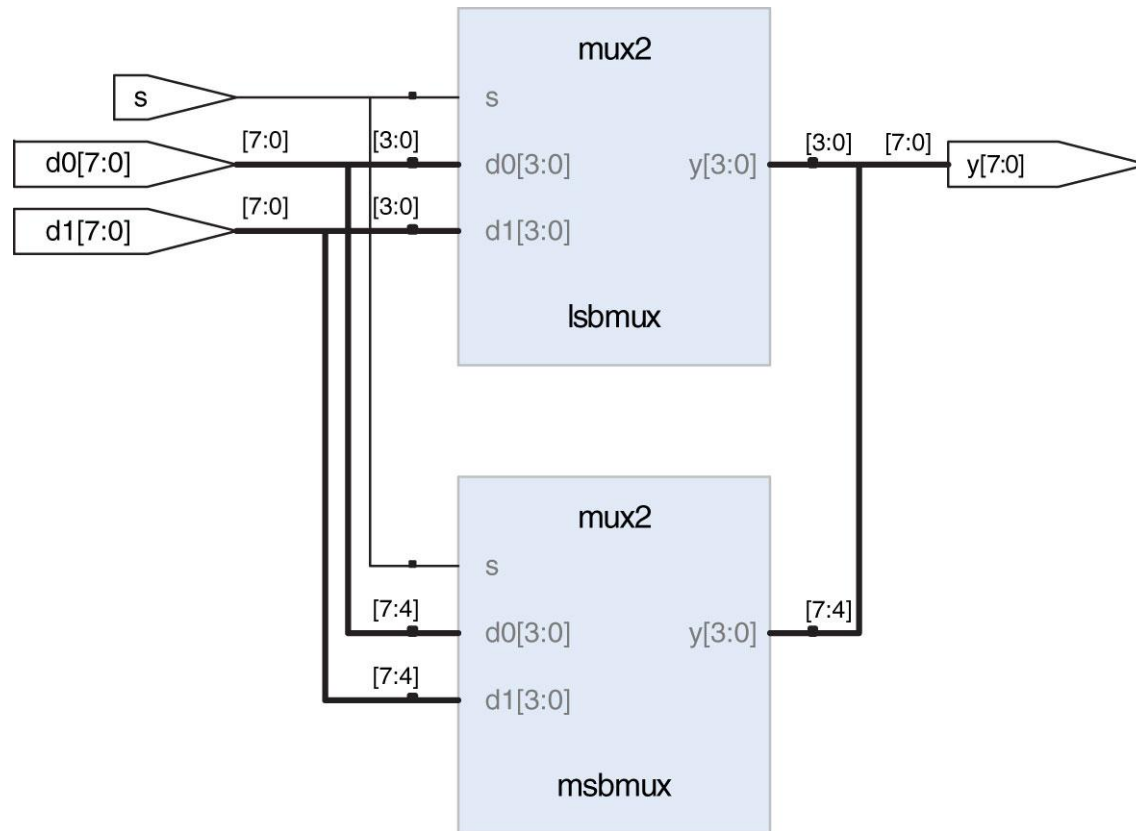


Figure 4.13 `mux2_8` synthesized circuit

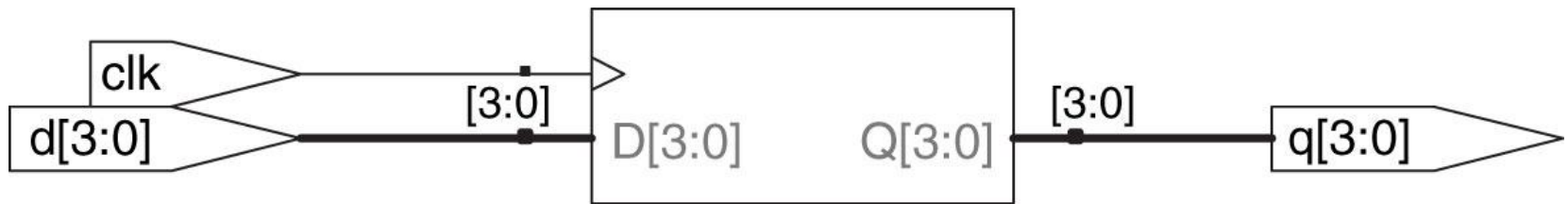
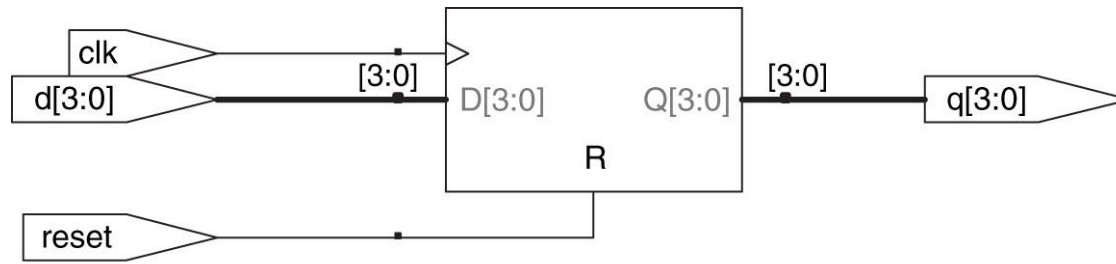
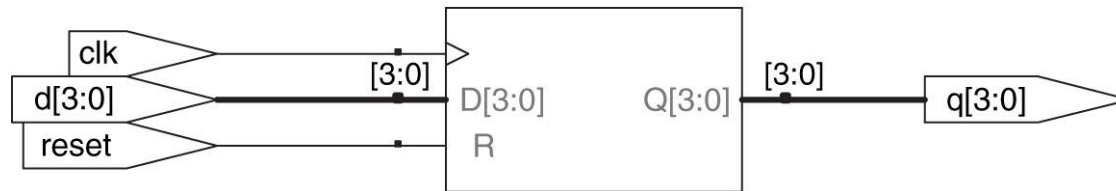


Figure 4.14 flop synthesized circuit



(a)



(b)

Figure 4.15 flopr synthesized circuit (a) asynchronous reset, (b) synchronous reset

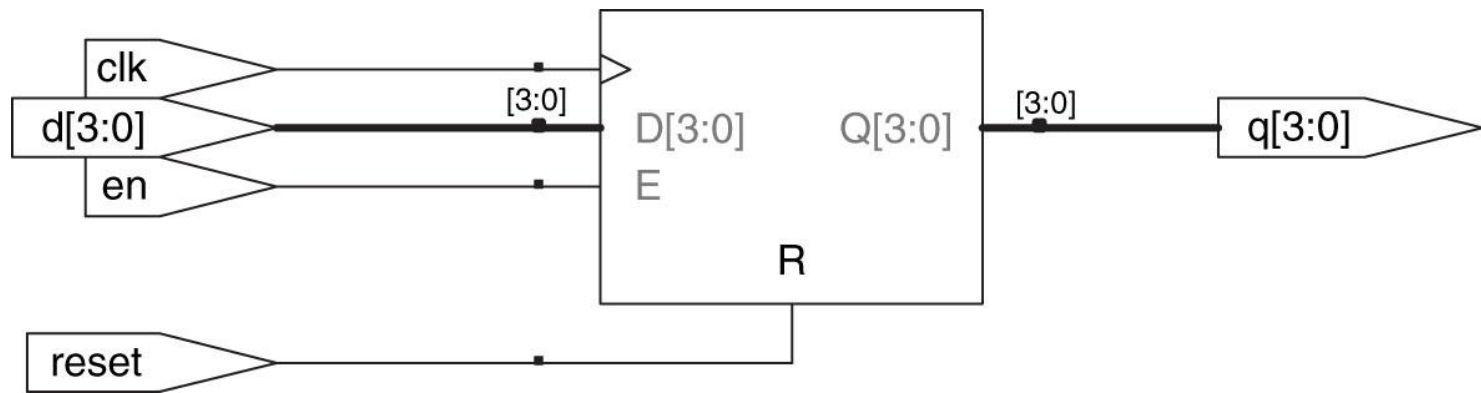


Figure 4.16 flopenr synthesized circuit

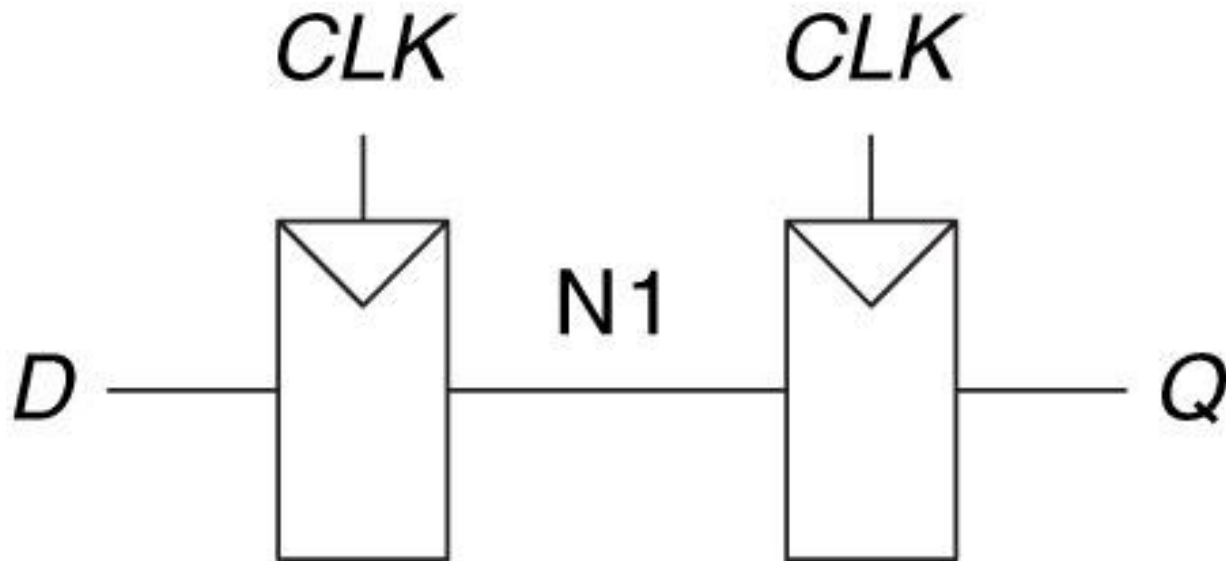


Figure 4.17 Synchronizer circuit

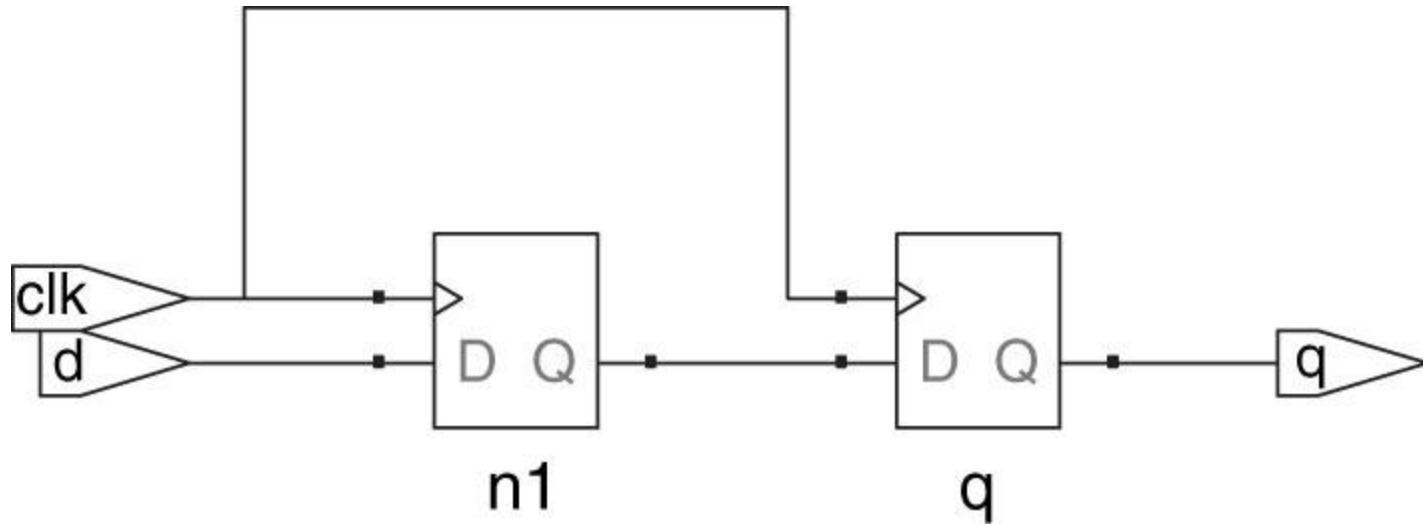


Figure 4.18 sync synthesized circuit

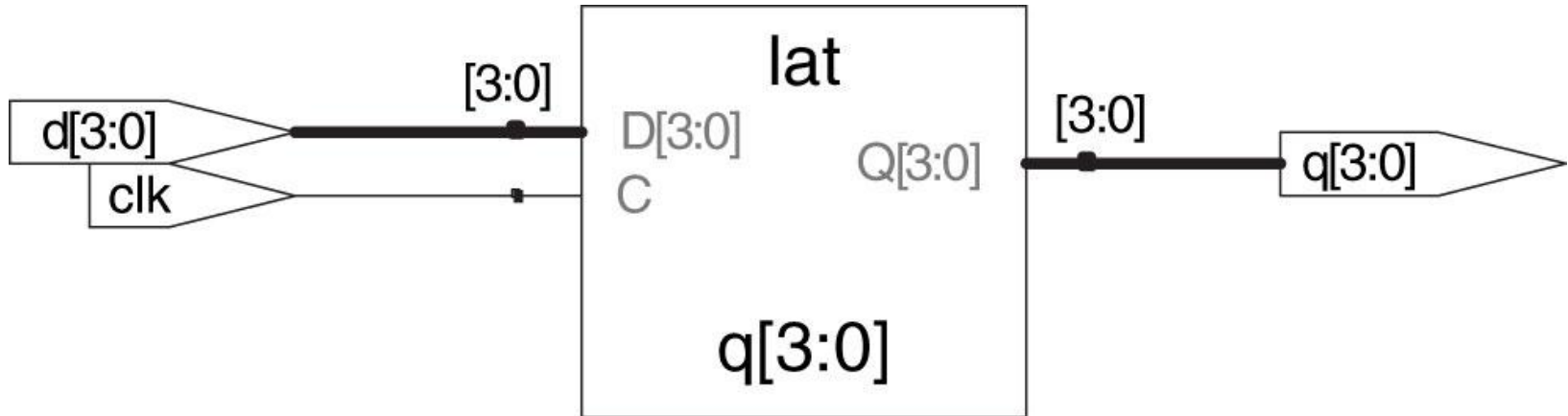


Figure 4.19 latch synthesized circuit



Figure 4.20 sevenseg synthesized circuit

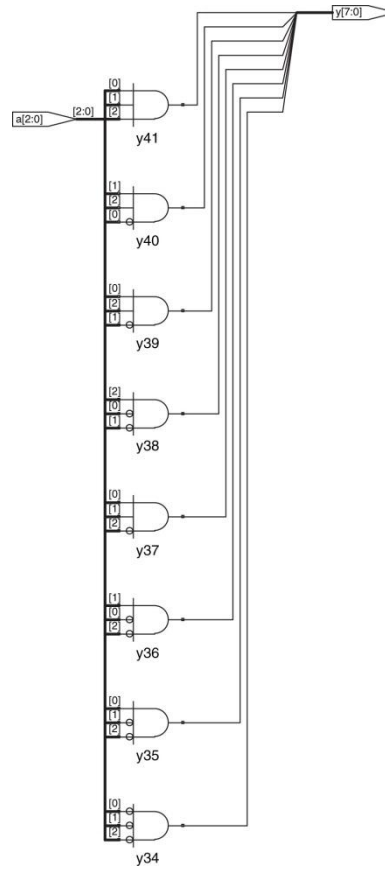


Figure 4.21 decoder3_8 synthesized circuit

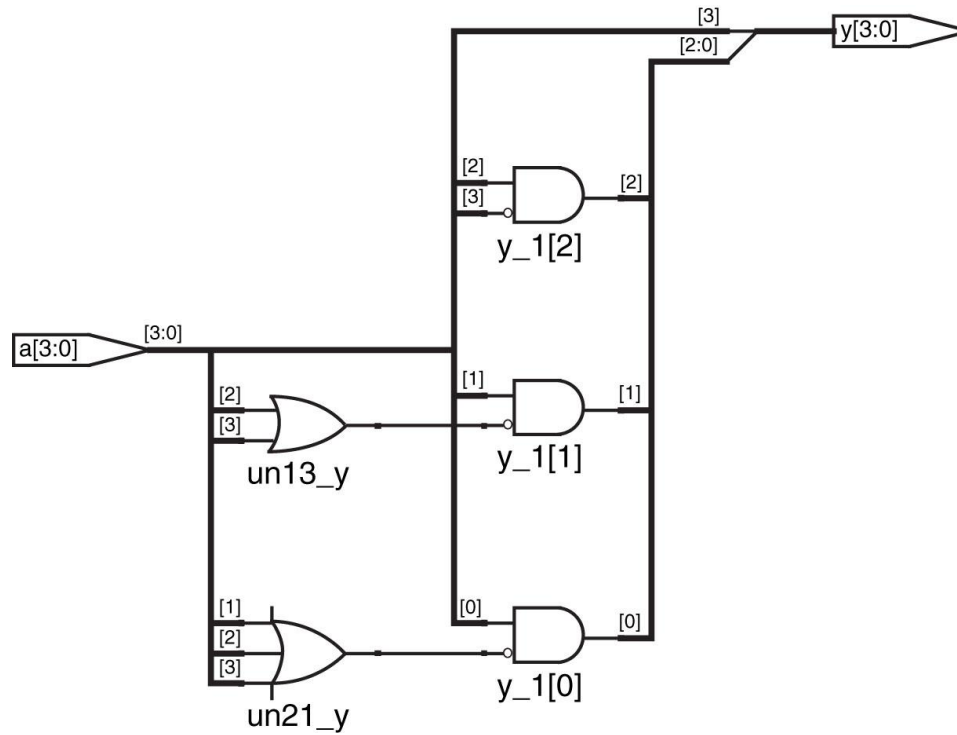


Figure 4.22 priorityckt synthesized circuit

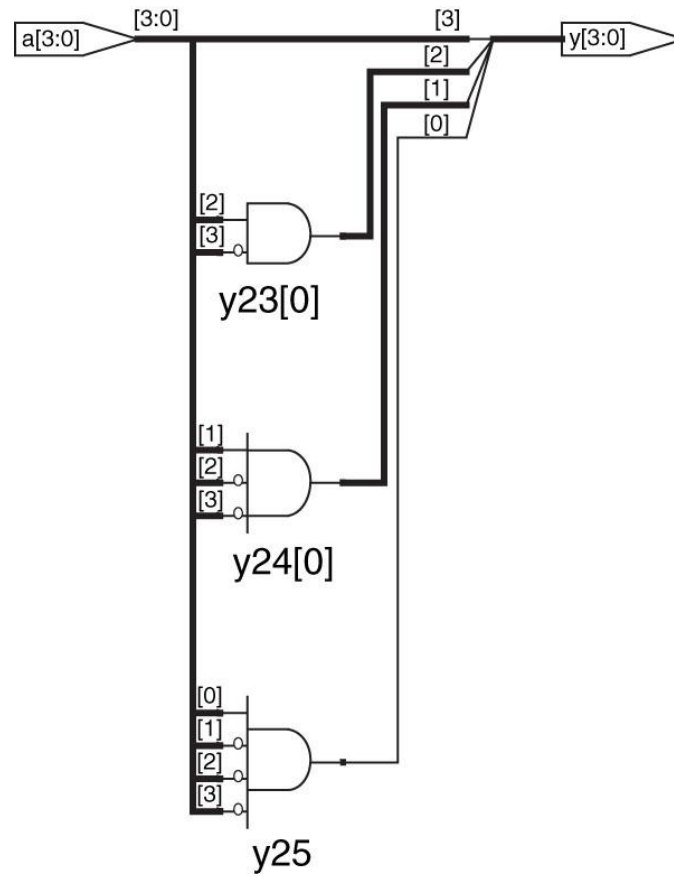


Figure 4.23 `priority_casez` synthesized circuit

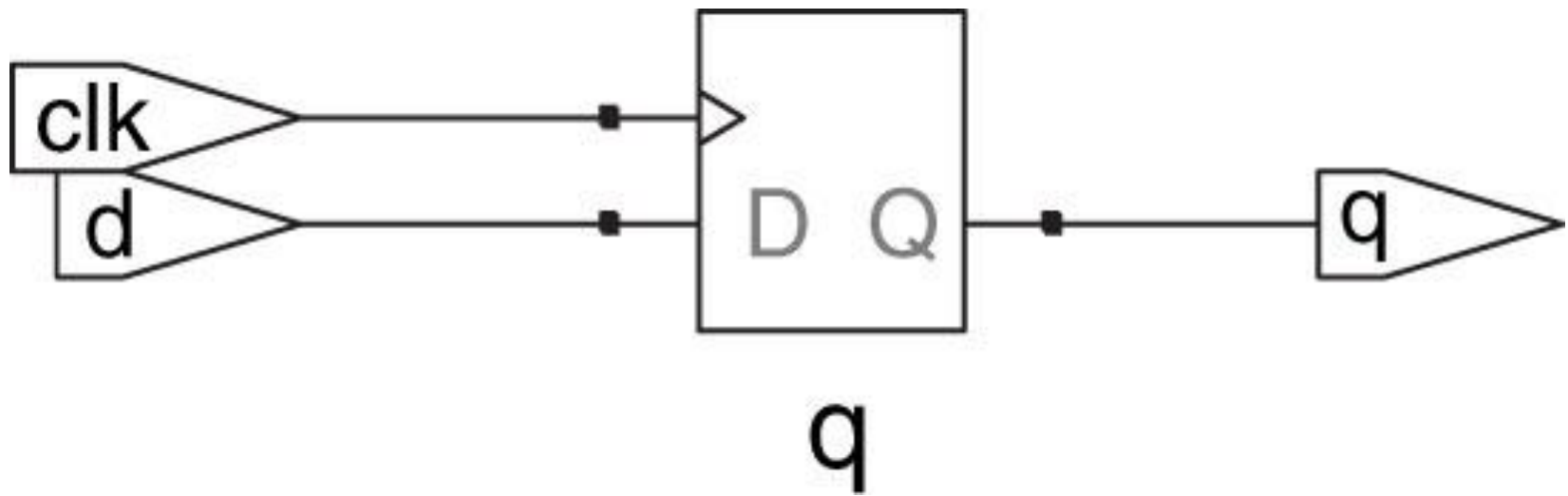


Figure 4.24 syncbad synthesized circuit

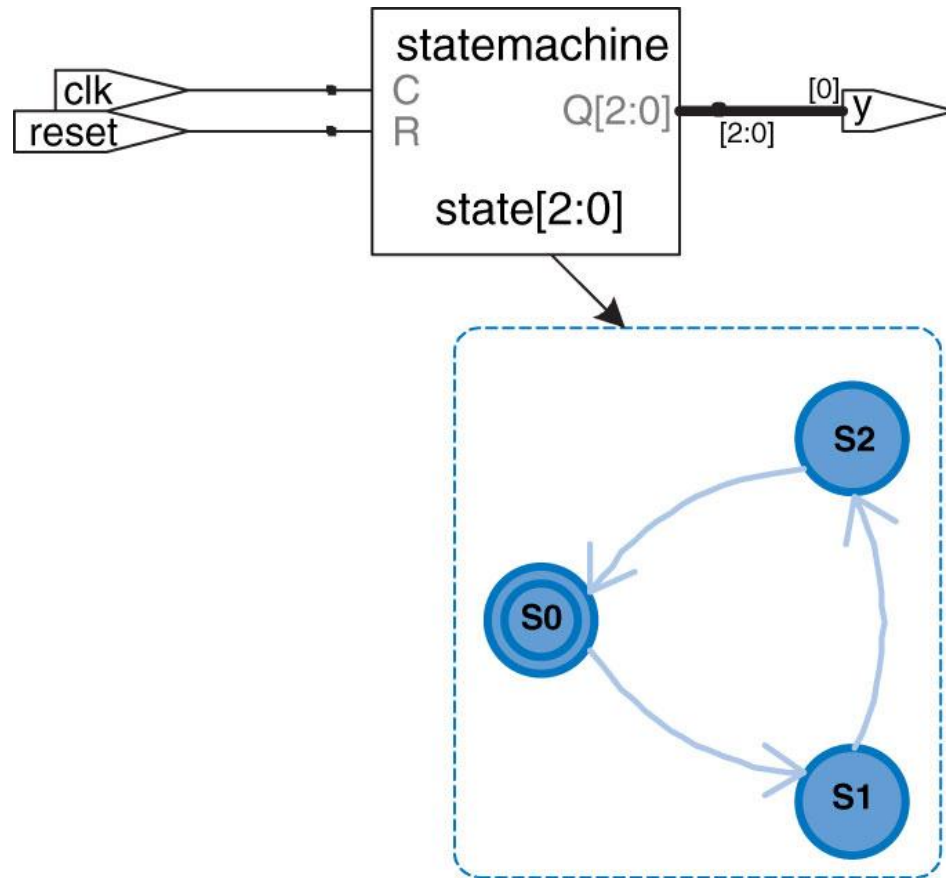


Figure 4.25 priority_casez synthesized circuit

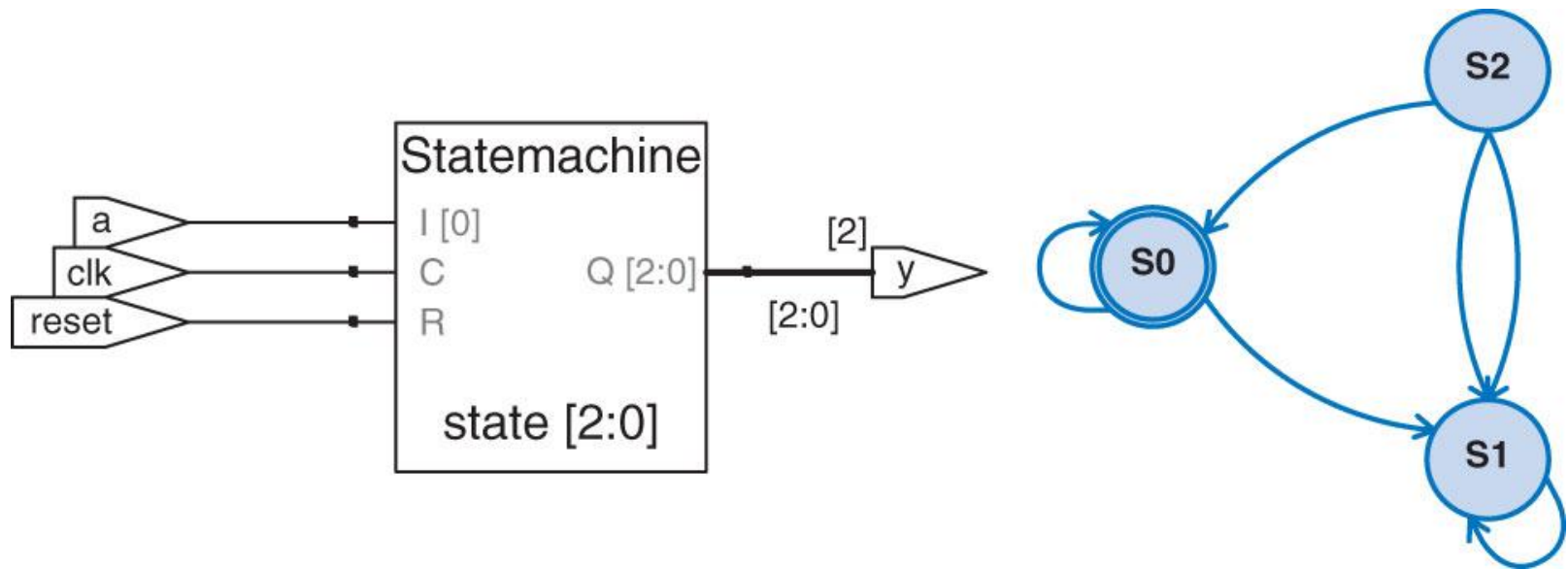


Figure 4.26 patternMoore synthesized circuit

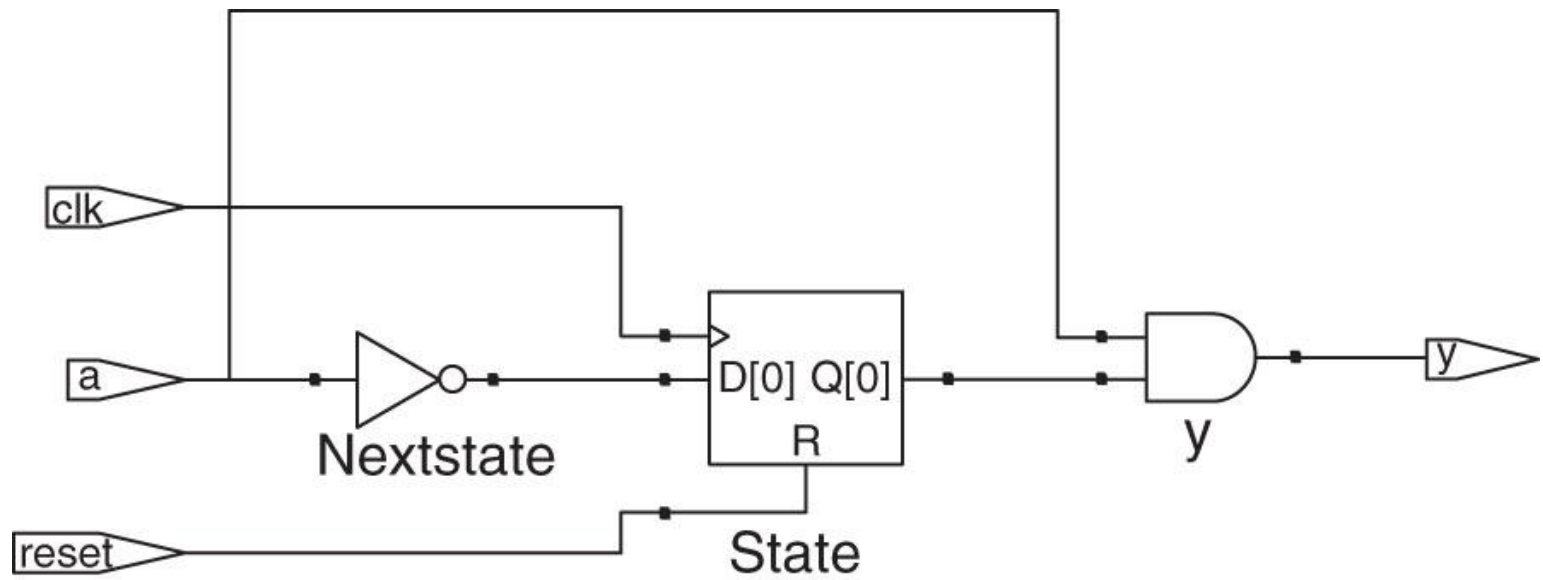


Figure 4.27 patternMealy synthesized circuit

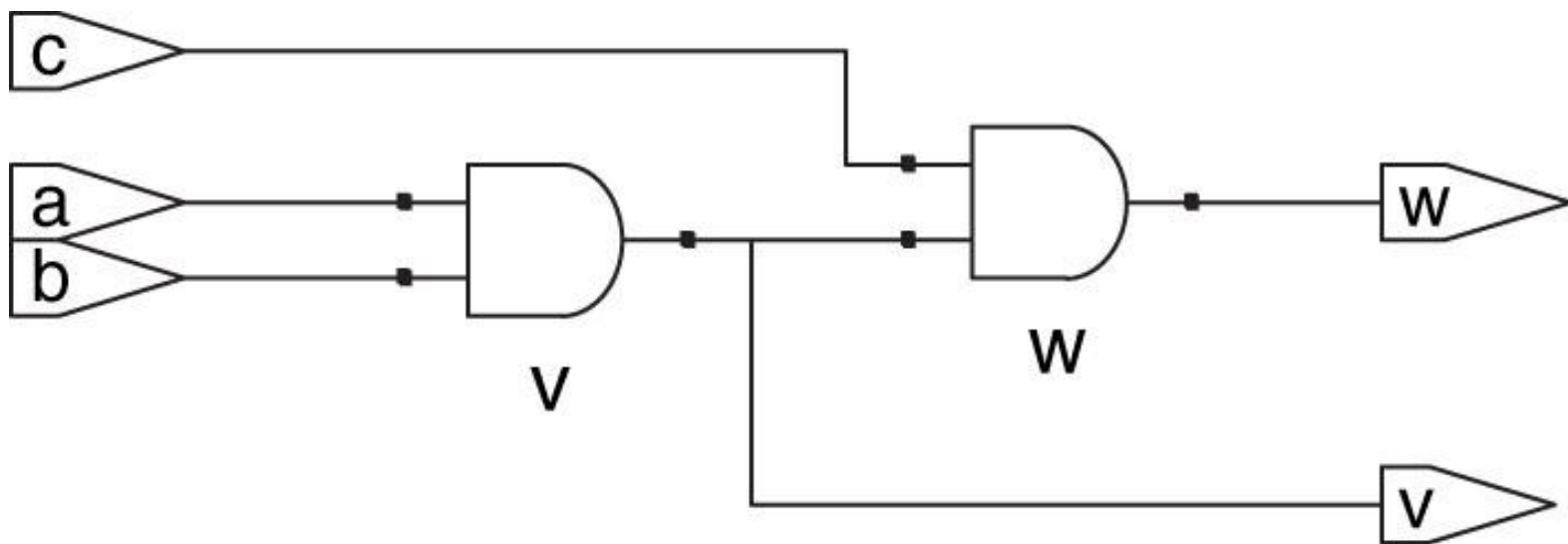


Figure 4.28 and23 synthesized circuit

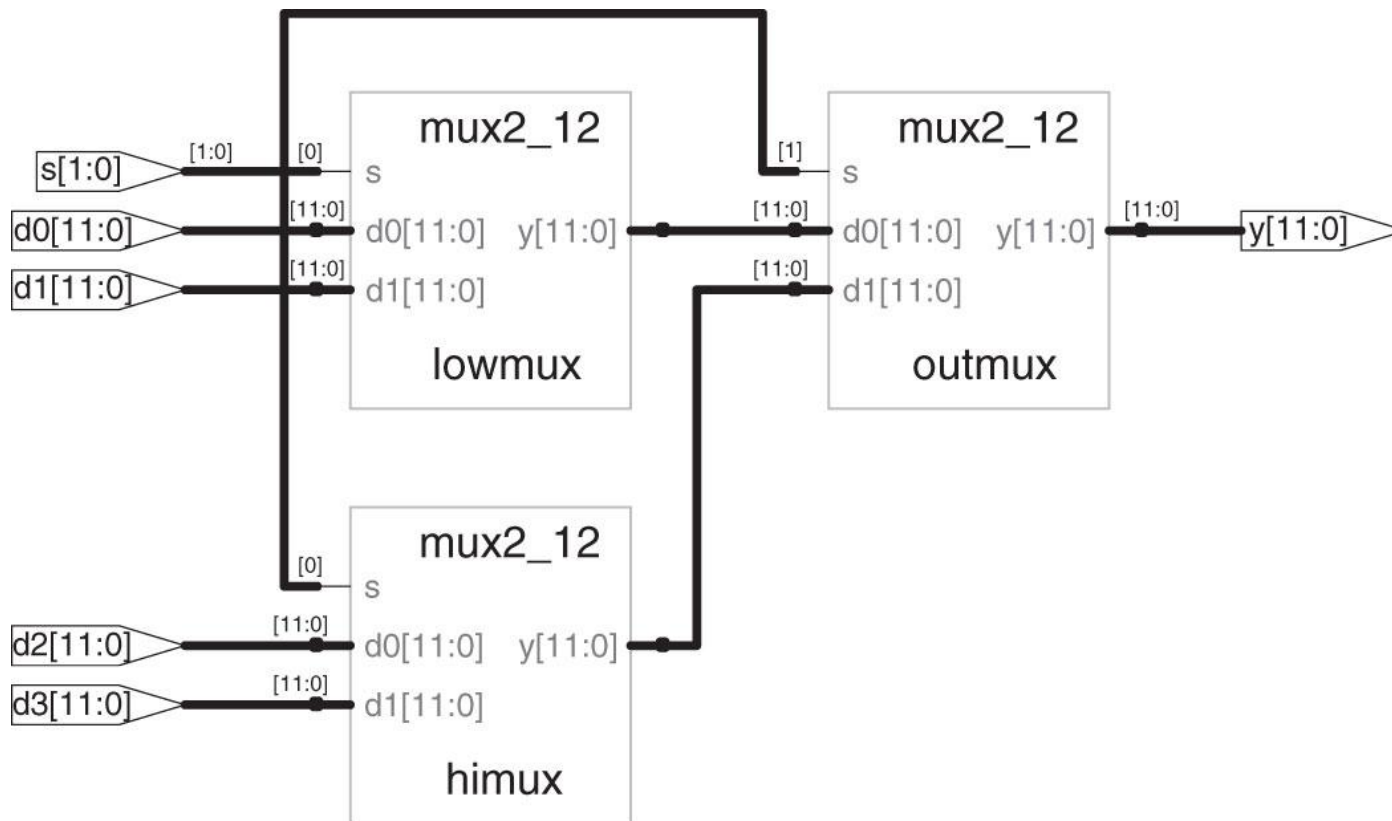


Figure 4.29 mux4_12 synthesized circuit

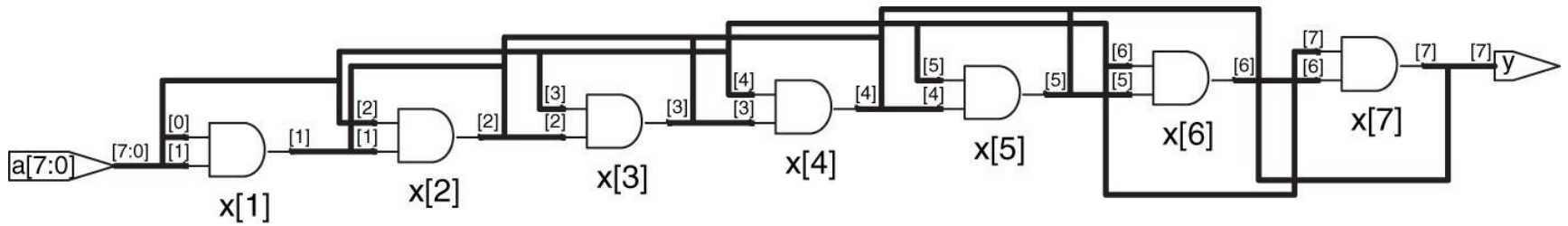


Figure 4.30 andN synthesized circuit

9/2

9/9


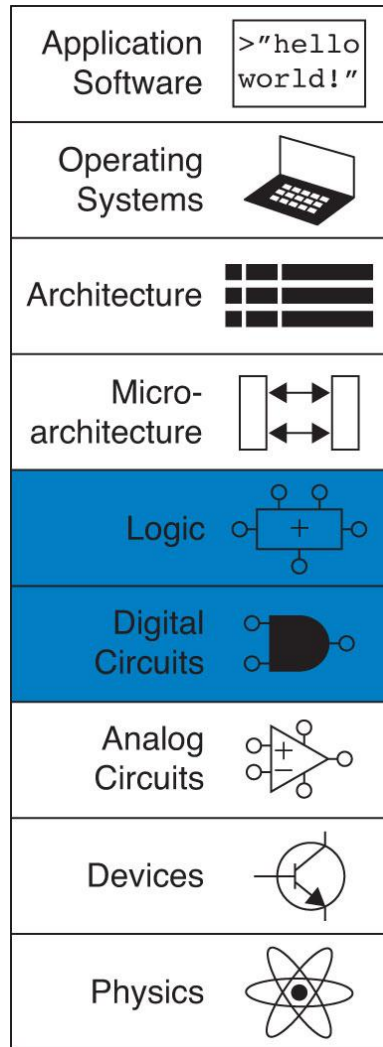
0800 Anton started
 1000 - stopped - Anton ✓ { 1.2700 9.032 847 025
 1300 1030 MP-AC 2.130476415 (1.50476415) 9.037 846 845 correct
 020 PRO 2 2.130476415
 correct 2.130676415
 Relays 6-2 in 023 failed special speed test
 in relay - 11.000 test -
 Relays changed
 1100 Started Cosine Tape (Sine check)
 1525 Started Multi Adder Test.
 1545  Relay #70 Panel F
 (moth) in relay.
 First actual case of bug being found.
 1645 Anton started.
 1700 closed down.

Figure M 01



UNN Figure 1