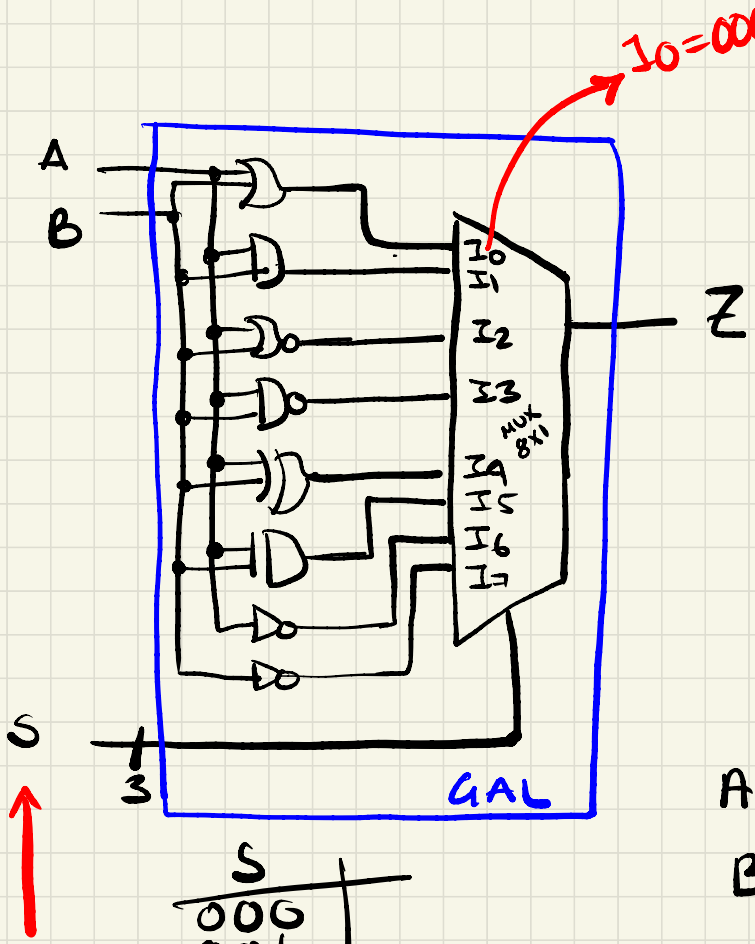

S
000
001
⋮
111

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY MUX IS
PORT (A,B:IN STD_LOGIC;
S:IN STD_LOGIC_VECTOR(2 DOWNTO 0);
Z:OUT STD_LOGIC
);
END ENTITY;

ARCHITECTURE A_MUX OF MUX IS
BEGIN
```

ARQ #1

```
with S SELECT
   Z <= A OR B  when "000",
        A AND B when "001",
        A NOR B  when "010",
        A NANB   when "011",
        A XOR B  when "100",
        A XNORB  when "101",
        NOT A    when "110",
        NOT B    when others;
END A-MUX;
```

ARQ #2

ETIQUETA: PROCESS (S)
BEGIN

Asig. Dir
CASE
IF
FOR-LOOP

```
CASE S IS
when "000" => Z <= A OR B;
when "001" => Z <= A AND B;
when "010" => Z <= A NOR B;
when "011" => Z <= A NAND B;
when "100" => Z <= A XOR B;
when "101" => Z <= A XNOR B;
when "110" => Z <= NOT A;
when others => Z <= NOT B;
END CASE; END PROCESS; END A_MUX;
```