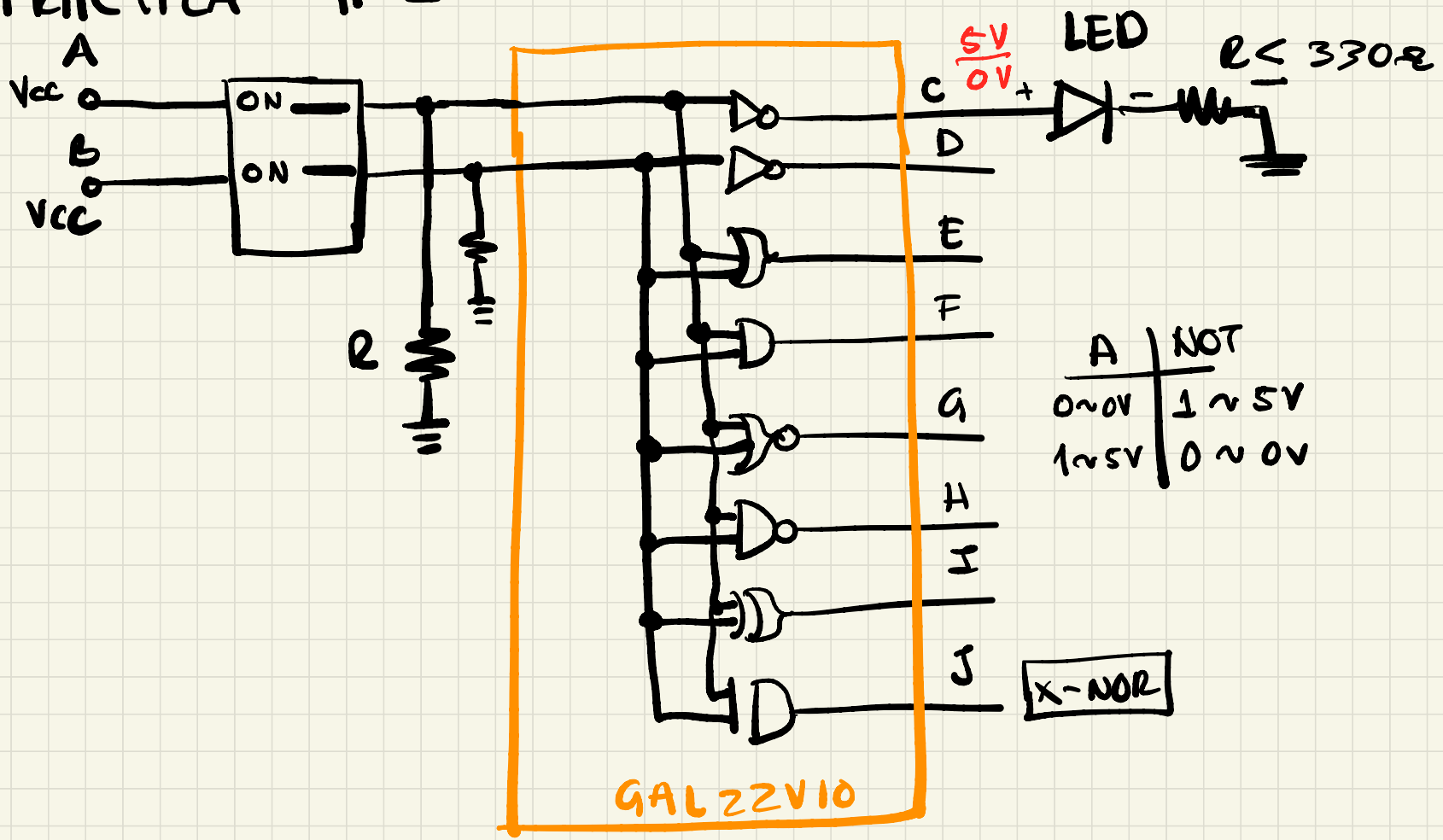
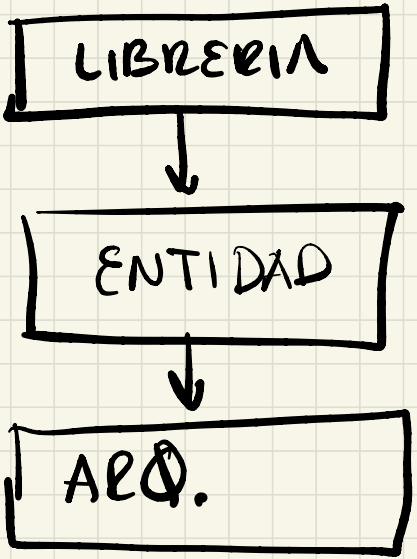
PRACTICA #1



A	NOT
0 ~ 0V	1 ~ 5V
1 ~ 5V	0 ~ 0V

X-NOR

UHDL (Verilog)




```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY P1 IS
PORT(A: IN STD_LOGIC;
     B: IN STD_LOGIC;
     C,D,E,F,G,H,I,J: OUT STD_LOGIC
     );
```

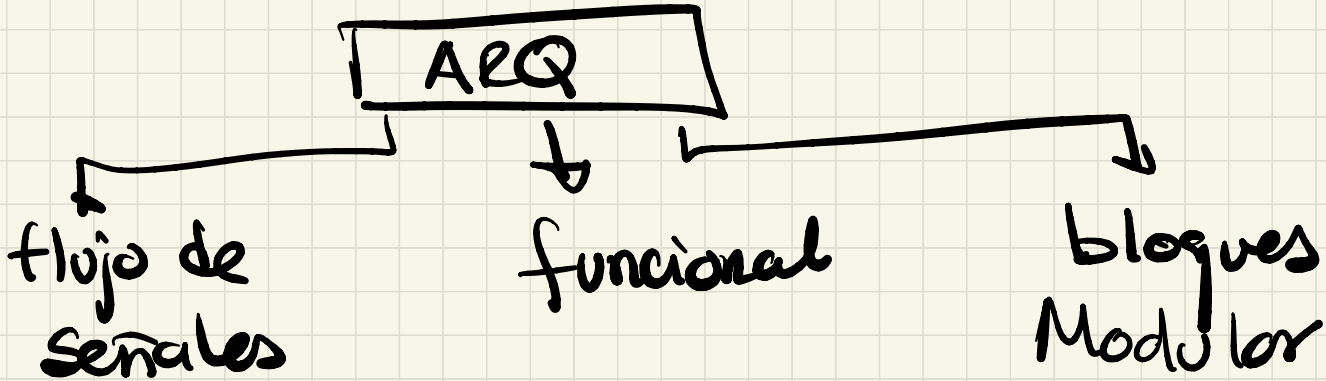
→ ASIGNACIÓN DE PINES

```
END ENTITY; (END P1;)
```

IN
OUT
INOUT

BIT < 0 1

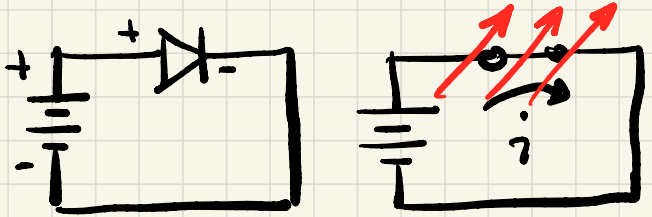
STD_LOGIC < 0 1 Z -1 > H L



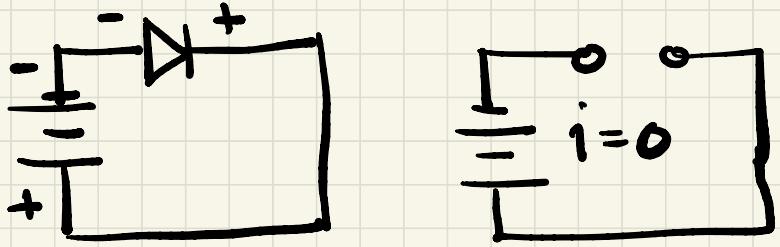

```
ARCHITECTURE A_P1 OF P1 IS
BEGIN
    C <= NOT A;
    D <= NOT B;
    E <= A OR B;
    F <= A AND B;
    G <= A NOR B;
    H <= A NAND B;
    I <= A XOR B;
    J <= A XNOR B;
END A_P1;
```

Asig. --

LED → DIODO



Polarización en directa



polarización en Inversa