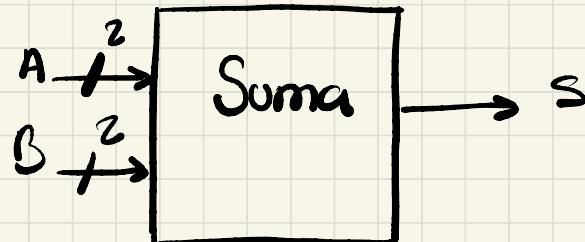


Adición o Suma

suma booleana OR



A	B	S_1, S_0
0+0		0 0
0+1		0 1
1+0		0 1
1+1		1 0

$$S_1 = \sum_m (3) = AB$$

$$S_0 = \sum_m (1, 2) = A \oplus B$$

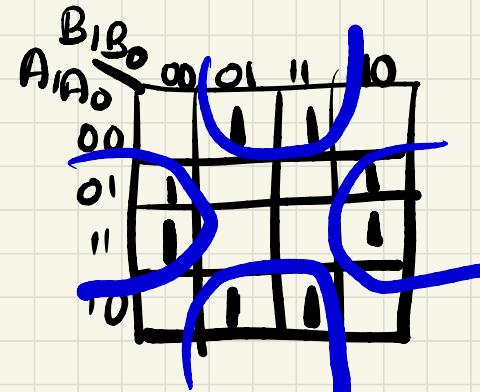
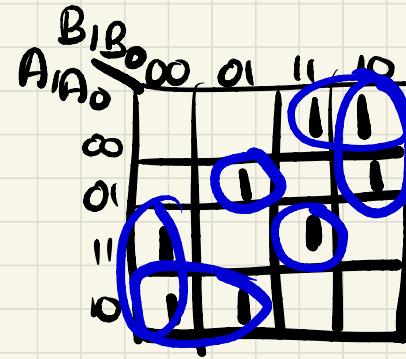
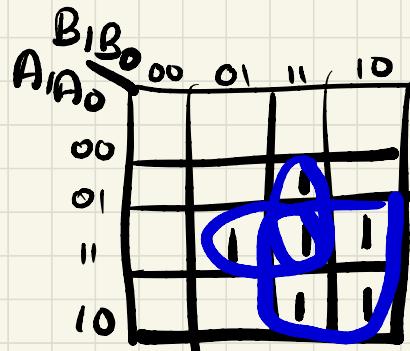
$A_1 A_0$	$B_1 B_0$	$S_2 S_1 S_0$
0 0	+ 0 0	0 0 0
0 0	+ 0 1	0 0 1
0 0	+ 1 0	0 1 0
0 0	+ 1 1	0 1 1
0 1	+ 0 0	0 0 1
0 1	+ 0 1	0 1 0
0 1	+ 1 0	0 1 1
0 1	+ 1 1	1 0 0
1 0	+ 0 0	0 1 0
1 0	+ 0 1	0 1 1
1 0	+ 1 0	1 0 0
1 0	+ 1 1	1 0 1
1 1	+ 0 0	0 1 1
1 1	+ 0 1	1 0 0
1 1	+ 1 0	1 0 1
1 1	+ 1 1	1 1 0

$A_1 A_0$	$B_1 B_0$	S_2	S_1	S_0
0 0	+ 0 0	0 0 0		
0 0	+ 0 1	0 0 1		
0 0	+ 1 0	0 1 0		
0 0	+ 1 1	0 1 1		
0 1	+ 0 0	0 0 1		
0 1	+ 0 1	0 1 0		
0 1	+ 1 0	0 1 1		
0 1	+ 1 1	1 0 0		
1 0	+ 0 0	0 1 0		
1 0	+ 0 1	0 1 1		
1 0	+ 1 0	1 0 0		
1 0	+ 1 1	1 0 1		
1 1	+ 0 0	0 1 1		
1 1	+ 0 1	1 0 0		
1 1	+ 1 0	1 0 1		
1 1	+ 1 1	1 1 0		

$$S_2 = \sum m(7, 10, 11, 13, 14, 15)$$

$$S_1 = \sum m(2, 3, 5, 6, 8, 9, 12, 15)$$

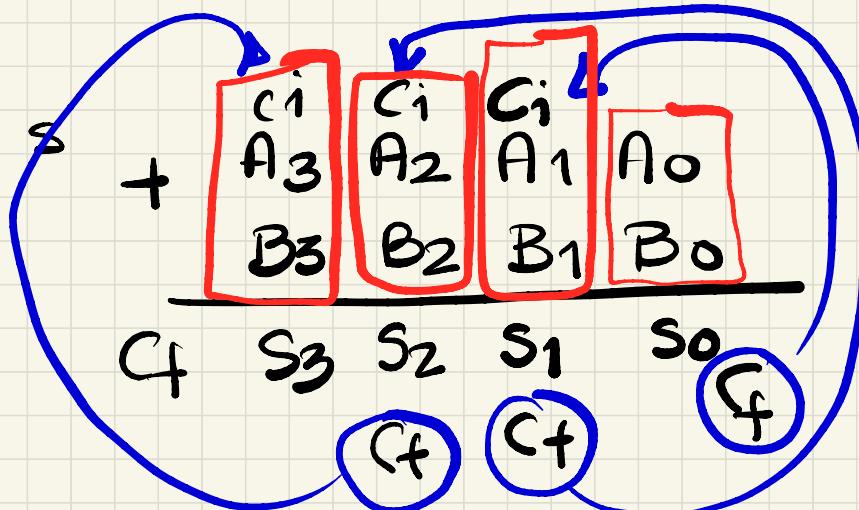
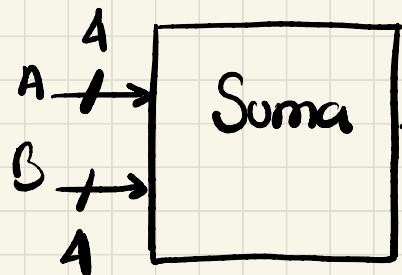
$$S_0 = \sum m(1, 3, 4, 6, 9, 11, 12, 14)$$



$$S_2 = A_1 B_1 + A_1 A_0 B_0 + A_0 B_1 B_0$$

$$S_1 = A_1 \bar{B}_1 \bar{B}_0 + A_1 \bar{A}_0 \bar{B}_1 + \bar{A}_1 \bar{A}_0 B_1 + \dots$$

$$S_0 = A_0 B_0 + \bar{A}_0 B_0$$



$$+ \begin{array}{r} 1 & 1 & 1 \\ 2 & 4 & 8 \\ 3 & 6 & 2 \\ \hline 6 & 1 & 1 & 3 \end{array}$$

A diagram illustrating a partial sum calculation. The inputs C_i, A and B are shown being added to produce the sum S and the carry C_f . The result is enclosed in a pink box.

$$A_0 + B_0 = C_f + S_0$$

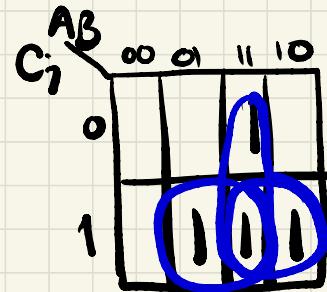
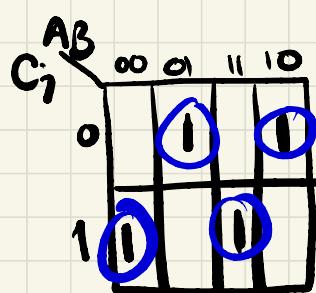
$$\begin{array}{r}
 & c_i \\
 + & A \\
 & B \\
 \hline
 S & C_f
 \end{array}$$

c_i	A	B	S	C_f
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

$$S_i X = A \oplus B$$

$$S = \sum_m (1, 2, 4, 7) = c_i \oplus A \oplus B$$

$$C_f = \sum_m (3, 5, 6, 7) = c_i A + c_i B + AB$$



$$S = \overline{c_i} \bar{A}B + \overline{c_i} A\bar{B} + c_i \bar{A}\bar{B} + c_i AB$$

$$S = \overline{c_i} (\bar{A}B + A\bar{B}) + c_i (\bar{A}\bar{B} + AB)$$

$$S = \overline{c_i} (A \oplus B) + c_i (A \odot B)$$

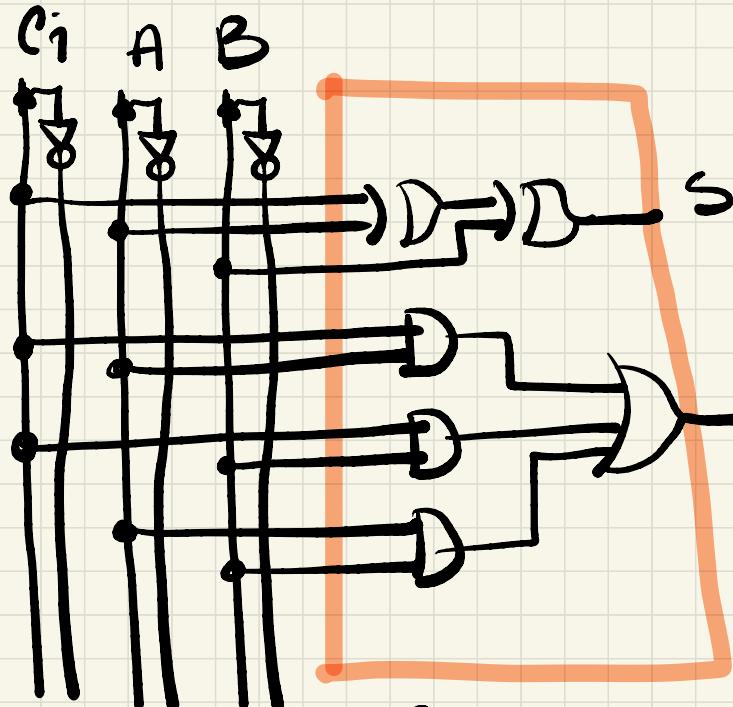
$$S = \overline{c_i} (A \oplus B) + c_i (\overline{A \oplus B})$$

$$S = \overline{c_i} X + c_i \overline{X} = c_i \oplus X$$

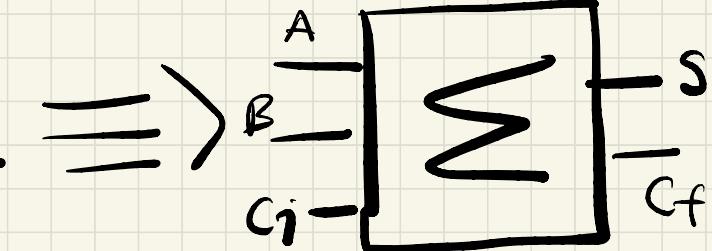
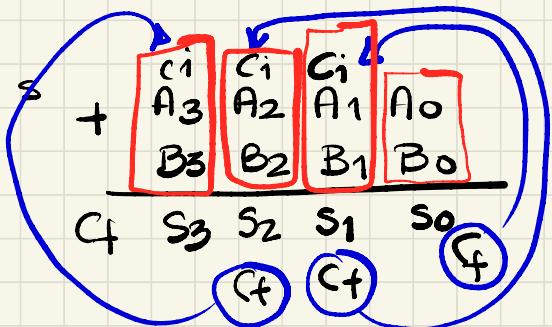
$$S = c_i \oplus A \oplus B$$

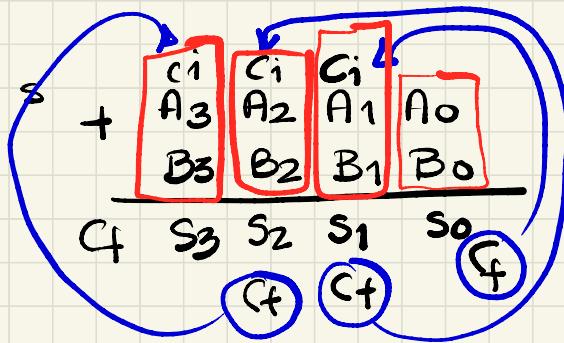
$$S = \sum_m (1, 2, 4, 7) = C_i \oplus A \oplus B$$

$$C_f = \sum_m (3, 5, 6, 7) = C_i A + C_i B + AB$$



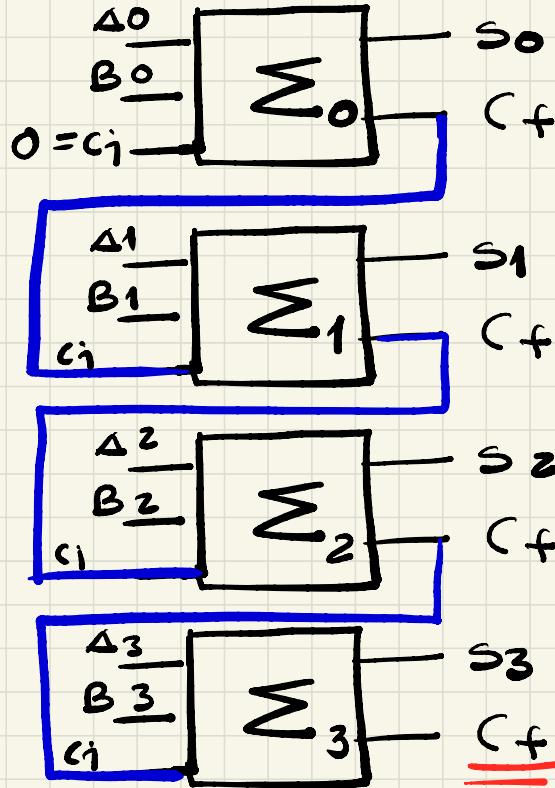
Sumador Completo





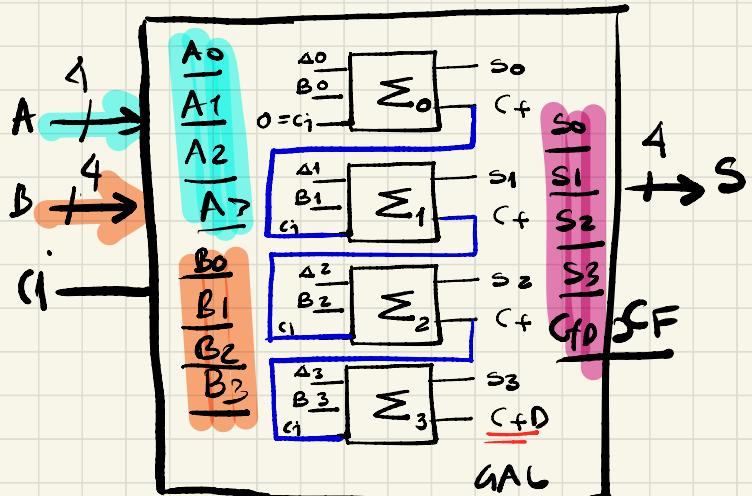
$$\begin{array}{r}
 101111 \\
 101101 \\
 + 111101 \\
 011011 \\
 \hline
 1000010
 \end{array}$$

Binary addition diagram showing the sum of 101111, 101101, and 111101. The result is 1000010. Red annotations show intermediate sums: 101111 + 101101 = 1000010, and 1000010 + 111101 = 10000111. Brackets labeled 'e' indicate the carry bit at each step.



Sumador Completo
de 4 bits.

desborde



$S_0 = C_1 \oplus A_0 \oplus B_0$

 $C_1 = C_1 A_0 + C_1 B_0 + B_0$

$S_1 = C_1 \oplus A_1 \oplus B_1$

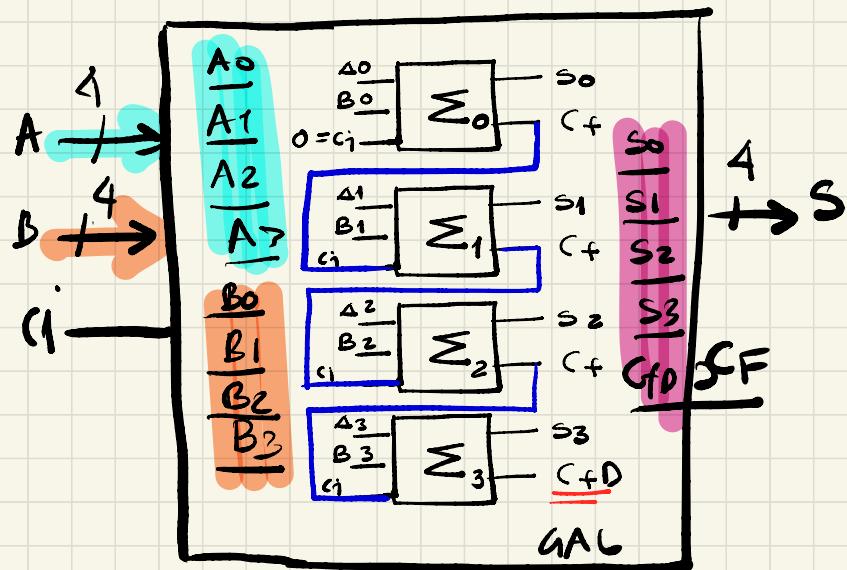
 $C_2 = C_1 A_1 + C_1 B_1 + A_1 B_1$

$S_2 = C_2 \oplus A_2 \oplus B_2$

 $C_3 = C_2 A_2 + C_2 B_2 + A_2 B_2$

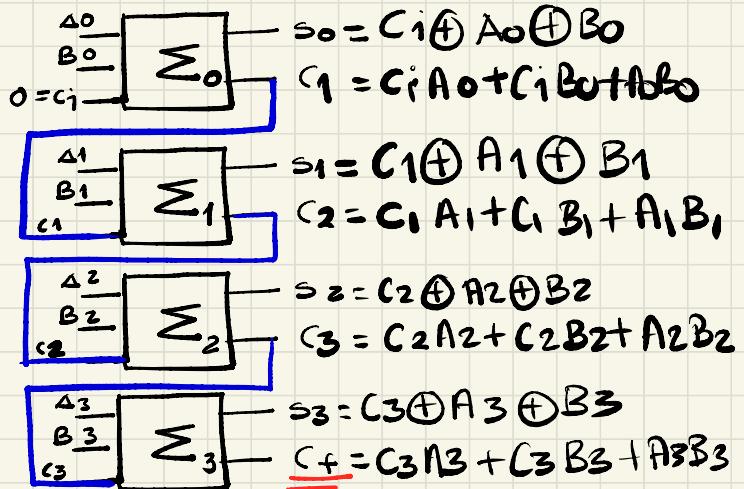
$S_3 = C_3 \oplus A_3 \oplus B_3$

$C_f = C_3 A_3 + C_3 B_3 + A_3 B_3$
desborde



LIBRARY IEEE;
 USE IEEE.STD-LOGIC-1164.ALL;
 ENTITY SV IS
 PORT(A,B: IN STD-LOGIC-VECTOR
 (3 DOWNTO 0);
 Ci: IN STD-LOGIC;
 S: OUT STD-LOGIC-VECTOR (3 DOWNTO 0);
 CF: OUT STD-LOGIC;
);
 END ENTITY;

Descripción
UHDL



$C [C(1) \ C(2) \ C(3)]$
 $S [S(3) \ S(2) \ S(1) \ S(0)]$

ARCHITECTURE A-SU OF SU IS

SIGNAL C: STD-LOGIC-VECTOR(1 TO 3);
BEGIN

$S(0) \leftarrow C_1 \text{ XOR } A(0) \text{ XOR } B(0);$
 $C(1) \leftarrow C_1 \text{ AND } A(0) \text{ OR } (C_1 \text{ AND } B(0)) \text{ OR } (A(0) \text{ AND } B(0));$

$S(1) \leftarrow C(1) \text{ XOR } A(1) \text{ XOR } B(1);$
 $C(2) \leftarrow C(1) \text{ AND } A(1) \text{ OR } (C(1) \text{ AND } B(1))$
 $\text{OR } A(1) \text{ AND } B(1);$

$S(2) \leftarrow C(2) \text{ XOR } A(2) \text{ XOR } B(2);$
 $C(3) \leftarrow C(2) \text{ AND } A(2) \text{ OR } (C(2) \text{ AND } B(2))$
 $\text{OR } A(2) \text{ AND } B(2);$

$S(3) \leftarrow C(3) \text{ XOR } A(3) \text{ XOR } B(3);$
 $CF \leftarrow C(3) \text{ AND } A(3) \text{ OR } (C(3) \text{ AND } B(3))$
 $\text{OR } A(3) \text{ AND } B(3);$
END A-SU;

Sentencia FOR

GENERATE



Inst. concurrentes

→ Sintaxis

LOOP

Inst. Secuenciales

PROCESS

GENERATE

↓

LOOP

CICLO: FOR I IN (RANGO)

Instrucciones {
GENERATE
WHEN-ELSE
WITH-SELECT
END GENERATE}

LOOP
GENERATE

IF
CASE-WHEN
END LOOP;

(I_{min} TO I_{max})

(I_{MAX} DOWNTO I_{MIN})

Funciones
Booleanas

$$S(0) \leftarrow C_1 \text{ XOR } A(0) \text{ XOR } B(0);$$
$$C(1) \leftarrow C_1 \text{ AND } A(0) \text{ OR } C_1 \text{ AND } B(0) \text{ OR } A(0) \text{ AND } B(0);$$
$$S(1) \leftarrow C(1) \text{ XOR } A(1) \text{ XOR } B(1);$$
$$C(2) \leftarrow C(1) \text{ AND } A(1) \text{ OR } C(1) \text{ AND } B(1) \\ \text{OR } A(1) \text{ AND } B(1);$$
$$S(2) \leftarrow C(2) \text{ XOR } A(2) \text{ XOR } B(2);$$
$$C(3) \leftarrow C(2) \text{ AND } A(2) \text{ OR } C(2) \text{ AND } B(2) \\ \text{OR } A(2) \text{ AND } B(2);$$
$$S(3) \leftarrow C(3) \text{ XOR } A(3) \text{ XOR } B(3);$$
$$CF \leftarrow C(3) \text{ AND } A(3) \text{ OR } C(3) \text{ AND } B(3) \\ \text{OR } A(3) \text{ AND } B(3);$$
$$C [C(0) \ C(1) \ C(2) \ C(3) \ C(4)]$$
$$\{ 0 \text{ TO } 4 \}$$
$$C(0) \leftarrow (1, \ CF \leftarrow C(4))$$

FOR I IN (0 TO 3) GENERATE

$$S(I) \leftarrow C(I) \text{ XOR } A(I) \text{ XOR } B(I);$$
$$C(I+1) \leftarrow C(I) \text{ AND } A(I)$$
$$\text{OR } C(I) \text{ AND } B(I) \text{ OR }$$
$$A(I) \text{ AND } B(I);$$

DESCRIPCION CON SENTENCA FOR

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
ENTITY SU IS
PORT(A,B: IN STD_LOGIC_VECTOR
      (3 DOWNTO 0);
      C1: IN STD_LOGIC;
      S: OUT STD_LOGIC_VECTOR (
      3 DOWNTO 0));
      CF: OUT STD_LOGIC
      );
END ENTITY;

ARCHITECTURE A_SU OF SU IS
SIGNAL C: STD_LOGIC_VECTOR (0 TO 4);
BEGIN
  C(0) <= C1;
```

FOR I IN (0 TO 3) GENERATE
 S(I) <= C(I) XOR A(I) XOR B(I);
 C(I+1) <= C(I) AND A(I) OR C(I) AND B(I)
 OR A(I) AND B(I);
END GENERATE;
CF <= C(4);
END A - SU;

C

DESCRIPCION CON EL OPERADOR "+"

```
LIBRARY IEEE;
```

```
USE IEEE.STD_LOGIC_1164.ALL;
```

```
USE IEEE.STD_LOGIC_UNSIGNED.ALL; → (+,-)
```

```
ENTITY SU IS
```

```
PORT(A,B: IN STD_LOGIC_VECTOR
```

```
(3 DOWNTO 0);
```

```
C: IN STD_LOGIC;
```

```
S: OUT STD_LOGIC_VECTOR(
```

```
4 DOWNTO 0)
```

```
);
```

```
END ENTITY;
```

```
ARCHITECTURE A-SU OF SU IS
```

```
BEGIN
```

```
S<= A + B;
```

OP.

$S \leq '0' \& A + '0' \& B;$

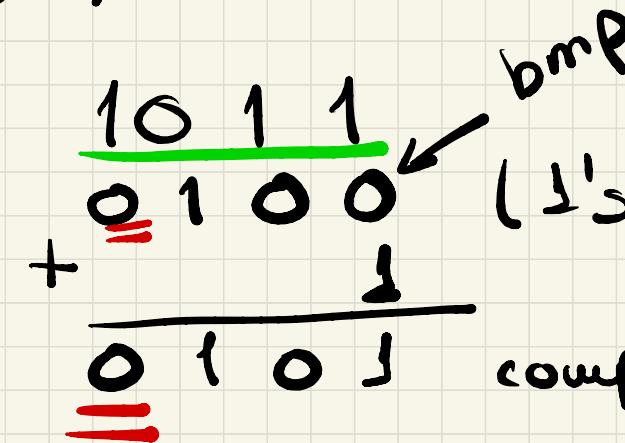
↳ 0 A(3) A(2) A(1) A(0)

COMPLEMENTOS

- Complemento a la base
- Complemento a la base -1

Sistema binario

- Complemento a la base → complemento a 2
- Complemento a la base -1 → complemento a 1
 $(2-1)$

① comp. a 1 
+ 0100

1

② comp. a 2 
+ 0100

0101 comp. a 2

$$\begin{array}{r}
 \text{10} \ 11 \ \text{?} \\
 \left\{ \begin{array}{l} \text{0100 comp. a3} \\ \text{0101 comp. a2} \end{array} \right. \\
 \downarrow \quad \downarrow \\
 \begin{array}{r}
 \begin{array}{r}
 \text{0101} \\
 + \text{1010} \\
 \hline
 \text{1011}
 \end{array} \text{ bnp } \\
 \text{comp. a1} \\
 + \text{1} \\
 \hline
 \text{1011} \text{ comp. a2}
 \end{array}
 \end{array}$$

$$\begin{array}{r}
 \text{10} \\
 + \text{1} \\
 \hline
 \text{10} \text{ compa2} \\
 \hline
 \begin{array}{c}
 " - " \xrightarrow{\text{---}} \overset{0}{1} \\
 \text{bit de signo}
 \end{array}
 \end{array}$$

Complemento 02

$$1011 \rightarrow +11$$

$$0101 \rightarrow -11$$

1011

bs

0 1011

1 1011

RESTA

Por Complemento a 2

$$\begin{array}{r} A_3 \ A_2 \ A_1 \ A_0 \\ - \ B_3 \ B_2 \ B_1 \ B_0 \\ \hline \end{array}$$

$$\begin{array}{r} 2'698 \\ - 1'752 \\ \hline 0946 \\ \hline 0 \end{array}$$

$$\begin{array}{r} A_3 \ A_2 \ A_1 \ A_0 \\ - \ (B_3 \ B_2 \ B_1 \ B_0 \text{ comp. a } 2) \\ \hline \end{array}$$

$$\left\{ \begin{array}{l} \begin{array}{r} A_3 \ A_2 \ A_1 \ A_0 \\ - (B_3 \ B_2 \ B_1 \ B_0) \\ \hline \end{array} \\ + \frac{(B_3 \ B_2 \ B_1 \ B_0) \text{ comp.}}{2} \end{array} \right.$$

Ejemplo:

$$\begin{array}{r} 1010 \\ - \boxed{10111} \\ \hline \end{array}$$

→ A
→ B

A red arrow points from the sum of the first two columns to the result.

$$\begin{array}{r} 0111 \\ + 1000 \\ \hline \boxed{1001} \end{array}$$

bnd
comp. a 1
comp. a 2

$$\begin{array}{r} 1010 \\ + 1001 \\ \hline \end{array}$$

10011

=
bay!!!

Ejemplo:

$$\begin{array}{r} 0111 \rightarrow A \\ - \boxed{1010} \rightarrow B \\ \hline 0111 \\ + 0110 \\ \hline 1101 \\ -3 \\ \hline \end{array}$$

$\begin{array}{r} 1010 \\ 0101 \\ + 1 \\ \hline \boxed{0110} \text{ comp02} \end{array}$

$\begin{array}{r} 1101 \\ 0010 \\ + 1 \\ \hline 0011 \end{array}$

Annotations:

- A red box highlights the number 1010 under B .
- A red arrow points from the sum 1101 to the result -3 .
- A pink arrow points from the result -3 to the final result 0011 .
- A red box highlights the result 0110 labeled "comp02".
- A red box highlights the result 0011 labeled "comp-a1".
- A red arrow points from the result 0110 to the result 0011 .
- A red arrow points from the result 0011 back to the result 0110 .
- A label "bmp" is written above the boxes for "comp02" and "comp-a1".

$A_3 A_2 A_1 A_0$ $\underline{+ (B_3 \ B_2 \ B_1 \ B_0) \text{ comp. a } 2}$ $A_3 \ A_2 \ A_1 \ A_0$

$$+ \begin{array}{cccc} \overline{B_3} & \overline{B_2} & \overline{B_1} & \overline{B_0} \\ \hline & & 1 & \end{array}$$

comp. a 1

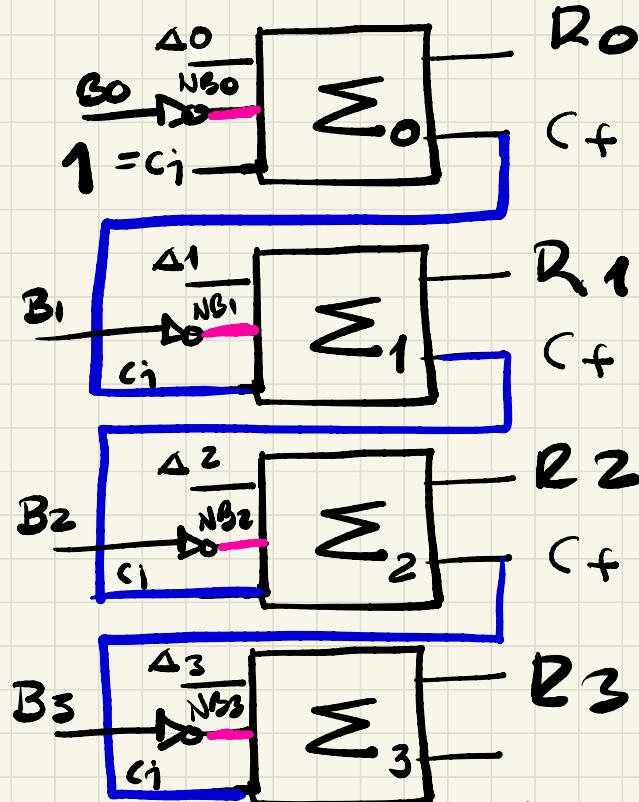
bnp

$\left. \begin{array}{c} \\ \\ \end{array} \right\} \text{ compa 2 de B}$

 $R_3 \ R_2 \ R_1 \ R_0$

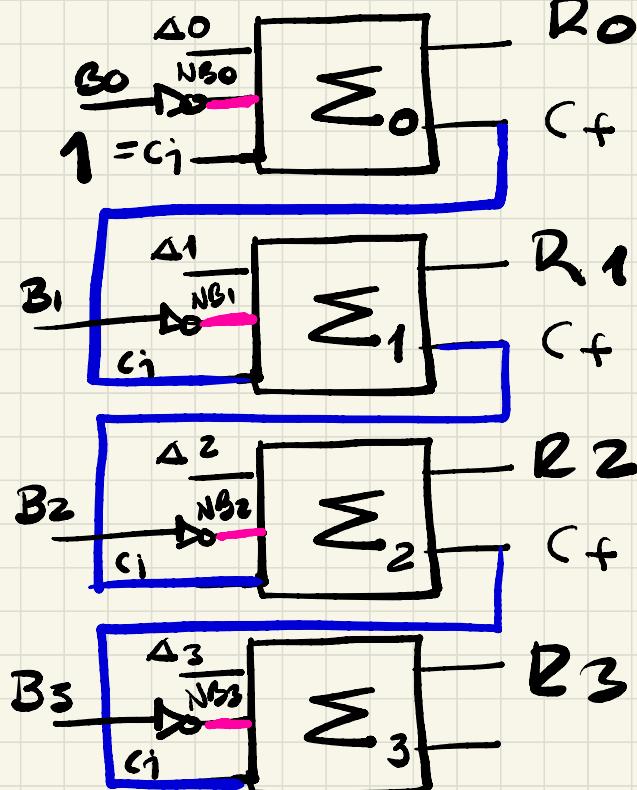
$$\begin{array}{r}
 A_3 \quad A_2 \quad A_1 \quad A_0 \\
 + \quad \overline{B_3} \quad \overline{B_2} \quad \overline{B_1} \quad \overline{B_0} \xleftarrow{\text{bnp}} \\
 \hline
 R_3 \quad R_2 \quad R_1 \quad R_0
 \end{array}$$

$1 = C_1$



PRACTICA 3

Sumador / Restador



C	0	B	\leftarrow sume
0	1	\overline{B}	\leftarrow restar

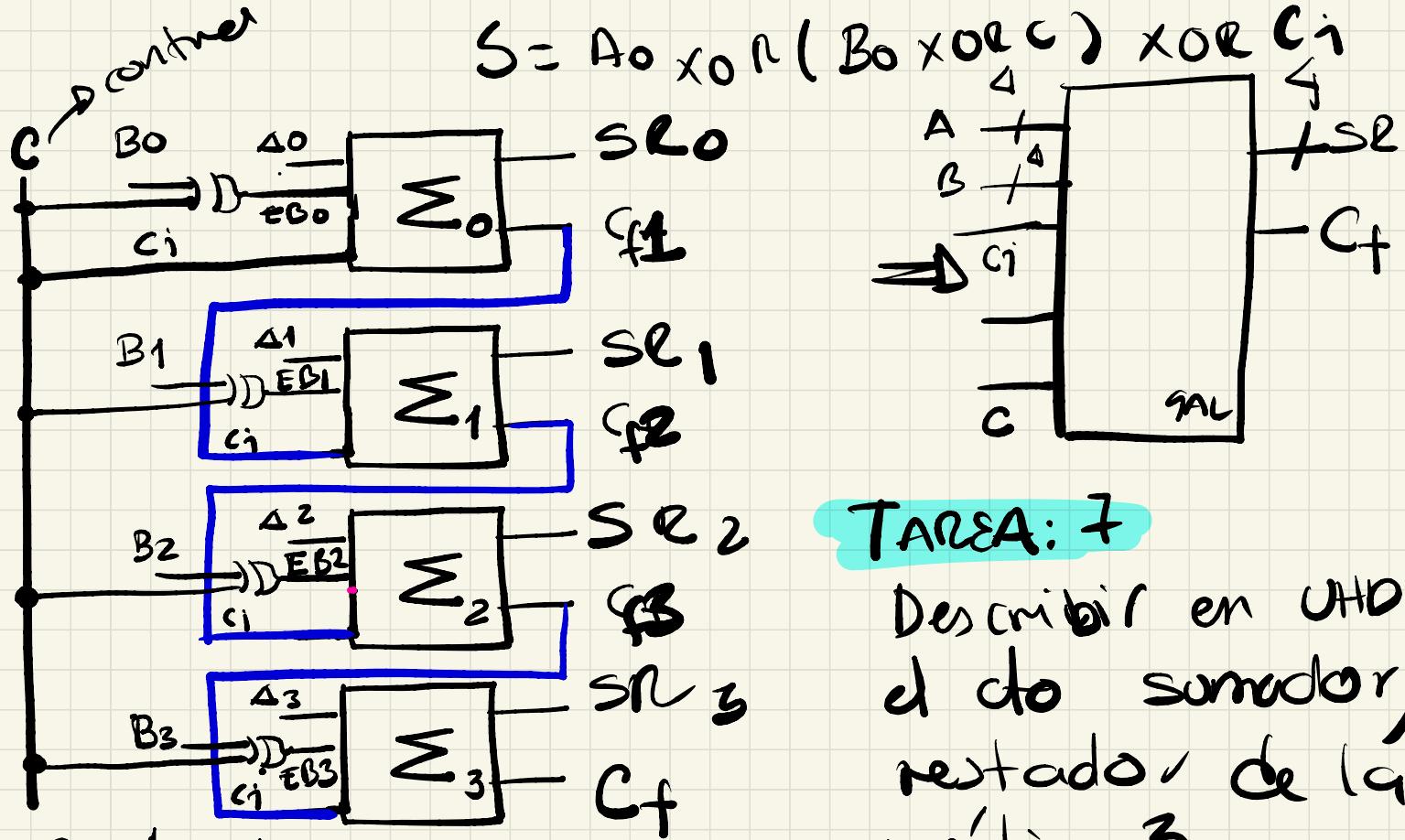
C	B	NB
0	0	0
0	1	1

B

\overline{B}

$$NB = \sum_m (1, 2)$$

$$NB = C \oplus B$$



TAREA: 7

Describir en VHDL
el do sumador/
restador de la

práctica 3
 $C_f = A_3 (B_3 \oplus \text{OR}(C)) \oplus A_3 C_i \oplus S_{R3} \oplus (B_3 \oplus \text{OR}(C)) C_3$