# Introduction to Very Large-Scale Integration (VLSI)

## Assessment

For the following projects, Design and Test bench are to be written in Verilog. Codes are to be submitted along with screenshots of the output & waveforms.

Use appropriate Modelling/statements as mentioned only.

1. Gate Level Modelling (Use $display)
    a. All Logic Gates.
    b. 4-bit Full Adder with Instantiating top-down methodology.
2. Data Flow Modelling (Use $display)
    a. 16:1 Mux using 4:1 Mux only.
    b. 8 to 3 Decoder.
3. Behavioral Modelling (Use $monitor)
    a. JK Flip Flop using conditional statements.
    b. Up-counter & Down-counter using loops.