ECE 4150/6250 – PreLab for Lab7

Objectives:

- Prepare your script and TB files.

(TA will move to the Lab7 in 15 mins)

Note: You can change the suggested "ece4150_6250" folder name to your own one in the labs thereafter.

Before running lab 7, perform the following steps:

Login to your workstation and open a terminal window. Type the following commands:

```
cd ~/ece4150_6250/lab5/src
cp /home/seas/vlsi/course_ece128/lab_files/lab5/tmax_atpg.tcl ~/ece4150_6250/lab5/src
```

Use gedit to edit the tmax_atpg.tcl. In the script, replace the commands under the # write out patterns (overwrite old files) with the following commands:

```
write_patterns ripplecarry4_clk.stil -format stil -replace
write_testbench -input ripplecarry4_clk.stil -output maxtb -replace
dc_shell -f dc_syn.tcl -f dc_test.tcl
tmax tmax_atpg.tcl
```

The last two lines automate what was done in lab5. It has regenerated all necessary files for lab #7. In the future, all you need to do to synthesize & run scan-ATPG is edit dc_syn.tcl, dc_test.tcl, and tmax_atpg.tcl and run them as you have above.

In terminal type:

```
        stil2verilog -generate_config myconfig
```

Edit the file: myconfig and find the line starts with set cfg_dut.. and rename it as ripplecarry4_clk

```
        set cfg_dut_module_name "ripplecarry4_clk"
```

Move maxtb.v file to src folder: mv maxtb.v ./src

Open up an editor (like gedit) and edit the file: gedit ~/ece4150_6250/lab5/src/maxtb.v

Right before the "end module" statement, add the following lines of verilog:

```
        initial begin
        $shm_open ("ripplecarry4_clk_scan_patterns.db") ;
        $shm_probe("AS");

        end
```

In terminal type:

```
        sim-nc maxtb.v ripplecarry4_clk_scan.v osu_scan.v osu05_stdcells.v
```

If you see no errors after running these files, you are ready to run lab7.

If you see errors, show your GTA, do not proceed to lab7 until he has cleared you.