ECE4150 - Lab 9 - CPU Project: Synthesis of Controller, Regfile, ALU

Objectives:
This lab is mandatory as is attendance, results of this lab must be uploaded to BLACKBOARD.
- the next several labs will be used to help you with the final CPU project
- this lab time must be used wisely so the student completes the final project in time before the end of the semester

1) Use synopsys to synthesize the CPU modules you've completed for HW thus far:
   a) Create a new directory for your CPU project:
      -open a terminal and type:

```
mkdir ~/ece4150_6250/project
mkdir ~/ece4150_6250/project/alu_regf
mkdir ~/ece4150_6250/project/alu_regf/src
mkdir ~/ece4150_6250/project/alu_regf/work
mkdir ~/ece4150_6250/project/alu_regf/db
mkdir ~/ece4150_6250/project/alu_regf/reports
mkdir ~/ece4150_6250/project/controller
mkdir ~/ece4150_6250/project/controller/src
mkdir ~/ece4150_6250/project/controller/work
mkdir ~/ece4150_6250/project/controller/db
mkdir ~/ece4150_6250/project/controller/reports
```

Note: you can modify the directory name "ece4150_6250" as need.

   b) copy the verilog files you've create in your HW's to the directories above:

```
#  HW #3 work
cp ~/ece128/hw3_prob4/alu.v ~/ece4150_6250/project/alu_regf/src
cp ~/ece128/hw3_prob4/alucontrol.v ~/ece4150_6250/project/alu_regf/src
cp ~/ece128/hw3_prob4/regfile.v ~/ece4150_6250/project/alu_regf/src
cp ~/ece128/hw3_prob4/alu_tb.v ~/ece4150_6250/project/alu_regf/src
(note you may have named the test bench in HW3 something different)

# HW #5 work
cp ~/ece128/hw5_prob4/controller.v ~/ece4150_6250/project/controller/src
cp ~/ece128/hw5_prob4/controller_tb.v ~/ece4150_6250/project/controller/src
(note you may have named the test bench in HW5 something different)
```

   c) Copy the appropriate synthesis scripts (see labs 2 & 4) into your proj. directory:

```
cp <the scripts> ~/ece4150_6250/project/alu
cp <the scripts> ~/ece4150_6250/project/controller

edit the synthesis scripts to match your module and file names
```

   d) For the ALU, since the regfile, alu, and alu_controller do not connect without the tb, synthesize each module separately. Create a separate script for each module.

   e) Not all things synthesize just because the verilog compiles. You may need to change your code to get your code the synthesize.
      -Use the bulk of today's lab time to get each component to synthesize

   f) Test each synthesiezd module with the test benches you've created in HW.
      -If things do not work, you must keep working on the synthesis
      -perhaps your clk is too fast/too slow/etc
      -you can adjust it in the synthesis script

2) Turn in (at the end of lab today in BLACKBOARD):
   a) Create word document that contains:
      Synthesis reports (all reports) for each of your modules (controller/regfile/alu/alucontroller)

   b) Show at the top of each section of your document how much area each module takes

   c) What is the fastest clock frequency you can choose for your modules thus far?
      -look at the timing report for each module, you want to change the clk frequency to meet the slack for the slowest of all your modules

```
   d) UPLOAD TO BLACKBOARD (under Homework - Lab / Lab 9 Upload)


3) If you have additional time (Extra Credit Opportunity):
   a) Use this lab time wisely, you have a GTA that you can ask questions.
   b) Do one of the following (or all if you have time):
         i) create the Program Counter Controller Module (see arch. document)
                  -make a directory: mkdir ~/ece4150_6250/project/pc
                                     mkdir ~/ece4150_6250/project/pc/src
                                     mkdir ~/ece4150_6250/project/pc/work
                                     mkdir ~/ece4150_6250/project/pc/db
         ii) modify the controller.v and alucontrol.v to support the ADDI instruction
                  -you will need to add additional states to the controller's FSM
                  -use other 'immediate' instructions as a model
         iii) complete the datapath.v module that was assigned in HW #6

   c) You will eventually have to do each of these things above,
      using the labtime to do it, will leave you more time for your
      senior design work at the end of the semester!
   d) You will receive extra credit in lecture (droping of lowest quiz grade) if you
      complete the above modules (i, ii, iii) & show output of succesful synthesis to the
      lecture instructor.
```