

VLSI SYSTEM DESIGN
(GRADUATE LEVEL)

N26F300

Fall 2022
Rev 1

Preliminary Project Planning Form

Due day: 2:00pm 11/09/2022

One per team. Submit to the course website on Moodle.

(Grades of this form is part of final project. **Please answer with cautions!**)

TEAM Name: ____男童俱樂部____

(If you want to change your team name, please also specify your old team name.)

Team Leader Name: 黃昱澄

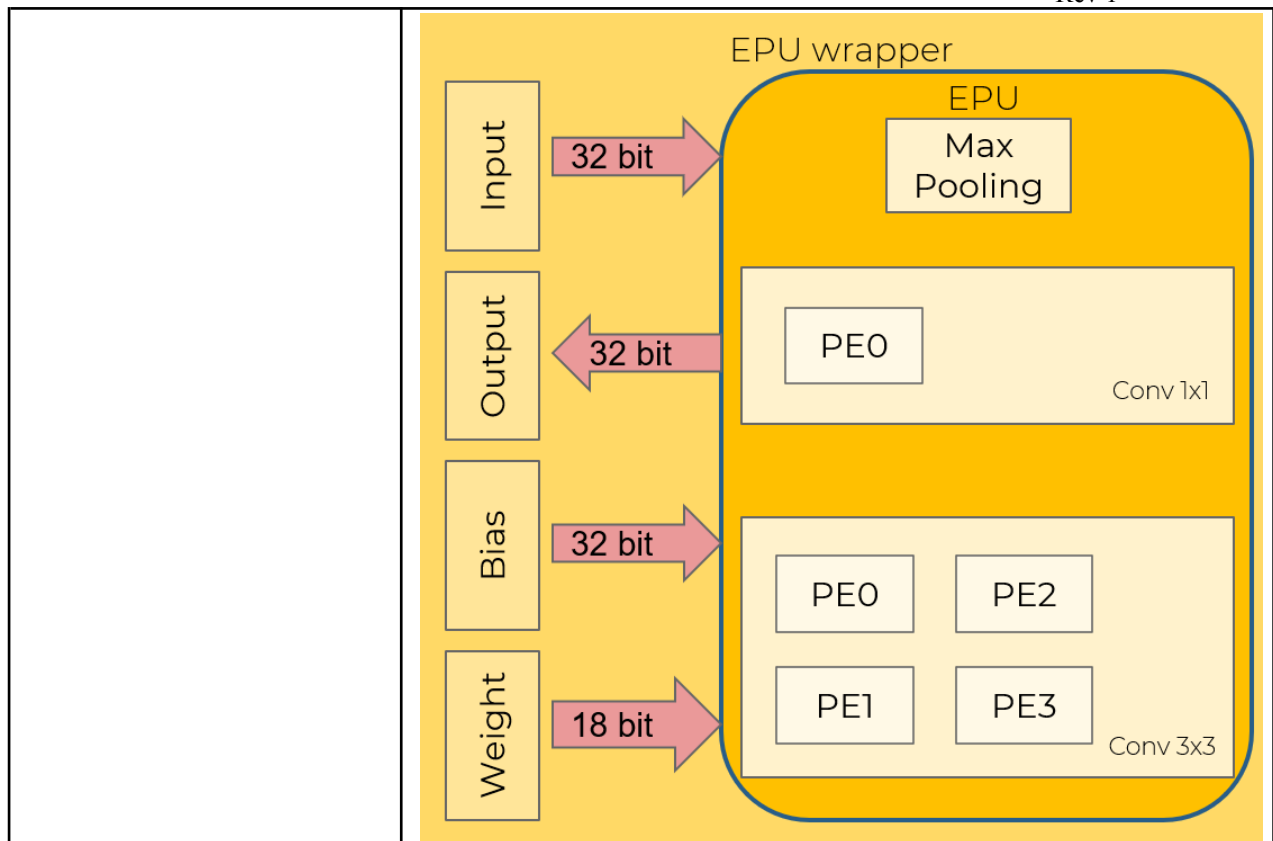
Members Name: 王昱承、黃冠予、俞杉麒、賴致文、陳奕萍

Target Application for ASPU or Duo-Core	A CNN accelerator for fruit recognition
<p><i>Please describe your target application with short motivation and key components that will be related to your application processor</i></p> <p><u>(Note that audio is one of applications. ADC/DAC is one of important components, but is not considered as an application.)</u></p>	<p>[Overview] Nowadays, Self-checkout system is getting more and more popular. However, in the process of selling fruit and vegetables in the supermarket, it still requires staff to recognize and weigh. And if consumers do not know the name of a fruit or vegetable, they may spend time looking for or waiting for service staff to get the information. Therefore, we promote a solution based on an ASIC CNN accelerator that is capable of recognizing variety of different fruit and vegetable images automatically which will be helpful for fruit sellers and consumers.</p> <p>[key parts with block diagram] Data will be transferred by Input and Output wrapper, and it is 32 bits to satisfy AXI's spec. Bias and Weight will transfer by Bias wrapper and Weight wrapper separately. Bias will be 32 bit. Since we use Clip-Q to compress memory size, 2 bits are required to store every weight in 3*3 kernel. Therefore weight will be 18 (2*9) bit.</p>

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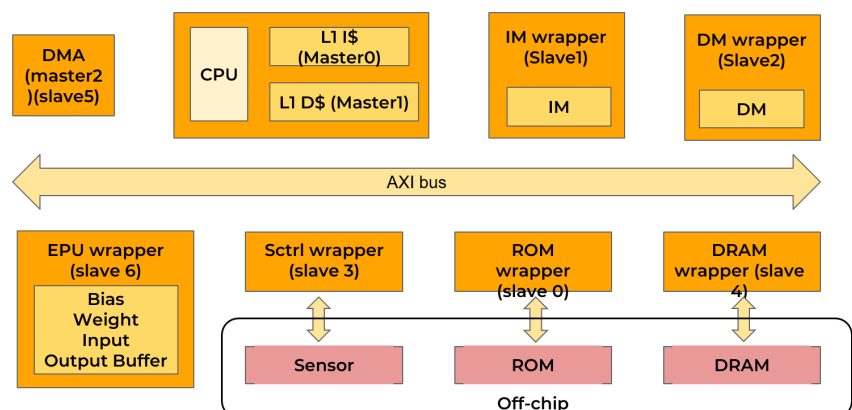
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Please describe your application with targeting specification and how the application processor will work with CPU & memory on both hardware and software sides.

dataflow: top module: Dram->AXI->DMA->AXI->EPU
EPU module: AXI->buffer(w, b...)->conv_and_acc
conv_and_acc: (conv3x3, conv1x1)->maxpool->output

- 1.Input Buffer : 15.4 MB
- 2.Weight Buffer :1.4 MB
- 3.Bias Buffer : 3.2 KB
- 4.Output Buffer : 15.4 MB



Please provide task assignment for every member. There shall be at least one person dedicate

Software : 王昱承、陳奕萍
Hardware : 黃昱澄、黃冠予
Validation : 俞杉麒、賴致文

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<p><i>to verification of IPs.</i></p> <p><i>Please provide project time schedule by providing all members milestones for their own tasks using a chart. Note that please plan by week and DO check the dates for demo and final presentation.</i></p> <p><u>Be aware of the schedule posted on the course website.</u></p>	<div><div><div>11月11日</div><div>11月21日</div><div>12月1日</div><div>12月11日</div><div>12月21日</div><div>12月31日</div></div><div><div>架設NIN神經網路</div><div>用CLIP-Q改善NIN</div><div>training</div><div>撰寫EPU</div><div>撰寫DMA</div><div>驗證電路正確性</div></div></div>
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