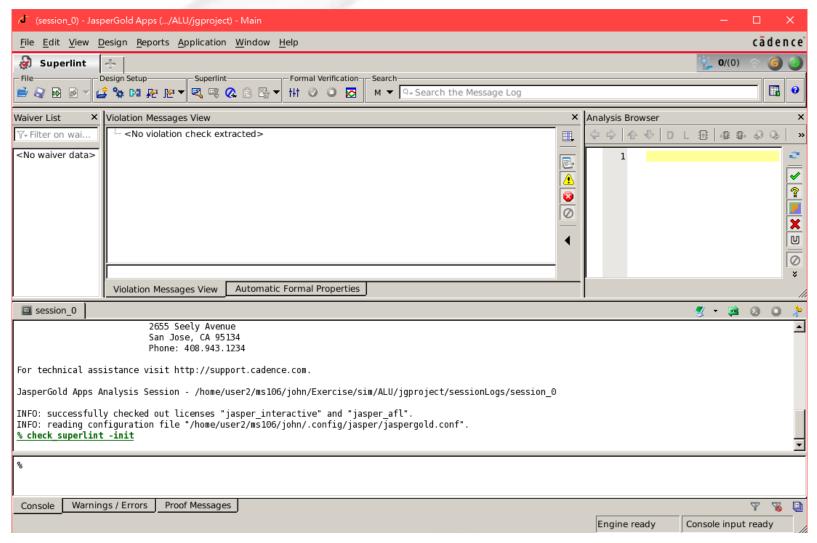


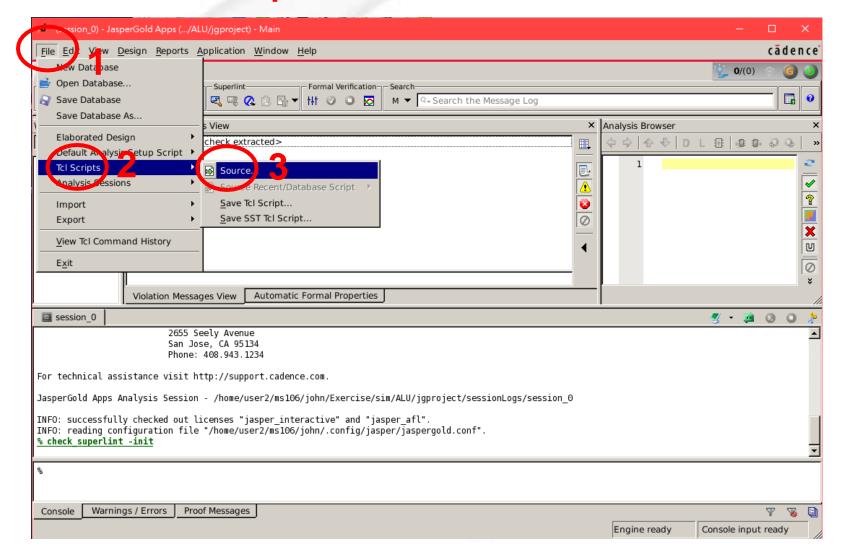
# Start Superlint

>>jg -superlint (or >>jg -superlint superlint.tcl )

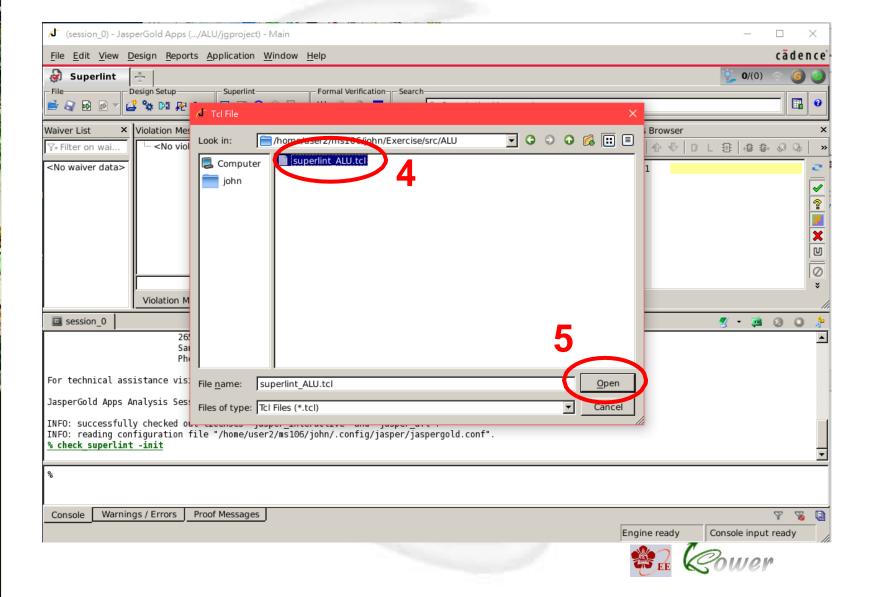


# Import Rule(1/2)

File -> Tcl Scripts -> Source



# Import Rule(2/2)







# Import Design (1/4)

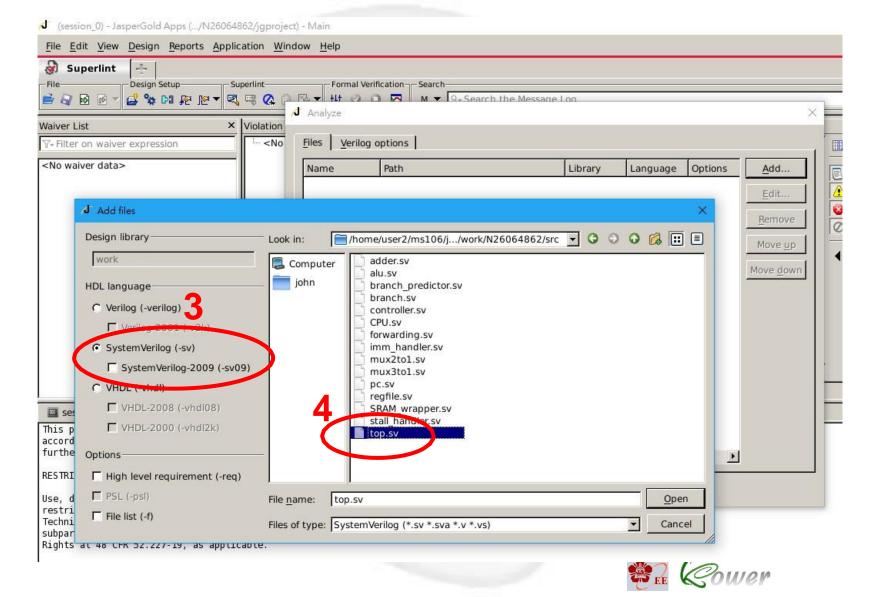
session_0) - JasperGold Apps (/N26064862/jgproject) - Main
<u>File Edit View Design Reports Application Window Help</u>
Surerlint -
File Design Salvo Superlint Formal Verification Search
E Q E V D D P P V Q R C R V HI V O N V R Search the Message Log
Waiver List   Violation Messages View
No waiver data>  No violation check extracted>
Violation Messages View Automatic Formal Properties
session_0
This product includes software developed by others and redistributed according to license agreement. See doc/third_party_readme.txt for further details.



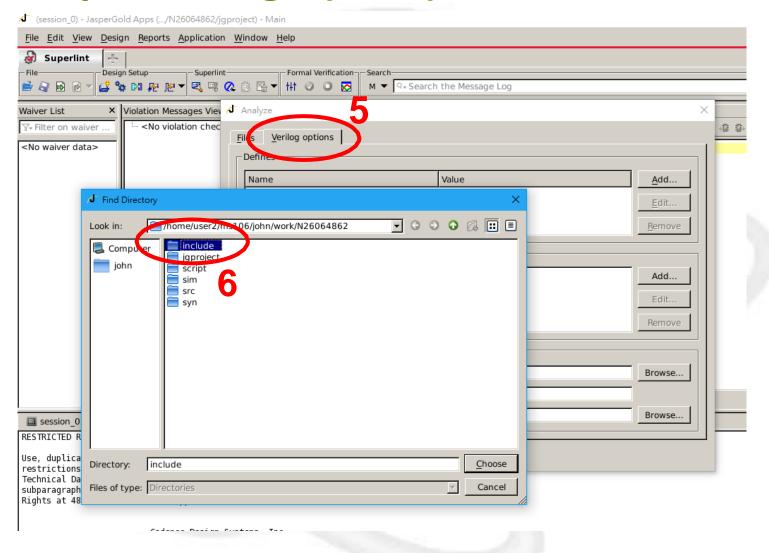
# Import Design (2/4)

(sess	d (session_0) - JasperGold Apps (/N26064862/jgproject) - Main					
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	C SystemVerilog (-sv)					
	☐ SystemVerilog-2009 (-sv09)					
	C VHDL (-vhdl)					
ses	□ VHDL-2008 (-vhdl08)					
This p	☐ VHDL-2000 (-vhdl2k)					
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restri Techni	☐ File list (-f)	Files of type: Verilog (*.v)   ▼ Cancel				
subpar Rights	at 48 CFK 52.227-19, as applicabl					
-		Comon				

# Import Design (3/4)



# Import Design (4/4)

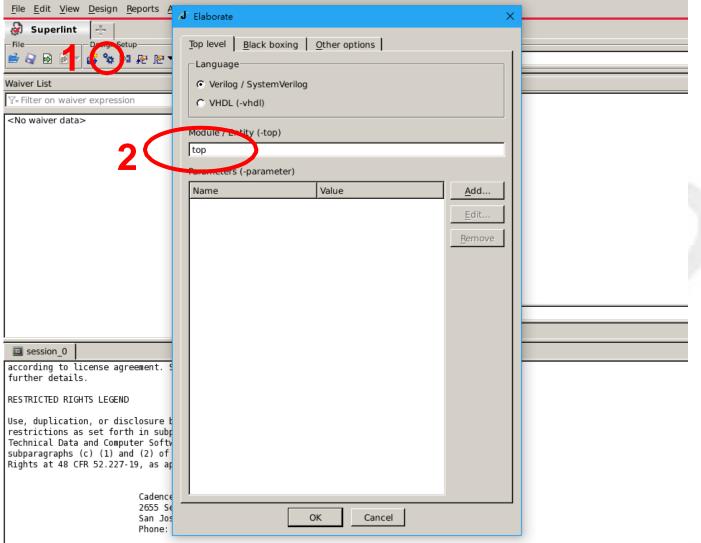




# LPHPLMB VLSI Design LAB

# Elaborate (1/2)

(session\_0) - JasperGold Apps (.../N26064862/jgproject) - Main



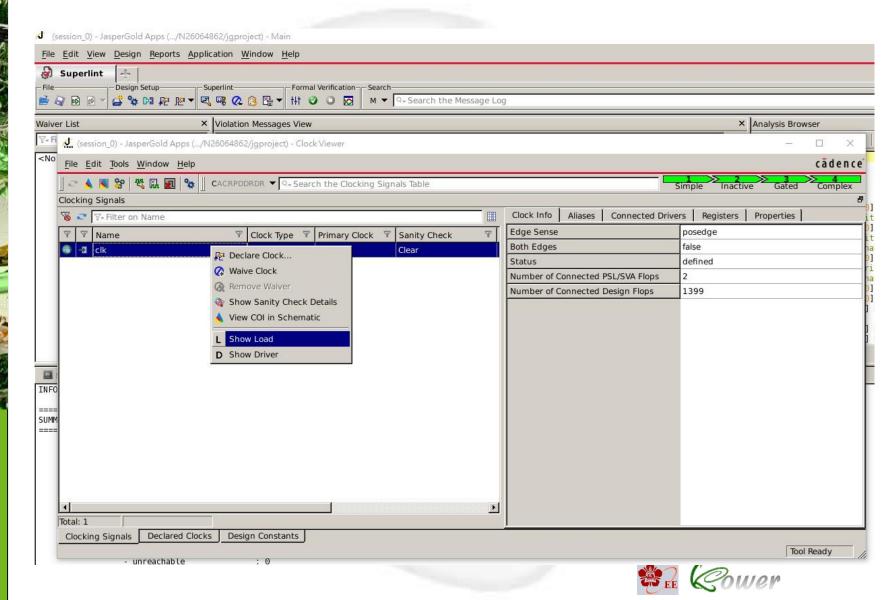




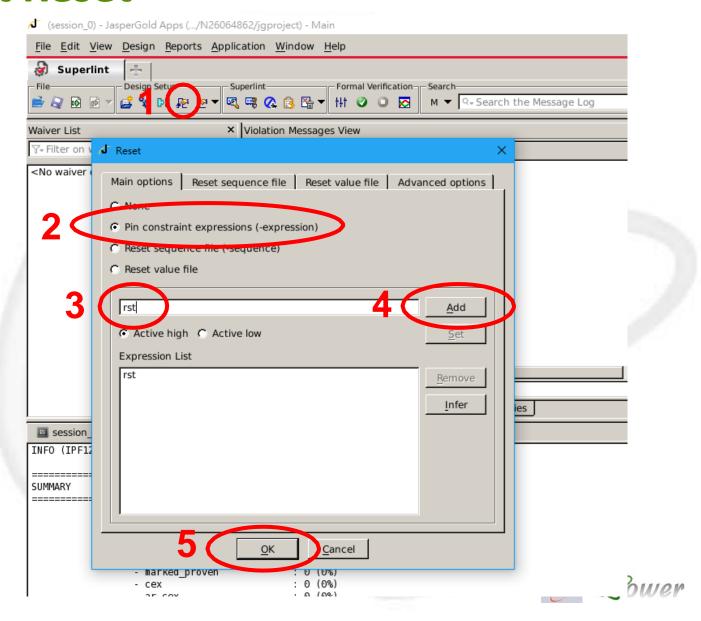
# Elaborate (2/2)

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	Modulus operators if output exceeds (-bbox_mod) 0	
	Power operators if output exceeds (-bbox_pow) 0	
	Modules (-bbox m)	
	Add	
	<u>Z</u> uu	
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session_0	Instances (-bbox i)	
according to license agreement. Set further details.	Add	
Ministry (Add Life State		
RESTRICTED RIGHTS LEGEND		
Use, duplication, or disclosure by restrictions as set forth in subpa		
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subparagraphs (c) (1) and (2) of C Rights at 48 CFR 52.227-19, as app		
Cadence (	<b>5</b>	
2655 See' San Jose		_
Phone: 40	OK Cincel	0
For technical assistance visit http	o://support.cadence.com.	501

#### **Set Clock**

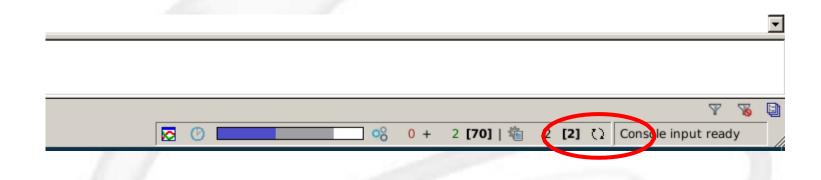


#### **Set Reset**





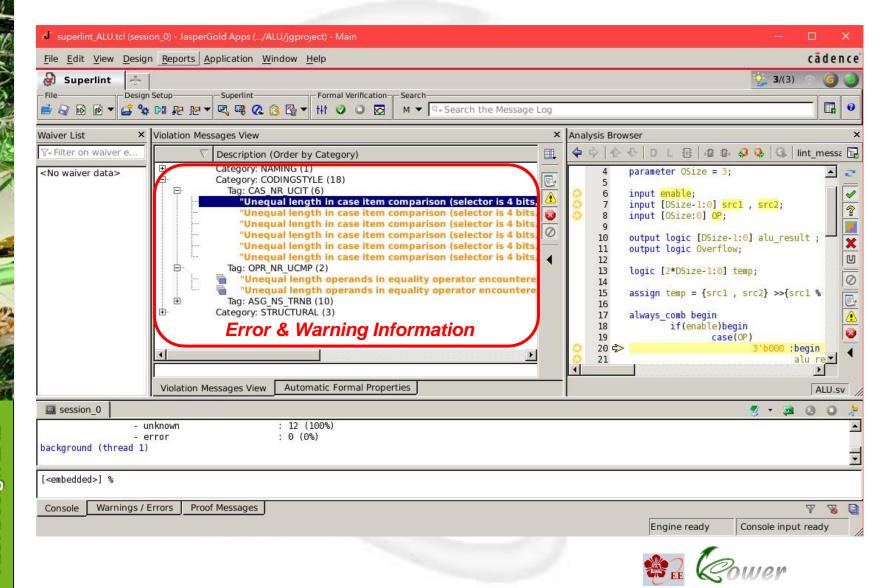
### **Busy state**



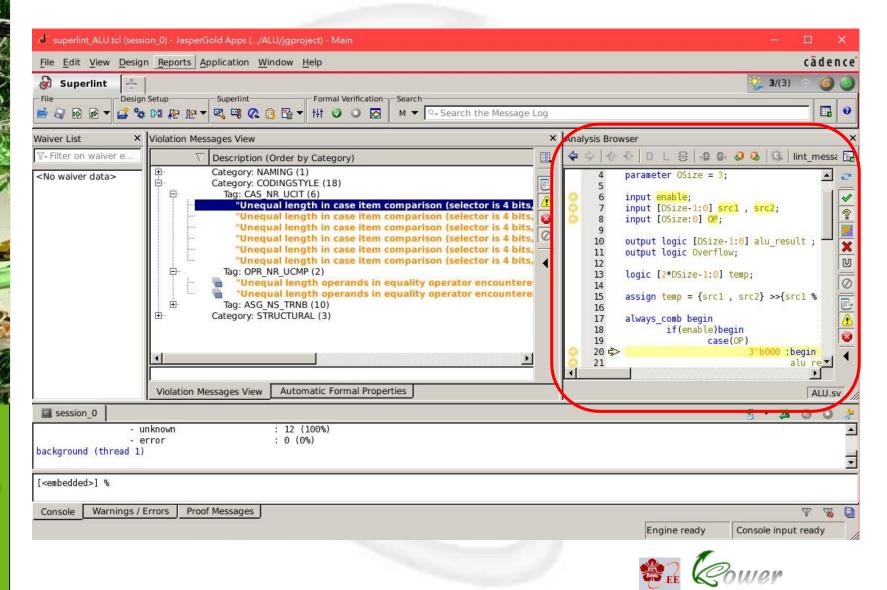




# Error & Warning Information(1/3)



# **Error & Warning Information(2/3)**





# Error & Warning Information(3/3)

#### > Let's check >> jaspergold\_superlint\_reference.pdf

#### CAS NR UCIT

Short Message: Unequal length in case item comparison (selector is %d bits, case tag expression is %d bits) in module/design-unit %s.

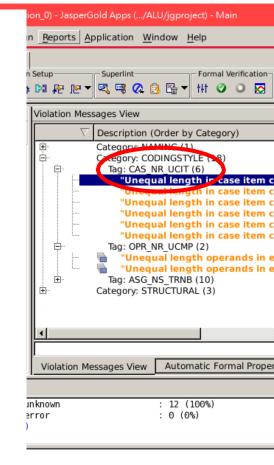
Severity	Warning
Description	A case tag expression was found to have a width, which was inconsistent with the case selector. This can result in unexpected comparison results in simulation and/or synthesis. It is recommended that all case tag expressions are specified with the same width as the case selector.

The following code illustrates the occurrence of CAS NR UCIT.

```
module uneq_length_case_item (a, b, c, sel, out1);
input a;
input b;
input c;
input [3:0] sel;
output out1;
reg out1;
always @(a or b or c or sel)
```

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Product Version 2018.06







## Warning example

- ✓ OPR\_NR\_UCMP
- √ ASG\_MS\_RPAD
- ✓ OPR\_NR\_UEOP
- √ ASG\_NS\_TRNB
- ➤ Let's check superlint.tcl





# Thank you for Vour attention!!

