Synthesis tool : Design Compiler

Advisor: Lih-Yih Chiou

Speaker: Katen

Date: 2021/09/22

EE

LPHPLAB
VLSI Design LAB

Outline

- Introduction
- Synthesis flow
- Appendix

Introduction

Introduction

- Three levels of design and the information that we can get
  - RTL Design & Simulation
    - Logical operations on signals
  - Synthesis
    - Wiring (without placing and routing information), timing
  - Layout
    - Place and route, timing(clock tree synthesis)
- We transform the RTL code into the gate-level code, so we know how the design is implemented with those cells.
- To make the simulation more realistic, we use cells that contains timing information.

Introduction

- **Tool : Design Compiler**
  - **Company : Synopsys**
  - **Version : 2018.06**
- **Before synthesis, you need to prepare…**
  - **Your RTL code**
  - **synopsys_dc.setup**

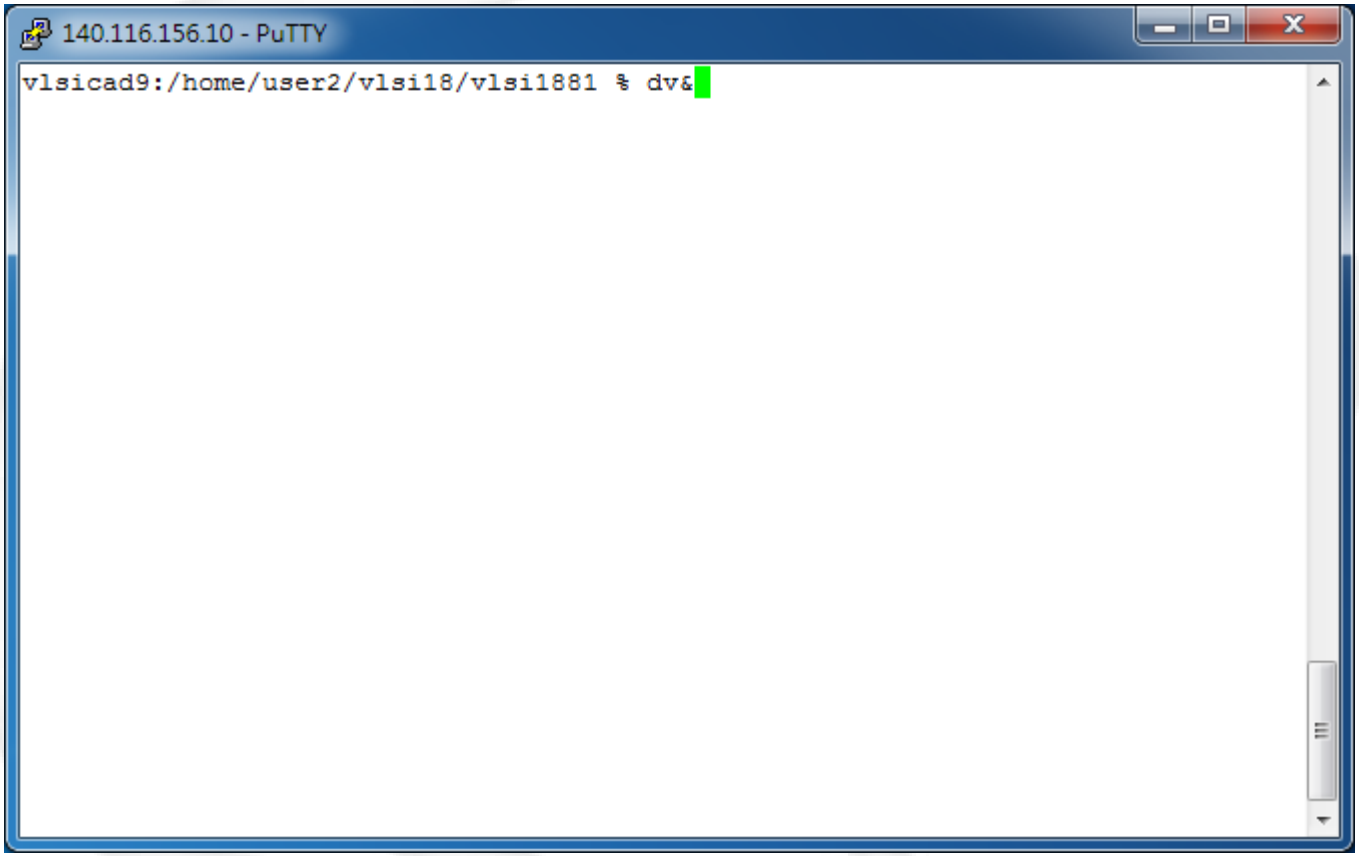
Synthesis flow

Synthesis flow

- Setup library
- Read file
- Define clock specification
- Define operating environment
- Compile
- Report & Analysis
- Save design

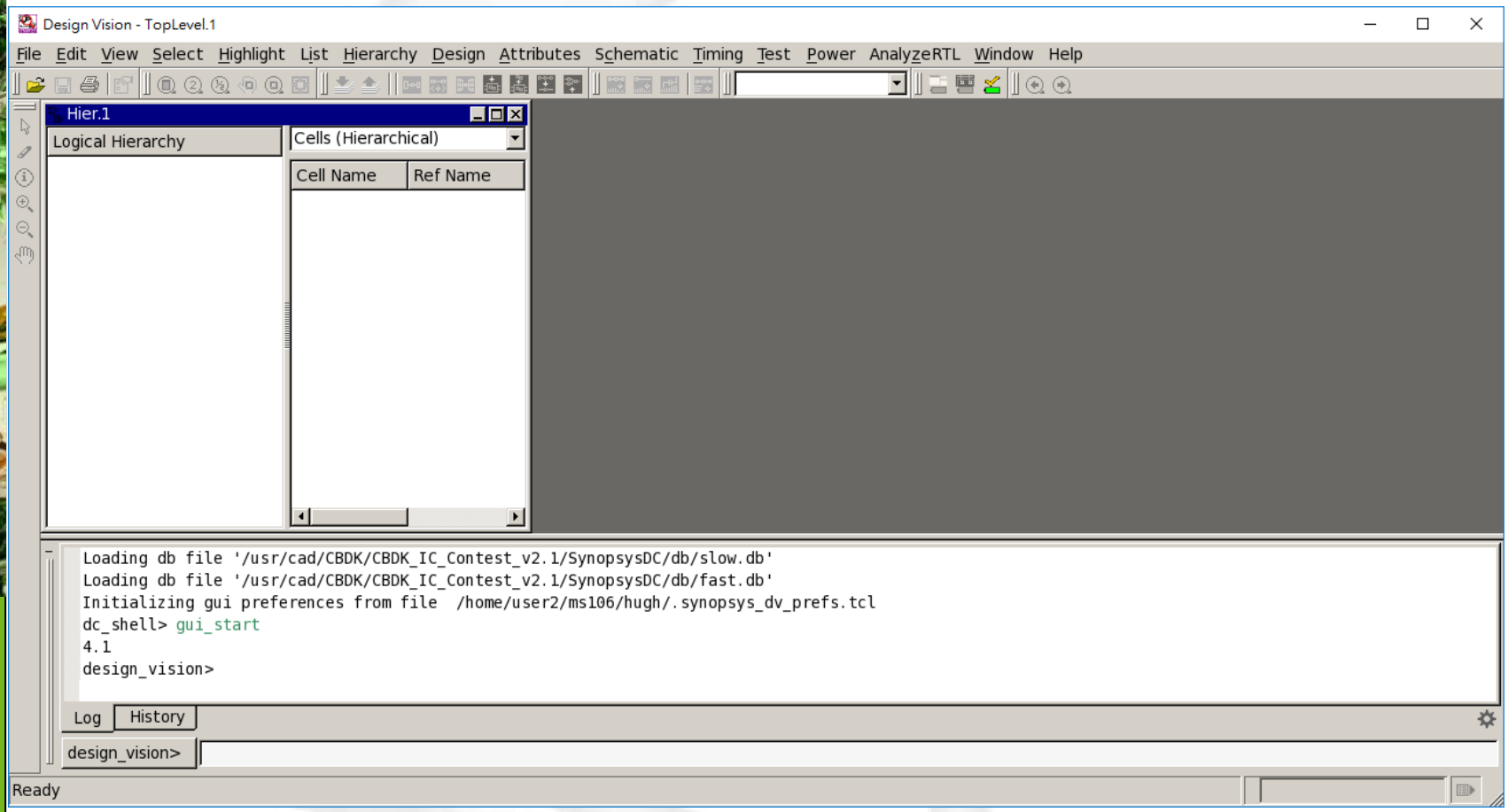
Design Compiler

- In the terminal, Enter dv.

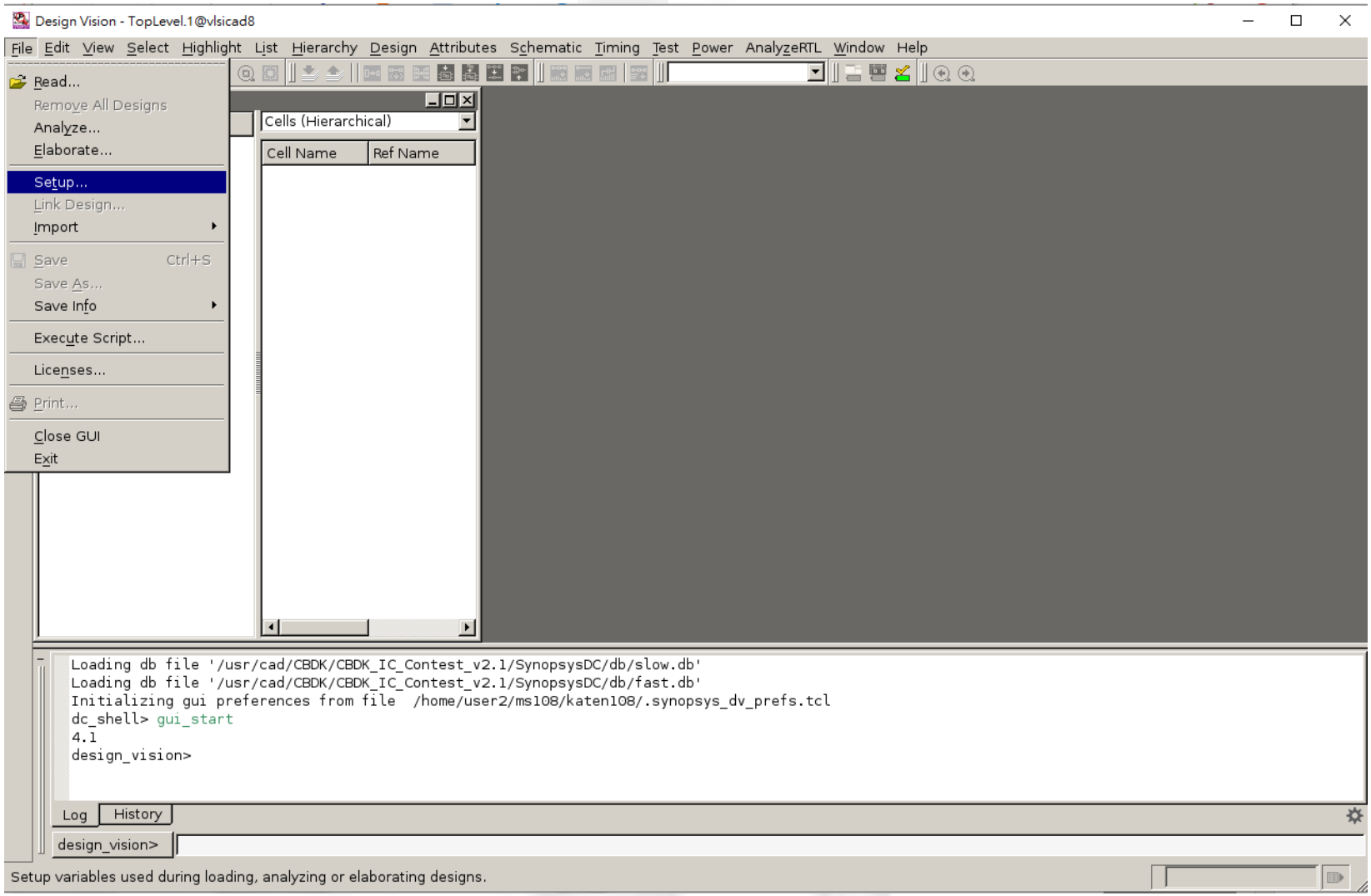


Open DC

- Check if there is any error.

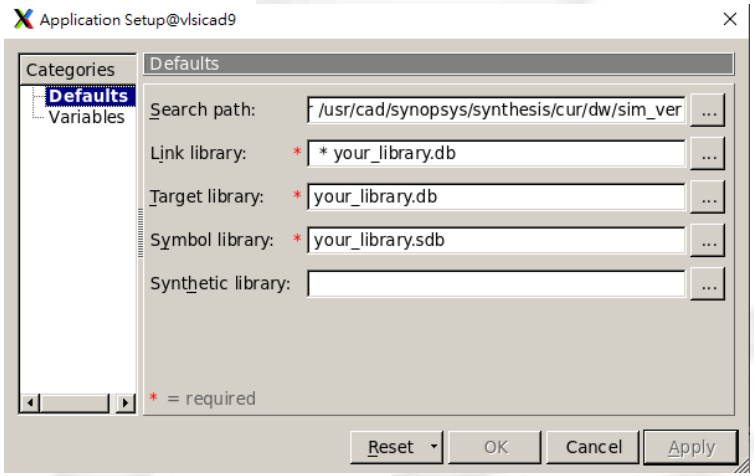


Check library

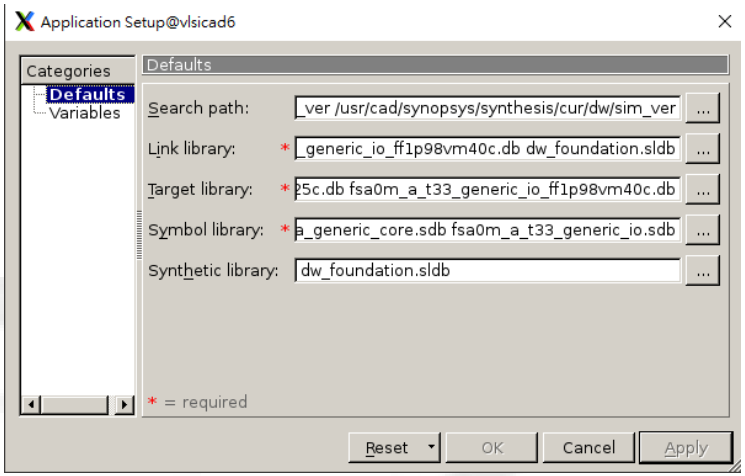


Check library

- Check whether library setup correctly



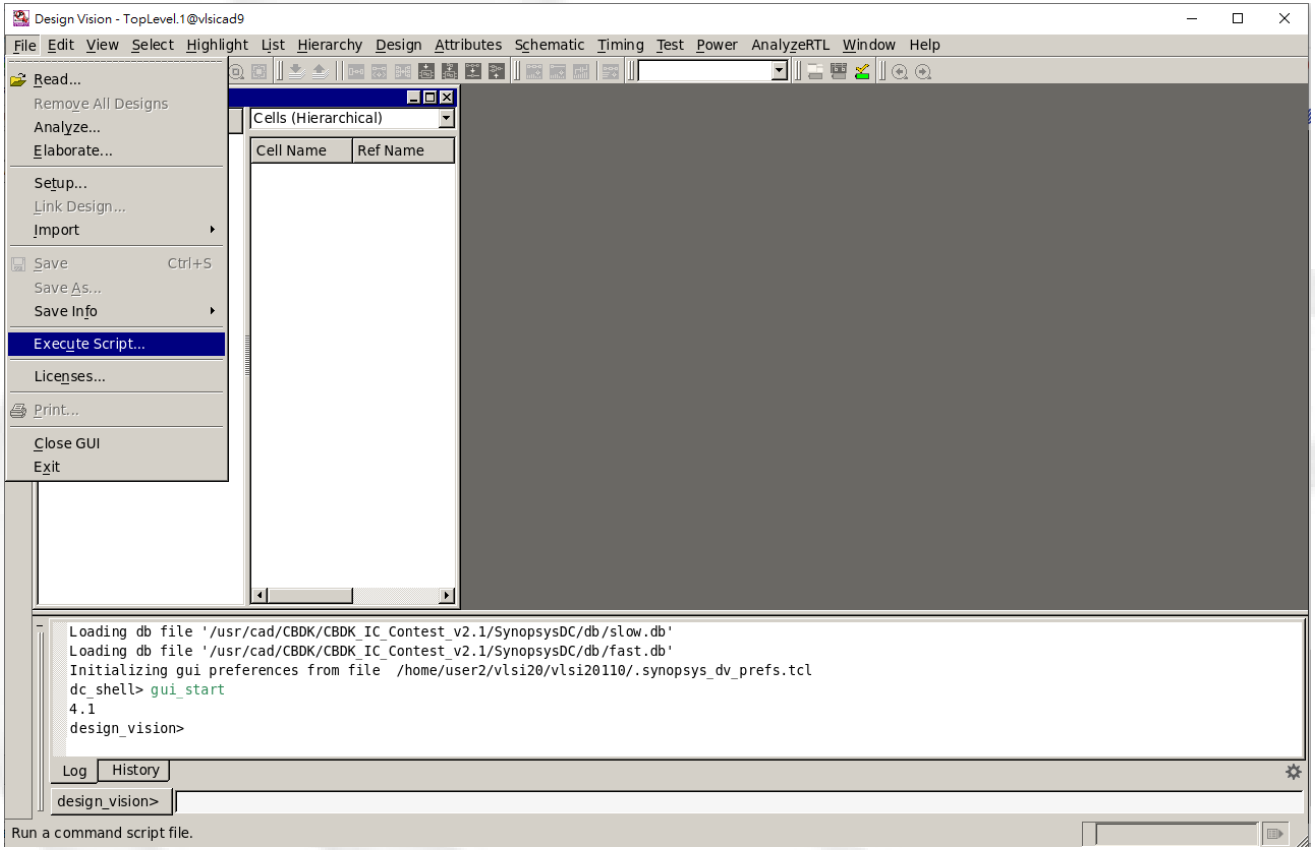
fail



success

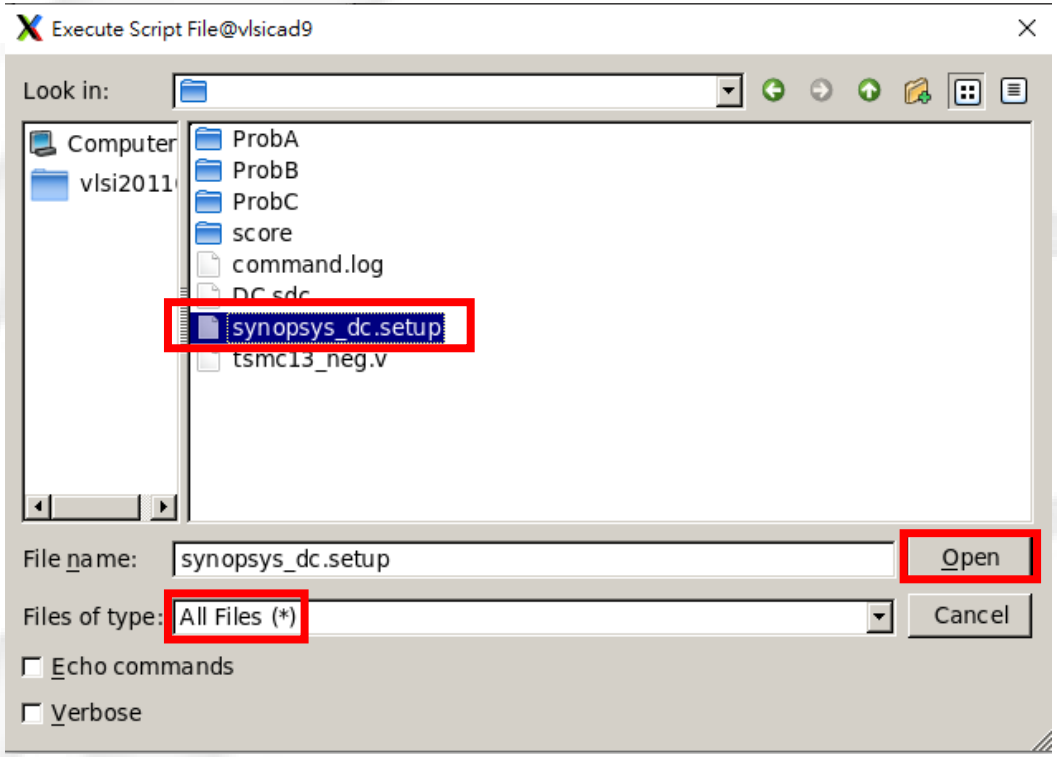
Check library

- If fail, read dc setup file



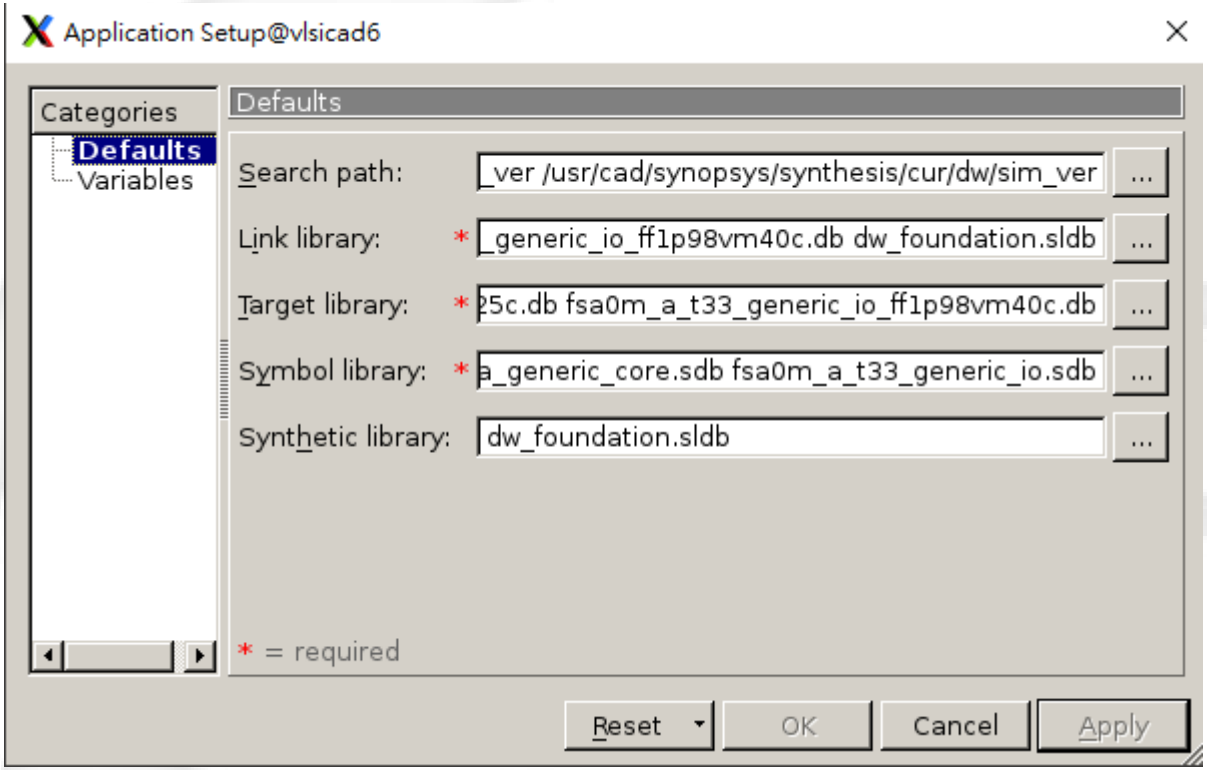
Check library

- If fail, read dc setup file



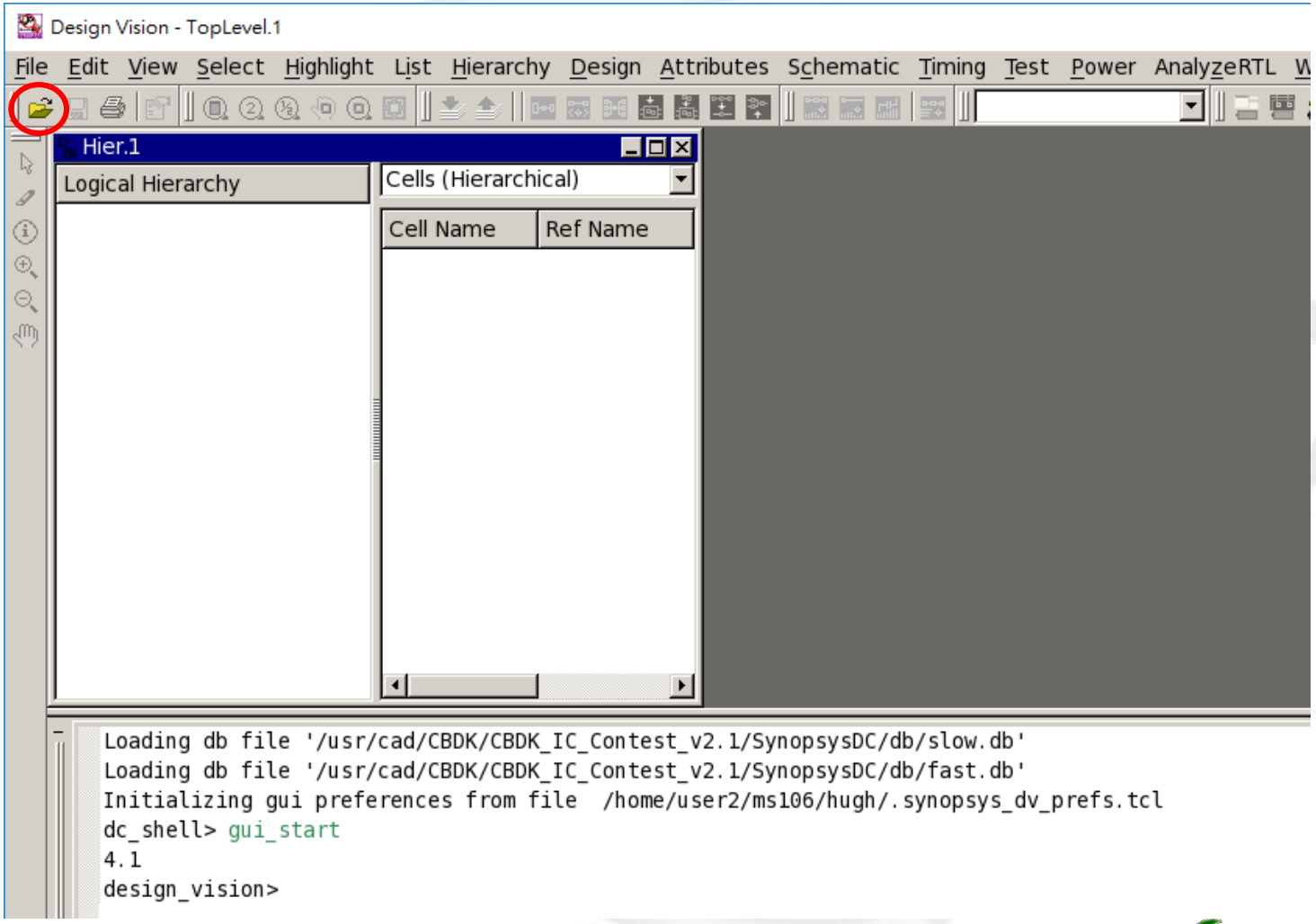
Check library

- Check library again



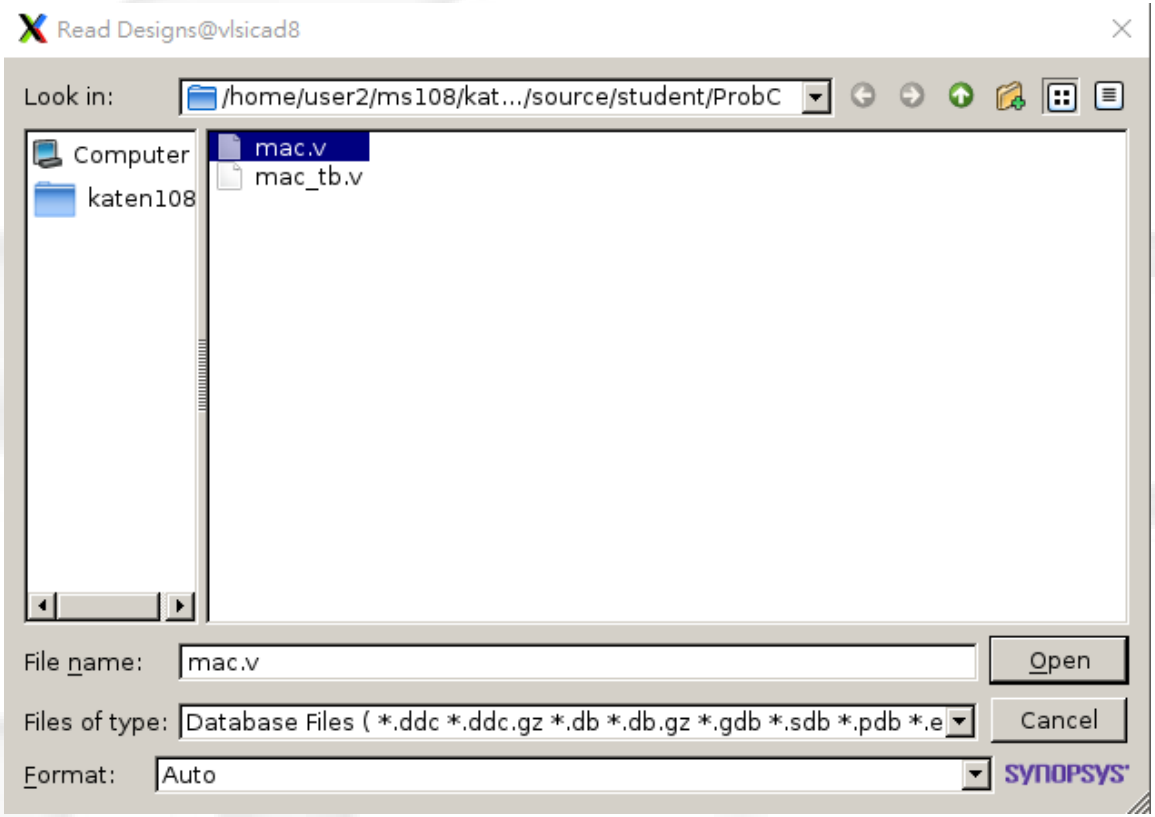
Read Files (1)

- File >> Read…



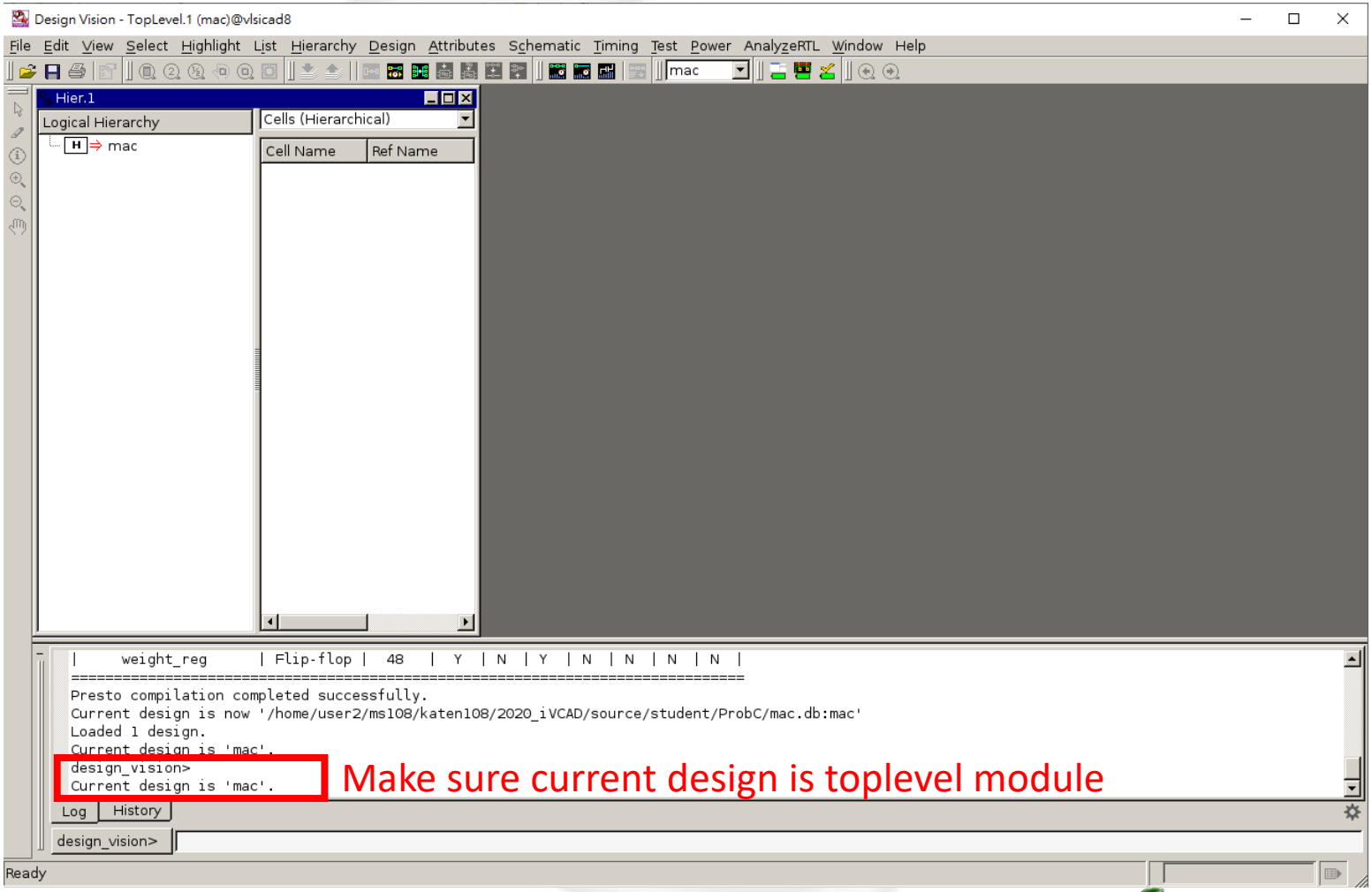
Read Files (2)

- Choose toplevel design



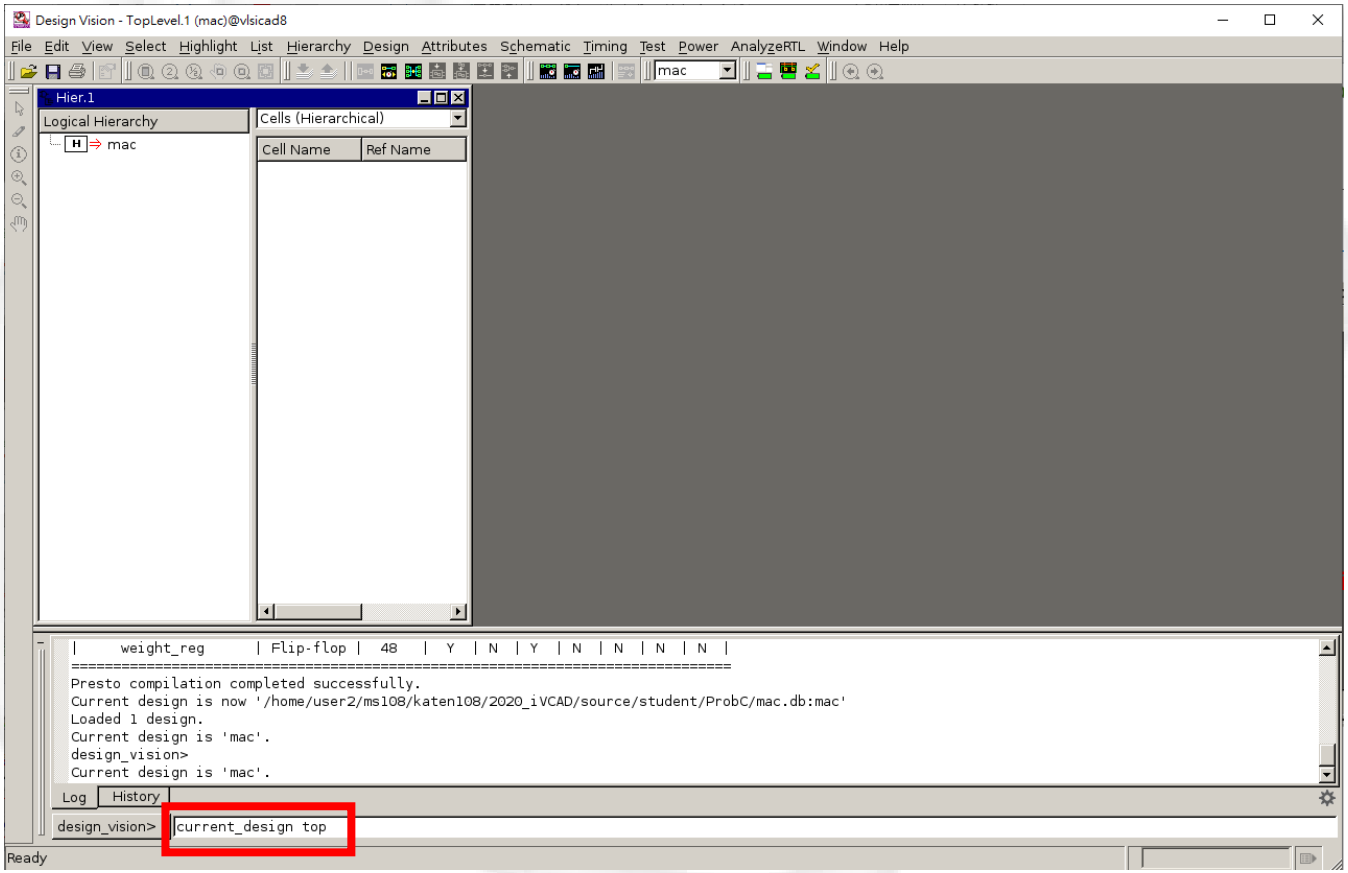
Read Files (3)

- Check if there is any error

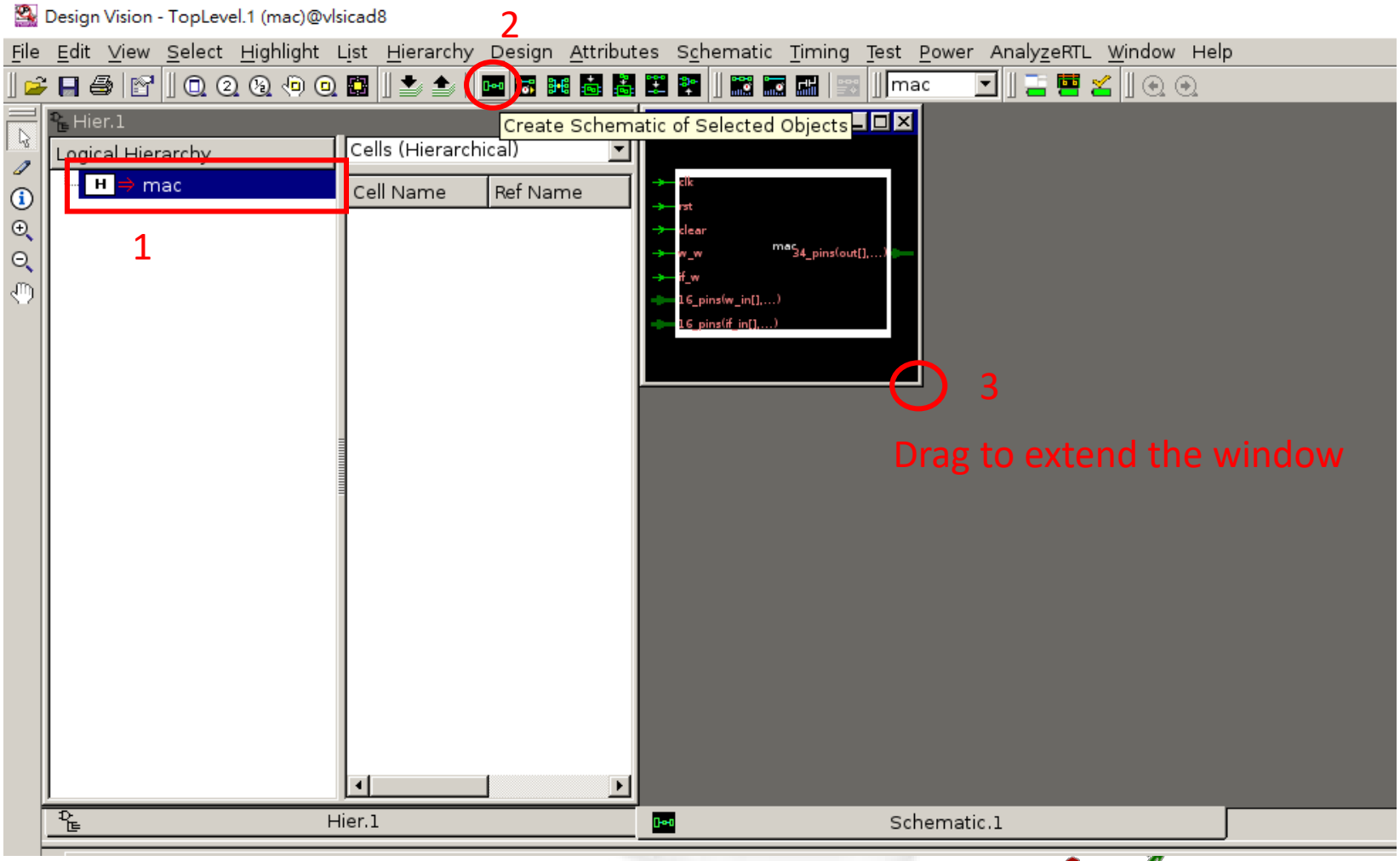


Read Files (4)

- If current design is not toplevel module , use command current_deign module_name to change current design to toplevel module

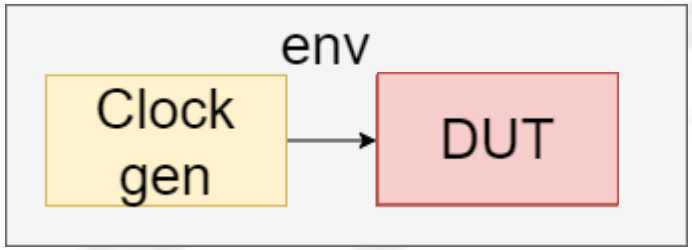


Open Schematic



What to do next ?

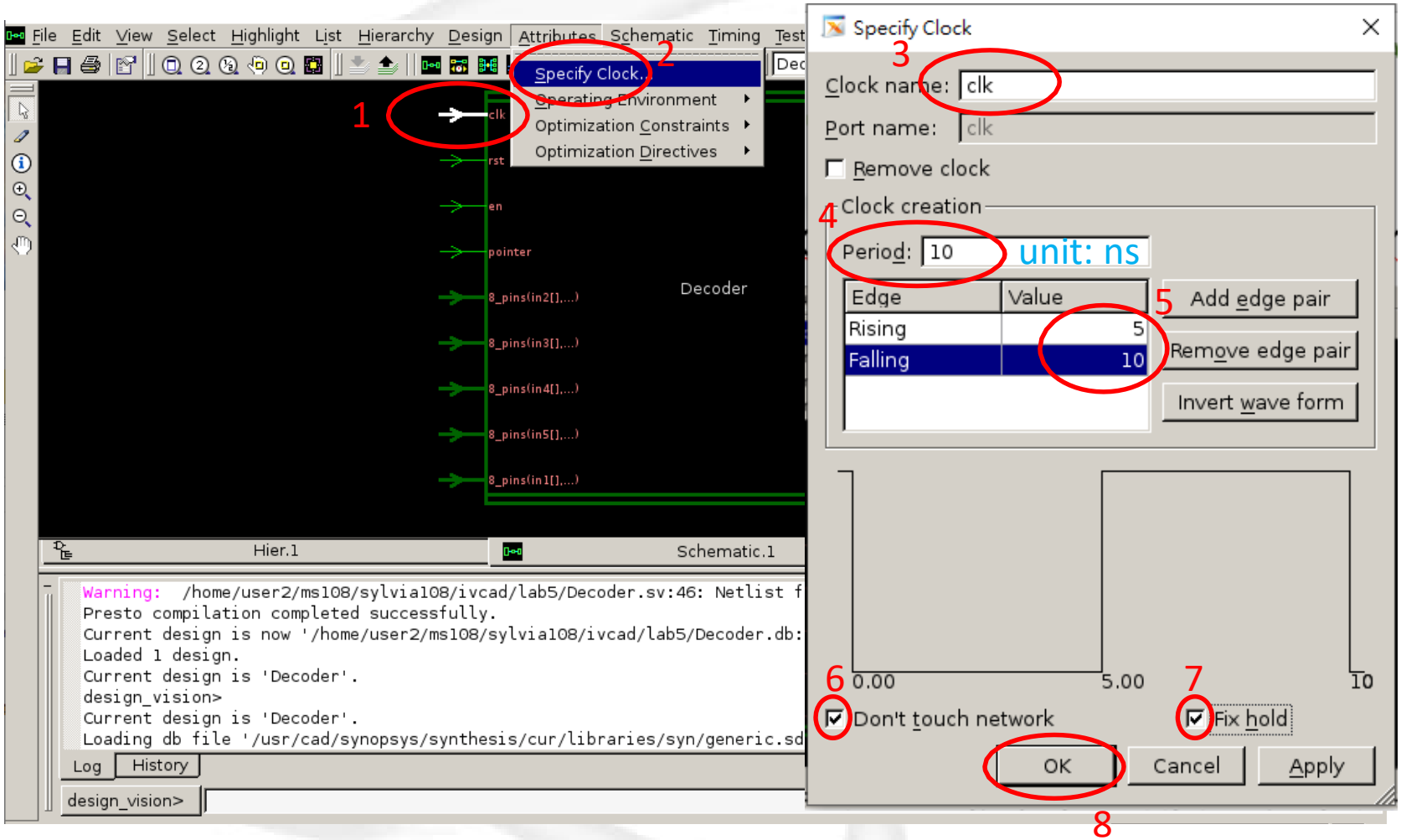
- Define Clock Specification
- Define operating environment



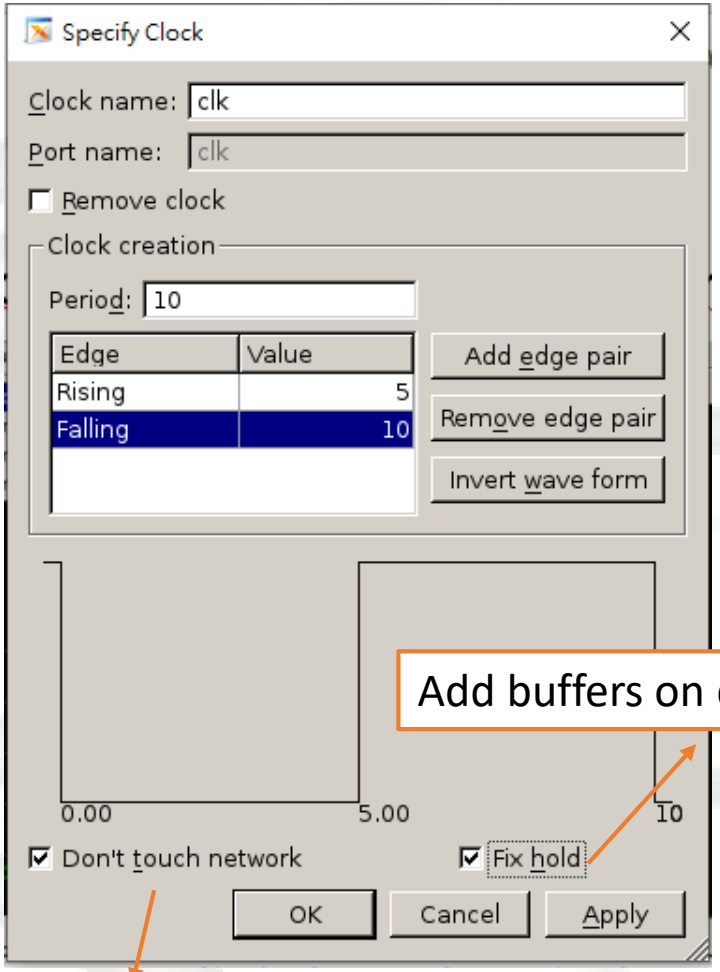
Define Clock Specification

- Period
- Waveform
- Uncertainty
  - Skew
- Latency
  - Source latency (optional)
  - Network latency
- Transition
  - Input transition (optional, not need if driving cell has set)
  - Clock transition (optional, it can merge with clock latency)

Clock Specification (1/2)



Clock Specification (2/2)



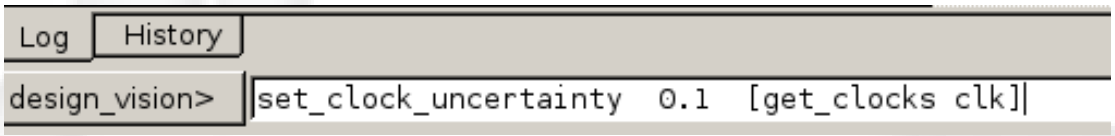
Add buffers on data path to satisfy hold time

Don’t add buffers on clock path

Why fix hold?

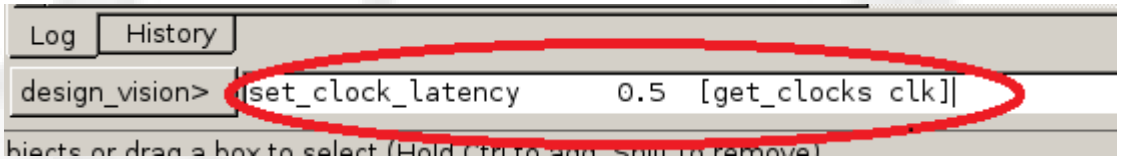
Set clock uncertainty & clock latency

- Set clock uncertainty
  - set_clock_uncertainty 0.1 [get_clocks clock_name]



What is clock uncertainty ?

- Set clock latency
  - set_clock_latency 0.5 [get_clocks clock_name]

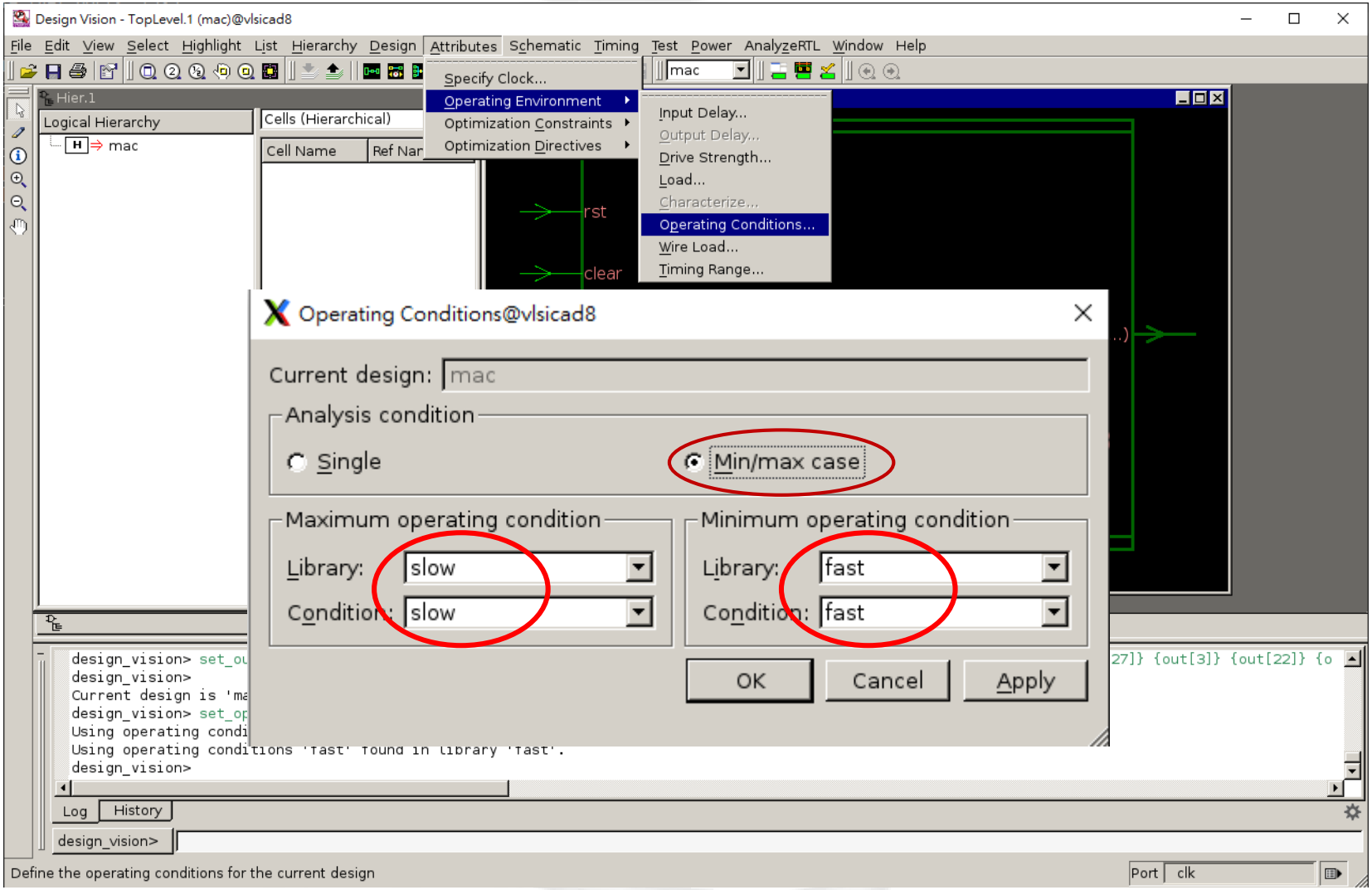


What is clock latency ?

Define operating environment

- Set operating conditions
- Set driving cell
- Set load
- Set input delay
- Set output delay
- Set wire load model

Operating Conditions



Set driving cell

- Script :
  - set_driving_cell -library tpz973gvwc -lib_cell PDIDGZ -pin {C} [all_inputs]

IO library, usually use slow library

Input pad you used

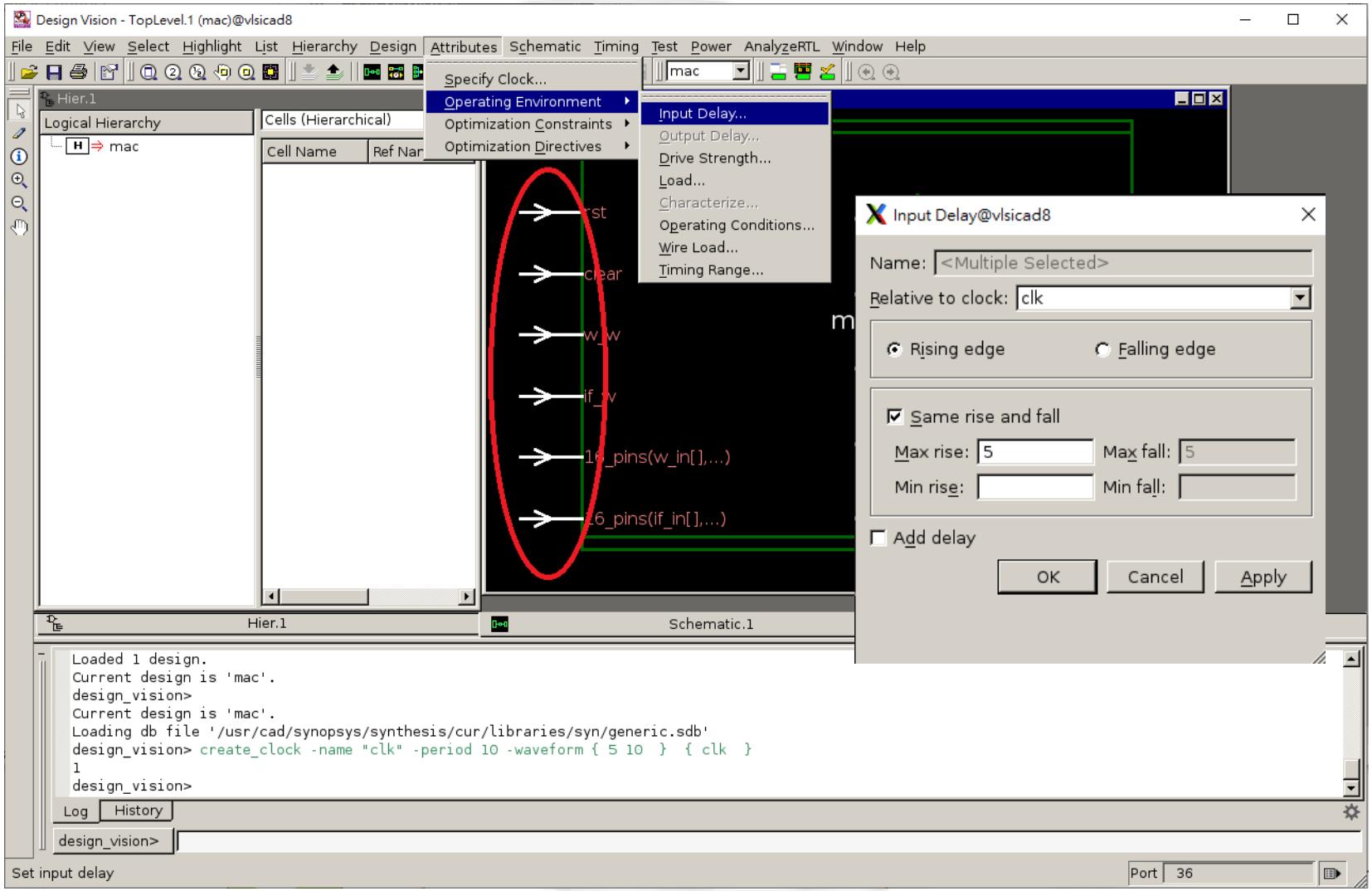
Port of input pad connect to top module

- You need to set driving cell, only when you synthesize top level module

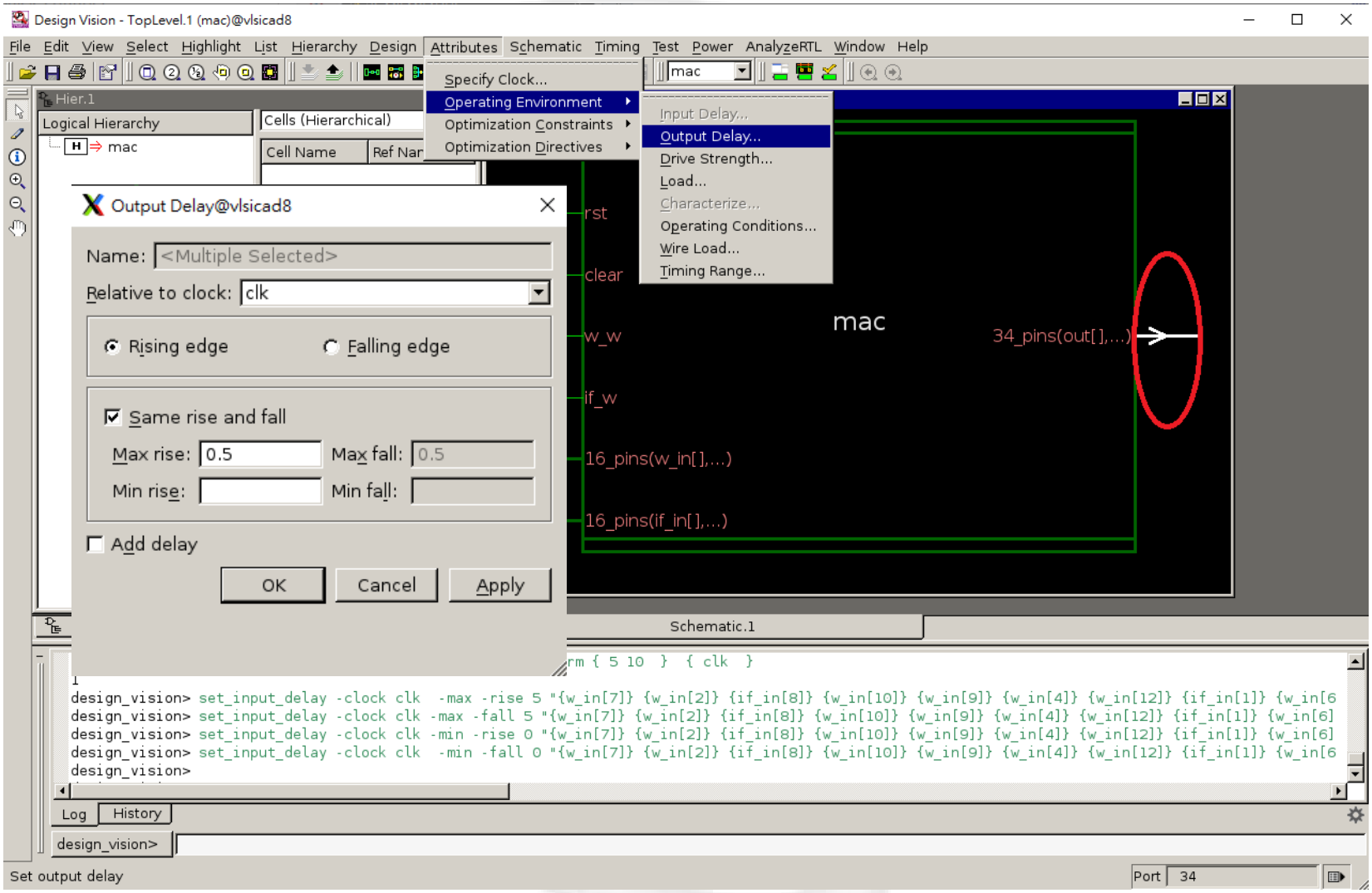
Set load

- Script :
  - set_load 0.05 [all_outputs]
  - set_load [load_of “tpz973gvwc/PDO16CDG/I”] [all_outputs]
- Value :
  - TSRI testing equipment : 40 pF
  - PCB : 10 pF
  - Top module to IO_pad : 0.05 pF
  - Load between modules : 0.002 pF

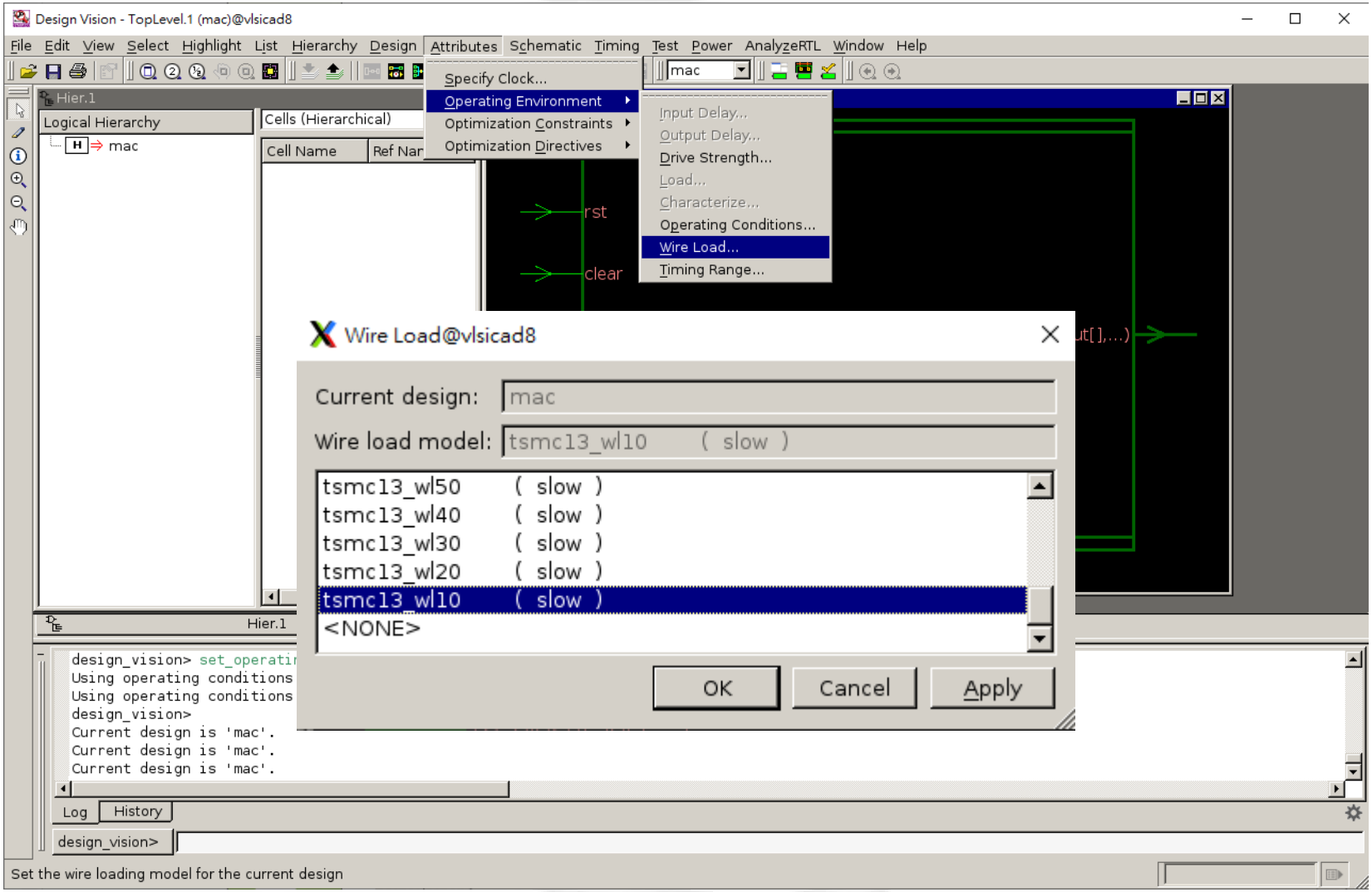
Input delay


Design Vision - TopLevel.1 (mac)@vlsicad8
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
Specify Clock...
Operating Environment
Optimization Constraints
Optimization Directives
Input Delay...
Output Delay...
Drive Strength...
Load...
Characterize...
Operating Conditions...
Wire Load...
Timing Range...
Logical Hierarchy
mac
Cells (Hierarchical)
Cell Name
Input Delay@vlsicad8
Name: <Multiple Selected>
Relative to clock: clk
Rising edge
Falling edge
Same rise and fall
Max rise: 5
Max fall: 5
Min rise:
Min fall:
Add delay
OK
Cancel
Apply
Hier.1
Schematic.1
Loaded 1 design.
Current design is 'mac'.
design_vision>
Current design is 'mac'.
Loading db file '/usr/cad/synopsys/synthesis/cur/libraries/syn/generic.sdb'
design_vision> create_clock -name "clk" -period 10 -waveform { 5 10 } { clk }
1
design_vision>
Log
History
design_vision>
Set input delay
Port 36

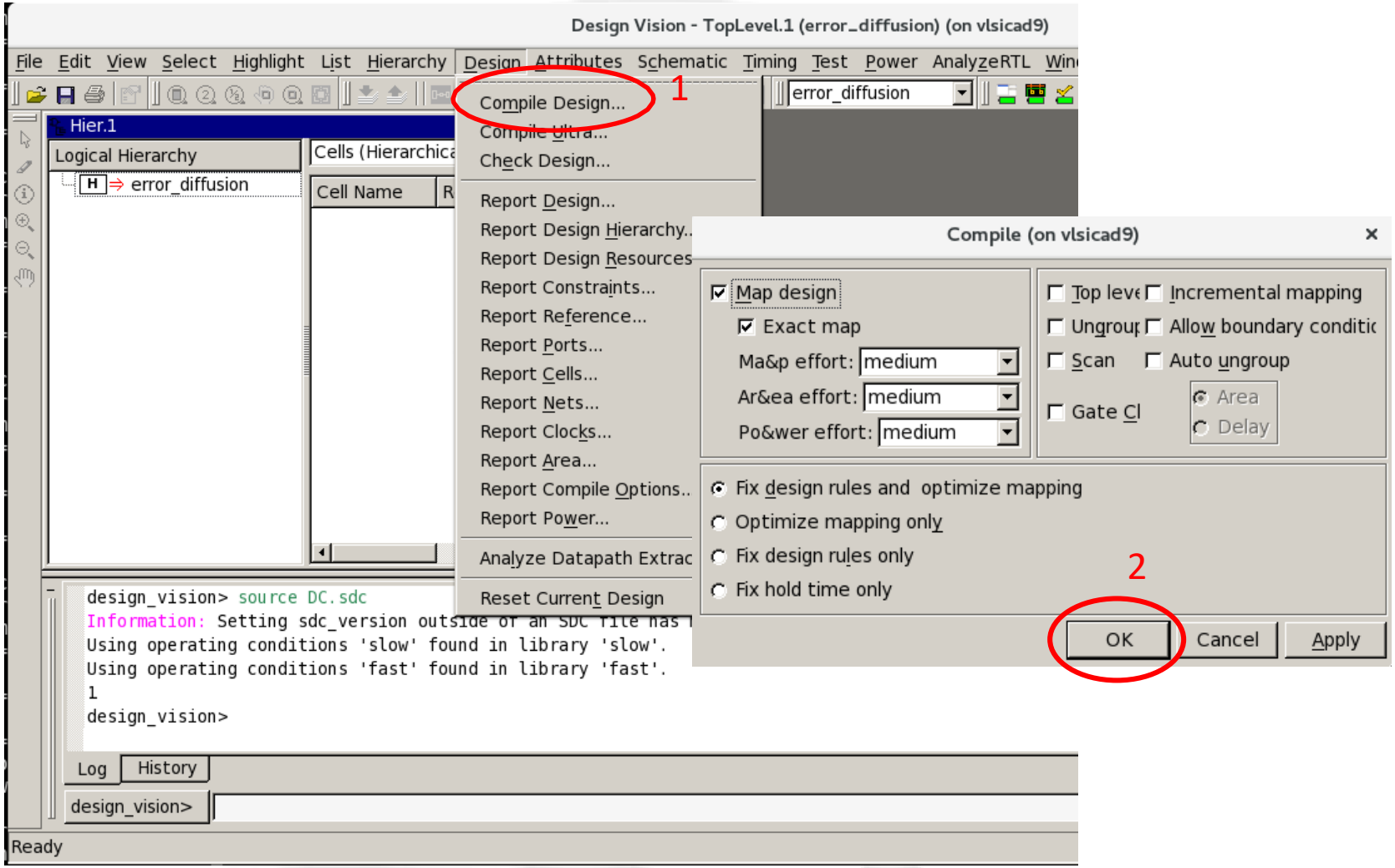
Output delay



Wire load

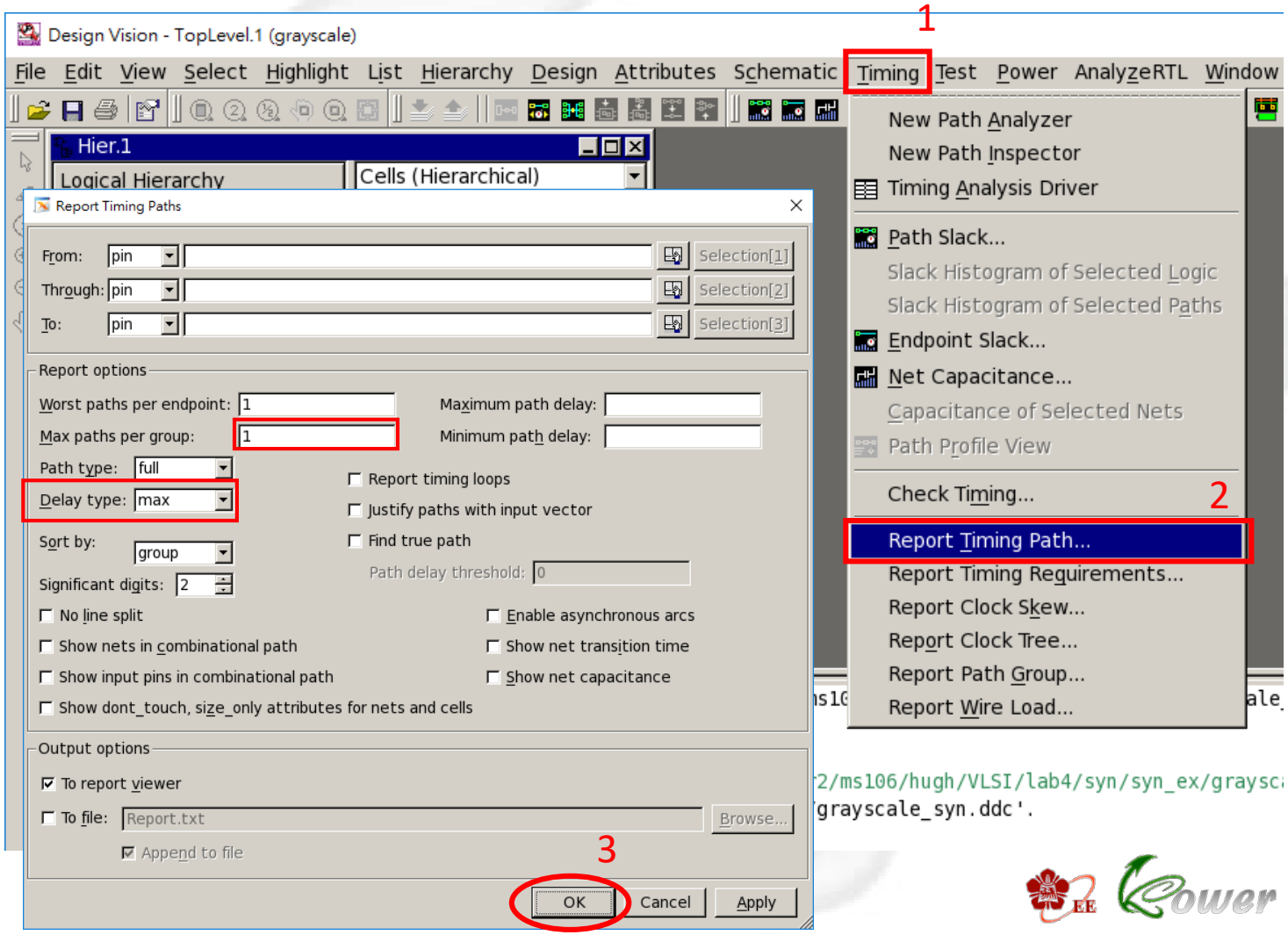

Design Vision - TopLevel.1 (mac)@vlsicad8
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
Specify Clock...
Operating Environment
Optimization Constraints
Optimization Directives
Input Delay...
Output Delay...
Drive Strength...
Load...
Characterize...
Operating Conditions...
Wire Load...
Timing Range...
Logical Hierarchy
mac
Cells (Hierarchical)
Cell Name
rst
clear
Wire Load@vlsicad8
Current design: mac
Wire load model: tsmc13_wl10 (slow)
tsmc13_wl50 (slow)
tsmc13_wl40 (slow)
tsmc13_wl30 (slow)
tsmc13_wl20 (slow)
tsmc13_wl10 (slow)
<NONE>
OK
Cancel
Apply
design_vision> set_operati
Using operating conditions
Using operating conditions
design_vision>
Current design is 'mac'.
Current design is 'mac'.
Current design is 'mac'.
Log
History
design_vision>
Set the wire loading model for the current design

Compile Design



Report Timing (1/2)

- Command: report_timing



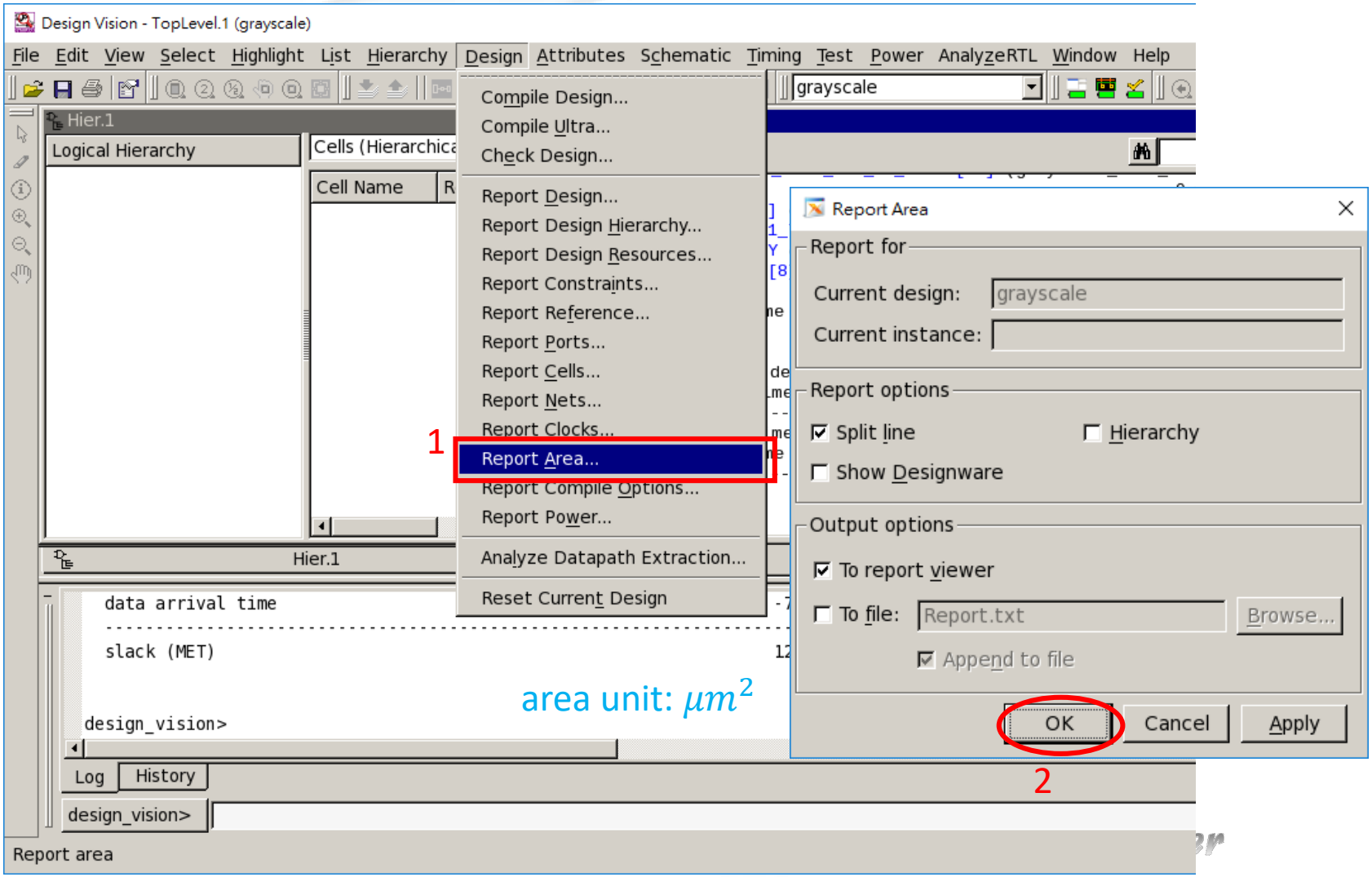
Report Timing (2/2)

- Slack must no less than 0, or it will lead to timing violation

```
Point                                                    Incr       Path
-------------------------------------------------------------------------
clock clk (rise edge)                                    0.00       0.00
clock network delay (ideal)                              0.50       0.50
input external delay                                     5.00       5.50 f
d[1] (in)                                                0.06       5.56 f
U78/Y (XOR2X1)                                           0.31       5.87 r
add_0_root_add_0_root_add_31_2/A[2] (grayscale_DW01_add_0)
                                                         0.00       5.87 r
add_0_root_add_0_root_add_31_2/U8/Y (OA21X4)             0.22       6.09 r
add_0_root_add_0_root_add_31_2/U9/Y (AO21XL)             0.47       6.56 r
add_0_root_add_0_root_add_31_2/U3/Y (NOR2X1)             0.21       6.77 f
add_0_root_add_0_root_add_31_2/U2/Y (OR2X1)              0.33       7.10 f
add_0_root_add_0_root_add_31_2/U12/Y (OAI2BB1X2)         0.13       7.23 r
add_0_root_add_0_root_add_31_2/U1_4/CO (ADDFHX2)         0.21       7.44 r
add_0_root_add_0_root_add_31_2/U1_5/CO (ADDFHX2)         0.22       7.66 r
add_0_root_add_0_root_add_31_2/U1_6/CO (ADDFHX4)         0.22       7.88 r
add_0_root_add_0_root_add_31_2/U4/Y (XOR2X1)             0.24       8.12 r
add_0_root_add_0_root_add_31_2/U1/Y (XOR2X2)             0.31       8.43 f
add_0_root_add_0_root_add_31_2/SUM[7] (grayscale_DW01_add_0)
                                                         0.00       8.43 f
add_39/A[2] (grayscale_DW01_inc_0)                       0.00       8.43 f
add_39/U1_1_2/CO (ADDHX1)                                0.34       8.77 f
add_39/U3/Y (AND2X2)                                     0.28       9.06 f
add_39/U6/Y (AND2X4)                                     0.20       9.26 f
add_39/U2/Y (AND2X2)                                     0.25       9.50 f
add_39/U13/Y (NAND2X1)                                   0.20       9.70 r
add_39/U1/Y (XOR2X2)                                     0.20       9.90 r
add_39/SUM[7] (grayscale_DW01_inc_0)                     0.00       9.90 r
U40/Y (AOI22X2)                                          0.17      10.07 f
U39/Y (OAI21X2)                                          0.15      10.22 r
q_reg[7]/D (DFFRX2)                                      0.00      10.22 r
data arrival time                                                  10.22

clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.50      10.50
clock uncertainty                                       -0.10      10.40
q_reg[7]/CK (DFFRX2)                                     0.00      10.40 r
library setup time                                      -0.18      10.22
data required time                                                 10.22
-------------------------------------------------------------------------
data required time                                                 10.22
data arrival time                                                 -10.22
-------------------------------------------------------------------------
slack (MET)                                                         0.00
```

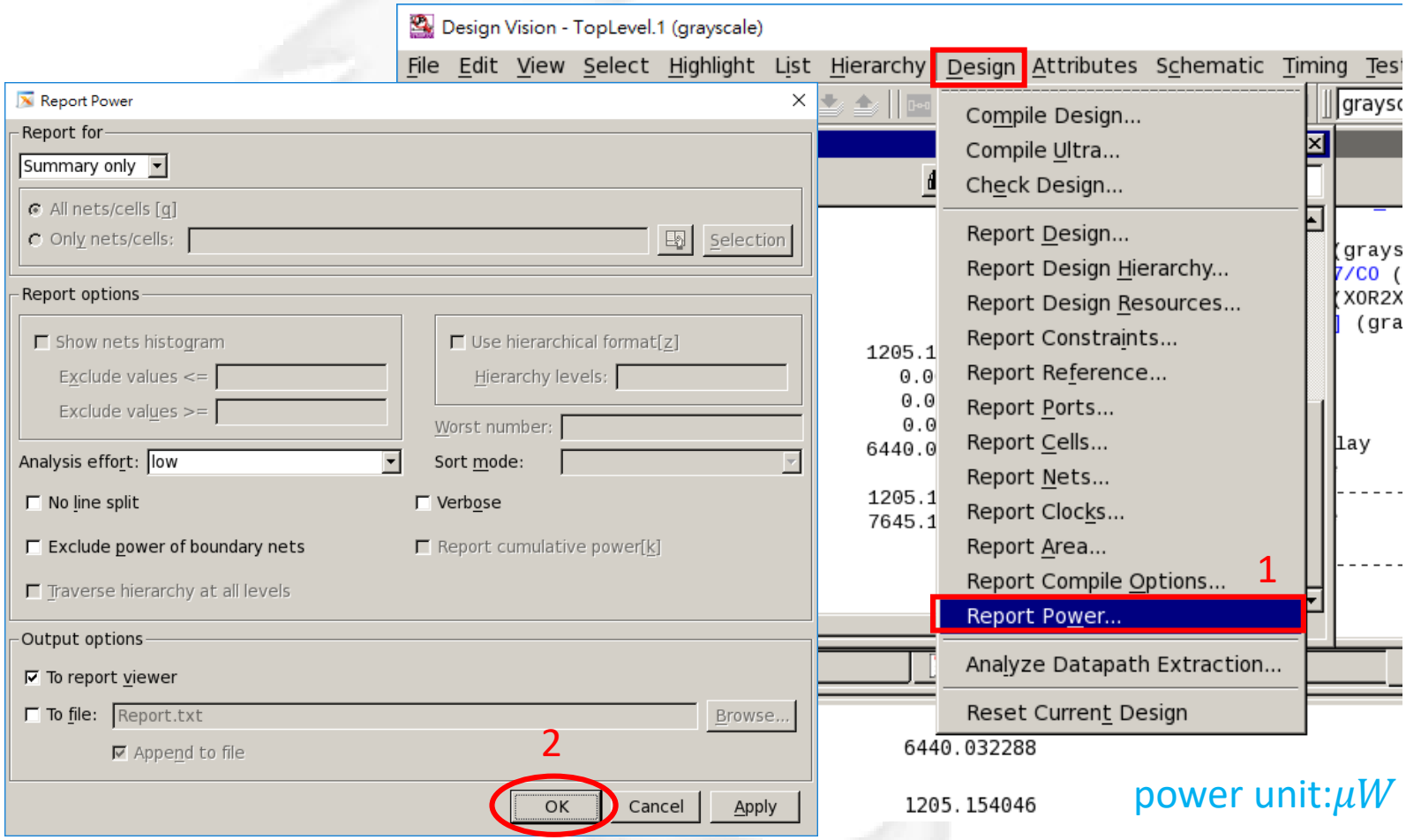
Report Area

- Command: report_area



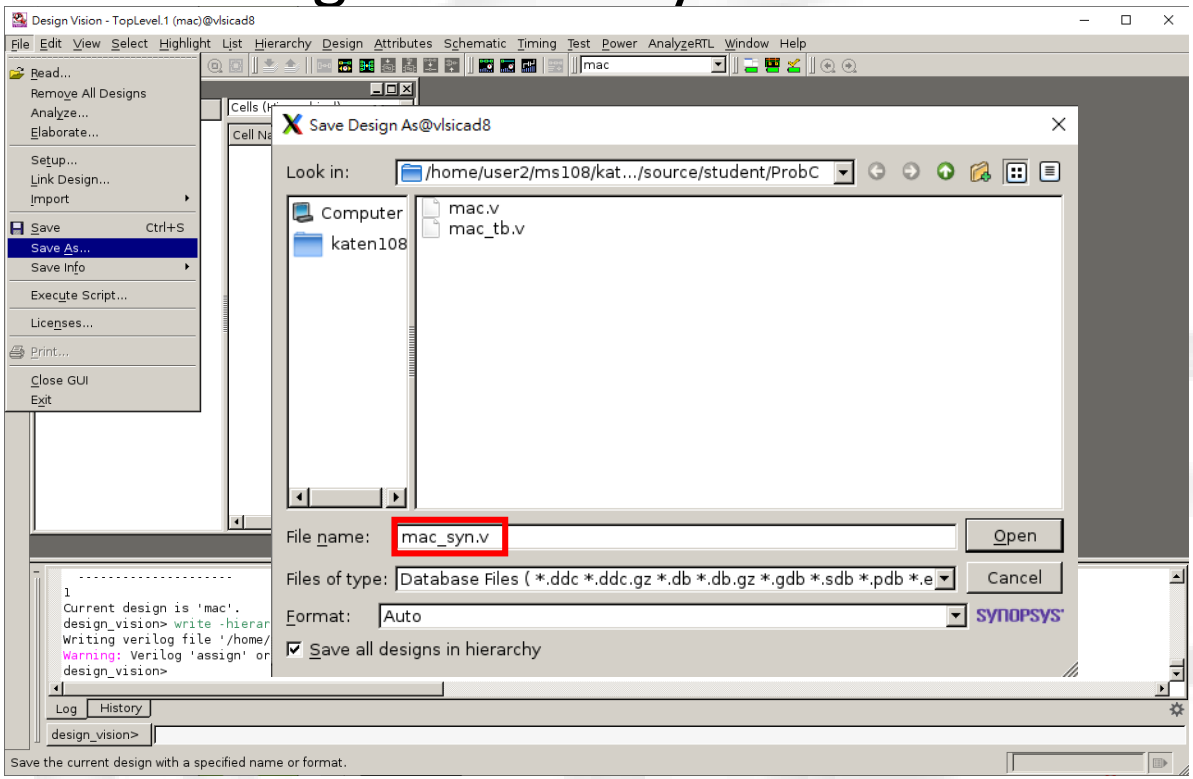
Report Power

- Command: report_power



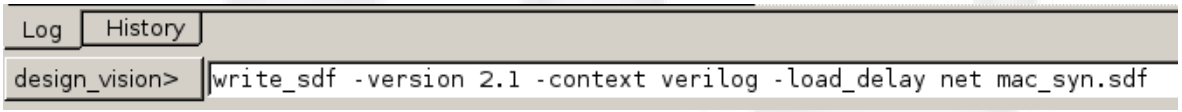
Save File

- The Verilog file after synthesis



- SDF File:

write_sdf -version 2.1 -context verilog -load_delay net filename.sdf

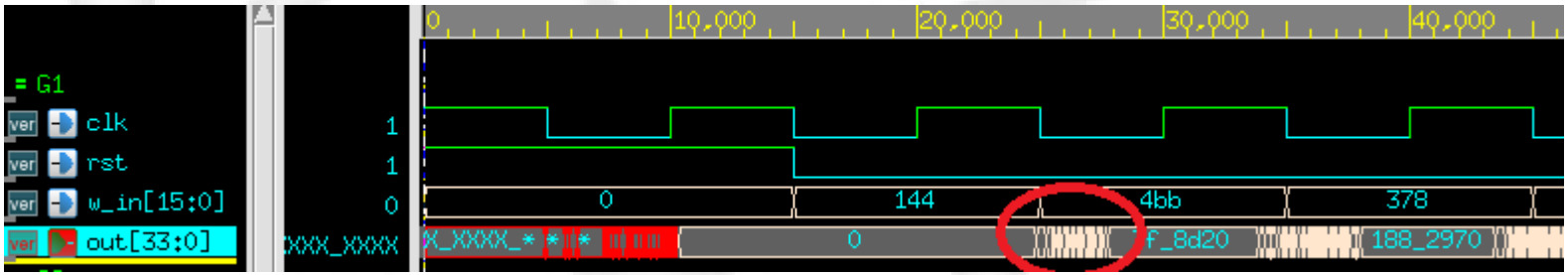


Post Simulation

- In your test bench
  - Apply delay in your design use command :
  - $sdf_annotate(“sdf_file_name”, module_instance_name)

```
mac m1(.clk(clk),.rst(rst),.clear(clear),.w_w(w_w),.w_in(w_in),.if_w(if_w),.if_in(if_in),.out(out));

`ifdef syn
initial $sdf_annotate("mac_syn.sdf",m1);
`endif
```

- Post sim waveform



Work with tcl

DC.sdc

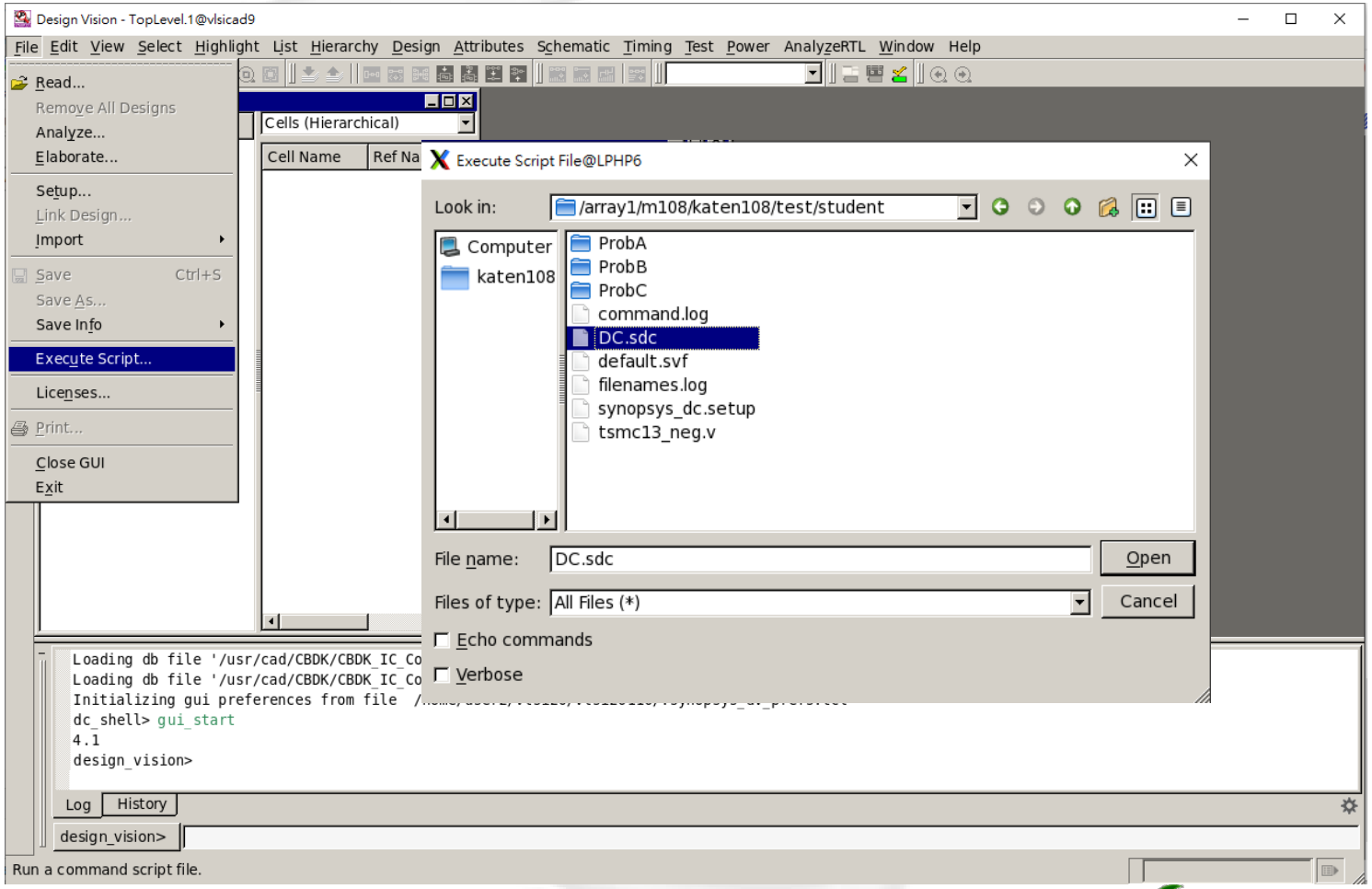
```
# operating conditions and boundary conditions #

set cycle  10.0        ;#clock period defined by designer

create_clock -period $cycle [get_ports  clk]
set_fix_hold                [get_clocks clk]
set_dont_touch_network      [get_clocks clk]
set_clock_uncertainty  0.1  [get_clocks clk]
set_clock_latency      0.5  [get_clocks clk]

set_input_delay  5      -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
set_output_delay 0.5    -clock clk [all_outputs]
set_load         0.1     [all_outputs]
set_drive        0.1     [all_inputs]

set_operating_conditions  -max slow  -min fast
set_wire_load_model -name tsmc13_wl10 -library slow

set_max_fanout 20 [all_inputs]
```

Work with tcl

- Setup library
- Read file
- Read script
- Compile
- Check report
- Save design

Work with tcl

- How to read script



Reference

- (C104) Logic Synthesis with Design Compiler training manual

Appendix

The DC Setup File

synopsys_dc.setup

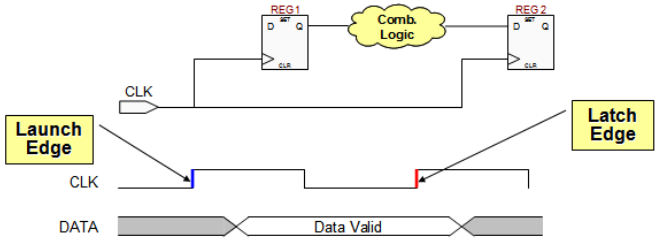
```
set company "CIC"
set designer "Student"

set CoreSearchPath /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/orig_lib/fsa0m_a/2009Q2v2.0/GENERIC_CORE/FrontEnd/synopsys/
set IOSearchPath /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/orig_lib/fsa0m_a/2008Q3v1.2/T33_GENERIC_IO/FrontEnd/synopsys/
set MemoryPath ../sim/SRAM\ ../sim/data_array\ ../sim/tag_array
set DefintionPath ../include

set search_path    "$CoreSearchPath $IOSearchPath $MemoryPath $DefintionPath $search_path"
set target_library " fsa0m_a_generic_core_ss1p62v125c.db fsa0m_a_generic_core_ff1p98vm40c.db SRAM_WC.db SRAM_BC.db dat
set synthetic_library "dw_foundation.sldb"
set link_library   "* $target_library $synthetic_library"
set symbol_library "fsa0m_a_generic_core.sdb fsa0m_a_t33_generic_io.sdb"

set_min_lib "fsa0m_a_generic_core_ss1p62v125c.db" \
        -min "fsa0m_a_generic_core_ff1p98vm40c.db"     ; # for core lib
set_min_lib "fsa0m_a_t33_generic_io_ss1p62v125c.db" \
        -min "fsa0m_a_t33_generic_io_ff1p98vm40c.db"   ; # for IO lib
set_min_lib "SRAM_WC.db" \
        -min "SRAM_BC.db"                              ; # for Memory
set_min_lib "data_array_WC.db" \
        -min "data_array_BC.db"                        ; # for Memory
set_min_lib "tag_array_WC.db" \
        -min "tag_array_BC.db"                         ; # for Memory

set verilogout_no_tri true
set hdlin_enable_presto_for_vhdl "TRUE"
set sh_enable_line_editing true
history keep 100
alias h history
```

Corner	Temperature	Voltage
SS	125	1.62
TT	25	1.8
FF	-40	1.98

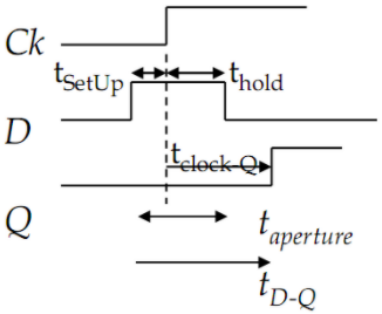
Back

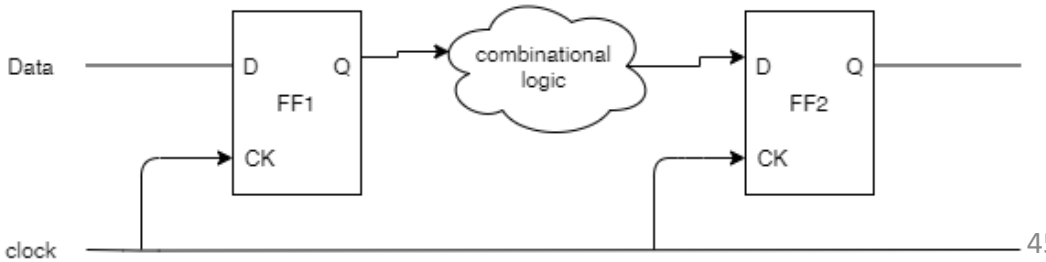
Timing violation

- **Setup time & hold time**
  - Setup time : the amount of time the data at the synchronous input (D) must be stable before the active edge of clock.
  - Hold time : the amount of time the data at the synchronous input (D) must be stable after the active edge of clock.
- **Launch edge & latch edge :**



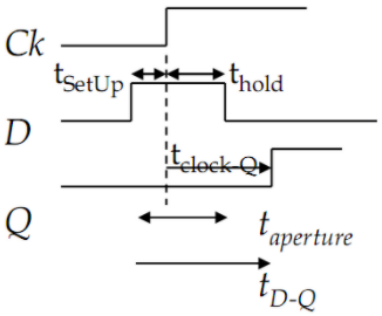
- **Arrival time**
  - Data arrival time (launch edge + clock source -> FF1/CK + FF1/CK -> FF1/Q + FF1/Q -> FF2/D + data transition time)
  - Clock arrival time (latch edge + clock source -> FF2/CK + clock transition time)

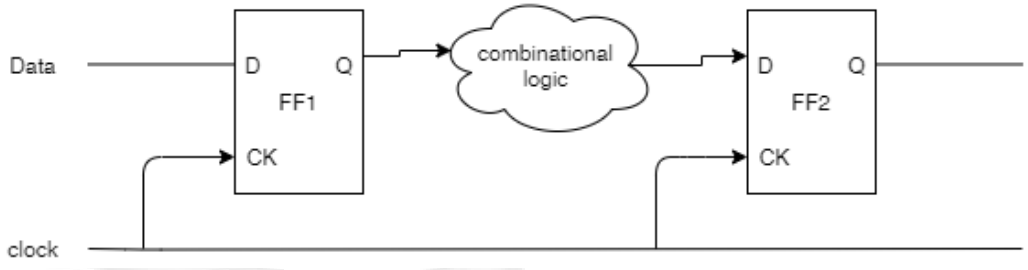




Timing violation

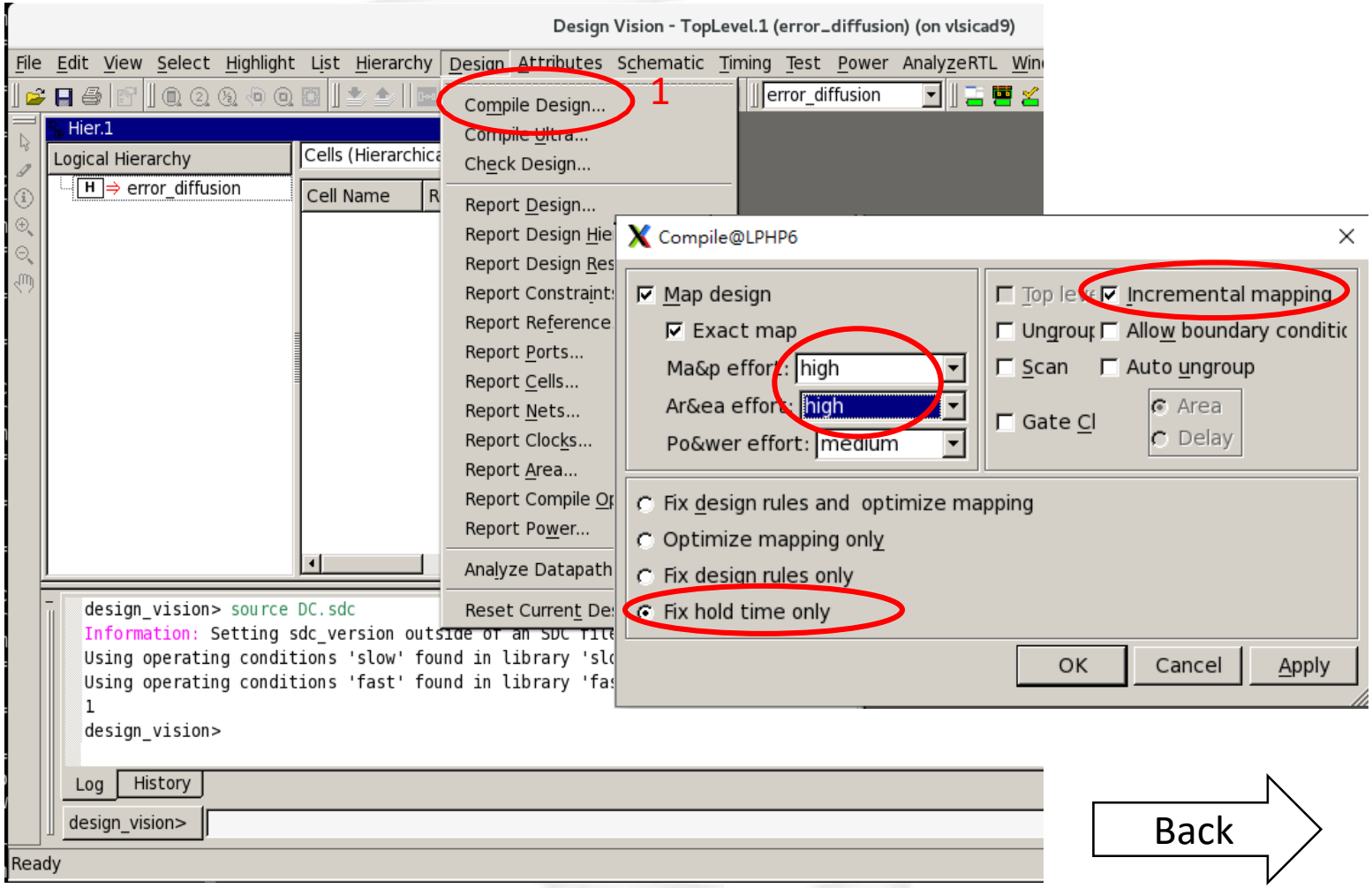
- Setup time violation (data path too long)
  - → Clock arrival time < Data arrival time + setup time
  - → How to fix ?
    - Add clock period
    - Add flip-flops in longest clock path
- Hold time violation (data path too short)
  - → Clock arrival time + hold time > Data arrival time
  - → How to fix ?
    - Fix hold (add buffers in data path)
    - Incremental compile





Timing violation

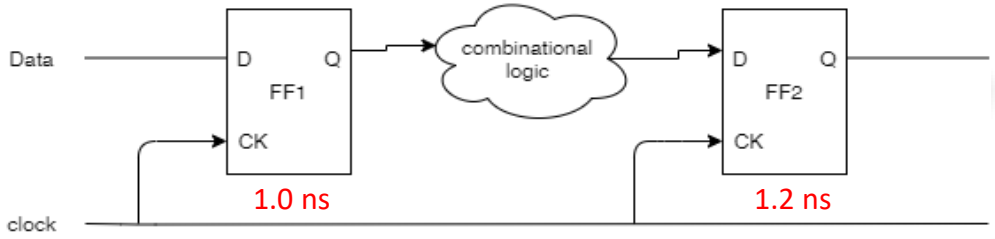
Incremental compile



Back

Clock uncertainty

- Clock uncertainty ≈ clock skew + clock jitter
- Clock skew
  - The maximum difference between the arrival of clock signals at sequential cells in one clock domain or between domains



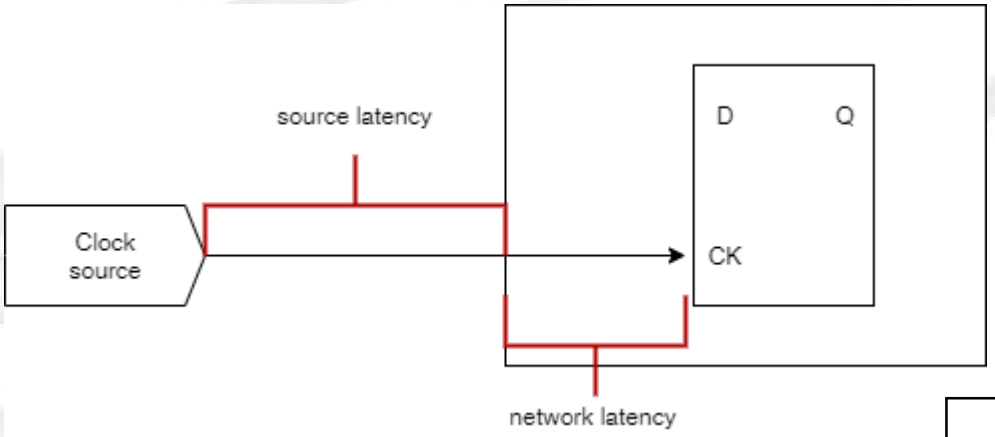
Clock skew = 1.2 – 1.0 = 0.2 (ns)

- Clock jitter
  - the timing variations of a set of signal edges from their ideal values

Back

Clock latency

- What is clock latency
  - Source latency
    - Propagation time from the actual clock origin to the clock definition point in the design
  - Network latency
    - Propagation time from the clock definition point in the design to the register's clock pin



Back

Thank you
For your attention!!