N26F300
VLSI SYSTEM DESIGN
(GRADUATE LEVEL)

Fall 2022

Instructor & TAs

Instructor: 邱瀝毅 (Lih-yih Chiou), Ph.D.

email: lihyih@mail.ncku.edu.tw

TEL: 06-2757575 ext 62379

Office: EE 95309 (奇美樓)

Course Website: http://moodle.ncku.edu.tw

TAs:潘姵羽/楊竣文/鄭俊升/張辰維

TEL: 06-2757575 ext 62400-2852

Room: EE95316 (奇美樓)

email: vivian.pan21@gmail.com

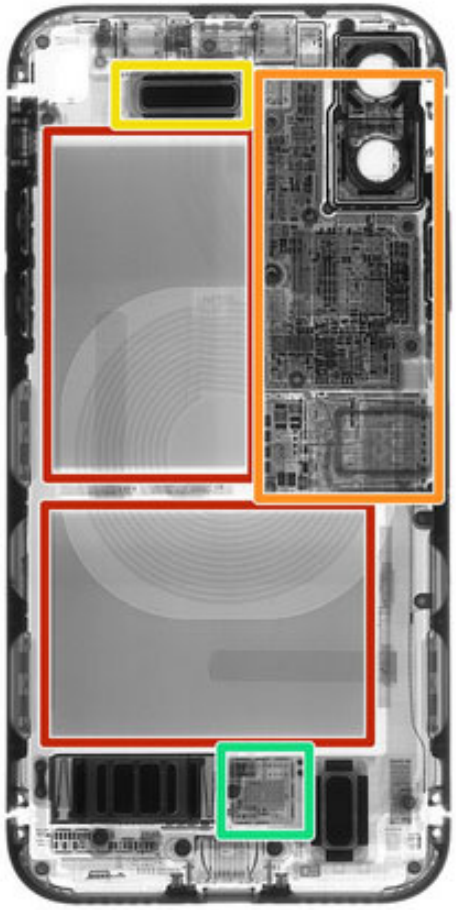
office hour: Mon. 15:00--17:00 EE95316

Electronic Device: iPhone X

- CPU: A11 Bionic with neural engine
- Cellular and Wireless
  - GSM, CDMA, 802.11ac, Bluetooth 5.0, NFC
- Location: GPS, GLONASS, Wi-Fi/Cellular
- Display
  - Super Retina: 2436x1125 pixel 458 dpi
- Camera, Photos & Video
- Battery & Charger
  - Lithium-ion battery/Qi wireless charger
- Audio playback
- TV and Video

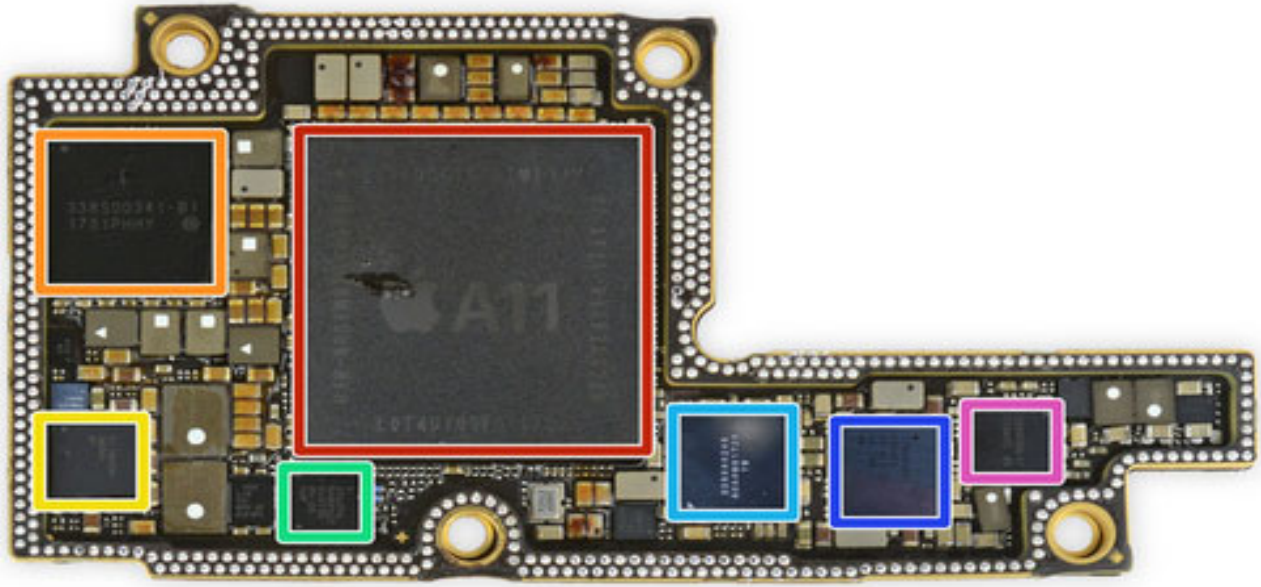
Source: www.ifixit.com

Recon Inside of iPhone X



Components Inside iPhone X (1/3)

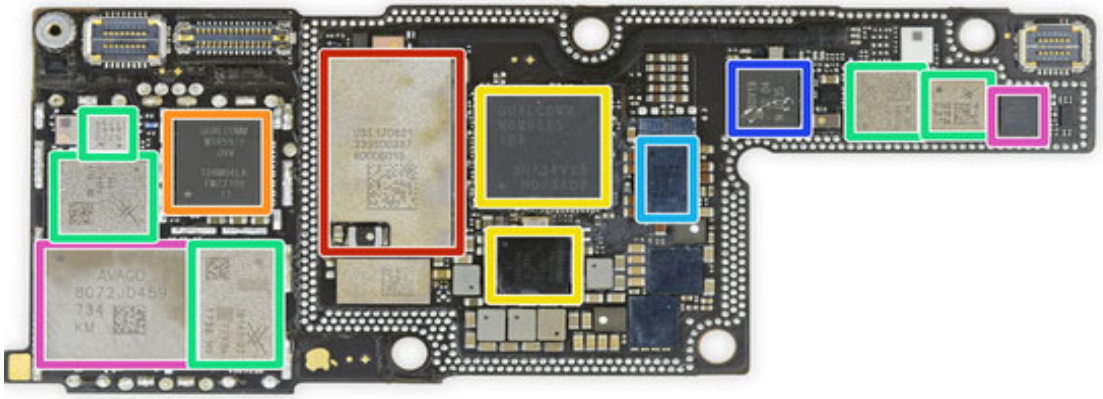
- A11 Bionic SoC 3GB LPDDR4x RAM
- Apple power management IC
- TI battery charger
- Apple audio codec
- Apple power management IC



Source: www.ifixit.com

Components Inside iPhone X (2/3)

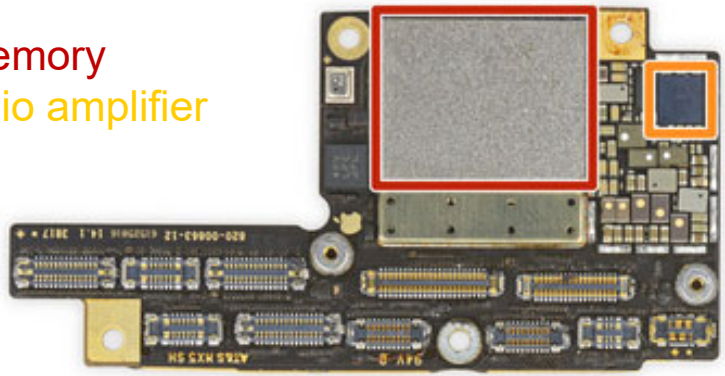
- Apple Wifi/Bluetooth module
- Qualcomm gigabit LTE transceiver
- Qualcomm Snapdragon X16 LTE modem
- Skyworks power amplifier module
- Broadcom wireless charging controller
- NXP NFC controller module
- Broadcom AFEM power amplifier

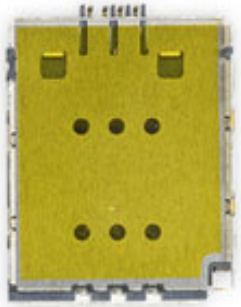


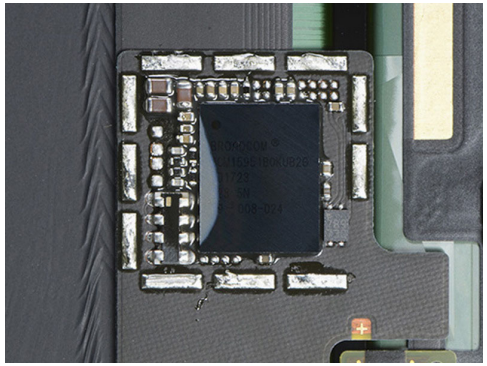
Source: www.ifixit.com

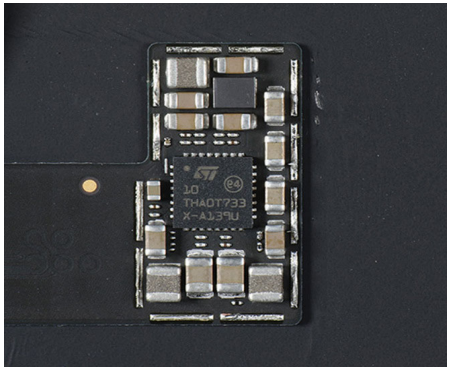
Components Inside iPhone X (3/3)

- Toshiba 64GB flash memory
- Apple/Cirrus Logic audio amplifier









- Broadcom touch screen controller
- STMicro OLED PMIC

Source: www.ifixit.com

Top 10 Fabless Companies in 2006

Company		2006 Revenue (US millions)
1	QUALCOMM	$4,331.0
2	Broadcom	$3,667.8
3	ScanDisk Corporation	$3,257.5
4	NVIDIA Corporation	$3,068.8
5	Marvell Technology Group Ltd.	$2,237.6
6	LSI Logic	$1,982.1
7	Xilinx, Inc.	$1,871.6
8	MediaTek Incorporation	$1,624.5
9	Altera	$1,285.5
10	Conexant Systems	$985.6

Source: www.fsa.org

Top 10 Fabless Companies in 2011

2011	2010	2009	公司名	2011年 營收（億美元）	主要產品
1	1	1	Qualcomm (高通)	99.1	手機晶片 、 無線通訊晶片
2	2	3	Broadcomm (博通)	71.6	手機晶片、無線通訊晶片 、 數據機與GPS晶片
3	3	2	**AMD**	65.7	繪圖晶片、fab to Global Foundries
4	6	5	Nvidia	39.4	繪圖晶片
5	4	6	Marvell (邁威爾)	34.4	網路晶片、 手機晶片
6	5	4	聯發科	29.7	光儲存晶片、 手機晶片、數位電視晶片
7	7	7	Xilinx(智霖)	22.7	可程式邏輯晶片 （主要用於家電及電腦週邊）
8	8	10	Altera (阿爾特拉)	20.6	可程式邏輯晶片
9	9	8	LSI	20.4	儲存晶片、 光儲存晶片
10	10	11	Avago (安華高)	13.4	類比晶片

Source: http://www.electroiq.com/articles/sst/2012/04/top-25-fabless-ic-companies-in-2011.html

Top 10 Fabless Companies 2014

2014	2013	2012	公司名	2014年 營收 (億美元)	主要產品
1	1	1	Qualcomm (高通)	191.0	手機晶片 、 無線通訊晶片
2	2	3	Broadcomm (博通)	83.6	手機晶片、無線通訊晶片、數據機與GPS晶片
3	4/13	5/11	MediaTek + MStar	71.42	手機晶片、數位電視晶片、無線通訊晶片、HDMI/HDCP
4	4	3	AMD	55.12	繪圖晶片、fab to Global Foundries
5	10/7	10/7	Avago (安華高) + LSI	50.87	類比晶片、儲存晶片、光儲存晶片
6	6	4	Nvidia	42.37	繪圖晶片
	6	6	Marvell (邁威爾)		網路晶片、 手機晶片
	8	8	Xilinx(智霖)		可程式邏輯晶片 (主要用於家電及電腦週邊)
	9	9	Altera (阿爾特拉)		可程式邏輯晶片
	11	12	Novatek (聯詠)		螢幕用驅動 IC，數位影音, 多媒體單晶片
	12	13	HiSilicon (海思)		數位電視晶片、網路監控晶片、手機晶片

Top 10 Fabless Companies 2015

2014	2013	公司名	2015年 營收百分比 (%)	主要產品
1	1	Qualcomm (高通)	17.80	手機晶片 、 無線通訊晶片
2	2	Broadcomm (博通)	9.30	手機晶片、無線通訊晶片、 數據機與GPS晶片
3	4/13	MediaTek + MStar	7.40	手機晶片、數位電視晶片、無線通訊晶片、HDMI/HDCP
4	4	AMD	4.20	繪圖晶片、fab to Global Foundries
5	10/7	Nvidia	3.70	類比晶片、儲存晶片、光儲存晶片
10	6	HiSilicon (海思)	3.40	繪圖晶片
6	6	Marvell (邁威爾)	3.10	網路晶片、 手機晶片
7	8	Xilinx(智霖)	2.40	可程式邏輯晶片 (主要用於家電及電腦週邊)
	9	Qorvo (RFMD和TriQuint)	2.30	射頻晶片
9	11	Novatek (聯詠)	1.80	螢幕用驅動 IC，數位影音, 多媒體單晶片

Source: http://www.electroiq.com/articles/sst/2012/04/top-25-fabless-ic-companies-in-2011.html

Top 10 Fabless Companies 2017

2017	2016	公司名	2017/2016 營收變化 百分比 (%)	主要產品
1	1	Qualcomm (高通)	11	手機晶片 、 無線通訊晶片
2	2	Broadcomm (博通)	16	手機晶片、無線通訊晶片、數據機與GPS晶片
3	5	Nvidia	44	繪圖、AI 晶片
4	3	MediaTek	-11	手機晶片、數位電視晶片、無線通訊晶片、HDMI/HDCP
5	4	Apple	3	Custom ICs for internal use
6	6	AMD	23	繪圖晶片、fab to Global Foundries
7	6	HiSilicon (海思)	21	網路控制、影視電話、無線網路、數位多媒體晶片
8	8	Xilinx(智霖)	7	可程式邏輯晶片 (主要用於家電及電腦週邊)
9	9	Marvell (邁威爾)	-1	網路晶片、 手機晶片
10		Unigroup (紫光)	9	無線網路、RF晶片

Source: ICInsight

Top 10 Fabless 2020

2020	2019	Company	2020/2019 Percentage of Change (%)	Major Product (IC)
1	2	Qualcomm (高通)	33.7	Mobile phone, Wireless
2	1	Broadcomm (博通)	2.9	Set top Box, Mobile Phone, Wireless, Processor, BT
3	3	Nvidia	52.2	GPU, AI
4	4	MediaTek	37.3	Mobile phone, digital TV, Wireless, HDMI/HDCP
5	5	AMD	45	GPU、fab to Global Foundries
6	6	Xilinx(智霖)	-5.6	Programmable Logic
7	7	Marvell (邁威爾)	8.7	Network, Mobile
8	8	Novatek (聯詠)	30.1	Display, MultiMedia
9	9	Realtek (瑞昱)	34.1	Network, SWITCH, WLAN, Audio Codec
10	10	Dialog (戴樂格)	-3.2	Power Management, Audio Codec, Sensor, IoT Wilress, BT

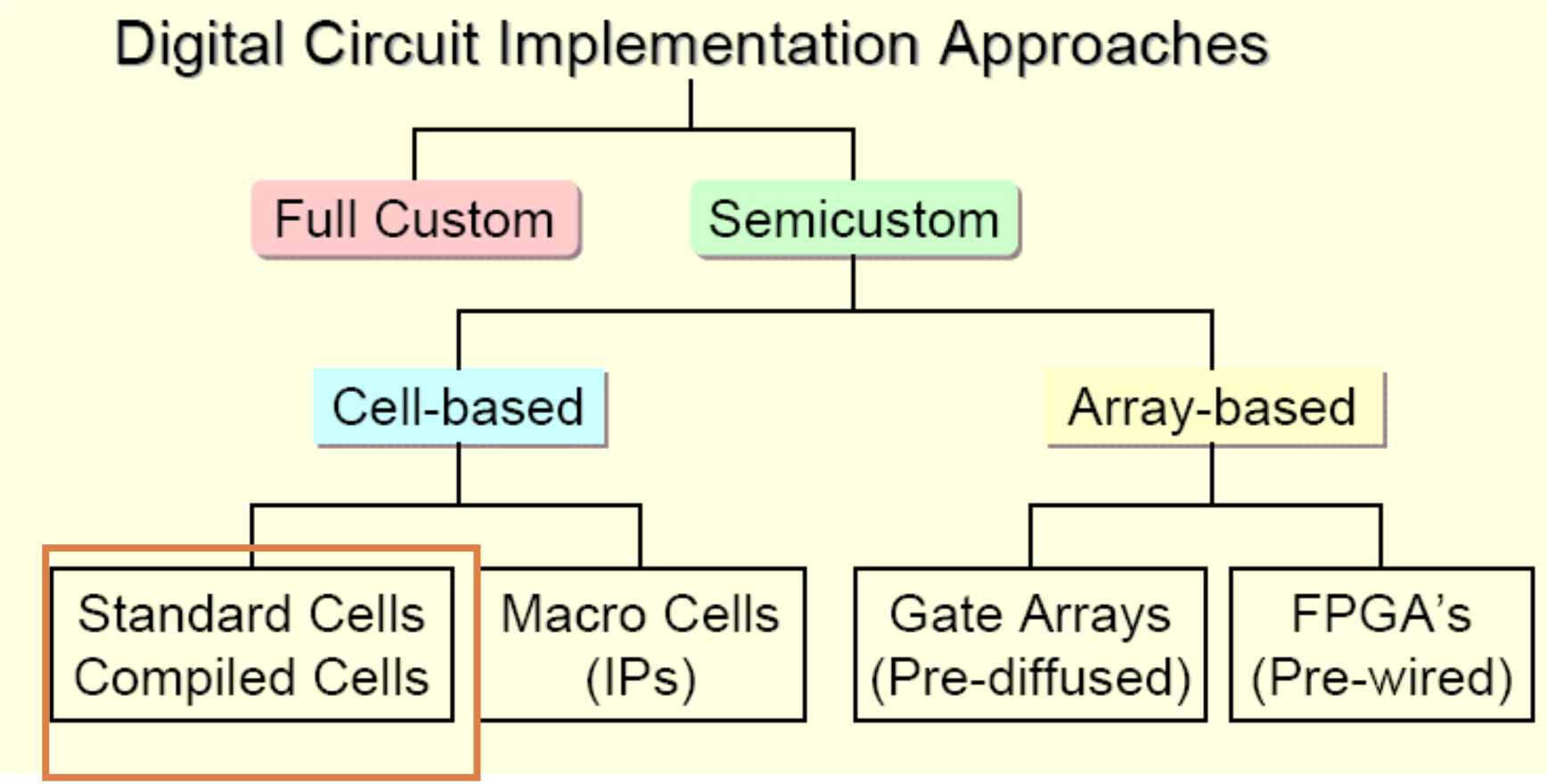
Source: ICInsight

Top 10 Fabless 2021

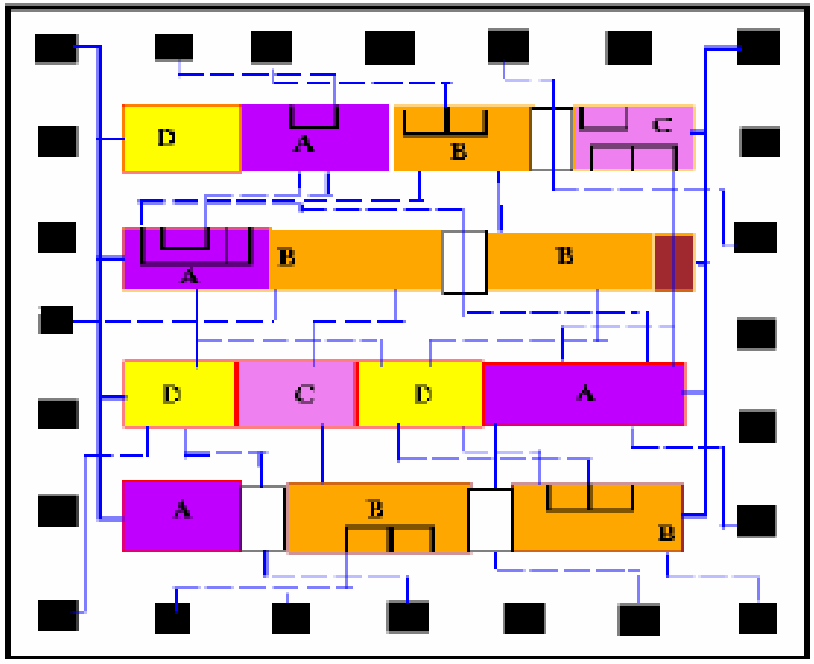
2021	2020	Company	2021/2020 Percentage of Change (%)	Major Product (IC)
1	1	Qualcomm (高通)	51	Mobile phone, Wireless
2	3	Nvidia	61	GPU, AI
3	2	Broadcomm (博通)	18	Set top Box, Mobile Phone, Wireless, Processor, BT
4	4	MediaTek	61	Mobile phone, digital TV, Wireless, HDMI/HDCP
5	5	AMD	68	GPU、fab to Global Foundries
6	8	Novatek (聯詠)	79	Display, MultiMedia
7	7	Marvell (邁威爾)	46	Network, Mobile
8	9	Realtek (瑞昱)	43	Network, SWITCH, WLAN, Audio Codec
9	6	Xilinx(智霖)	20	Programmable Logic
10	-	Himax (奇景)	74	Display

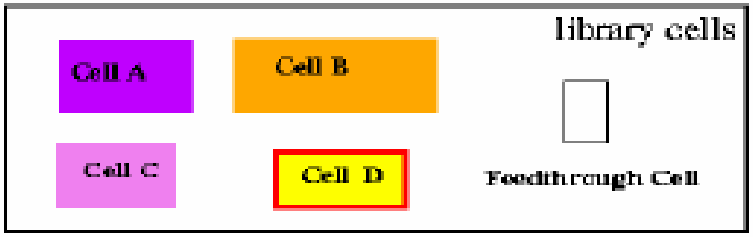
Source: TrendForce, Mar. 2022

Target Digital Design Implementation



Standard Cell Design Style



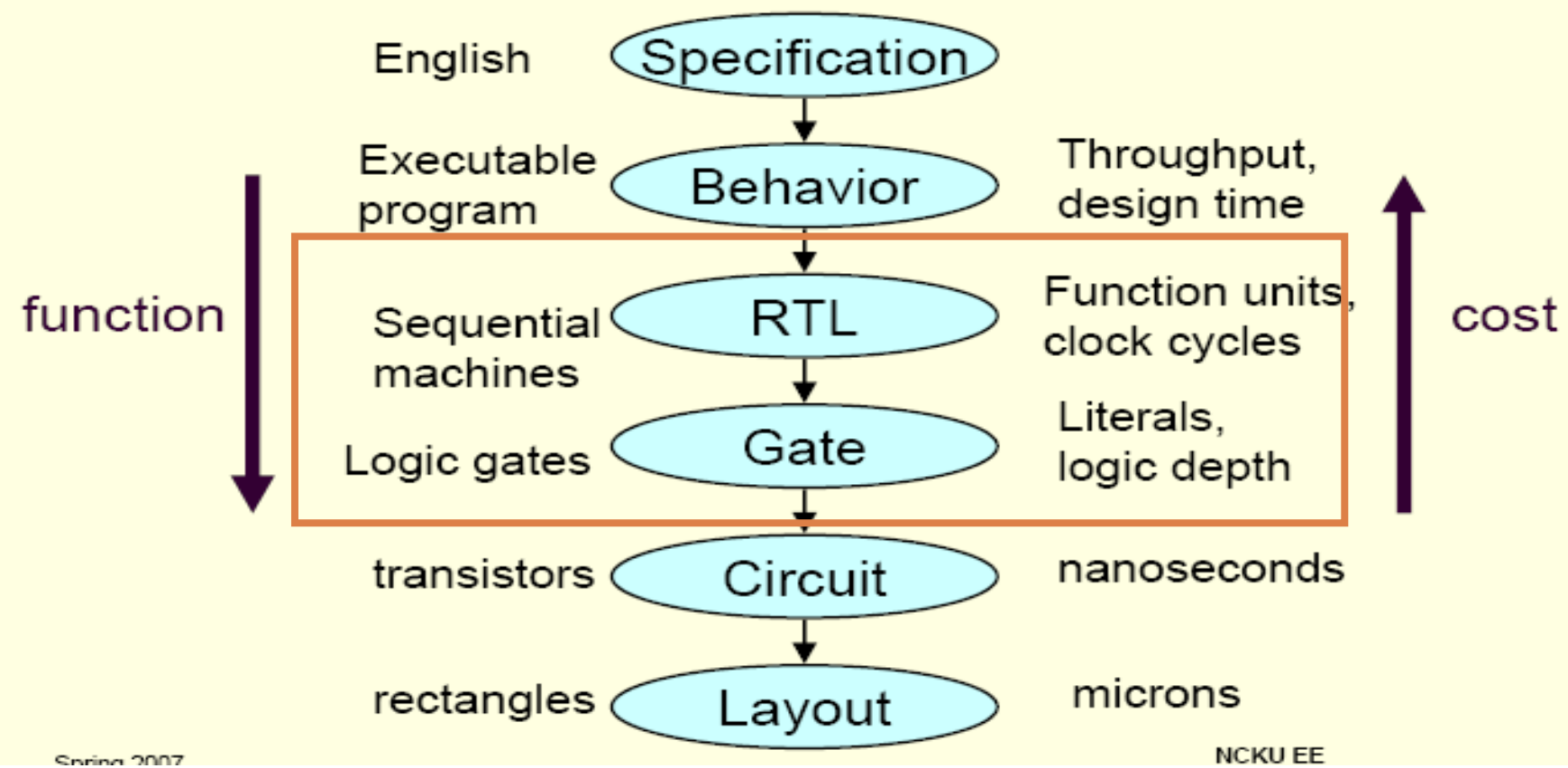


Selects pre-design cells (of the same height) to implement logic

These cells may be

- Logic gates: nand2, NOT, and2, and4, nor2, mux2, decoder etc.
- Latches: latchx1, latchrx2, …
- Flip-flops: pdffx1, pdffx2,…
- Basic blocks: fulladder

Target Levels of Design Abstractions



Course Objectives

- Provide fundamental design concepts
  - Modeling systems using Verilog/SystemVerilog-HDL
  - Digital IC design flow using modern CAD tools
  - Design of synchronous systems
  - Synthesis of HDL
- Establish design and analysis skills for
  - Multi-cycle architecture
  - Pipelined architectures
  - SoC architecture

Course Prerequisites

- Digital Logic Design (MUST)
  - Boolean algebra
  - Logic minimization
  - Arithmetic units (+,-,*, AND, OR, …)
  - Finite state machine
- Computer Organization (MUST)
  - Multi-cycle CPU
  - Pipeline CPU
  - Cache
- Verilog HDL (Entry-level, Required)
- Self-motivation in learning CAD tools (MUST)

Outline

- Basic Digital IC System Design (6 weeks)
  - VLSI digital design flow/EDA tools
  - Digital design using Verilog/SystemVerilog
  - Synthesis and verification of digital modules
- Advanced IC System Design (6 weeks)
  - Design of a digital processor with a bus subsystem
  - Special Issues of IC System design (Industrial Talks)
- Project (6 weeks)
  - Proposal
  - Demo
  - Presentation

Hours Arrangement (when pandemic prevention protocol enforced)

- Lecture (on-line, pre-recorded, or on-site)
  - Time: Wednesday 2:10-5:00pm
  - On-line: Teams/Webex/ GoogleMT
  - Location: EE 92331 for on-site
  - Located on Moodle
- Tutorials (pre-recorded excepted the first few ones)
  - Dates and Time: Posted on Moodle
- Laboratory (Use workstations in your own lab as often as possible, SoC lab only for checking compatibility and special EDA tools. NOT OPEN for remote access.)
  - Location: EE 4F Computer Lab or SoC Lab (EE 95312@ChiMei Bld) (10 max.)
  - Will close when level-3 pandemic alert issues.

General Rules of the Laboratory

- DO NOT LOCK TERMINALS. Otherwise, your right will be suspended (7 days x number of violations)
- Door of SoC Lab shall be closed if no class in progress. Please be aware of the epidemic prevention protocol by washing your hands, wearing a mask and enter w/ your ID card swapped.
- Close AC of SoC Lab if you are the last one to leave!
- NO FOOD or DRINK in the computer labs

Grading Policy

- **Grading will be based on the following items and subject to minor change w/o notice:**
  - Homework assignments 40~50%
  - Discussion & Participation 05~10%
  - Final project report/demo 40~50%

Homework Assignments

- Principles
  - Help you to learn the materials
  - Promote self-motivated learning capability as a graduate student
  - Focus on your learning and perform self-evaluation

- Ideas
  - Time-limited HW assignment
  - A series of lab work as homework
  - A project-oriented homework

Homework Assignments

- 4 homework assignments
- Submit electronically through the course website before the specified time and date. No credits if sent by emails to TA unless you are instructed to do so.
- If not submit in time, your assignment is considered OVERDUE and get NO credit.
  - Those, who resubmit with TA approval within 48 hrs after due day because of incomplete code or package submission, will received 50% penalty of your assignment credits. After 48 hrs, No credit.
- If your code can not be compiled or rerun by tools in SoC Lab, that particular assignment gets NO credit.
- If not follow specified rules by an assignment, you cannot get full credits.

Teaching Methods

- Interactive classroom
  - In-class discussion (group/individual), feedback mechanism, lecture, on-line quizzes (prepare your web camera first)
- Insights provided by industry professionals
  - Senior designers/directors/CTO from IC industry to share their experiences in IC design career and review/grade your projects
- Maker-style Homework
  - Guided assignments
  - Realistic final project – assemble team, proposal, project management, implementation, demonstration, presentation and review

Final Project

- Principles
  - Use learned design skills for your target applications
  - Need team work (4~6 persons/team)
  - Promote self-tracking capability as a graduate student
  - Focus on end results AND **NOT allow to use IP generators**

- Ideas
  - Propose and present your interested project based on requirements
  - Discuss your team project regularly in person or on Moodle
  - Emphasize on verified designs with state-of-the-art methods
  - Plan and meet schedules like IC industry

Final Project

- **Tentative Schedule**
  - Submit your Proj. member form 14:00@ Moodle (09/14)
  - Proposal presentation with pre-recorded video (11/09, 11/16, 11/23)
  - Project submission/Demo (01/10, Tue.)

    09:00 @Moodle ; 10:00 ~ 18:00 @EE95312 (SoC Lab)
  - Project Presentation (01/12, Thu.) Room (TBA)
- **Topic**
  - **Design a digital SoC consisting of a general pipeline processor and another core, either an application processor or computing processor, via an on-chip bus, AXI, in synthesizable RTL and eventually to P&R. The micro-processor system shall be verified. (Detailed guidelines will be posted later)**

Course Policy

- Encourage you to discuss assigned problems with peers.
- Must complete his/her assignment independently or as specified. NOT allow to share codes in any means, either partially or fully. **We will perform similarity check across all attending students, current or before. (Actually we did find several and those students DO get "zero.")**
- Any person/team who is found to be dishonesty in homework assignments, examines/quizzes, or the project, the involved person(s) will receive an ***"0"*** on the evaluated instrument (*paper, exam, project, homework, etc.*)
  - It is NOT allowed to do illegal access, via third party or unauthorized involvement. Those who do Illegal access will **receive extra penalty** (倒扣 至少該作業的50%分數) for his/her behavior.

Warning! Warning! Warning!

- This course is designed to finish a realistic IC design project. The work load of the course is extremely HIGH. Really! NOT JOKING! REALLY! NOT recommend to those have little time or just want to taste the flavor of IC design.
- The first 1~2 homework assignments, you need to prove that you can learn fast and debug your design effectively. (1st HW, 5-stage CPU w/ synthesis, 5 weeks)
- Make sure your advisor know and agree you to take this high-workload course. (Like IC industry, deadlines are hard!) Also, you need to have workstations in your own lab.

Actions Related to Pandemic Prevention if Physically Attending the Class

- Bring your student ID and tap over the card reader at the classroom and laboratories.
- Wear a mask whenever necessary.
- No unauthorized access to computer rooms.
- Lecturing/tutoring using hybrid (virtual-physical), pre-recorded, on-line fashions.
- DO follow advises by TAs on requests of this matter.

Attention: Action Needed!!

- **Submit your head photo.**
- Check in course overview acknowledge (確認已閱讀教學課綱) on the *Moodle*.
- Consent rules of using SoC Lab (確認SoC實驗室使用規則) on the *Moodle*.
- Fill TSRI technology application form, student back ground survey, and project team member form. No team, no enrollment.
- All 7 things need to be done before deadline.
- Otherwise, RESERVE the right to cancel your lab account and accesses to SoC lab.

Notes: SoC Lab Entrance Authorization

- Applying SoC Lab entrance authorization needs to have your department entrance card number.
- Do it today by filling your card ID number in the cloud. How to obtain your card ID number? When swapping over the card reader before SOC Lab, you can write down your number.
- Due to pandemic prevention requirements, your card only allow you to enter the room. It will be considered improper to enter without card pass.
- As stated earlier, you shall use workstations in your own research lab mainly. SoC lab will close midnight-8:00am tentatively. Open schedule will be posted later.

Tutorials on 9/07

- Contents
  - 9/07: Working environment, Basics of Linux, Verilog compiler/simulator (NC-Verilog), Verdi, RISC-V Tools, SuperLint, and HW1 explanation
- Lab hours
  - Find your own time to learn and practice on workstations of your own lab or SoC lab. Note that setting of your own research lab will be different. You need to adjust by your lab workstation manager.

Must-Filled Survey

已經在moodle的學生
填寫表單的QR code

加簽學生要填寫
表單的 QR code

Reference Books

- "Advanced Digital Design with Verilog HDL," Michael D. Ciletti, Prentice Hall, 2003. ISBN: 0-13-089161-4
- "FSM based Digital Design using Verilog HDL," Peter Minns and Ian Elliott, Wiley, 2008. ISBN: 978-0-470-06070-4
- "Digital Design: An Embedded System Approach Using Verilog," by Peter J. Ashenden. Weste and David Harris, Morgan Kaufmann, 2008. ISBN: 978-0-12-369527-7
- "Computer Organization and Design: The Hardware/Software Interface," 3th ed. by David A. Patterson and John L. Hennessy, Morgan Kaufmann Pub., 2005. ISBN: 981-2592-17-2
- "Verilog HDL: A Guide to Digital Design and Synthesis," 2nd ed. by Samir Palnitkar, Prentice Hall, 2003. ISBN: 0-13-044911-3
- "SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling," 2nd ed. By S. Sutherland etc., Springer, 2006. ISBN: 0-387-33399-1.
- "Digital Integrated Circuit Design using Verilog and SystemVerilog," by Ronald Mehler, Elsevier, 2014. ISBN: 978-0-12-408059-1.
- "SystemVerilog for Verification: a Guide to learning the testbench language features," 3rd ed., by C.Spear & G. Tumbush, Springer 2012. ISBN: 978-1-4614-0714-0.