Innovus

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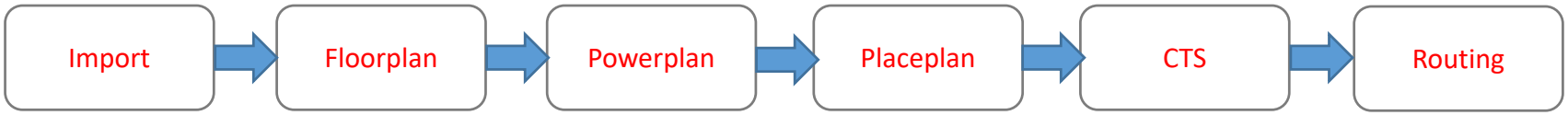
Outline

- Introduction
- Import design
- Floorplan
- Powerplan
- Clock Tree Synthesis
- Routing
- DRC / LVS / Antenna
- Save / Export Files
- Report Design
- Reference

Introduction

- Innovus, successor of SoC Encounter, which developed by Cadence, is an Automatic Placement & Routing (APR) tool.
- With this tool, you can export the synthesized gate level netlist to the GDS layout.
  - GDS: Graphic Design System, a database file format for IC layout



Open GUI

- [innovus/build] $ innovus Do not use &
- [innovus] $ make innovus
  - In this exercise & homework

```
[            N26094728]$ make innovus
maxpend=1
mkdir -p ./build
cd ./build; \
innovus

Cadence Innovus(TM) Implementation System.
Copyright 2018 Cadence Design Systems, Inc. All rights reserved worldwide.

Version:        v18.11-s100_1, built Mon Sep 17 18:39:52 PDT 2018
Options:
Date:           Wed Sep 29 17:03:51 2021
Host:           LPHP3 (x86_64 w/Linux 3.10.0-1062.4.1.el7.x86_64) (16cores*64cpus*Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz 22528KB)
OS:             CentOS Linux release 7.7.1908 (Core)

License:
                invs    Innovus Implementation System   18.1    checkout succeeded
                8 CPU jobs allowed with the current license(s). Use setMultiCpuUsage to set your required CPU count.
Create and set the environment variable TMPDIR to /tmp/innovus_temp_223879_LPHP3_eric109_T5fm7A.

Change the soft stacksize limit to 0.2%RAM (256 mbytes). Set global soft_stack_size_limit to change the value.

**INFO:  MMMC transition support version v31-84

innovus 1>
```

Import design

Set the design constraints

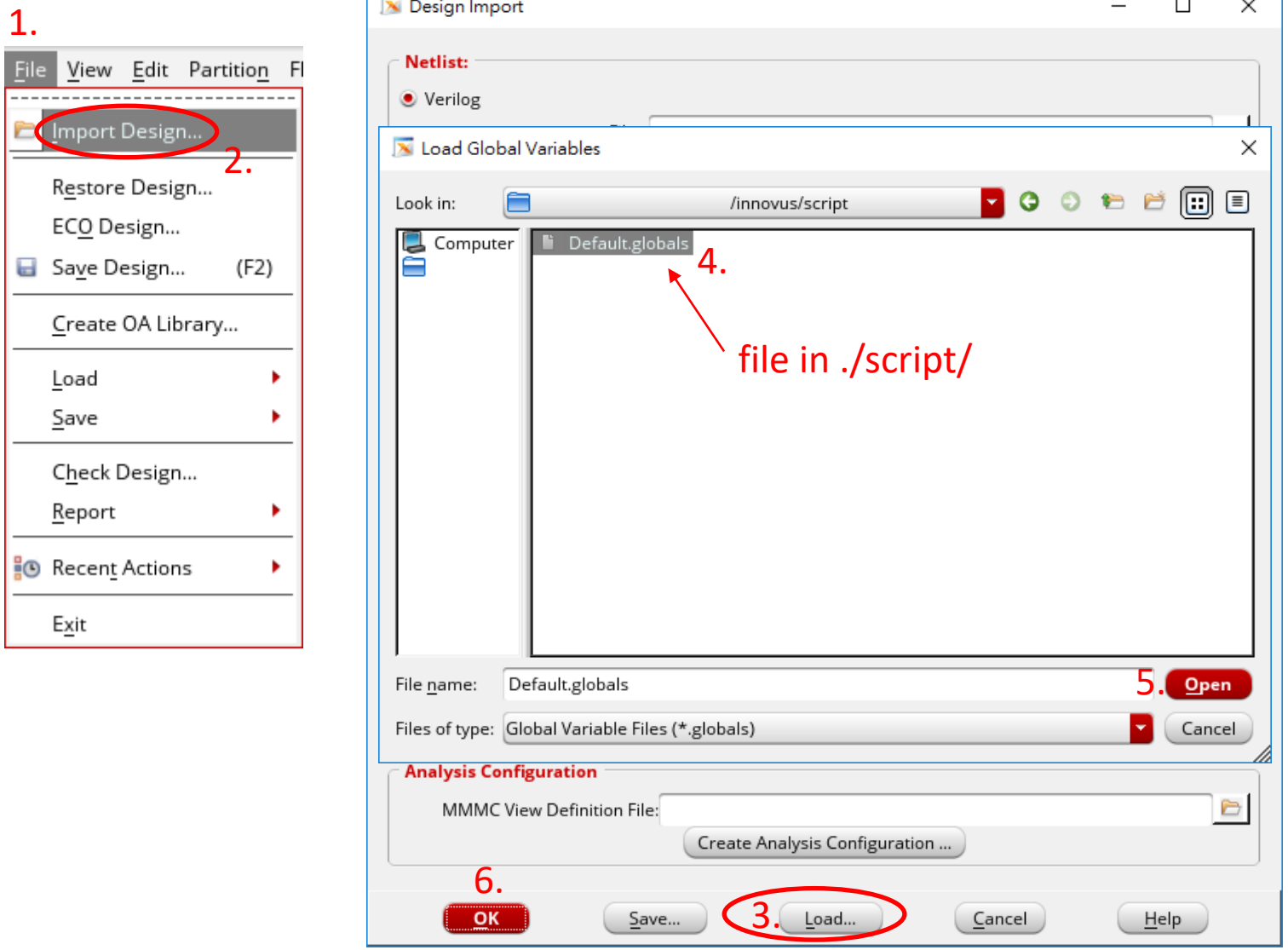
- Uniquify instantiated cell types
  - Let the multiple modules have different name, which means each module is different.
  - For example, there are 2 SRAM modules, but they are different. If we don't uniquify the modules, the process will stop and have errors.

```
innovus 1> set init_design_uniquify 1
1
```

- Prevent tool from adding any new assign statements to the Verilog netlist

```
innovus 2> set init_no_new_assigns 1
1
```

Import Design



Default.globals

- Design setup, including the design node LEF file and the MMMC view file.
  - LEF file: Physical library, including process technology and APR technology

```
set ::TimeLib::tsgMarkCellLatchConstructFlag 1$
set conf_qxconf_file {NULL}$
set conf_qxlib_file {NULL}$
set defHierChar {/}$
set distributed_client_message_echo {1}$
set distributed_mmmc_disable_reports_auto_redirection {0}$
set eco_post_client_restore_command {update_timing ; write_eco_opt_db ;}$
set enc_enable_print_mode_command_reset_options 1$
set init_design_uniquify 1$
set init_gnd_net {GND}$
set init_lef_file {/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lef/header6_V55_20ka_cic.lef$
                   /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lef/BONDPAD.lef$
                   /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lef/fsa0m_a_generic_core.lef$
                   /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lef/fsa0m_a_t33_generic_io.lef$
                   ../sim/SRAM/SRAM.lef ../sim/data_array/data_array.lef ../sim/tag_array/tag_array.lef$
                   /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lef/FSA0M_A_GENERIC_CORE_ANT_V55.lef$
                   /usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lef/FSA0M_A_T33_GENERIC_IO_ANT_V55.lef
                   }$
set init_mmmc_file {../script/MMMC.view}$
set init_pwr_net {VCC}$
set init_top_cell {top}$
set init_verilog {../syn/top_syn.v}$
set latch_time_borrow_mode max_borrow$
set pegDefaultResScaleFactor 1$
set pegDetailResScaleFactor 1$
set report_inactive_arcs_format {from to when arc_type sense reason}$
set soft_stack_size_limit {56}$
set tso_post_client_restore_command {update_timing ; write_eco_opt_db ;}$
```

LEF File

MMMC View

MMMC View

MMMC: Multi-Mode Multi Corner

- Using different constraints to optimize the design
  - Timing libraries(Max, Min, Typical)
  - Capacitance Table

```
# Version:1.0 MMMC View Definition File$
# Do Not Remove Above Line$
create_rc_corner -name RC -cap_table {/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/u18_Faraday.CapTbl} -preRoute_res {1.0} -preRoute_cap {1.0} -preRoute_clkres {0.0} -preRoute_clkcap {0.0} -postRoute_res {1.0} -postRoute_cap {1.0} -postRoute_xcap {1.0} -postRoute_clkres {0.0} -postRoute_clkcap {0.0}$
$
create_library_set -name lib_max -timing {/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lib/fsa0m_a_generic_core_ss1p62v125c.lib ../sim/SRAM/SRAM_WC.lib ../sim/data_array/data_array_WC.lib ../sim/tag_array/tag_array_WC.lib} -si {/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/celtic/u18_ss.cdb}$
create_library_set -name lib_min -timing {/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lib/fsa0m_a_generic_core_ff1p98vm40c.lib ../sim/SRAM/SRAM_BC.lib ../sim/data_array/data_array_BC.lib ../sim/tag_array/tag_array_BC.lib} -si {/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/celtic/u18_ff.cdb}$
create_library_set -name lib_typ -timing {/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/lib/fsa0m_a_generic_core_tt1p8v25c.lib ../sim/SRAM/SRAM_TC.lib ../sim/data_array/data_array_TC.lib ../sim/tag_array/tag_array_TC.lib} -si {/usr/cad/CBDK/CBDK018_UMC_Faraday_v1.0/CIC/SOCE/celtic/u18_tt.cdb}$
$
create_constraint_mode -name CM -sdc_files {../script/APR.sdc}$
$
create_delay_corner -name DC_max -library_set {lib_max} -rc_corner {RC}$
create_delay_corner -name DC_min -library_set {lib_min} -rc_corner {RC}$
create_delay_corner -name DC_typ -library_set {lib_typ} -rc_corner {RC}$
$
create_analysis_view -name AV_max -constraint_mode {CM} -delay_corner {DC_max}$
create_analysis_view -name AV_min -constraint_mode {CM} -delay_corner {DC_min}$
create_analysis_view -name AV_typ -constraint_mode {CM} -delay_corner {DC_typ}$
$
set_analysis_view -setup {AV_max AV_typ} -hold {AV_min}$
```

Capacitance table

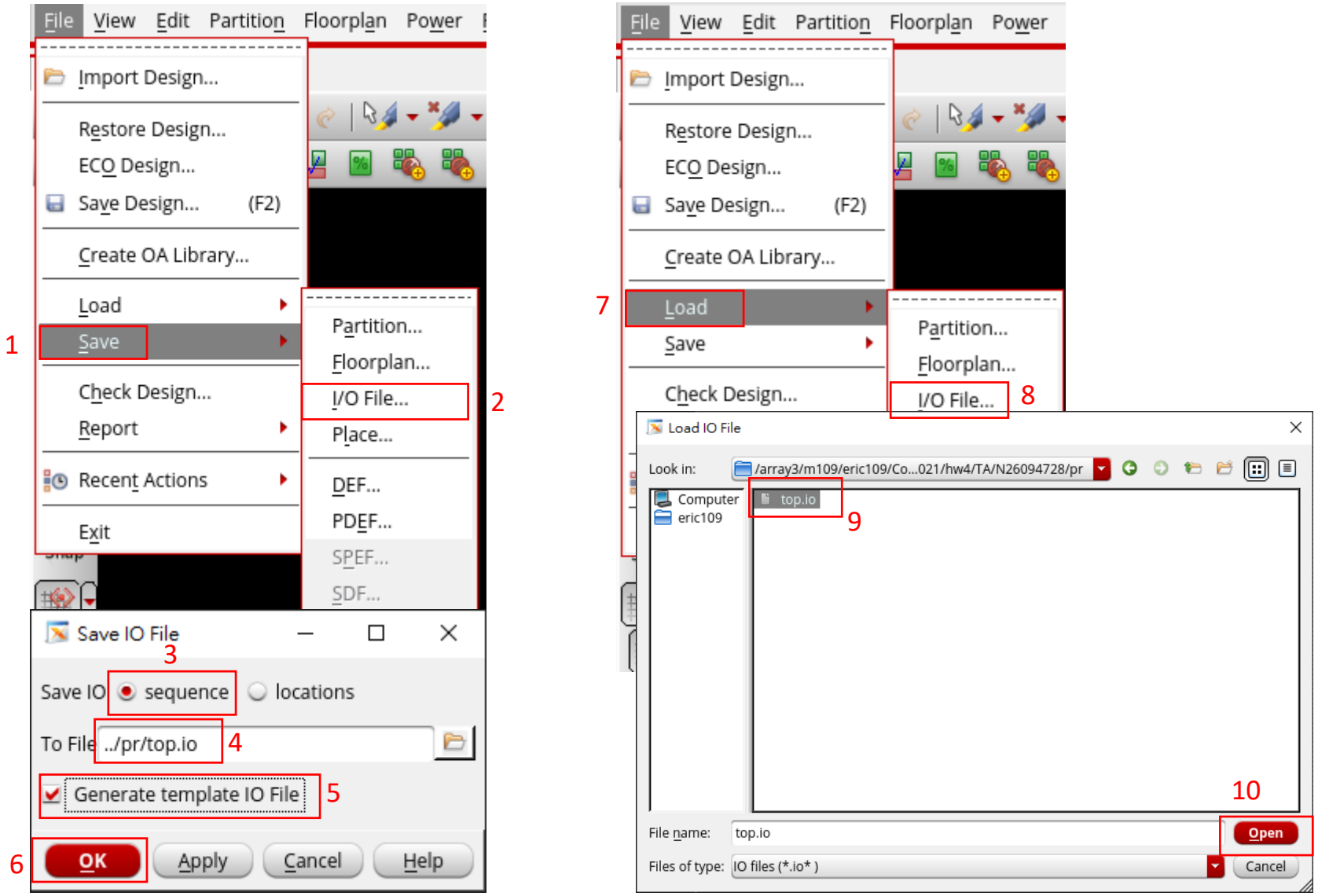
Different timing library(Max, Min, Typical

Design constraint

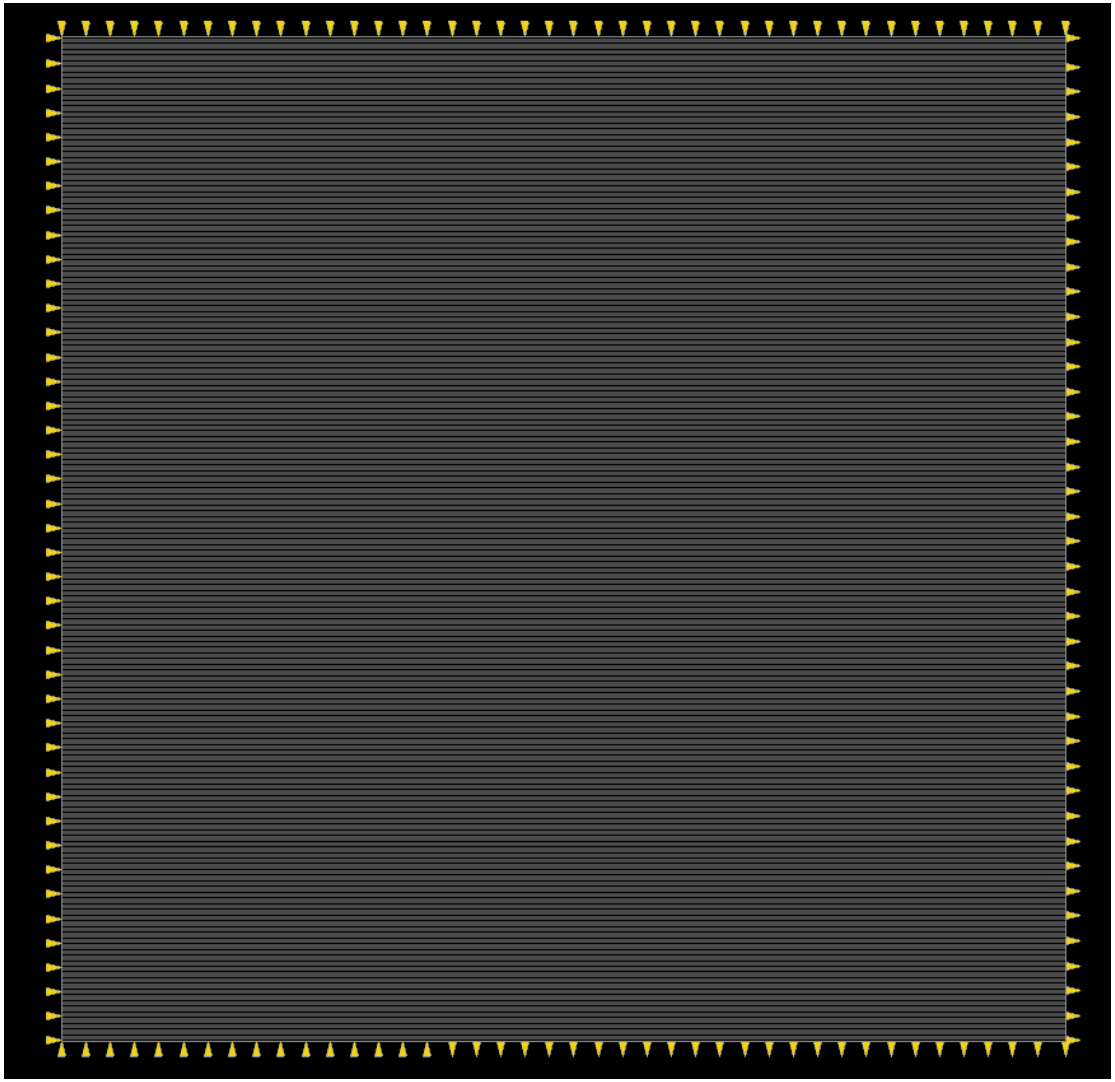
Combine timing & RC table to create delay corner

Set different analysis view for different timing issues

IO Pins(1/2)


File View Edit Partition Floorplan Power
Import Design...
Restore Design...
ECO Design...
Save Design... (F2)
Create OA Library...
Load
Save
Check Design...
Report
Recent Actions
Exit
Partition...
Floorplan...
I/O File...
Place...
DEF...
PDEF...
SPEF...
SDF...
1
2
Save IO File
3
Save IO sequence locations
To File ../pr/top.io
4
Generate template IO File
5
6
OK Apply Cancel Help
7
8
Load IO File
Look in: /array3/m109/eric109/Co...021/hw4/TA/N26094728/pr
Computer
eric109
top.io
9
10
File name: top.io
Open
Files of type: IO files (*.io*)
Cancel

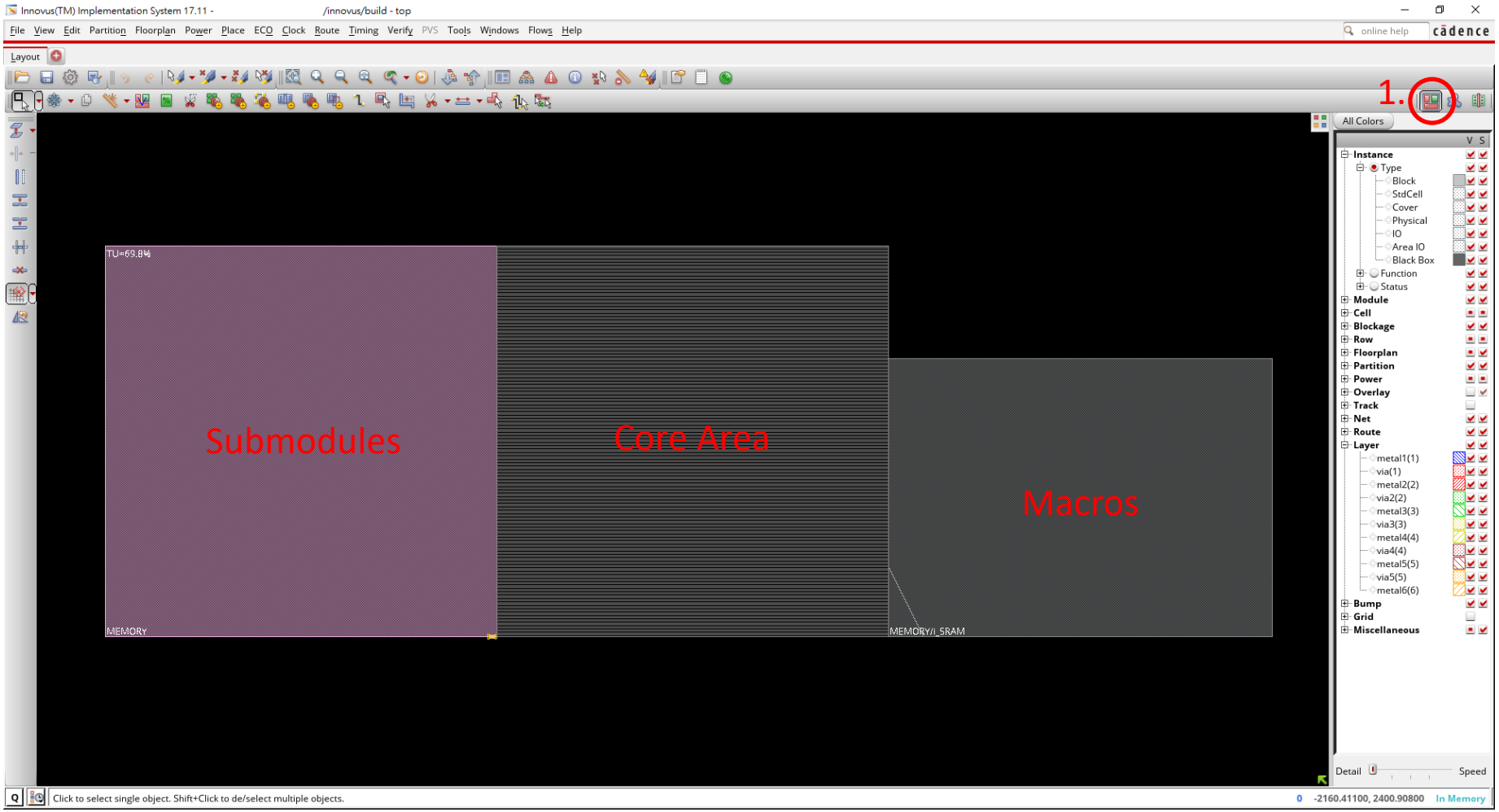
IO Pins(2/2)



Floorplan

Place the macro

First Floorplan View



Purpose and Set environment

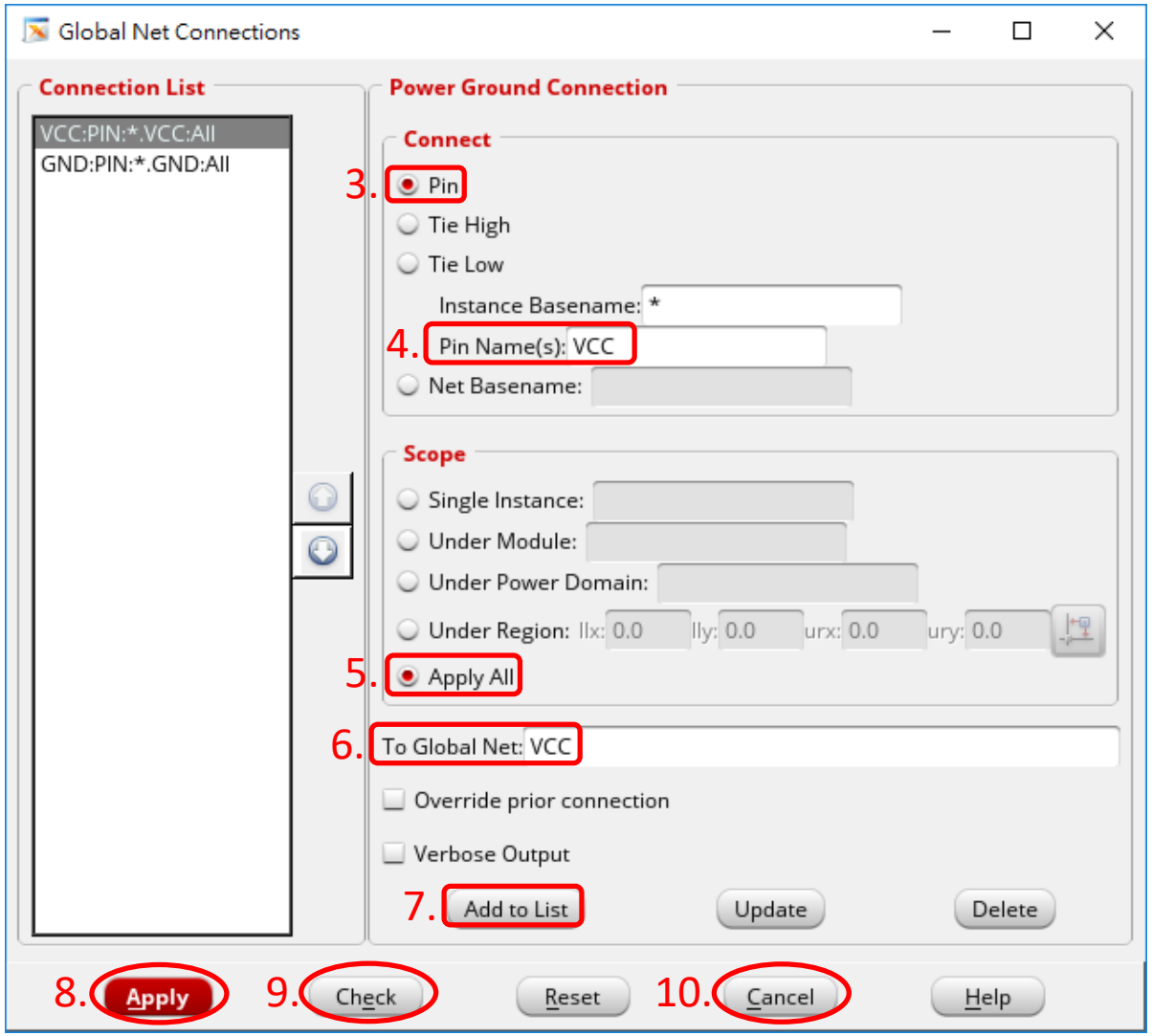
- Purposes
  - IO Pads locations, Power pads number and location
  - Macro placement, such as memory
  - Placement & Routing blockage
- Set environment
  - Remove assign statements from the Verilog

```
innovus 3> remove_assigns
```

  - Set process mode

```
innovus 4> setDesignMode -process 180
```

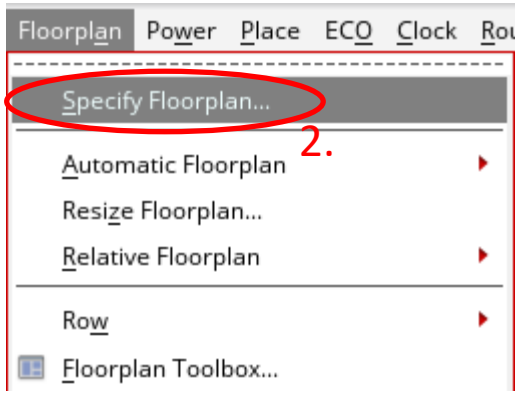
Connect Global Nets



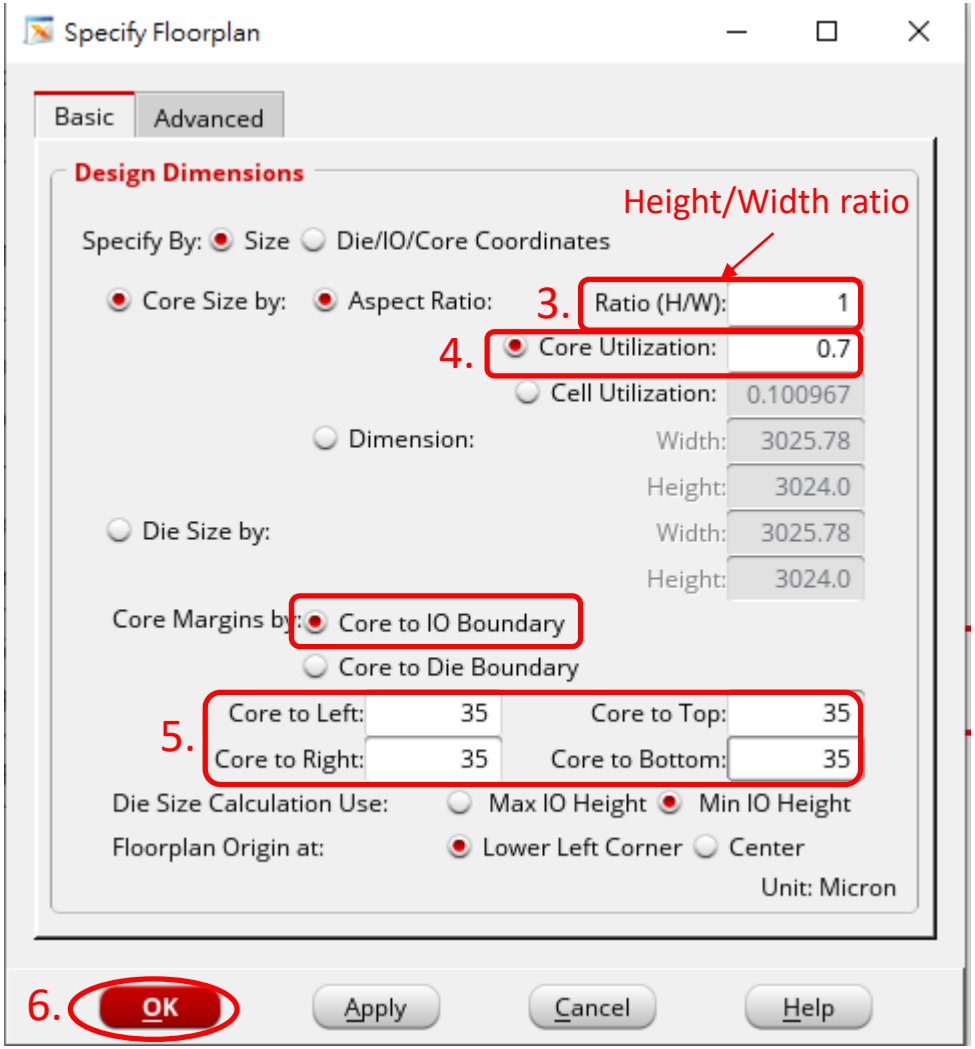
Repeat Step 3. -> 7.
First: VCC
Second: GND

Specify Floorplan

1.

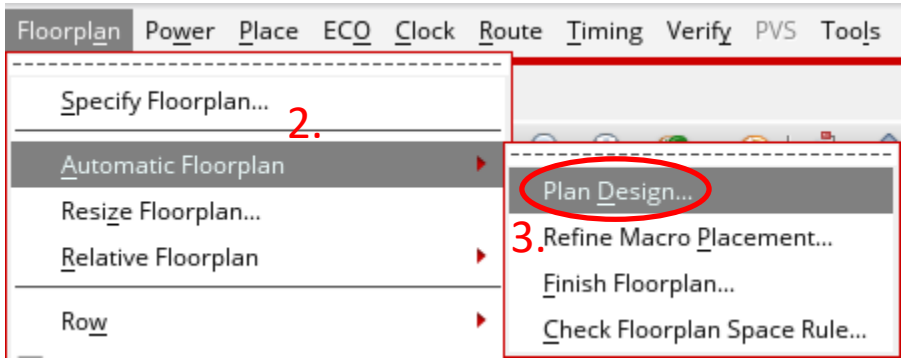


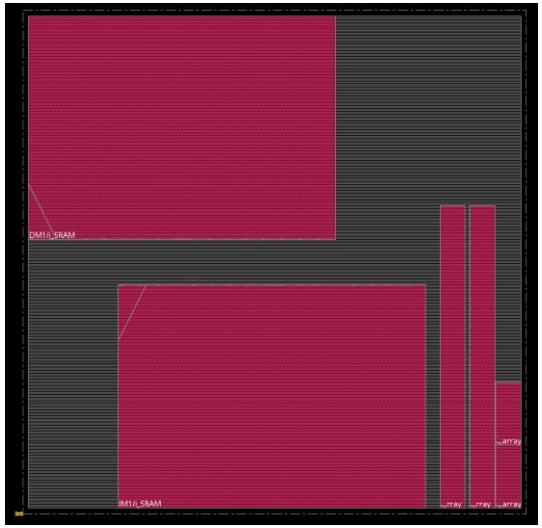
$$\text{Core utilization} = \frac{std\ cell + macro\ cell}{core\ area}$$



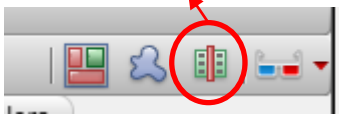
Plan Design(1/4)

1.

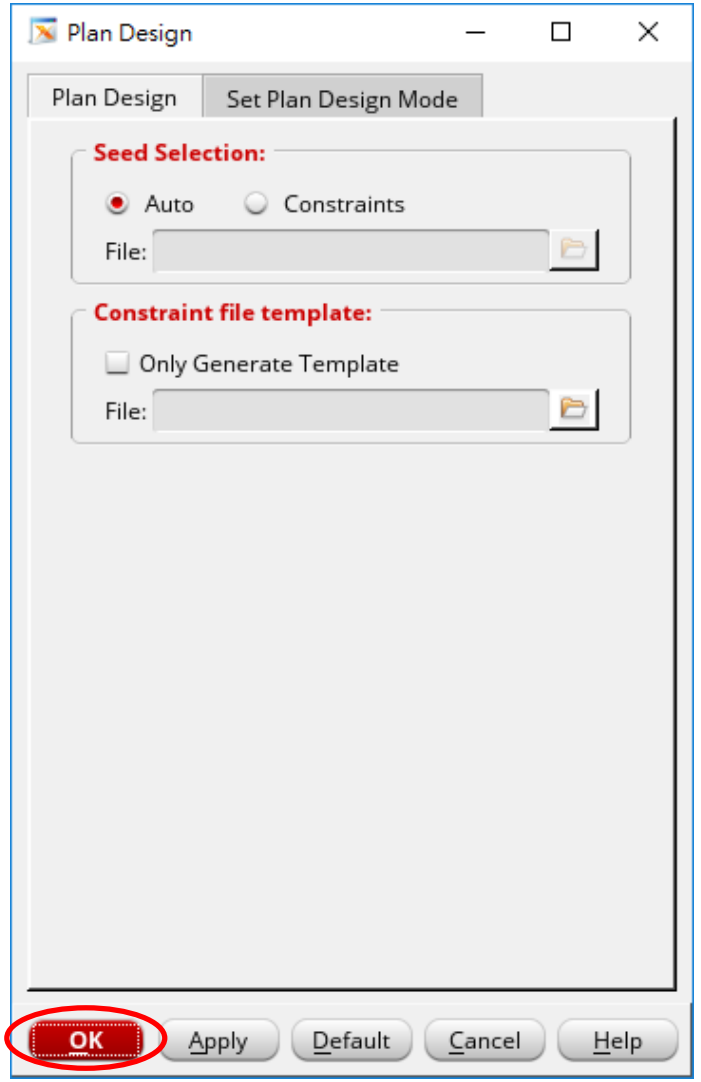




Result in physical view

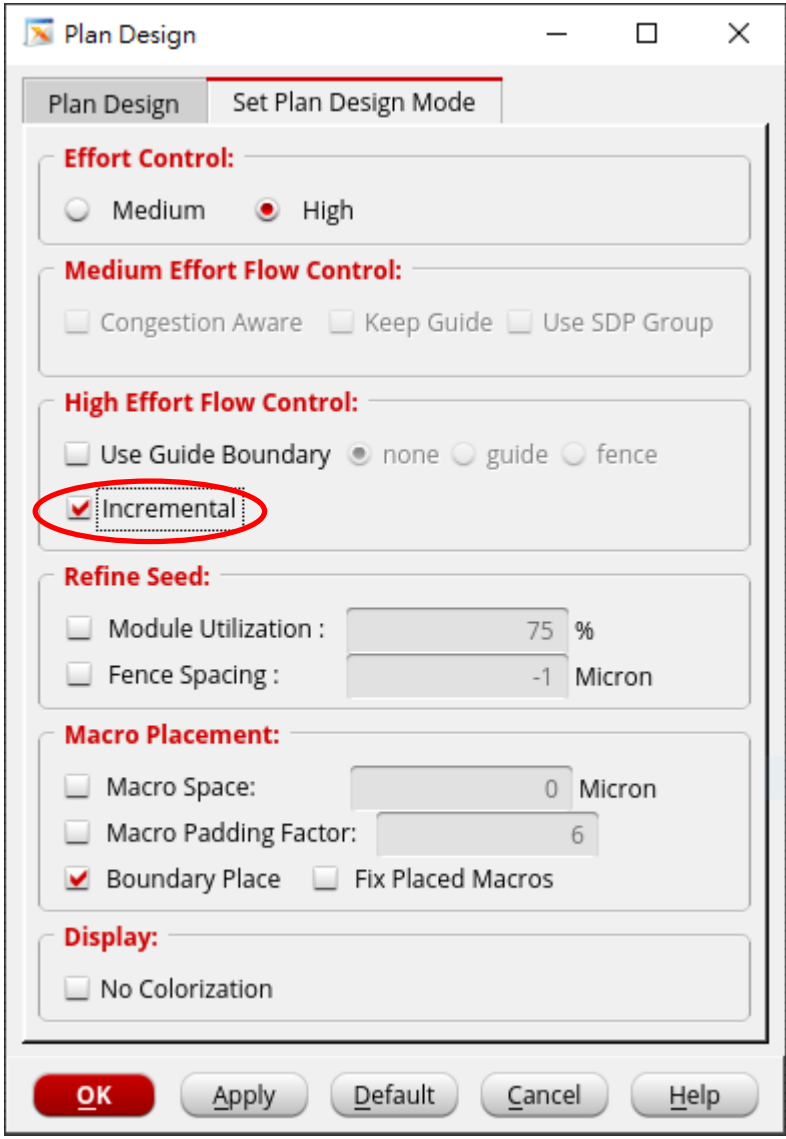


You can use this icon to move macro



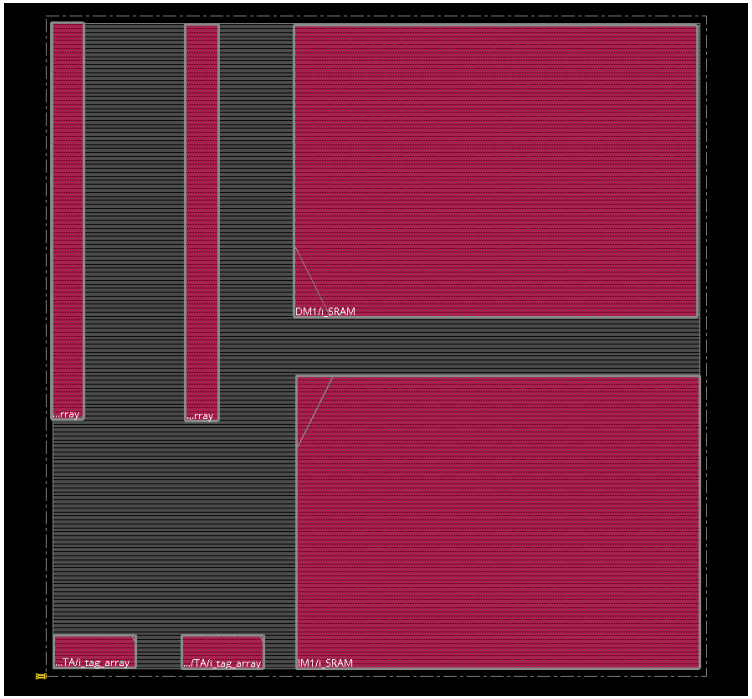
Plan Design(2/4)

- If the first-time placement is not what you prefer to be, you can use the "Incremental" option to re-allocate the location of macros based on the current placement
- With few times of incremental placement, the placement will be fix.



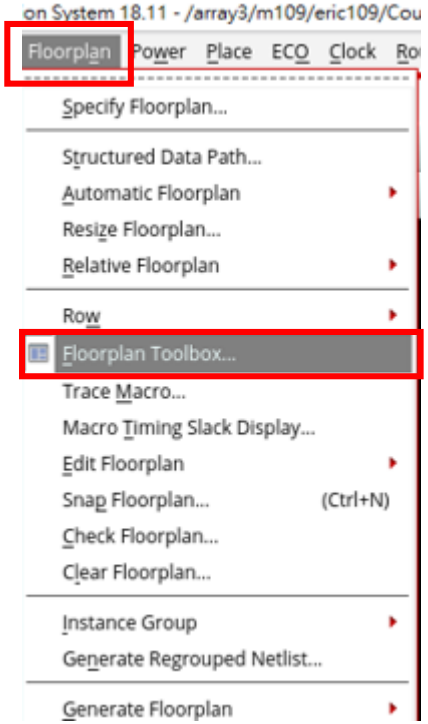
Plan Design(3/4)

- Tips for macro placement
  - Place macros around chip periphery
  - Consider connections to fixed cells
  - Orient macros to minimize distance between pins
  - Reserve space for power grid and signal routing and possible buffer insertion
  - Keep edges pf macros aligned if possible



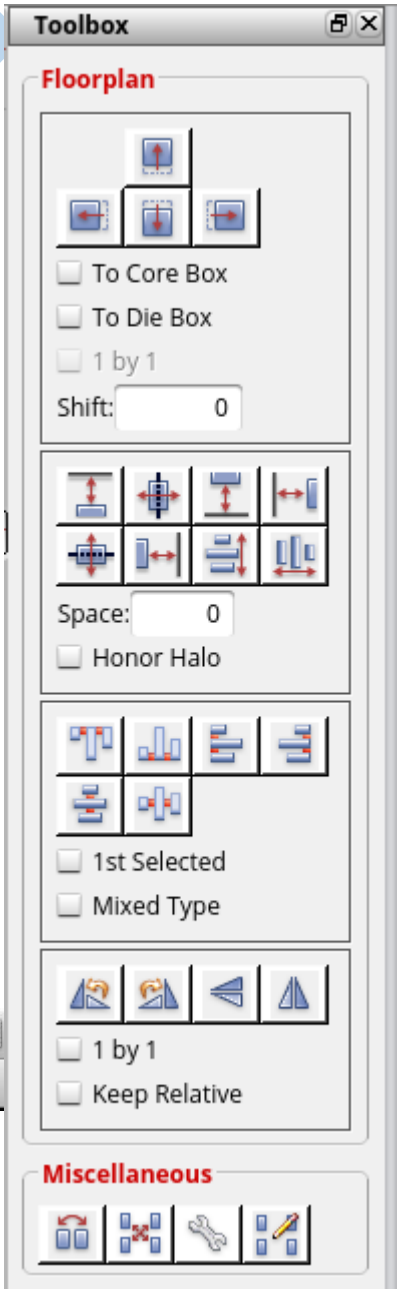
Plan Design(4/4)

Floorplan -> Floorplan Toolbox



- All kinds of tools
  - Shift
  - Spacing
  - Alignment
  - Rotation

Click the icon in Toolbox

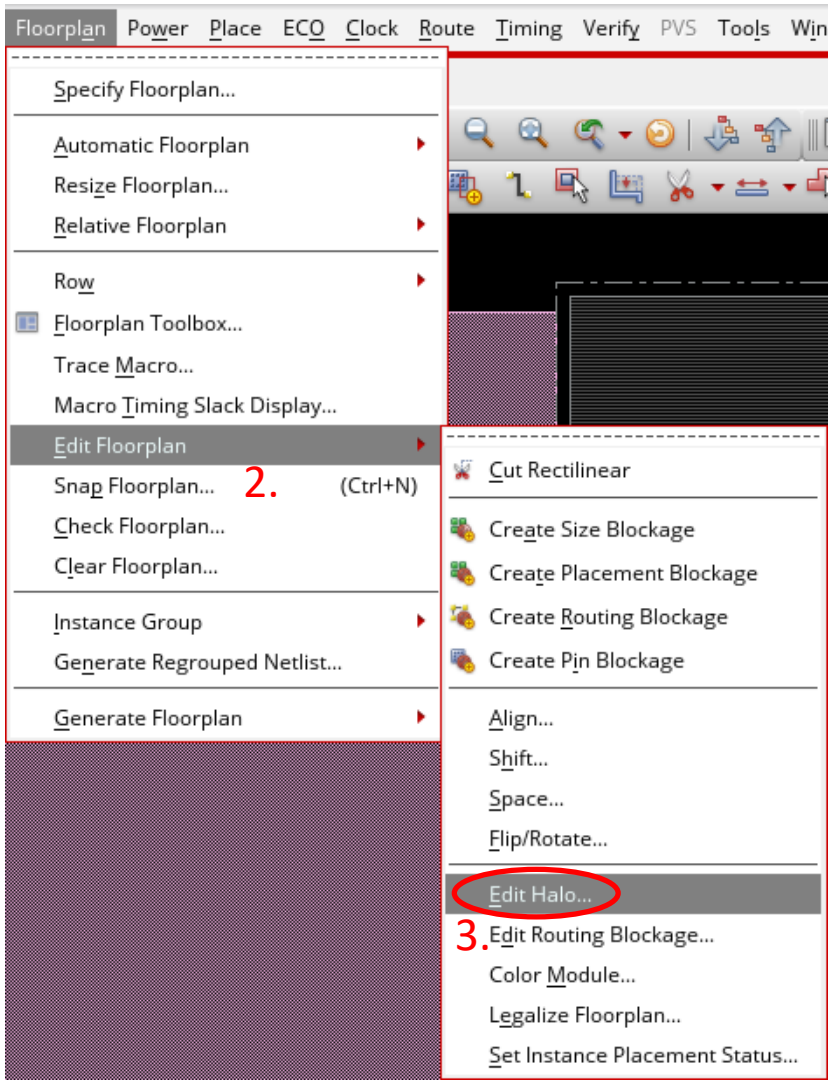


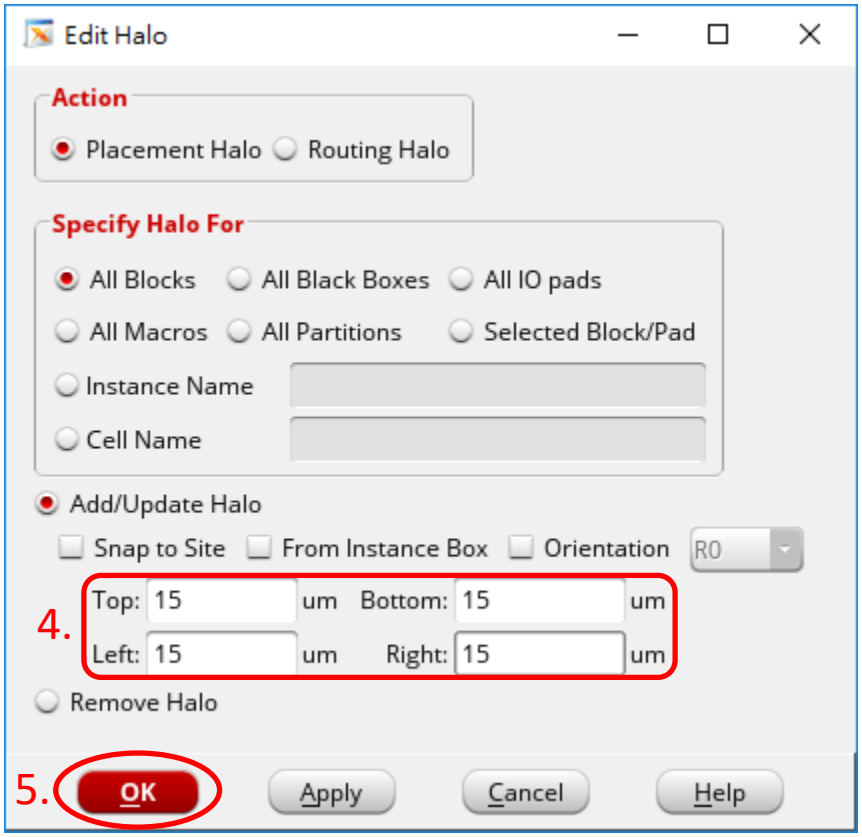
Add Halo

- Blockage is used to avoid unwanted wire in certain area
- Halo is the blockage for blocks such as memory
- Two types of Halo
  - Placement Halo
    - Prevent the placement of blocks and standard cells in order to reduce the congestion around blocks
  - Routing Halo
    - Reduce the possibility of long wire routing closed to the blocks
    - Long wire has higher cost and has DRC violations if too close to the blocks.

Add Placement Halo (1/2)

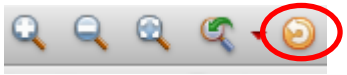
1.

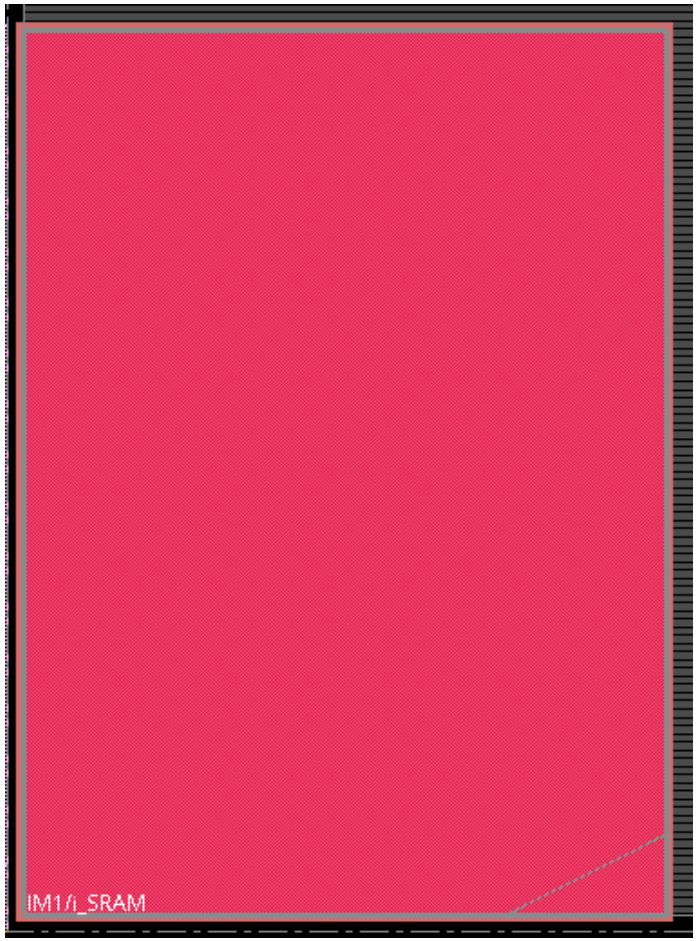




Add Placement Halo (1/2)

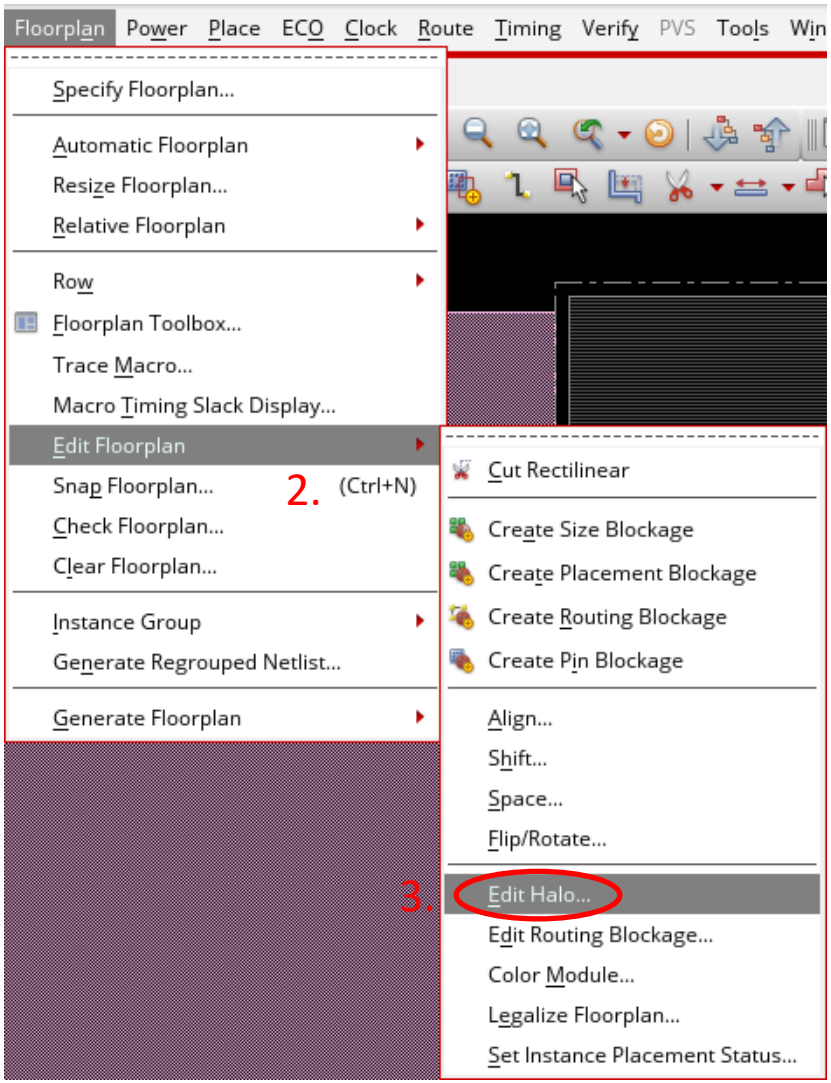
- Click redraw icon

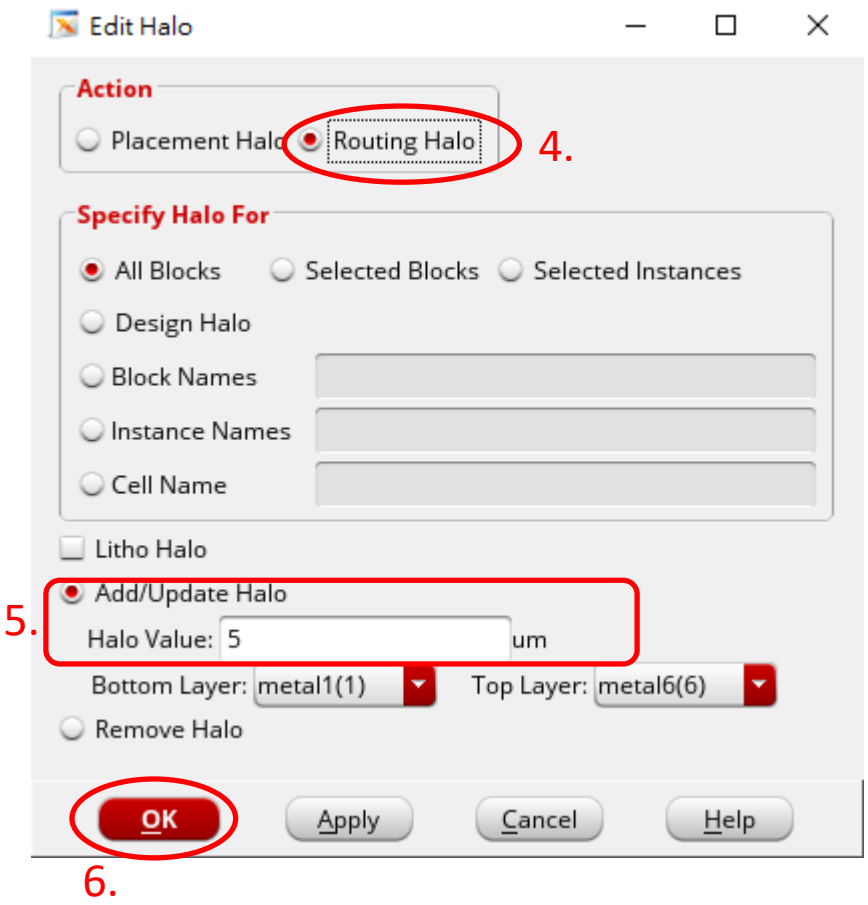




Add Routing Halo (1/2)

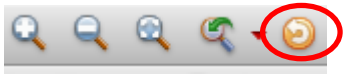
1.





Add Routing Halo (2/2)

- Click redraw icon



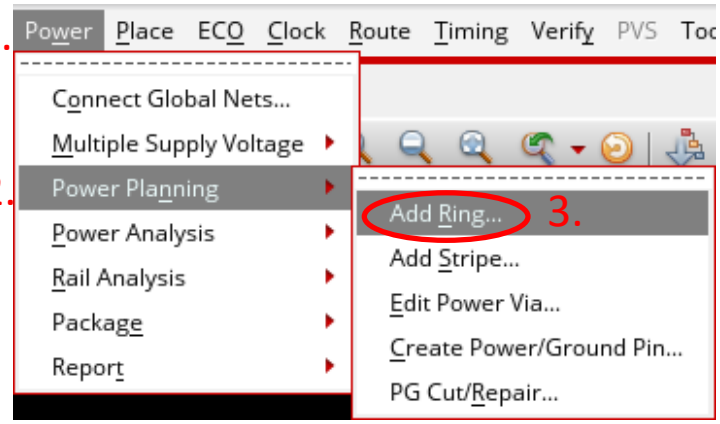
Powerplan

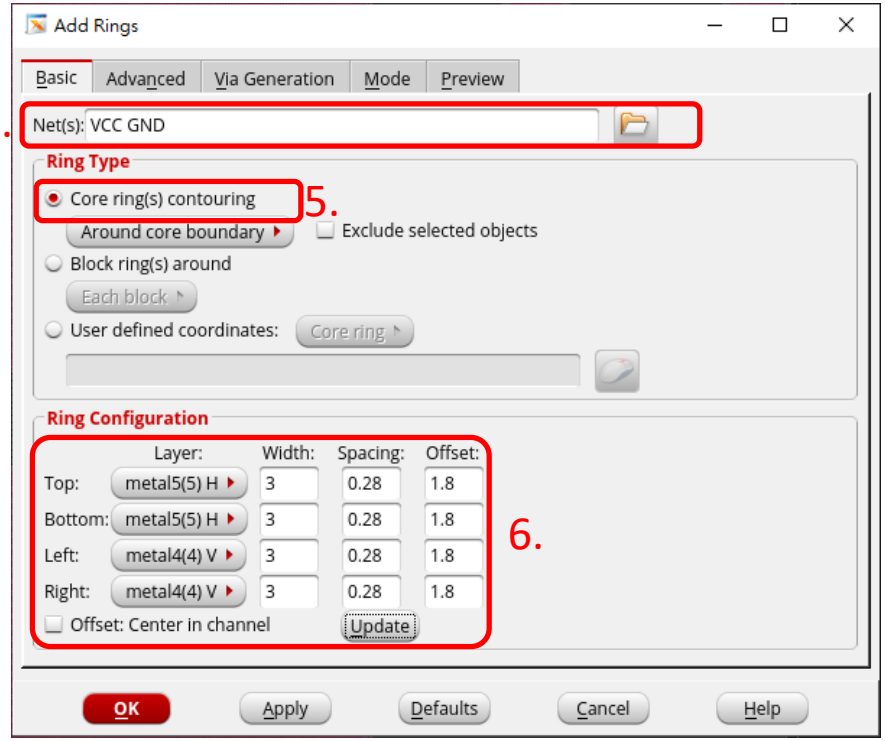
Place the power wires for all kinds of cells/blocks

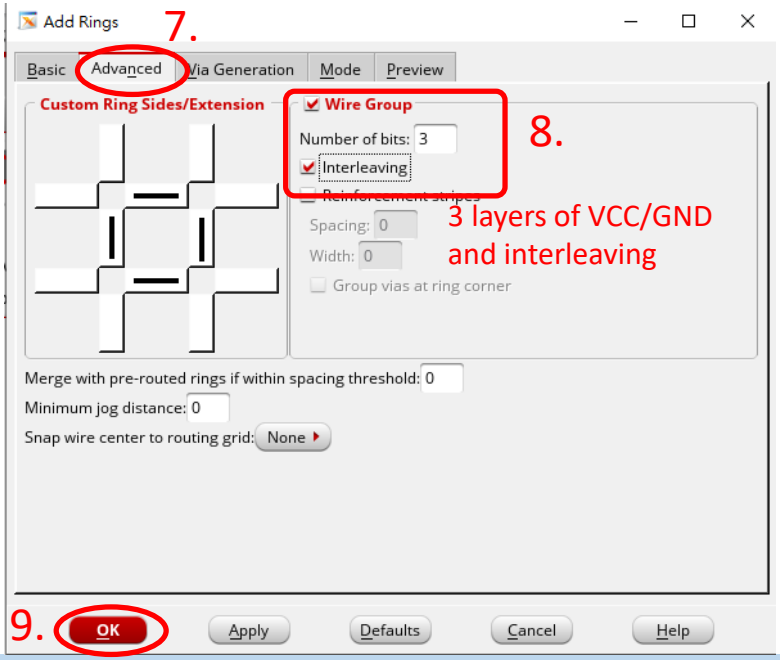
Power wire

- There are many types of power wire for different objectives.
- Core Ring
  - Power ring supply power from IO Pad for the core
- Block Ring
  - Power ring supply power from Core ring for the block
- Block Pins
  - Connect the block ring to the core ring
- Power Stripe
  - Additional power wires (same metal as ring) to reduce the IR drop
- Follow Pins
  - The power wires for standard cells

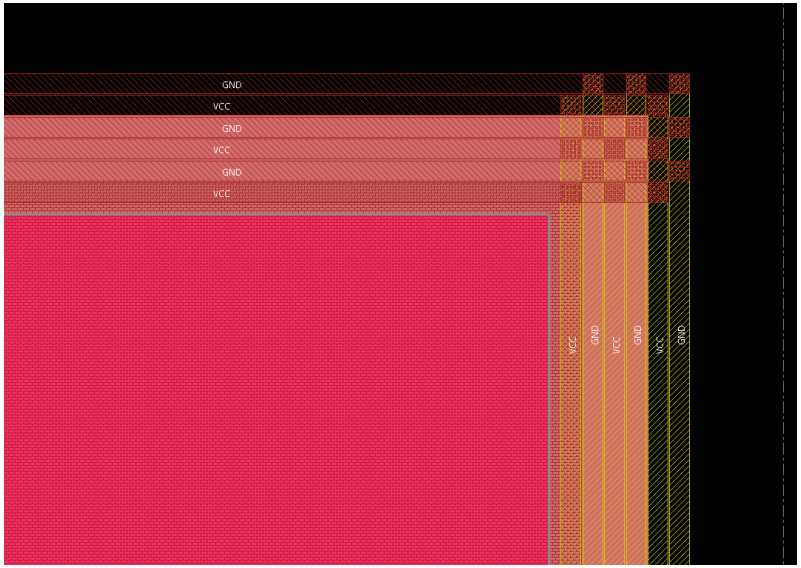
Create Core Ring(1/2)

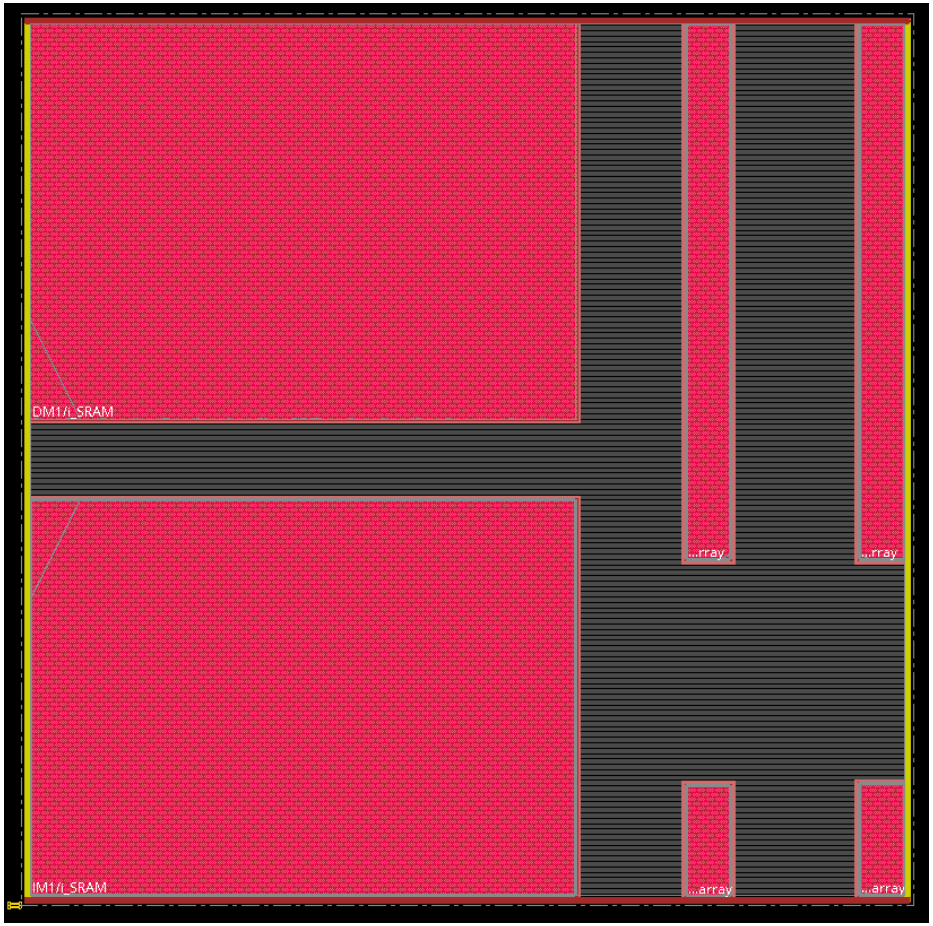






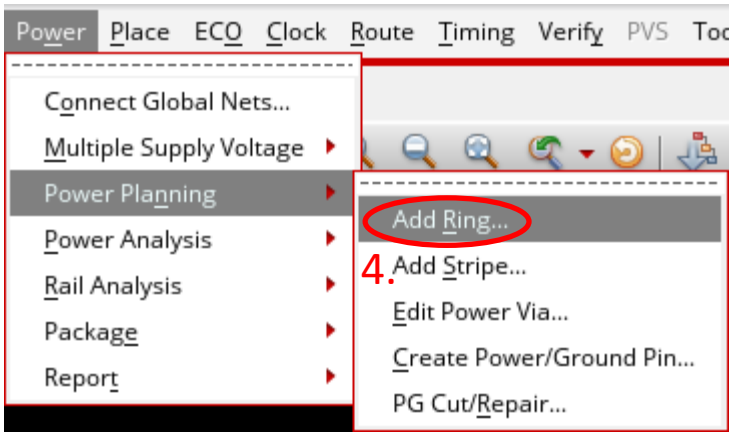
Create Core Ring(2/2)





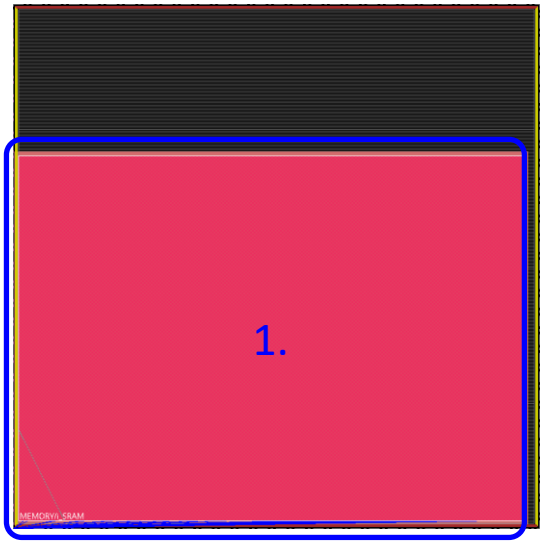
Create Block Ring (1/2)

2.

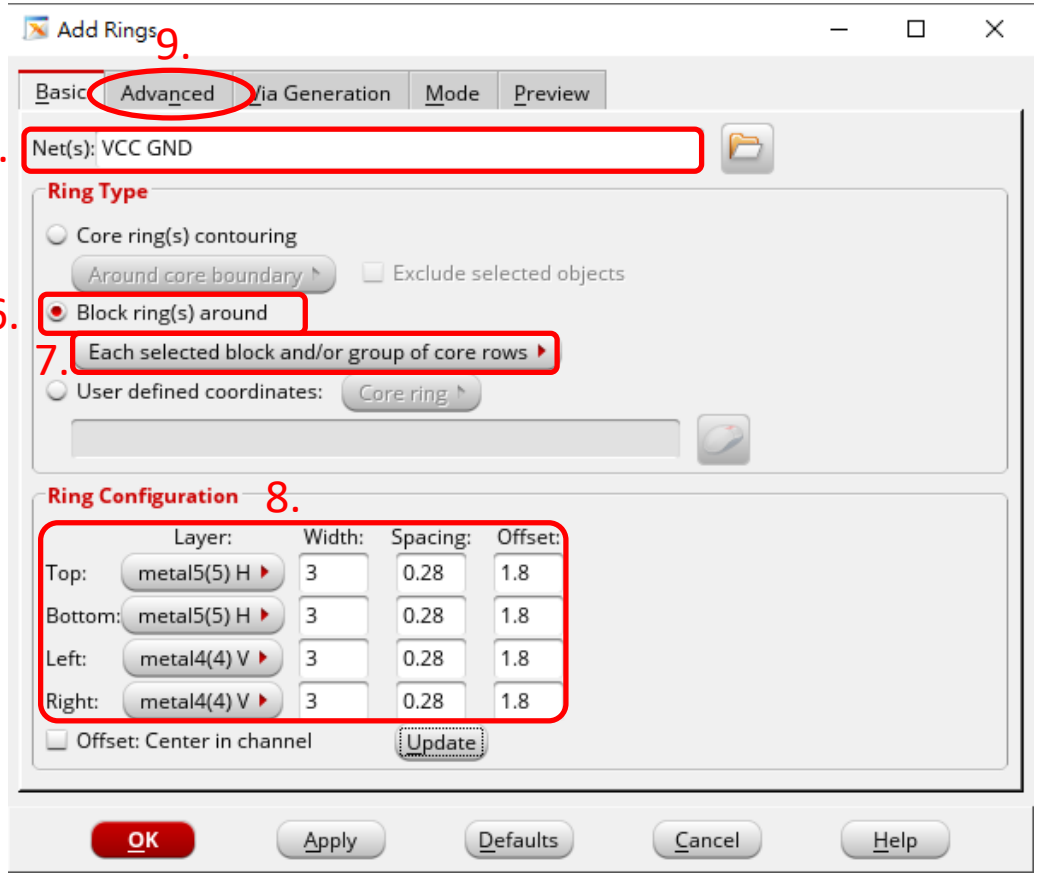


3.

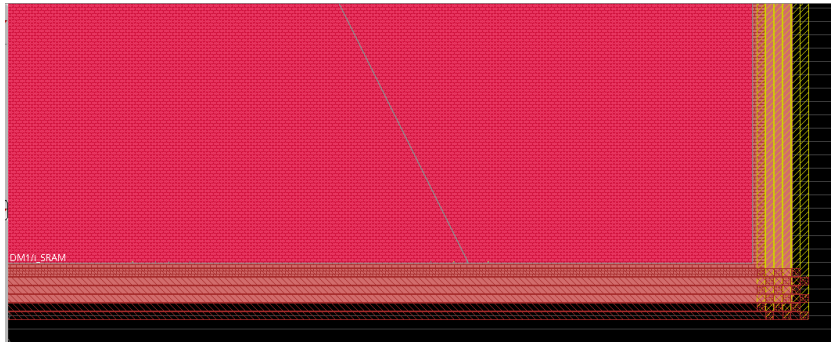
4.

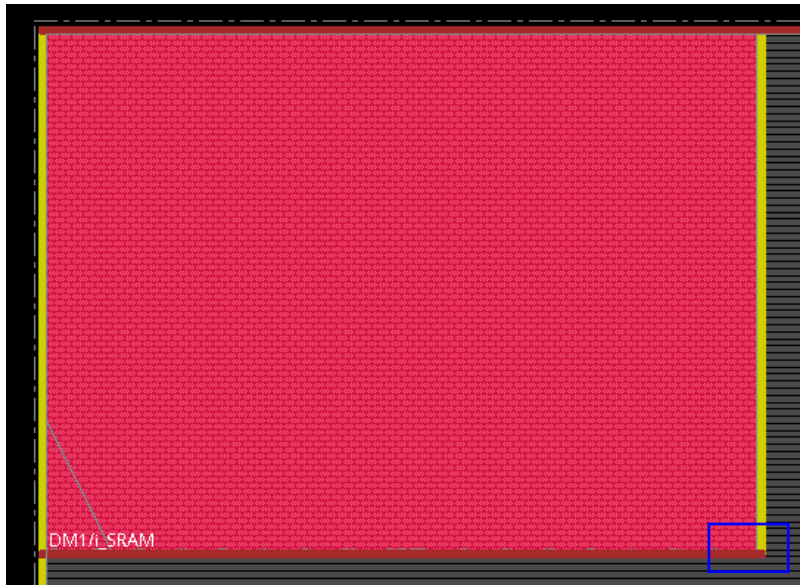


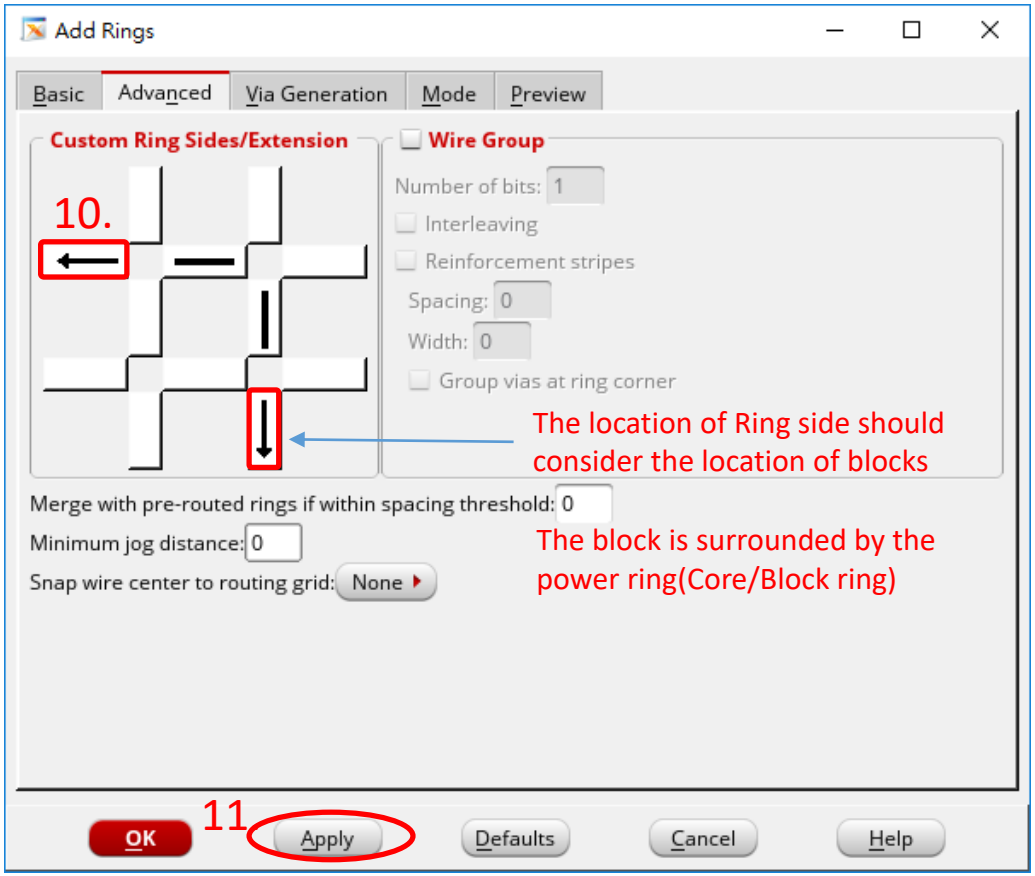
Select the block



Create Block Ring (2/2)

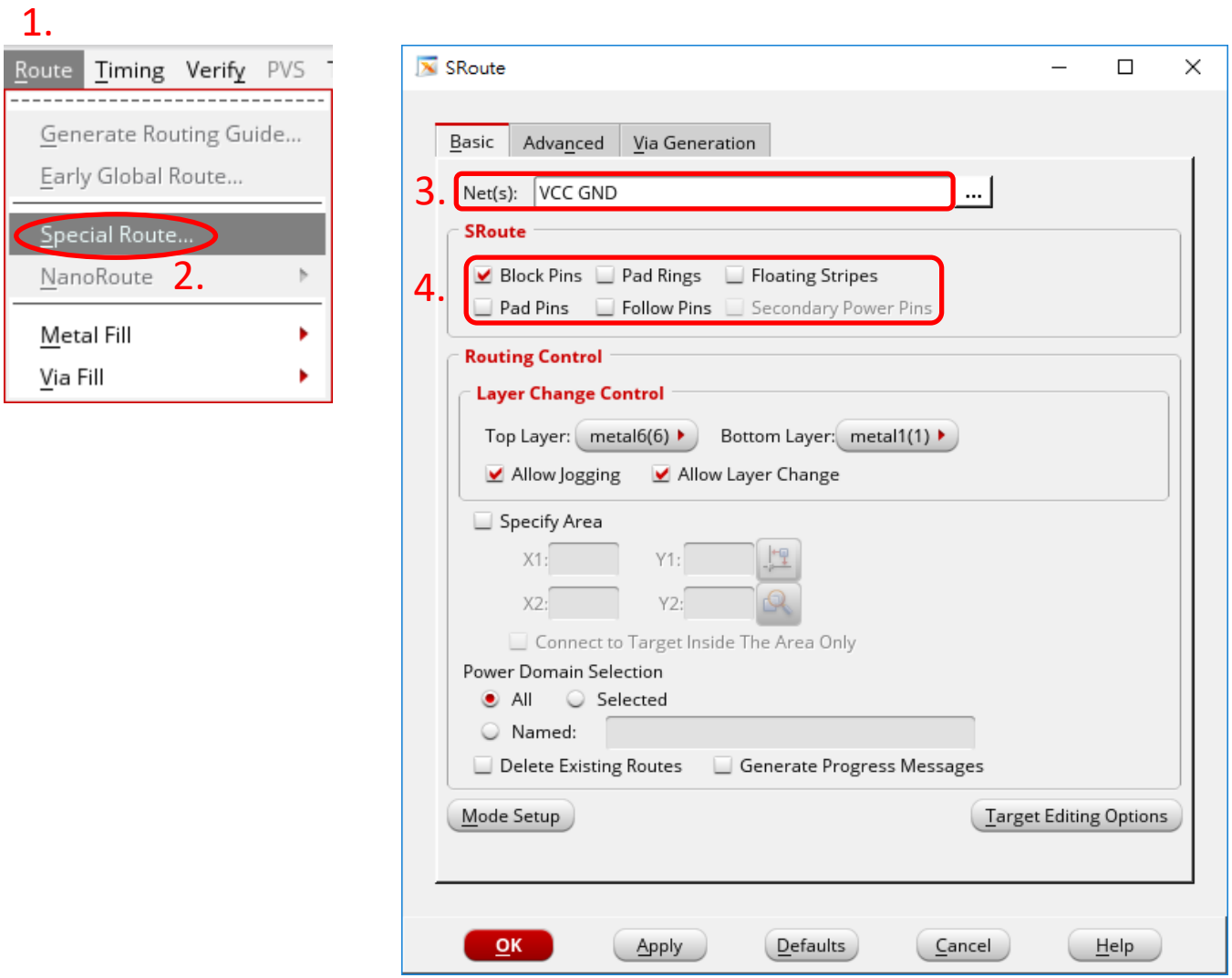




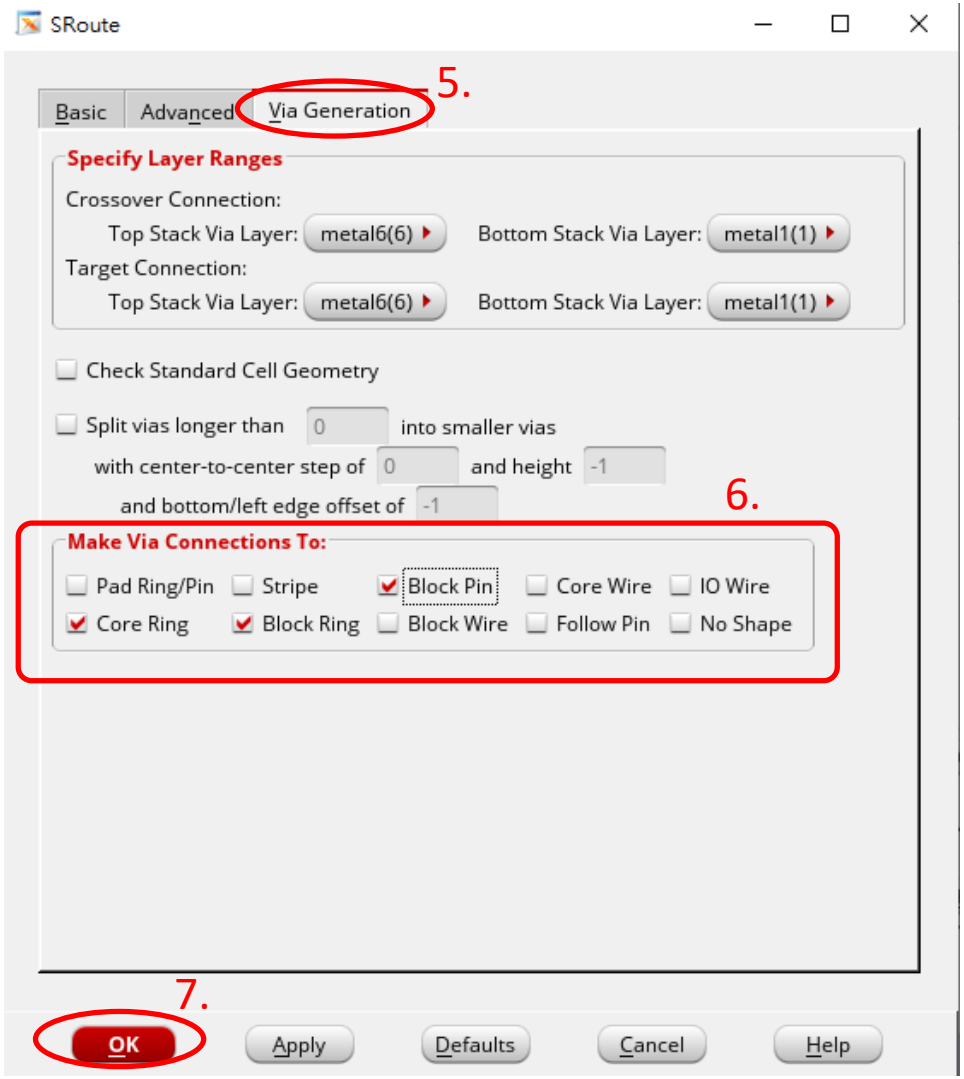


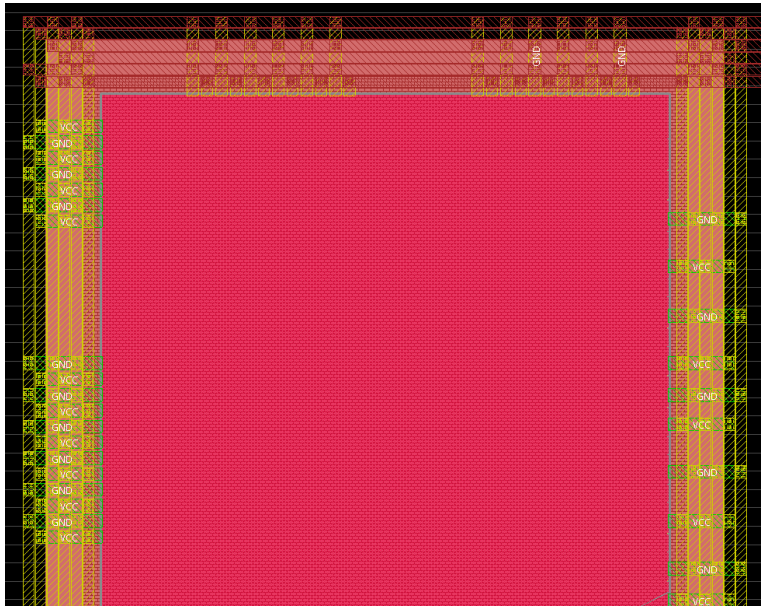
Repeat step 1~11 for all blocks

Connect Block Pins (1/2)



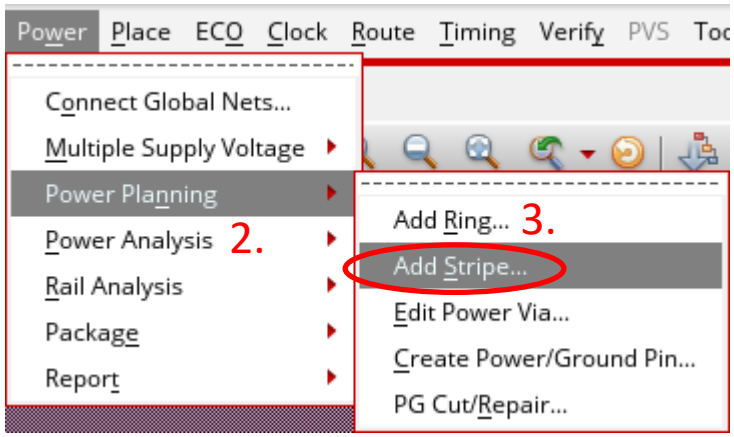
Connect Block Pins (2/2)

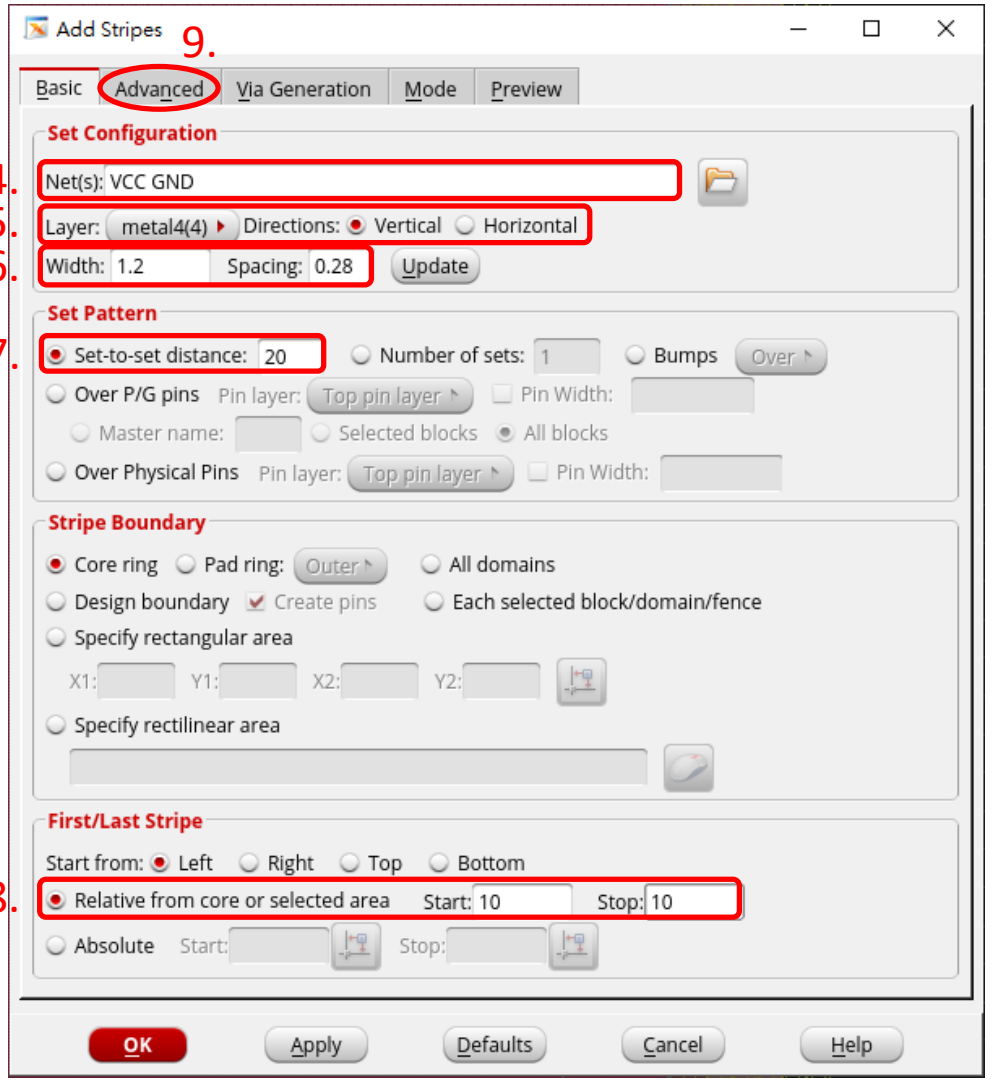




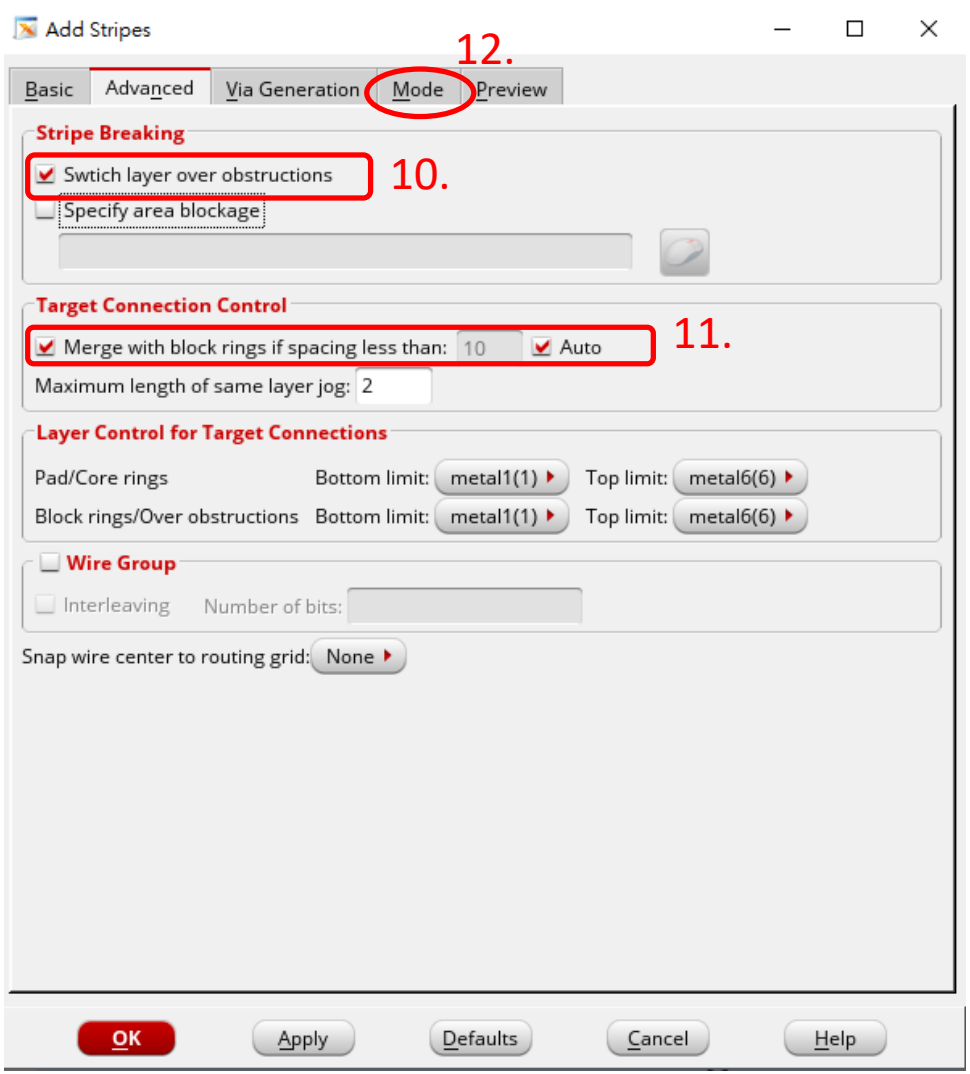
Create Power Stripe (1/3)

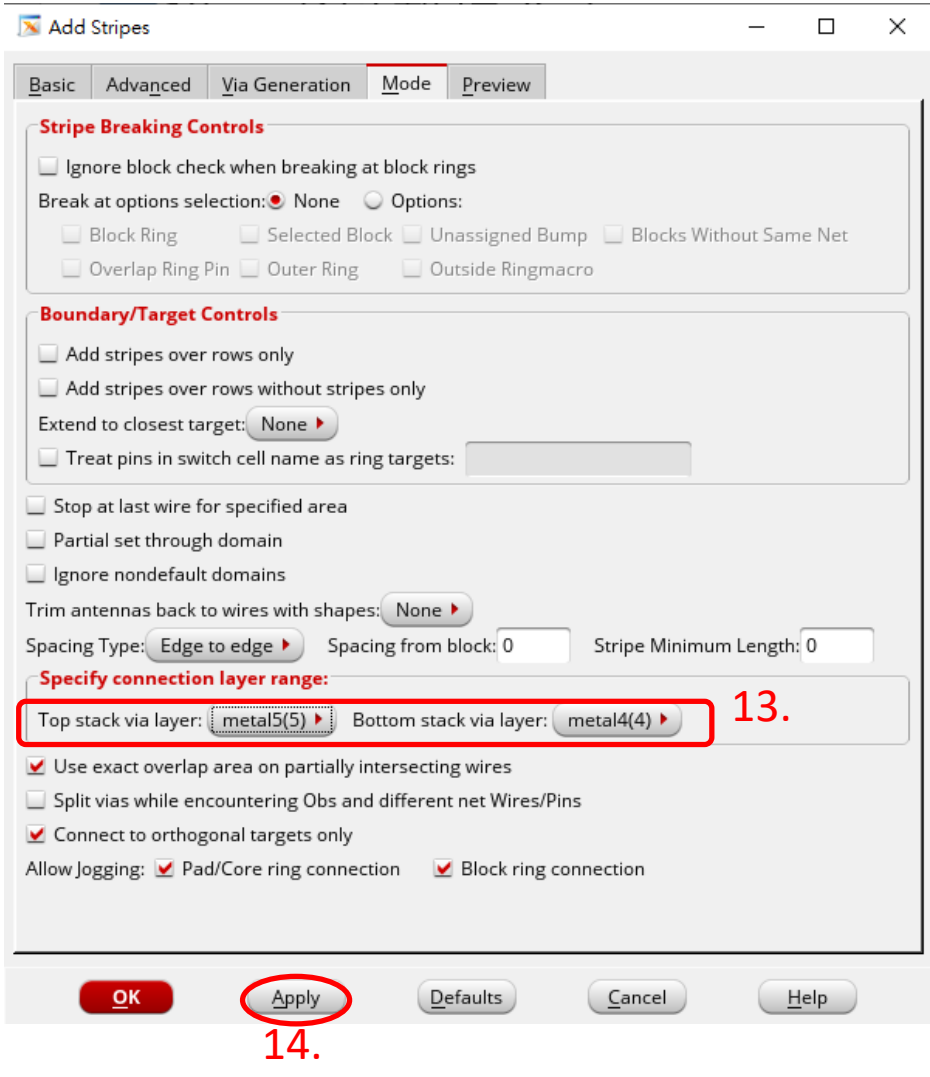
1.





Create Power Stripe (2/3)

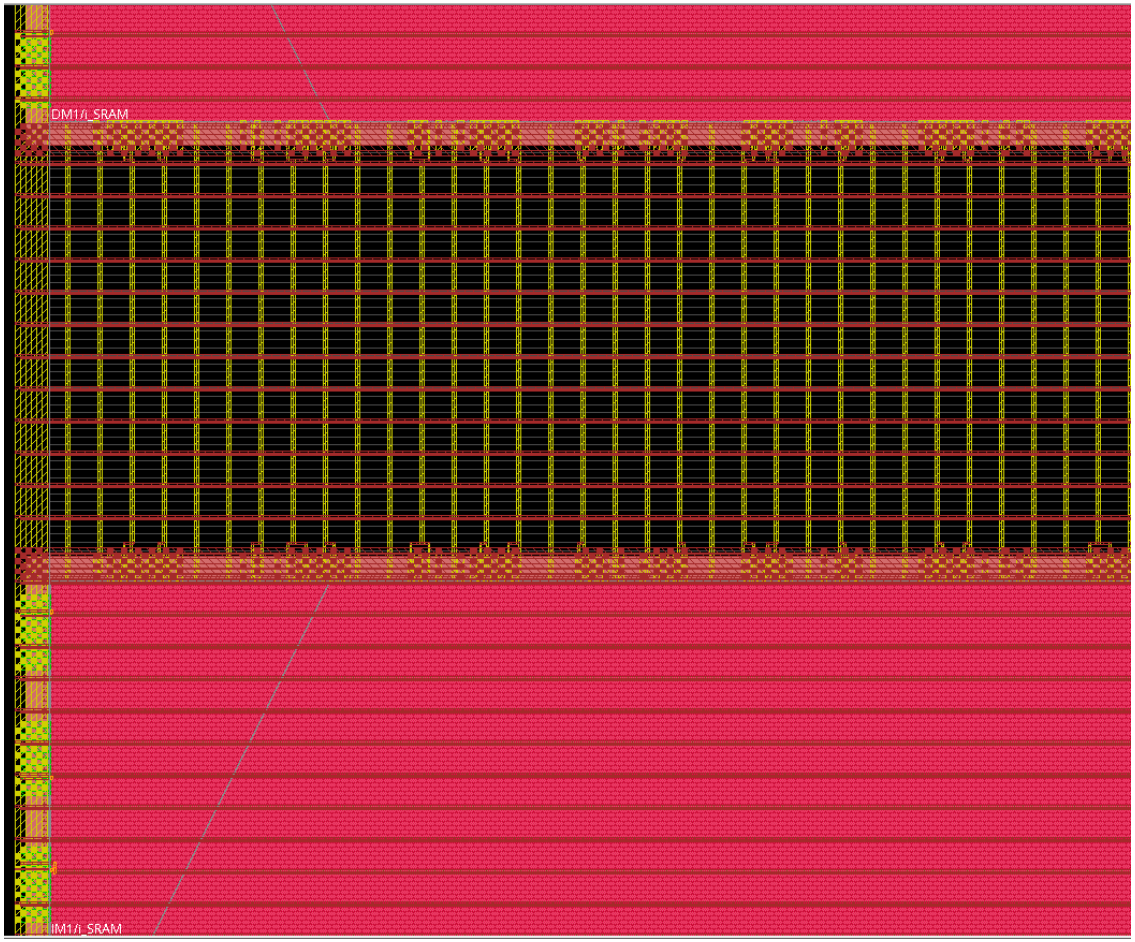




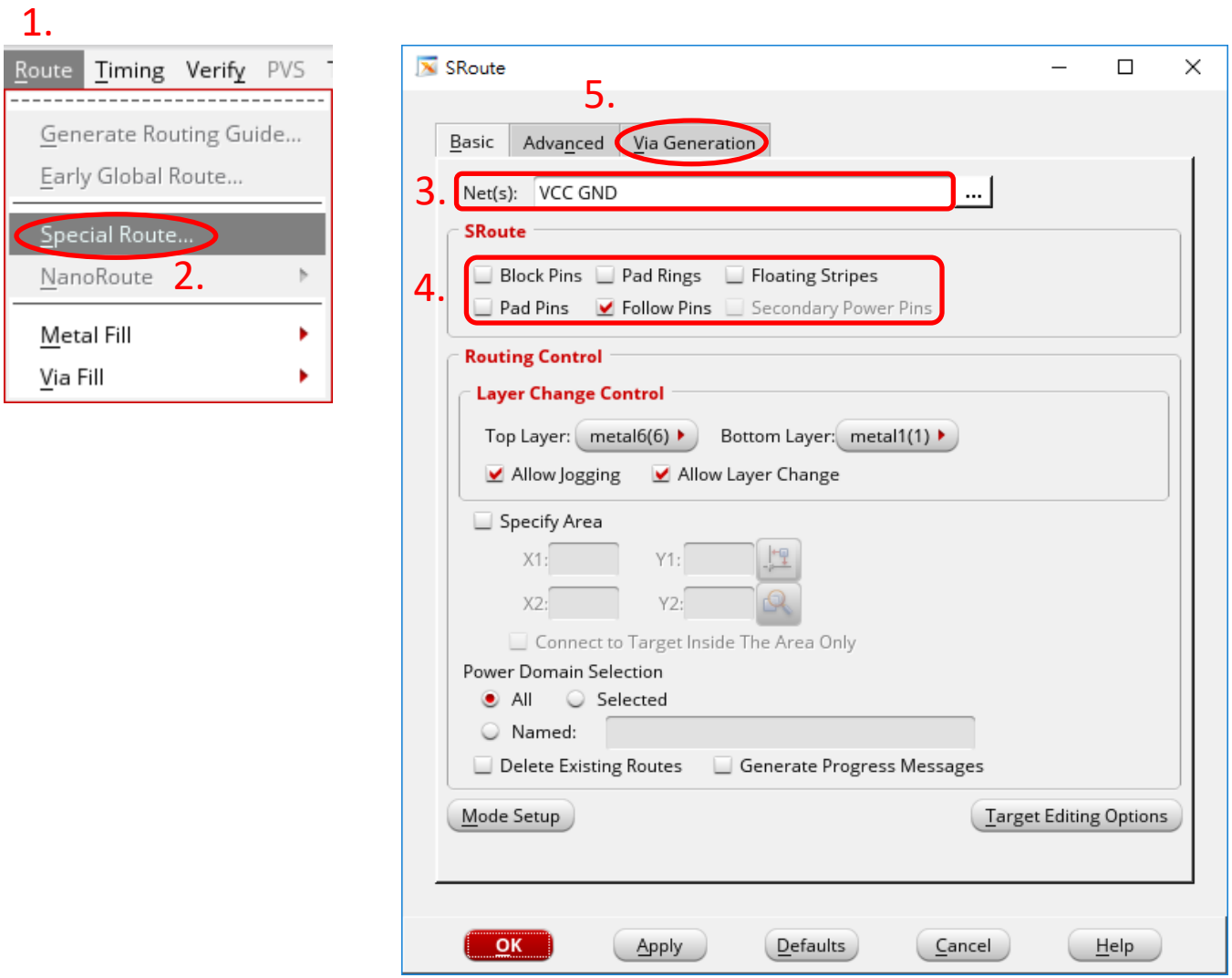
Create Power Stripe (3/3)

Repeat Step 5. -> 14.

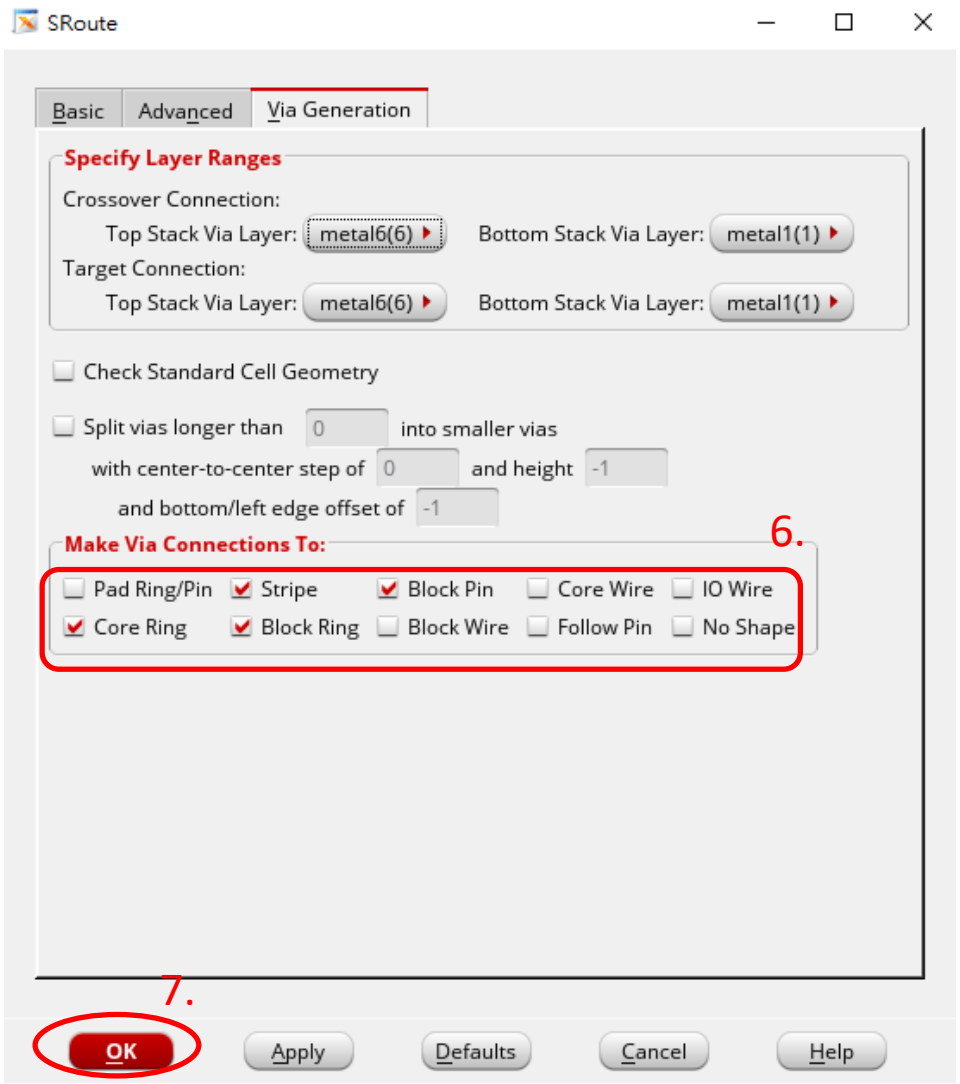
- First: metal 4 / Vertical
- Second: metal 5 / Horizontal

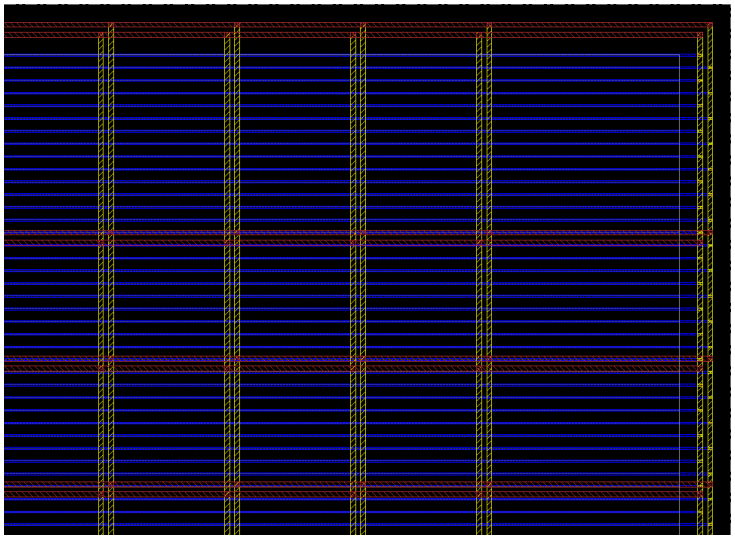


Connect Follow Pins (1/2)



Connect Follow Pins (2/2)

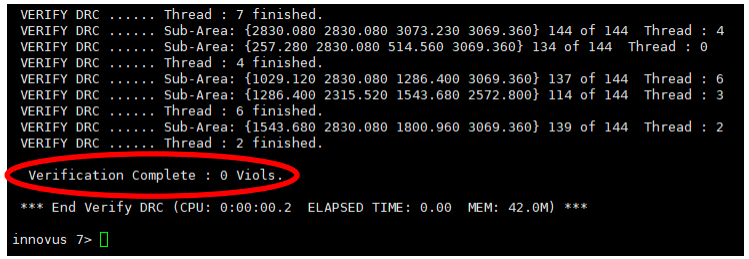


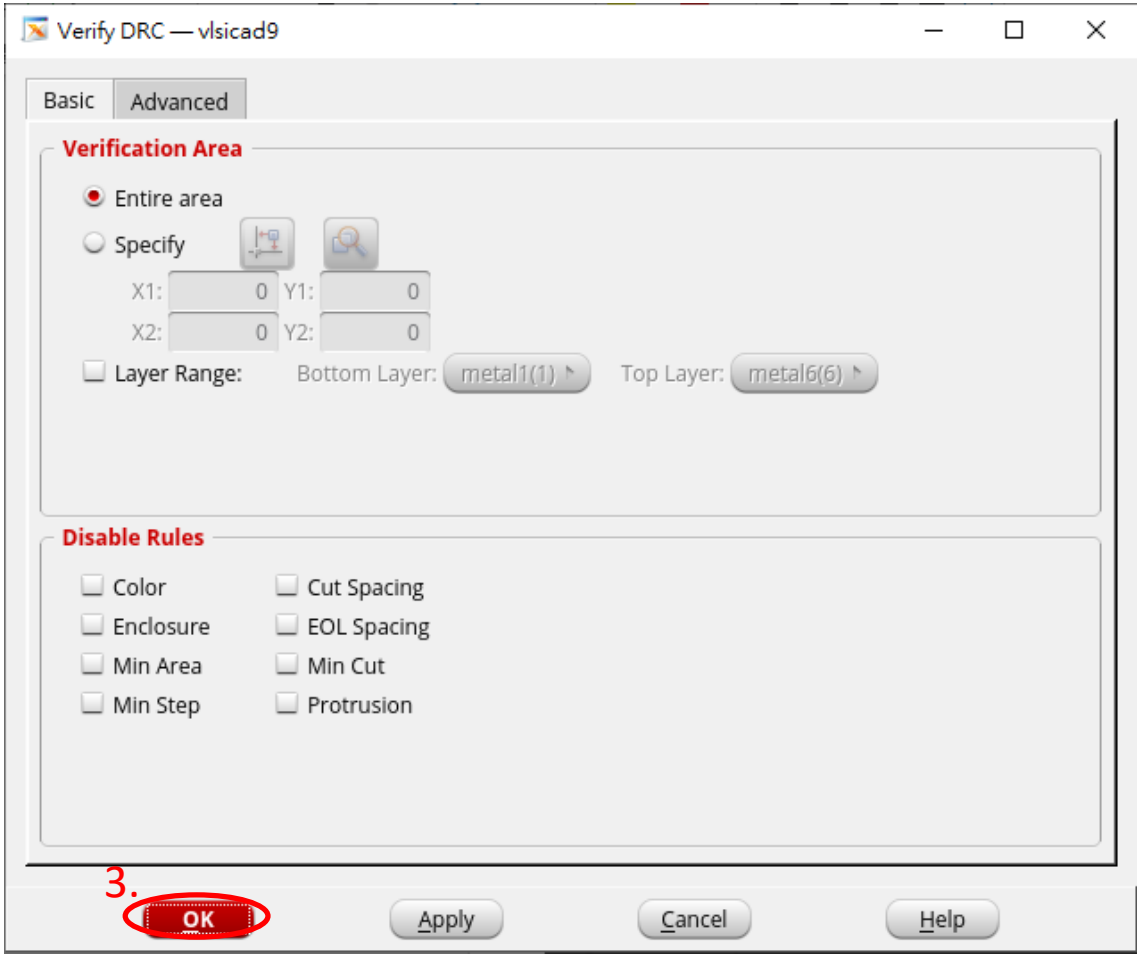


Verify DRC

1.

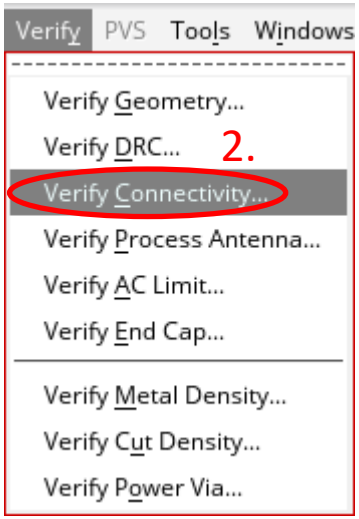

Verify
Pegasus
Tools
Window
Verify DRC...
Verify Connectivity...
Verify Process Antenna...
Verify AC Limit...
Verify End Cap...
Verify Metal Density...
Verify Cut Density...
Verify Power Via...
2.


VERIFY DRC ..... Thread : 7 finished.
VERIFY DRC ..... Sub-Area: {2830.080 2830.080 3073.230 3069.360} 144 of 144 Thread : 4
VERIFY DRC ..... Sub-Area: {257.280 2830.080 514.560 3069.360} 134 of 144 Thread : 0
VERIFY DRC ..... Thread : 4 finished.
VERIFY DRC ..... Sub-Area: {1029.120 2830.080 1286.400 3069.360} 137 of 144 Thread : 6
VERIFY DRC ..... Sub-Area: {1286.400 2315.520 1543.680 2572.800} 114 of 144 Thread : 3
VERIFY DRC ..... Thread : 6 finished.
VERIFY DRC ..... Sub-Area: {1543.680 2830.080 1800.960 3069.360} 139 of 144 Thread : 2
VERIFY DRC ..... Thread : 2 finished.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:00.2 ELAPSED TIME: 0.00 MEM: 42.0M) ***
innovus 7>

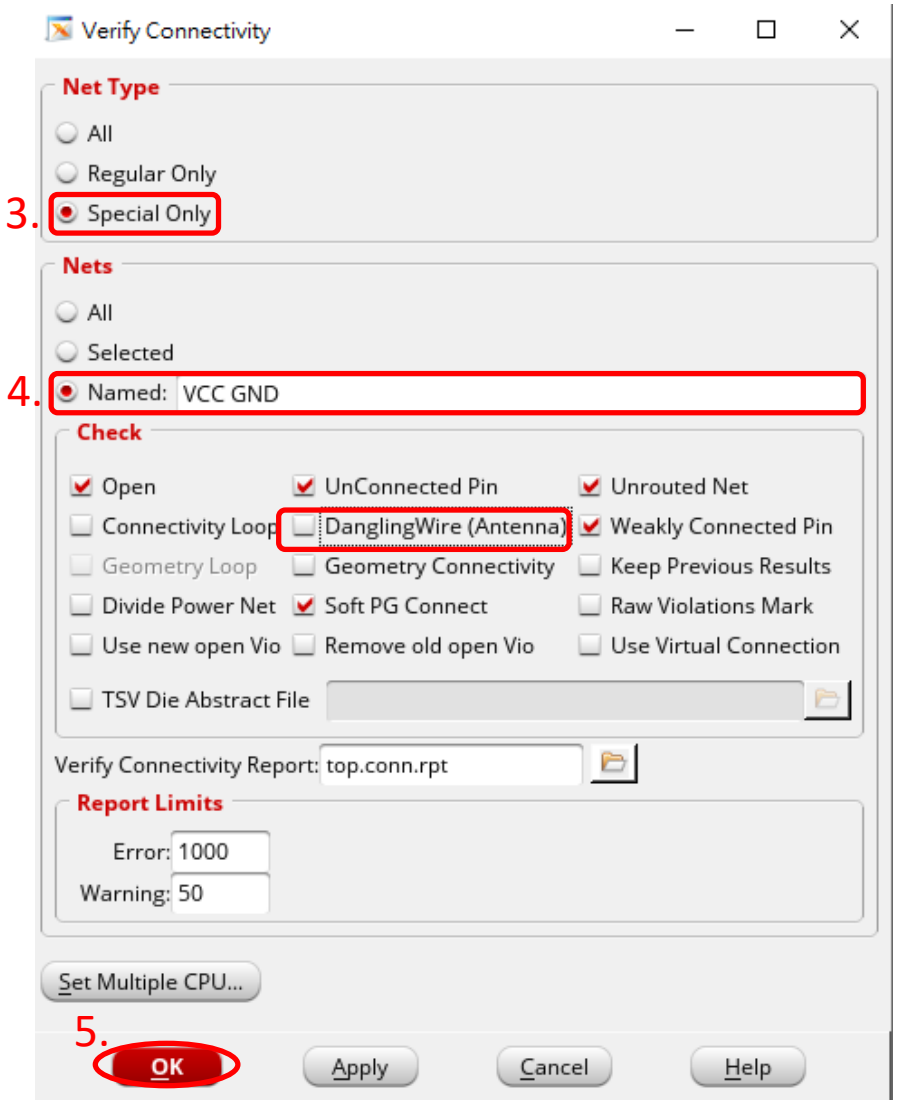

Verify DRC — vlsicad9
Basic
Advanced
Verification Area
Entire area
Specify
X1: 0 Y1: 0
X2: 0 Y2: 0
Layer Range:
Bottom Layer: metal1(1)
Top Layer: metal6(6)
Disable Rules
Color
Cut Spacing
Enclosure
EOL Spacing
Min Area
Min Cut
Min Step
Protrusion
3.
OK
Apply
Cancel
Help

Verify Connectivity

1.




```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.5  MEM: 10.723M)
```



Placement

Place the standard cell

Place Standard Cells

- Placement + pre-CTS Optimization

```
innovus 10> place_opt_design
```

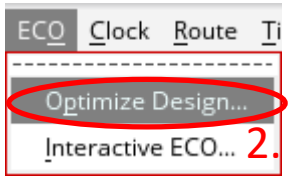
- Check timing report

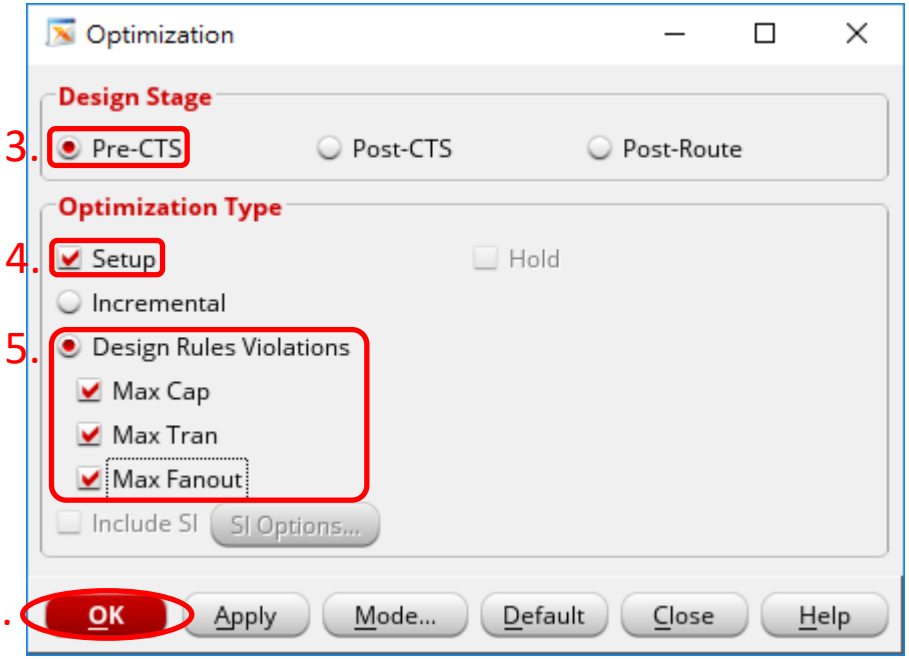
```
+--------------------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | default |
+--------------------+---------+---------+---------+---------+
|           WNS (ns):|  0.001  |  0.001  |  3.791  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |
|          All Paths:|  4010   |  2292   |  1818   |    0    |
+--------------------+---------+---------+---------+---------+
```

If worst negative slacks (WNS) < 0, you need to optimize design

Optimize Design (Optional)

1.





If worst negative slacks (WNS) < 0, you need to optimize design

Clock Tree Synthesis

Create the clock tree which is the most important in the design

CCOpt

- Clock Concurrent Optimization
  - Create the clock tree and optimize the design at the same time

```
innovus 3> source ../script/ccopt.tcl
```

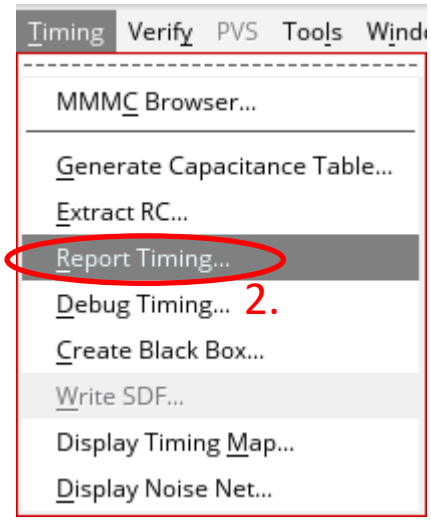
- Two steps
  - CCOpt design
  - Setup & hold time optimization

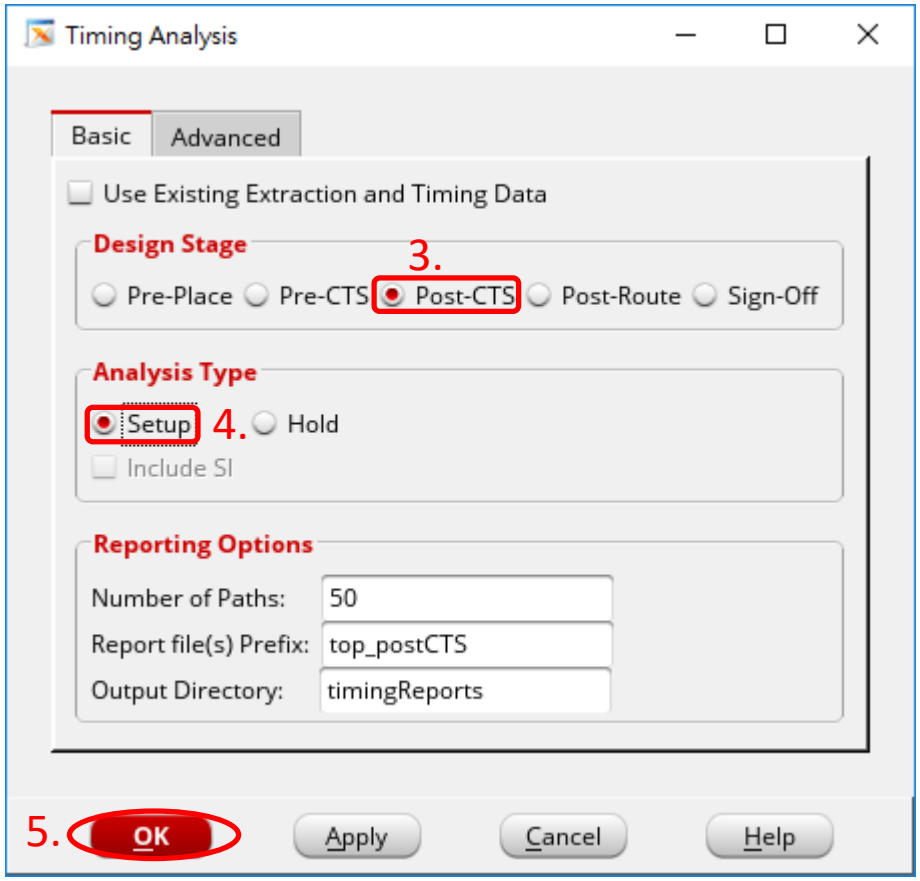
```
Runtime Summary
===============
Clock Runtime:  (63%) Core CTS          7.53 (Init 5.61, Construction 1.45, Implementation 0.11, eGRPC 0.16, PostConditioning 0.04, Other 0.16)
Clock Runtime:  (31%) CTS services      3.73 (RefinePlace 0.44, EarlyGlobalClock 0.60, NanoRoute 2.40, ExtractRC 0.26, TimingAnalysis 0.03)
Clock Runtime:   (5%) Other CTS         0.68 (Init 0.36, CongRepair 0.31)
Clock Runtime: (100%) Total            11.93

Synthesizing clock trees with CCOpt done.
**WARN: (IMPSP-9025):   No scan chain specified/traced.
Type 'man IMPSP-9025' for more detail.

*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   IMPEXT-3530          5  The process node is not set. Use the com...
WARNING   IMPESI-3086          1  The cell '%s' does not have characterize...
WARNING   IMPSP-9025           1  No scan chain specified/traced.
WARNING   IMPCCOPT-1361        3  Routing configuration for %s nets in clo...
ERROR     IMPCCOPT-5054        1  Net %s is not completely connected after...
WARNING   IMPCCOPT-2015        2  %s will not update I/O latencies for the...
WARNING   IMPTCM-77            1  Option "%s" for command %s is obsolete a...
*** Message Summary: 13 warning(s), 1 error(s)
```

ERROR IMPCCOPT-5054 can be ignored

Report Timing - Setup

1.

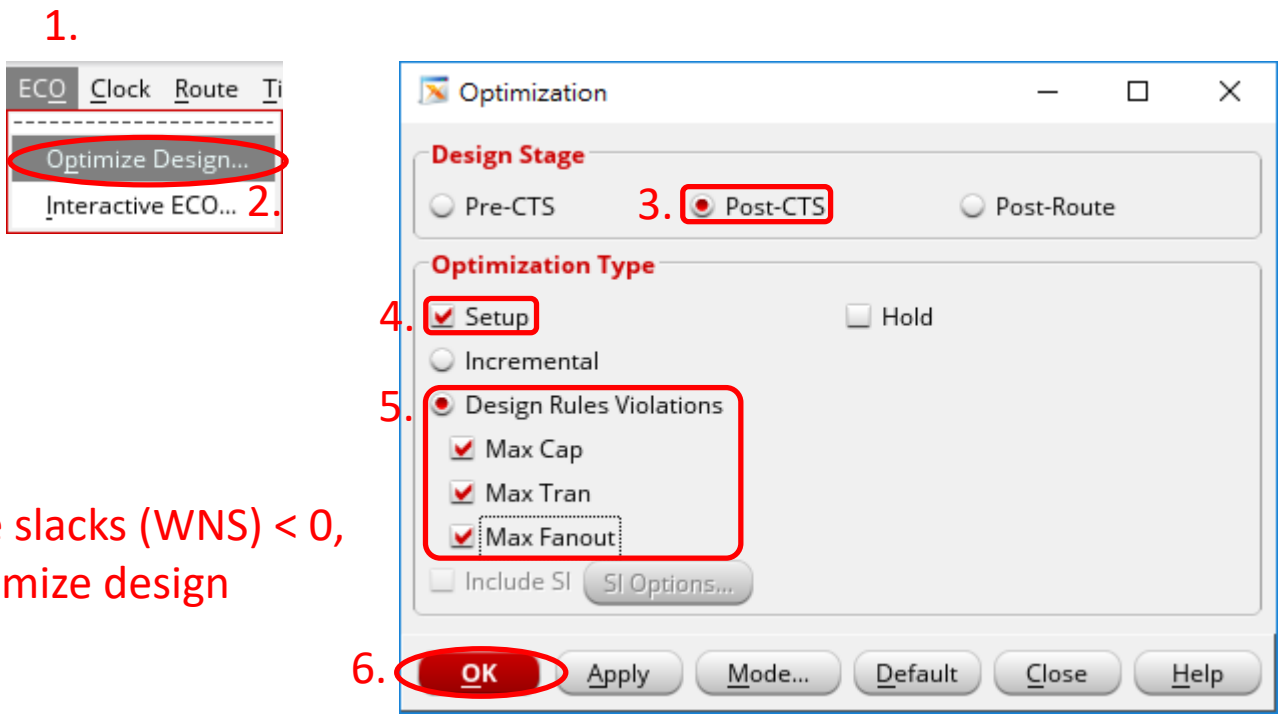




Setup mode	all	reg2reg	default
WNS (ns):	1.155	1.754	1.155
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	116	67	100

If worst negative slacks (WNS) < 0, you need to optimize design

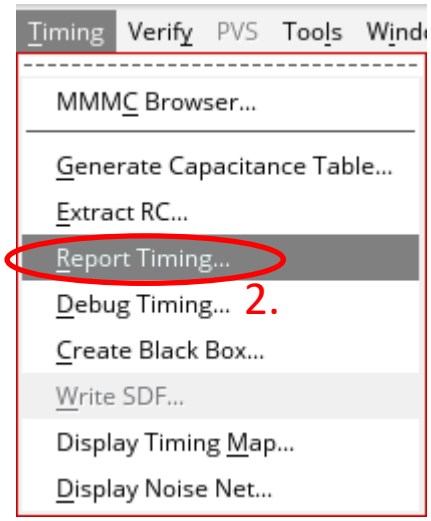
Optimize Design – Setup (Optional)

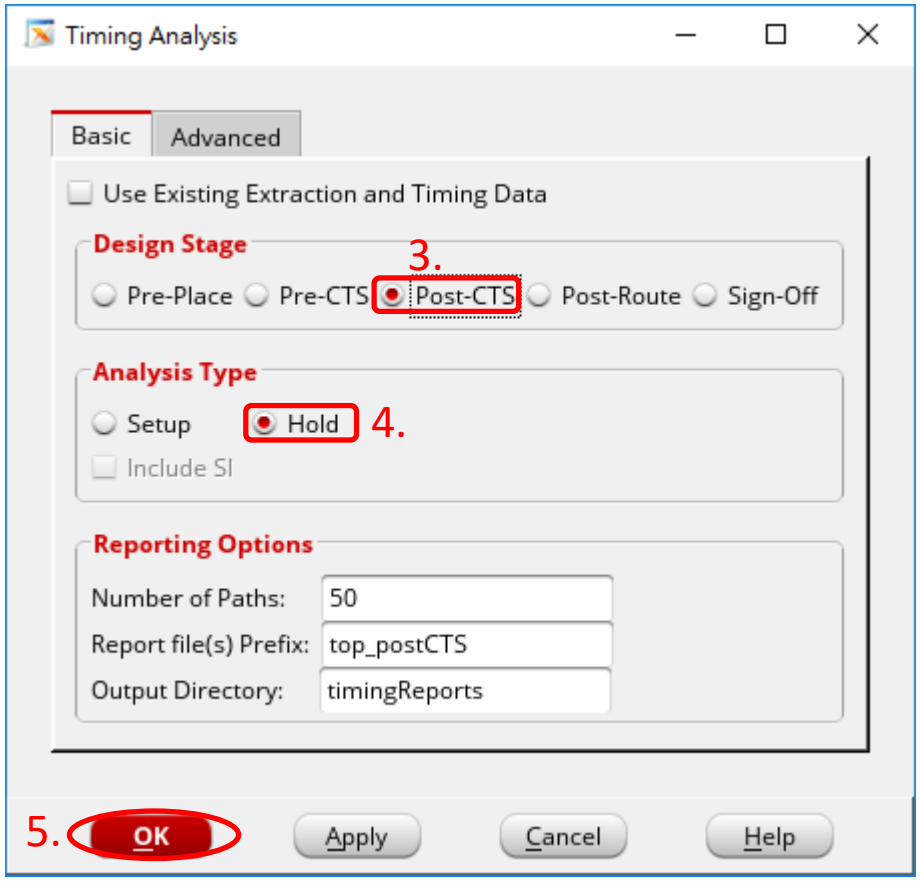


If worst negative slacks (WNS) < 0, you need to optimize design

Report Timing - Hold

1.



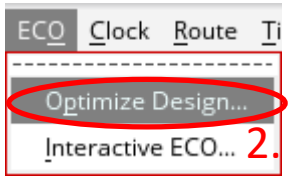


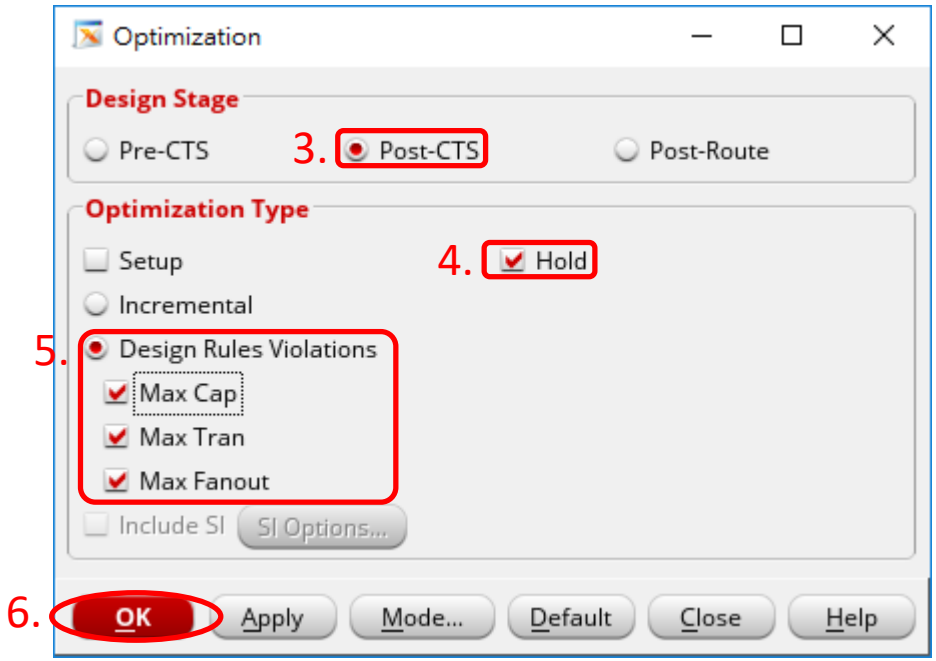
Hold mode	all	reg2reg	default
WNS (ns):	-0.061	0.127	-0.061
TNS (ns):	-1.154	0.000	-1.154
Violating Paths:	23	0	23
All Paths:	116	67	100

If worst negative slacks (WNS) < 0, you need to optimize design

Optimize Design – Hold (Optional)

1.

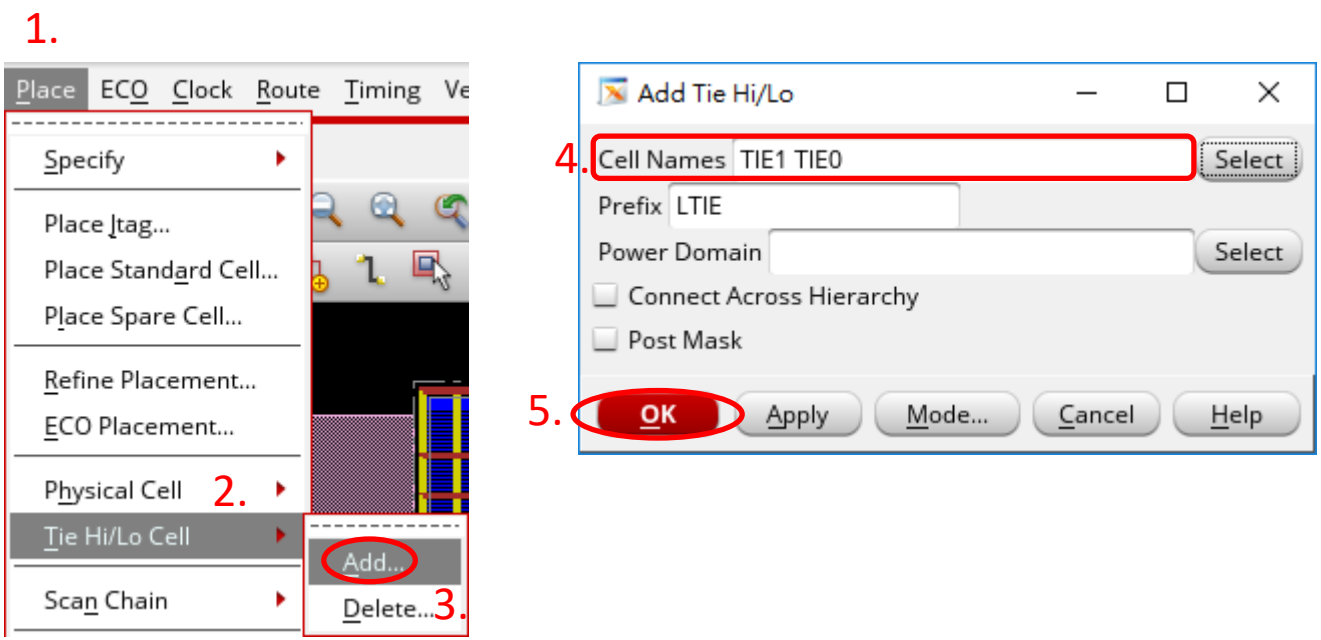




Hold mode	all	reg2reg	default
WNS (ns):	0.035	0.127	0.035
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	116	67	100

If worst negative slacks (WNS) < 0, you need to optimize design

Add Tie Hi/Lo Cells

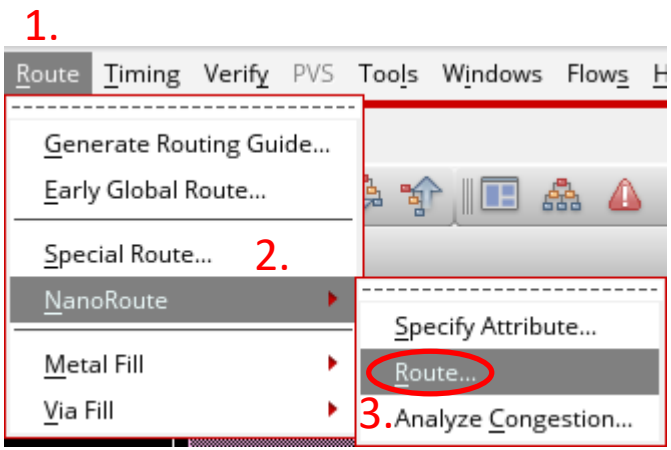


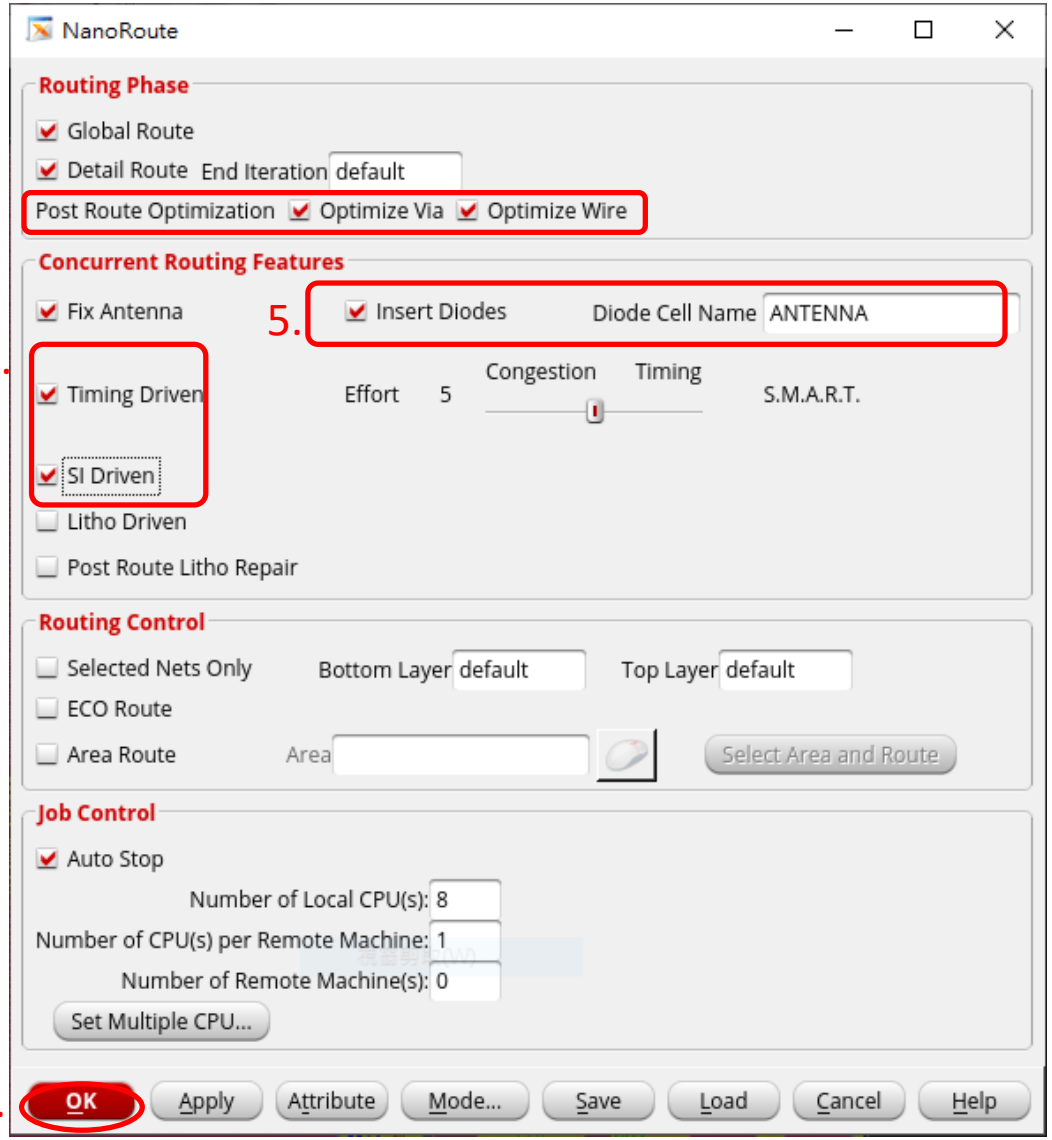
- Tiehi/Tielo cell connect tiehi/tielo net to supply voltage or ground with resister
- Tiehi/Tielo cell is added for ESD protection

Routing

Adding wires to connect the whole design

Route

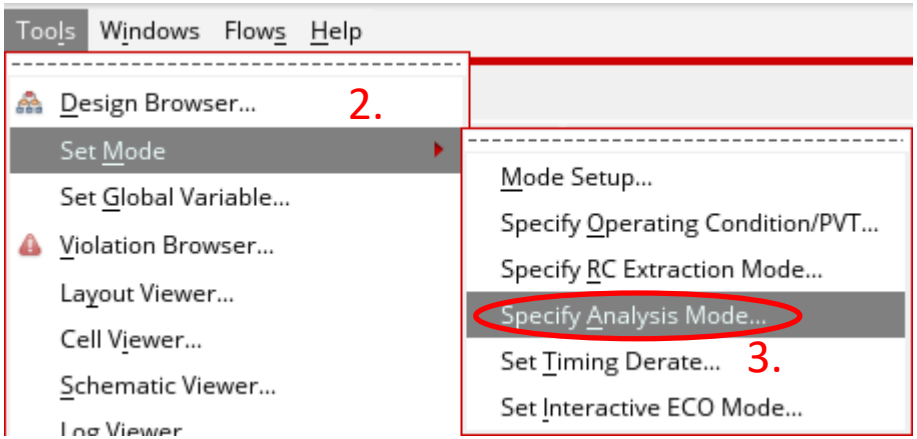


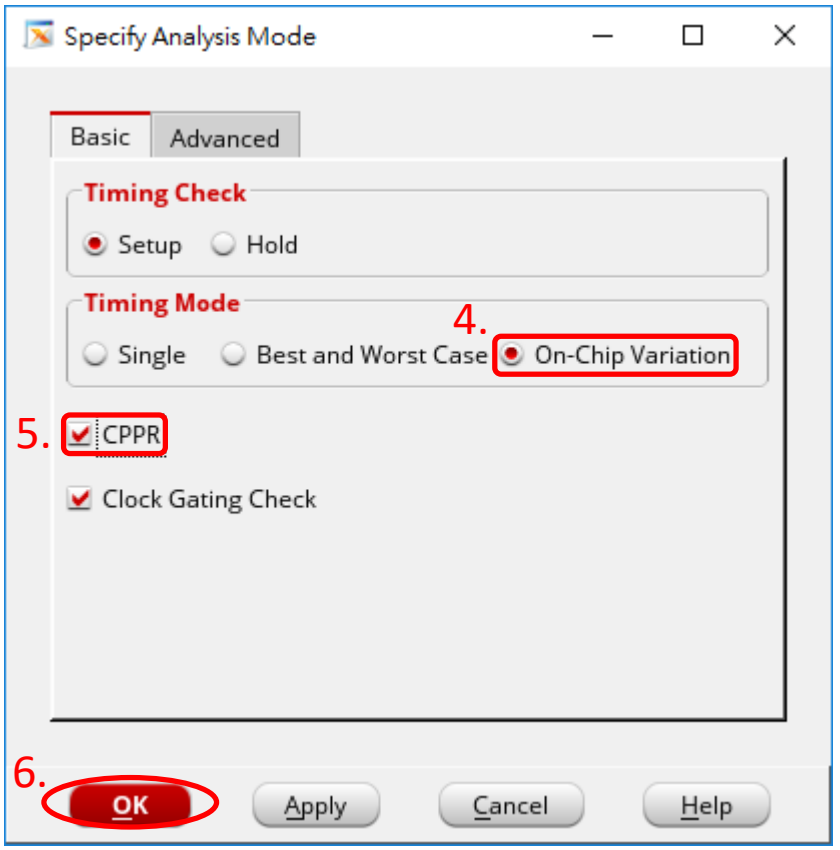


- Optimize Via
  - Add via for yield issue
- Optimize Wire
  - Some wires can use same metal in different direction
- Antenna
  - Fix antenna effect
- SI Driven
  - Prevent signal integrity

Specify Analysis Mode

1.





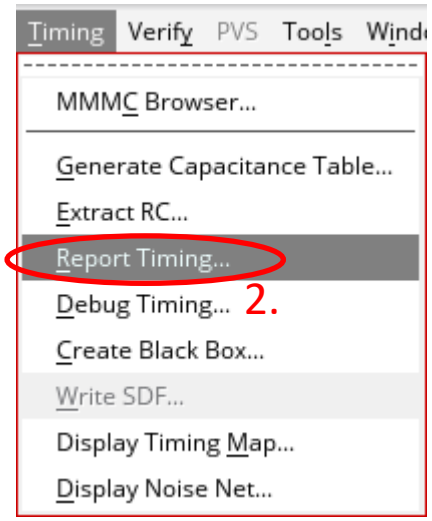
7.

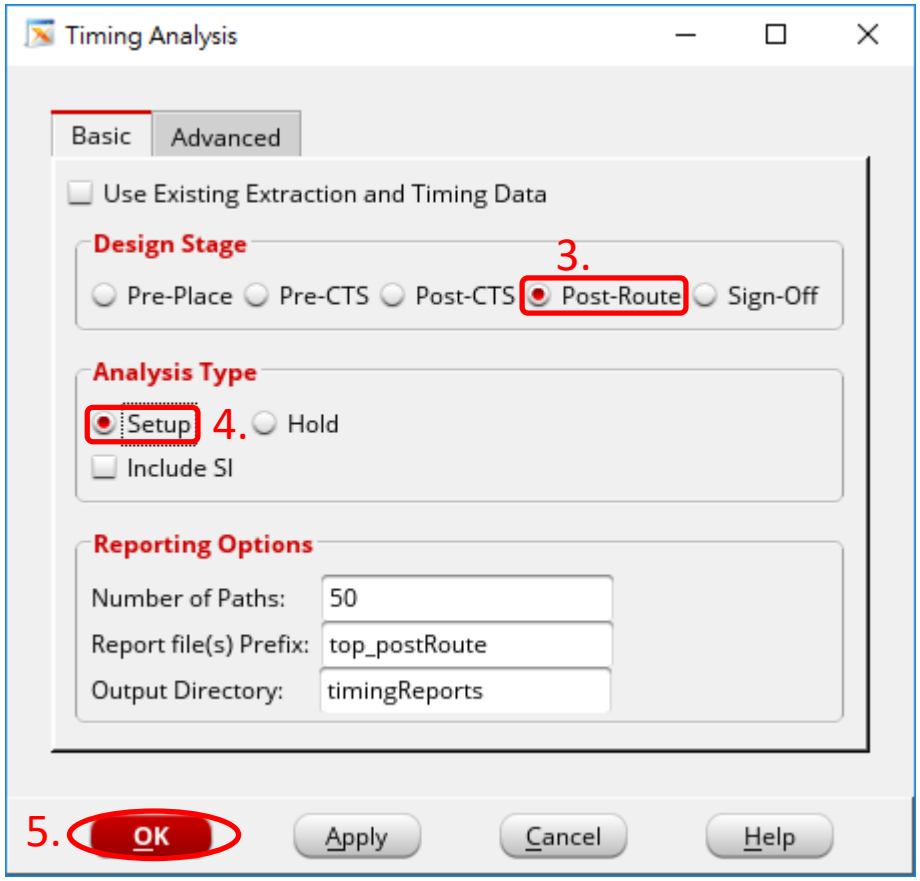
```
innovus 15> setDelayCalMode -SIAware true
```

CPPR: Clock Path Pessimism Removal

Report Timing (Setup)

1.

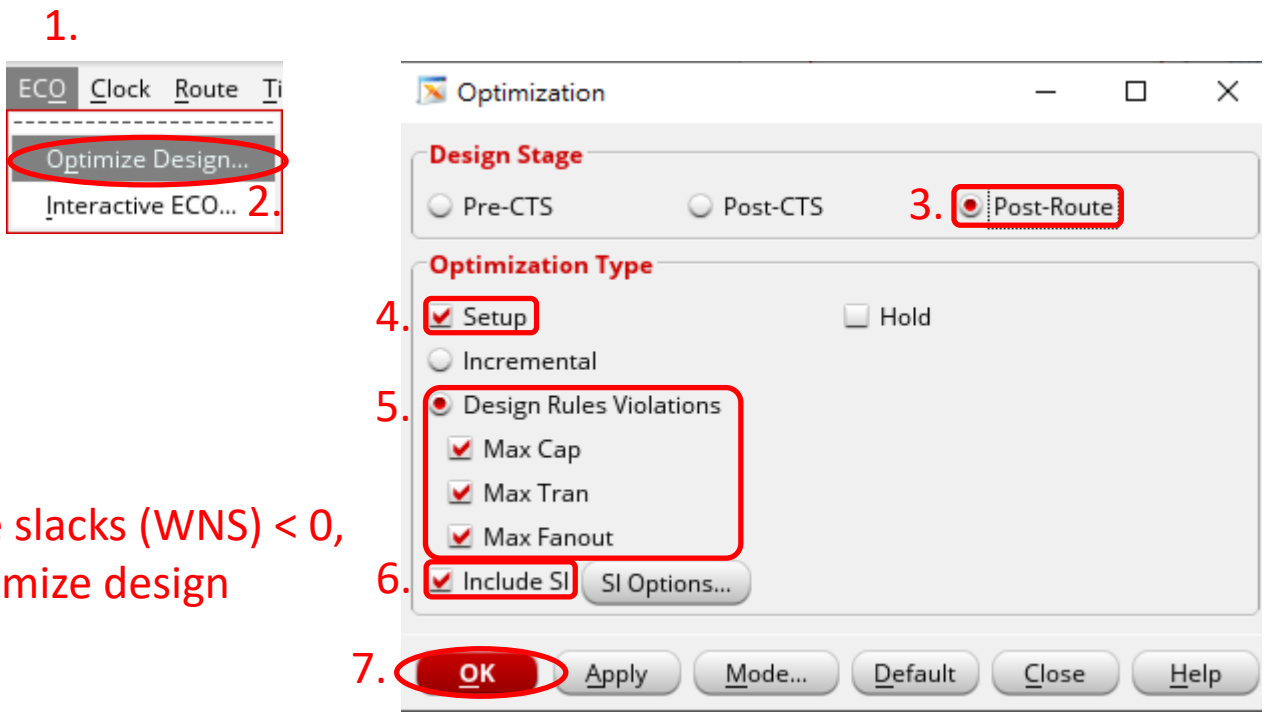




Setup mode	all	reg2reg	default
WNS (ns):	0.719	1.515	0.719
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	116	67	100

If worst negative slacks (WNS) < 0, you need to optimize design

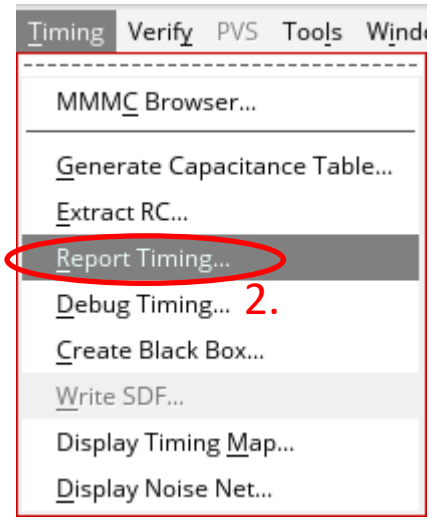
Optimize Design (Setup)

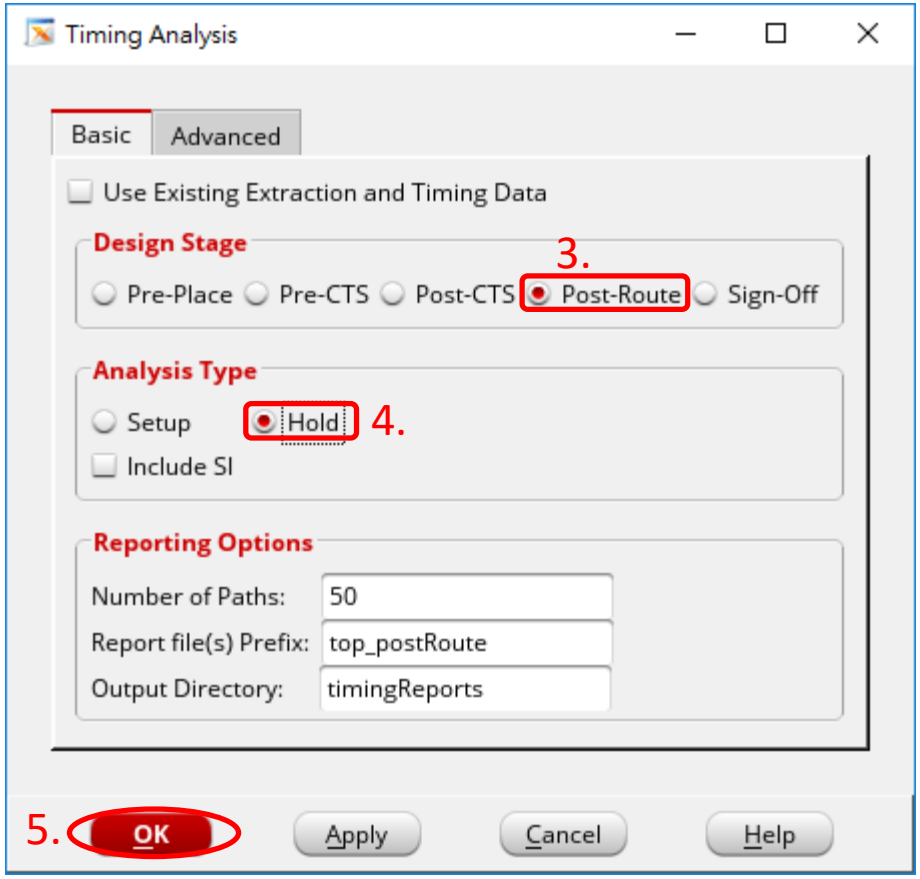


If worst negative slacks (WNS) < 0, you need to optimize design

Report Timing (Hold)

1.

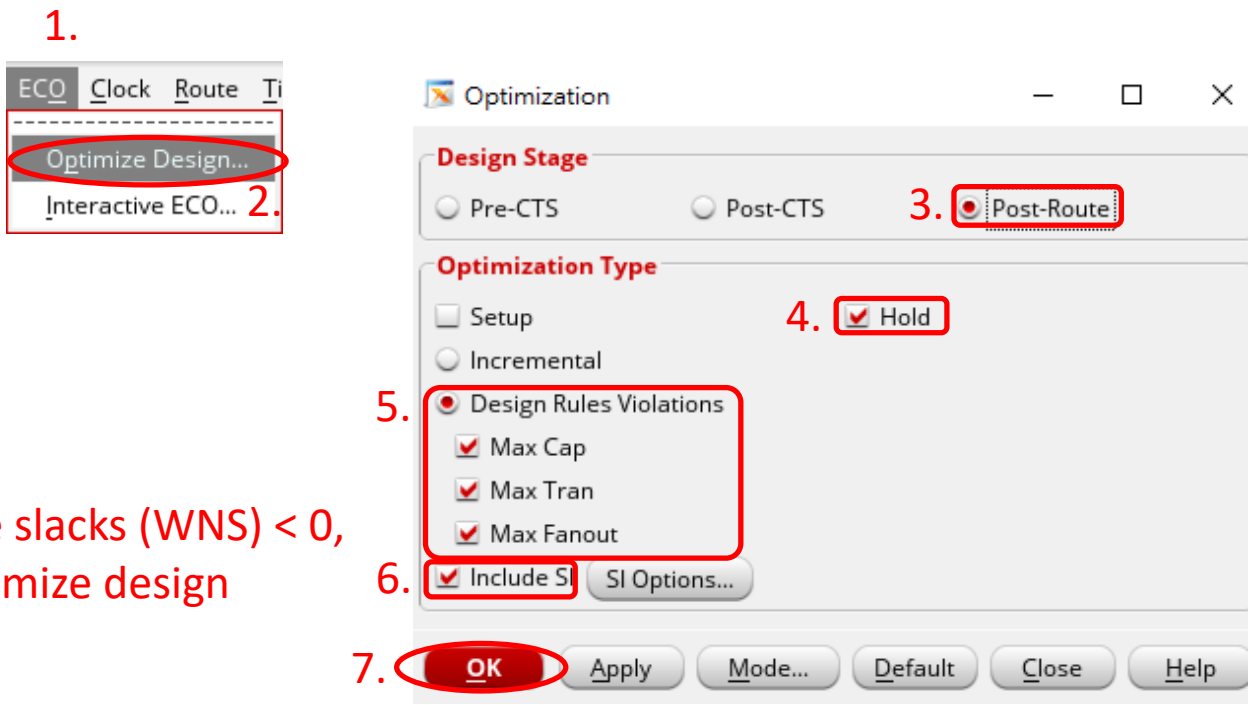




Hold mode	all	reg2reg	default
WNS (ns):	0.064	0.140	0.064
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	116	67	100

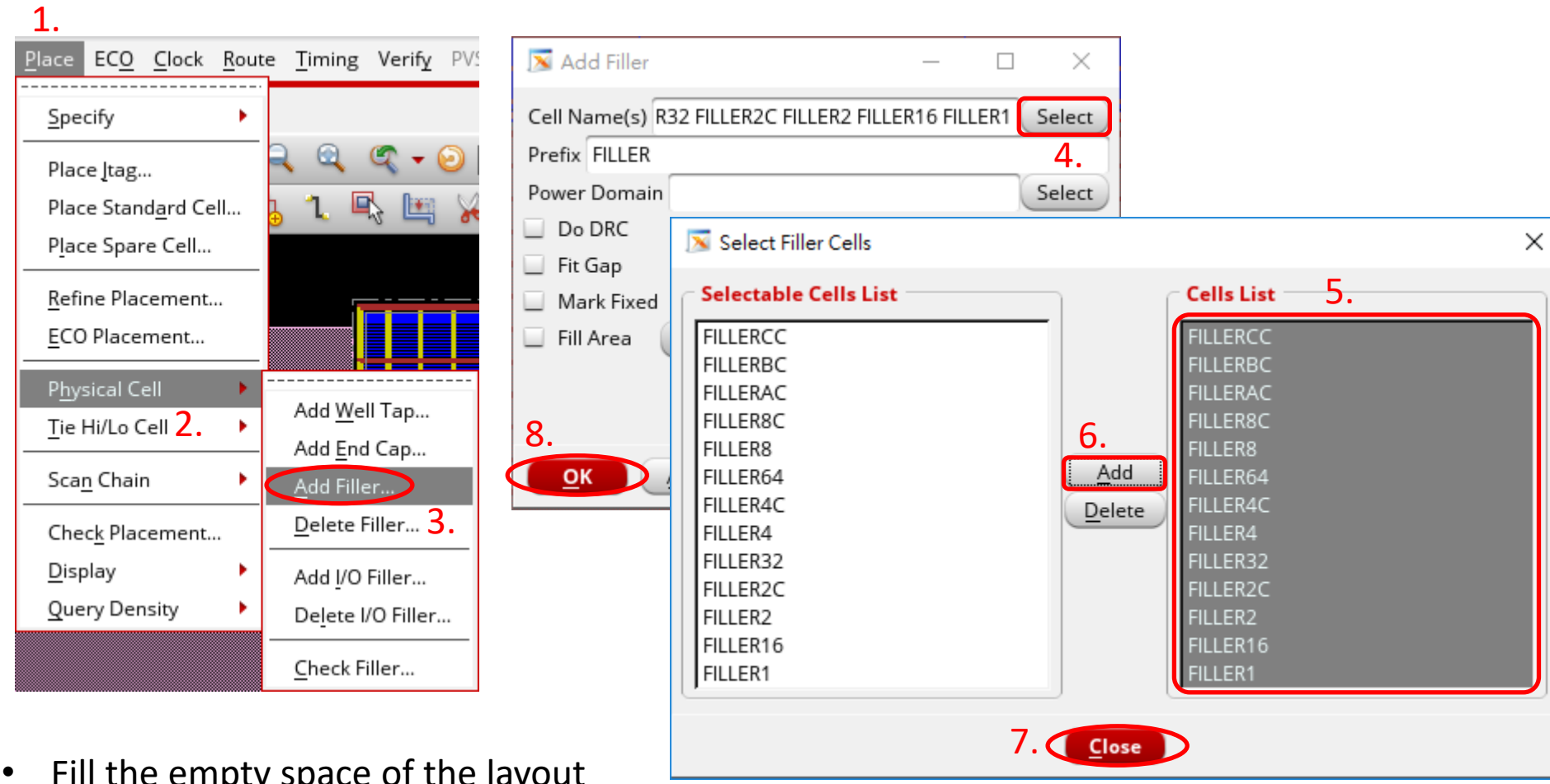
If worst negative slacks (WNS) < 0, you need to optimize design

Optimize Design (Hold)



If worst negative slacks (WNS) < 0, you need to optimize design

Add Core Filler



- Fill the empty space of the layout
- Connect the NWELL/PWELL layer in core rows

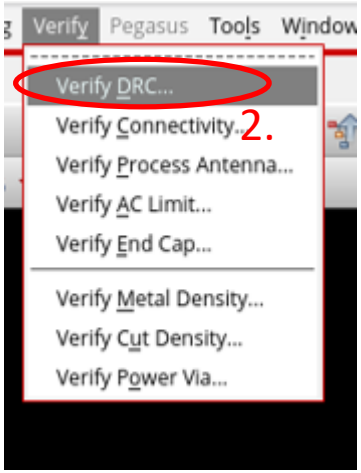
DRC / LVS / Antenna

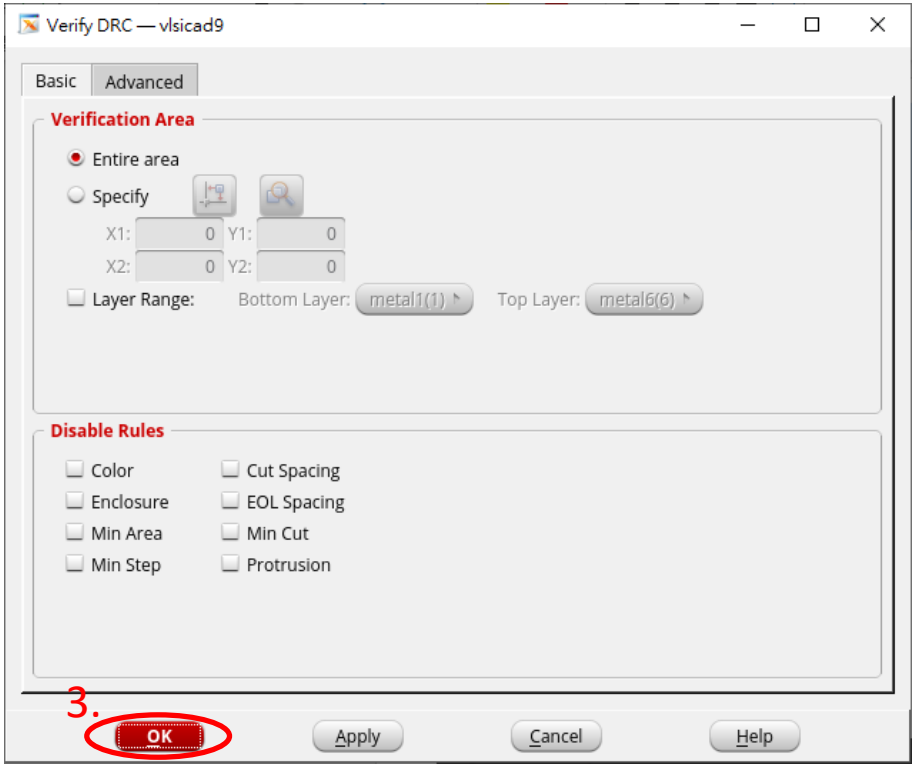
Check the design

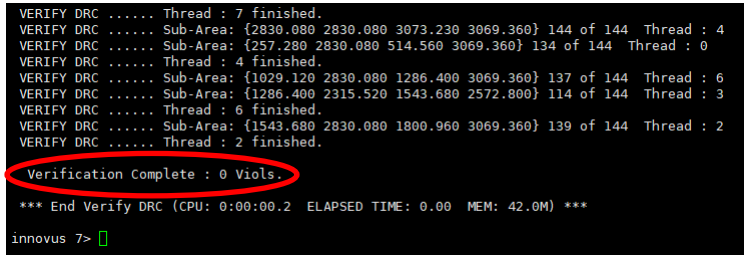
Verify DRC

- Design Rule Check
  - Check if the layout violate the foundry constraint or not.
  - Including
    - Minimum Width
    - Minimum Spacing
    - Short
    - and other characteristics

1.



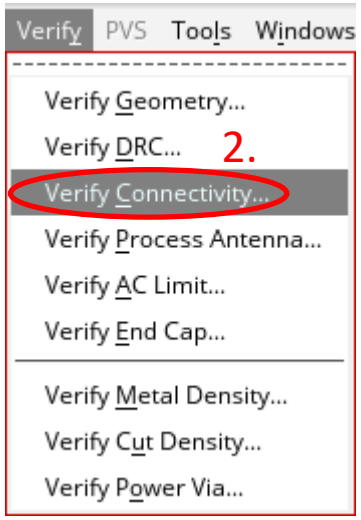




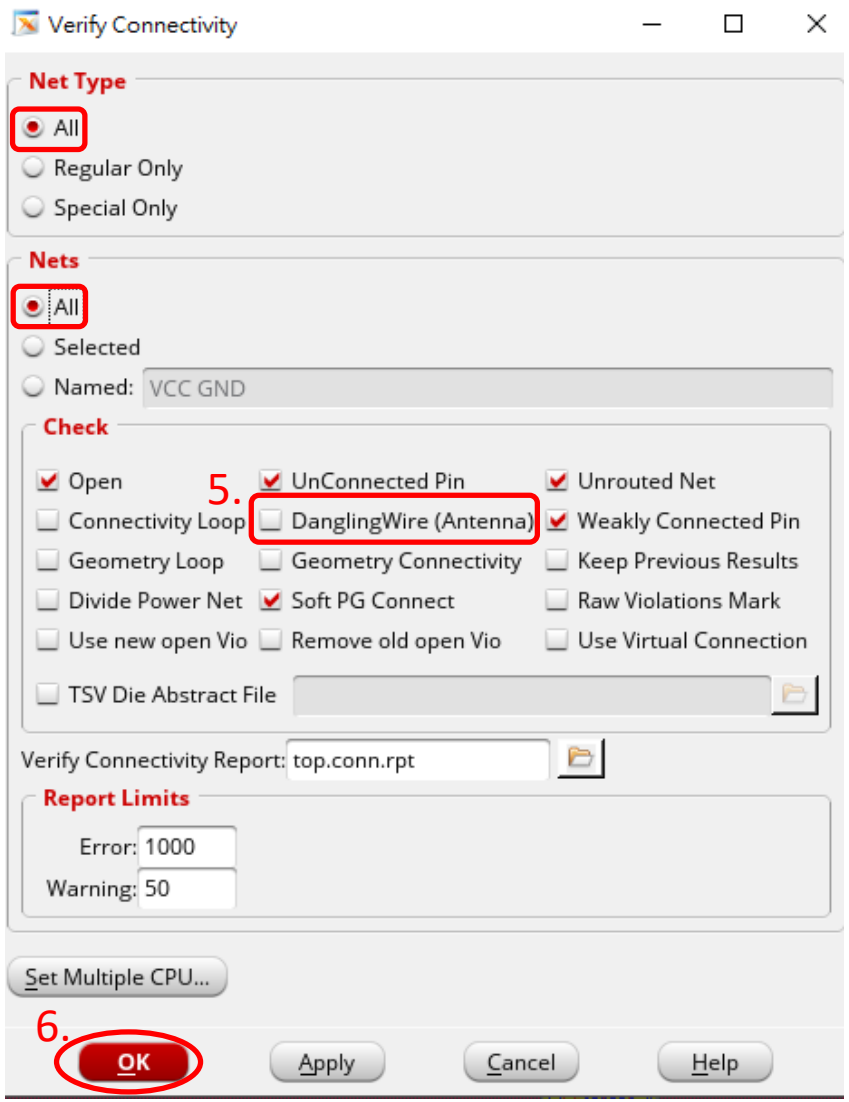
Verify Connectivity (LVS)

- Layout versus Schematic
  - Check if the layout is same as the netlist

1.



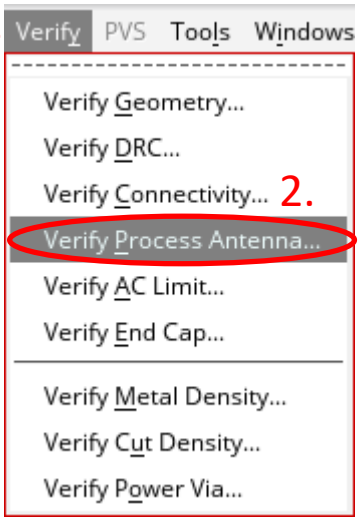

```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:01.9  MEM: 58.309M)
```

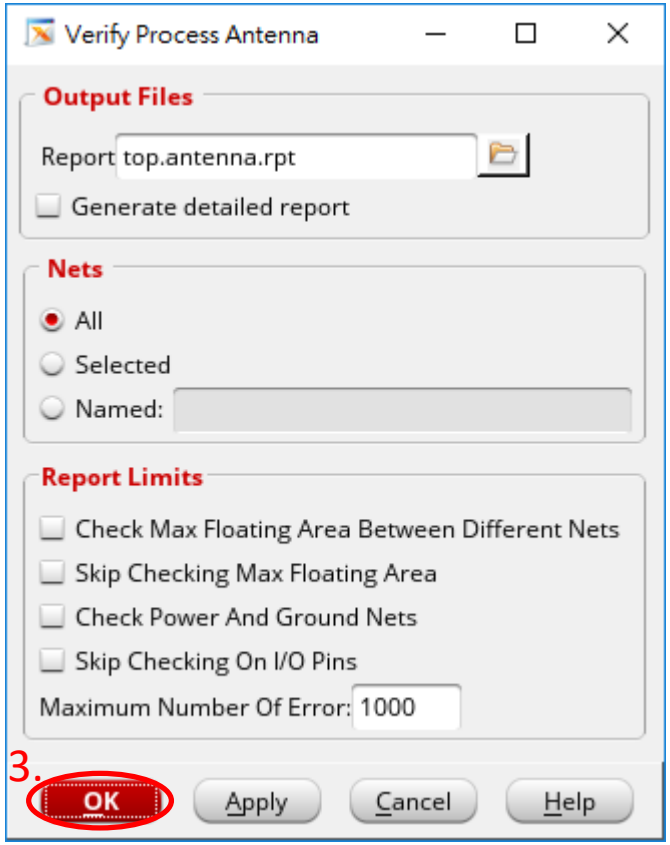


Verify Process Antenna

- Process Antenna
  - Check if the layout has antenna effect or not

1.

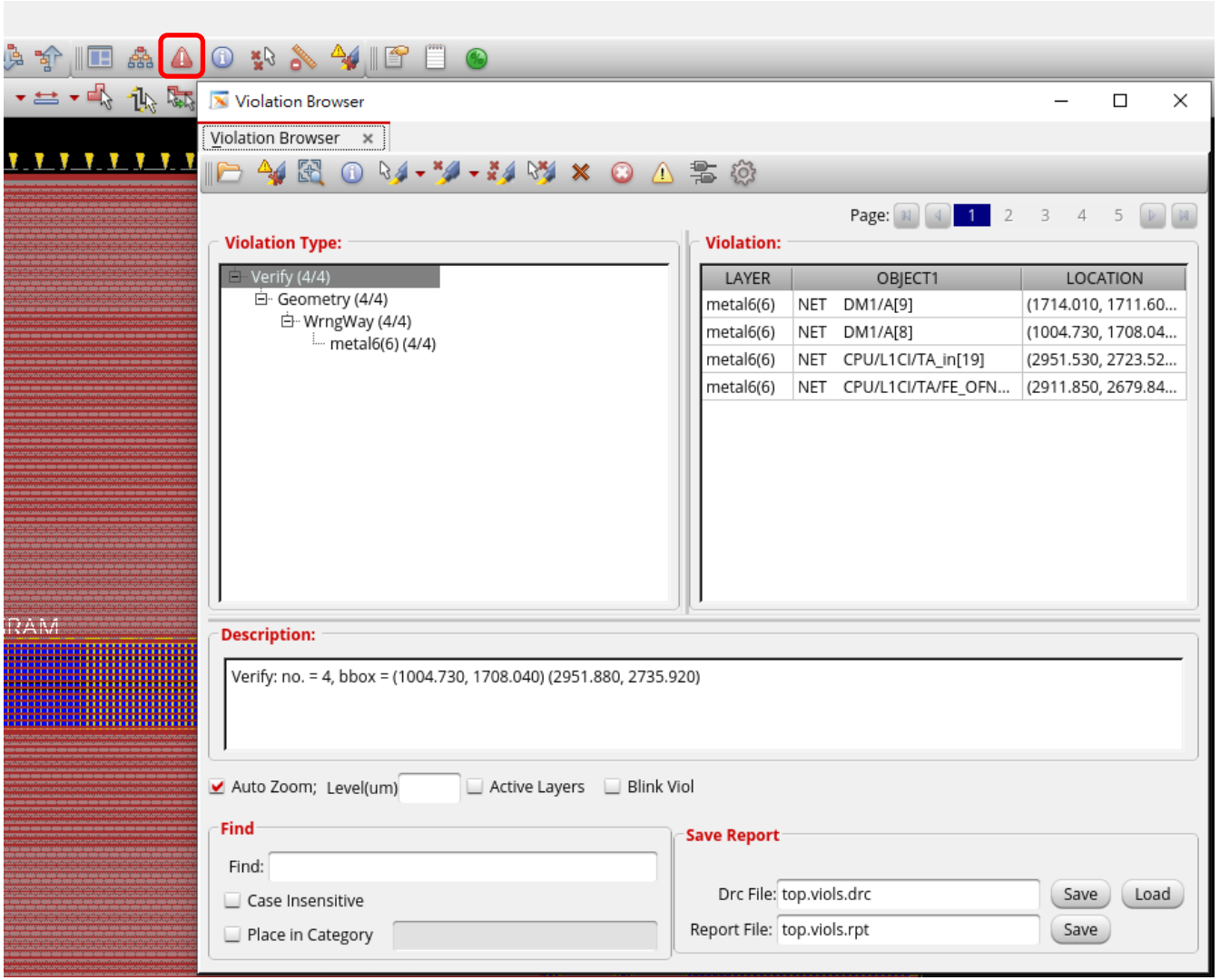





```
******* START VERIFY ANTENNA ********
Report File: top.antenna.rpt
LEF Macro File: top.antenna.lef
5000 nets processed: 0 violations
10000 nets processed: 0 violations
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time: 0:00:01.4  MEM: 0.305M)
```

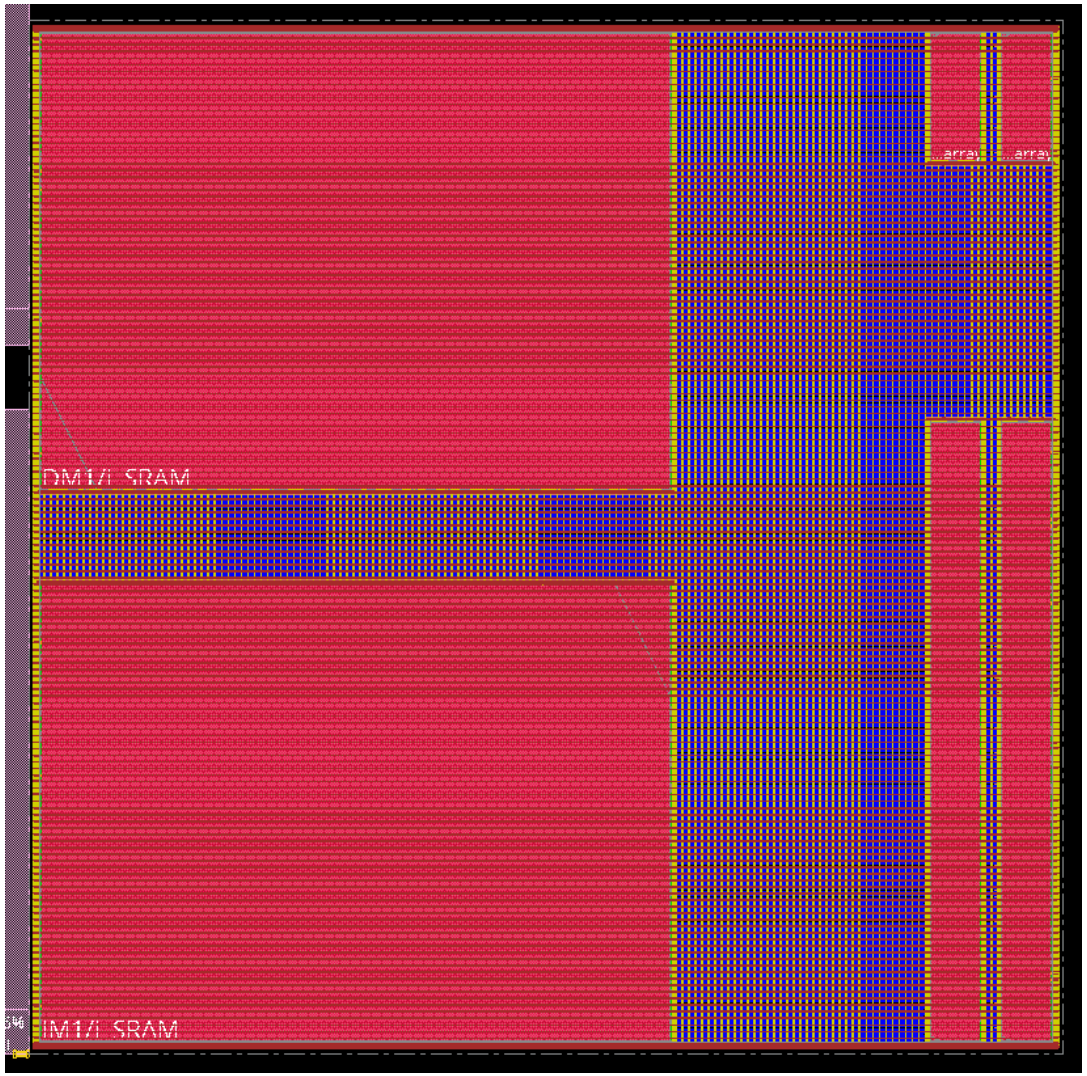
Check violations

- Make sure at least the LVS has no error
  - Affect the functionality of the circuit
- Other violations can use the Violation Browser to check.
  - Or double click the cross icon in physical view.



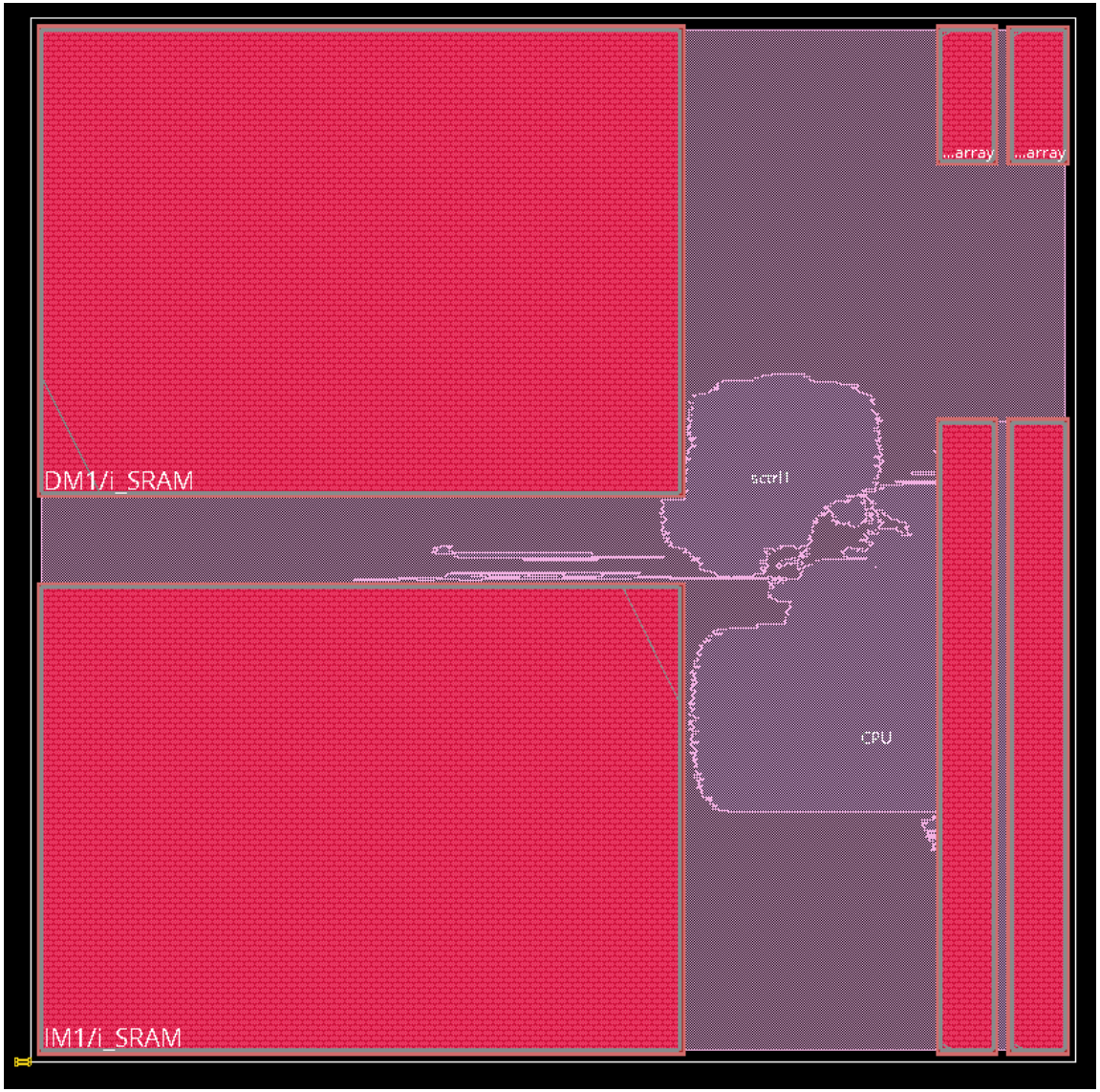
Floorplan View

- The location of hard macro
- The layout of power wiress



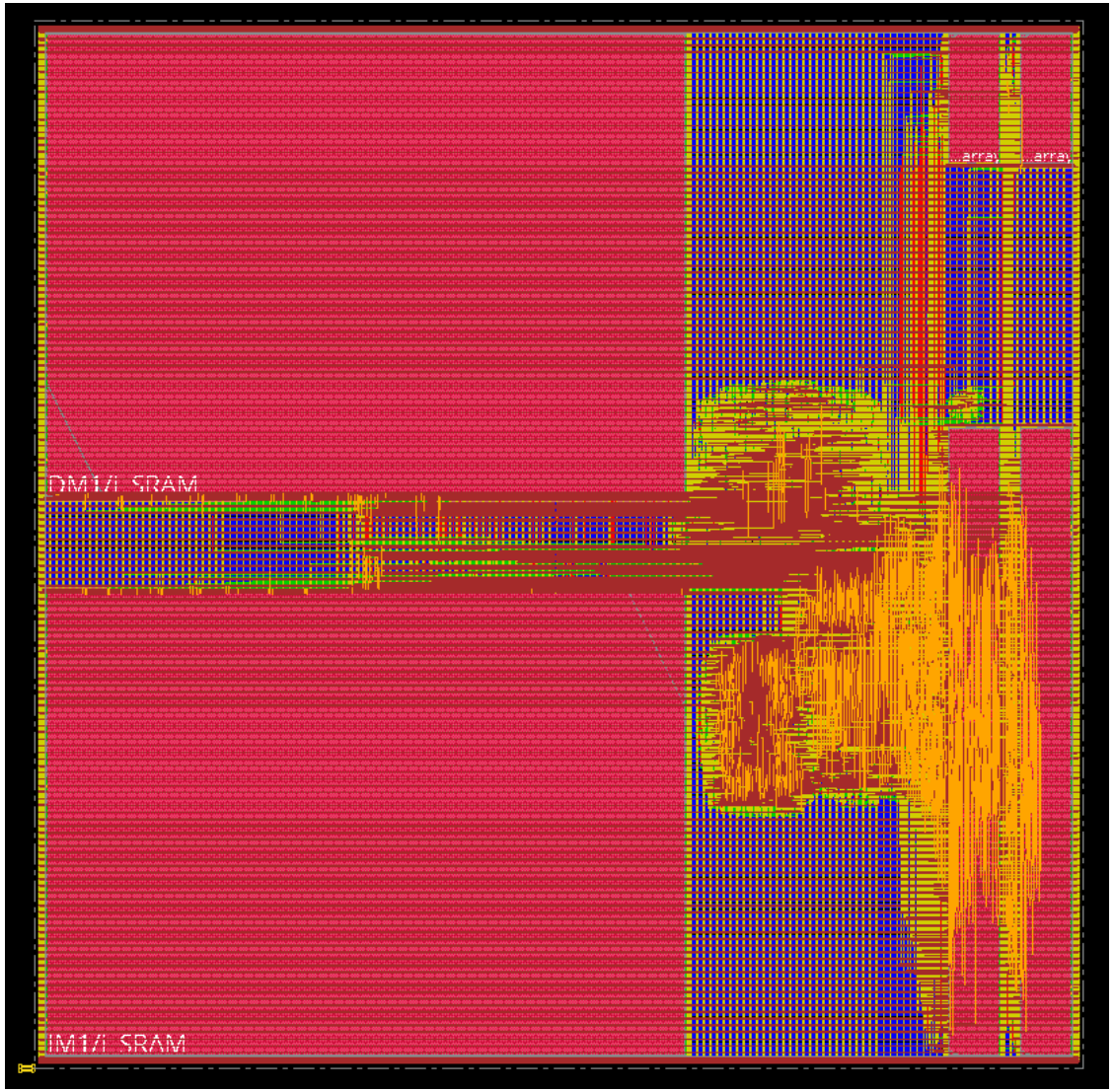
Amoeba View

- The distribution of soft modules
- Soft module
  - Composed by standard cells
  - For example, CPU is the soft module in our design.



Physical View

- All the wires and modules
  - Hard macro – Memory
  - Soft module – standard cells
  - Metal
  - Via

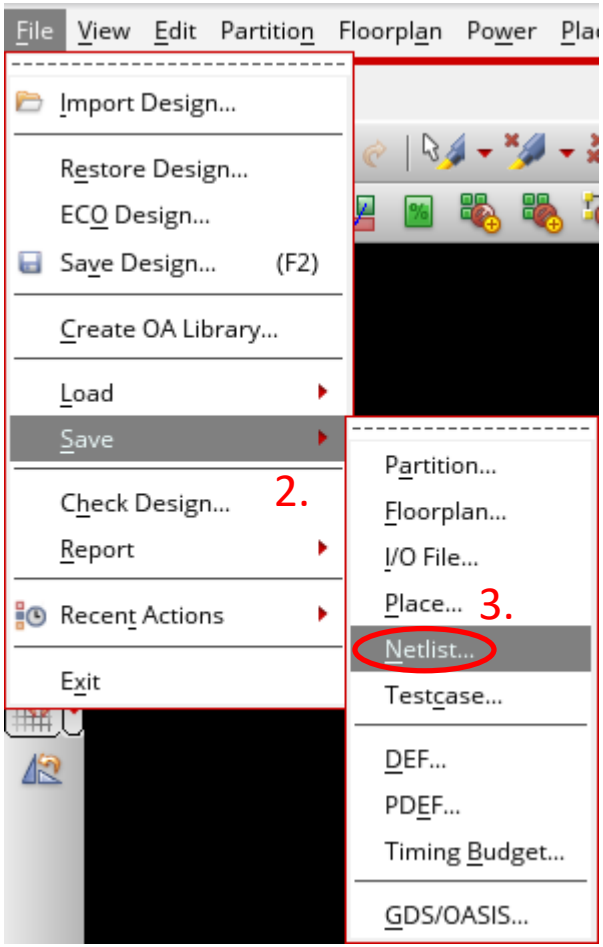


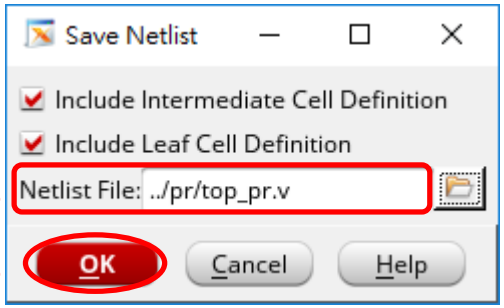
Save / Export Files

Saving the netlist, SDF file and the GDS file

Save Netlist

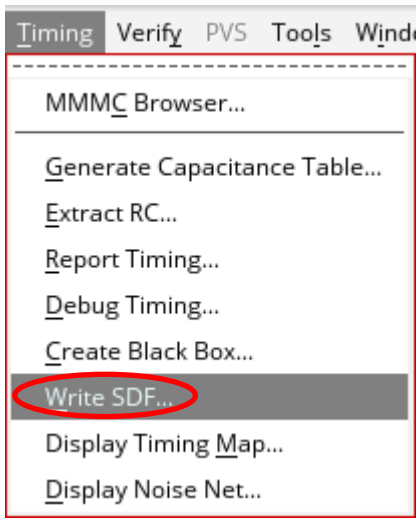
1.





Save SDF File

1.

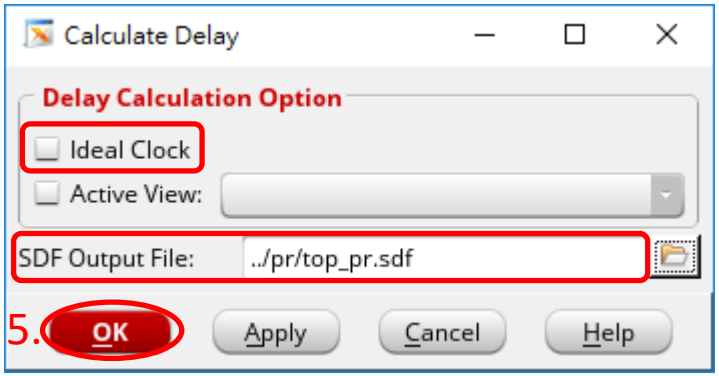


2.

3.

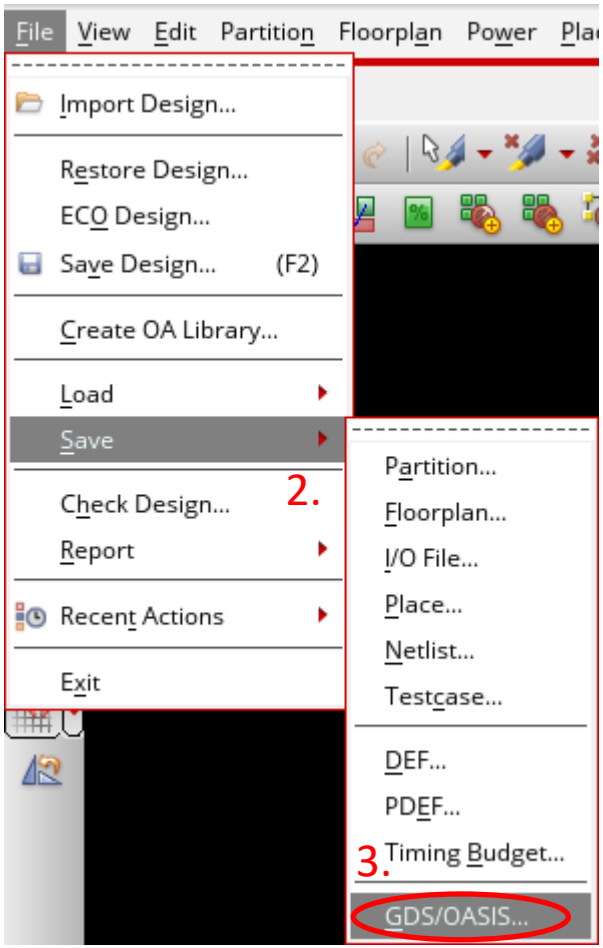
4.

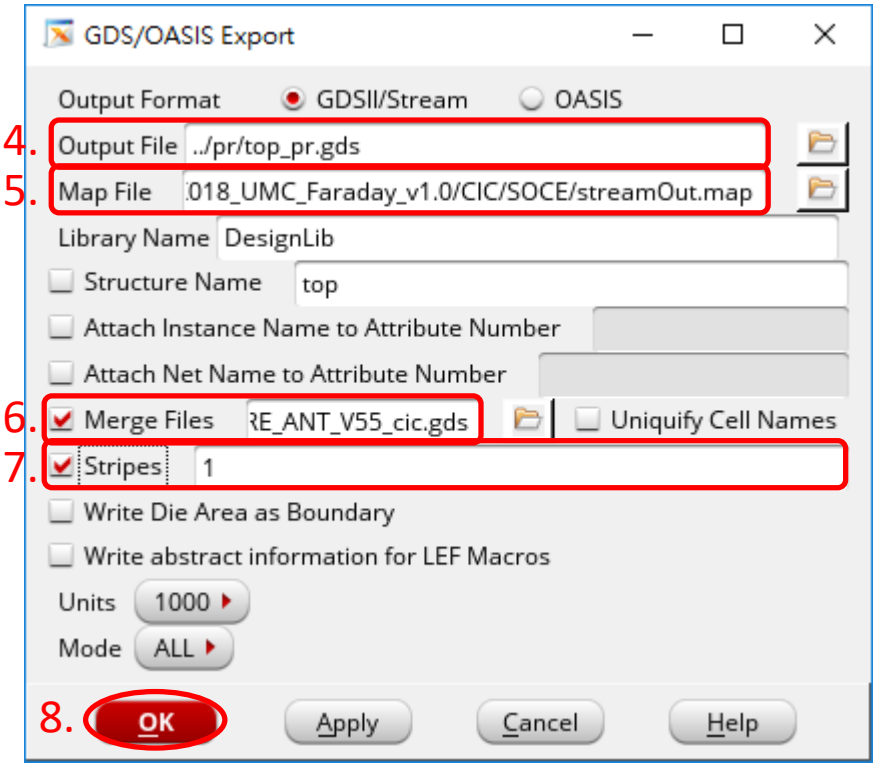
5.



Save GDS File

1.

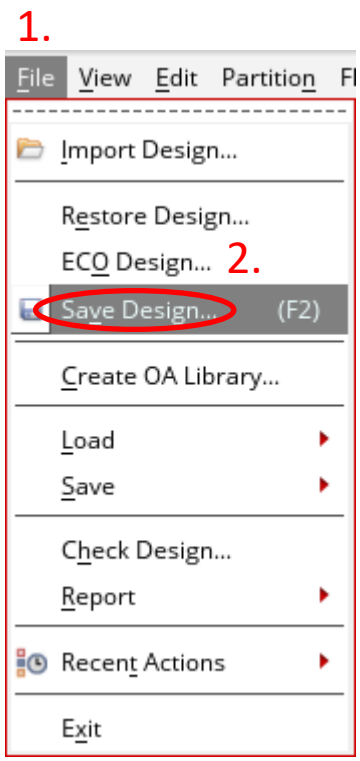


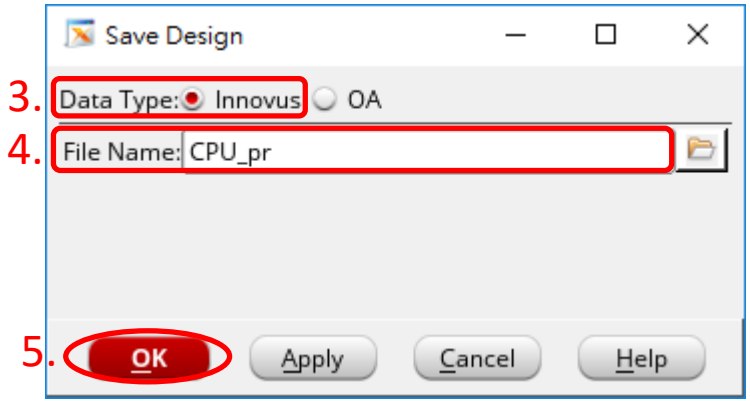


Or use: (This one is better!!!)

```
innovus 4> source ../script/savegds.tcl
```

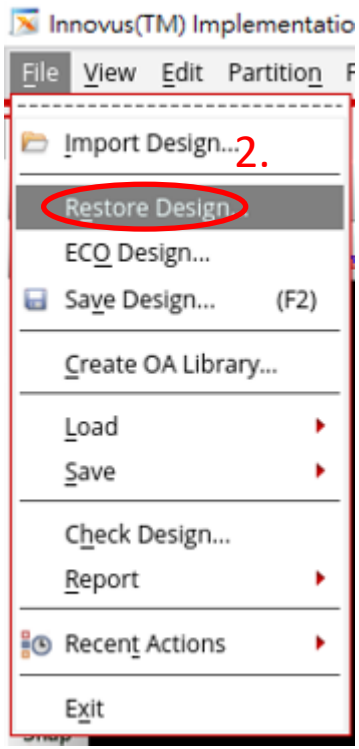
Save Design

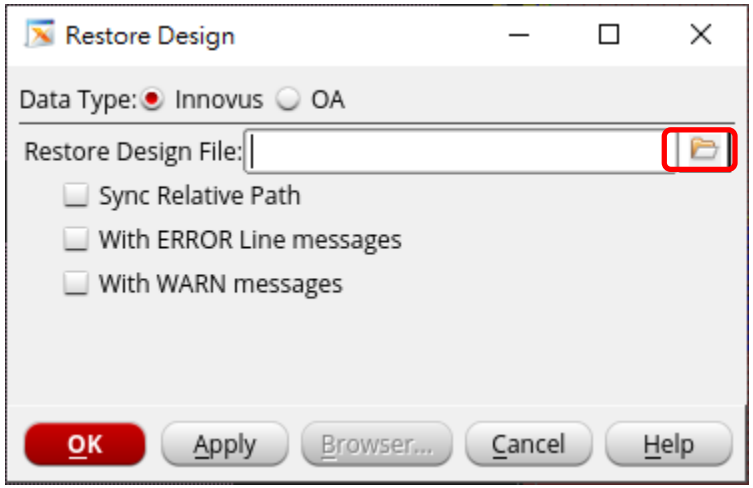




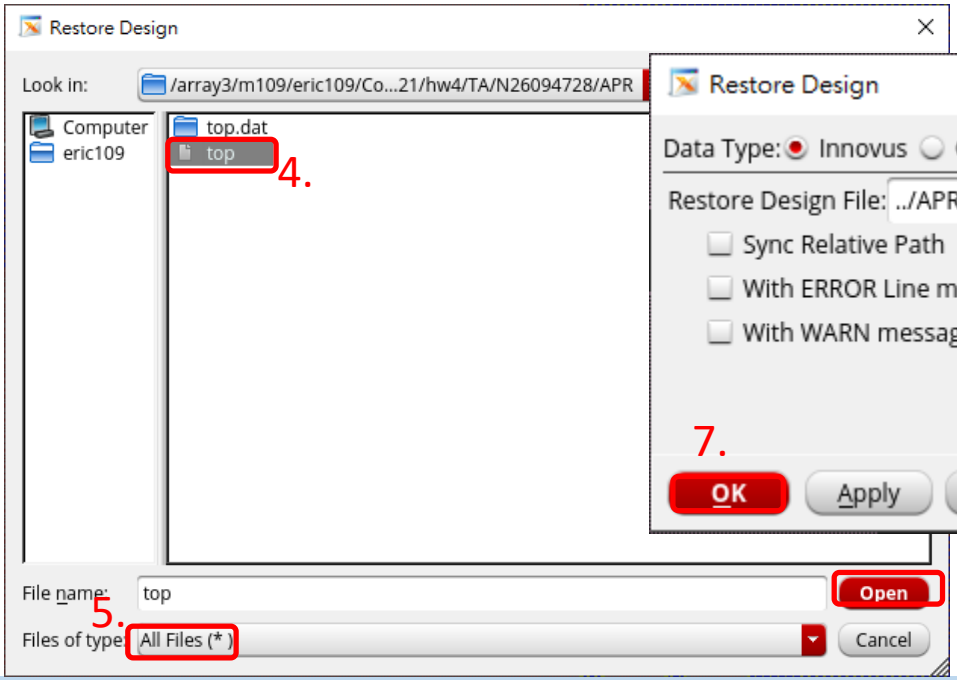
- You can save the design after each stage in case of the Innovus suddenly break down.
- Remember to change the saving directory in case that you make clean to remove the build directory.

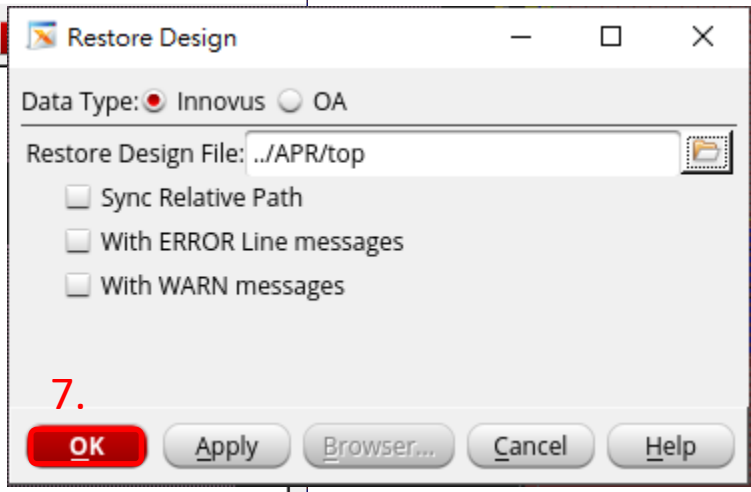
Restore Design





- Restoring the previous stage if the current stage has some problem.



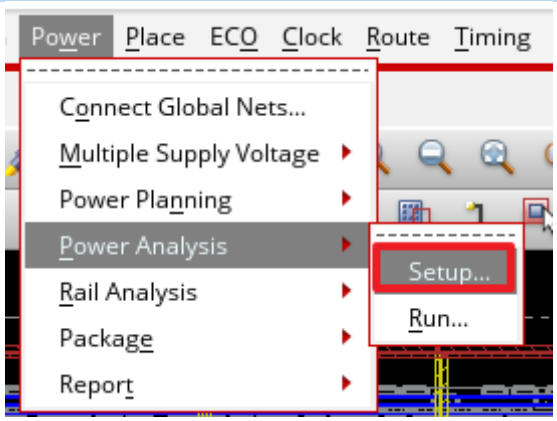


Area

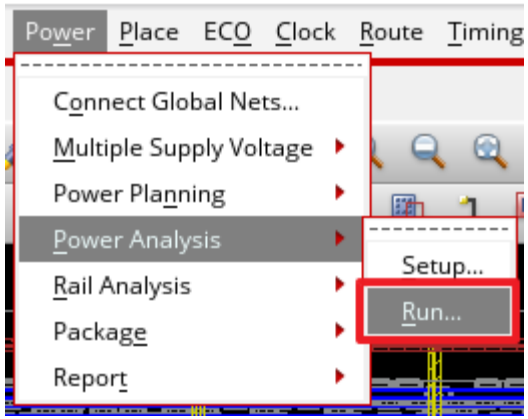
```
innovus 3> analyzeFloorplan
**WARN: (IMPAFPU-9006): Command 'analyzeFloorplan' is obsolete. Please use commands 'placeDesi
+ create_ps_per_micron_model + timeDesign -proto + load_timing_debug_report -proto' to analyze
 for the floorplan.
**WARN: (IMPTR-9997):   The getTrialRouteMode command is obsolete and should not be used anymo
 this release but will be removed in a future release.  You should change to use getRouteMode
rlyGlobalRoute which is the replacement tool for trialRoute.
Start to collect the design information.
Build netlist information for Cell top.
Finished collecting the design information.
Average module density = 1.000.
Density for the design = 1.000.
       = stdcell_area 1032210 sites (3225450 um^2) / alloc_area 1032210 sites (3225450 um^2).
Pin Density = 0.02635.
            = total # of pins 80400 / total area 3051432.
************************** Analyze Floorplan **************************
   Die Area(um^2)              : 9976236.48
   Core Area(um^2)             : 9535114.71
   Chip Density (Counting Std Cells and MACROs and IOs): 93.066%
   Core Density (Counting Std Cells and MACROs): 97.372%
   Average utilization         : 100.000%
   Number of instance(s)       : 62064
   Number of Macro(s)          : 6
   Number of IO Pin(s)         : 167
   Number of Power Domain(s)   : 0
************************** Estimation Results **************************
************************************************************************
```

- After analyzeFloorplan command, the layout will be destroyed, so remember saving the design before using this command.

Power(1/2)

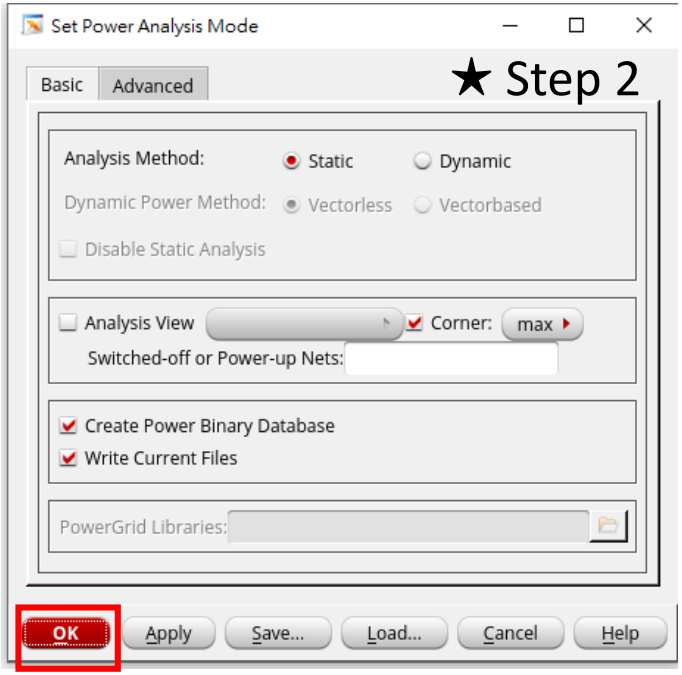


★ Step 1

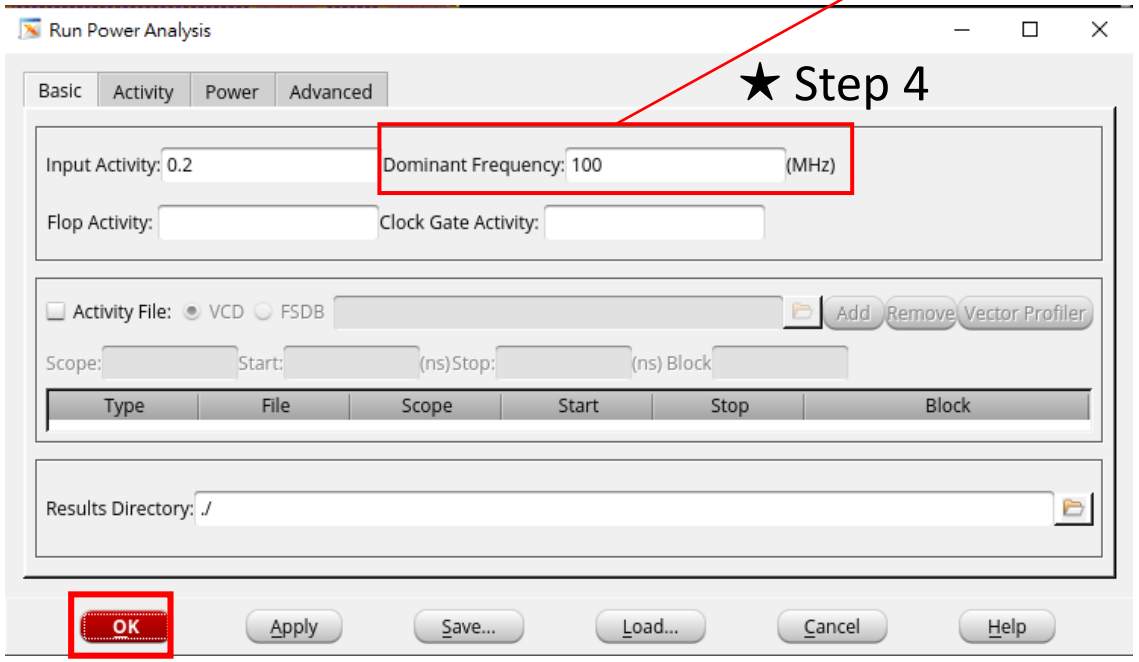


★ Step 3

Modify the frequency for your design



★ Step 2



★ Step 4

Power(2/2)

```
Total Power
--------------------------------------------------------------------------------
Total Internal Power:      189.64096161            90.8694%
Total Switching Power:      17.75457229             8.5074%
Total Leakage Power:         1.30072671             0.6233%
Total Power:               208.69625843 mW
--------------------------------------------------------------------------------
Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1200.39MB/2225.98MB/1200.39MB)
```

Reference

- CIC Training Manual – Cell-Based IC Physical Design and Verification with Innovus, January 2021
- Training Course of SoC Encounter (http://www.ee.ncu.edu.tw/~jfli/vlsidi/lecture/soc)
- Cell-Based IC Physical Design and Verification - SoC Encounter (http://mspic.ee.nchu.edu.tw/class_course/university/97_VLSI-design/handout/4-1.Soc_Encounter.pdf)
- Cadence Help

Thanks for your participation and attendance ! !