

Spyglass CDC verification

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Outline

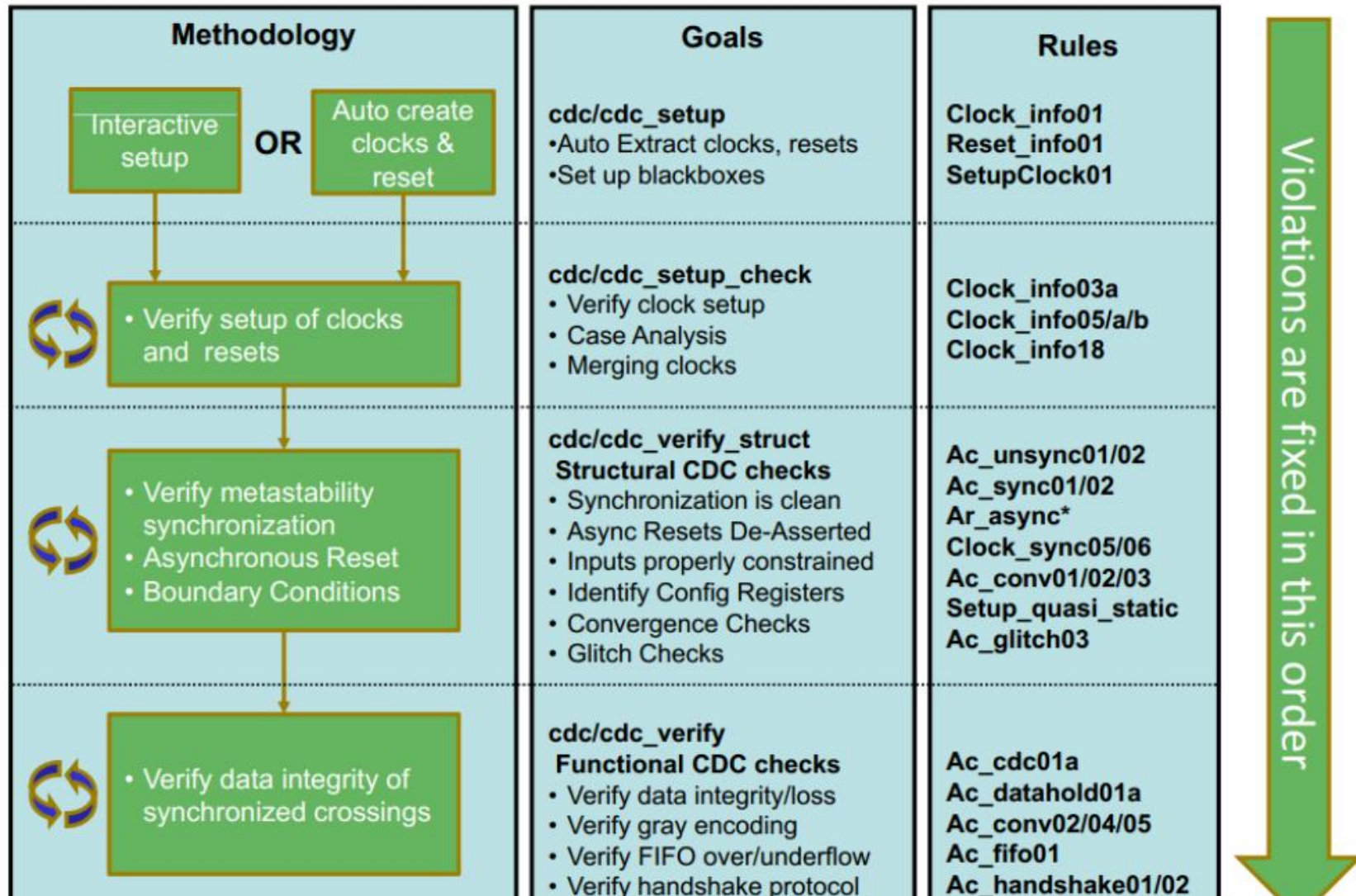
- Introduction
- Import design
- CDC verification

Introduction

- Spyglass is the early design analysis tool enabled efficient verification and optimization of soc designs
- With this tool, designers can gain insight into their designs early in the RTL process.
 - Lint, CDC, LP, DFT, Constraint



Spyglass CDC verification flow



Open GUI

■ [spyglass/build] \$ spyglass

■ [spyglass] \$ make spyglass

➤ In this exercise & homework

```
[N26101039_mul]$ make spyglass
```

```
maxpend=1  
cd ./build; \  
spyglass
```

```
          SpyGlass (R)  
        Synopsys TestMAX(TM)
```

```
Version P-2019.06 for linux64 - Jun 02, 2019
```

```
Copyright (c) 2001 - 2019 Synopsys, Inc.
```

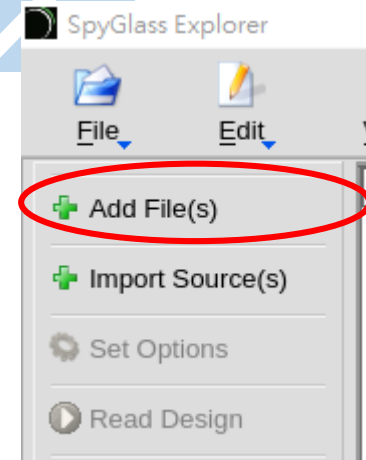
```
This software and the associated documentation are proprietary to Synopsys,  
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or distribution of this software is strictly prohibited.
```

Import design

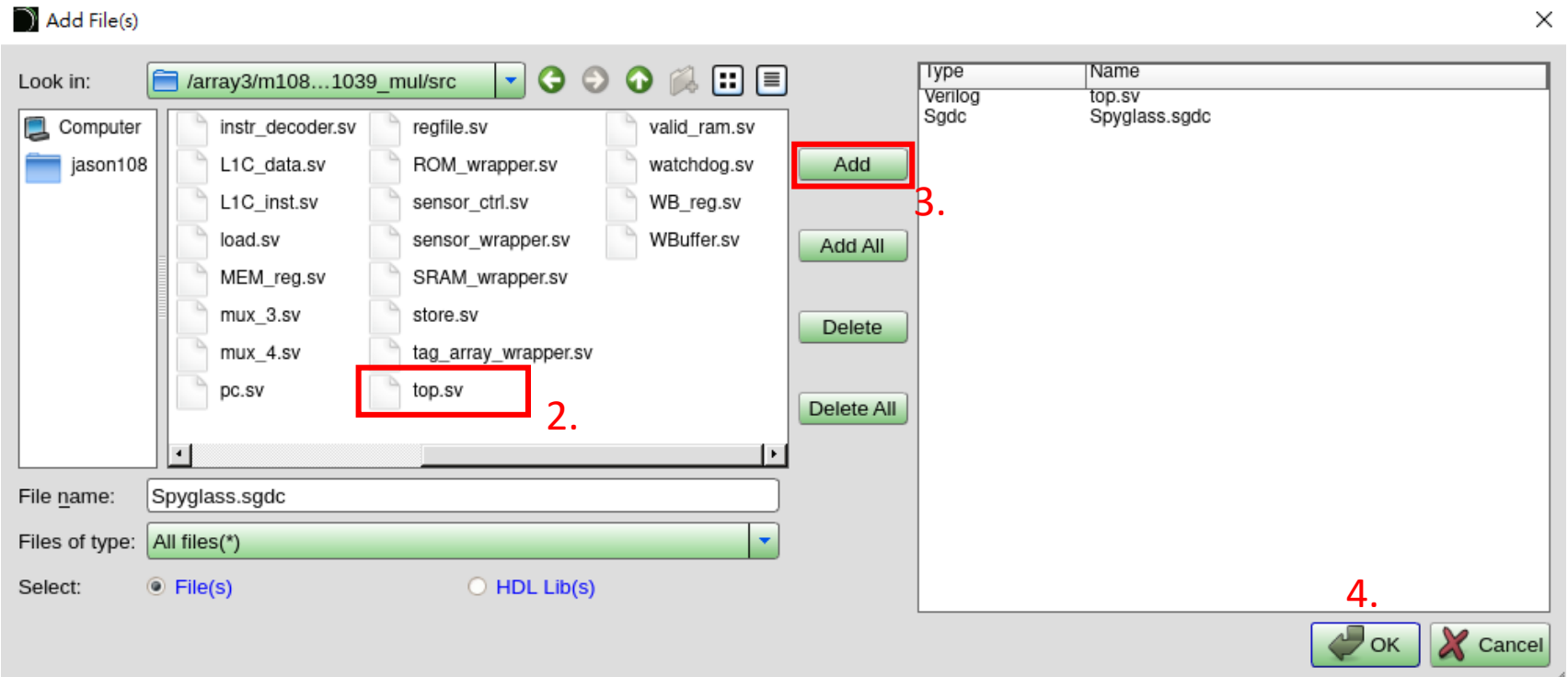
Import design

Read design file(.v/.sv)

- read_file -type verilog "top module file"
- read_file -type sgdc "sgdc file"



1.

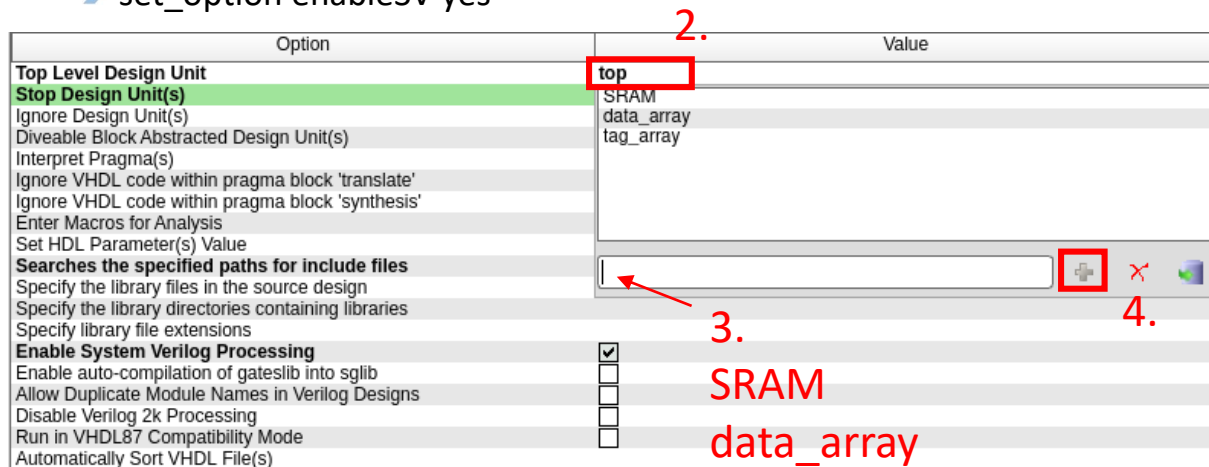
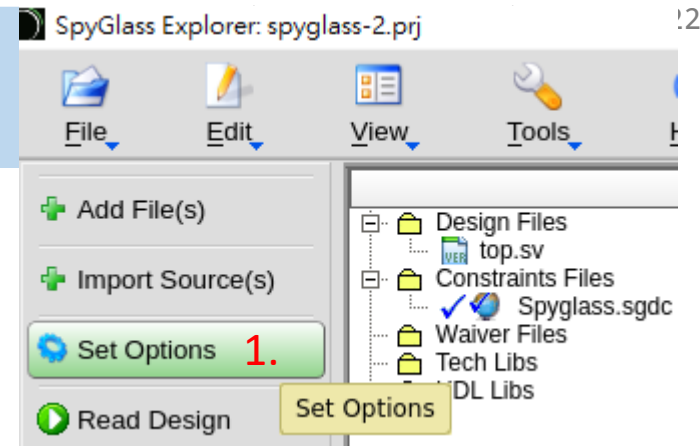


4.

Option settings

Read design & constraint file

- set_option top "top module name"
- set_option stop "blackbox module name"
- set_option incdir "path"
- set_option enableSV yes



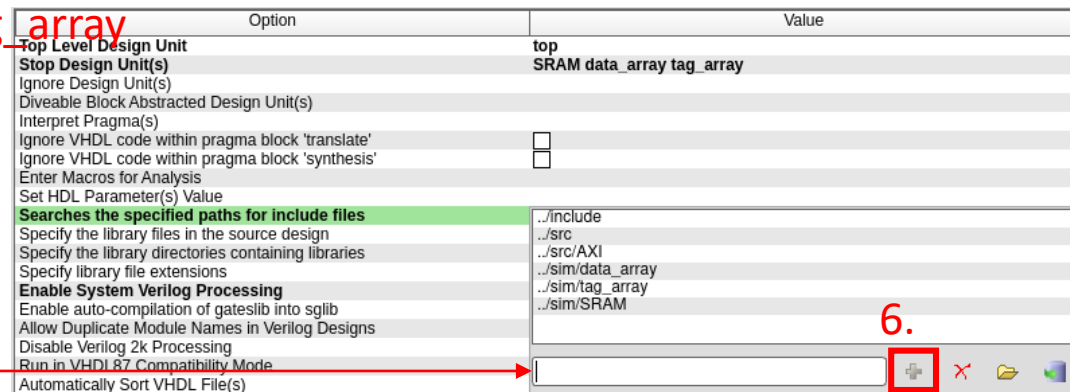
2.

3.

SRAM

data_array

tag_array



5.

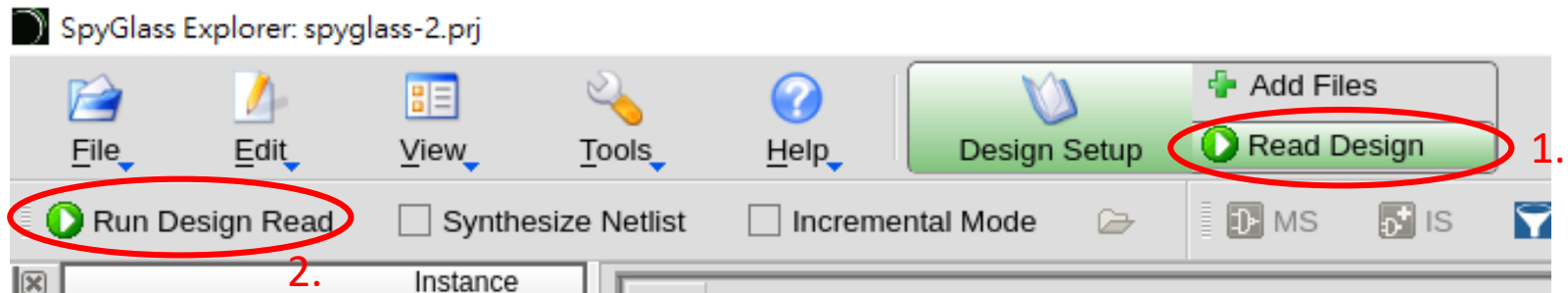
Your include file path

Read design

► Compile and analyze your design

- `current_goal Design_Read -alltop`
- `link_design -force`
- Fatel, Error violations must be resolved in this state

► Every time you modify your design, you need to run “Read Design”



► Or you can source the tcl file at spyglass shell at this homework

- `"source ../script/Spyglass_CDC.tcl"`

CDC verification

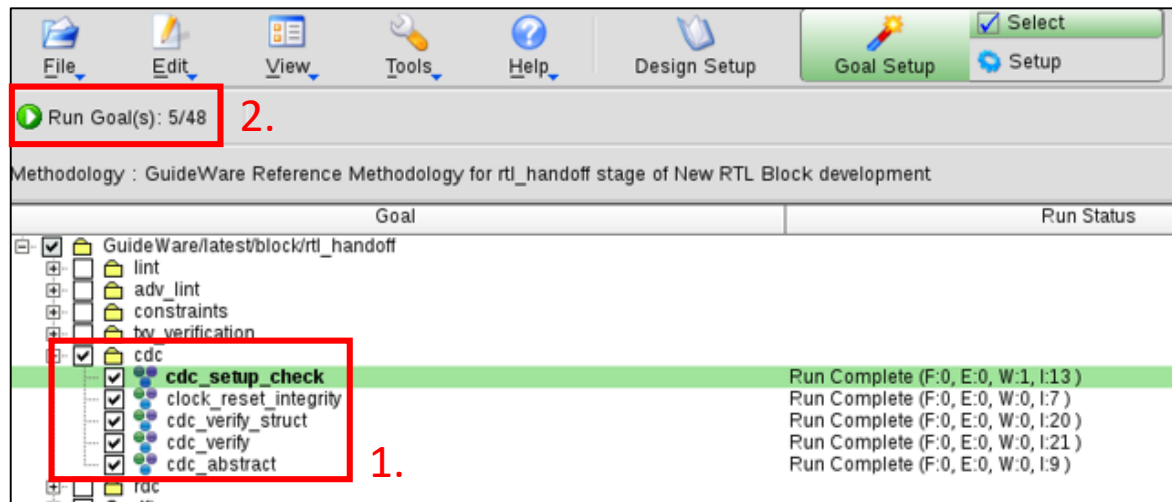
Start CDC check with spyglass

Goal setup

➤ Analyze a specific task “CDC”

Run Goal

➤ It will start to analyze your goal



Violation severity

Analyze results

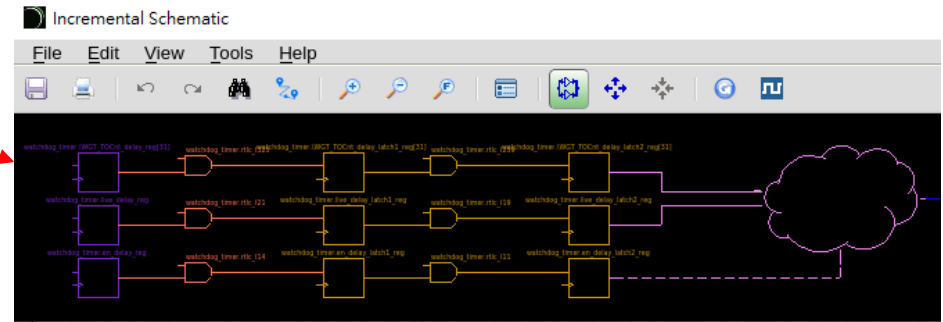
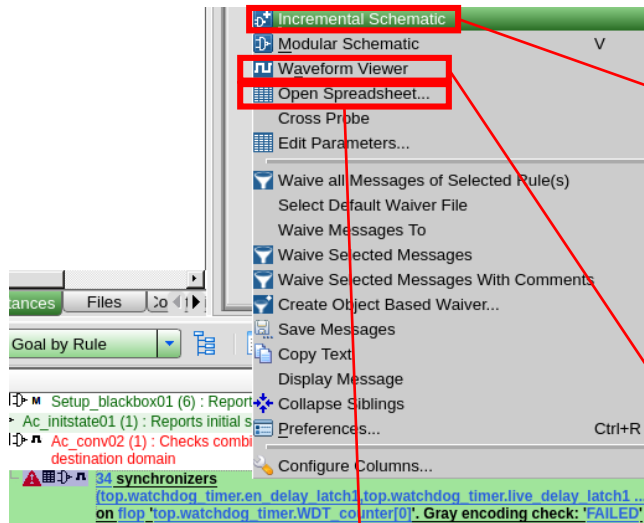
- Fatal
- Error
- Warning
- Information

Fatal, Error, warning violations must be resolved in this state

message	file
<div> <div>Message Tree (Total: 129, Displayed: 129, Waived: 0)</div> <div> <div>Design Read (16)</div> <div>cdc/cdc_verify_struct (113)</div> <div> <div>Reset_info09a (2) : Reports unconstrained asynchronous reset nets</div> <div>Reset_check12 (1) : Reports flops/latches/sequential element that do not get active reset during power on reset</div> <div>Clock_info03b (61) : Flags cases not checked for clock domain crossings as the data pin of flop/latch is tied to constant</div> <div>Setup_port01 (2) : Reports unconstrained ports summary for top design unit</div> <div>Setup_blackbox01 (6) : Reports unconstrained pins summary for black-boxes</div> <div>Ac_conv02 (1) : Checks combinational convergence of same-domain signals synchronized in the same destination domain</div> <div>Ac_crossing01 (1) : Generates spreadsheet for Crossing Matrix view</div> <div>Ac_sync01 (3) : Checks synchronized crossing for scalar signals</div> <div>Ac_sync02 (1) : Checks synchronized crossing for vector signals</div> <div>Clock_info15 (1) : Generates the PortClockMatrix report and abstracted model for input ports</div> <div>Setup_quasi_static01 (1) : Reports likely quasi-static candidates in the design</div> </div> </div> </div>	

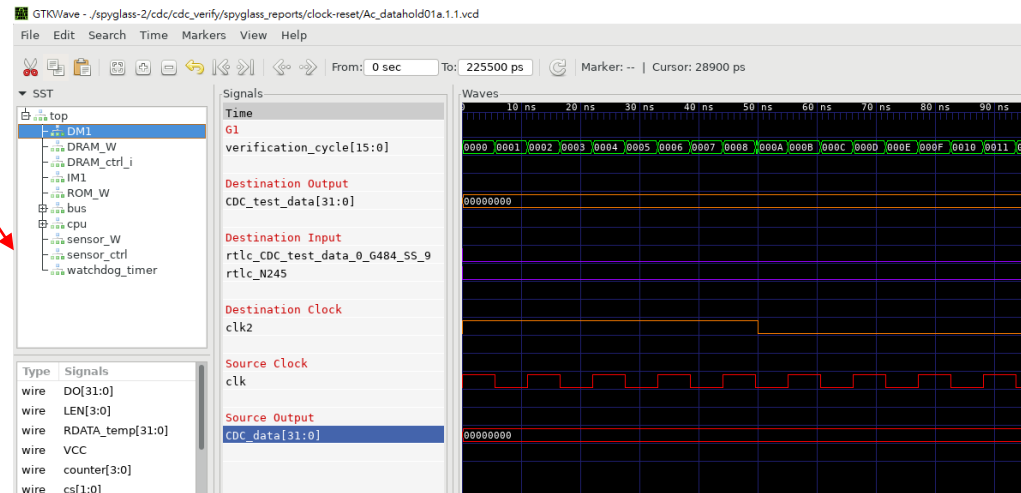
Debugging Violations

- Click “Incremental Schematic” to see simplified schematic
- Click “Open Spreadsheet” to see more detail reason
- Click “Waveform Viewer” to see failure signals



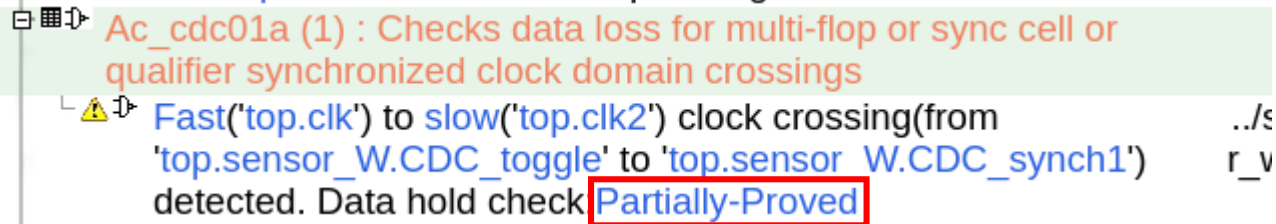
ac_conv_01.csv

	A	B	C	D
	Schematic	Type	Signal Name	Source
1	1	Converging Gate	top.watchdog_timer.WDT_counter[0]	top.watchdog_timer
2	2	Destination flop	top.watchdog_timer.en_delay_latch1	top.watchdog_timer
3	3	Destination flop	top.watchdog_timer.live_delay_latch1	top.watchdog_timer
4	4	Destination flop	top.watchdog_timer.WGT_TOCnt_delay_latch1[31:0]	top.watchdog_timer.WGT_TOCnt



Partially-proved warning

- Spyglass provides the number of cycles that have been explored during which no violation has been found.



- Set the fa_atime parameter to increase the amount of time that Spyglass spends on validating a single property.
 - "Set_parameter fa_time 100"

```
sg_shell> set_parameter fa_atime 100
100
sg_shell>
```