JasperGold ABVIP Tutorial

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EE

LPHPLAB
VLSI Design LAB

Outline

- □ Introduction of ABVIP for AXI
- □ ABVIP Tool Guide

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Introduction of ABVIP for AXI

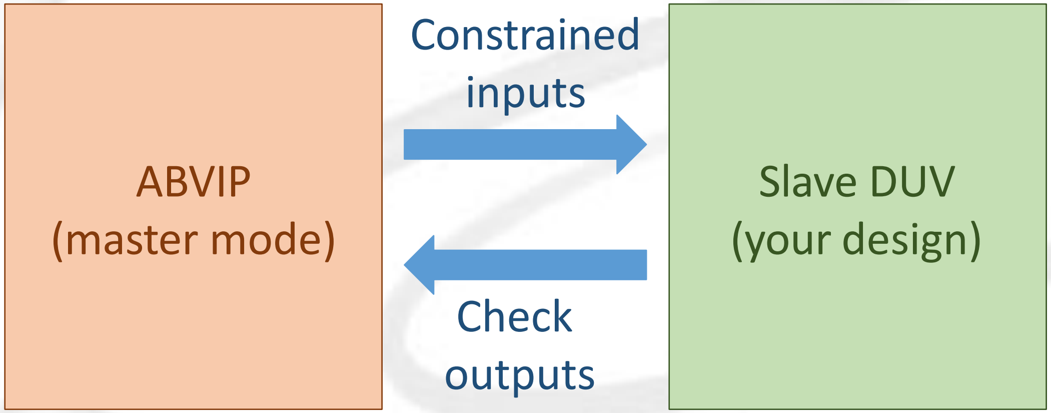
- □ Assertion-Based Verification Intellectual Property (ABVIP) consists of libraries for verifying the compliance of DUT to a given standard protocol.
- □ Can be used to automatically constrain inputs and target outputs of standard bus interfaces using built-in protocol properties.
- □ Consist of RTL written in SystemVerilog and assertions written in SVA.
- □ You won’t need to manually write properties!

Introduction of ABVIP for AXI

- In formal verification, the ABVIP acts as an active agent or as a passive agent.
  - Active Agent Use model: Constrain interface to act as virtual master(s) or slave(s) to verify Slave DUV or Master DUV respectively. For bridge or interconnect verification, multiple ABVIP instances can be used to constrain input interface signals to act as virtual slave(s) and master(s) to verify Bridge DUV .
  - Passive Agent Use model: Check for protocol errors.
  - Do extensive coverage measurements.

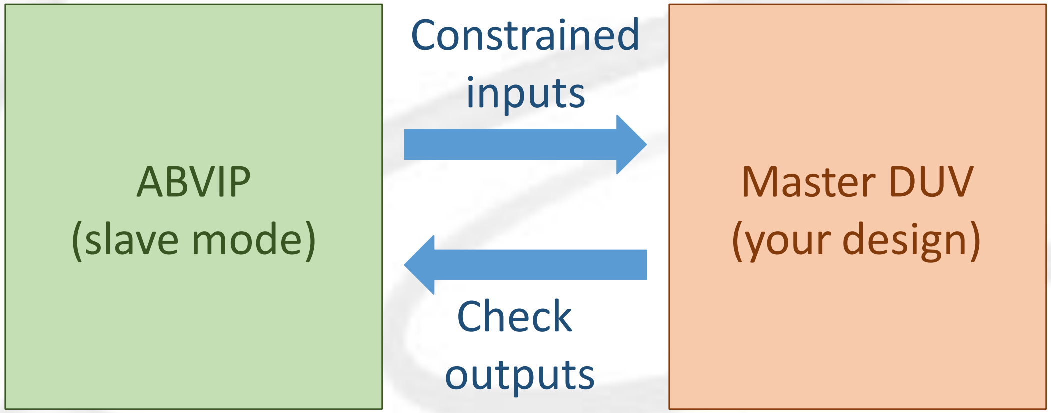
Slave DUV

- ABVIP act as a virtual master, which provides the correct AXI constraints on slave inputs.
- ABVIP provides the required AXI assertions on slave outputs to verify the functionality of Slave DUV.



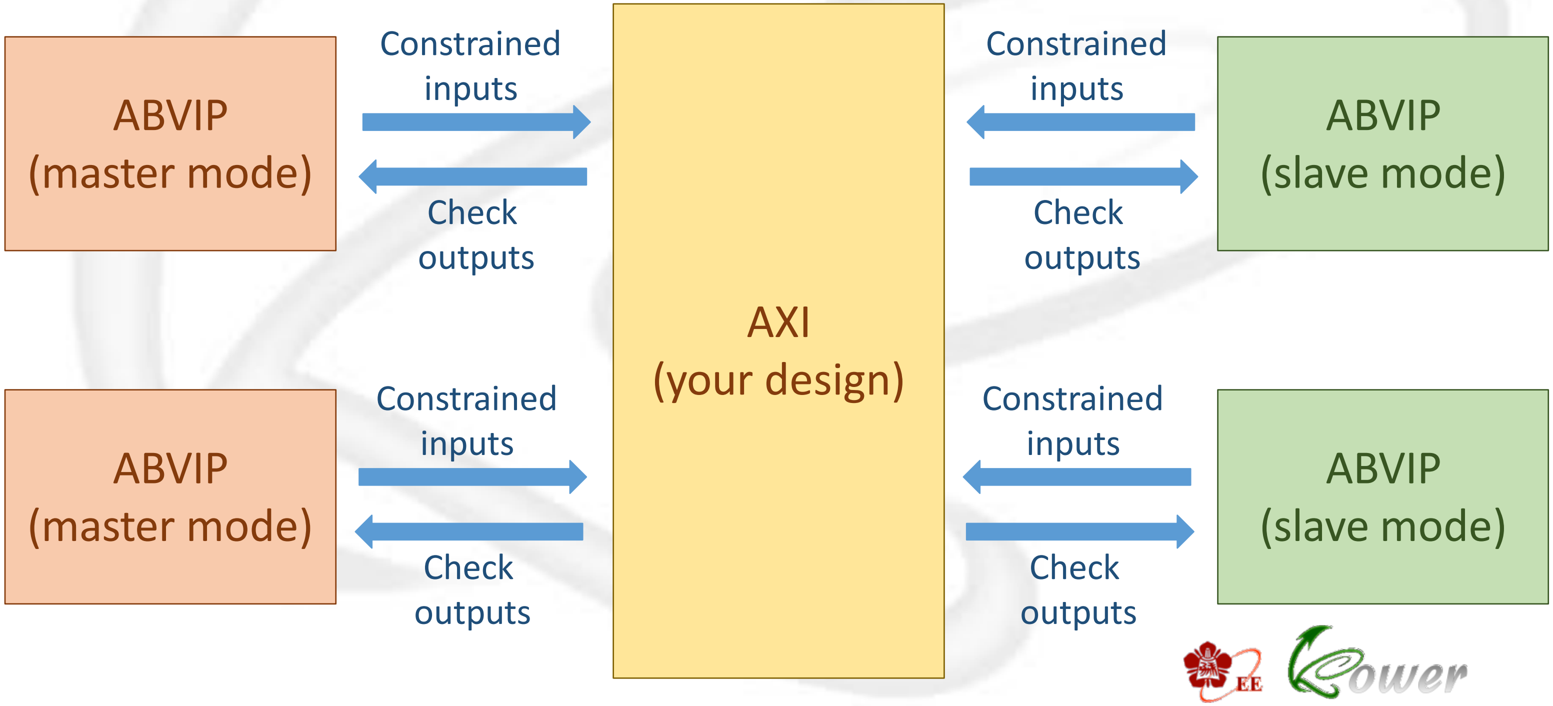
Master DUV

- ABVIP act as a virtual slave, which provides the correct AXI constraints on master inputs.
- ABVIP provides the required AXI assertions on master outputs to verify the functionality of Master DUV.



Bridge DUV

- ABVIP act as virtual slaves and masters, which provides the correct AXI constraints on bridge inputs.
- ABVIP provides the required AXI assertions on bridge outputs to verify the functionality of Bridge DUV.
- The configuration can be cascaded adding to the interconnection.



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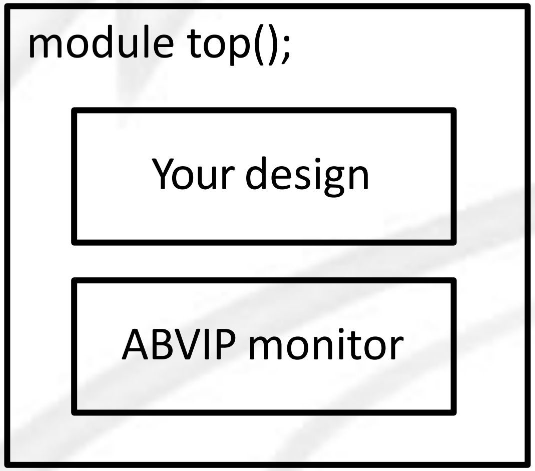
ABVIP Tool Guide

- You should bind your design in
  - vip/bridge_duv/top.v
  - vip/master_duv/top.v
  - vip/slave_duv/top.v

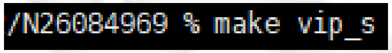


module top();

Your design

ABVIP monitor

- Run %make vip_b/vip_m/vip_s

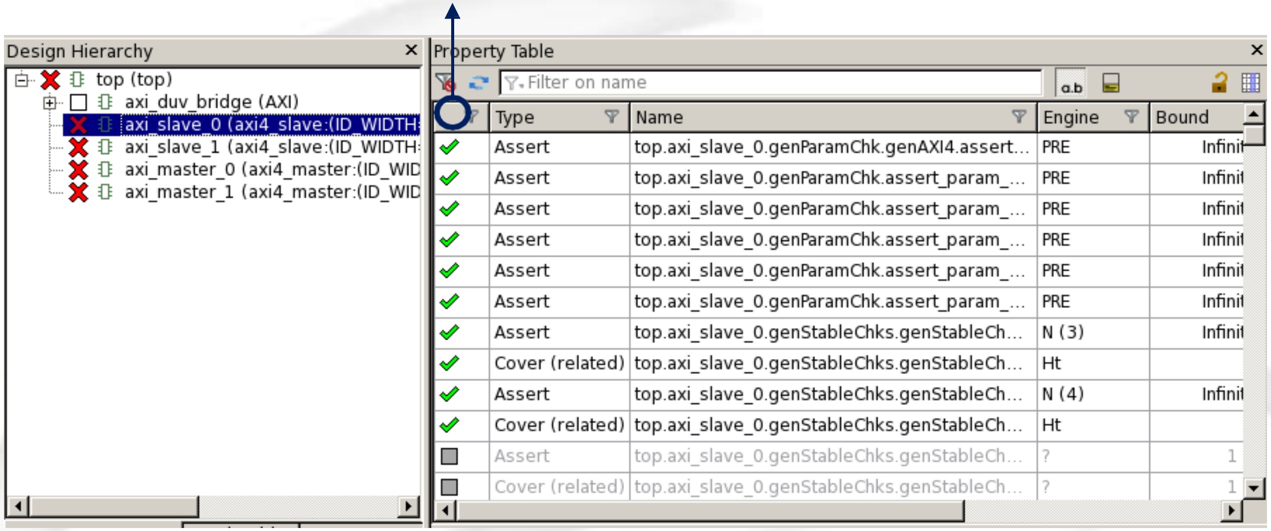


```
/N26084969 % make vip_s
```

  - Run script

ABVIP Tool Guide

sort



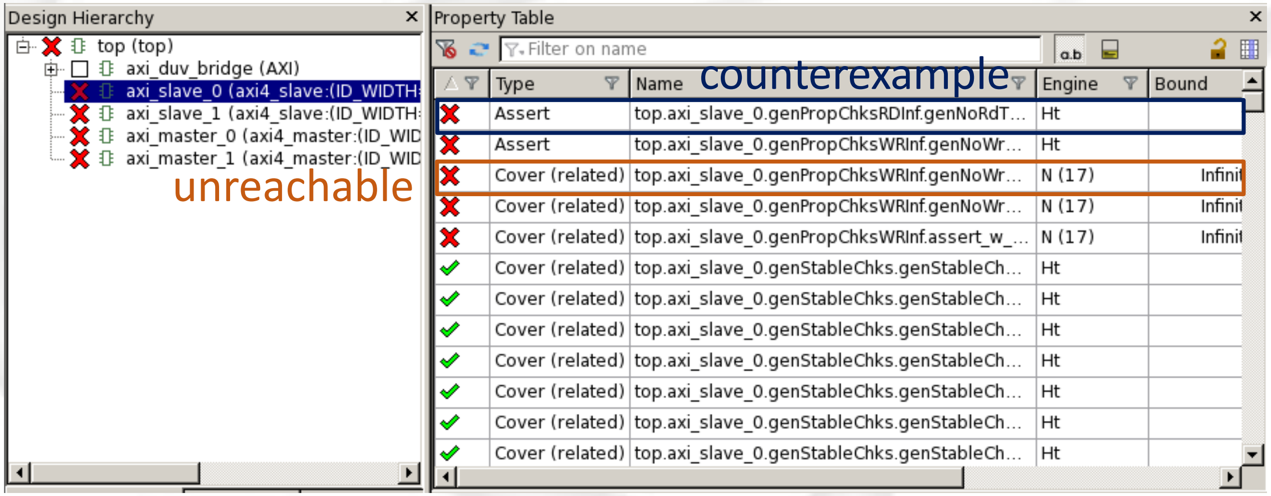
Design Hierarchy

- ✗ top (top)
  - □ axi_duv_bridge (AXI)
  - ✗ axi_slave_0 (axi4_slave:(ID_WIDTH=
  - ✗ axi_slave_1 (axi4_slave:(ID_WIDTH=
  - ✗ axi_master_0 (axi4_master:(ID_WID
  - ✗ axi_master_1 (axi4_master:(ID_WID

Property Table

Filter on name

	Type	Name	Engine	Bound
✓	Assert	top.axi_slave_0.genParamChk.genAXI4.assert...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genStableChks.genStableCh...	N (3)	Infinit
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
✓	Assert	top.axi_slave_0.genStableChks.genStableCh...	N (4)	Infinit
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
■	Assert	top.axi_slave_0.genStableChks.genStableCh...	?	1
■	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	?	1



Design Hierarchy

- ✗ top (top)
  - □ axi_duv_bridge (AXI)
  - ✗ axi_slave_0 (axi4_slave:(ID_WIDTH=
  - ✗ axi_slave_1 (axi4_slave:(ID_WIDTH=
  - ✗ axi_master_0 (axi4_master:(ID_WID
  - ✗ axi_master_1 (axi4_master:(ID_WID

unreachable

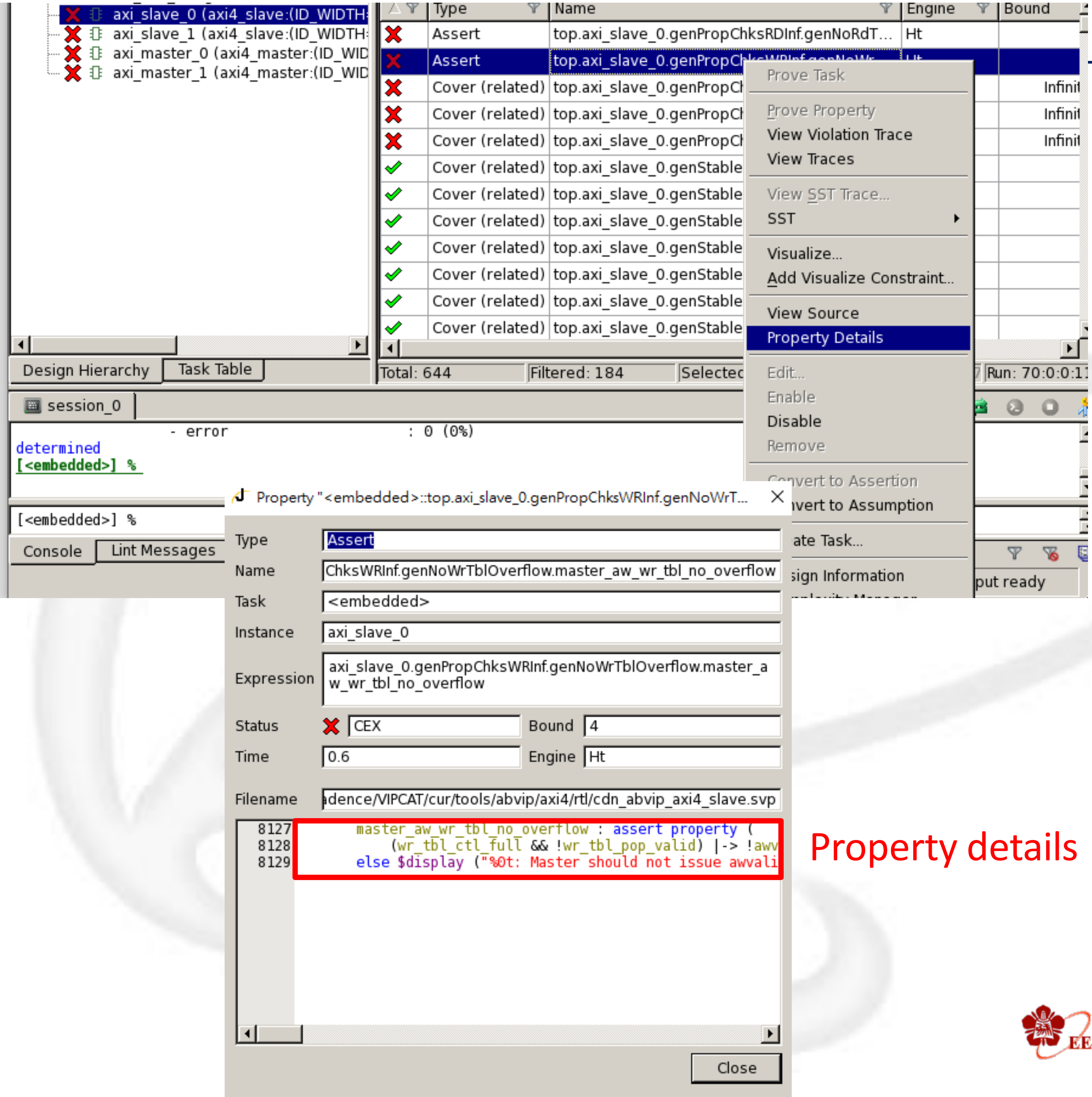
Property Table

Filter on name

counterexample

	Type	Name	Engine	Bound
✗	Assert	top.axi_slave_0.genPropChksRDInf.genNoRdT...	Ht	
✗	Assert	top.axi_slave_0.genPropChksWRInf.genNoWr...	Ht	
✗	Cover (related)	top.axi_slave_0.genPropChksWRInf.genNoWr...	N (17)	Infinit
✗	Cover (related)	top.axi_slave_0.genPropChksWRInf.genNoWr...	N (17)	Infinit
✗	Cover (related)	top.axi_slave_0.genPropChksWRInf.assert_w_...	N (17)	Infinit
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	

ABVIP Tool Guide



Type	Name	Engine	Bound
✗ Assert	top.axi_slave_0.genPropChksRDInf.genNoRdT...	Ht	
✗ Assert	top.axi_slave_0.genPropChksWRInf.genNoWr...	Ht	
✗ Cover (related)	top.axi_slave_0.genPropCh		Infinit
✗ Cover (related)	top.axi_slave_0.genPropCh		Infinit
✗ Cover (related)	top.axi_slave_0.genPropCh		Infinit
✓ Cover (related)	top.axi_slave_0.genStable		
✓ Cover (related)	top.axi_slave_0.genStable		
✓ Cover (related)	top.axi_slave_0.genStable		
✓ Cover (related)	top.axi_slave_0.genStable		
✓ Cover (related)	top.axi_slave_0.genStable		
✓ Cover (related)	top.axi_slave_0.genStable		
✓ Cover (related)	top.axi_slave_0.genStable		

Total: 644 Filtered: 184 Selectec ... Run: 70:0:0:1

```
                    - error                          : 0 (0%)
determined
[<embedded>] %
```

```
[<embedded>] %
```

put ready

Property "<embedded>::top.axi_slave_0.genPropChksWRInf.genNoWrT...

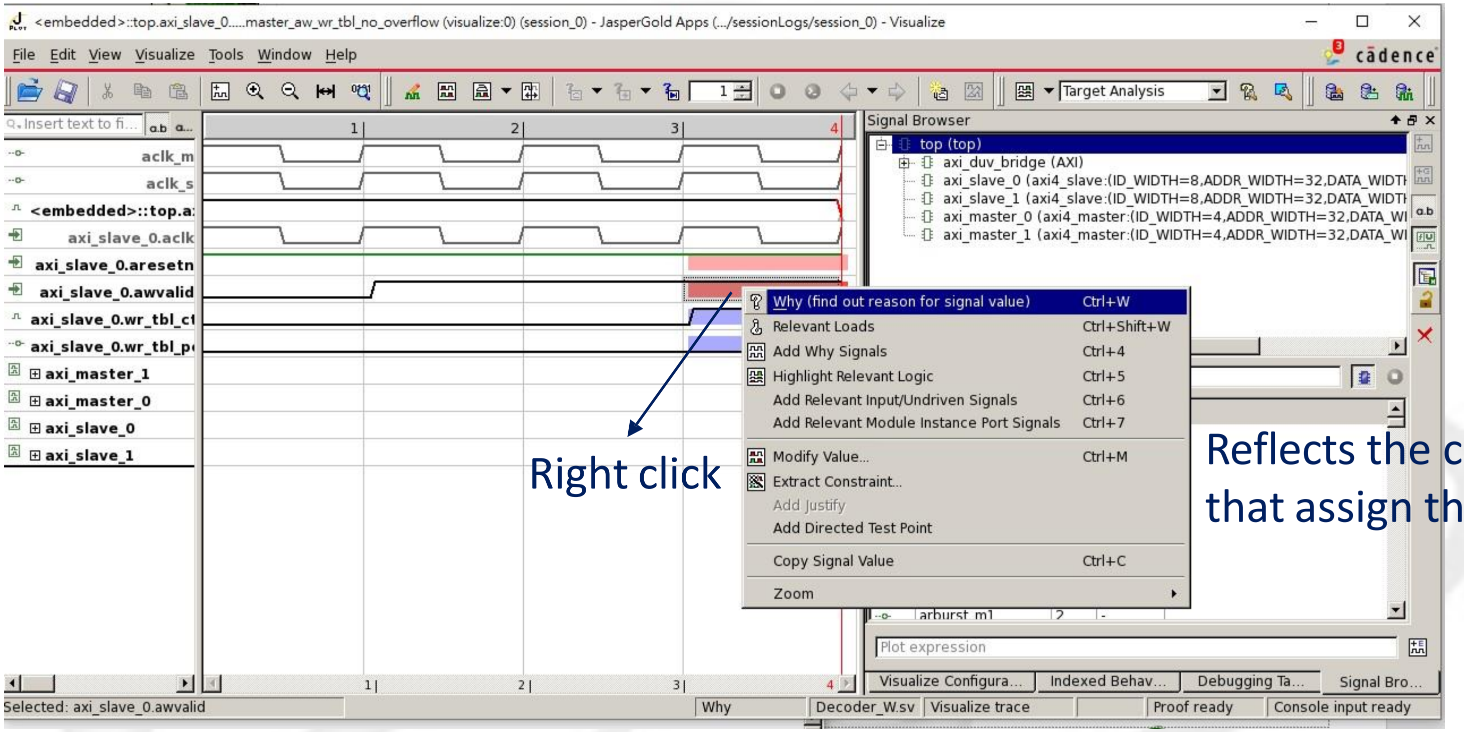
Type	Assert
Name	ChksWRInf.genNoWrTblOverflow.master_aw_wr_tbl_no_overflow
Task	<embedded>
Instance	axi_slave_0
Expression	axi_slave_0.genPropChksWRInf.genNoWrTblOverflow.master_aw_wr_tbl_no_overflow
Status	✗ CEX
Bound	4
Time	0.6
Engine	Ht
Filename	dence/VIPCAT/cur/tools/abvip/axi4/rtl/cdn_abvip_axi4_slave.svp

```
      master_aw_wr_tbl_no_overflow : assert property (
          (wr_tbl_ctl_full && !wr_tbl_pop_valid) |-> !awv
      else $display ("%0t: Master should not issue awvali
```

Right click

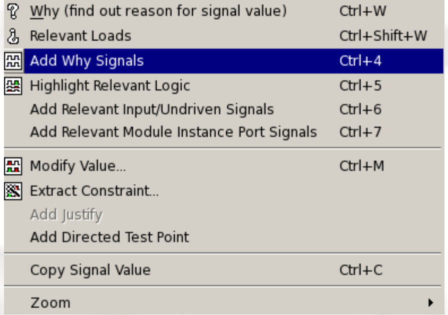
Property details

ABVIP Tool Guide


<embedded>::top.axi_slave_0.....master_aw_wr_tbl_no_overflow (visualize:0) (session_0) - JasperGold Apps (.../sessionLogs/session_0) - Visualize
File Edit View Visualize Tools Window Help
cadence
Target Analysis
Insert text to fi...
aclk_m
aclk_s
<embedded>::top.a
axi_slave_0.aclk
axi_slave_0.aresetn
axi_slave_0.awvalid
axi_slave_0.wr_tbl_ct
axi_slave_0.wr_tbl_p
axi_master_1
axi_master_0
axi_slave_0
axi_slave_1
Signal Browser
top (top)
axi_duv_bridge (AXI)
axi_slave_0 (axi4_slave:(ID_WIDTH=8,ADDR_WIDTH=32,DATA_WIDTH
axi_slave_1 (axi4_slave:(ID_WIDTH=8,ADDR_WIDTH=32,DATA_WIDTH
axi_master_0 (axi4_master:(ID_WIDTH=4,ADDR_WIDTH=32,DATA_WI
axi_master_1 (axi4_master:(ID_WIDTH=4,ADDR_WIDTH=32,DATA_WI
Why (find out reason for signal value) Ctrl+W
Relevant Loads Ctrl+Shift+W
Add Why Signals Ctrl+4
Highlight Relevant Logic Ctrl+5
Add Relevant Input/Undriven Signals Ctrl+6
Add Relevant Module Instance Port Signals Ctrl+7
Modify Value... Ctrl+M
Extract Constraint...
Add Justify
Add Directed Test Point
Copy Signal Value Ctrl+C
Zoom
arburst_m1
Plot expression
Visualize Configura...
Indexed Behav...
Debugging Ta...
Signal Bro...
Selected: axi_slave_0.awvalid
Why
Decoder_W.sv
Visualize trace
Proof ready
Console input ready

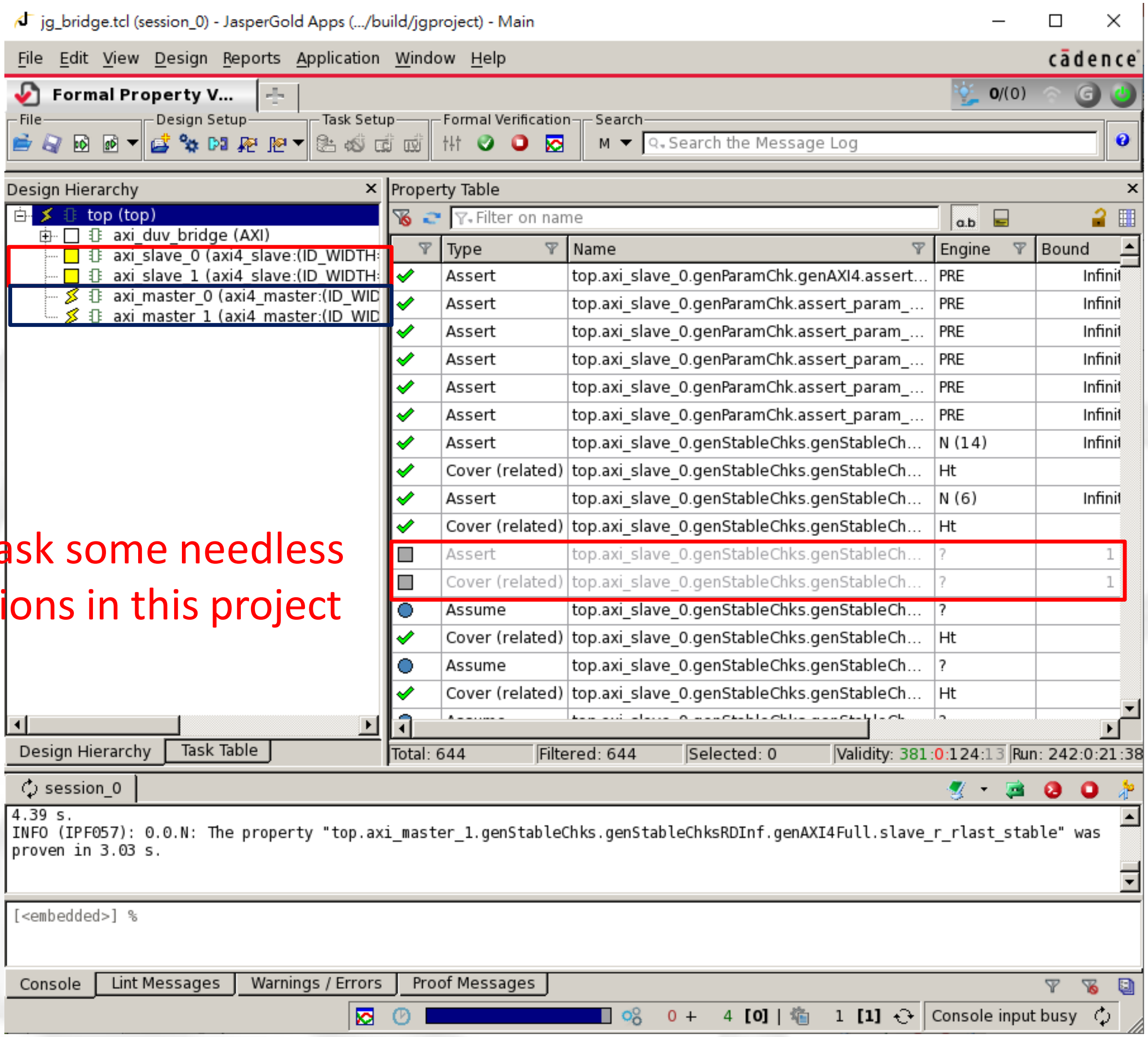
Right click

Reflects the code that assign the value


Why (find out reason for signal value) Ctrl+W
Relevant Loads Ctrl+Shift+W
Add Why Signals Ctrl+4
Highlight Relevant Logic Ctrl+5
Add Relevant Input/Undriven Signals Ctrl+6
Add Relevant Module Instance Port Signals Ctrl+7
Modify Value... Ctrl+M
Extract Constraint...
Add Justify
Add Directed Test Point
Copy Signal Value Ctrl+C
Zoom

Reflects the signals related to current signal

ABVIP Tool Guide



jg_bridge.tcl (session_0) - JasperGold Apps (.../build/jgproject) - Main

pass

processing

We mask some needless assertions in this project

Design Hierarchy:

- top (top)
  - axi_duv_bridge (AXI)
  - axi_slave_0 (axi4_slave:(ID_WIDTH:
  - axi_slave_1 (axi4_slave:(ID_WIDTH:
  - axi_master_0 (axi4_master:(ID_WIC
  - axi_master_1 (axi4_master:(ID_WIC

Property Table:

	Type	Name	Engine	Bound
✓	Assert	top.axi_slave_0.genParamChk.genAXI4.assert...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genParamChk.assert_param_...	PRE	Infinit
✓	Assert	top.axi_slave_0.genStableChks.genStableCh...	N (14)	Infinit
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
✓	Assert	top.axi_slave_0.genStableChks.genStableCh...	N (6)	Infinit
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
■	Assert	top.axi_slave_0.genStableChks.genStableCh...	?	1
■	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	?	1
●	Assume	top.axi_slave_0.genStableChks.genStableCh...	?	
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
●	Assume	top.axi_slave_0.genStableChks.genStableCh...	?	
✓	Cover (related)	top.axi_slave_0.genStableChks.genStableCh...	Ht	
●	Assume	top.axi_slave_0.genStableChks.genStableCh...	?	

Total: 644 | Filtered: 644 | Selected: 0 | Validity: 381:0:124:13 | Run: 242:0:21:38

```
4.39 s.
INFO (IPF057): 0.0.N: The property "top.axi_master_1.genStableChks.genStableChksRDInf.genAXI4Full.slave_r_rlast_stable" was
proven in 3.03 s.
```

```
[<embedded>] %
```

Thanks for your participation and attendance !