Spyglass CDC verification

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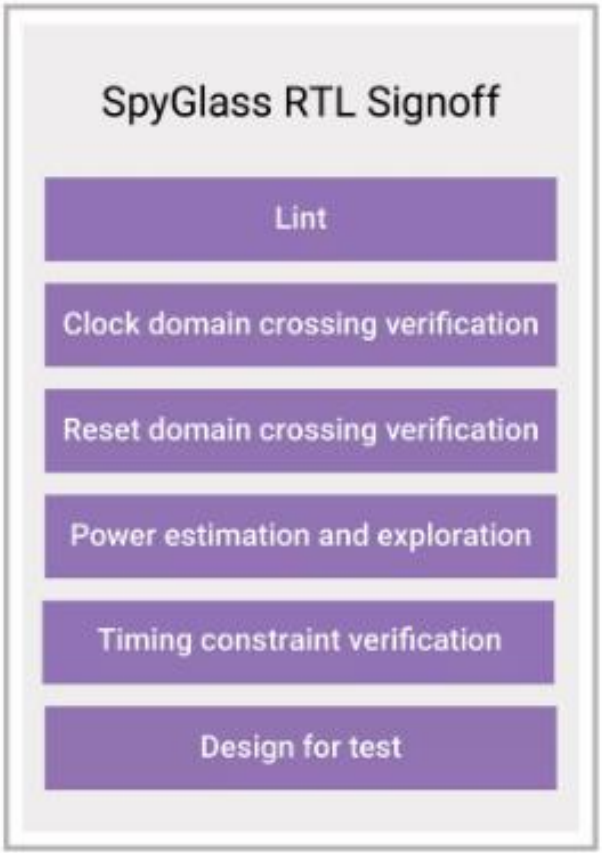
Outline

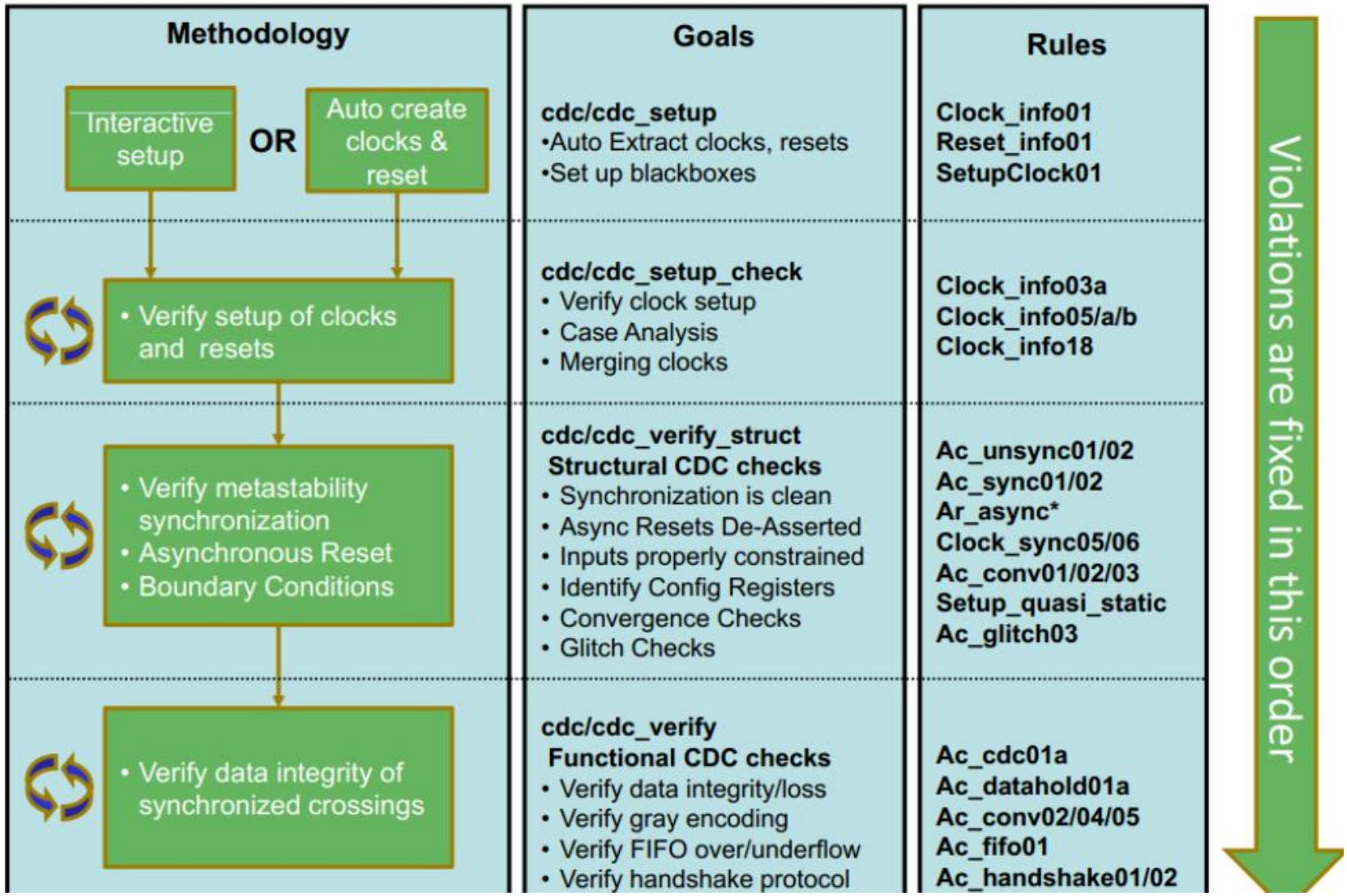
- Introduction
- Import design
- CDC verification

Introduction

- Spyglass is the early design analysis tool enabled efficient verification and optimization of soc designs
- With this tool, designers can gain insight into their designs early in the RTL process.
  - Lint, CDC, LP, DFT, Constraint



Spyglass CDC verification flow



Open GUI

- [spyglass/build] $ spyglass
- [spyglass] $ make spyglass
  - In this exercise & homework

```
[               N26101039_mul]$ make spyglass
maxpend=1
cd ./build; \
spyglass

                                SpyGlass (R)
                            Synopsys TestMAX(TM)

                  Version P-2019.06 for linux64 - Jun 02, 2019

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```
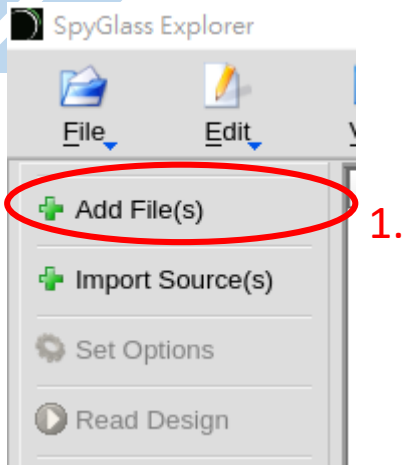
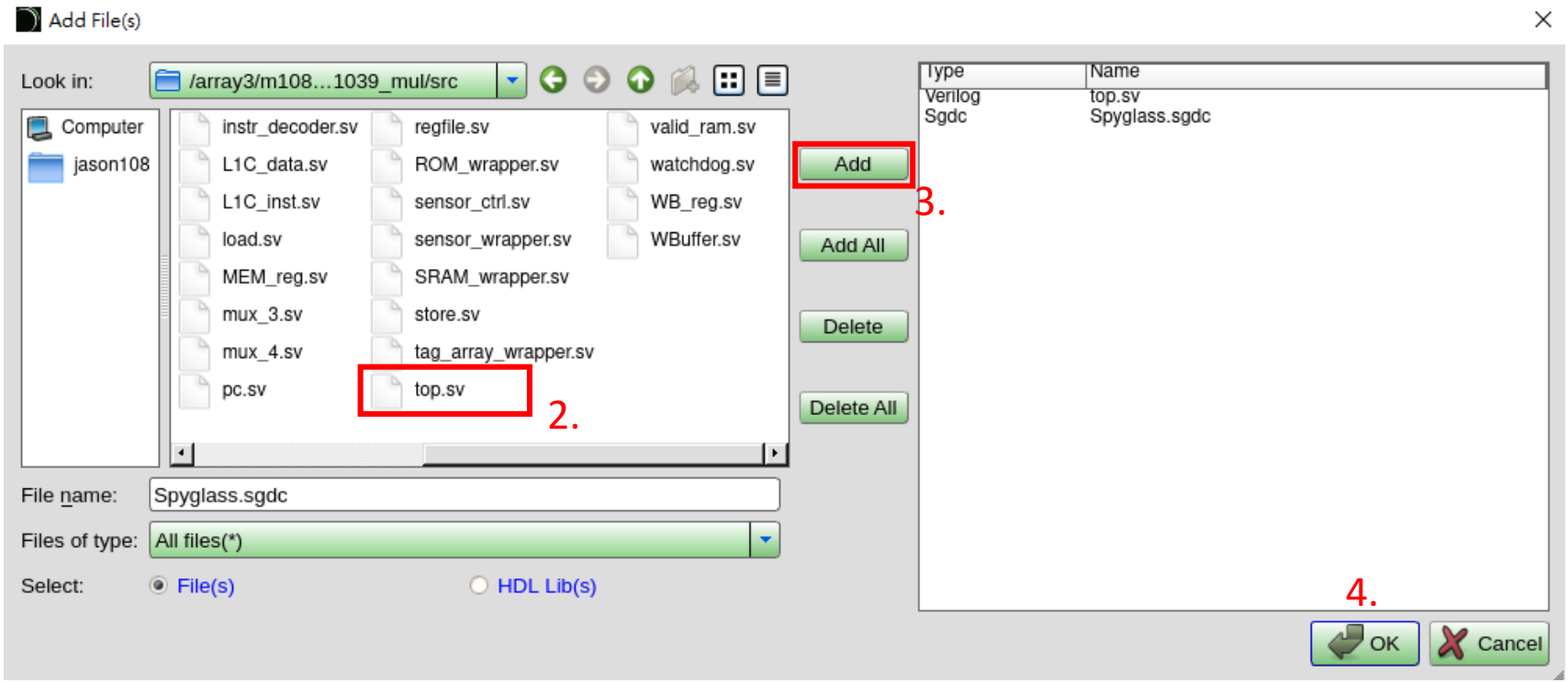

Import design

Import design

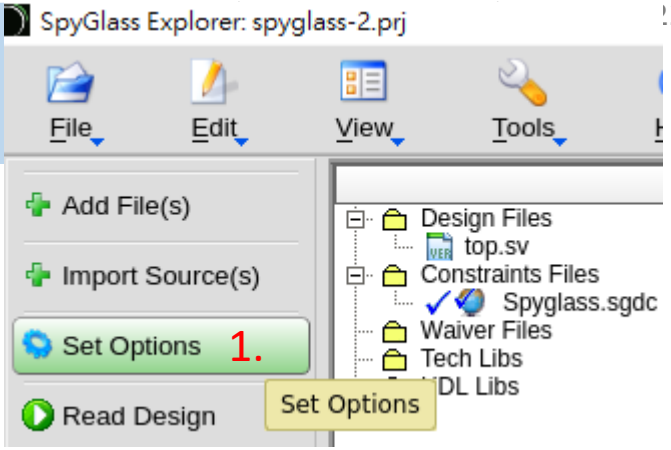
- Read design file(.v/.sv)
  - read_file –type verilog “top module file”
  - read_file -type sgdc “sgdc file”

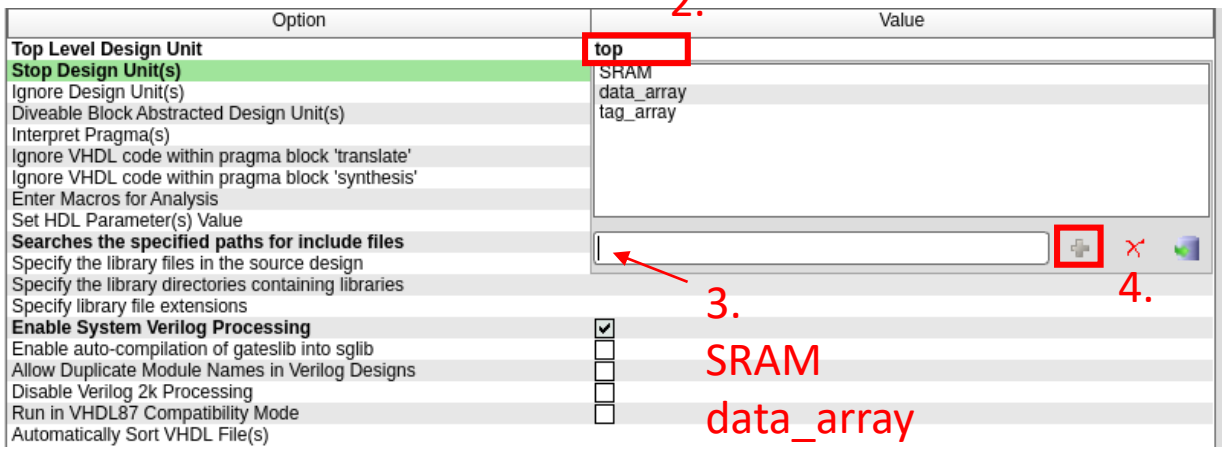




Option settings

- Read design & constraint file
  - set_option top “top module name”
  - set_option stop “blackbox module name”
  - set_option incdir “path”
  - set_option enableSV yes

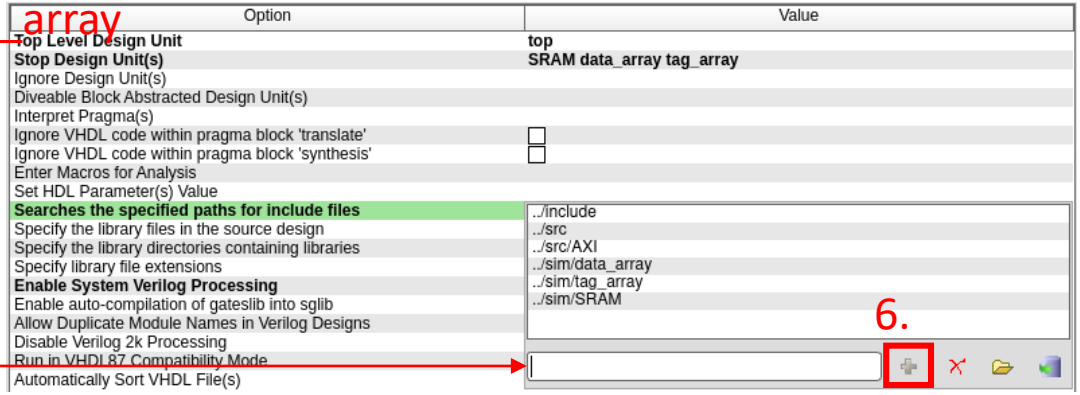




SRAM

data_array

tag_array



5.

Your include file path

Read design

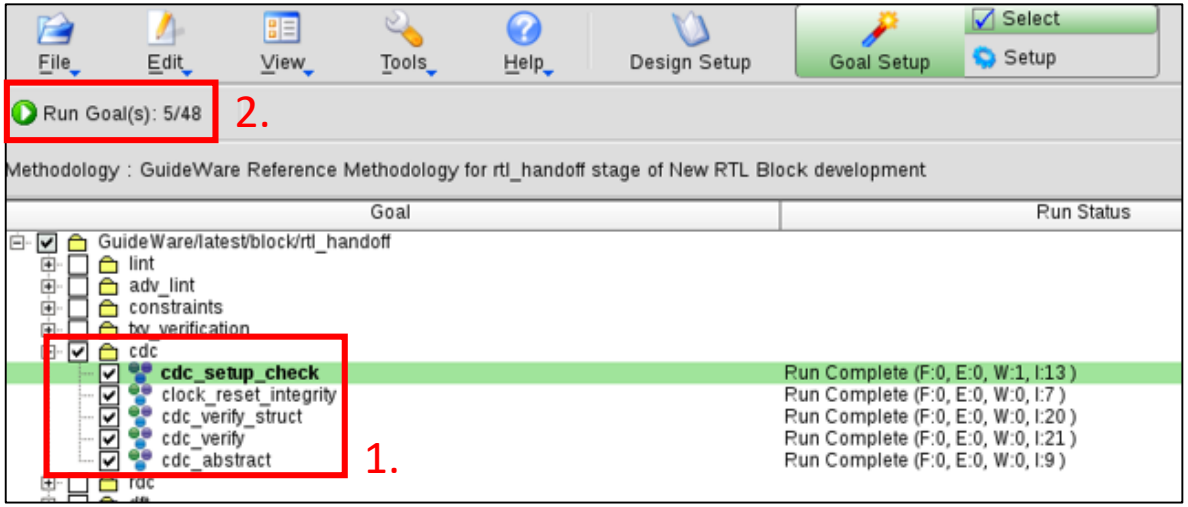
- Compile and analyze your design
  - current_goal Design_Read -alltop
  - link_design –force
  - Fatel, Error violations must be resolved in this state
- Every time you modify your design, you need to run “Read Design”

- Or you can source the tcl file at spyglass shell at this homework
  - “source ../script/Spyglass_CDC.tcl”

CDC verification

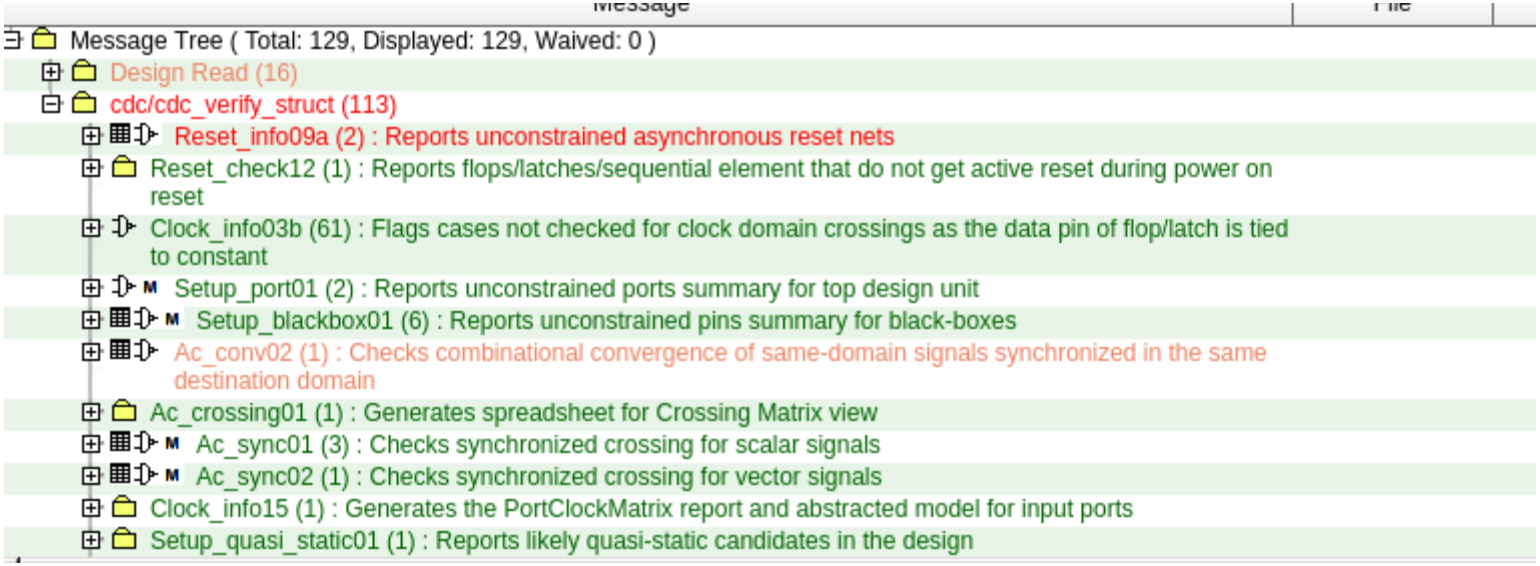
Start CDC check with spyglass

- Goal setup
  - Analyze a specific task “CDC”
- Run Goal
  - It will start to analyze your goal



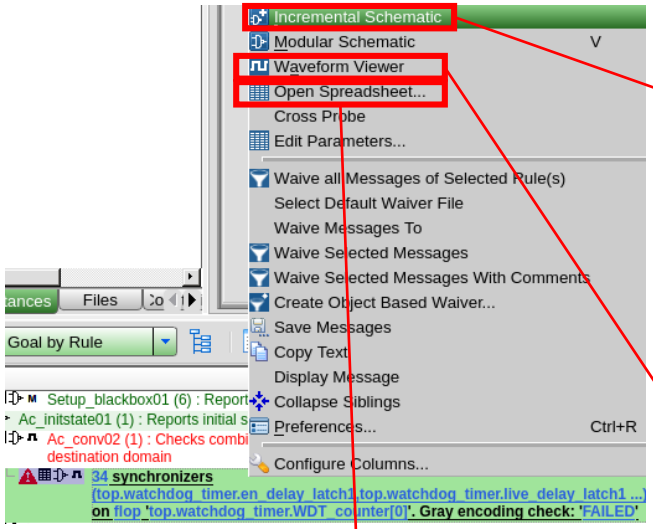
Violation severity

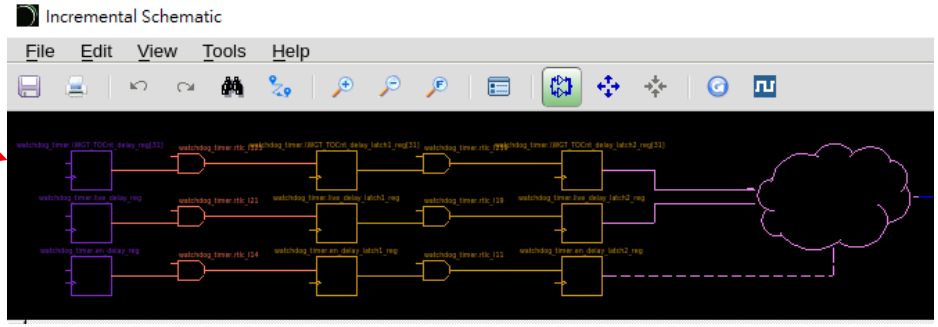
- Analyze results
  - Fatal
  - Error
  - Warning
  - Information
- Fatal, Error, warning violations must be resolved in this state

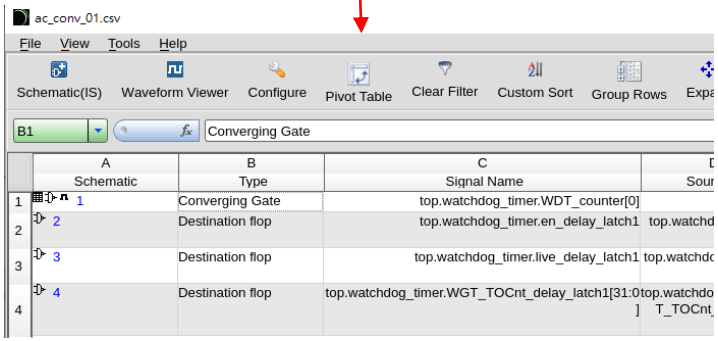


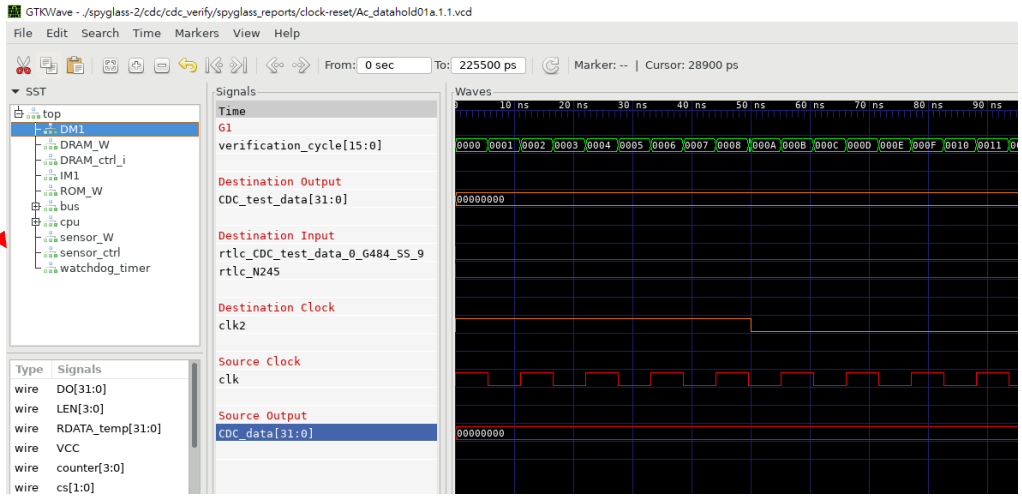
Debugging Violations

- Click “Incremental Schematic” to see simplified schematic
- Click “Open Spreadsheet” to see more detail reason
- Click “Waveform Viewer” to see failure signals



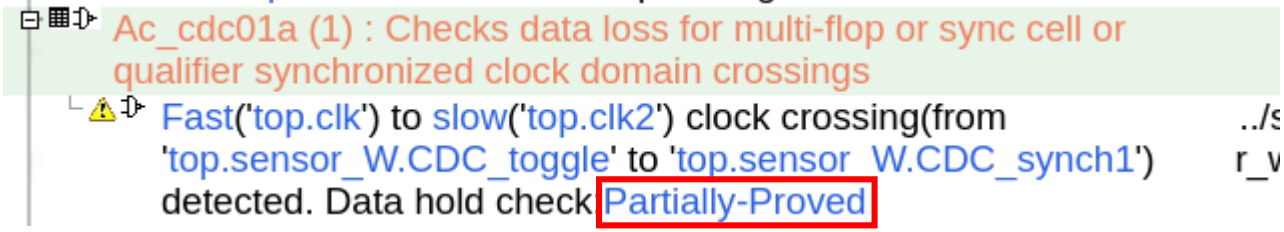






Partially-proved warning

- Spyglass provides the number of cycles that have been explored during which no violation has been found.



- Set the fa_atime parameter to increase the amount of time that Spyglass spends on validating a single property.
  - "Set_parameter fa_time 100"

```
sg_shell> set_parameter fa_atime 100
100
sg_shell>
```