

# Tutorial 1

## Using NC-Verilog & nWave

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# Outline

1. Introduction
2. Compiling & Simulating using NC-Verilog
3. Viewing Waveform using nWave

# Introduction (1/2)

- **NC-Verilog** is a HDL Simulator tool developed by **Cadence**.
- HDL is abbreviation of **Hardware Description Language**
- **Main function:**
  - Check HDL code for syntax error
  - Simulate and dump waveform
  - Support co-simulation on behavioral, RTL, Gate-level



# Introduction (2/2)

- **Verdi** is an HDL Debug and Analysis tool developed by **Spring Software**.
- **Function**
  - Trace HDL source code
  - Schematic diagram
  - Waveform
  - State diagram.

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# Compiling & Simulating Using NC-Verilog(1/4)

- To compile & simulate the verilog code:

- Only Compile the test1.v

> **ncverilog** test1.v

- Compile & simulate the test1.v & test\_tb.v

> **ncverilog** test\_tb.v +define+T1 +access+r

Choose test1.v

Dump .fsdb file

- Compile & simulate the test2.v & test\_tb.v

> **ncverilog** test\_tb.v +define+T2 +access+r

Choose test2.v

Dump .fsdb file

# Compiling & Simulating Using NC-Verilog(2/4)

```
[eric109@LPHP3 source]$ ncverilog test_tb.v +define+T1 +access+r
ncverilog(64): 15 20-s000 (4) Copyright 1995-2017 Cadence Design Systems, Inc.
file: test_tb.v
```

Command

```
module worklib.test1:v
  errors: 0, warnings: 0
module worklib.test_tb:v
  errors: 0, warnings: 0
  Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Building instance overlay tables: ..... Done
Generating native compiled code:
  worklib.test1:v <0x6344732d>
    streams: 0, words: 0
  worklib.test_tb:v <0x3ab8750b>
    streams: 6, words: 10196
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances  Unique
Modules:           2      2
Registers:         3      3
Scalar wires:      4      -
Initial blocks:    4      4
Cont. assignments: 0      2
Pseudo assignments: 2      2
Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.test_tb:v
Loading snapshot worklib.test_tb.v ..... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
```

Compiling results & error messages

```
*****
**                                     **
** Congratulations !!                 **
** No Syntax Error!!                 **
**                                     **
*****
                                     |__|
                                     / 0.0 |
                                     / ^ ^ \
                                     | ^ ^ ^ |w|
                                     \m_m_|

0ns in1=0 , in2=1 , out1=0 , out2=1
10ns in1=1 , in2=1 , out1=1 , out2=1
20ns in1=0 , in2=0 , out1=0 , out2=0
30ns in1=1 , in2=0 , out1=0 , out2=1
Simulation complete via $finish(1) at time 40 NS + 0
./test_tb.v:67 #10 $finish;
ncsim> exit
```

Simulation results

# Compiling & Simulating Using NC-Verilog(3/4)

- Three NC-Verilog message levels
  - Warning message - indicate that there may be something wrong with the model and continue to run
  - Error message - indicate that a user error has occurred at compile time or at run time
  - Information message - provide information about your source description



# Compiling & Simulating Using NC-Verilog(4/4)

- Error messages

```

vlsicad6:/home/user2/ms104/patty/VSD2016/Lab1/ ncverilog test_tb.sv +define+test2 +access+r +sv
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: test_tb.sv
      out3
      |
ncvlog: *E,ILLPDL (test2.sv,3|16): Mixing of ansi & non-ansi style port declaration is not legal
(`include file: test2.sv line 4, file: test_tb.sv line 6)
input  in1, in2;
      |
ncvlog: *E,EXPSMC (test2.sv,7|14): expecting a semicolon(';') [12.1(IEEE)].
(`include file: test2.sv line 7, file: test_tb.sv line 6)
output out1 out2, out3;
      |
ncvlog: *E,ILLPDL (test2.sv,8|10): Mixing of ansi & non-ansi style port declaration is not legal
(`include file: test2.sv line 8, file: test_tb.sv line 6)
output out1 out2, out3;
      |
ncvlog: *E,SVNOTY (test2.sv,8|10): Syntactically this identifier appears to begin a datatype but
it does not refer to a visible datatype in the current scope.
(`include file: test2.sv line 8, file: test_tb.sv line 6)
assign out2 = in1 | in2; // in1 or in2
      |
ncvlog: *E,EXPSMC (test2.sv,11|15): expecting a semicolon(';') [6.1(IEEE)].
(`include file: test2.sv line 11, file: test_tb.sv line 6)
      module worklib,test1:sv
          errors: 5, warnings: 0
          in1 = 0; in2 = 1;
          |
ncvlog: *E,WANOTL (test_tb.sv,29|9): A net is not a legal lvalue in this context [9.3.1(IEEE)].
          in1 = 0; in2 = 1;
          |

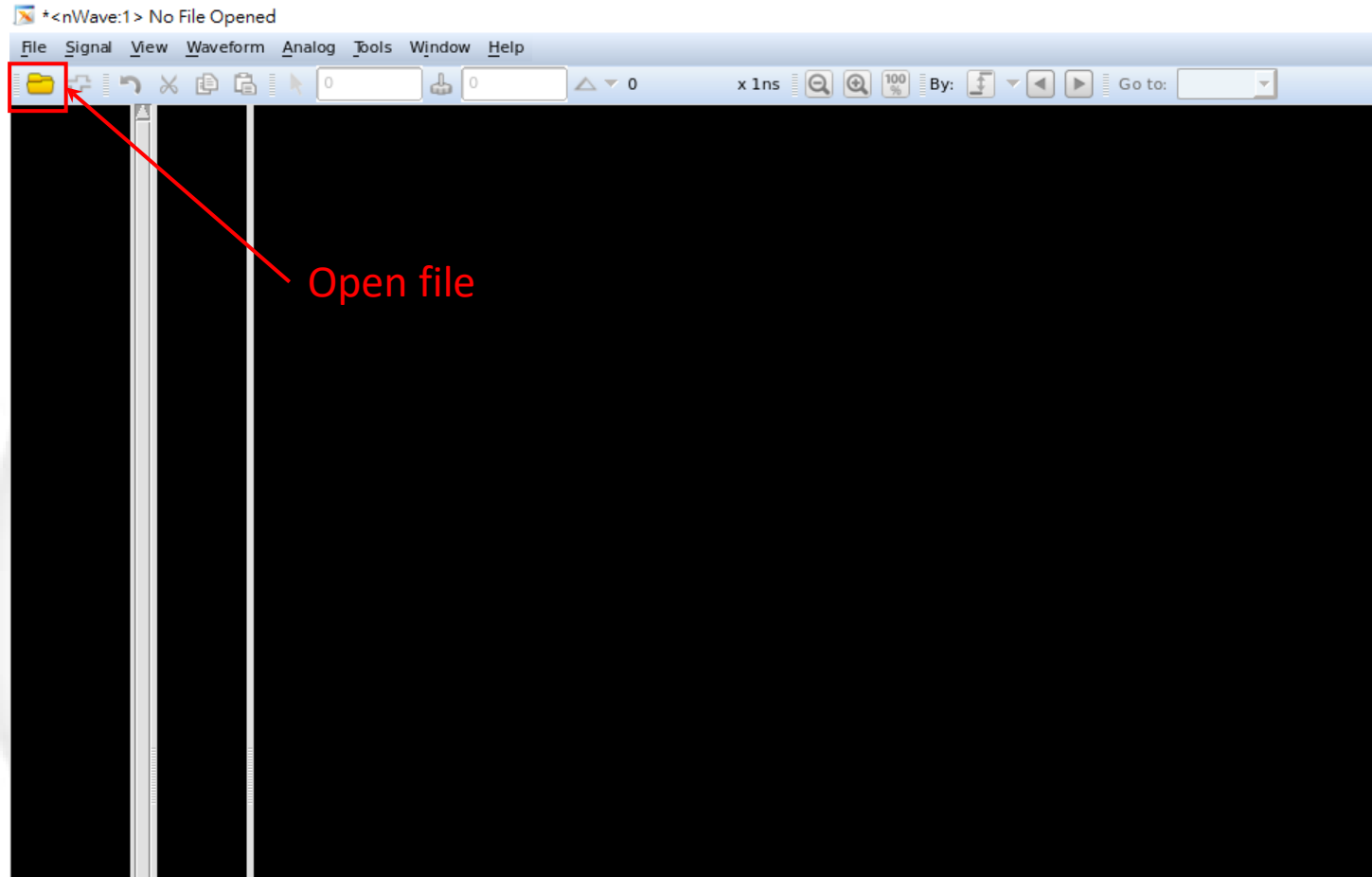
```

# Outline

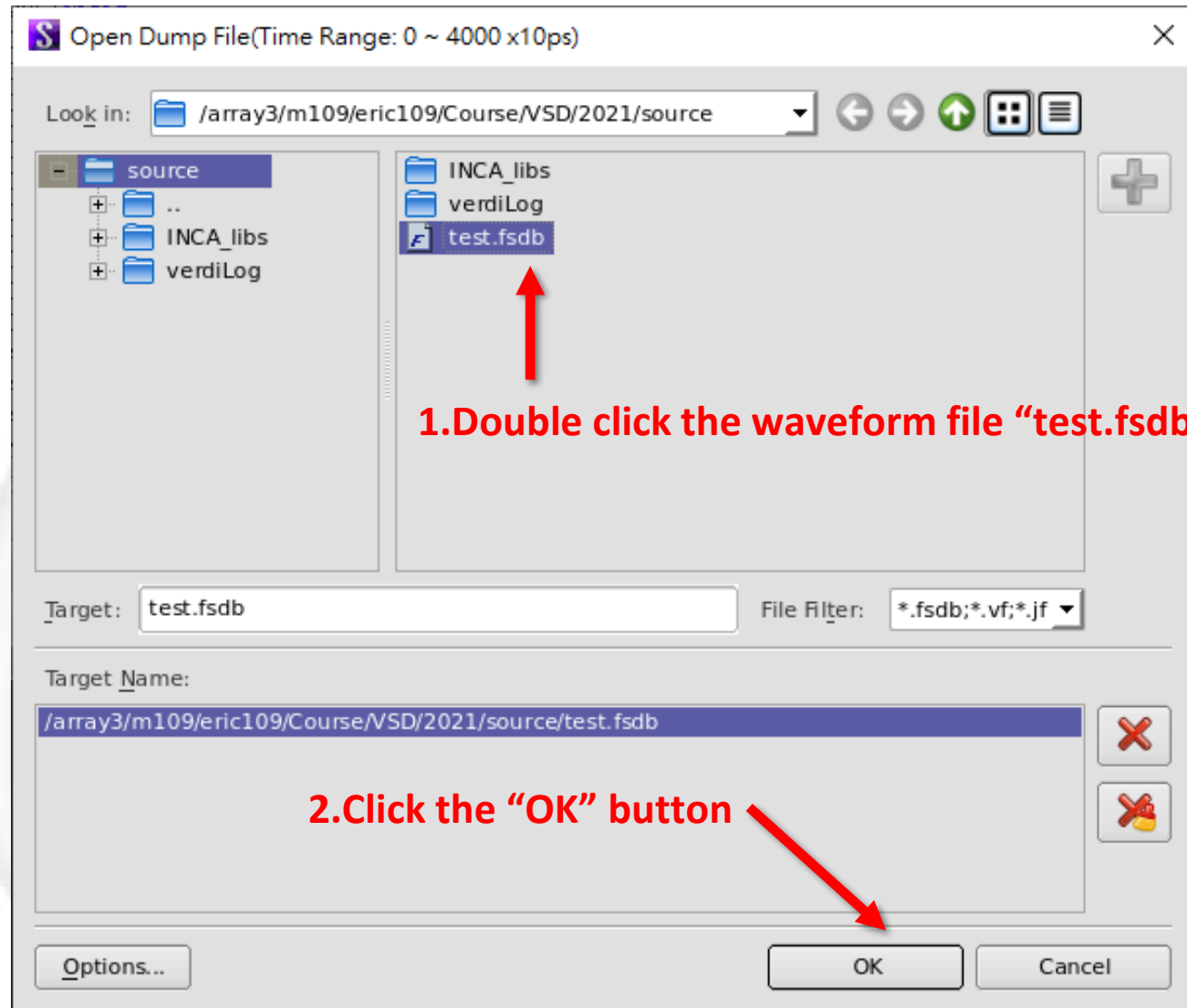
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# Viewing Waveform using nWave (1/4)

Input **nWave &** in terminal to open nWave window



## Viewing Waveform using nWave (2/4)





# Viewing Waveform using nWave (3/4)

\*<nWave:1> /array3/m109/eric109/Course/VSD/2021/source/test.fsdb

File Signal View Waveform Analog Tools Window Help

0 x 10ps 100% By: Go to: G1

**1** Click the "Get Signals"

Scope: /test\_tb Signal: \*

test\_tb(test\_tb)  
t0(test1)

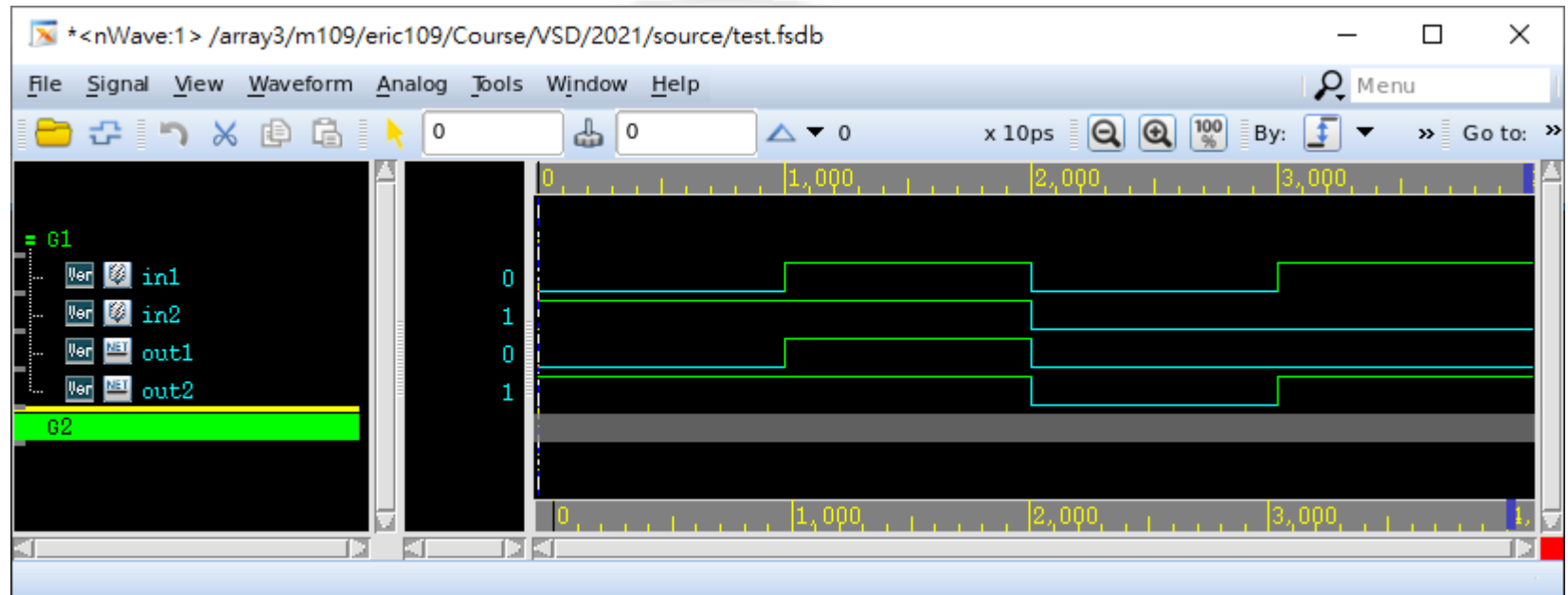
in1	out1	out[31:0]	LOGIC_HIGH
in2	out2	LOGIC_LOW	BLANK

**2** Select the signals to be monitored

**3** Click the "OK" button

Options... ALL Apply OK Cancel

# Viewing Waveform using Verdi (6/6)



in1	0	1	0	1
in2	1	1	0	0
out1 = in1 & in2	0	1	0	0
out2 = in1   in2	1	1	0	1

# Thank you for your attention!!