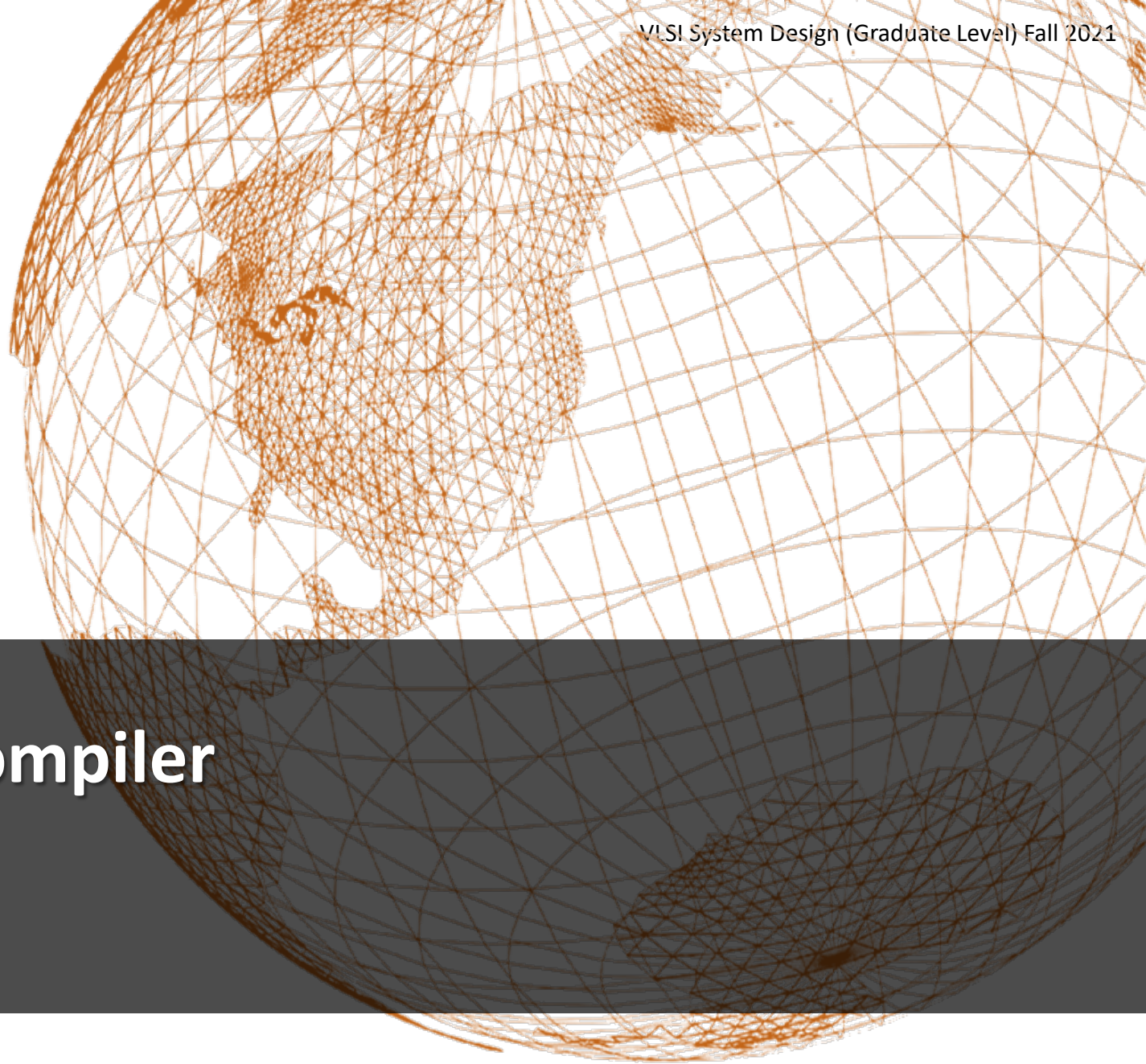


Memory Compiler

Outline

- Generate memory
- Adapt memory to cell library
- .lib to .db
- .lef to .gds
- File list

Generate memory

- There are many kinds of format Memory Compiler can generate.
- In this course, we need
  - Datasheet(.ds)
  - Verilog model(.v)
  - Synopsys liberty model(.lib)
  - Cadence LEF model(.lef)
  - GDSII layout model(.gds)
    - Use another tool

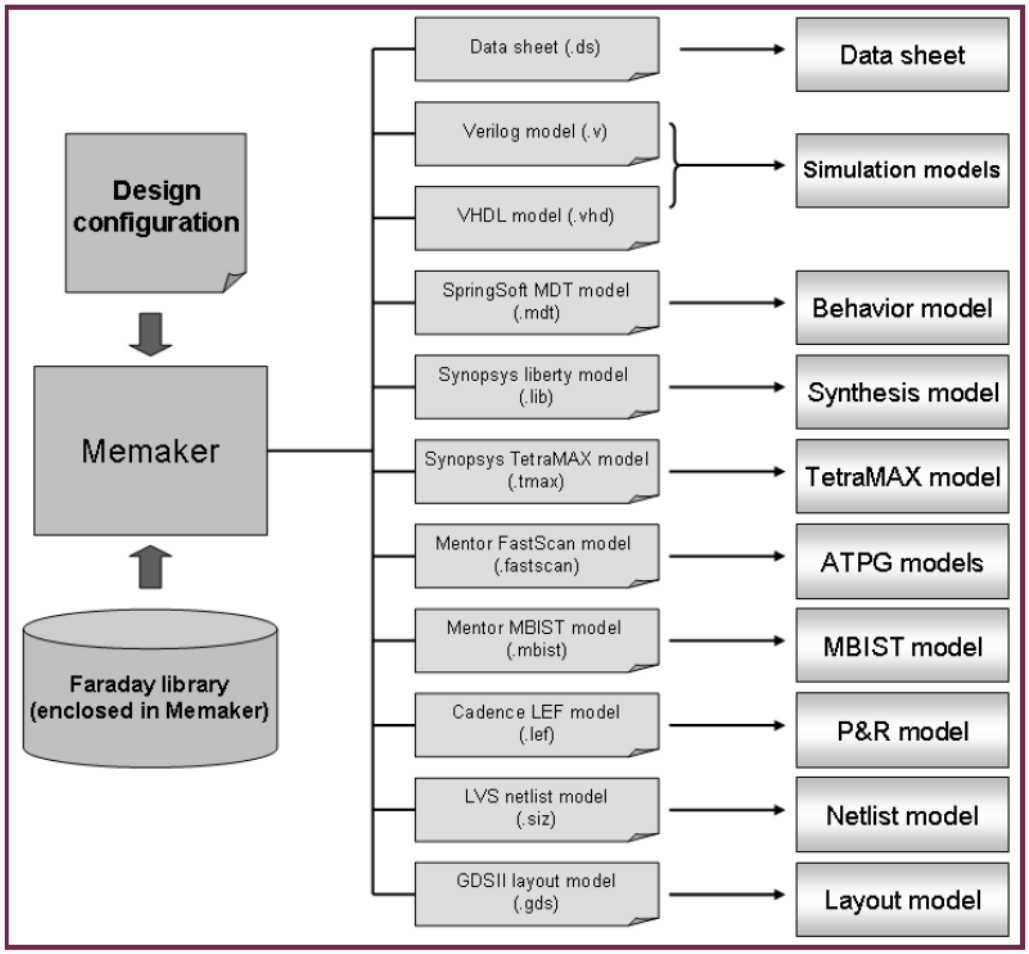
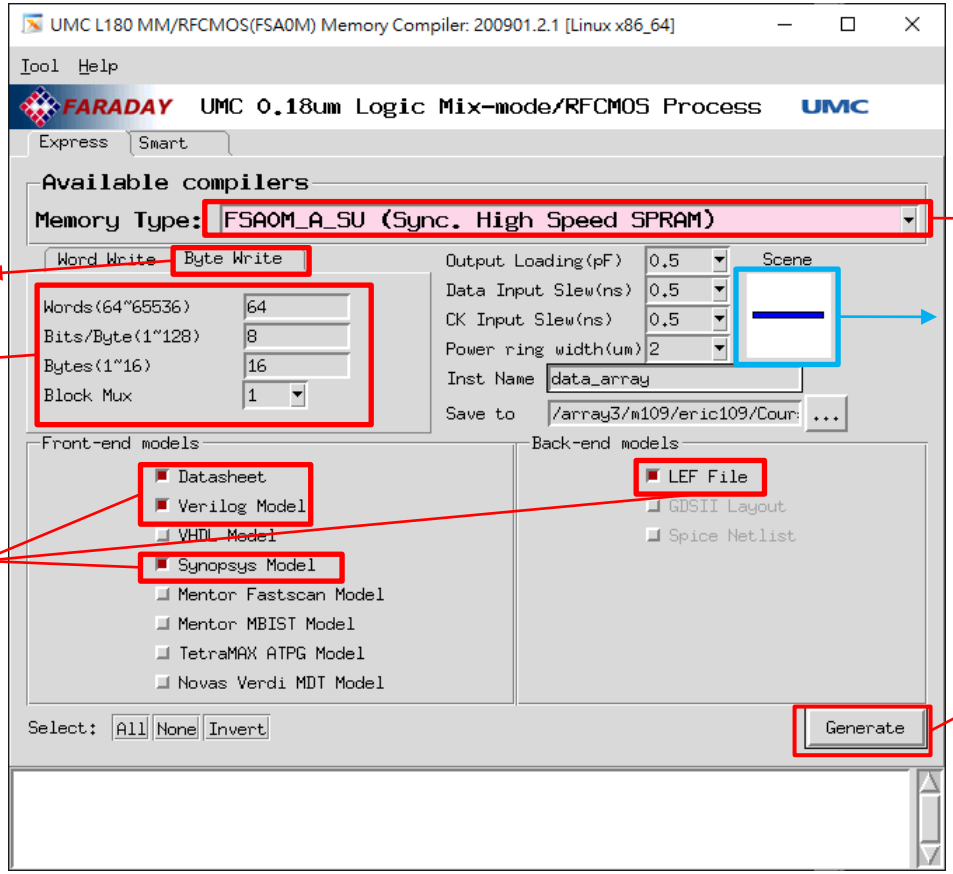


Figure 2-1. Memaker Input/Output Relationship

Generate memory

- Take data array as an example
- ***$memaker***



1 Choose single port SRAM

Be aware of the shape of SRAM
It affects the floorplan in APR

2 Choose Byte alignment

3 Design the size

4 Select the file type to generate

5 Generate!!!

Adapt memory to cell library

- $ chmod +x U18MemakerLEF.sh
- $ ./U18MemakerLEF.sh data_array.lef
  - ➔ Replace the naming rule of LEF file to synchronize with U18 Library

```
48    SHAPE ABUTMENT ;
49   PORT
50    LAYER ME4 ;
51    RECT 1886.780 129.700 1887.900 132.940
     ;
52    LAYER ME3 ;
53    RECT 1886.780 129.700 1887.900 132.940
     ;
54    LAYER ME2 ;
55    RECT 1886.780 129.700 1887.900 132.940
     ;
56    LAYER ME1 ;
57    RECT 1886.780 129.700 1887.900 132.940
     ;
58   END
59   PORT
60    LAYER ME4 ;
61    RECT 1886.780 121.860 1887.900 125.100
     ;
62    LAYER ME3 ;
```

```
53 LAYER metal1
54 +-- 12 lines: TYPE ROUTING ;----------
66 END metal1
67
68 LAYER via
69 +--  2 lines: TYPE CUT ;--------------
71 END via
72
73 LAYER metal2
74 +-- 13 lines: TYPE ROUTING ;----------
87 END metal2
88
89 LAYER via2
90 +--  2 lines: TYPE CUT ;--------------
92 END via2
93
94 LAYER metal3
95    ¦ TYPE ROUTING ;
96    ¦ WIDTH 0.280 ;
97    ¦ SPACING 0.280 ;
```

/data_array.lef <CIC/SOCE/lef/header6_V55_20ka_cic.lef [RO]

.lib to .db

- $ lc_shell
- lc_shell> read_lib data_array_BC.lib
- lc_shell> write_lib data_array _BC -format db -output data_array_BC.db
- Repeat for BC/TC/WC corner
- lc_shell is a tool provided by Synopsys
  - ➔ It transforms the timing file from .lib(ASCII format) into .db (Binary format).
  - ➔ The .db is more rapidly ready by the Synopsys tool than the .lib file

```
lc_shell> read_lib data_array_BC.lib
Reading '                                    /data_array_BC.lib' ...
Warning: Line 45, The default_operating_conditions is not defined. operating_conditions 'BCCOM' is set
        as the default_operating_conditions. (LBDB-663)
Warning: Line 45, The 'internal_power_calculation' attribute in char_config group is required for NLPM library.
        No default can be applied to this attribute. (LBDB-366)
Technology library 'data_array_BC' read successfully
1
lc_shell> write_lib data_array_BC -format db -output data_array_BC.db
Wrote the 'data_array_BC' library to '                                    /data_array_BC.db' successfully
1
```

.lef to .gds

- Since the Memory Compiler didn't provide the GDSII layout file, we need to translate the LEF file into GDSII layout file.
- Remember to adapt the LEF file first (Page5)
- $perl lef2gds_v1.pl data_array.lef

```
[eric109@LPHP3 Mem]$ perl lef2gds_v1.pl data_array.lef
== Read techfile lef2gds_U18.tech ==
== Read lef data_array.lef ==
Cell: data_array
[eric109@LPHP3 Mem]$
```

File list

- .ds – Datasheet
- .lef – Physical Layout File
- .v – Verilog File
  - ➔ Gate level file
  - ➔ The behavior model can be modified from SRAM module provided in previous homework according to the specification you design.
- .lib – Library timing File (ASCII format)
  - ➔ Including BC/TC/WC
- .db – Library timing File (Binary format)
  - ➔ Including BC/TC/WC
- .gds – GDSII Layout File