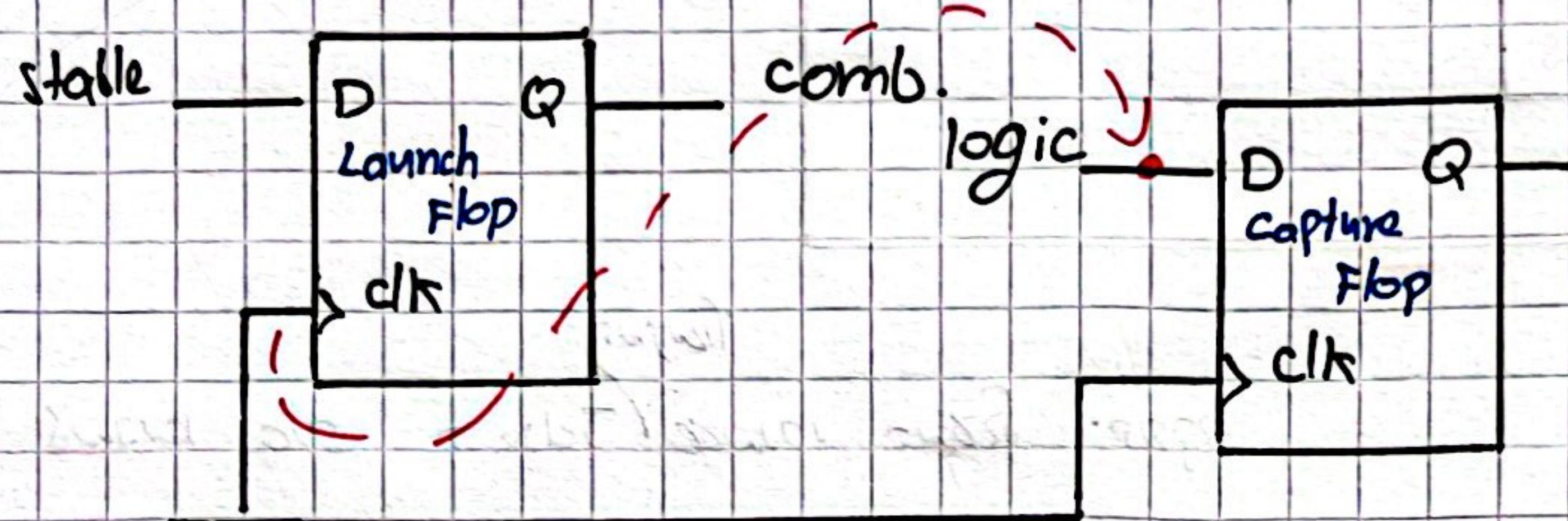


Setup Analysis

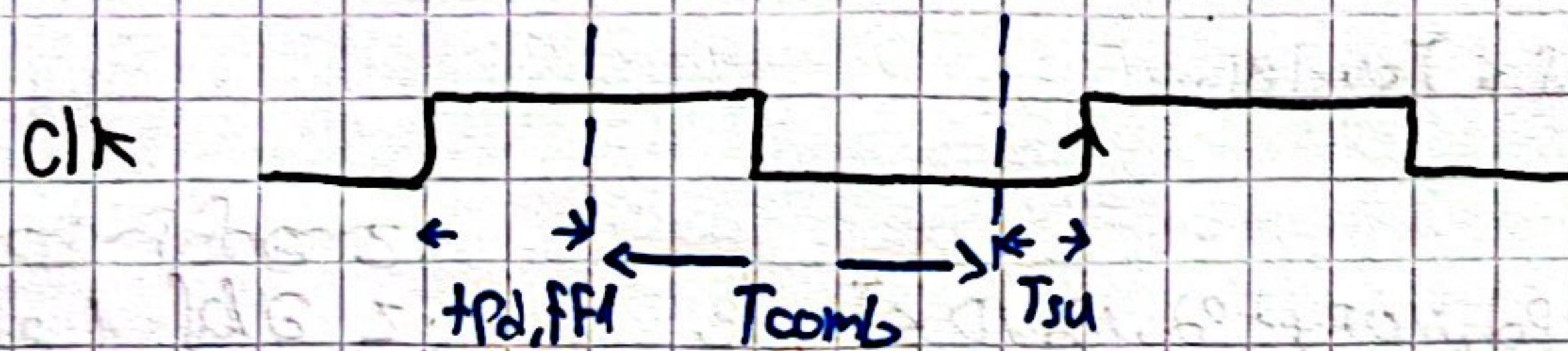
we want that our devices will be working as fast as possible, therefore we want a higher frequency of the clock system.

But, we can't just increase the clock frequency because it effects on the Tcycle which constraints setup condition.



• $\delta_{ff1} \leq t_{su}$ signal capture flop? $\delta_e \leq \delta_{ff2}$ 8-8 data? δ_e •

. δ_e $\leq \tau_{ICD}$



$$\rightarrow t_{pd, FF1} + t_{pd, CL} + t_{setup, FF2} \leq T_{clk}$$

For clock skew questions:

* Assume skew Δ_1 for Launch flop.

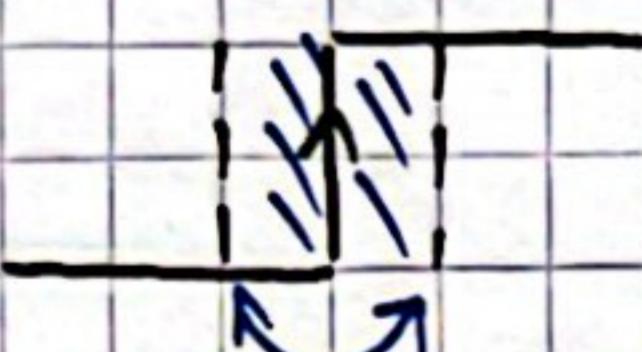
* Assume skew Δ_2 for Capture flop.

$$\Delta = \Delta_2 - \Delta_1$$

$$\rightarrow t_{pd, FF1} + t_{pd, CL} + t_{setup, FF2} < T_{clk} + \Delta$$

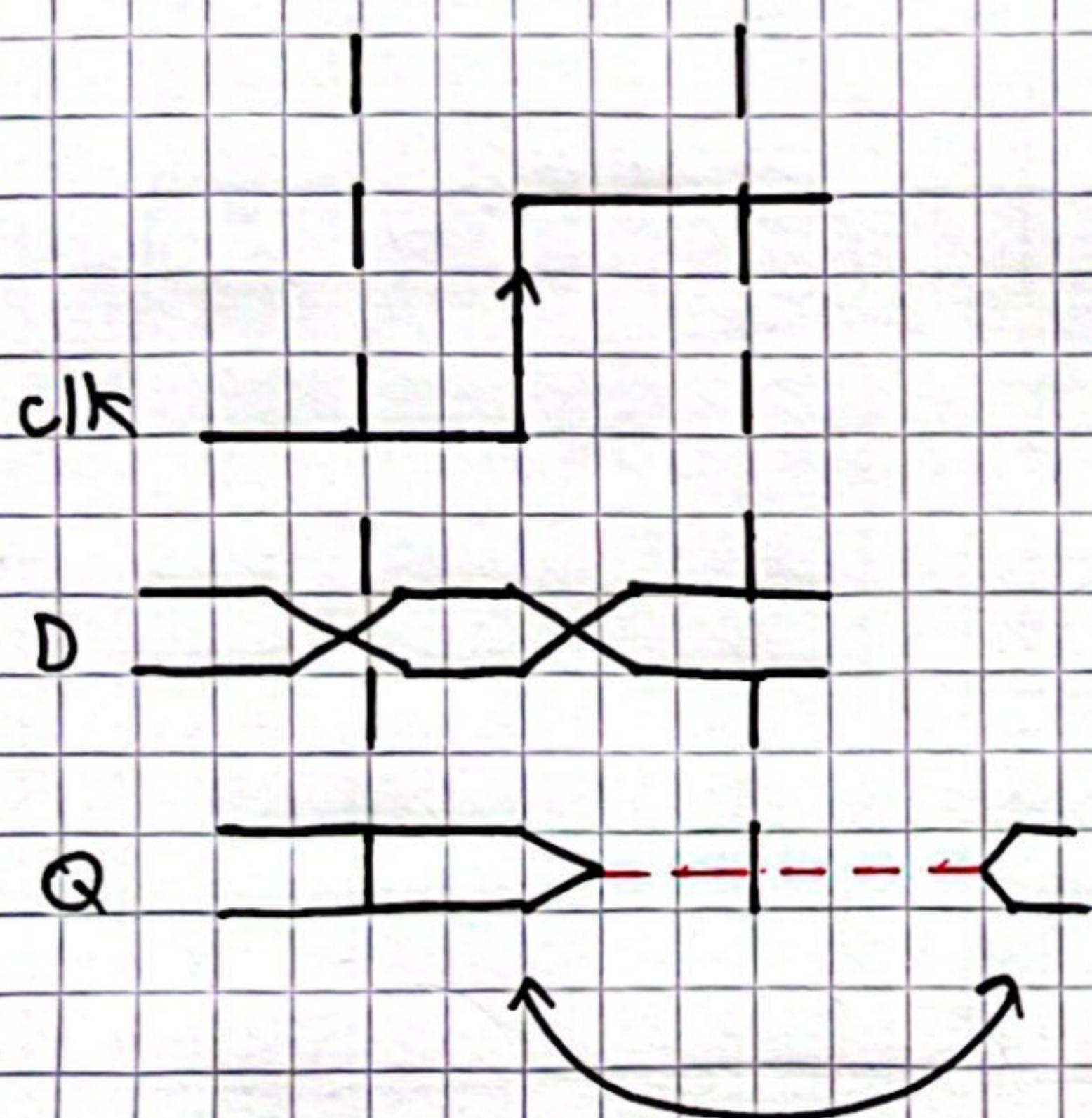
Metastability:

- Why was it so important to keep up with setup & hold constraints?



Do not disturb zone
of the flip-flop.

- If the data input changes during the "do not disturb" window then the output Q will be '1'/'0' randomly.

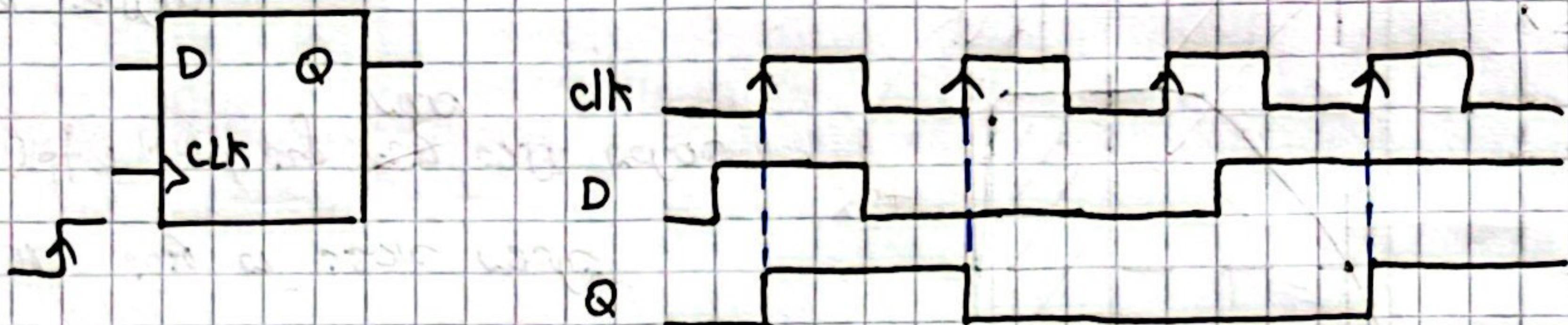


t_{res} , the time from the clock pulse
to a stable output.

Introduction to setup 4 hold times :

לעומת ה-DFlop השם נקבע כ-1.18e-10 או 1.18 × 10⁻¹⁰.

כִּי מֵתְּנָא כִּי תַּחֲזִקְנָא כִּי תַּמְלִיכְנָא כִּי תַּעֲמִידְנָא כִּי תַּעֲמִידְנָא כִּי תַּמְלִיכְנָא כִּי תַּחֲזִקְנָא כִּי מֵתְּנָא

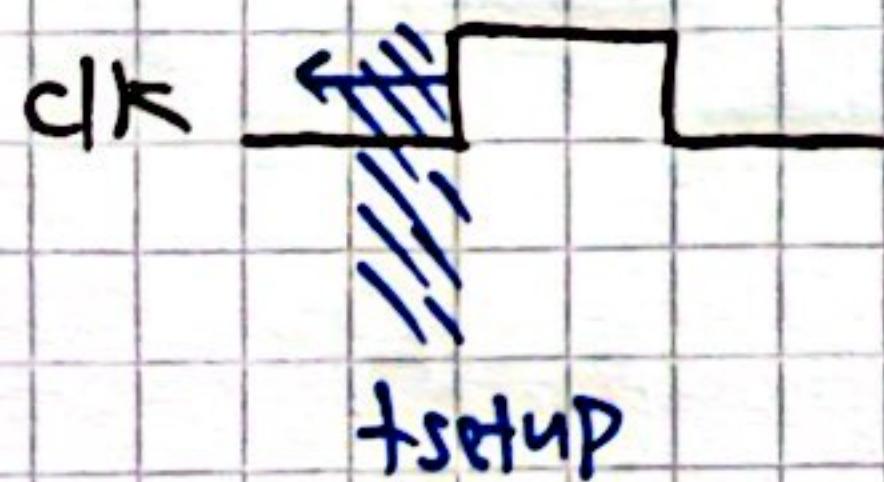


כש-כך נשים בראות שפניהם מחרצת עזירה.

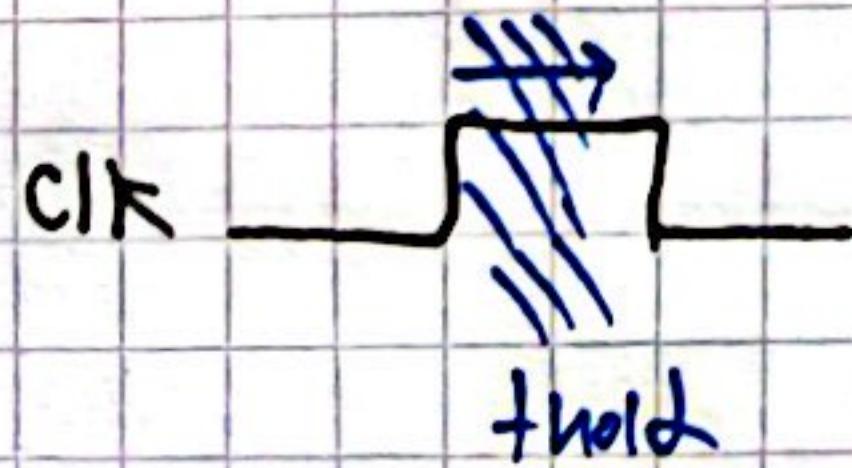
722

- **Setup time:** The minimum amount of time before the clock's active edge that the data must be stable for it to be latched correctly. //

כדר-טָהָרָה מִמְּלֵאָה גַּם כִּי בְּבָרֶךְ

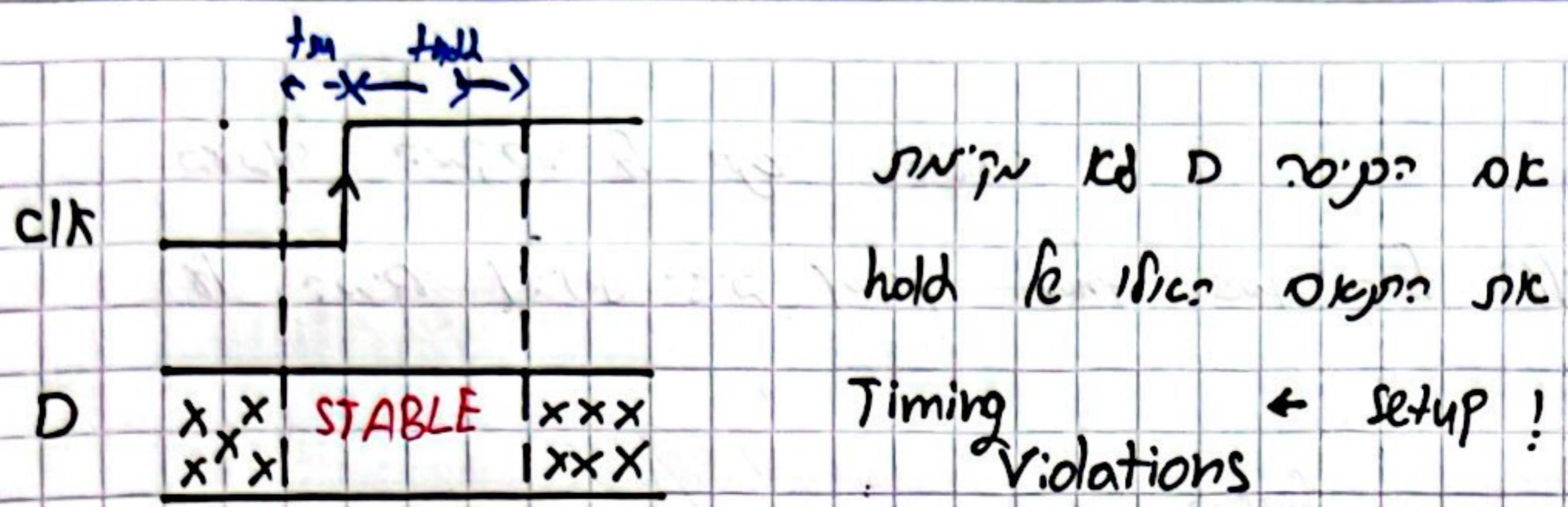


- * hold time: The minimum amount of time after the clock's active edge that the data must be stable. // 'skjønt' nvs=



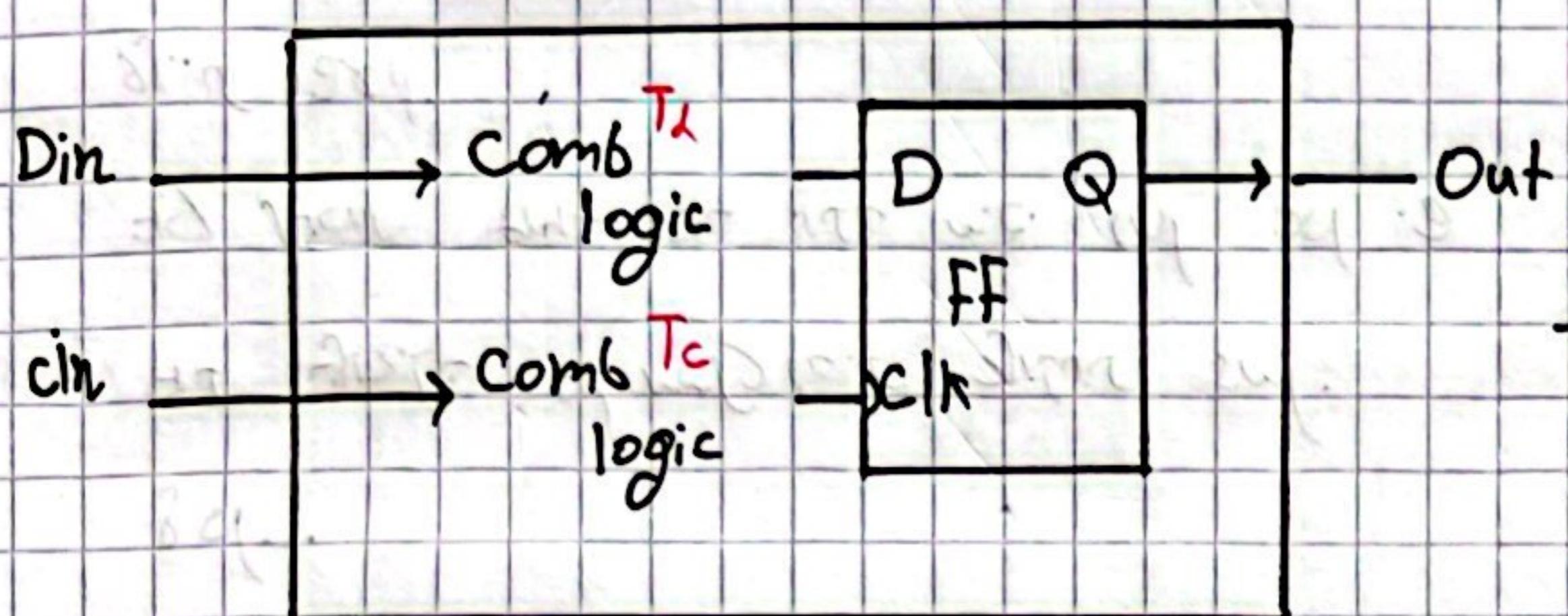
వీ వాళ్ల పునర్జీ

• ۱۸۰ مارچ ۱۹۷۵



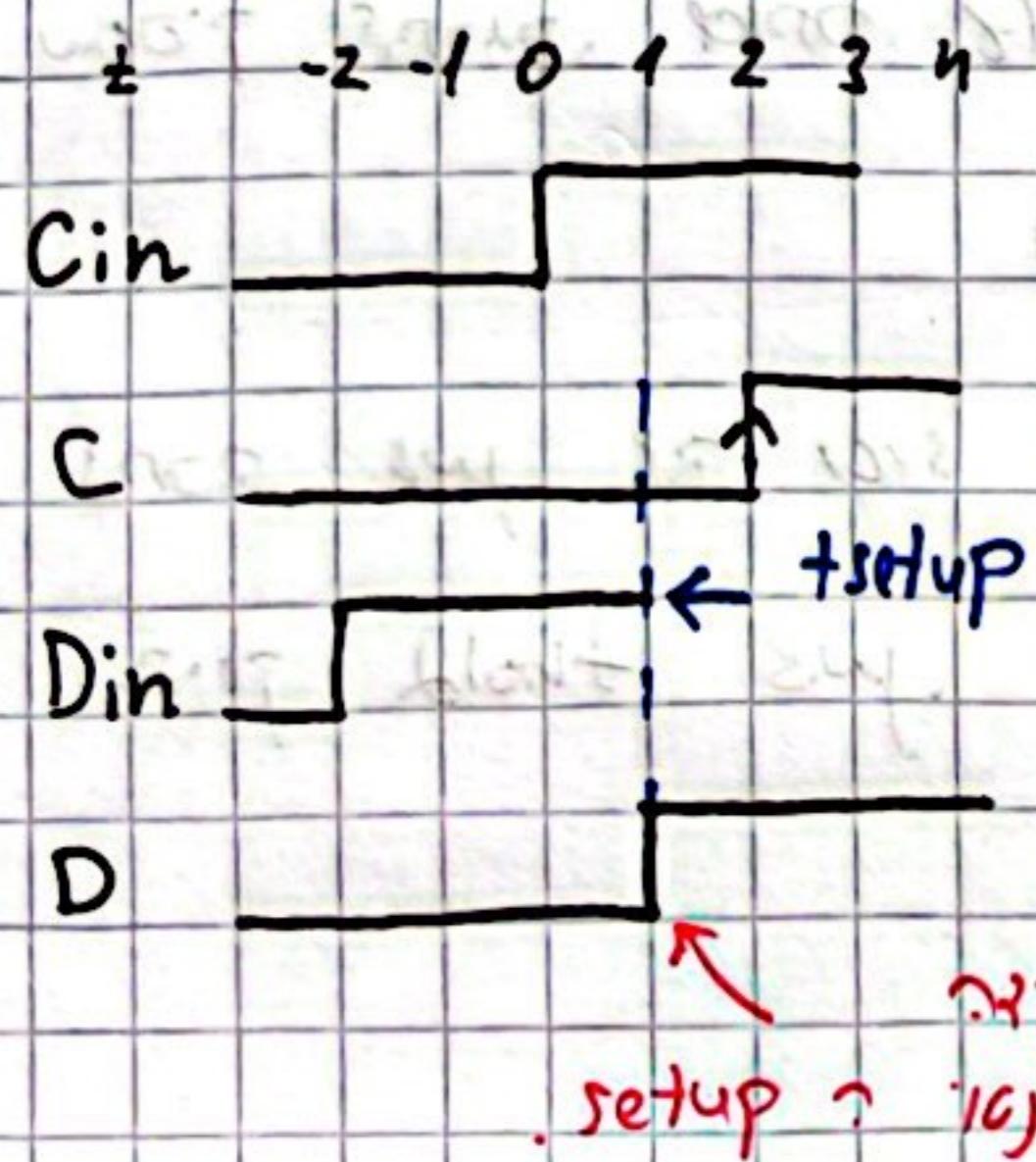
הו קבץ כפיה מושג בsetup, hold וclock וdata נסוברים.

כפיה כפיה.

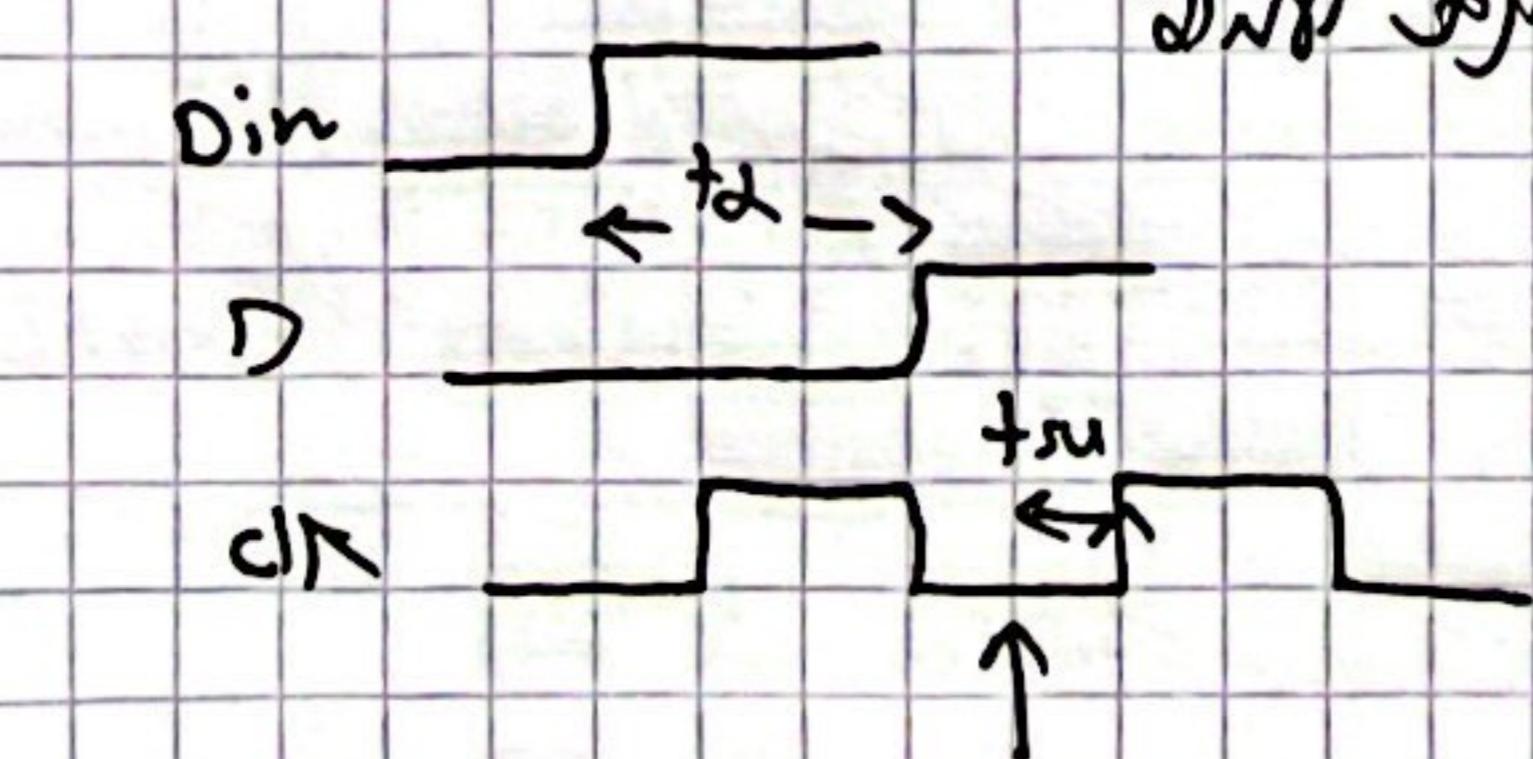


$$t_{hold} = T_c$$

$$T_d = 3, T_c = 2, t_{su} : t_{hold} = 1$$

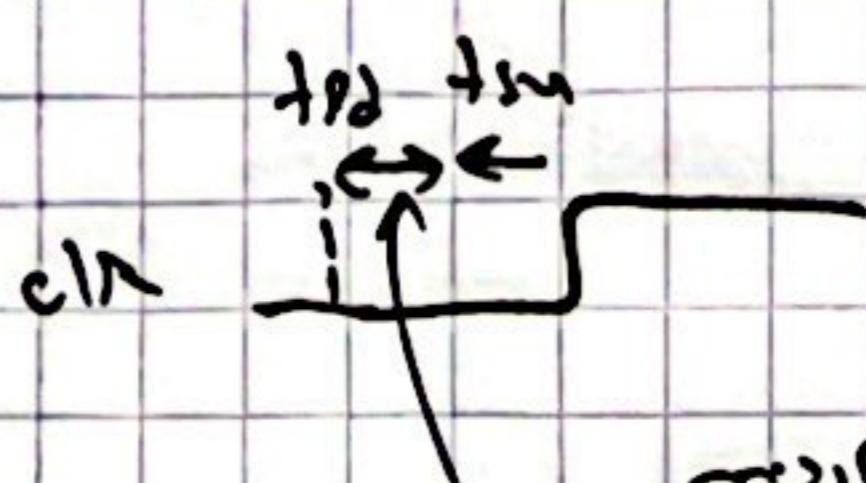


: skew t_{skew}



הו קבץ כפיה מושג בskew.

$$t_{skew} = t_{pd} + t_{setup}$$



הו קבץ כפיה מושג בhold.

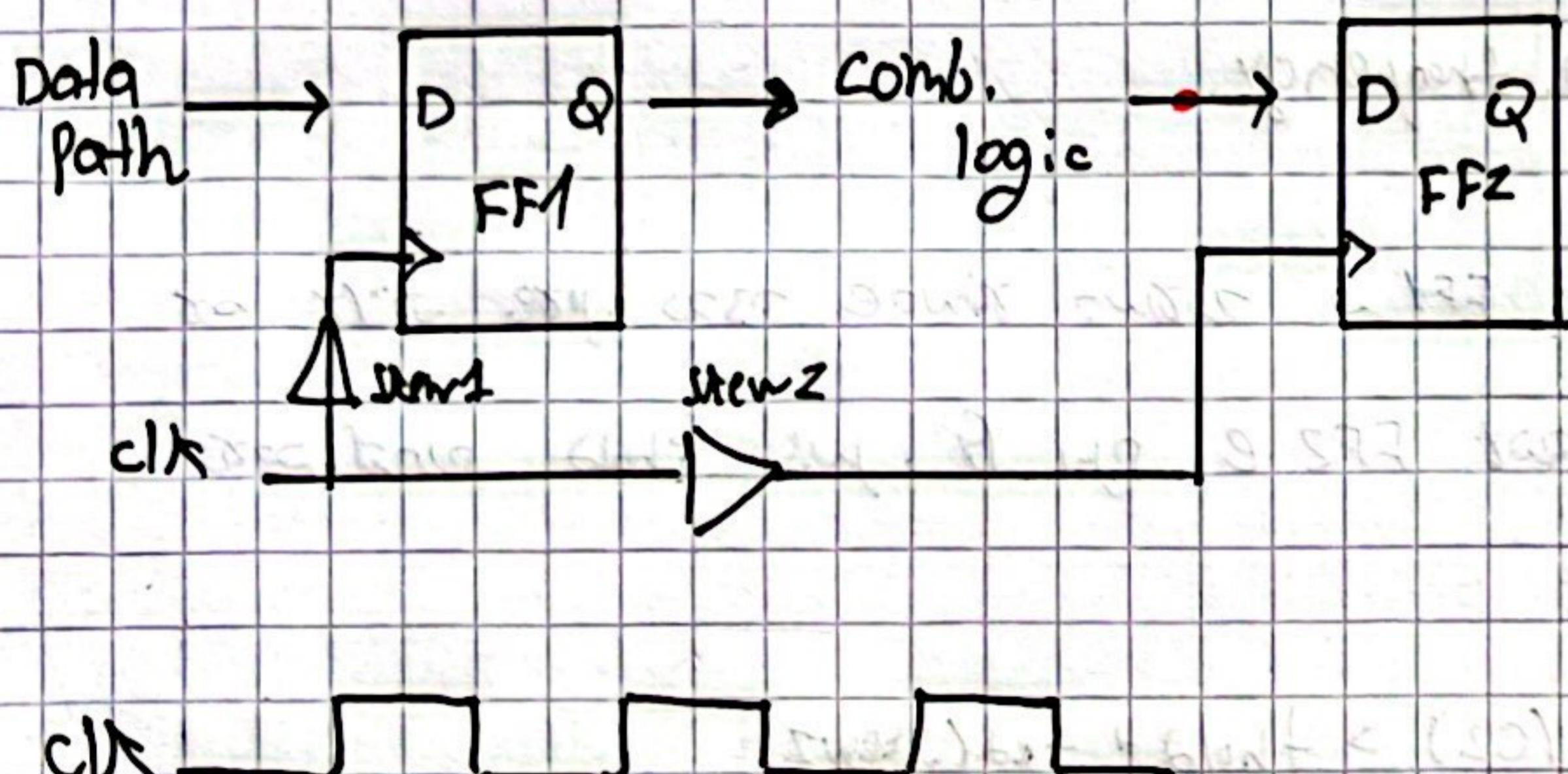
why setup & hold time exists?

1. Setup violation may cause incorrect data to be captured.

2. Hold violation may cause incorrect data to be latched.

(כדי) שורש פורסם בפנוי מושג רוחני יפה יפה?

Setup Analysis



* Static timing Analysis is performed to ensure that the correct data is present at the data input of each synchronous device.

→ why would things go wrong?

השאלה היא: מהו מושג רוחני ביחס לזמן אמת?

Equation for setup analysis:

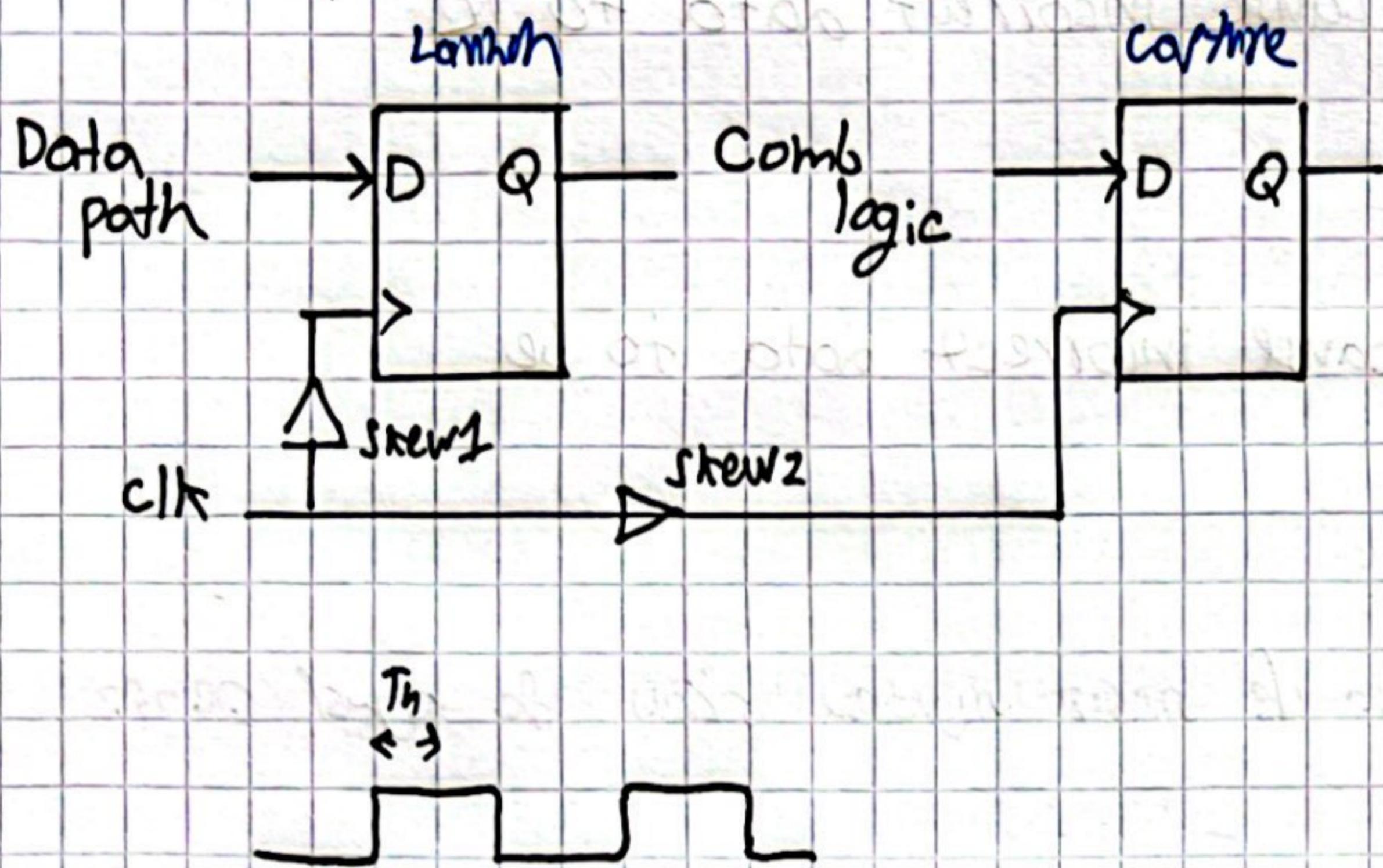
$$\Delta \text{skew}_1 + t_{pd}(\text{FF1}) + t_{pd}(\text{CL}) < T_{clk} - t_{\text{setup}}(\text{FF2}) + \Delta \text{skew}_2$$

Data Arrival time to D₂ Data Required time

setup? יוגע מושג רוחני? If then skew?

: מילויים

Hold Analysis :



The data that is launched at the current clock edge should not travel to the capture flop before the hold time has passed after the clock edge.

while dealing with hold analysis, there is no concern about the clock frequency.

Equation for hold analysis :

$$t_{cd}(\text{skew1}) + t_{cd}(\text{FF1}) + t_{cd}(\text{CL}) > \text{hold} + t_{cd}(\text{skew2})$$

Data Arrival Time

Data Required Time

→

$$t_{cd}(\text{skew1}) + t_{cd}(\text{FF1}) + t_{cd}(\text{CL}) + t_{cd}(\text{skew2}) > \text{hold}$$

Notes:

• Hold time is required to prevent race condition.

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