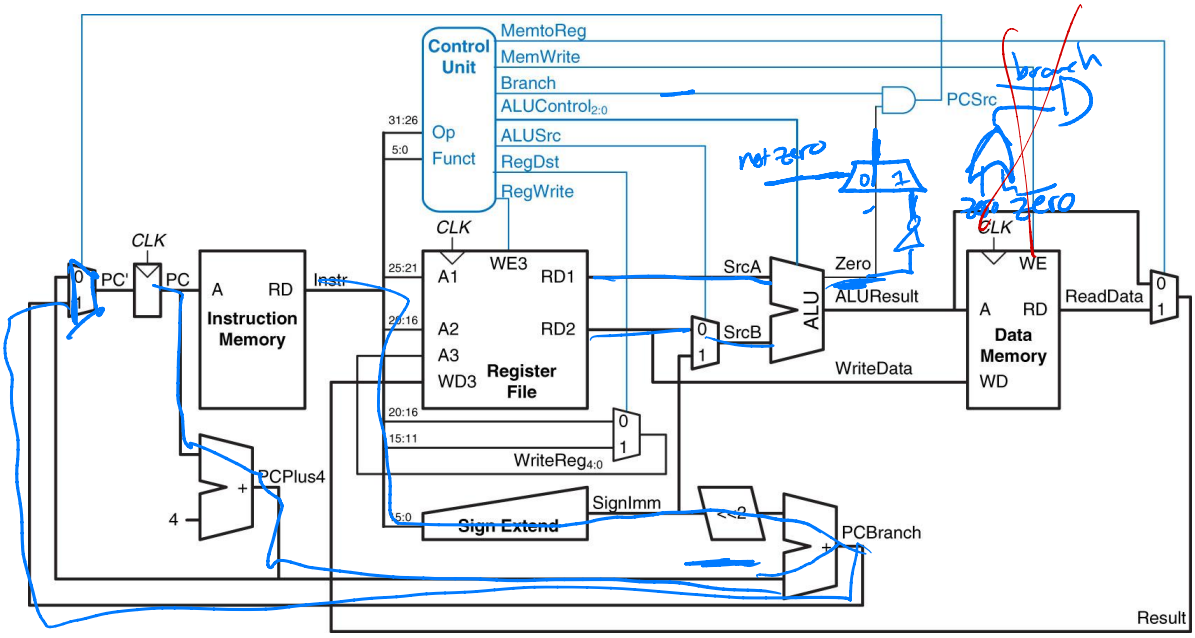
Given the single-cycle processor design below, implement the bne (branch if not equal) instruction, with an opcode of 000101. The instruction format is the same as the beq instruction, but the branch is taken if the operands are not equal. Update the controller truth table appropriately and show any changes to the datapath if necessary. Explain your design.



Instruction	$Op_{5:0}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	$ALUOp_{1:0}$	not zero
R-type	000000	1	1	0	0	0	0	10	X
lw	100011	1	0	1	0	0	0	00	X
sw	101011	0	X	1	0	1	X	00	X
beq	000100	0	X	0	1	0	X	01	0
bne	000101	0	X	0	1	0	X	01	1