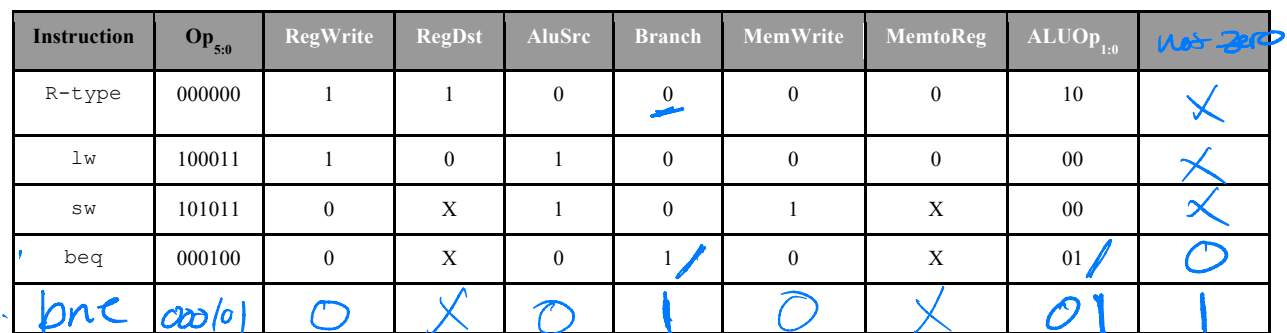


The diagram illustrates a processor architecture with the following components and connections:

- Control Unit:** Receives `MemToReg`, `MemWrite`, `Branch`, `ALUControl2:0`, `ALUSrc`, `RegDst`, and `RegWrite`. It outputs `Op` (31:26) and `Funct` (5:0).
- Instruction Memory:** Receives `PC` and `CLK`. It outputs `Instr` (25:21) to the Register File and `PCPlus4` (4) to the PC adder.
- Register File:** Receives `CLK` and `Instr`. It outputs `RD1` (25:21) to `SrcA`, `RD2` (25:16) to `SrcB`, and `WD3` (20:16) to the ALU. It also outputs `WriteReg4:0` (15:11) to the ALU and `SignImm` (5:0) to the PC branch adder.
- ALU:** Receives `SrcA`, `SrcB`, and `ALUControl2:0`. It outputs `ALUResult` to the Data Memory and `Zero` to the branch logic.
- Data Memory:** Receives `WriteData` and `WriteEn` (0/1). It outputs `ReadData` (0/1) to the PC branch adder.
- PC Logic:** The `PC` register receives `PC` and `CLK`. It outputs `PC` to the Instruction Memory and `PCSrc` to the branch logic. The `PCBranch` adder receives `PC`, `PCPlus4`, and `SignImm` (shifted left by 2). It outputs `PC` to the Instruction Memory.
- Handwritten Annotations:**
 - `not zero` and `branch` are written near the branch logic.
 - `26 zero` is written near the `Zero` signal.
 - `PCSrc` is written near the `PC` register output.
 - `PCPlus4` is written near the 4-bit adder.
 - `SignImm` is written near the 5-bit sign extension block.
 - `PCBranch` is written near the 32-bit adder.



branch

zero zero

subtract

branch zero

bne

zero

zero

subtract

branch
zero

bne
zero

zero