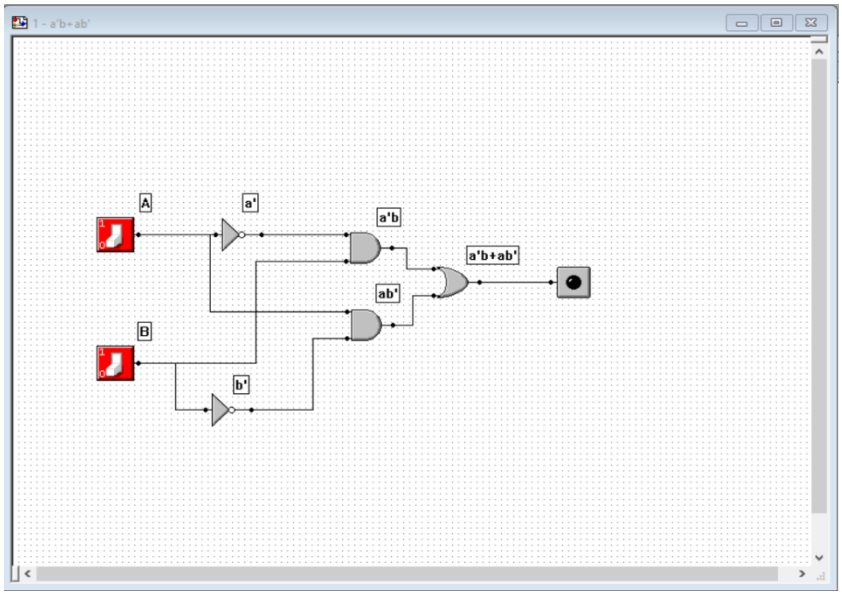
Hardware Organization Lab 3

Q1.

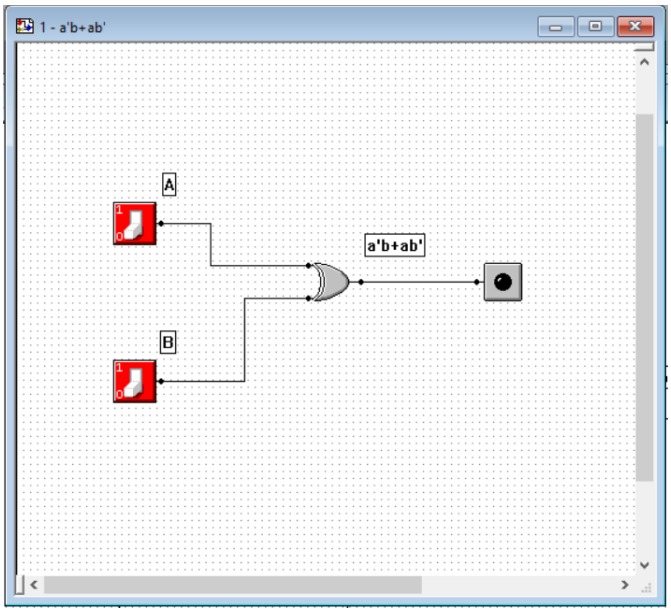


Equation: a'b+ab'

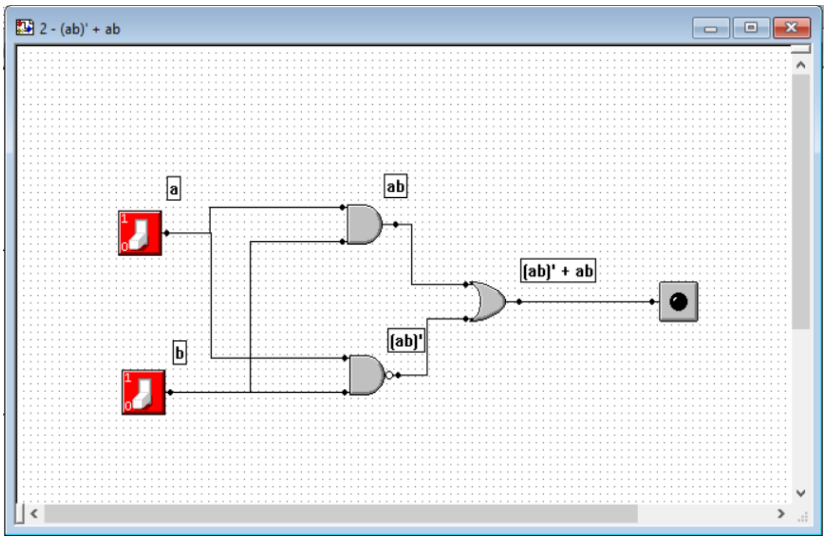
Truth Table:

A	B	A'B	AB'	A'B+AB'
1	1	0	0	0
1	0	0	1	1
0	1	1	0	1
0	0	0	0	0

This can be replaced using a XOR gate



Q2.

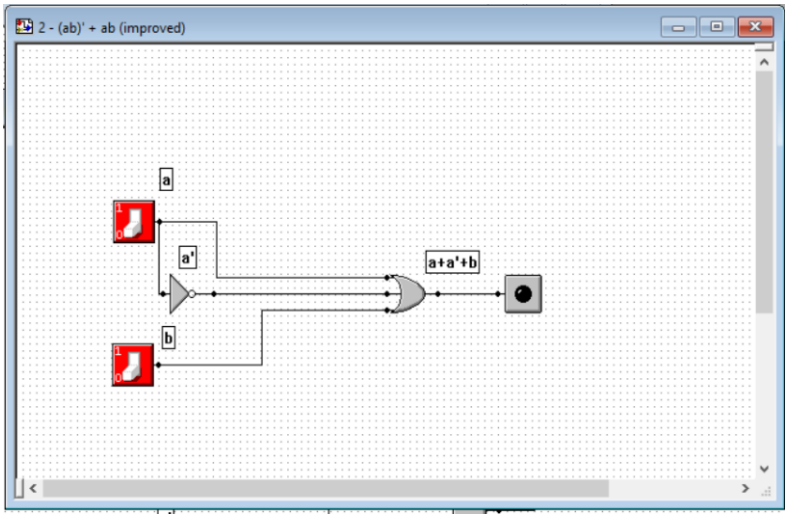


Equation: (ab)’ + ab

Truth table:

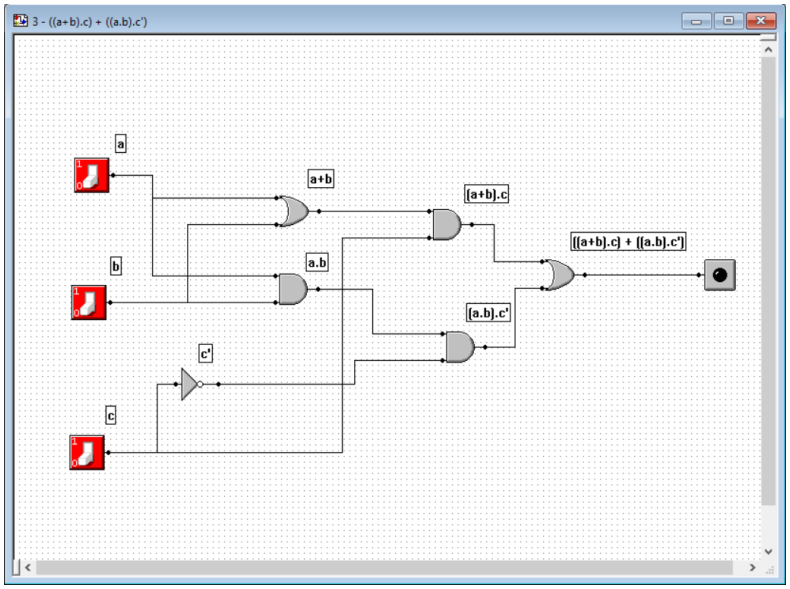
A	B	AB	(AB)’	(Ab)’+(ab)
1	1	1	0	1
1	0	0	1	1
0	1	0	1	1
0	0	0	1	1

This can be replaced by a simpler circuit:



Equation: a+a’+b

Q3

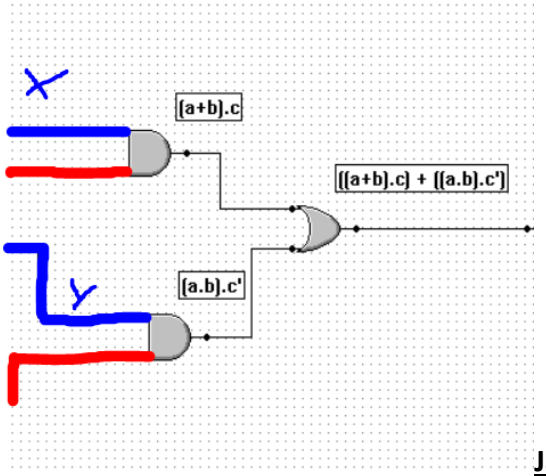


Equation: ((a+b).c) + ((a.b).c')

Truth Table:

A	B	C	A+B	A.B	(A+B).C	(A.B).C'	((A+B).C + ((A.B).C')
1	1	1	1	1	1	0	1
1	1	0	1	1	0	1	1
1	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	0	0	0
1	0	1	1	0	1	0	1
0	0	0	0	0	0	0	0

This part of the circuit is acting as a 2-1 mux:



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