Big Shot Operator's Manual

MPF Edition
Version 1
October 14, 2014

Table of Contents

Game Description

This documentation is for the Gottlieb Big Shot EM conversion done by Brian Madden and Gabe Knuth of Mission Pinball. The aim of this project was to convert a non-working EM to a modern pinball platform (in this case the P-ROC platform from pinballcontrollers.com). Our desired result is a game that plays and behaves identically to the original but is more resilient and not as susceptible to the failures that render so many older pinball machines useless.

It's also intended to demonstrate the flexibility of the Mission Pinball Framework, namely through the incorporation of the score and credit reels.

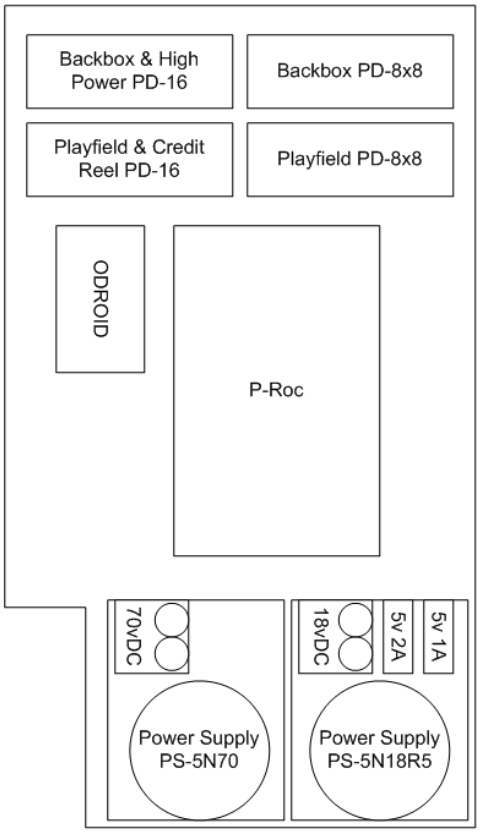
Virtually all internal components of the game have been removed (and preserved). What follows is a list of components that were kept:

- Chimes
- Knocker
- Plumb bob
- Coin Mech
- All playfield components, including coils and switches (except EOS switches)
- Score reels
- Credit unit

Any documentation that exists for Big Shot does not apply, spare part numbers for components that remain in the game. Throw out your schematics, everyone, we're using software now!

Hardware

This game is based upon the P-ROC platform, which combines a controller unit (the P-ROC) with several driver boards. The P-ROC is controlled via the Mission Pinball Framework, a Python-based framework that is run via a host computer. This computer can be anything from a full-fledged desktop or laptop to a single-board computer such as a Raspberry Pi, BeagleBone Black, or, as is the case with Big Shot, an ODROID. Everything is powered by a single 500W power supply with 5vdc and 18vdc taps.



The components are laid out on the main board in the cabinet approximately as shown. Since the ODROID boots quickly and auto-launches the game code, there's nothing else needed than to simply power the game on with a switch under the cabinet.

Later we'll detail this board and the connectors in detail.

P-ROC

In addition to being the interface to the game code, the P-ROC is also responsible for handing low level coils (slingshots and flippers, for instance) and two types of switches: Matrix or Direct. There is no applicable difference between the two, and we ended up extensively using both. Playfield switches are handled in an 8x8 switch matrix, while cabinet switches and backbox switches are direct. Direct switches are

slightly easier to wire since they share a common wire, but ultimately it's the same amount of work. We could have just as easily used an 8x16 switch matrix (which the P-ROC supports).

ODROID

The P-ROC plugs into the ODROID via a USB cable. The ODROID itself runs Xubuntu 13.10, though it can run many flavors of Linux and even Android. The device itself is essentially the same hardware as you would find in a Samasung Galaxy S3 smartphone. It runs for under $100, and is significantly more powerful than a Raspberry Pi. For Big Shot, though, a Raspberry Pi would likely also work since it doesn't have to drive a DMD.

Power Supply

Big Shot receives its power from two 500W Antek power supplies. The primary power supply is model PS-5N18R5R52A. This supply was chosen as a suitable replacement for Big Shot, which originally ran on 25vAC. It delivers us two outputs: a high-power 18vDC and a 5vDC output running at 2A. We're using 18vDC to power both the coils and the lamp matrix, and 5vDC to power the ODROID, P-ROC, driver boards, and the switch matrix.

The secondary power supply is a PS-5N70 that we're using solely for the drop target reset coils. Originally these four coils (two per bank) were driven by line voltage! We didn't want to have 110vAC under the playfield, and the force required resulted in too much current draw for the PD-16 driver boards, so we moved around some coils and dedicated one bank of a PD-16 to 70vDC.

Driver Boards

The driver boards are used to control objects in the game via the P-ROC. Big Shot uses four driver boards, two PD-16s and two PD-8x8s. One PD-16 is used to drive the coils on the playfield and in the cabinet, as well as the two coils used by the credit reel. Another PD-16 is used by the eight score reel coils and the drop target bank reset coils.

The PD-8x8s are used to control lamp matrices. Since each PD-8x8 can connect to 64 lamps (8x8=64) and there are 79 lamps in Big Shot, we are using two boards. One is used for the lamp matrix on the playfield and coin door, while the other is used for the lamp matrix in the backbox.

For the sake of coolness, we aren't using GI for this game. Rather, each bulb is independently addressable and is controlled by code. This approach will allow us to create enhanced light shows for future "modern" modes.

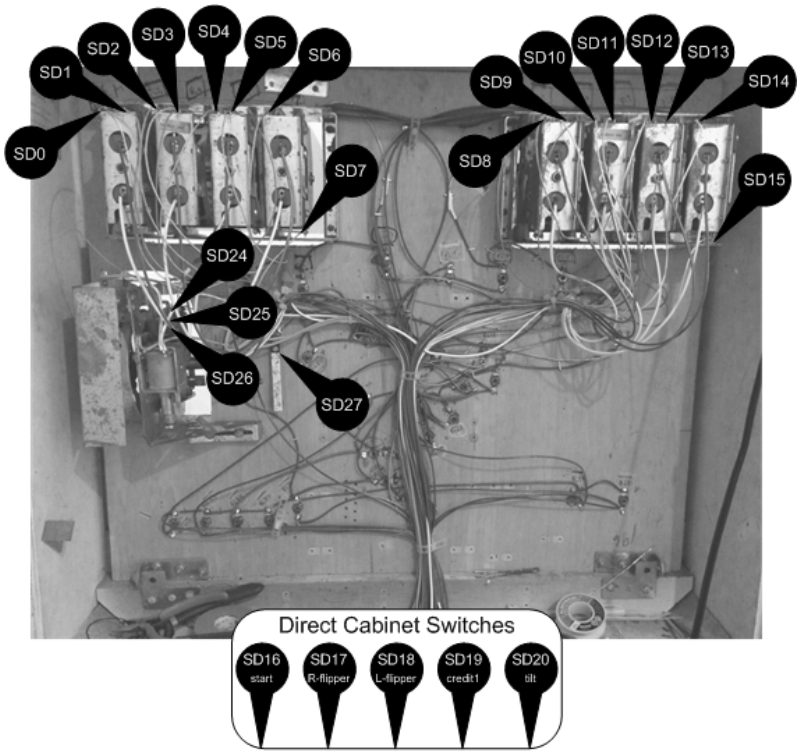
Switches

Playfield Switch Matrix

		0	1	2	3	4
		OR/GRAY	OR/YEL	OR/WHT	OR/GRN	OR/BLK
0 PUR/GRY	Tag	balllive	balllive	balllive	balllive	
	Name	topLaneMid	drop15	drop1	slingL	Not Used
	Label	Middle Rollover Top Lane	Right Bank 15	Left Bank 1	Left Slingshot	
1 PUR/YEL	Tag	balllive	balllive	balllive	balllive	
	Name	topLaneLeft	drop14	drop2	slingR	Not Used
	Label	Left Rollover Top Lane	Right Bank 14	Left Bank 2	Right Slingshot	
2 PUR/WHT	Tag	balllive	balllive	balllive	earlydrain	balllive
	Name	topLaneRight	drop13	drop3	leftOutlane	behindSolids
	Label	Right Rollover Top Lane	Right Bank 13	Left Bank 3	Left Outlane	Behind Left Drop Targetrs
3 PUR/GRN	Tag	balllive	balllive	balllive	balllive	balllive
	Name	popBumper	drop12	drop4	leftInlane	behindStripes
	Label	Pop Bumper	Right Bank 12	Left Bank 4	Left Inlane	Behind Right Drop Targets
4 PUR/BLU	Tag	balllive	balllive	balllive	earlydrain	
	Name	eightBallEject	drop11	drop5	rightOutlane	Not Used
	Label	8 Ball Center Hole Switch	Right Bank 11	Left Bank 5	Right Outlane	
5 PUR/GLD	Tag		balllive	balllive	balllive	
	Name	drain	drop10	drop6	rightInlane	Not Used
	Label	Trough Enter	Right Bank 10	Left Bank 6	Right Inlane	
6 PUR/OR	Tag		balllive	balllive	balllive	balllive
	Name	plungerLane*	midRtLane	midLtLane	ltMidStandup	midLtRubber
	Label	Plunger Lane Switch	Mid Left Lane Rollover	Mid Left Lane Rollover	Left Middle Target (above 8 ball)	Left Middle Lane (behind rubber)
7 PUR/PNK	Tag		balllive	balllive	balllive	balllive
	Name	drainEject	drop9	drop7	rtMidStandup	midRtRubber
	Label	Trough Eject Switch	Right Bank 9	Left Bank 7	Right Middle Target (above 8 ball)	Right Middle Lane (behind rubber)

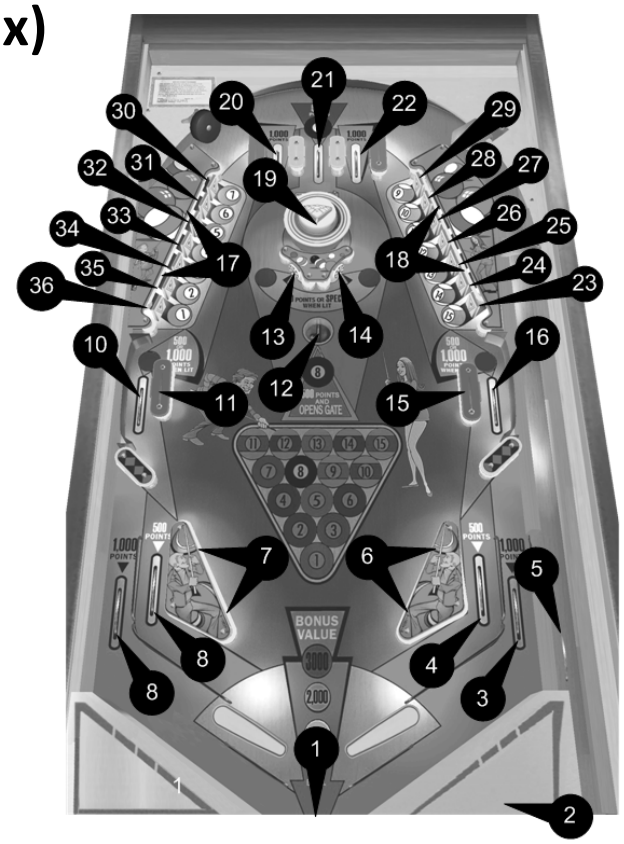
* Normally Closed

Backbox Switches (Direct)



Num	Name	Label	Wire Color
SD0	score_2p_10_0	2nd Player Tens Score - 0 Position	YEL/BLU
SD1	score_2p_10_5	2nd Player Tens Score - 5 Position	YEL/RED
SD2	score_2p_100_0	2nd Player Hundreds Score - 0 Position	YEL/GRN
SD3	score_2p_100_5	2nd Player Hundreds Score - 5 Position	YEL/PNK
SD4	score_2p_1k_0	2nd Player Thousands Score - 0 Position	YEL/GRAY
SD5	score_2p_1k_5	2nd Player Thousands Score - 5 Position	YEL/PUR
SD6	score_2p_10k_0	2nd Player Ten Thousands Score - 0 Position	YEL/BRN
SD7	score_2p_10k_5	2nd Player Ten Thousands Score - 5 Position	YEL/OR
SD8	score_1p_10_0	1st Player Tens Score - 0 Position	WH/BLU
SD9	score_1p_10_5	1st Player Tens Score - 5 Position	WH/RED
SD10	score_1p_100_0	1st Player Hundreds Score - 0 Position	WH/OR
SD11	score_1p_100_5	1st Player Hundreds Score - 5 Position	WH/YEL
SD12	score_1p_1k_0	1st Player Thousands Score - 0 Position	WH/PUR
SD13	score_1p_1k_5	1st Player Thousands Score - 5 Position	WH/BRN
SD14	score_1p_10k_0	1st Player Ten Thousands Score - 0 Position	WH/OR
SD15	score_1p_10k_5	1st Player Tens Thousands Score - 5 Position	WH/PNK
SD16	startButton	Start Button	BLU/LT BLU
SD17	flipperRight	Right Flipper Button	BLU/YEL
SD18	flipperLeft	Left Flipper Button	BLU/OR
SD19	classicMode	Used for Time Machine switch	BLU/GOLD
SD20	tilt	Plumb Bob Tilt	BLU/GRAY
SD21	(not used)		
SD22	(not used)		
SD23	(not used)		
SD24	creditWheel_0	Credit Wheel 0 Position	BLU/WH
SD25	creditWheel_max	Credit Wheel Max Position	BLU/GRN
SD26	creditWheel_1Plus	Credit Wheel - more than 1, less than max	BLU/RD
SD27	slamTilt	SlamTilt (Normally Closed)	BLU/PNK
SD28	(not used)		
SD29	(not used)		
SD30	(not used)		
SD31	(not used)		

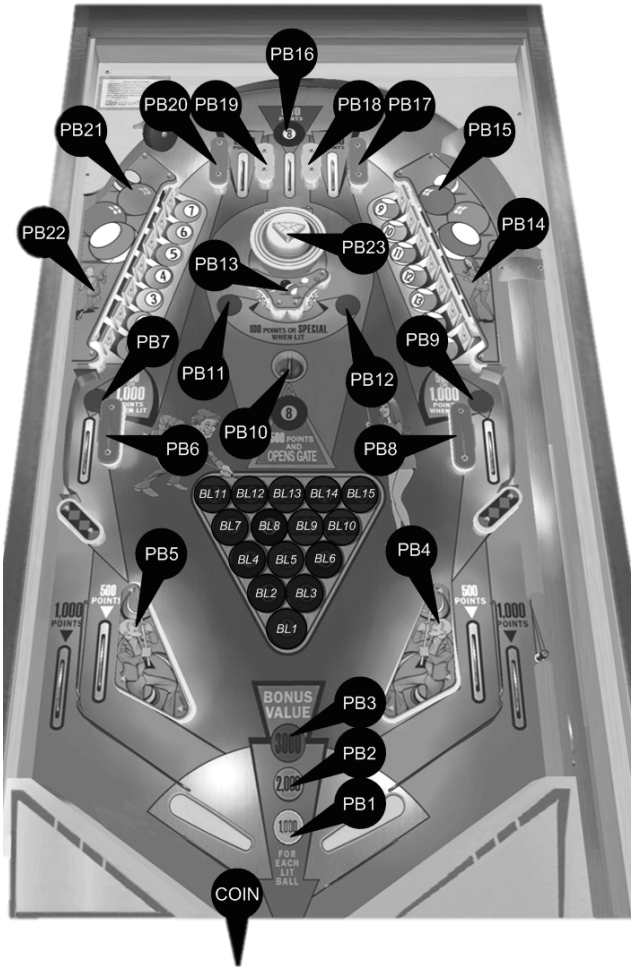
Playfield Switches (Matrix)



#	Name	Col/Row	#	Name	Col/Row
1	drain	0/5	19	popBumper	0/3
2	drainEject	0/6	20	topLaneLeft	0/1
3	rightOutlane	3/4	21	topLaneMid	0/0
4	rightInlane	3/5	22	topLaneRight	0/2
5	plungerLane	0/7	23	drop15	1/0
6	slingR	3/1	24	drop14	1/1
7	slingL	0/1	25	drop13	1/2
8	leftInlane	3/3	26	drop12	1/3
9	leftOutlane	3/2	27	drop11	1/4
10	midLtLane	2/7	28	drop10	1/5
11	midLtRubber	4/0	29	drop09	1/6
12	eightBallEject	0/4	30	drop7	2/0
13	ltMidStandup	3/7	31	drop6	2/1
14	rtMidStandup	3/6	32	drop5	2/2
15	midRtRubber	4/1	33	drop4	2/3
16	midRtLane	1/7	34	drop3	2/4
17	behindSolids	4/2	35	drop2	2/5
18	behindStripes	4/3	36	drop1	2/6

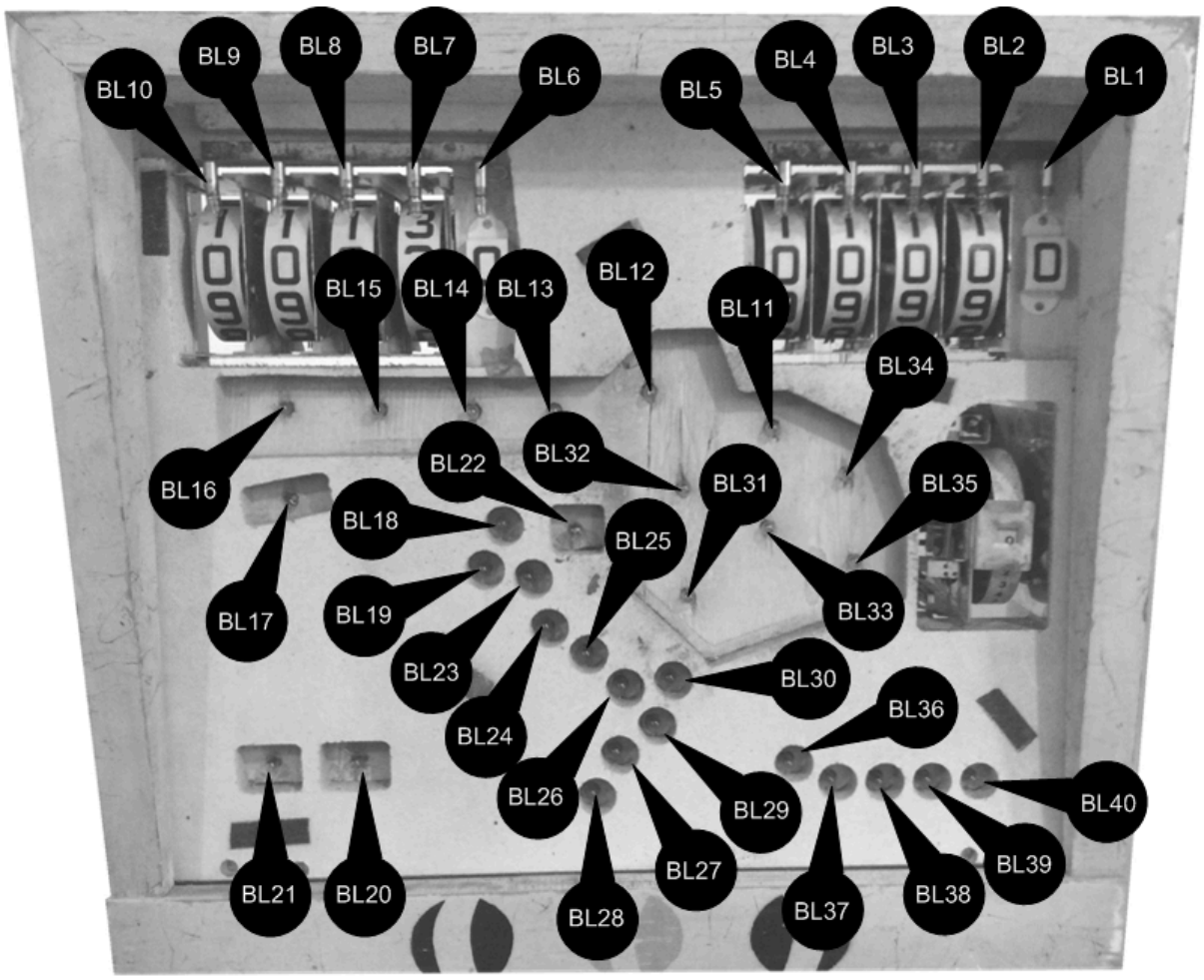
Lamps

Playfield Lamps



Playfield PD8x8 Address 2		0 WHT/GRN	1 WHT/OR	2 WHT/YEL	3 WHT/RED	4 WHT/BLU	5 WHT/GRY	6 WHT/PNK	7 WHT/PUR
0 YEL/GRN	Tag				GI	GI			GI
	Name	*bonus1k*	*bonus2k*	*bonus3k*	*ltSling*	*ltMidLane*	*ltMid1k*	*ltSpecial*	*midPlastic*
	Label	PB1	PB2	PB3	PB5	PB6	PB7	PB11	PB13
1 YEL/BLK	Tag	GI	GI		GI	GI	GI		
	Name	*rtSling*	*rtMidLane*	*rtMid1k*	*rtBank2*	*rtBank1*	*popBumper*	*rtSpecial*	*eightBallHole*
	Label	PB4	PB8	PB9	PB14	PB15	PB23	PB12	PB10
2 YEL/PUR	Tag	GI	GI	GI	GI	GI	GI		GI
	Name	*ltBank1*	*ltBank2*	*topLtLane*	*topMid1*	*topMid2*	*topRtLane*	*eightBall500*	*coinDoor*
	Label	PB22	PB21	PB20	PB19	PB18	PB17	PB16	COINDoor
3 YEL/RED	Tag								
	Name	*ball1*	*ball2*	*ball3*	*ball4*	*ball5*	*ball6*	*ball7*	*NOT USED*
	Label	BALL1	BALL2	BALL3	BALL4	BALL5	BALL6	BALL7	Not Used
4 YEL/BLU	Tag								
	Name	*ball8*	*ball9*	*ball10*	*ball11*	*ball12*	*ball13*	*ball14*	*ball15*
	Label	BALL8	BALL9	BALL10	BALL11	BALL12	BALL13	BALL14	BALL15

Backbox Lamps



Backbox PD8x8 Address 3		0 BRN/BLU	1 BRN/RED	2 BRN/WH	3 BRN/GRN	4 BRN/YEL	5 BRN/GRY	6 BRN/OR	7 BRN/PNK
0 PUR/BLU	Tag						GI	GI	GI
	Name	player2_1	player2_10	player2_100	player2_1k	player2_10k	rtBody	midBody2	guysHair
	Label	BL1	BL2	BL3	BL4	BL5	BL34	BL11	BL12
1 PUR/RED	Tag						GI	GI	GI
	Name	player1_1	player1_10	player1_100	player1_1k	player1_10k	h	g_s	b_i
	Label	BL6	BL7	BL8	BL9	BL10	BL14	BL15	BL16
2 PUR/WH	Tag	GI							
	Name	o_t	gameOver	match90	match80	match70	match60	match50	tilt
	Label	BL13	BL22	BL18	BL19	BL23	BL24	BL25	BL17
3 PUR/GRN	Tag						GI	GI	GI
	Name	match40	match10	match00	match20	match30	ltLeg	ltBody	midBody1
	Label	BL26	BL27	BL28	BL29	BL30	BL31	BL32	BL33
4 PUR/YEL	Tag								GI
	Name	player2	player1	bip2	bip4	bip1	bip3	bip5	rtLeg
	Label	BL20	BL21	BL36	BL37	BL38	BL39	BL40	BL35

Connectors

PD-16 Boards (coils)

Playfield & Credit Reel Bank A Common: WHT/GRN
PD-16 Address 0 Bank B Common: WHT/BRN & WHT/RED

Num	Label	Bank	Pin	Color
0	flipperLeftMain	A	1	GRY/YEL
1	flipperRightMain	A	3	GRY/WHT
2	gameCounter	A	4	GRY/BLK
3	knocker	A	5	GRY/BRN
4	chime1	A	6	GRY/RED
5	chime2	A	7	GRY/GRN
6	chime3	A	8	GRY/BLU
7	troughEject	A	9	GRY/PNK
0	diverter	B	1	BRN/PNK
1	popBumper	B	2	BRN/YEL
2	eightBallKickout	B	4	BRN/GRY
3	creditAdd	B	5	YEL/BRN
4	creditSubtract	B	6	YEL/RED
5	leftSling	B	7	BRN/GRN
6	rightSling	B	8	BRN/WHT
7	(not used)	B	9	

Backbox & High Power Bank A Common: WHT/PUR
PD-16 Address 1 Bank B Common: WHT/BLU

	Num	Label	Bank	Pin	Color
	0	player1_10	A	1	PUR/YEL
	1	player1_100	A	3	PUR/WHT
	2	player1_1k	A	4	PUR/OR
	3	player1_10k	A	5	PUR/BLU
	4	player2_10	A	6	PUR/PNK
	5	player2_100	A	7	PUR/GRY
	6	player2_1k	A	8	PUR/GRN
	7	player2_10k	A	9	PUR/GLD
70 volts DC	0	rightBankReset1	B	1	BRN/BLU
70 volts DC	1	rightBankReset2	B	2	YEL/BLK
70 volts DC	2	leftBankReset1	B	4	BRN/RED
70 volts DC	3	leftBankReset2	B	5	YEL/BLU
70 volts DC	4	(not used)	B	6	
70 volts DC	5	(not used)	B	7	
70 volts DC	6	(not used)	B	8	
70 volts DC	7	(not used)	B	9	

PD-8x8 Connectors (Lamps)

Backbox

PD-8x8 Address 3

J7 9-pin .156

Pin	Color	Name
1	Brn/Blu	Row 0
2	Key	Key Pin
3	Brn/Red	Row 1
4	Brn/Wh	Row 2
5	Brn/Grn	Row 3
6	Brn/Yel	Row 4
7	Brn/Gray	Row 5
8	Brn/Or	Row 6
9	Brn/Pnk	Row 7

J11 9-pin .156

Pin	Color	Name
1	Pur/Blu	Column 0
2	Pur/Rd	Column 1
3	Key	Key Pin
4	Pur/Wh	Column 2
5	Pur/Grn	Column 3
6	Pur/Yel	Column 4
7	NC	Not Connected
8	NC	Not Connected
9	NC	Not Connected

Playfield

PD-8x8 Address 4

J7 9-pin .156

Pin	Color	Name
1	Wh/Grn	Row 0
2	Key	Key Pin
3	Wh/Or	Row 1
4	Wh/Yel	Row 2
5	Wh/Rd	Row 3
6	Wh/Blu	Row 4
7	Wh/Gray	Row 5
8	Wh/Pnk	Row 6
9	Wh/Pur	Row 7

J11 9-pin .156

Pin	Color	Name
1	Yel/Grn	Column 0
2	Yel/Blk	Column 1
3	Key	Key Pin
4	Yel/Pur	Column 2
5	Yel/Rd	Column 3
6	Yel/Blu	Column 4
7	NC	Not Connected
8	NC	Not Connected
9	NC	Not Connected

P-ROC Connectors

Category Direct Switches
Board P-ROC

J6 10 pin .100

Pin	Color	Name
1	Yel/Or	Player 2, 10k, 5
2	Yel/Brn	Player 2, 10k, 0
3	Yel/Pur	Player 2, 1k, 5
4	Yel/Gry	Player 2, 1k, 0
5	*Key*	*Key Pin*
6	Yel/Pnk	Player 2, 100, 5
7	Yel/Grn	Player 2, 100, 0
8	Yel/Rd	Player 2, 10, 5
9	Yel/Blu	Player 2, 10, 0
10	Gray	Ground/Common

J15 12 pin .100

Pin	Color	Name
1	Gray	*Ground/Common*
2	Wh/Blu	Player 1, 10, 0
3	Wh/Rd	Player 1, 10, 5
4	Wh/Grn	Player 1, 100, 0
5	*Key*	*Key Pin*
6	Wh/Yel	Player 1, 100, 5
7	Wh/Pur	Player 1, 1k, 0
8	Wh/Brn	Player 1, 1k, 5
9	Wh/Or	Player 1, 10k, 0
10	Wh/Pnk	Player 1, 10k, 5
11	Gray	Ground/Common
12	*NC*	*Not Connected*

J25 10 pin .100

Pin	Color	Name
1	Blu/Wh	Credit Reel 0
2	*Key*	*Key Pin*
3	Blu/Rd	Credit Reel 1+
4	Blu/Grn	Credit Reel Max
5	Blu/Pnk	Slam Tilt
6	*NC*	*Not Connected*
7	*NC*	*Not Connected*
8	*NC*	*Not Connected*
9	*NC*	*Not Connected*
10	Gray	Ground/Common

J33 10 pin .100

Pin	Color	Name
1	Blu/Lt Blu	Start Button
2	Blu/Yel	Right Flipper
3	*Key*	*Key Pin*
4	Blu/Or	Left Flipper
5	Blu/Gold	Time Machine
6	Blu/Gray	Tilt
7	*NC*	*Not Connected*
8	*NC*	*Not Connected*
9	*NC*	*Not Connected*
10	Gray	Ground/Common

Category Matrix Switches
Board P-ROC

J21 9 pin .100 Columns

Pin	Color	Name
1	Or/Gry	Column 0
2	Key	Key Pin
3	Or/Yel	Column 1
4	Or/Wh	Column 2
5	Or/Grn	Column 3
6	Or/Blk	Column 4
7	NC	Not Connected
8	NC	Not Connected
9	NC	Not Connected

J24 10 pin .100 Rows

Pin	Color	Name
1	Pur/Gry	Row 0
2	Pur/Yel	Row 1
3	Pur/Wh	Row 2
4	Key	Key Pin
5	Pur/Grn	Row 3
6	Pur/Blu	Row 4
7	Pur/Gld	Row 5
8	Pur/Or	Row 6
9	Pur/Pnk	Row 7
10	Gray	Ground

Game Operation

Big Shot is powered by a HardKernel ODROID U3 running Ubuntu 13.10. Though this release is no longer supported by Ubuntu, later releases are not yet supported by the computer due to the specialized nature of the SoC (System-on-Chip) used. When a supported version of Ubuntu is released, it can be upgraded without issue.

ODROID Power

Power for the ODROID is supplied via a transformer plugged in to the “always-hot” outlet inside the cabinet. When the machine is plugged in, the ODROID turns on. It then waits for the P-ROC to turn on before running game code. Since the P-ROC and all other power is switched on/off by the under-cabinet toggle switch, the behavior of turning the machine on/off is just like any other pinball machine.

Since the ODROID always runs, it is necessary to power down the computer gracefully before unplugging the pinball machine. This is not ideal, and can be addressed with a smart UPS that plugs directly into the ODROID that can buffer power while the machine shuts down gracefully (at which point all power would be switched), but the UPS board is not yet available.

The filesystem has been partially locked to prevent damage from accidental loss of power.

Remotely connecting to the machine

The ODROID has been hardcoded with IP addresses on each of its interfaces. The Ethernet jack is set to 10.1.2.250, and the wireless has been set to 192.168.1.250. Simply ssh to one of those IPs with the username “odroid” to access the terminal.

You can also copy files back and forth using sFTP with the same setup.

Troubleshooting

There is extensive logging in the Mission Pinball Framework. To see a log of the game, connect to the terminal and browse to /media/mpf/logs. There you'll see a log file from every game played, and inside each log file you'll see just about every event you can imagine.

If the game is crashing, likely due to some change when developing, the logs aren't always enough. In some situations, it's useful to see the terminal while a game is running. Since the game normally runs in the background, we have to take a few steps to start a game at the console.

First, if the game is currently running (not likely since this is the crashing section), you need to stop it. To do this, run the command `sudo top` and look for the process called "python." From there, press "k" (for kill), then type in the Process ID that you see next to "python". Press Enter twice, and the game should turn off.

To run the game from the command prompt, run the following commands:

```
cd /media/mpf
./startup.sh
```

The startup.sh script runs a more elaborate command:

```
python mpf.py machine_files/big_shot -c config/odroid_config -v
```

This command breaks down to:

- `python` – Runs python!
- `mpf.py` – Specifies the primary Mission Pinball Framework python file
- `machine_files/big_shot` – Specifies the path to machine-specific files like shows, scriptlets, and config files
- `-c config/odroid_config` – Optional. Specifies a specific config file. In this case, one specifically made for the ODROID that disables the LCD and keyboard support since neither are present
- `-v` – Optional. Turns on verbose logging.

A more detailed command reference can be found at MissionPinball.com as part of the Mission Pinball Framework documentation.

Appendix: Spec Sheets

P-ROC Spec Sheet

P-ROC

Pinball – Remote Operations Controller

by Gerry Stellenberg

Version 2.3 – June 10, 2011

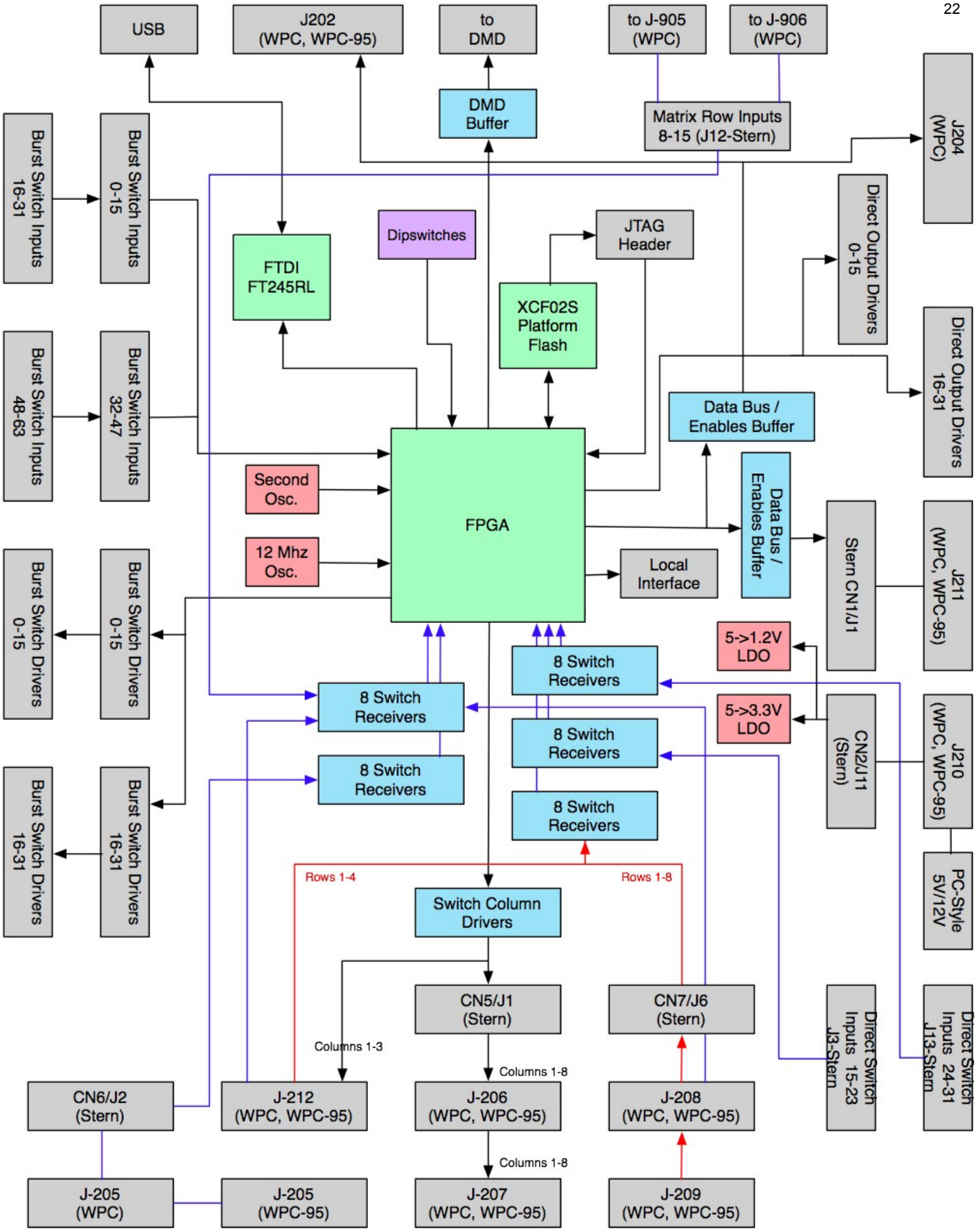
Table of Contents

1 Introduction

The P-ROC is designed to control all of the real-time signaling features on a pinball machine. Major functionality includes:

- Communication with a host processor via USB
- Communication with an embedded controller via a custom local interface
- Ability to drive and receive results for 224 switches
  - 32 direct switches
    - 16 should be compatible with WPC/WPC-95 direct switch inputs
  - 128 switches in an 8x16 matrix
    - Compatible with WPC/WPC-95 8x8 switch matrices
    - Compatible with Stern Whitestar 8x8 and S.A.M. 8x16 switch matrices
  - 64 individual burst switches for frequency controlled IR devices
- Ability to drive 216 logic level outputs
  - 32 direct outputs (for immediate response)
  - 184 multiplexed/matrixed outputs
    - Compatible with WPC/WPC-95/Whitestar/S.A.M. driving circuits
  - Outputs can be programmed by a host or can change as a result of switch events
  - Outputs can be configured to drive until turned off or until a timer expires
  - Outputs can be configured to automatically turn on at programmed time intervals with an optional timer
  - Outputs can be configured to turn on/off repeatedly with on/off timers.
- Ability to drive a serial chain of PinballControllers.com Driver Boards
  - Driver Boards can be fed multiplexed output data
  - Driver Boards can be programmed directly by software
- Ability to drive a Dot Matrix Display
- Ability to disable all drivers when communication with the host is lost

2 Block Diagram



3 Theory of Operation

The P-ROC consists primarily of an FPGA, supporting logic, and a bunch of connectors. The FPGA is responsible for driving all of the real-time signaling features on a pinball machine. The FPGA has direct control of the switch inputs and outputs, drive outputs, and DMD outputs. Upon power-up, the FPGA receives its default configuration from an onboard Xilinx System Flash (XCF02S). It then waits for additional configuration information from a host software program over a USB bus or from an embedded controller through a local interface port.

The USB signaling is handled by an FTDI FT245RL device, which has a FIFO interface connected to the FPGA. All information being delivered to the FPGA is held in the FIFO until the FPGA reads it. Similarly, all data written into the FIFO by the FPGA is held until the host requests it.

The local interface port allows the P-ROC to be controlled by an embedded controller connected to the P-ROC through a 16-bit ribbon cable. This port connects directly to the FPGA. When not used for the local interface, this port connects to a PinballControllers.com Master Driver Board through the 16-bit ribbon cable.

Once configured by the host software program, the FPGA continuously performs functions such as driving the switch outputs, scanning the switch inputs, and turning on and off the output drivers either due to a change of state in a switch or due to a request from the host software program. The FPGA is also used to drive an external dot matrix display, reprogram the Xilinx System Flash, read the on-board dipswitches, and toggle status LEDs. The FPGA can also be configured to disable all output drivers if an internal watchdog timer expires.

4 Functional Descriptions

4.1 USB

A USB interface is used to connect the P-ROC to a host computer. Connectivity is provided with a type-B USB connector, and the signaling is controlled by an FTDI FT245RL device. The FTDI chip's FIFO (first-in first-out memory) is connected to the FPGA, which can read data from and write data into the FIFO. This interface is enabled when dipswitch 2 is off.

4.2 Local Interface

A local interface is provided for connectivity to an embedded microcontroller. Connectivity is provided through a 16-bit ribbon cable header (J34) using 4 data bits and 4 control bits. This interface is enabled when dipswitch 2 is on.

4.3 Serial Driver Board Interface

When dipswitch 2 is off, disabling the local interface, the 16-bit ribbon cable header (J34) can be connected to a PinballControllers.com Master Driver Board (or Master combo board) which is the first board in a chain of Driver Boards.

4.4 Switch Drivers and Outputs

There are three types of switch circuits:

- Burst – All 32 drivers and 64 inputs are connected directly to the FPGA. The drivers can be configured in the FPGA to drive a certain number of pulses, each a configurable number of microseconds, before turning off for another configurable number of microseconds. This functionality is necessary to enable frequency tuned infrared receivers to accurately receive infrared light from the pulsed emitters.

- Direct – There are 32 direct switch inputs, and there are no drivers. The driver side of each direct switch is simply grounded. The switch inputs are individually compared with a reference, and the comparison results are fed into the FPGA. Note, when using an 8x16 switch matrix (description follows), the 1st 8 direct switches are used for the matrix.

- Matrix – There are 8 column drivers and 16 row inputs which allow the FPGA to scan 128 externally matrixed switches. The drivers are connected directly to the FPGA. The 16 row inputs are individually compared with a reference, and the comparison results are fed into the FPGA. Note, the second set of 8 row inputs use the same comparison circuitry as the first 8 direct switch inputs.

4.5 Output Drivers

There are two types of output drivers:

- Direct – All 32 direct drivers are connected directly to the FPGA.

- Bussed/Muxed – The 176 bussed/muxed drivers are multiplexed on an 8-bit data bus with enable bits. The enable bits can be configured as individual enables or encoded enables for compatibility with WPC/WPC-95 and Stern Whitestar and S.A.M. systems.
  - When configured as individual enables, 6 enable bits are used for bussed drivers, and 2 are used to enable the matrix columns and rows. Therefore, in this mode, the total number of usable bussed drivers is limited to 48, and the matrix is limited to an 8x8 matrix.
  - When configured as encoded enables, four enable bits are used to encode the enables.
    - Any multiple of 8 drivers can be used for the matrix, leaving the remaining drivers for use outside the matrix.
    - If no matrix is used, all 16 encoded values can be used to enable 8 drivers. So the number of usable drivers would be limited to 128.
    - If an 8x16 matrix is used, consuming 128 drivers and 3 enable values, only 48 drivers would remain for use outside the matrix.
  - These drivers are also sent out on the Serial Driver Board Interface when dipswitch 2 is off.

Each output driver can operate in four ways:

- Solid – Output drivers can be configured to be on until they are reconfigured to be off.

- Timed – Output drivers can be configured to be on for a specific number of milliseconds before turning off.

- Scheduled – Output drivers can be configured to turn on at scheduled times and stay on for a specific number of milliseconds before the schedule is disabled. The scheduled times can be one or more points in time spaced approximately 1/32 of a second apart.

- Patter – Output drivers can be configured to turn repeatedly turn on for a specific number of milliseconds and then off for a specific number of milliseconds.

4.6 Dot Matrix Display Driver

The FPGA can control the driving of an external dot matrix display. Internal FPGA memory is filled by the host software program, and the FPGA will periodically retrieve the next available data word from the memory, convert it into the dot matrix display signals, and output those signals.

4.7 Clocks

Everything runs off of a 12 Mhz Clock (clk_a). 12 Mhz is used because the FTDI chip runs at 12 Mhz. Because most of the internal logic is based off of microsecond or millisecond timing, 12 Mhz provides plenty of resolution while making it trivial to meet timing in the FPGA.

A secondary clock may be provided for future functionality. The frequency is TBD.

4.8 Configuration

On power-up, the FPGA, operating in Master Serial mode, automatically loads itself from the Xilinx Platform Flash. Once loaded the FPGA waits to be further configured by the host through the USB bus.

If the FPGA ever needs to be updated, it is capable of driving the JTAG pins connected to the Xilinx Platform Flash. The host software can write an image into the FPGA which will then write the image into the Platform Flash. Note, if this operation begins and does not completely successfully, the image in the Platform Flash will be corrupted. This will keep the FPGA from automatically loading correctly on future power-ups until the Platform Flash is replaced or reprogrammed.

A JTAG header is provided as another way to load the FPGA or to rewrite the image in the Xilinx Platform Flash. Using the JTAG header requires a Xilinx programming cable connected to a computer running Xilinx's programming software.

4.9 Dipswitches

There are 4 dipswitches on the P-ROC. They are used as follows:

Switch	Function
1	Off : WPC On : Stern
2	Off : FTDI On : Local
3	Off : DMD On : enables[9:12]
4	Undefined

Switch 1 controls the polarity of the clear signal. When switch 1 is off, the signal goes high to disable driver circuits and low to activate them (needed by WPC). When switch 1 is a on, the signal goes low to disable driver circuits and high to activate them (needed by Stern).

Switch 2 determines which host interface is active. When switch 2 is off, the FTDI FIFO interface is used. Otherwise, the local bus interface is used.

Switch 3 determines the default operation of the DMD pins. When off, the DMD pins carry the DMD signals. When on, the DMD pins carry output driver enables 9 through 12 as follows:

DMD Signal	Output Driver Enable
rdata	9
rclk	10
latch	11
sdata	12

In addition to the DMD, these signals go to J36, which is equivalent to the WPC CPU board's Display Port header (J204). This mapping ensures that output driver enables 9 through 12 match J204's DIS1 through DIS4 signals, respectively. J204's DIS_STROBE signal is mapped to enable 8 on the P-ROC.

4.10 Status

There are 3 power leds. When behaving normally, they should all on when the board has power.

LED	Voltage Indication
D49	Switch Power (WPC: 12V, Stern: 5V)
D50	3.3V
D52	5V

There are 8 LEDs on the board to provide visual indications about the functionality of the board. The LEDs are driven by the FPGA as follows:

LED	Meaning
D41	FPGA initialized properly
D42	12 Mhz clock operational
D43	USB communications established
D44	Watchdog timer expired (Drivers disabled)
D45	Pattern*
D46	Pattern*
D47	Pattern*
D48	Pattern*

* D45 through D48 display a rotating pattern. Normal operation is indicated by a single light rotating counter clockwise.

4.11 Connectors

J1	WPC Direct Switch Inputs to Fliptronic II Board (J906)	
6-pin Molex: 0.100” spacing		
1	Direct Switch Input 0	I
2	KEY	N/A
3	Direct Switch Input 2	I
4	Direct Switch Input 4	I
5	Direct Switch Input 6	I
6	Ground	O

J2	WPC Direct Switch Inputs to Fliptronic II Board (J905)	
6-pin Molex: 0.100” spacing		
1	Direct Switch Input 1	I
2	Direct Switch Input 3	I
3	Direct Switch Input 5	I
4	KEY	N/A
5	Direct Switch Input 7	I
6	Ground	O

J3	Dot Matrix Display				
24-pin Header: 0.100” spacing					
1	Data Enable	O	2	Ground	O
3	Row Data	O	4	Ground	O
5	Row clock	O	6	Ground	O
7	Column Latch	O	8	Ground	O
9	Dot Clock	O	10	Ground	O
11	S Data	O	12	Ground	O
13	Ground	O	14	Ground	O

J4	WPC-x Output Driver Data/Enables to Fliptronic II Board				
36-pin Header 0.100” spacing					
1	Output Driver Data 7	O	2	Ground	O
3	Output Driver Data 6	O	4	Ground	O
5	Output Driver Data 5	O	6	Ground	O

7	Output Driver Data 4	O	8	Ground	O[33]
9	Output Driver Data 3	O	10	Ground	O
11	Output Driver Data 2	O	12	Ground	O
13	Output Driver Data 1	O	14	Ground	O
15	Output Driver Data 0	O	16	Ground	O
17	VCC	O	18	Ground	O
19	Ground	O	20	Ground	O
21	VCC	O	22	Ground	O
23	Output Driver Enable 0	O	24	Ground	O
25	Ground	O	26	Ground	O
27	Clear	O	28	Ground	O
29	Ground	O	30	Ground	O
31	Ground	O	32	N/C	N/A
33	NC	N/A	34	N/C	N/A

J5	**USB**	
4-pin USB Type B		
1	5B	I
2	Data-	I/O
3	Data+	I/O
4	Ground	I

J6	**Stern S.A.M. Switch Row Inputs 8-15**	
10-pin Molex: 0.156” spacing		
1	Direct Switch Input 7 / Row 15	I
2	Direct Switch Input 6 / Row 14	I
3	Direct Switch Input 5 / Row 13	I
4	Direct Switch Input 4 / Row 12	I
5	KEY	N/A
6	Direct Switch Input 3 / Row 11	I
7	Direct Switch Input 2 / Row 10	I
8	Direct Switch Input 1 / Row 9	I
9	Direct Switch Input 0 / Row 8	I

10	Ground	O

J7	Burst Switches				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 16	O
3	3.3V	O	4	Burst Switch Driver 17	O
5	Burst Switch Driver 22	O	6	Burst Switch Driver 18	O
7	Ground	O	8	Burst Switch Driver 19	O
9	Ground	O	10	Burst Switch Driver 20	O
11	Ground	O	12	Burst Switch Driver 21	O
13	Burst Switch Driver 23	O	14	Burst Switch Input 16	O
15	Ground	O	16	Burst Switch Input 17	O
17	Ground	O	18	Burst Switch Input 18	O
19	Ground	O	20	Burst Switch Input 19	O
21	Burst Switch Input 23	O	22	Burst Switch Input 20	O
23	3.3V	O	24	Burst Switch Input 21	O
25	3.3V	O	26	Burst Switch Input 22	O

J8	Burst Switches				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 0	O
3	3.3V	O	4	Burst Switch Driver 1	O
5	Burst Switch Driver 6	O	6	Burst Switch Driver 2	O
7	Ground	O	8	Burst Switch Driver 3	O
9	Ground	O	10	Burst Switch Driver 4	O
11	Ground	O	12	Burst Switch Driver 5	O
13	Burst Switch Driver 7	O	14	Burst Switch Input 32	O
15	Ground	O	16	Burst Switch Input 33	O
17	Ground	O	18	Burst Switch Input 34	O
19	Ground	O	20	Burst Switch Input 35	O
21	Burst Switch Input 39	O	22	Burst Switch Input 36	O
23	3.3V	O	24	Burst Switch Input 37	O
25	3.3V	O	26	Burst Switch Input 39	O

J9	Burst Switches				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 8	O
3	3.3V	O	4	Burst Switch Driver 9	O
5	Burst Switch Driver 14	O	6	Burst Switch Driver 10	O

7	Ground	O	8	Burst Switch Driver 11	O
9	Ground	O	10	Burst Switch Driver 12	O
11	Ground	O	12	Burst Switch Driver 13	O
13	Burst Switch Driver 15	O	14	Burst Switch Input 8	O
15	Ground	O	16	Burst Switch Input 9	O
17	Ground	O	18	Burst Switch Input 10	O
19	Ground	O	20	Burst Switch Input 11	O
21	Burst Switch Input 15	O	22	Burst Switch Input 12	O
23	3.3V	O	24	Burst Switch Input 13	O
25	3.3V	O	26	Burst Switch Input 14	O

J10	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 24	O
3	3.3V	O	4	Burst Switch Driver 25	O
5	Burst Switch Driver 30	O	6	Burst Switch Driver 26	O
7	Ground	O	8	Burst Switch Driver 27	O
9	Ground	O	10	Burst Switch Driver 28	O
11	Ground	O	12	Burst Switch Driver 29	O
13	Burst Switch Driver 31	O	14	Burst Switch Input 56	O
15	Ground	O	16	Burst Switch Input 57	O
17	Ground	O	18	Burst Switch Input 58	O
19	Ground	O	20	Burst Switch Input 59	O
21	Burst Switch Input 63	O	22	Burst Switch Input 60	O
23	3.3V	O	24	Burst Switch Input 61	O
25	3.3V	O	26	Burst Switch Input 62	O

J11	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 16	O
3	3.3V	O	4	Burst Switch Driver 17	O
5	Burst Switch Driver 22	O	6	Burst Switch Driver 18	O
7	Ground	O	8	Burst Switch Driver 19	O
9	Ground	O	10	Burst Switch Driver 20	O
11	Ground	O	12	Burst Switch Driver 21	O
13	Burst Switch Driver 23	O	14	Burst Switch Input 48	O
15	Ground	O	16	Burst Switch Input 49	O
17	Ground	O	18	Burst Switch Input 50	O

19	Ground	O	20	Burst Switch Input 51	O
21	Burst Switch Input 55	O	22	Burst Switch Input 52	O
23	3.3V	O	24	Burst Switch Input 53	O
25	3.3V	O	26	Burst Switch Input 54	O

J12	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 0	O
3	3.3V	O	4	Burst Switch Driver 1	O
5	Burst Switch Driver 6	O	6	Burst Switch Driver 2	O
7	Ground	O	8	Burst Switch Driver 3	O
9	Ground	O	10	Burst Switch Driver 4	O
11	Ground	O	12	Burst Switch Driver 5	O
13	Burst Switch Driver 7	O	14	Burst Switch Input 0	O
15	Ground	O	16	Burst Switch Input 1	O
17	Ground	O	18	Burst Switch Input 2	O
19	Ground	O	20	Burst Switch Input 3	O
21	Burst Switch Input 7	O	22	Burst Switch Input 4	O
23	3.3V	O	24	Burst Switch Input 5	O
25	3.3V	O	26	Burst Switch Input 6	O

J13	**Burst Switches**				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	Burst Switch Driver 8	O
3	3.3V	O	4	Burst Switch Driver 9	O
5	Burst Switch Driver 14	O	6	Burst Switch Driver 10	O
7	Ground	O	8	Burst Switch Driver 11	O
9	Ground	O	10	Burst Switch Driver 12	O
11	Ground	O	12	Burst Switch Driver 13	O
13	Burst Switch Driver 15	O	14	Burst Switch Input 40	O
15	Ground	O	16	Burst Switch Input 41	O
17	Ground	O	18	Burst Switch Input 42	O
19	Ground	O	20	Burst Switch Input 43	O
21	Burst Switch Input 47	O	22	Burst Switch Input 44	O
23	3.3V	O	24	Burst Switch Input 45	O
25	3.3V	O	26	Burst Switch Input 46	O

J14	**Burst Switches**
26-pin Header: 0.100” spacing	

1	3.3V	O	2	Burst Switch Driver 24	O
3	3.3V	O	4	Burst Switch Driver 25	O
5	Burst Switch Driver 30	O	6	Burst Switch Driver 26	O
7	Ground	O	8	Burst Switch Driver 27	O
9	Ground	O	10	Burst Switch Driver 28	O
11	Ground	O	12	Burst Switch Driver 29	O
13	Burst Switch Driver 31	O	14	Burst Switch Input 24	O
15	Ground	O	16	Burst Switch Input 25	O
17	Ground	O	18	Burst Switch Input 26	O
19	Ground	O	20	Burst Switch Input 27	O
21	Burst Switch Input 31	O	22	Burst Switch Input 27	O
23	3.3V	O	24	Burst Switch Input 29	O
25	3.3V	O	26	Burst Switch Input 30	O

J15	**Stern Whitestar & S.A.M. Direct Switch Inputs**	
12-pin Molex: 0.156” spacing		
1	Ground	O
2	Direct Switch Input 8	I
3	Direct Switch Input 9	I
4	Direct Switch Input 10	I
5	KEY	N/A
6	Direct Switch Input 11	I
7	Direct Switch Input 12	I
8	Direct Switch Input 13	I
9	Direct Switch Input 14	I
10	Direct Switch Input 15	I
11	Ground	O
12	NC	N/A

J16	**WPC Switch Column/Row WPC-95 Switch Column/Row, Direct**	
13-pin Molex: 0.100” spacing		
1	Column 1	O
2	Column 2	O
3	Column 3	O
4	Row 1	I
5	KEY	N/A

6	Row 2	I
7	Row 3	I
8	Row 4	I
9	Direct Switch Input 0	I
10	Direct Switch Input 1	I
11	Direct Switch Input 2	I
12	Direct Switch Input 3	I
13	Ground	O

J17	**Unused**

J18	**WPC Direct Switch Inputs**	
12-pin Molex: 0.100” spacing		
1	Direct Switch Input 8	I
2	Direct Switch Input 9	I
3	Direct Switch Input 10	I
4	Direct Switch Input 11	I
5	NC	N/A
6	Direct Switch Input 12	I
7	Direct Switch Input 13	I
8	Direct Switch Input 14	I
9	Direct Switch Input 15	I
10	Ground	O
11	KEY	N/A
12	Switch Clear	O

J19/J20	**WPC-x Switch Column Drivers**	
9-Pin Molex: 0.100” spacing		
1	Column 0	O
2	Column 1	O
3	Column 2	O
4	Column 3	O
5	Column 4	O
6	Column 5	O
7	Column 6	O
8	KEY	N/A
9	Column 7	O

J21	Stern Whitestar & S.A.M. Switch Column Drivers	
9-Pin Molex: 0.156” spacing		
1	Column 0	O
2	KEY	N/A
3	Column 1	O
4	Column 2	O
5	Column 3	O
6	Column 4	O
7	Column 5	O
8	Column 6	O
9	Column 7	O

J22	WPC-x Switch Row Inputs	
9-pin Molex: 0.100” spacing		
1	Row 0	I
2	Row 1	I
3	Row 2	I
4	Row 3	I
5	Row 4	I
6	KEY	N/A
7	Row 5	I
8	Row 6	I
9	Row 7	I

J23	WPC Switch Row Inputs WPC-95 Switch Row Inputs, Direct Inputs	
14-pin Molex: 0.100” spacing		
1	Row 0	I
2	Row 1	I
3	Row 2	I
4	Row 3	I
5	Row 4	I
6	KEY	N/A
7	Row 5	I
8	Row 6	I
9	Row 7	I
10	Direct Switch Input 4	I

11	Direct Switch Input 5	I
12	Direct Switch Input 6	I
13	Direct Switch Input 7	I
14	Ground	O

J24	**Stern Whitestar & S.A.M. Switch Row Inputs 0-7**	
10-pin Molex: 0.156” spacing		
1	Row 0	I
2	Row 1	I
3	Row 2	I
4	KEY	N/A
5	Row 3	I
6	Row 4	I
7	Row 5	I
8	Row 6	I
9	Row 7	I
10	Ground	O

J25	**Stern S.A.M. Direct Switch Inputs 24-31**	
10-pin Molex: 0.156” spacing		
1	Direct Switch Input 24	I
2	KEY	N/A
3	Direct Switch Input 25	I
4	Direct Switch Input 26	I
5	Direct Switch Input 27	I
6	Direct Switch Input 28	I
7	Direct Switch Input 29	I
8	Direct Switch Input 30	I
9	Direct Switch Input 31	I
10	Ground	O

J26	**Power**	
4-pin Molex: 0.200” spacing		
1	12V	I
2	Ground	I
3	Ground	I
4	VCC (5V)	I

J27	WPC-x Output Driver Data/Enables to Power Driver Board				
34-pin Header: 0.100” spacing					
1	NC	N/A	2	Ground	O
3	NC	N/A	4	Ground	O
5	NC	N/A	6	Ground	O
7	Output Driver Row Enable	O	8	Output Driver Column Enable	O
9	Output Driver Enable 2	O	10	Output Driver Enable 4	O
11	Output Driver Enable 3	O	12	Ouptut Driver Enable 1	O
13	Output Driver Enable 5	O	14	Ground	O
15	Output Driver Data 7	O	16	Ground	O
17	Output Driver Data 6	O	18	Ground	O
19	Output Driver Data 5	O	20	Ground	O
21	Output Driver Data 4	O	22	Ground	O
23	Output Driver Data 3	O	24	Ground	O
25	Output Driver Data 2	O	26	Ground	O
27	Output Driver Data 1	O	28	Ground	O
29	Output Driver Data 0	O	30	Ground	O
31	Clear	O	32	Output Driver Enable 0*	O
33	NC	N/A	34	Enable_Strobe	I

- Note – Pin 32 is connected to Jumper W2 on WPC Power Driver Boards and to the flipper driver enable on WPC-95 Power Driver Boards. For consistency across WPC and WPC-95, the flipper driver enable signal goes to the Fliptronic II board on WPC systems. Therefore, when using this board with a WPC Power Driver Board, disconnect jumper W2 to ensure proper operation of the Fliptronic II board. Failure to remove jumper W2 could create a short if the 18V power rail fails.

J28	Direct Output Drivers 0-15				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	3.3V	O
3	Direct Output Driver 0	O	4	Direct Output Driver 1	O
5	Ground	O	6	Direct Output Driver 2	O
7	Direct Output Driver 3	O	8	Direct Output Driver 4	O
9	Ground	O	10	Direct Output Driver 5	O
11	Direct Output Driver 6	O	12	Direct Output Driver 7	O
13	Ground	O	14	KEY	O
15	Direct Output Driver 8	O	16	Direct Output Driver 9	O
17	Ground	O	18	Direct Output Driver 10	O
19	Direct Output Driver 11	O	20	Direct Output Driver 12	O
21	Ground	O	22	Direct Output Driver 13	O
23	Direct Output Driver 14	O	24	Direct Output Driver 15	O

25	3.3V	O	26	3.3V	O

J29	Direct Output Drivers 16-31				
26-pin Header: 0.100” spacing					
1	3.3V	O	2	3.3V	O
3	Direct Output Driver 16	O	4	Direct Output Driver 17	O
5	Ground	O	6	Direct Output Driver 18	O
7	Direct Output Driver 19	O	8	Direct Output Driver 20	O
9	Ground	O	10	Direct Output Driver 21	O
11	Direct Output Driver 22	O	12	Direct Output Driver 23	O
13	Ground	O	14	KEY	O
15	Direct Output Driver 24	O	16	Direct Output Driver 25	O
17	Ground	O	18	Direct Output Driver 26	O
19	Direct Output Driver 27	O	20	Direct Output Driver 28	O
21	Ground	O	22	Direct Output Driver 29	O
23	Direct Output Driver 30	O	24	Direct Output Driver 31	O
25	3.3V	O	26	3.3V	O

J30	Stern Output Driver Data/Enables to Power Driver Board				
20-pin Header: 0.100” spacing					
1	Output Driver Data 3	O	2	Output Driver Data 4	O
3	Output Driver Data 2	O	4	Output Driver Data 5	O
5	Output Driver Data 1	O	6	Output Driver Data 6	O
7	Output Driver Data 0	O	8	Output Driver Data 7	O
9	NC	N/A	10	NC	N/A
11	Output Driver Enable 7	O	12	Output Driver Enable 0	O
13	Clear	O	14	Output Driver Enable 1	O
15	Output Driver Enable 5 / IOSTB	O	16	Output Driver Enable 2	O
17	Output Driver Enable 4	O	18	Output Driver Enable 3	O
19	Ground	O	20	Ground	O

J31	Stern Whitestar & S.A.M. Power	
6-pin Molex: 0.156” spacing		
1	5V	I
2	Ground	I
3	-12V	I
4	Ground	I
5	KEY	N/A

6	12V	I

J32	WPC-x Power	
7-pin Molex: 0.156” spacing		
1	Ground	I
2	NC	N/A
3	Ground	I
4	VCC (5V)	I
5	VCC (5V)	I
6	12V	I
7	12V	I

J33	Stern S.A.M. Direct Switch Inputs 16-23	
10-pin Molex: 0.156” spacing		
1	Direct Switch Input 16	I
2	Direct Switch Input 17	I
3	KEY	N/A
4	Direct Switch Input 18	I
5	Direct Switch Input 29	I
6	Direct Switch Input 20	I
7	Direct Switch Input 21	I
8	Direct Switch Input 22	I
9	Direct Switch Input 23	I
10	Ground	O

J34	Local Interface (dipswitch 2 on)	
16-pin Header: 0.100” spacing		
1	Local Data 0	I/O
2	Ground	O
3	Local Data 1	I/O
4	Ground	O
5	Local Data 2	I/O
6	Ground	O
7	Local Data 3	I/O
8	Ground	O
9	Local Read	I
10	Ground	O
11	Local Write	I
12	Ground	O
13	Local Full	O
14	Ground	O
15	Local Empty	O
16	Ground	O

J34	Serial Driver Board Interface (dipswitch 2 off)	
16-pin Header: 0.100” spacing		
1	Serial Driver Board Data	O
2	Ground	O
3	RESERVED	N/A
4	Ground	O
5	RESERVED	N/A
6	Ground	O
7	RESERVED	N/A
8	Ground	O
9	RESERVED	N/A
10	Ground	O
11	RESERVED	N/A
12	Ground	O
13	RESERVED	N/A
14	Ground	O
15	RESERVED	N/A
16	Ground	O

J35	JTAG Port	
14-pin Header: 2mm spacing		
1	Ground	O
2	3.3V	O
3	Ground	O
4	TMS	I
5	Ground	O
6	TCK	I
7	Ground	O
8	TDO	O
9	Ground	O
10	TDI	I
11	Ground	O
12	Ground	O
13	Ground	O
14	Ground	O

J36	WPC Display Port	
26-pin Header: 2mm spacing		
1	Output Driver Enable 12	O
2	Output Driver Enable 11	O
3	Output Driver Enable 10	O
4	Ground	O
5	Output Driver Enable 9	O
4	Ground	O
7	Output Driver Enable 8	O
8	Ground	O
9	Clear	O
10	Ground	O
11	Data 7	O
12	Ground	O
13	Data 6	O
14	Ground	O
15	Data 5	O
16	Ground	O
17	Data 4	O
18	Ground	O
19	Data 3	O
20	Ground	O
21	Data 2	O
22	Ground	O
23	Data 1	O
24	Ground	O
25	Data 0	O
26	Ground	O

4.12 Power

There are 3 power connectors that can be used to connect the 12V and 5V power rails. Only one should be used at any one time. J26 is pin compatible with a standard personal computer 4-pin power supply cable commonly used to power disk drives. J32 is pin compatible with the power supply cable used in WPC and WPC-95 pinball machines. J31 is pin compatible with the power supply cable used in Stern Whitestar and S.A.M. pinball machines.

3.3V is created from the 5V supply using a 3 amp LDO in a DD-PACK package. Components are available from ST Micro, Linear Tech, TI, and National Semi. 3.3V is used by most of the parts on the board. In addition, external burst switch circuitry is expected to use 3.3V from this board.

1.2V is created from the 5V supply using a 300 milliamp LDO in a SOT23-5 package. Components are available from On Semi and Analog Devices. 1.2V is used for the FPGA's core.

5V is optionally used to power the 74HCT244 buffers used on the output driver data/enables bus and the dot matrix display signals. Resistor stuff options allow the buffers to alternatively run on 3.3V. Which voltage to use depends on the circuitry connected to J3, J4, J27, and J30.

The switch voltage depends on which power connector is used to power the board. WPC machines use a 12V switch matrix; so if J26 or J32 is used, the incoming 12V powers the switch voltage. Stern machines use a 5V switch matrix; so if J31 is used, its 12V feeds a 5V LDO, which creates the switch voltage.

PD-8x8 Spec Sheet

Power Driver Matrix 8x8

Version 1.0 – July 11, 2011

http://www.pinballcontrollers.com

General Description:

The P-ROC Driver Boards are used to control the activation of connected devices by turning on or off power to the devices in response to commands from a P-ROC. The boards receive commands from the P-ROC over an RS-485 serial bus which allows many boards to be chained together and used simultaneously. There are three different types of Driver Boards that can be used to make up a chain: Master, Power Driver 16, and Power Driver Matrix 8x8.

Power Driver Matrix 8x8 Details:

The Power Driver Matrix 8x8 has one bank of 8 p-channel MOSFETs (bank A) and one bank of 8 n-channel MOSFETs (bank B). The p-channel FETs supply power to external devices when activated, and the n-channel FETs create a path to ground when activated. Each bank has a power input header.

Bank A can accept DC power up to 20V. The power goes through a fuse and then to the p-channel FETs which can supply it to the external devices through a keyed 9-pin header.

Bank B works identically to each bank on the Power Driver 16 board, accepting DC input power of up to 80V, using that as a reference for the n-channel FETs, and providing a convenience output header that can be used to supply constant power to external devices. The FETs are connected to a keyed 9-pin header, and they complete the path to ground when commanded to by the P-ROC.

These board are typically used to control lamp/LED matrixes as large as 8x8. Larger matrixes can be controlled by chaining multiple boards together.

All 16 circuits require an active high signal from the controller (P-ROC, Arduino, etc) to turn on and an active low signal to turn off. Logic on the board itself takes care of driving the transistors properly.

Connectors:

J1	Logic Power	Required
2-pin Molex: 0.156” spacing		
1	5V	I
2	Ground	I

J9	Serial Data In	Required
2-pin Molex: 0.100” spacing		
1	Serial+	I
2	Serial-	I

J10	Serial Data Out	Not Required
2-pin Molex: 0.100” spacing		
1	Serial+	O
2	Serial-	O

J2	Bank A High Power In	Required if using Bank A
3-pin Molex: 0.156” spacing		
1	5 to 20V DC	I
2	KEY	N/A
3	Ground	I

J7	Bank A Device Power Outputs	Required if using Bank A
9-pin Molex: 0.156” spacing		
1	Bank A – Data 0	I
2	KEY	N/A
3	Bank A – Data 1	I
4	Bank A – Data 2	I
5	Bank A – Data 3	I
6	Bank A – Data 4	I
7	Bank A – Data 5	I
8	Bank A – Data 6	I
9	Bank A – Data 7	I

J6	Bank B High Power In	Required if using Bank B
3-pin Molex: 0.156” spacing		
1	5 to 80V DC	I
2	KEY	N/A
3	Ground	I

J4	Bank B High Power Out	Recommended if using Bank B
3-pin Molex: 0.156” spacing		
1	Fused High Power Out	O
2	Fused High Power Out	O
3	KEY	N/A

J11	Bank B Device Inputs	Required if using Bank B
9-pin Molex: 0.156” spacing		
1	Bank B – Data 0	I
2	Bank B – Data 1	I
3	KEY	N/A
4	Bank B – Data 2	I
5	Bank B – Data 3	I
6	Bank B – Data 4	I
7	Bank B – Data 5	I
8	Bank B – Data 6	I
9	Bank B – Data 7	I

Addressing:

In order to receive the correct data from the P-ROC, each board's address needs to be set appropriately. The following table describes how to use the dipswitches to set the board address:

Dipswitch	Meaning*
1	Address bit 0
2	Address bit 1
3	Address bit 2
4	Address bit 3

*On=1, Off=0

When the P-ROC is configured, groups of 8 data bits are assigned to indexes. Bits 3:1 of those indexes should correspond to the desired Driver Board's address, and bit 0 corresponds to the desired bank (0=Bank A, 1=Bank B). The following table illustrates how direct addresses and P-ROC group enable indexes map to the Driver Board addresses and banks:

Driver Board Address / Register Address	**P-ROC Driver Group Enable Index**	**Driver Board Address / Bank**
0 / 0	0	0 / A
0 / 1	1	0 / B
1 / 0	2	1 / A
1 / 1	3	1 / B
2 / 0	4	2 / A
2 / 1	5	2 / B
3 / 0	6	3 / A
3 / 1	7	3 / B
4 / 0	8	4 / A
4 / 1	9	4 / B
5 / 0	10	5 / A
5 / 1	11	5 / B
6 / 0	12	6 / A
6 / 1	13	6 / B
7 / 0	14	7 / A
7 / 1	15	7 / B
x / 0	N/A	x / A
x / 1	N/A	x / B

LEDs:

LED	Meaning
D1	Fused Bank A power
D2	5V
D3	3.3V
D5	Fused Bank B power
D14	Watchdog expired

Dipswitches:

Switch	Meaning*
1	Address bit 0
2	Address bit 1
3	Address bit 2
4	Address bit 3
5	N/A
6	Watchdog disable
7	N/A
8	Terminate serial bus

* On=1, Off=0

Protection:

Fuses

High Power In goes through a fuse in each bank:

Bank A: F3
Bank B: F2

It's recommended that users use the High Power Out connector on bank B (J4) to supply constant power to the devices being controlled with the board. This will help isolate device problems on each bank by hopefully preventing issues on one bank from affect devices on other banks. **Users should make sure to use a fuse with the proper current rating for their application.** If a fuse came installed in the board, it is not guaranteed to be the proper rating for every application.

Watchdog

Each board has a watchdog circuit that will keep the FETs deactivated when the board is not receiving commands from the Master. This could happen due to a failure in the P-ROC or in the Master, or it could be due to a wiring issue in the serial chain. LED D14 lights up when the FETs are deactivated due to the watchdog timer expiring.

Note – This watchdog functionality is disabled when dipswitch 6 is on.

Serial Chain Termination:

The last board in the physical chain (not necessarily the highest address) needs to be set to terminate the serial chain. This is done by setting dipswitch 8 on.

PDB Procotol:

The PDB Protocol describes the format of data being received on the Data input pin (J8: pin-1). This is also the format of the serial data sent out on J10.

Serial Bus Protocol (PDB Protocol)	
Bit	**Field**
Byte 0	{0,0,Board Address[5:0]}
<between bytes>	1-5 IDLE clock cycles
Byte 1	{0,0,0,0,0,Command[2:0]}: 0: Read 1: Write 2: RESERVED 3: RESERVED 4: RESERVED 5: RESERVED 6: RESERVED 7: Clear all registers on board
<between bytes>	1-5 IDLE clock cycles
Byte 2	{0,0,Register Address[5:0]}: 0: Bank A 1: Bank B
<between bytes>	1-5 IDLE clock cycles
Byte 3	{0,0,0,0,Bank data bits[7:4]}
<between bytes>	1-5 IDLE clock cycles
Byte 4	{0,0,0,0,Bank data bits[3:0]}

Each byte is sent MSB first.

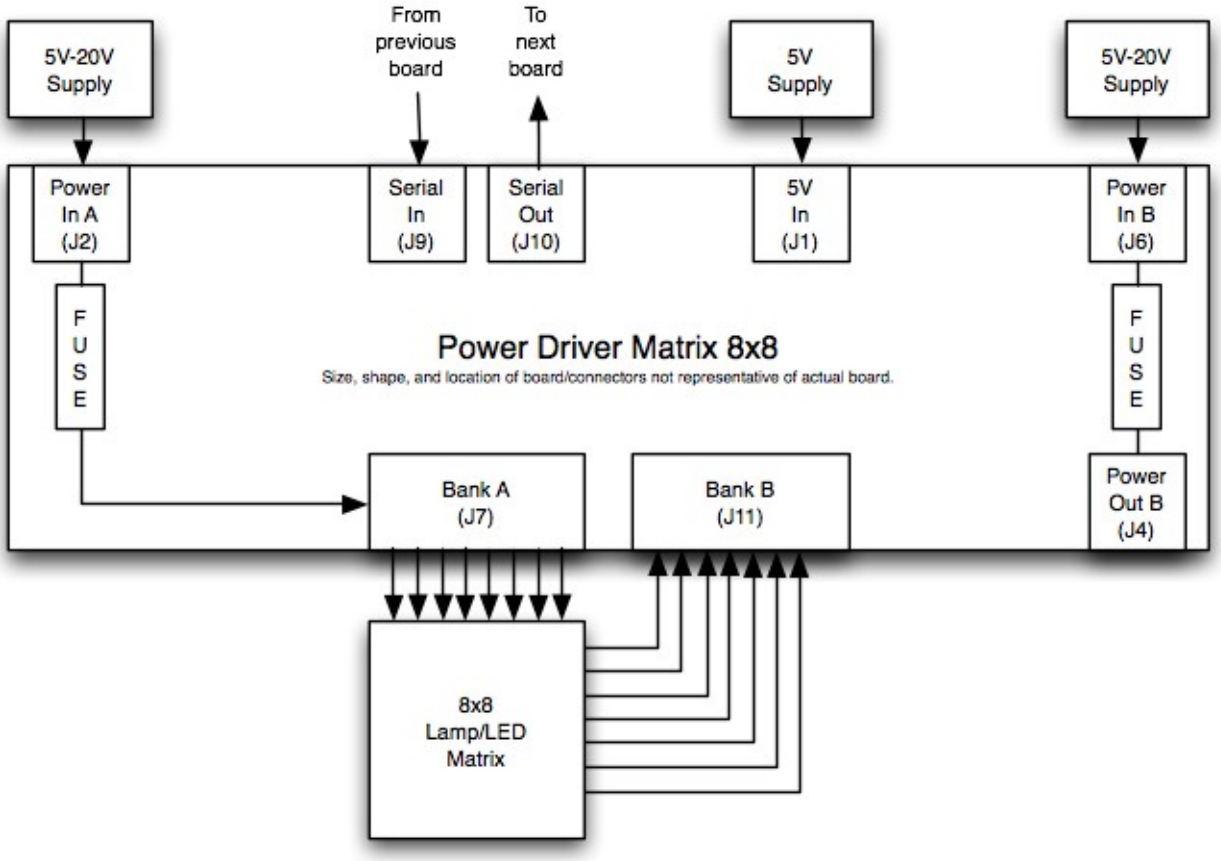
A transaction consists of 5 data bytes. There must be at least 10 IDLE cycles between transactions. Between each byte of a transaction there must be between 1 and 5 IDLE cycles.

The data signal must be high during all IDLE cycles.

Data must be sent at 8 MHz, 125ns per bit.

The Bank data bits in Bytes 3 and 4 are all active high. A '1' will turn the corresponding circuit on, and a '0' will turn the corresponding circuit off.

Example Usage:



Getting Started:

Hardware

- Mount the board using the 4 mounting holes.
- Connect a 5V supply to J1.
- Connect J9 to the previous board in your chain using a 2-wire cable. If the boards are separated by more than a few feet, a shielded & twisted pair is recommended. For short runs, any 2-wire cable should suffice.
- If using Bank A (Source Bank):
  - Connect your power source (5V-20V DC) to J2.
  - Connect your Bank A devices to J7 so the Driver Board can source power to your devices when commanded.
  - Use an appropriately rated fuse for your application in F3.
- If using Bank B (Sink Bank):
  - Connect your power source (5V-80V DC) to J6.
  - Use J4 to supply power to your Bank B devices.
  - Connect your Bank B devices to J11 so the Driver Board can complete the path to ground to activate your devices when commanded.
  - Use an appropriately rated fuse for your application in F2.

Software

- If using a P-ROC:
  - Once configured, the P-ROC can automatically control a chain of Driver Boards. Configure the P-ROC's Output Controller to use active high polarity, and then set up the P-ROC's Driver Groups as appropriate for your application. For sample configurations and help, visit the PinballControllers.com Driver Board forum at http://www.pinballcontrollers.com/forum/index.php?board=16.0 .
  - Alternatively, software can control the Driver Board chain directly through the P-ROC by issuing writes to the P-ROC's Serial Bus Output register. Refer to the P-ROC FPGA Specifications for more details.
- If using a microcontroller:
  - Implement the PDB Protocol described earlier in this document. Sample code for the Arduino microcontroller can be found at: http://www.pinballcontrollers.com/index.php/products/driver-boards/driver-board-faq/83.

PD-16 Spec Sheet

Power Driver 16

Version 1.0 – July 11, 2011

http://www.pinballcontrollers.com

General Description:

The P-ROC Driver Boards are used to control the activation of connected devices by turning on or off power to the devices in response to commands from a P-ROC. The boards receive commands from the P-ROC over an RS-485 serial bus which allows many boards to be chained together and used simultaneously. There are three different types of Driver Boards that can be used to make up a chain: Master, Power Driver 16, and Power Driver Matrix 8x8.

Power Driver 16 Details:

The Power Driver 16 has two banks of 8 n-channel MOSFETs. Each FET is individually controlled and creates a path to ground when activated. Each bank has a power input header on which it can accept DC power up to 80V. The input power goes through a fuse and is used as a reference for the n-channel FETS. The fused power also goes to a convenience power output header which can be used to supply constant power to one side of the external devices.

The other side of the external devices are connected to the FETs via a keyed 9-pin header. When the FETs are activated in response to commands from the P-ROC, the path to ground is completed, and the devices are activated.

These boards are typically used to control pinball machine features such as coils, motors, flashlamps, individual lamps/leds, etc.

All 16 circuits require an active high signal from the controller (P-ROC, Arduino, etc) to turn on and an active low signal to turn off. Logic on the board itself takes care of driving the transistors properly.

Connectors:

J1	Logic Power	Required
2-pin Molex: 0.156” spacing		
1	5V	I
2	Ground	I

J9	Serial Data In	Required
2-pin Molex: 0.100” spacing		
1	Serial+	I
2	Serial-	I

J10	Serial Data Out	Not Required
2-pin Molex: 0.100” spacing		
1	Serial+	O
2	Serial-	O

J5	Bank A High Power In	Required if using Bank A
3-pin Molex: 0.156” spacing		
1	5 to 80V DC	I
2	KEY	N/A
3	Ground	I

J3	Bank A High Power Out	Recommended if using Bank A
3-pin Molex: 0.156” spacing		
1	Fused High Power Out	O
2	Fused High Power Out	O
3	KEY	N/A

J7	Bank A Device Power Inputs	Required if using Bank A
9-pin Molex: 0.156” spacing		
1	Bank A – Data 0	I
2	KEY	N/A

3	Bank A – Data 1	I
4	Bank A – Data 2	I
5	Bank A – Data 3	I
6	Bank A – Data 4	I
7	Bank A – Data 5	I
8	Bank A – Data 6	I
9	Bank A – Data 7	I

J6	**Bank B High Power In**	**Required if using Bank B**
3-pin Molex: 0.156” spacing		
1	5 to 80V DC	I
2	KEY	N/A
3	Ground	I

J4	**Bank B High Power Out**	**Recommended if using Bank B**
3-pin Molex: 0.156” spacing		
1	Fused High Power Out	O
2	Fused High Power Out	O
3	KEY	N/A

J11	**Bank B Device Power Inputs**	**Required if using Bank B**
9-pin Molex: 0.156” spacing		
1	Bank B – Data 0	I
2	Bank B – Data 1	I
3	KEY	N/A
4	Bank B – Data 2	I
5	Bank B – Data 3	I
6	Bank B – Data 4	I
7	Bank B – Data 5	I
8	Bank B – Data 6	I
9	Bank B – Data 7	I

Addressing:

In order to receive the correct data from the P-ROC, each board's address needs to be set appropriately. The following table describes how to use the dipswitches to set the board address:

Dipswitch	Meaning
1	Address bit 0*
2	Address bit 1*
3	Address bit 2*
4	Address bit 3*

*On=1, Off=0

When the P-ROC is configured, groups of 8 data bits are assigned to indexes. Bits 3:1 of those indexes should correspond to the desired Driver Board's address, and bit 0 corresponds to the desired bank (0=Bank A, 1=Bank B). The following table illustrates how direct addresses and P-ROC group enable indexes map to the Driver Board addresses and banks:

Driver Board Address / Register Address	**P-ROC Driver Group Enable Index**	**Driver Board Address / Bank**
0 / 0	0	0 / A
0 / 1	1	0 / B
1 / 0	2	1 / A
1 / 1	3	1 / B
2 / 0	4	2 / A
2 / 1	5	2 / B
3 / 0	6	3 / A
3 / 1	7	3 / B
4 / 0	8	4 / A
4 / 1	9	4 / B
5 / 0	10	5 / A
5 / 1	11	5 / B
6 / 0	12	6 / A
6 / 1	13	6 / B
7 / 0	14	7 / A
7 / 1	15	7 / B
x / 0	N/A	x / A
x / 1	N/A	x / B

LEDs:

LED	Meaning
D2	5V
D3	3.3V
D4	Fused Bank A power
D5	Fused Bank B power
D14	Watchdog expired

Dipswitches:

Switch	Meaning*
1	Address bit 0
2	Address bit 1
3	Address bit 2
4	Address bit 3
5	N/A
6	Watchdog disable
7	N/A
8	Terminate serial bus

* On=1, Off=0

Protection:

Fuses

High Power In goes through a fuse in each bank:

Bank A: F1
Bank B: F2

It's recommended that users use the High Power Out connectors to supply constant power to the devices being controlled with the board. Bank A devices should get power from J3, and bank B devices should get power from J4. This will help isolate device problems on each bank by hopefully preventing issues on one bank from affect devices on other banks. **Users should make sure to use a fuse with the proper current rating for their application.** If a fuse came installed in the board, it is not guaranteed to be the proper rating for every application.

Watchdog

Each board has a watchdog circuit that will keep the FETs deactivated when the board is not receiving commands from the Master. This could happen due to a failure in the P-ROC or in the Master, or it could be due to a wiring issue in the serial chain. LED D14 lights up when the FETs are deactivated due to the watchdog timer expiring.

Note – This watchdog functionality is disabled when dipswitch 6 is on.

Flyback Diodes

Each transistor circuit includes a flyback diode to eliminate voltage spikes on inductive loads, such as coils. It is therefore unnecessary to put diodes on coils activated by this board.

Serial Chain Termination:

The last board in the physical chain (not necessarily the highest address) needs to be set to terminate the serial chain. This is done by setting dipswitch 8 on.

PDB Procotol:

The PDB Protocol describes the format of data being received on the Data input pin (J8: pin-1). This is also the format of the serial data sent out on J10.

Serial Bus Protocol (PDB Protocol)	
Bit	**Field**
Byte 0	{0,0,Board Address[5:0]}
<between bytes>	1-5 IDLE clock cycles
Byte 1	{0,0,0,0,0,Command[2:0]}: 0: Read 1: Write 2: RESERVED 3: RESERVED 4: RESERVED 5: RESERVED 6: RESERVED 7: Clear all registers on board
<between bytes>	1-5 IDLE clock cycles
Byte 2	{0,0,Register Address[5:0]}: 0: Bank A 1: Bank B
<between bytes>	1-5 IDLE clock cycles
Byte 3	{0,0,0,0,Bank data bits[7:4]}
<between bytes>	1-5 IDLE clock cycles
Byte 4	{0,0,0,0,Bank data bits[3:0]}

Each byte is sent MSB first.

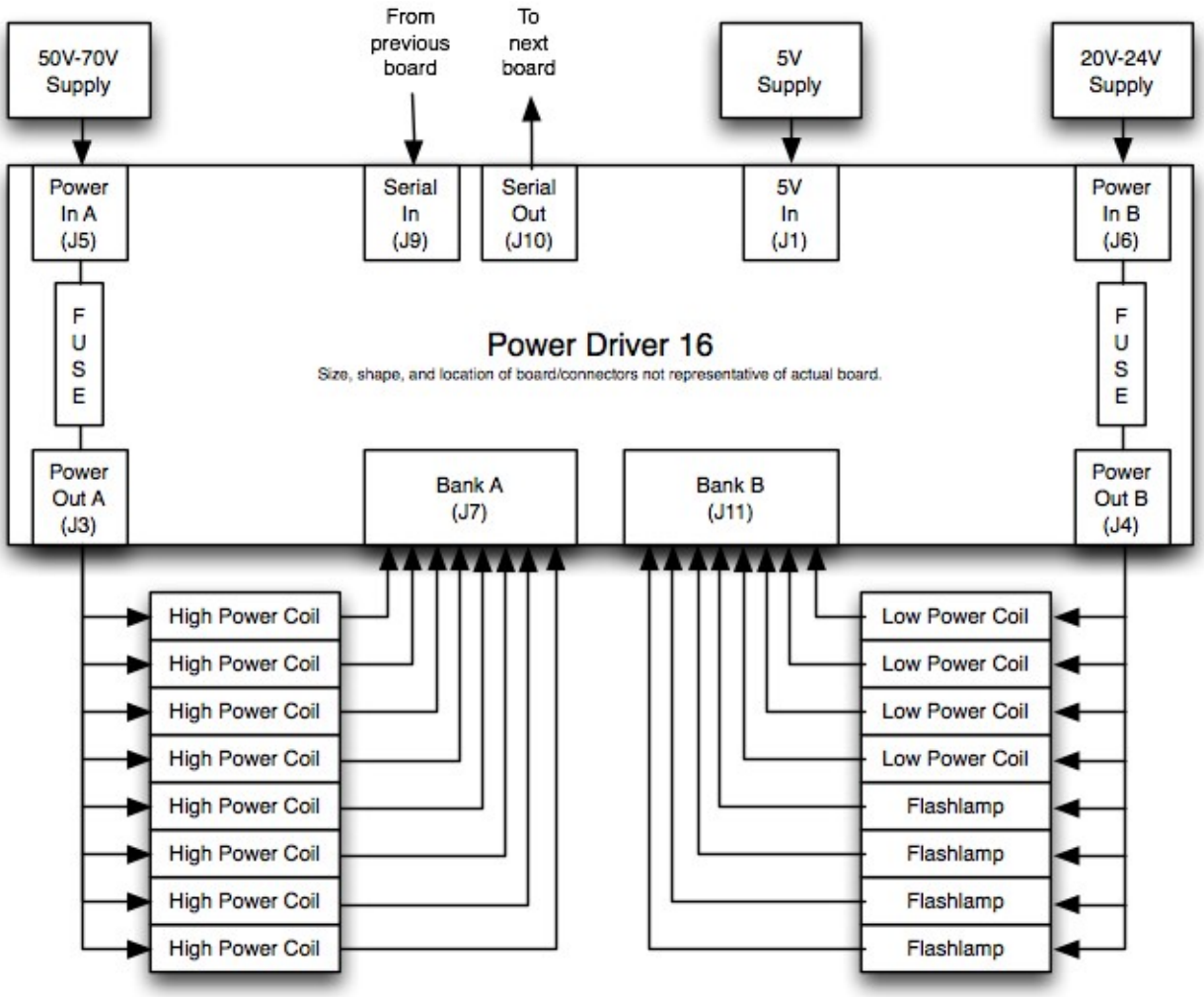
A transaction consists of 5 data bytes. There must be at least 10 IDLE cycles between transactions. Between each byte of a transaction there must be between 1 and 5 IDLE cycles.

The data signal must be high during all IDLE cycles.

Data must be sent at 8 MHz, 125ns per bit.

The Bank data bits in Bytes 3 and 4 are all active high. A '1' will turn the corresponding circuit on, and a '0' will turn the corresponding circuit off.

Example Usage:



Getting Started:

Hardware

- Mount the board using the 4 mounting holes.
- Connect a 5V supply to J1.
- Connect J9 to the previous board in your chain using a 2-wire cable. If the boards are separated by more than a few feet, a shielded & twisted pair is recommended. For short runs, any 2-wire cable should suffice.
- If using Bank A:
  - Connect your power source (5V-80V DC) to J5.
  - Use J3 to supply power to your Bank A devices.
  - Connect your Bank A devices to J7 so the Driver Board can complete the path to ground to activate your devices when commanded.
  - Use an appropriately rated fuse for your application in F1.
- If using Bank B:
  - Connect your power source (5V-80V DC) to J6.
  - Use J4 to supply power to your Bank B devices.
  - Connect your Bank B devices to J11 so the Driver Board can complete the path to ground to activate your devices when commanded.
  - Use an appropriately rated fuse for your application in F2.

Software

- If using a P-ROC:
  - Once configured, the P-ROC can automatically control a chain of Driver Boards. Configure the P-ROC's Output Controller to use active high polarity, and then set up the P-ROC's Driver Groups as appropriate for your application. For sample configurations and help, visit the PinballControllers.com Driver Board forum at http://www.pinballcontrollers.com/forum/index.php?board=16.0 .
  - Alternatively, software can control the Driver Board chain directly through the P-ROC by issuing writes to the P-ROC's Serial Bus Output register. Refer to the P-ROC FPGA Specifications for more details.
- If using a microcontroller:
  - Implement the PDB Protocol described earlier in this document. Sample code for the Arduino microcontroller can be found at: http://www.pinballcontrollers.com/index.php/products/driver-boards/driver-board-faq/83.

