**Semnale control MIPS16 pentru Anexa 5**

*Opcode 000 - tip R tip I tip J*

*Func 000 – xnor Opcode: Opcode:*

*001 – add 001 – lw 111 - jump*

*010 - sub 010 - sw*

*011 – sll 011 - beq*

*100 - srl 100 - bgt*

*101 – and 101 – blt*

*110 - or 110 - addi*

*111 – xor*

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instructiune** | **Opcode** *Instr(15-13)* | **RegDst** | **ExtOp** | **ALUSrc** | **Branch** | **Blt** | **Bgt** | **Jump** | **MemWrite** | **MemtoReg** | **Reg Write** | **func**  *Instr(2-0)* |
| add | 000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 001 |
| sub | 000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 010 |
| sll | 000 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 011 |
| srl | 000 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 100 |
| and | 000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 101 |
| or | 000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 110 |
| xor | 000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 111 |
| xnor | 000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 000 |
| lw | 001 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | --- |
| sw | 010 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | --- |
| beq | 011 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | --- |
| bgt | 100 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | --- |
| blt | 101 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | --- |
| addi | 110 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | --- |
| Jump | 111 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | --- |