

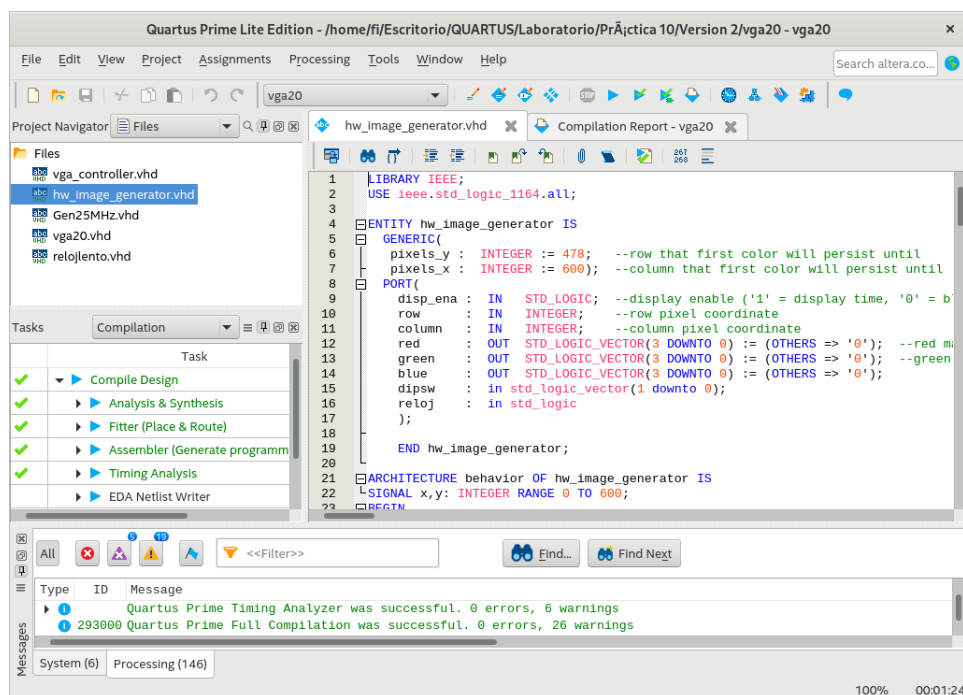
# Laboratorio de Diseño Digital Moderno

## Experimento No. 14 Manejo de VGA

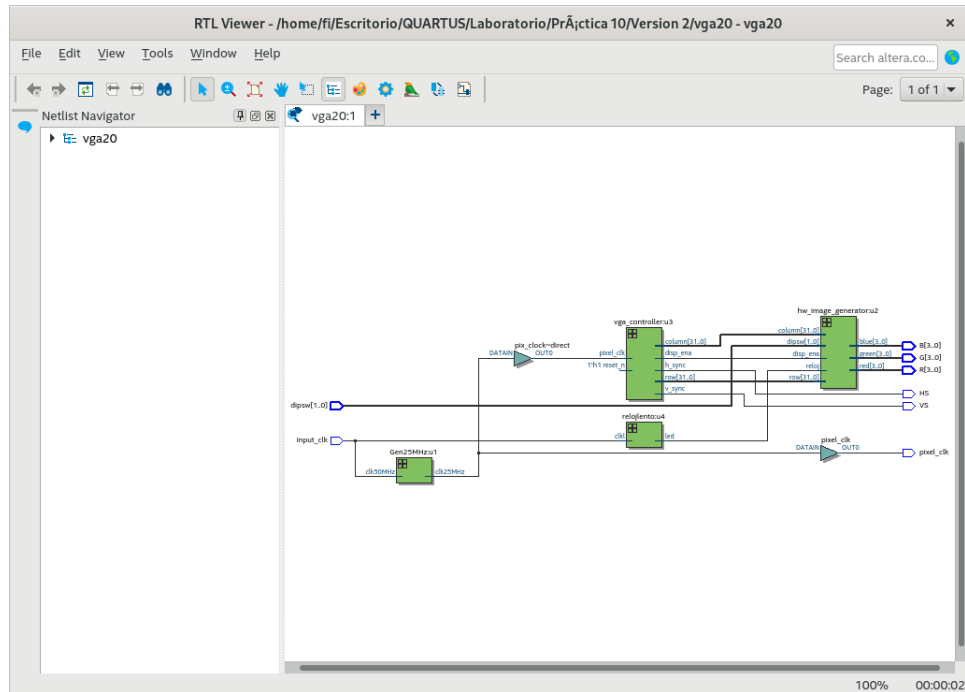
May 23, 2022

## 1 Creación de VGA

### 1.1 Compilación



## 1.2 Diagrama RTL



## 1.3 Asignación de pines

Pin Planner - /home/fi/Escritorio/QUARTUS/Laboratorio/Práctica 10/Version 2/vga20 - vga20

File Edit View Processing Tools Window Help

Groups

Named: \*

Node Name Direction

B[3:0] Output Group

dipsw[1:0] Input Group

Groups Report

Tasks

Early Pin Planning

Early Pin Planning...

Run I/O Assignment Analysis

Top View - Wire Bond

MAX 10 - 10M50DAF484C7G

Pin Legend

Symbol Pin Type

User I/O

User assigned...

Fitter assigne...

Unbonded pad

Reserved pin

Other configu...

DEV\_OE

DEV\_CLR

DIFF\_n

DIFF\_p

Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength
B[3]	Output	PIN_N2	2	B2_NO	PIN_N2	2.5 V	Reserved	12mA (default)
B[2]	Output	PIN_P4	2	B2_NO	PIN_P4	2.5 V	Reserved	12mA (default)
B[1]	Output	PIN_T1	2	B2_NO	PIN_T1	2.5 V	Reserved	12mA (default)
B[0]	Output	PIN_P1	2	B2_NO	PIN_P1	2.5 V	Reserved	12mA (default)
dipsw[1]	Input	PIN_C11	7	B7_NO	PIN_C11	2.5 V	Reserved	12mA (default)
dipsw[0]	Input	PIN_C10	7	B7_NO	PIN_C10	2.5 V	Reserved	12mA (default)
G[3]	Output	PIN_R1	2	B2_NO	PIN_R1	2.5 V	Reserved	12mA (default)
G[2]	Output	PIN_R2	2	B2_NO	PIN_R2	2.5 V	Reserved	12mA (default)
G[1]	Output	PIN_T2	2	B2_NO	PIN_T2	2.5 V	Reserved	12mA (default)
G[0]	Output	PIN_W1	2	B2_NO	PIN_W1	2.5 V	Reserved	12mA (default)
HS	Output	PIN_N3	2	B2_NO	PIN_N3	2.5 V	Reserved	12mA (default)
input_clk	Input	PIN_P11	3	B3_NO	PIN_P11	2.5 V	Reserved	12mA (default)
pixel_clk	Output	PIN_A8	7	B7_NO	PIN_A8	2.5 V	Reserved	12mA (default)
R[3]	Output	PIN_Y1	3	B3_NO	PIN_Y1	2.5 V	Reserved	12mA (default)
R[2]	Output	PIN_Y2	3	B3_NO	PIN_Y2	2.5 V	Reserved	12mA (default)
R[1]	Output	PIN_V1	2	B2_NO	PIN_V1	2.5 V	Reserved	12mA (default)
R[0]	Output	PIN_AA1	3	B3_NO	PIN_AA1	2.5 V	Reserved	12mA (default)

0% 00:00:00

## 1.4 Descarga a tarjeta

