Digital System Design Project 3 – State Minimization

B11030001 葉衍巖

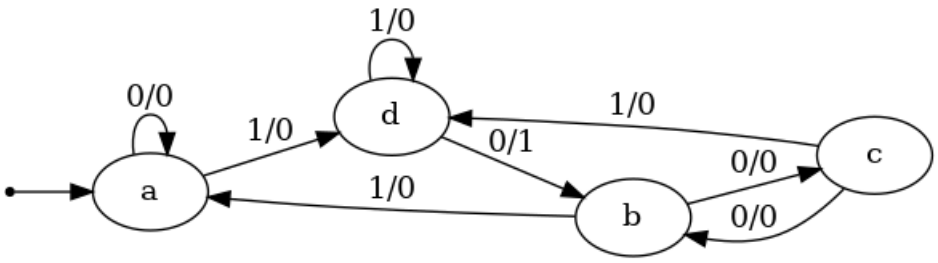
Input kiss content:

```
.start_kiss
.i 1
.o 1
.p 8
.s 4
.r a
0 a a 0
1 a d 0
0 b c 0
1 b a 0
0 c b 0
1 c d 0
0 d b 0
1 d d 0
.end_kiss
```

Output kiss content:

```
.start_kiss
.i 1
.o 1
.p 2
.s 1
.r a
0 a a 0
1 a a 0
.end_kiss
```

Screenshot of STG (before):



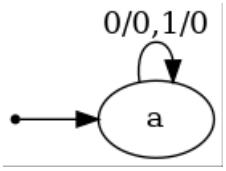
Content:

```
digraph STG{
rankdir=LR;

INIT [shape = point];
a [label="a"];
b [label="b"];
c [label="c"];
d [label="d"];

INIT -> a;
a -> a [label="0/0"];
a -> d [label="1/0"];
b -> c [label="0/0"];
b -> a [label="1/0"];
c -> b [label="0/0"];
c -> d [label="1/0"];
d -> b [label="0/1"];
d -> d [label="1/0"];
}
```

Screenshot of STG (after):



Content:

```
digraph STG{
rankdir=LR;

INIT [shape = point];
a [label="a"];

INIT -> a;
a -> a [label="0/0,1/0"];
}
```