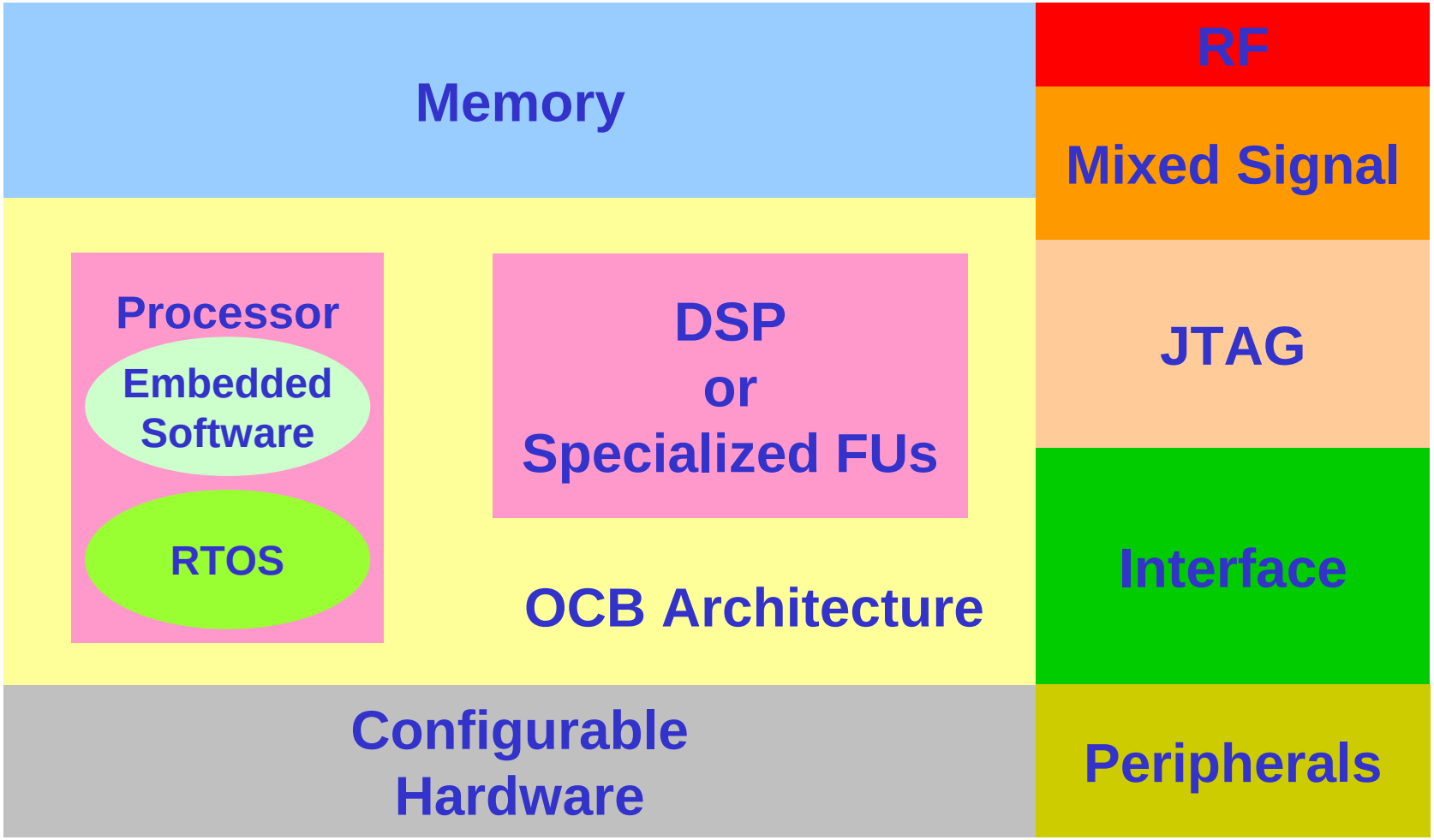
CS2022: 數位系統設計

Digital System Design Flow

Outline

- Toy Design Flow Example
- Digital System Design Flow
- Computer-Aided Design

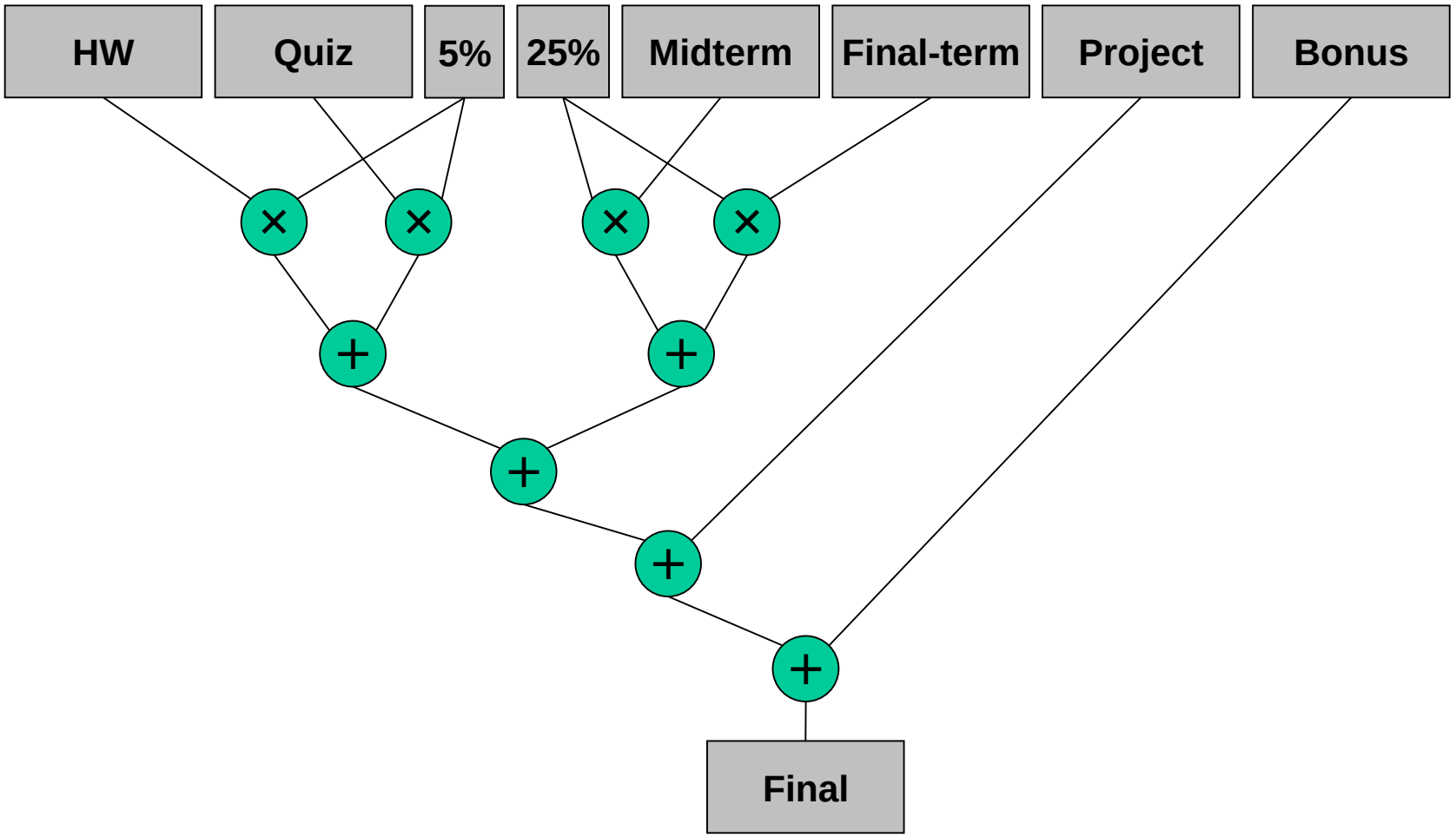
Example of a Complex Digital System



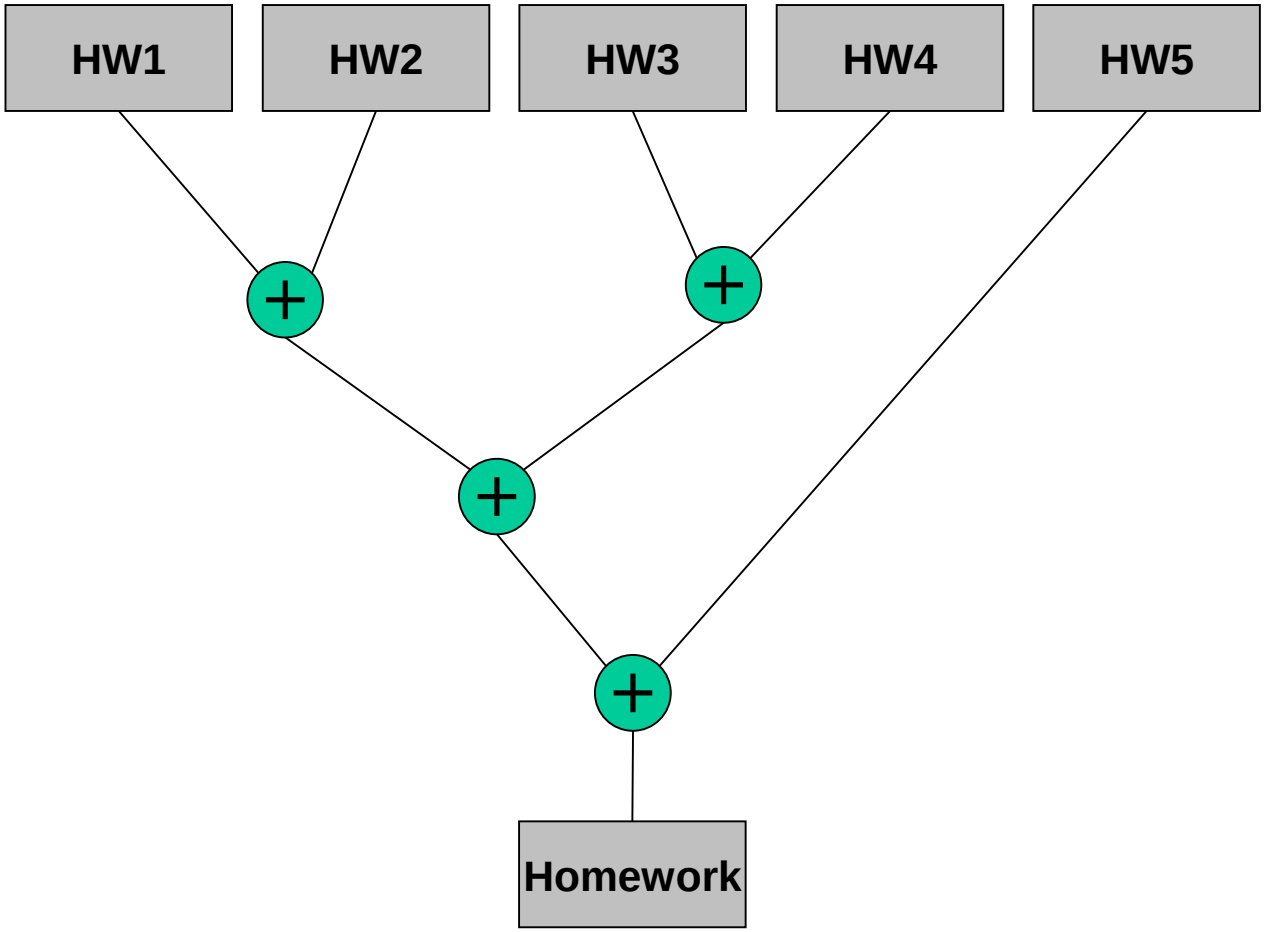
Let's Design a Grading System

- 5 homework assignments (25%)
- 6 in-class quizzes (ignore lowest score) (25%)
- 1 midterm examination (25%)
- 1 final-term examination (25%)
- 1 extra term project
- Some bonus – class participation

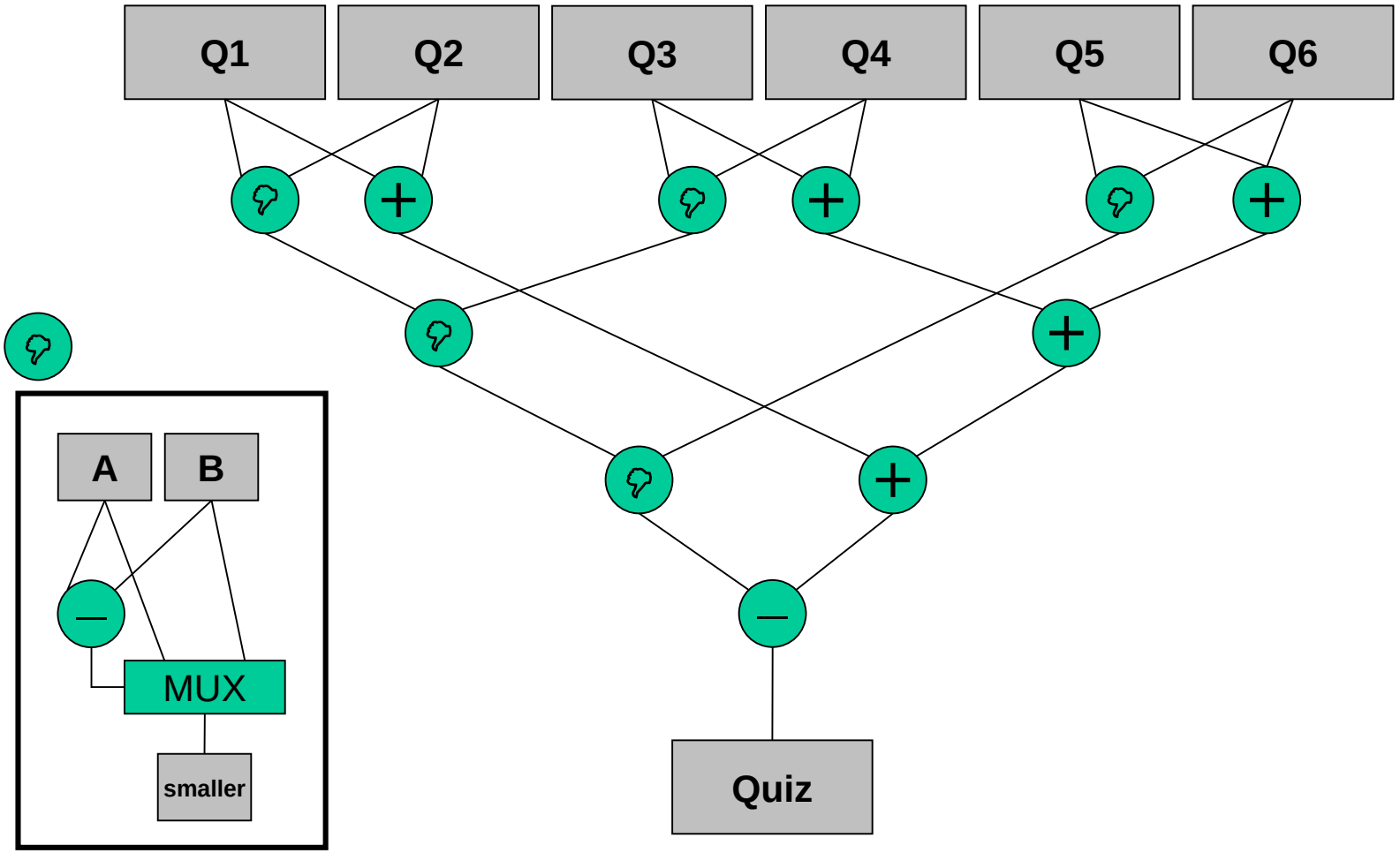
Overall Data Flow Graph (Hierarchical)



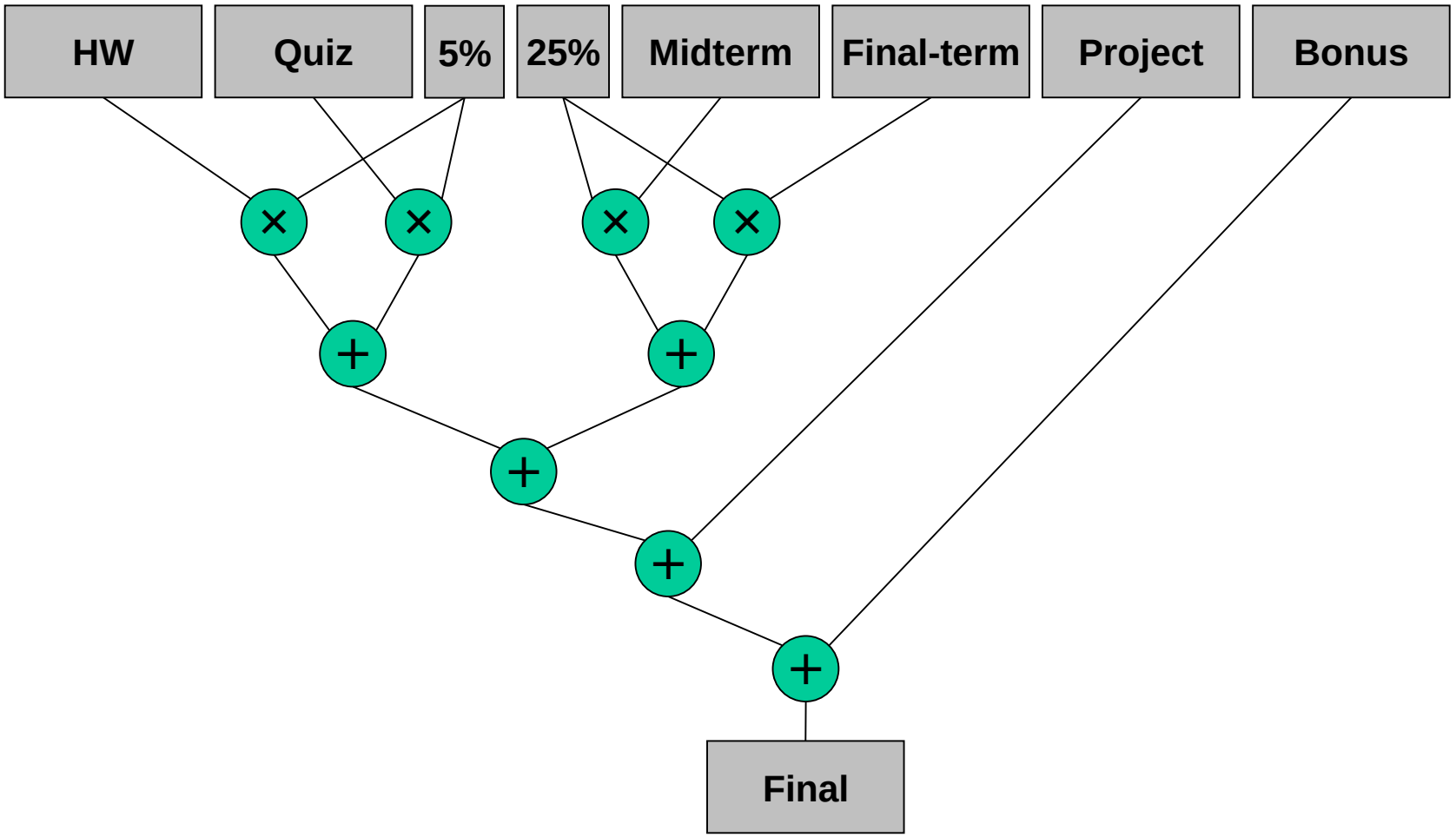
Data Flow Graph: Homework



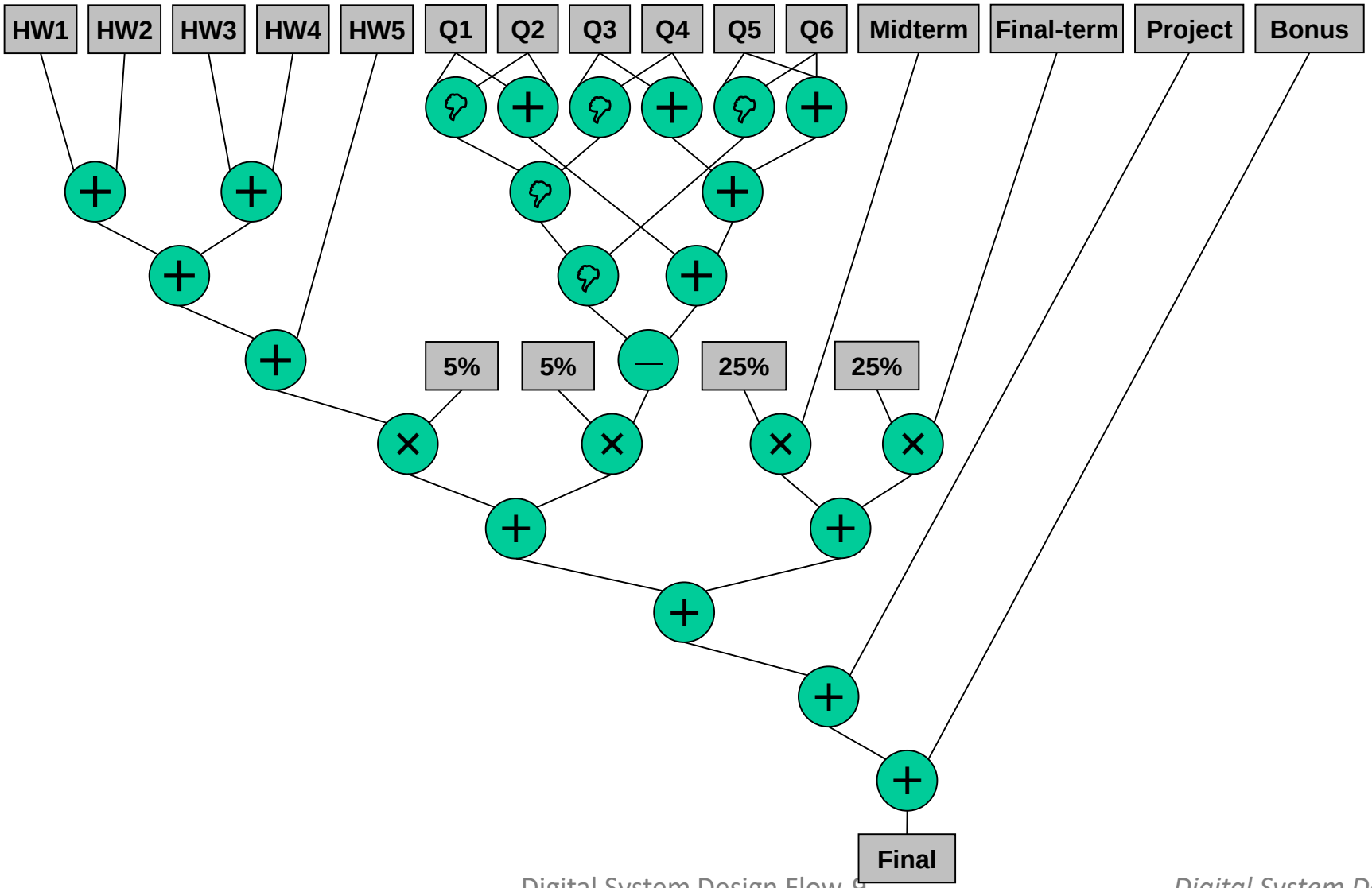
Data Flow Graph: Quiz



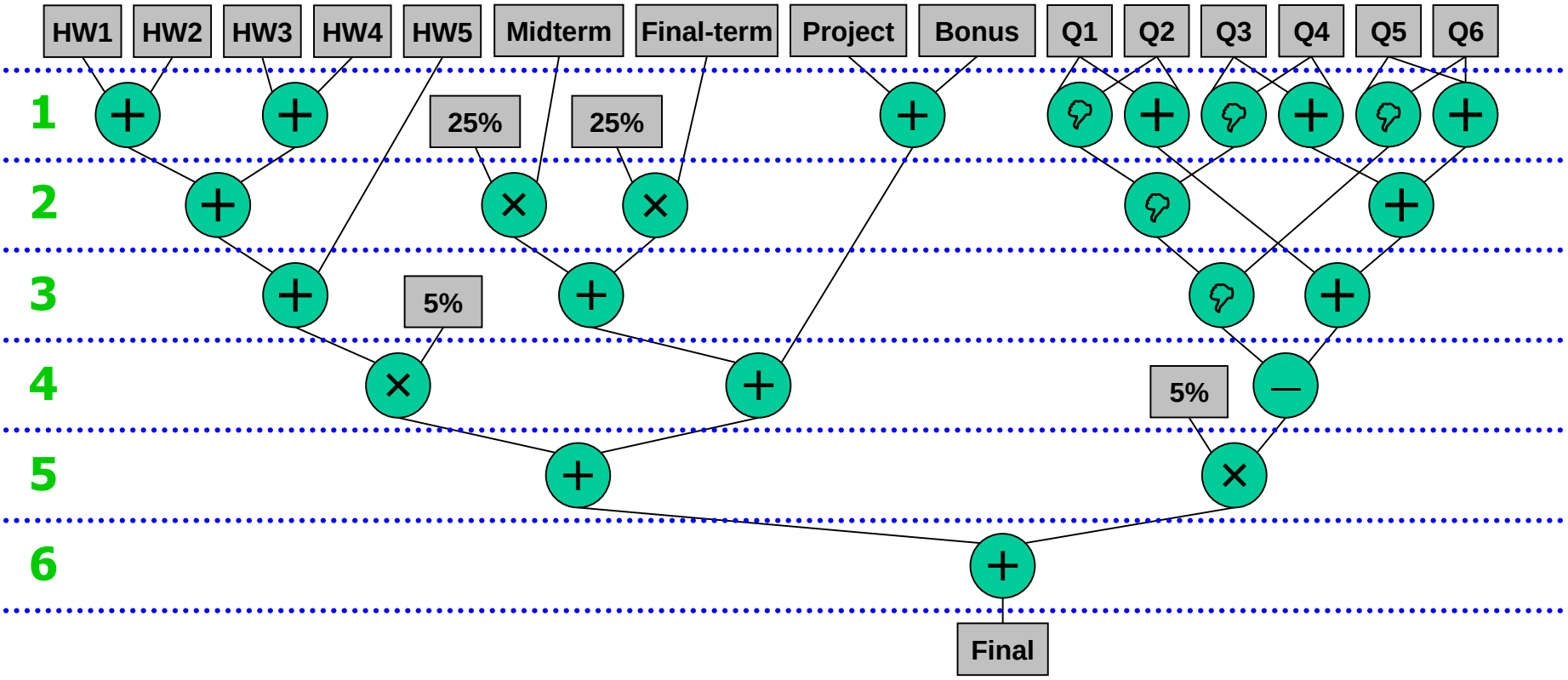
Overall Data Flow Graph (Hierarchical)



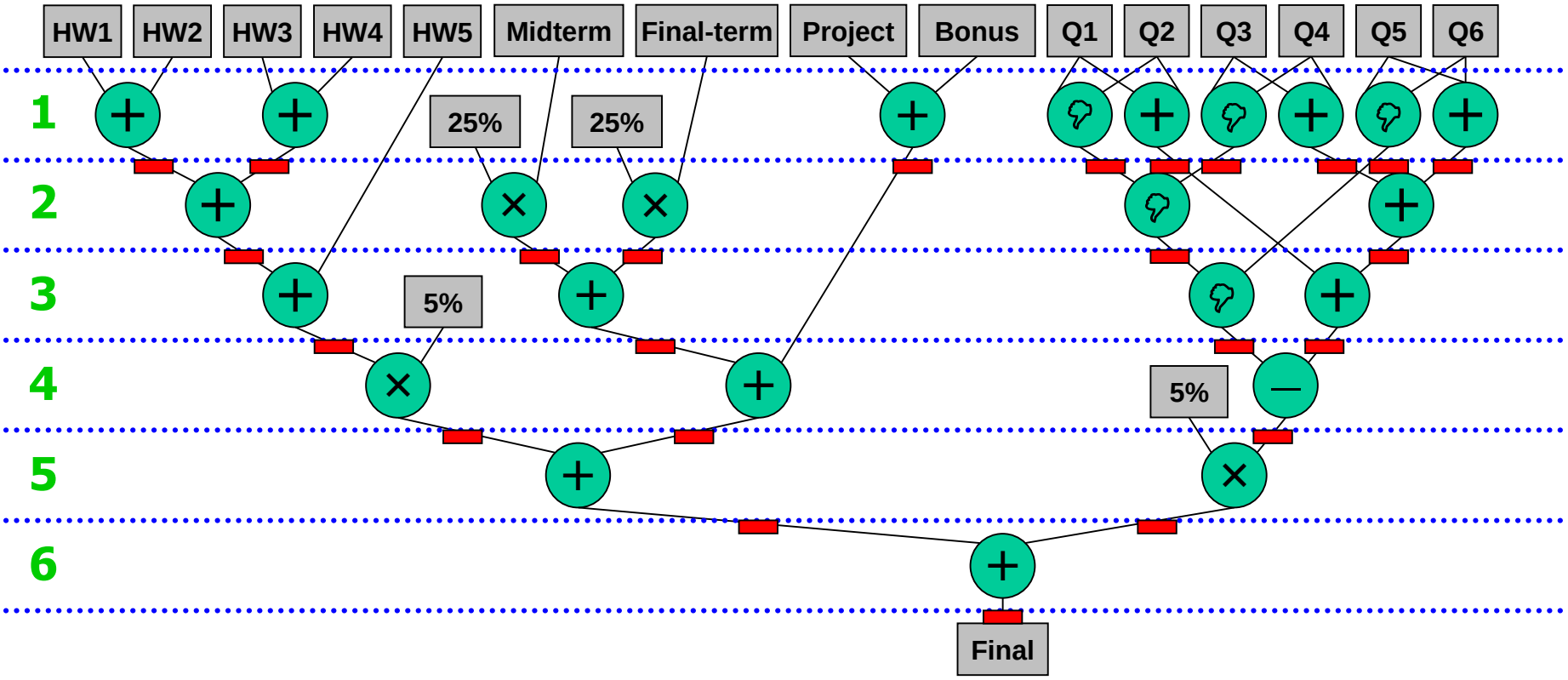
Overall Data Flow Graph (Collapsed)



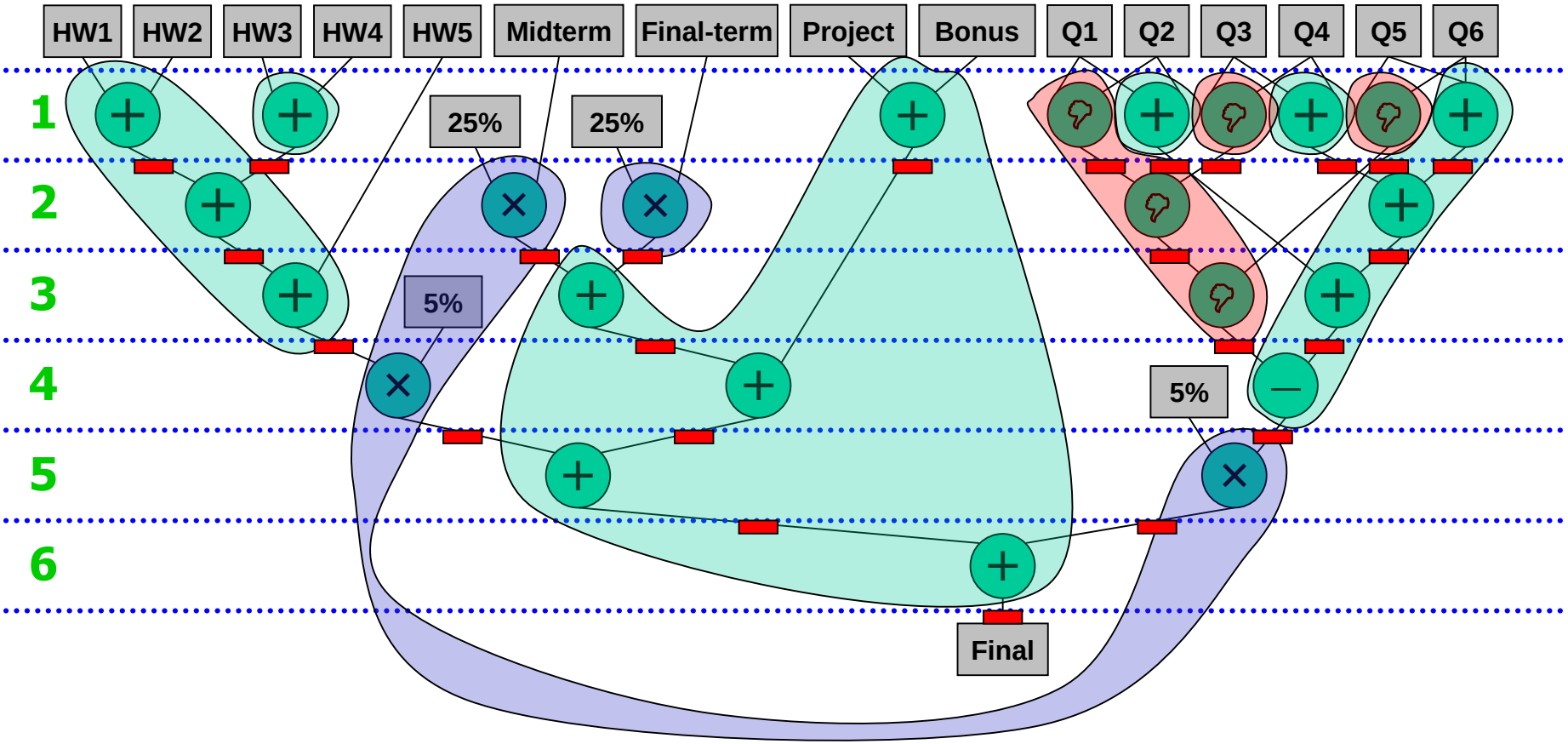
Data Flow with Control Steps



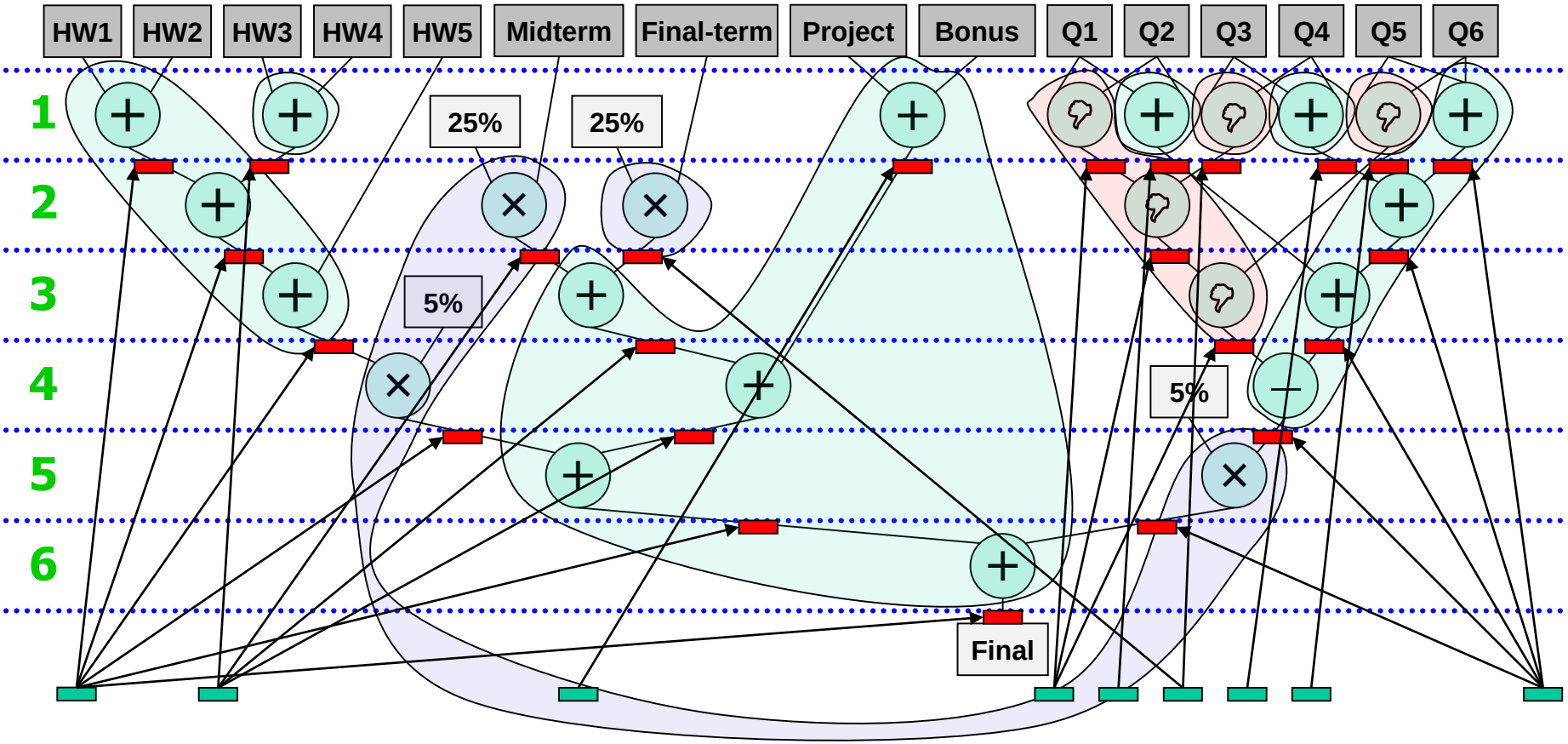
Multi-cycle Implementation



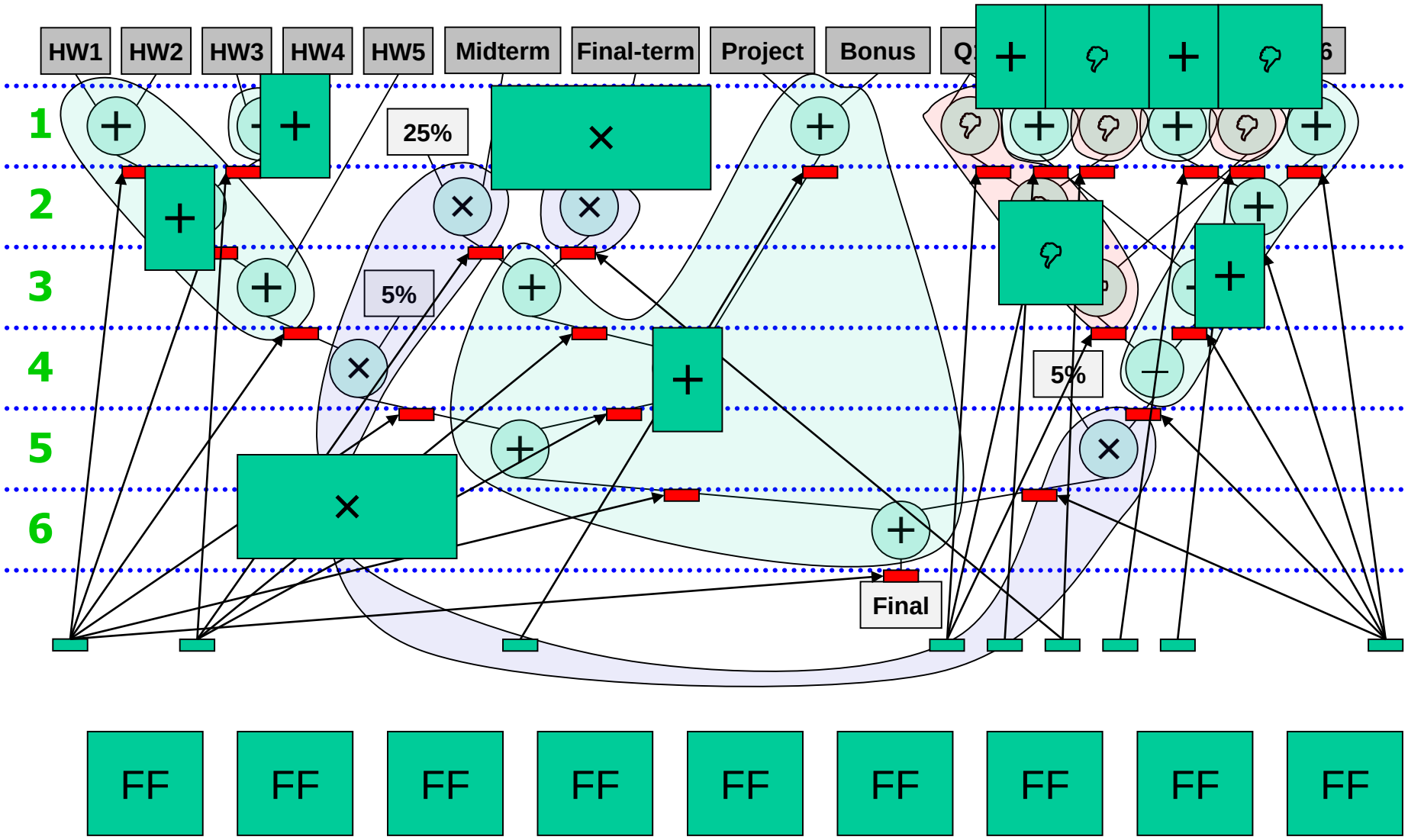
Resource Binding



Register Binding



Resource Allocation



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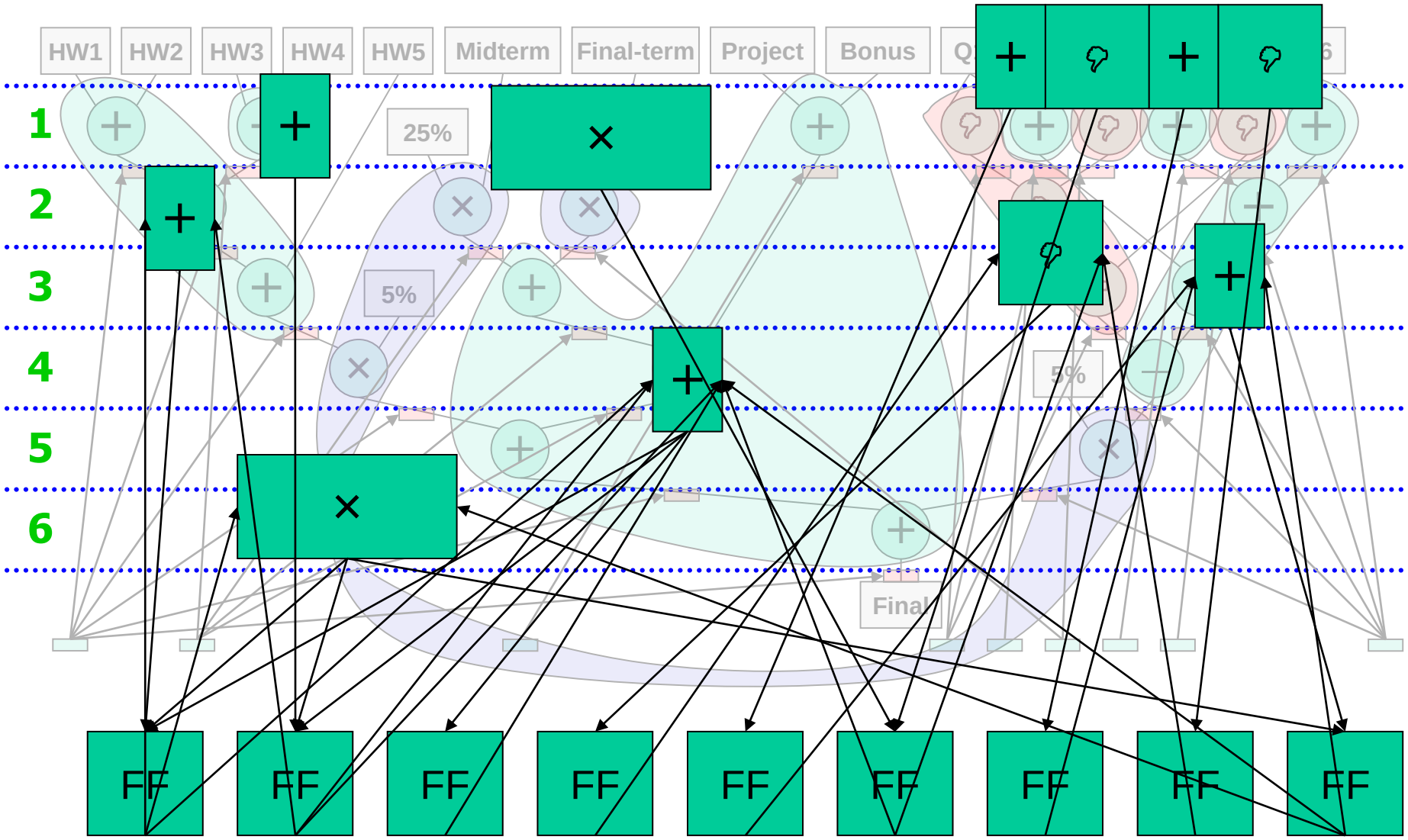
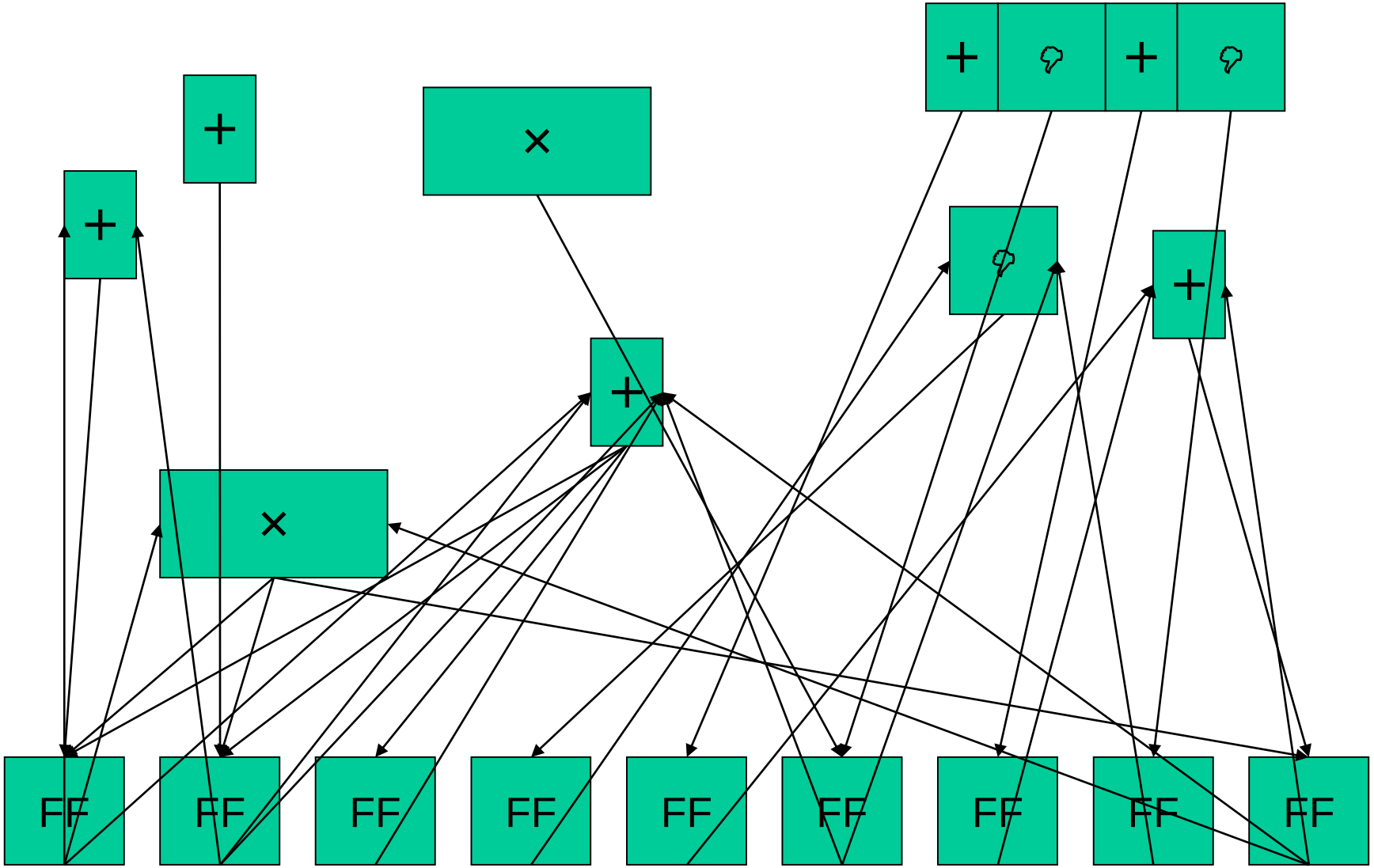
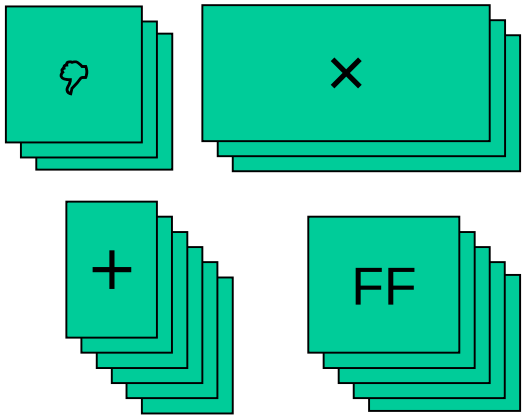


Cell and Module Connectivity



Floorplanning



1-row height

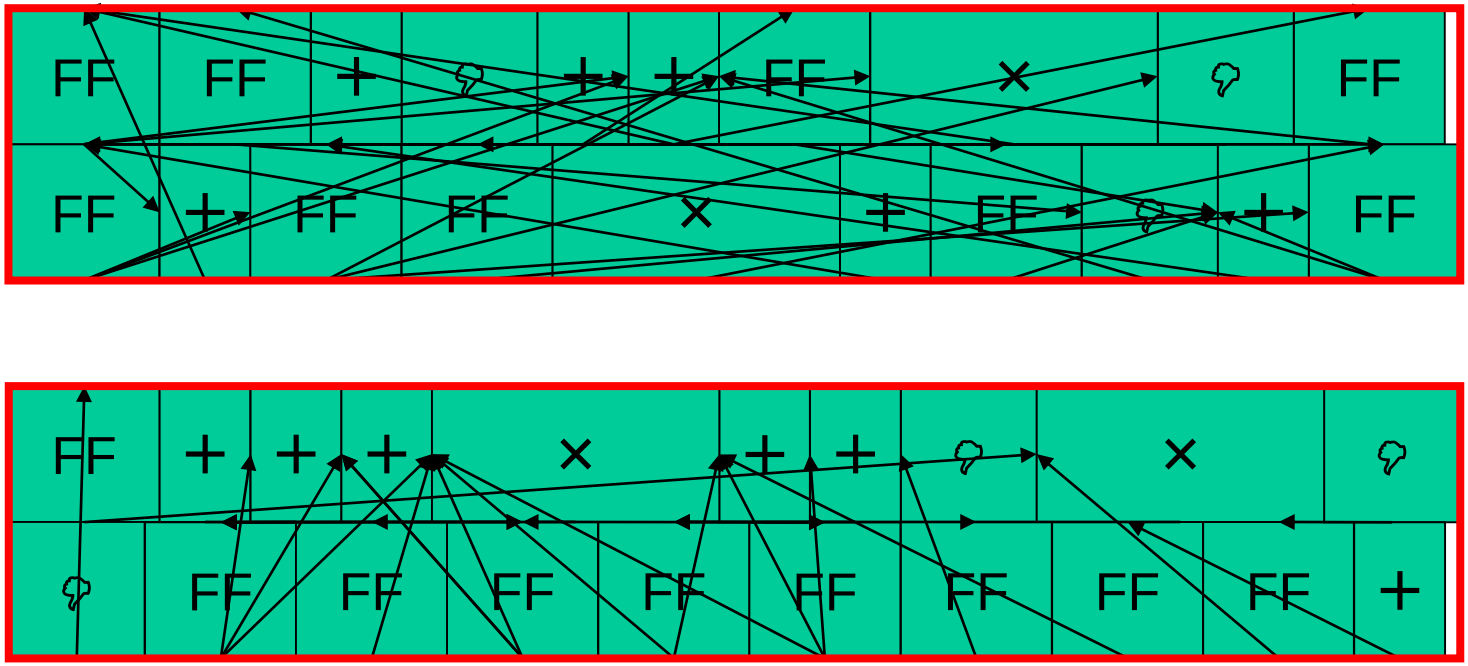
2-row height

3-row height

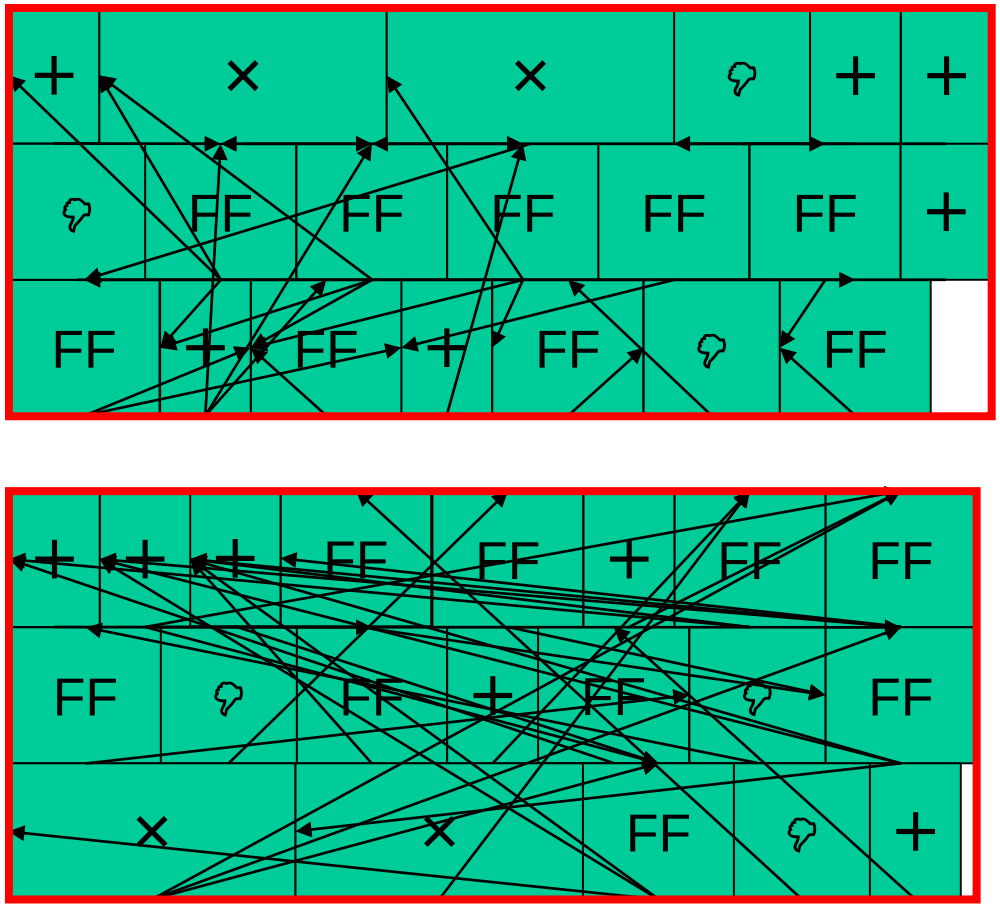
4-row height

5-row height

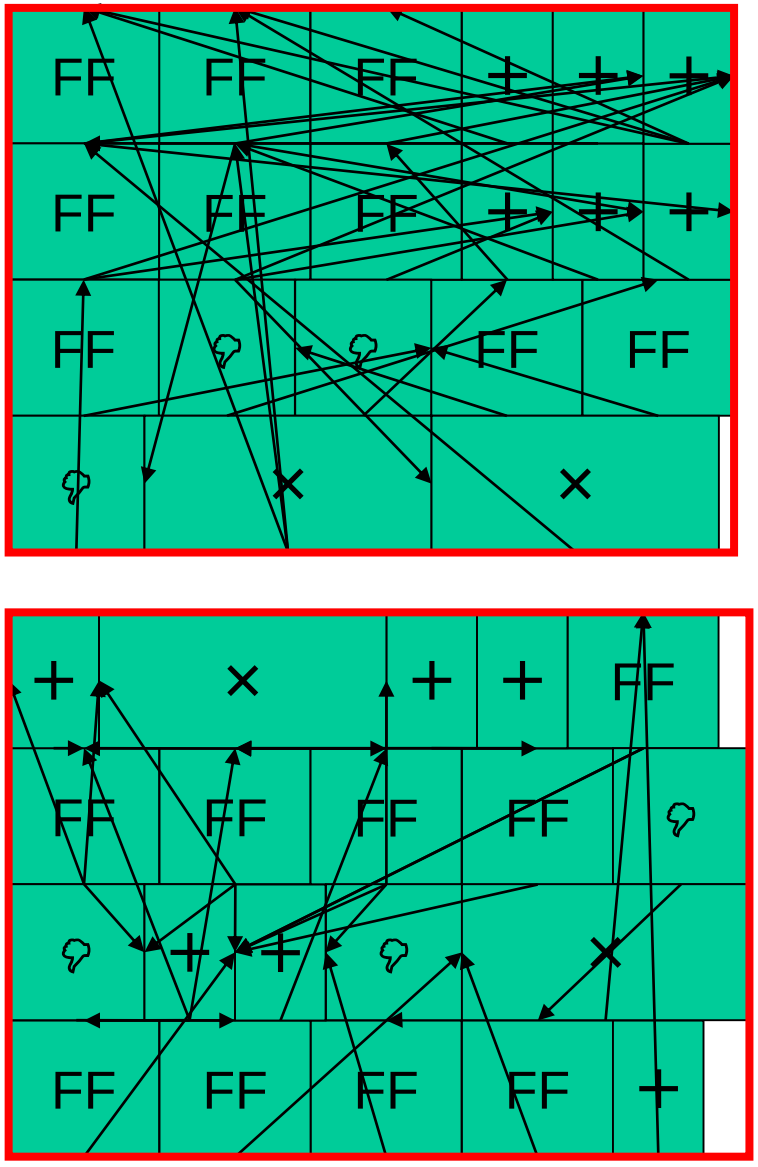
Cell Placement in 2 Rows



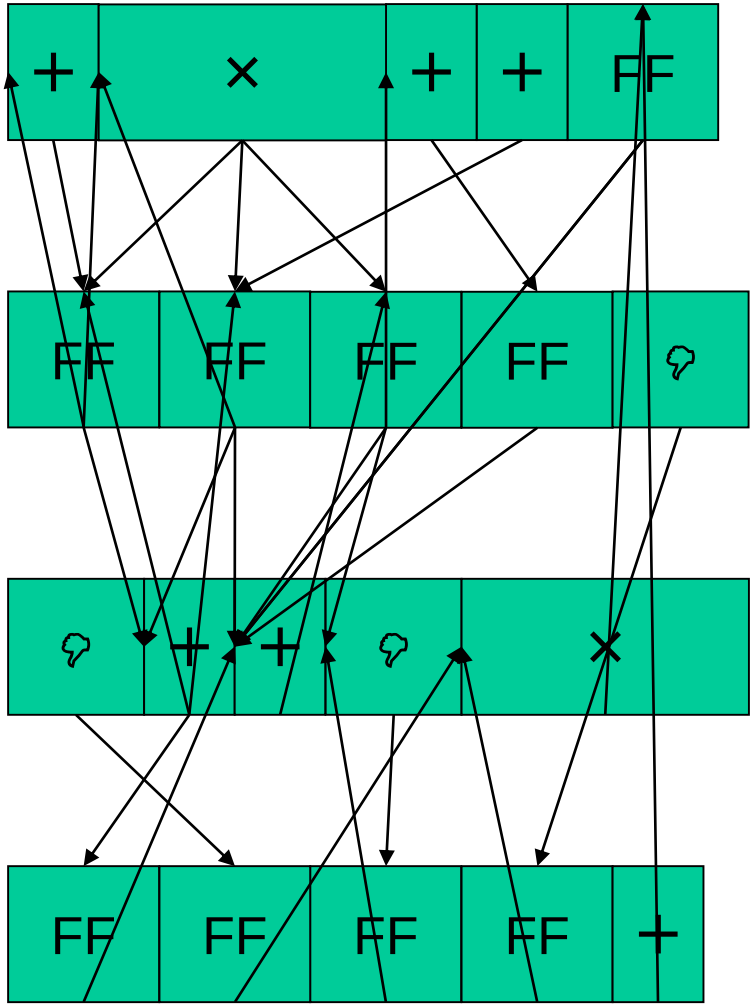
Cell Placement in 3 Rows



Cell Placement in 4 Rows



Routing



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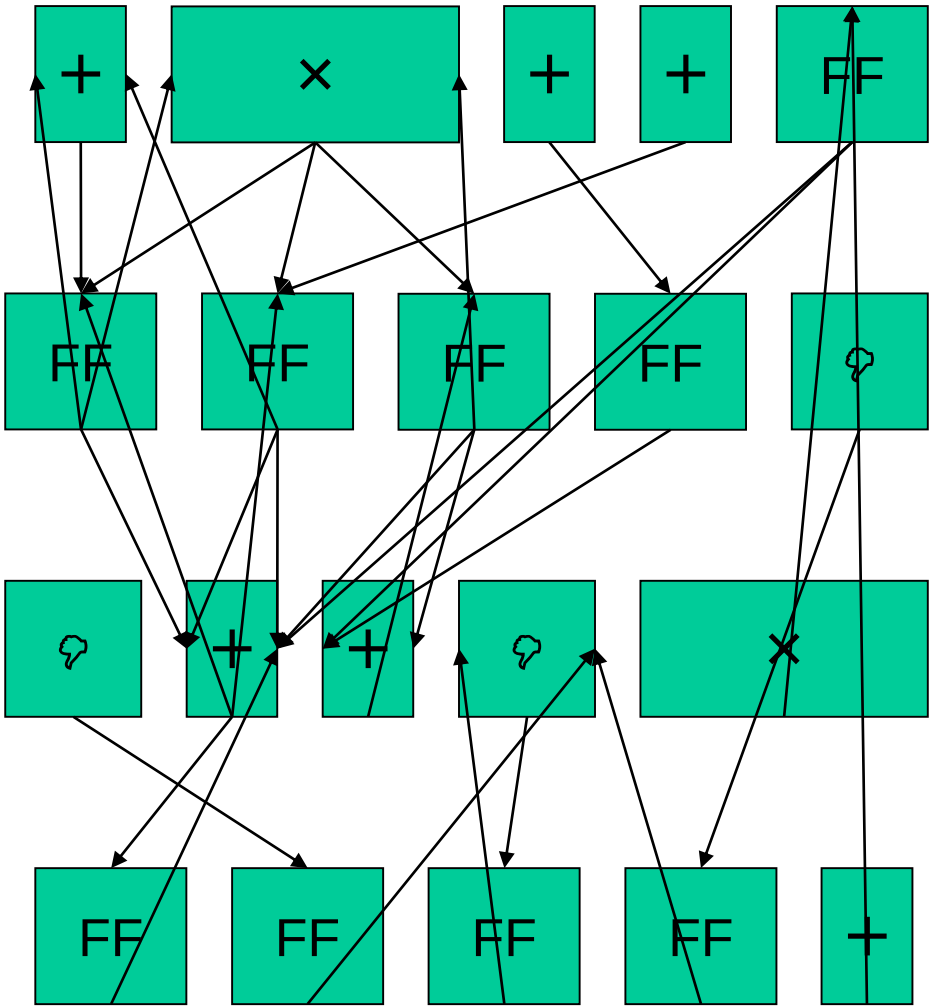
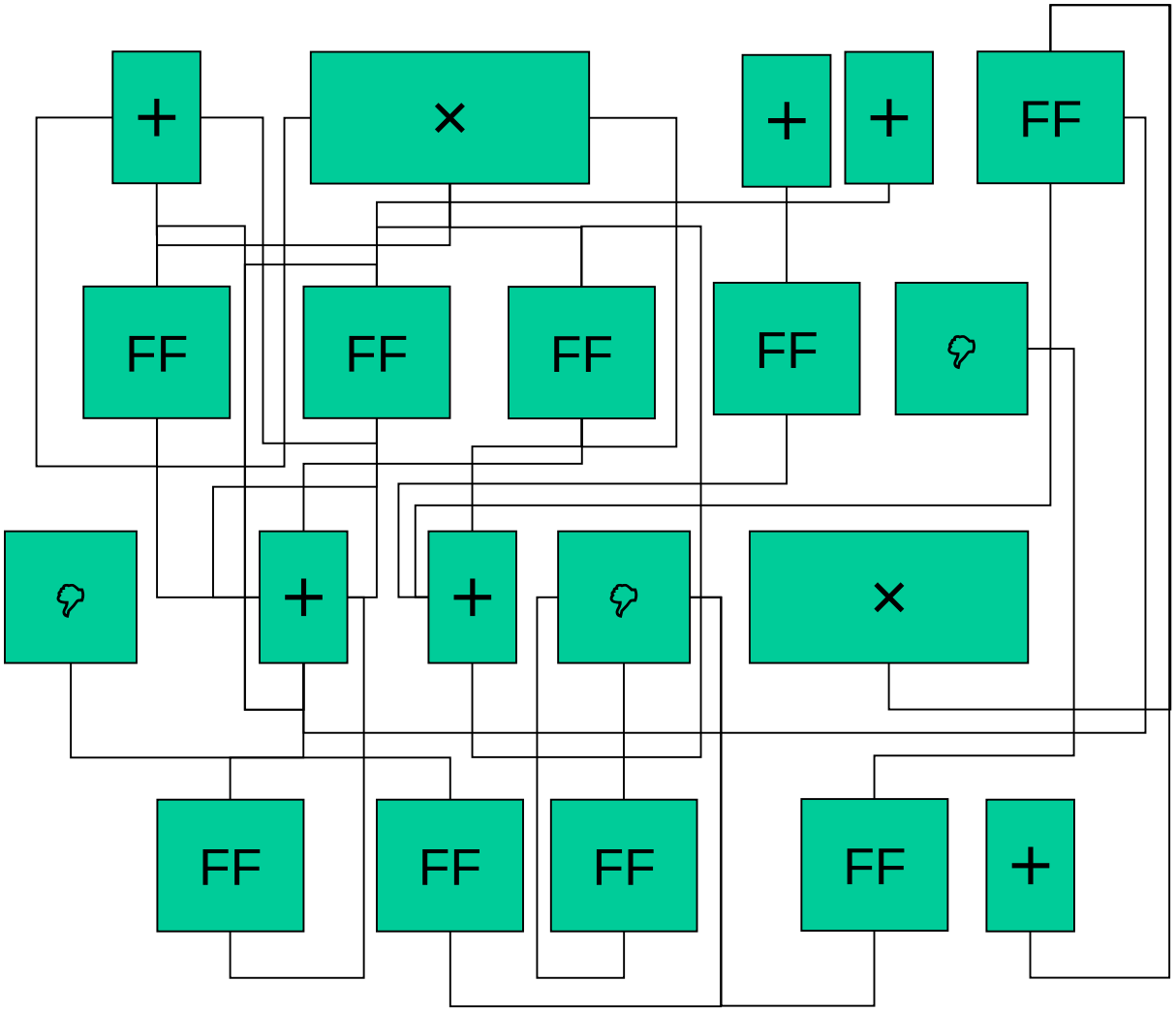
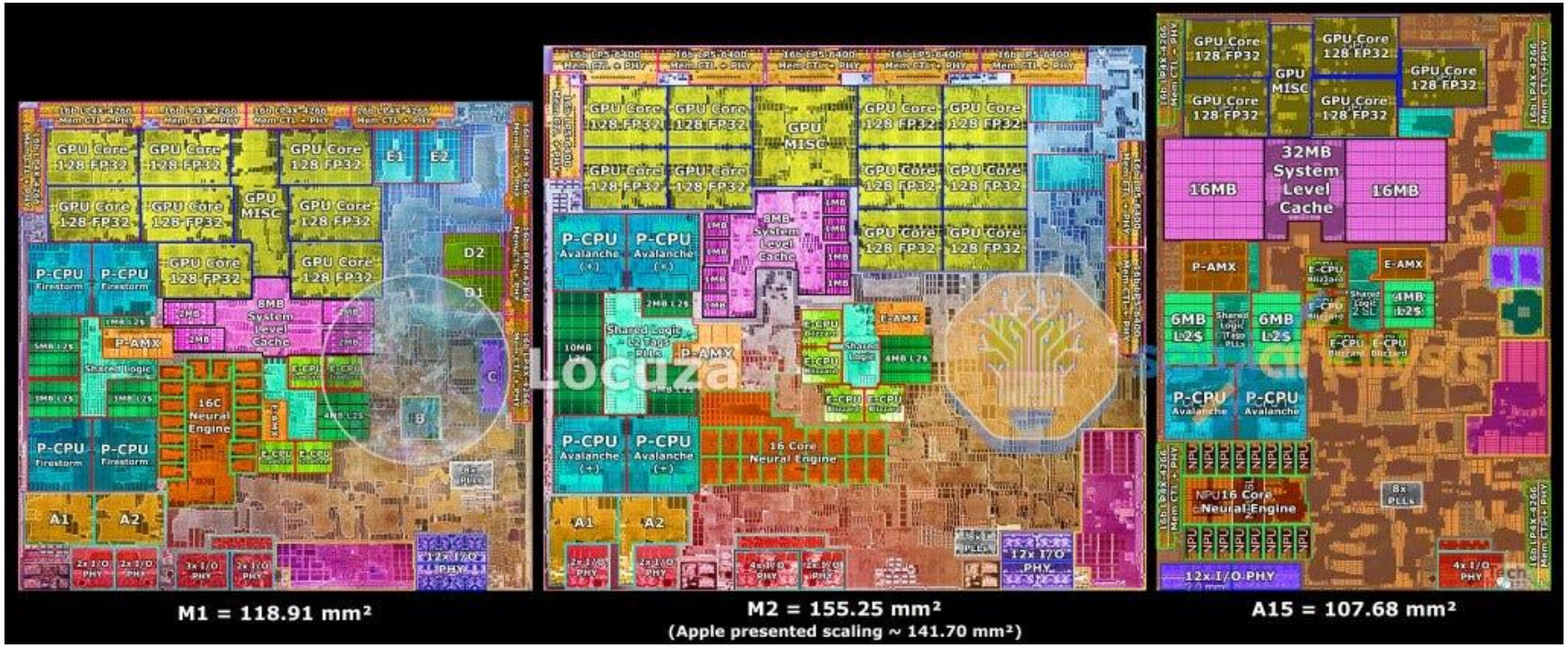


Routing



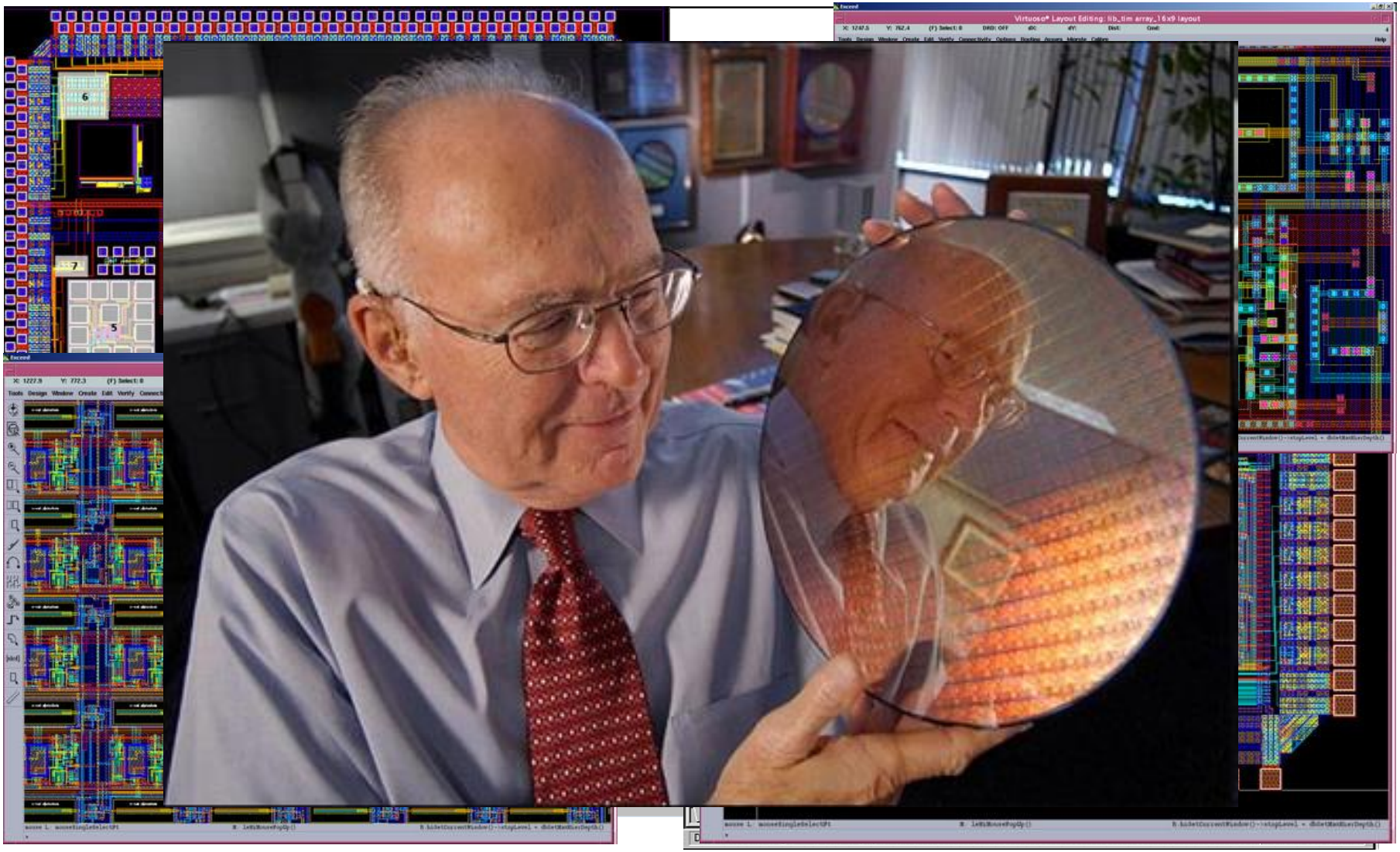
Layout and Spec of Modern Systems

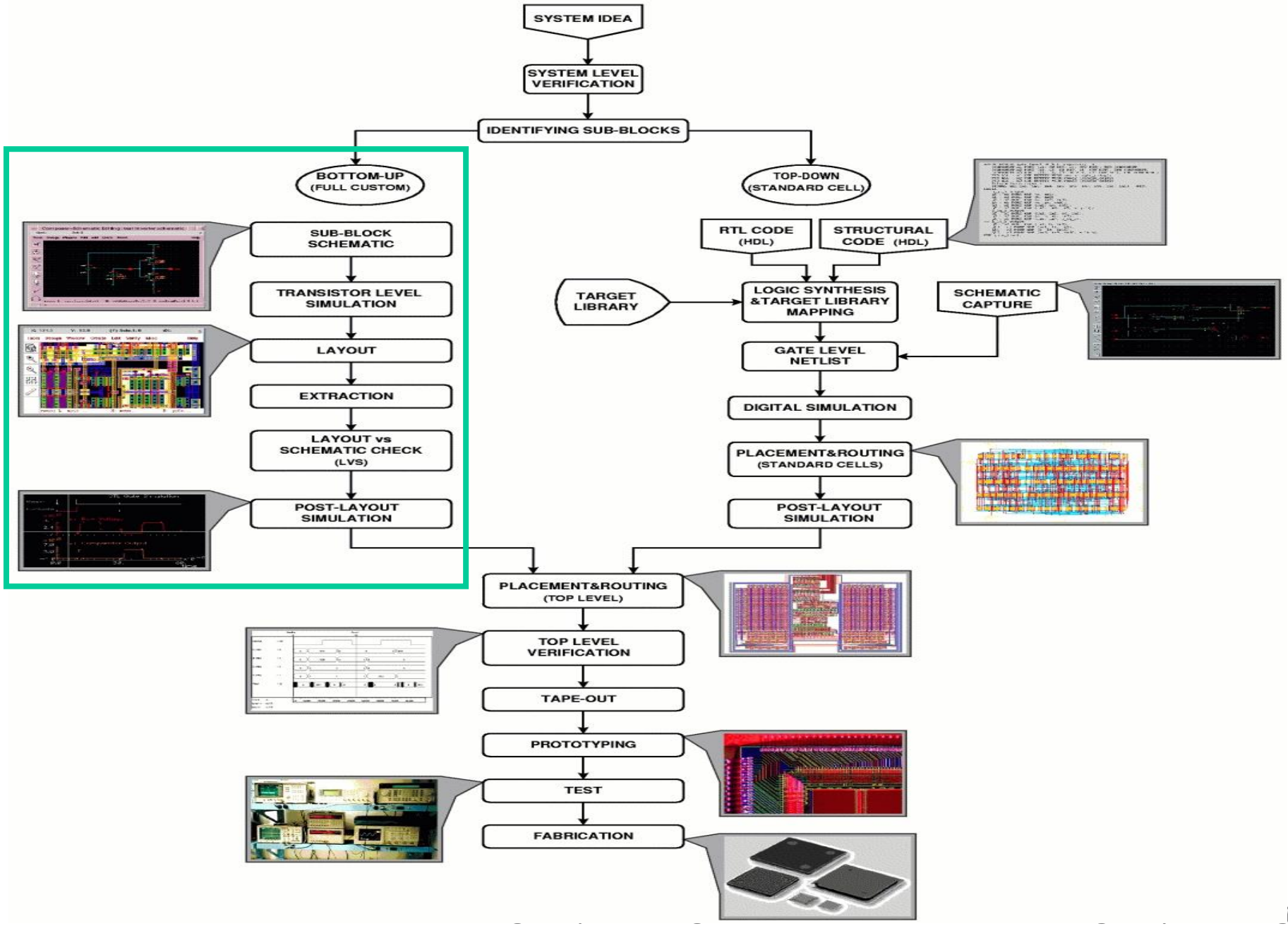


Apple Chips Specs				
Chip	Process Node	Die Size (mm²)	Transistor Count (billions)	Transistor Density (millions/mm²)
A13	N7	94.48	8.5	89.97
A14	N5	88.45	11.8	133.41
A15	N5	107.68	15	139.3
M1	N5	118.91	16	134.56
M2[(1)]	N5	155.25	20	128.82
M2[(2)]	N5	141.7	20	141.14

1. Estimated die size based on scaling identical structures
2. Apple presented die size

CAD for Digital System Design

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SYSTEM LEVEL VERIFICATION
IDENTIFYING SUB-BLOCKS
BOTTOM-UP (FULL CUSTOM)
SUB-BLOCK SCHEMATIC
TRANSISTOR LEVEL SIMULATION
LAYOUT
EXTRACTION
LAYOUT vs SCHEMATIC CHECK (LVS)
POST-LAYOUT SIMULATION
TOP-DOWN (STANDARD CELL)
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STRUCTURAL CODE (HDL)
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GATE LEVEL NETLIST
DIGITAL SIMULATION
PLACEMENT&ROUTING (STANDARD CELLS)
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TAPE-OUT
PROTOTYPING
TEST
FABRICATION

SUB-BLOCK SCHEMATIC

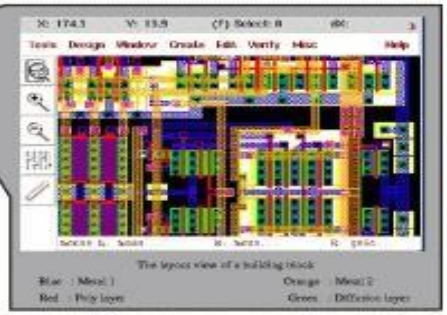
Transistor-level schematic drawings of the circuit blocks are created in Schematic Editor.

TRANSISTOR LEVEL SIMULATION

SPICE(or equivalent) simulation of circuit blocks is used to verify their functionality.

LAYOUT

Mask-layout of all circuit blocks are created in Layout Editor.



EXTRACTION

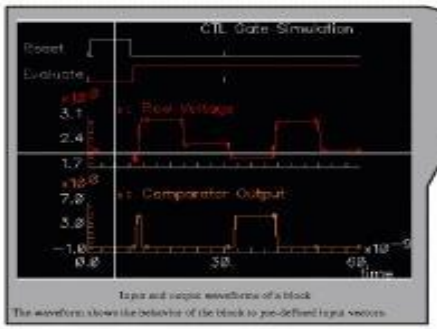
Actual device dimensions and parasitic parameters are determined from mask layout.

LAYOUT vs SCHEMATIC CHECK (LVS)

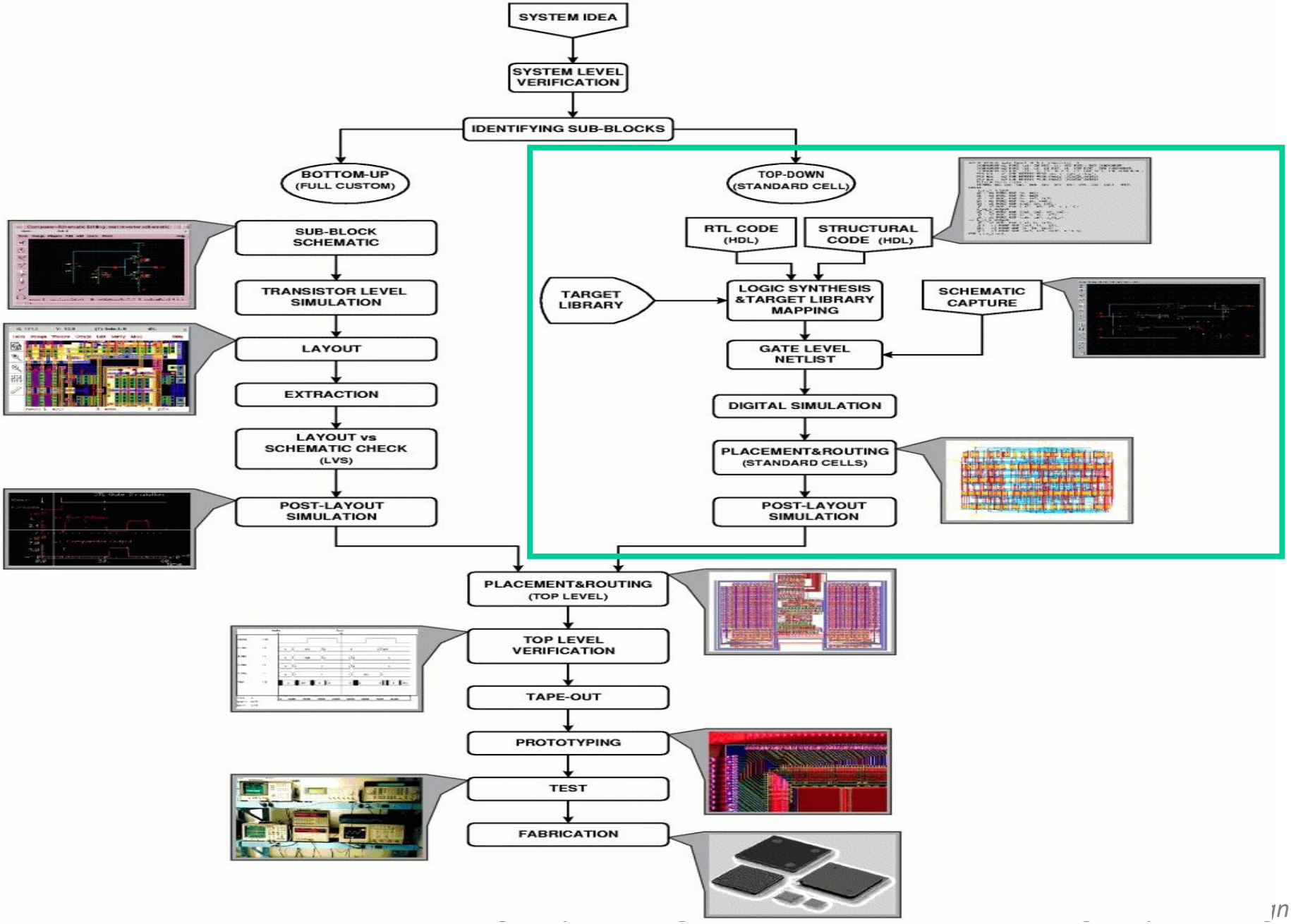
Automatic comparison of mask layout and circuit schematic.

POST-LAYOUT SIMULATION

Final SPICE simulation of the circuit of the circuit blocks using extracted parameters.



gn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```
module adder(x, y, carry, out);
input [31:0] x, y;
output reg carry;
output reg [31:0] out;
always@(*) begin
    {carry,out[31:0]} = x+y;
end
endmodule
```

RTL CODE (HDL)

Register-transfer level code to describe logic functionality.

STRUCTURAL CODE (HDL)

Detailed code to describe gate-level structure.

TARGET LIBRARY

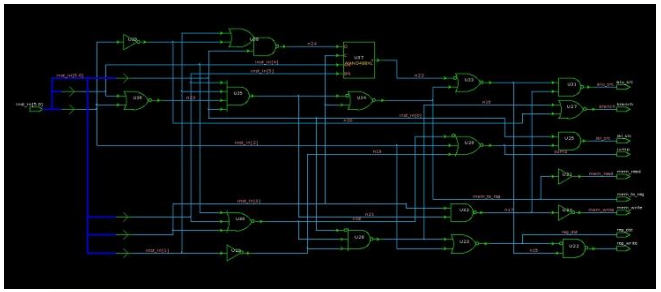
Available cells and functions.

LOGIC SYNTHESIS & TARGET LIBRARY MAPPING

Generate gate-level description using target library cells.

SCHEMATIC CAPTURE

Alternative to HDL code.



GATE LEVEL NETLIST

DIGITAL SIMULATION

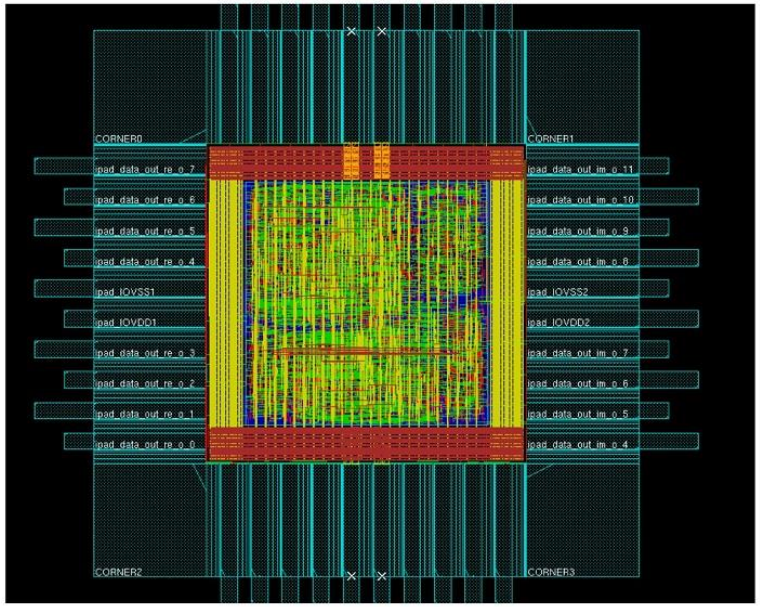
Verify the logic functionality of the circuit.

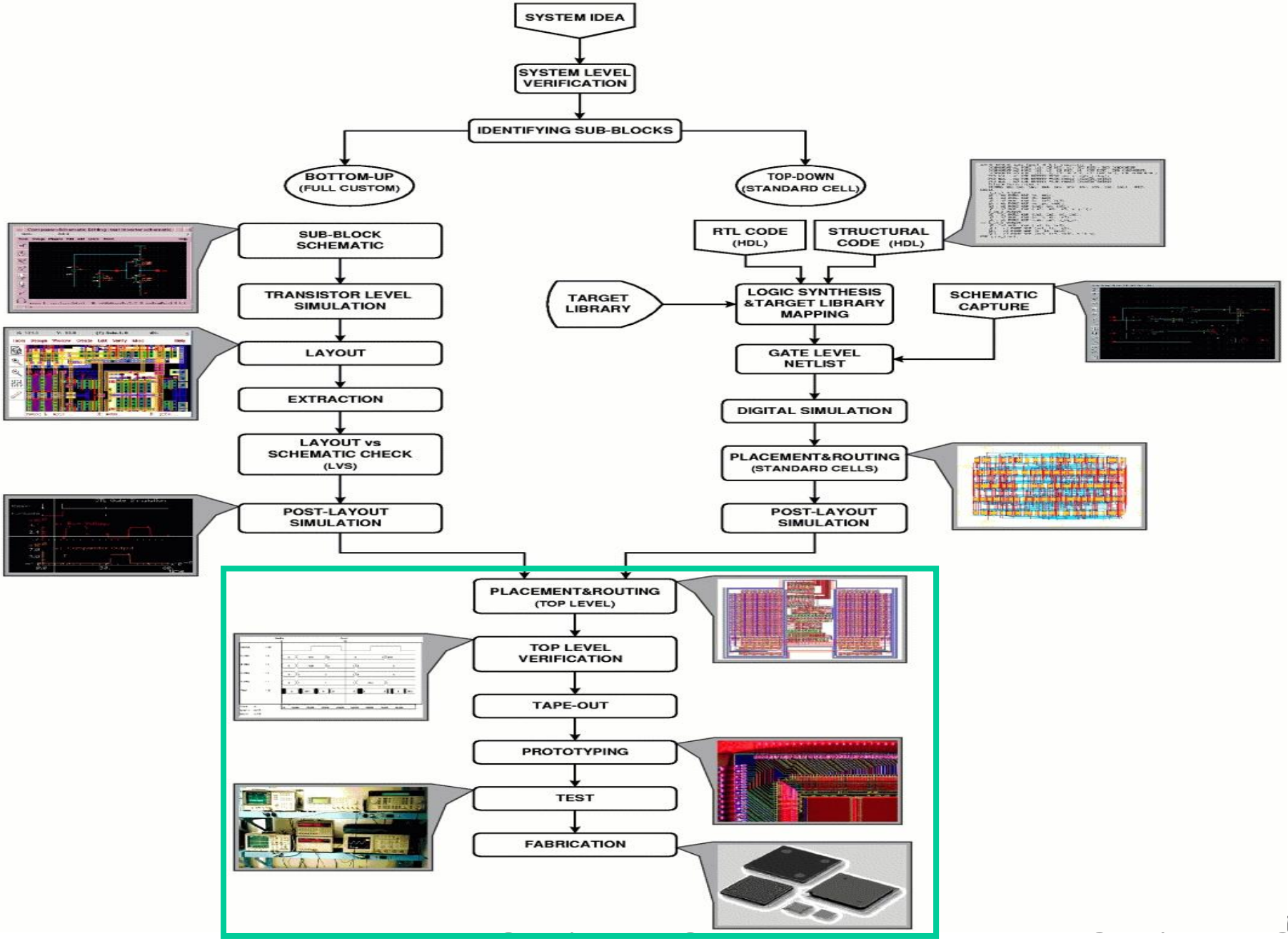
PLACEMENT&ROUTING (STANDARD CELLS)

Create the circuit layout using an automatic placement and routing tool.

POST-LAYOUT SIMULATION

Final logic simulation to verify actual delays and circuit performance.

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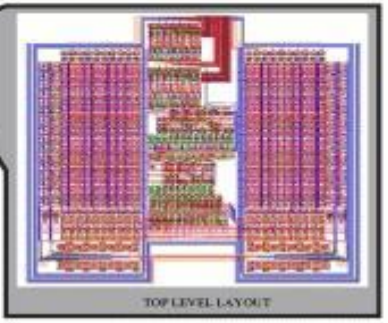
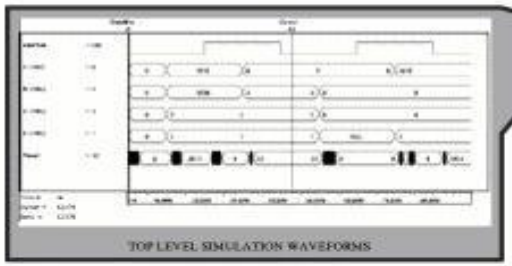
PLACEMENT&ROUTING (TOP LEVEL)

Mask level layout of the entire chip



TOP LEVEL VERIFICATION

Simulation (mixed-mode) to verify functionality and performance of the entire chip.

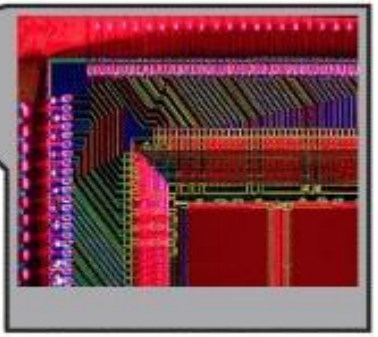


TAPE-OUT

Create universal format file to describe mask layers to manufacturer.

PROTOTYPING

Sample chips manufactured in fab.

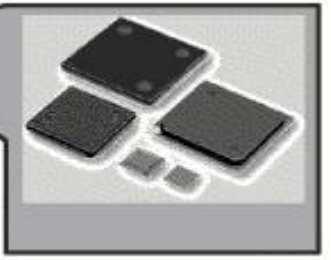


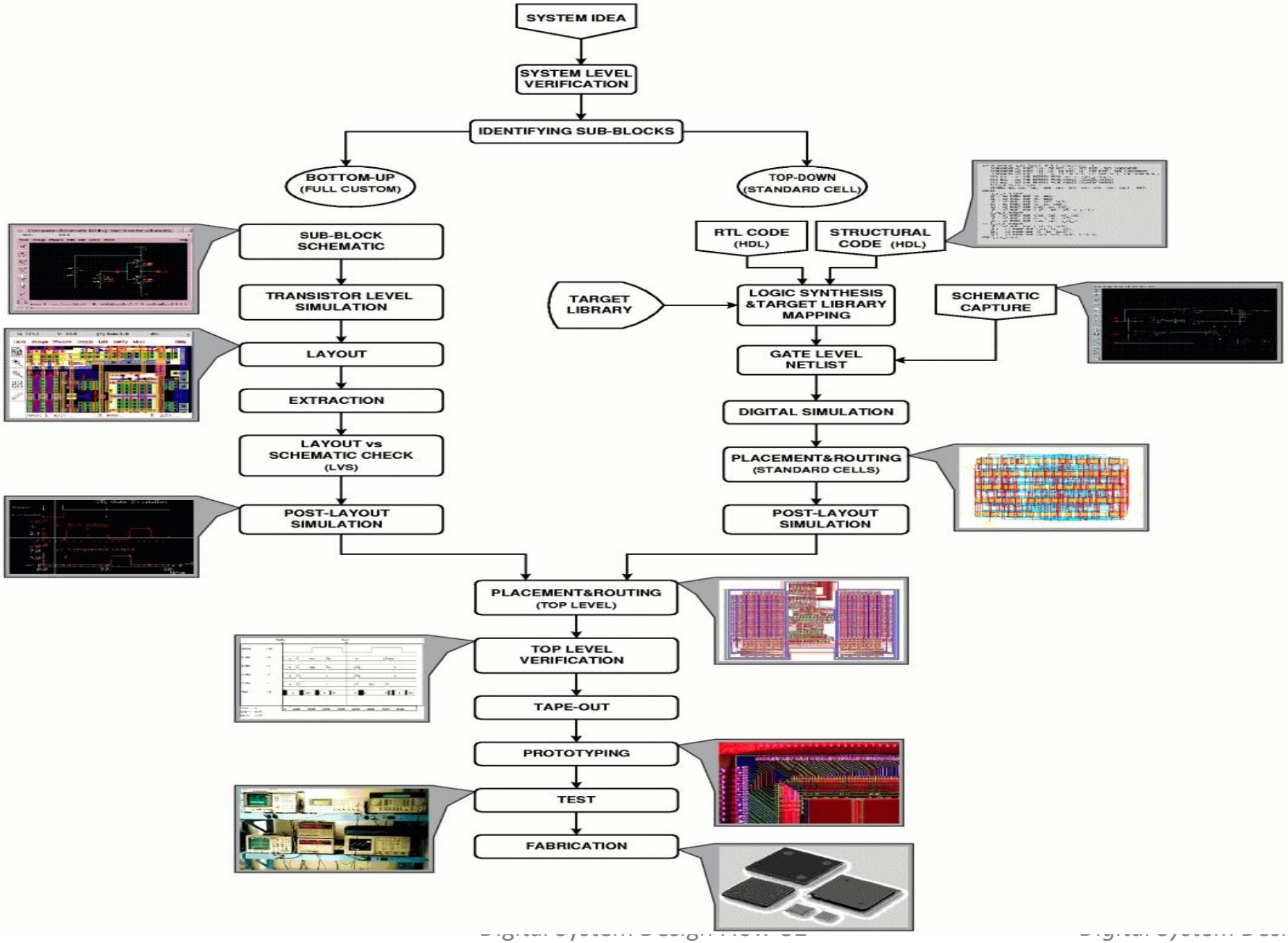
TEST

Performance verification and debugging of the prototype.

FABRICATION

Mass-production of the designed chip.

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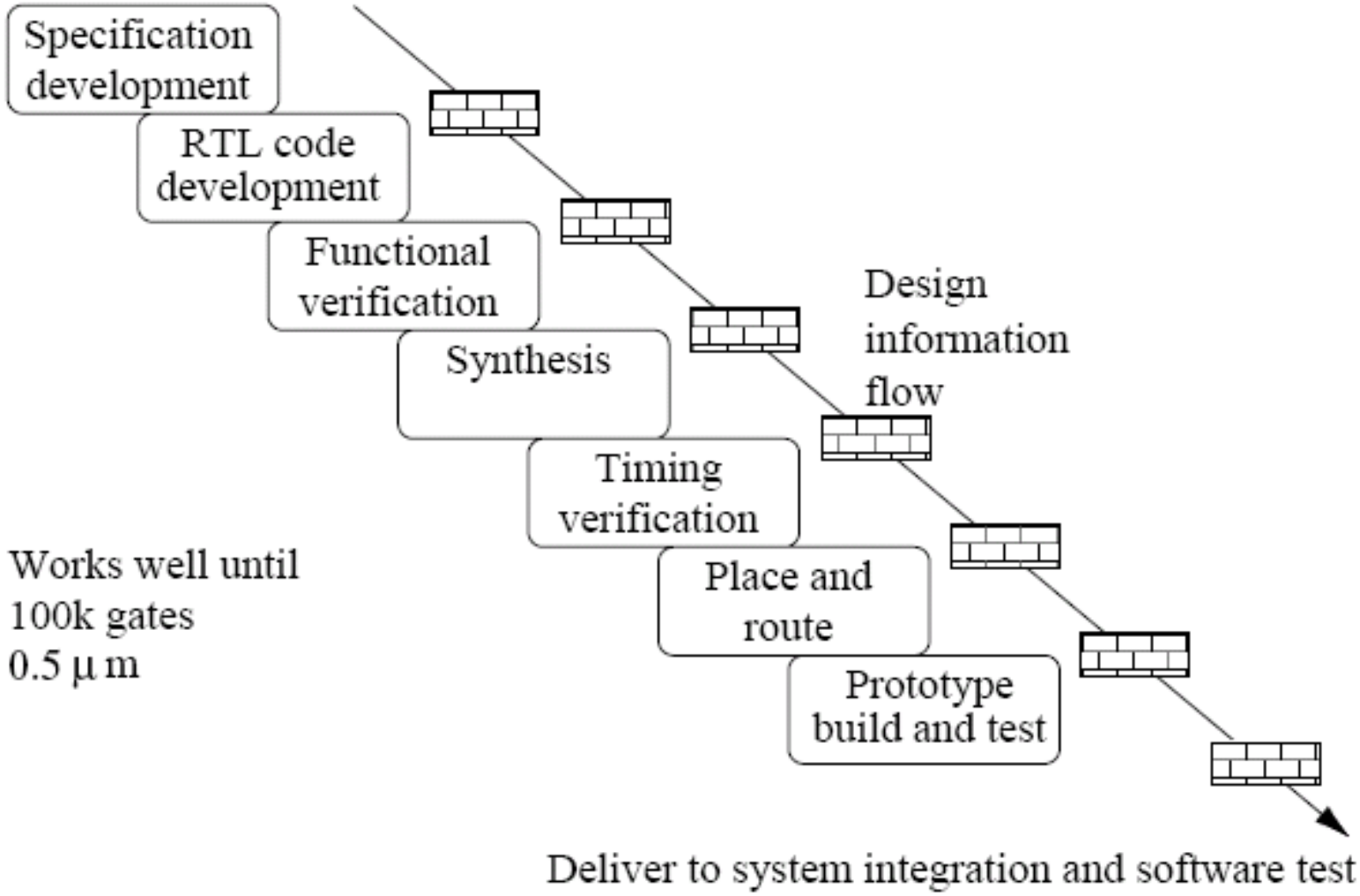
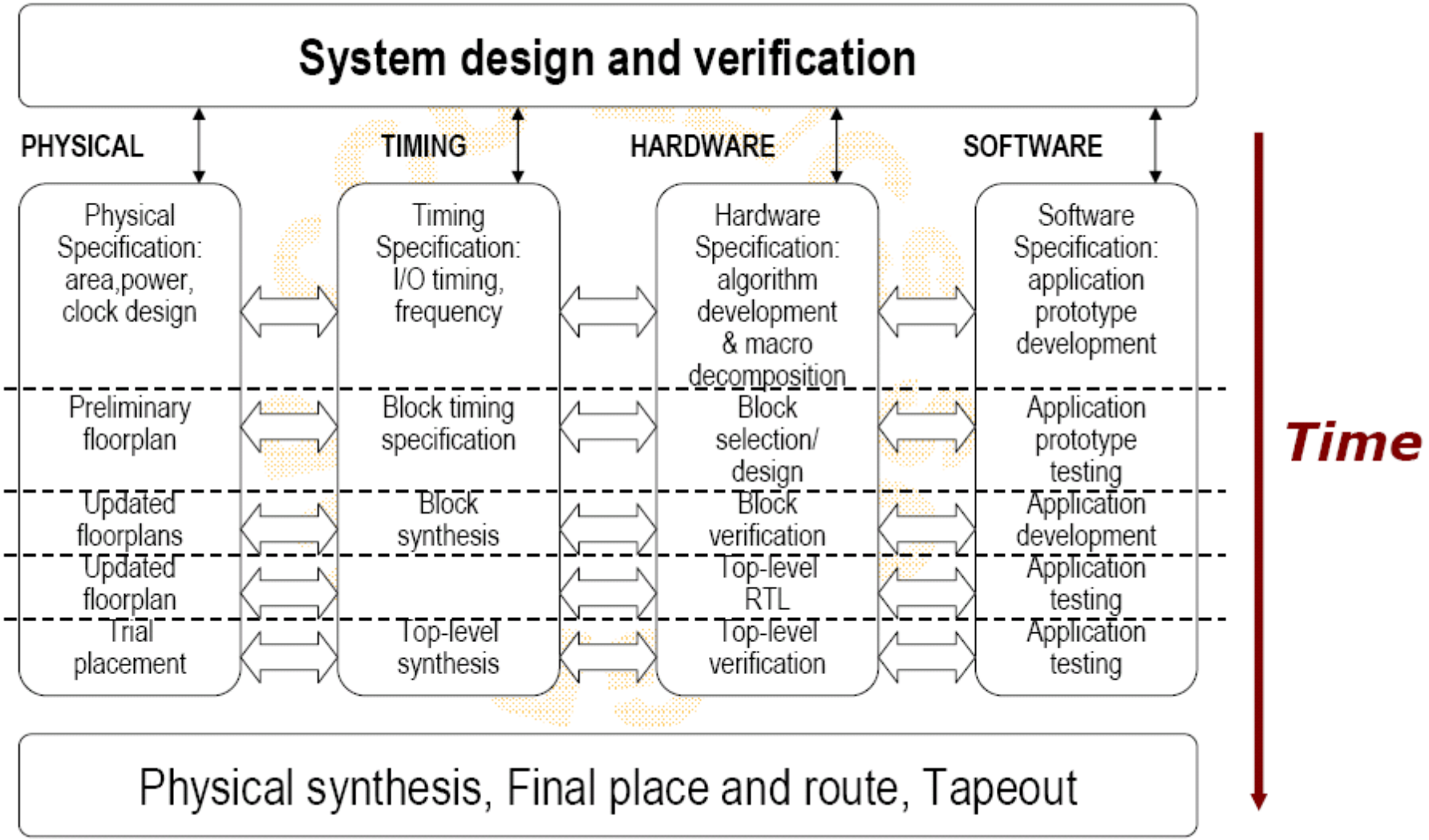
Traditional Waterfall Model

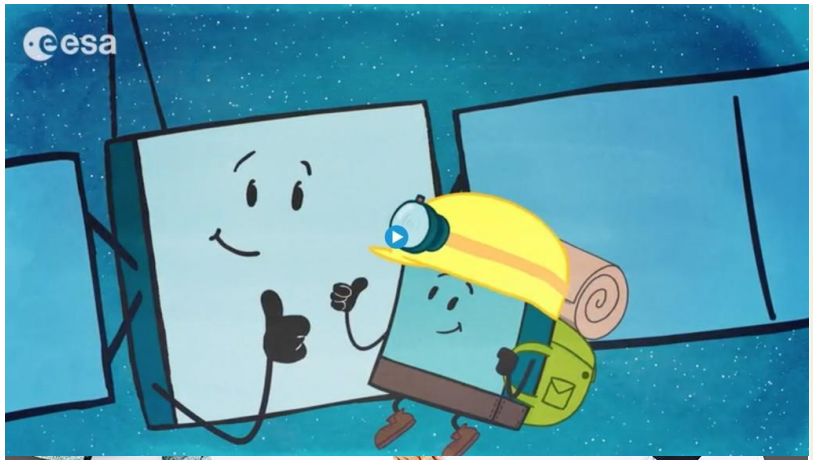


Spiral SOC Design Flow

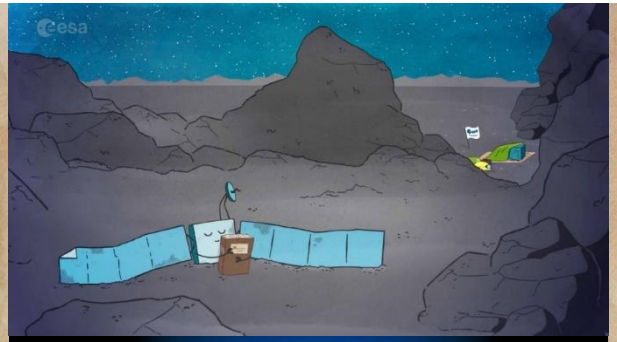


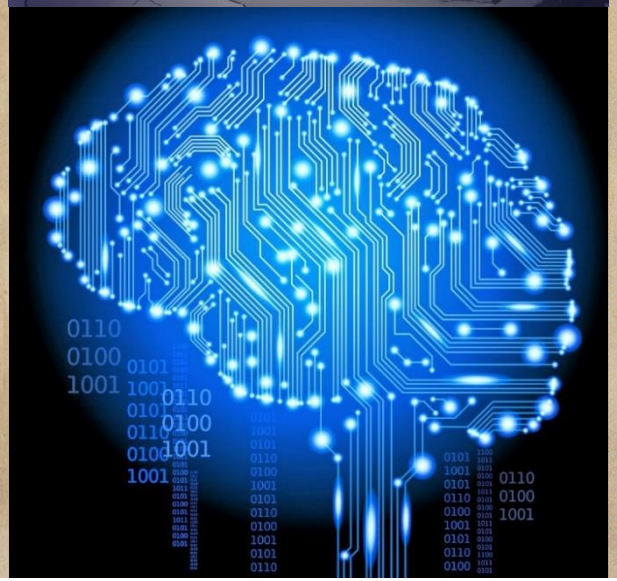
Digital Systems

- **Finite primitive elements create almost infinite possibilities!**
  - **Enabling technology for almost EVERYTHING we take for granted today!**



Farewell & Happy New Year





羅賽塔和菲萊的彗星大冒險
https://www.youtube.com/playlist?list=PLzYYnhQlXmVGDAJ9Dmn7V_alS5VBpZvMp

We thank you for pushing the frontiers of knowledge for the advancement of humanity. ☺