SEMÁFARO

Projeto – I Unidade

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Tabela Verdade

	A	B	C	D	S_LO,	S_NS
A	0	0	1	1	1	0
	0	1	1	1	1	0
	1	0	1	1	1	0
	1	1	1	1	1	0
B	0	0	0	1	1	0
	0	0	1	0	1	0
C	1	1	0	0	0	1
	1	1	0	1	0	1
	1	1	1	0	0	1
D	0	1	0	0	0	1
	1	0	0	0	0	1
E	0	0	0	0	1	0
F	1	0	1	0	1	0
	0	1	1	0	1	0
	1	0	0	1	1	0
	0	1	0	1	1	0

A. O sinal da direção (L/O) será verde quando as duas pistas C e D estiverem ocupadas;

B. O sinal da direção (L/O) será verde sempre que as pistas C ou D estiverem ocupadas, mas com as A e B desocupadas;

C. O sinal da direção (N/S) será verde sempre que as duas pistas A e B estiverem ocupadas, mas as pistas C ou D estiverem desocupadas;

D. O sinal da direção N/S será verde quando as pistas A ou B estiverem ocupadas e enquanto ambas as pistas C e D estiverem vazias;

E. O sinal da direção leste-oeste será verde quando não houver veículo presente;

F. Nos casos omissos, C e D têm preferência sobre A e B.

Equações 01

S_LO = ABCD + A B' C D + A B' C D' +AB'C'D + A'BCD+A'BCD'+A'BC'D + A'B'CD+A'B'CD'+A'B'C'D+ A'B'C′D′

S_LO= ACD(B+B') + A B' C D' + AB'C'D + A'BCD + A'BCD' + A'BC'D + A'B'CD + A'B'CD' + A'B'C'D + A'B'C'D′

S_LO = ACD + A B' C D' + AB'C'D + A'BCD + A'BCD' + A'BC'D + A'B'CD + A'B'CD' + A'B'C'D + A'B'C'D′

S_LO = ACD + A B' C D' + AB'C'D + A'BCD + A'BCD' + A'BC'D + A'B'C(D + D') + A'B'C'D + A'B'C′D′

S_LO = ACD + A B' C D' + AB'C'D + A'BCD + A'BCD' + A'BC'D + A'B'C + A'B'C'D + A'B'C'D′

S_LO = ACD + A B' C D' + AB'C'D + A'BCD + A'BCD' + A'BC'D + A'B'C + A'B'C'(D + D′)

S_LO = ACD + A B' C D' + AB'C'D + A'BCD + A'BCD' + A'BC'D + A'B'C + A'B′C′

S_LO = ACD + A B' C D' + AB'C'D + A'BCD + A'BCD' + A'BC'D + A'B'(C + C′)

S_LO = ACD + A B' C D' + AB'C'D + A'BCD + A'BCD' + A'BC'D + A′B′

S_LO = ACD + A B' C D' + AB'C'D + A'BC(D + D') + A'BC'D + A'B′

Equações 01

S_LO = ACD + A B' C D' + AB'C'D + A'BC + A'BC'D + A'B'

S_LO = AC(D + [B' D']) + AB'C'D + A'BC + A'BC'D + A'B'

S_LO = AC(D + B') + AB'C'D + A'BC + A'BC'D + A'B'

S_LO = ACD + ACB' + AB'C'D + A'BC + A'BC'D + A'B'

S_LO = ACD + ACB' + AB'C'D + A'BC + A'BD + A'B'

S_LO = ACD + ACB' + AB'C'D + A'BC + A'D + A'B'

S_LO = ACD + ACB' + AB'C'D + A'BC + A'D + A'B'

S_LO = ACD + ACB' + AB'D + A'C + A'D + A'B'

S_LO = CD + CB' + B'D + A'C + A'D + A'B'

Equações 02

S_NS = ABC'D′ + ABC′D + ABCD′ + A'BC'D′ + AB'C'D′

S_NS = ABC'[D′+D] + ABCD′ + A'BC′D + AB'C'D′

S_NS = AB[C'+CD′] + A'BC′D + AB'C'D′

S_NS = AB[[C'+C][C'+D′]] + A'BC′D + AB'C'D′

S_NS = AB[C'+D′] + A'BC′D + AB'C′D′

S_NS = ABC′ + ABD′ + A'BC′D + AB'C′D′

S_NS = ABC′ + A'BC′D + AD'[B+B'C′]

Equações 02

S_NS = ABC′ + A'BC′D + AD'[(B+B'](B+C′)]

S_NS = ABC′ + A'BC′D + AD'(B+C′)

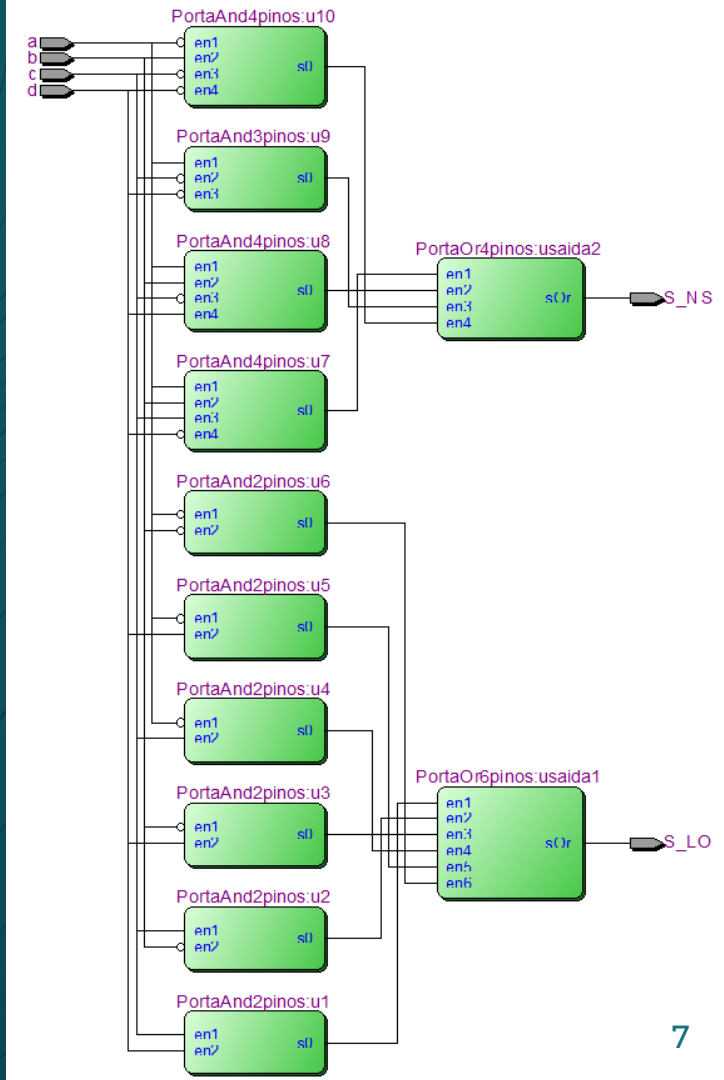
S_NS = ABC′ + A'BC′D + ABD′ + AC'D′

S_NS = BC'(A+A′D) + ABD′ + AC'D′

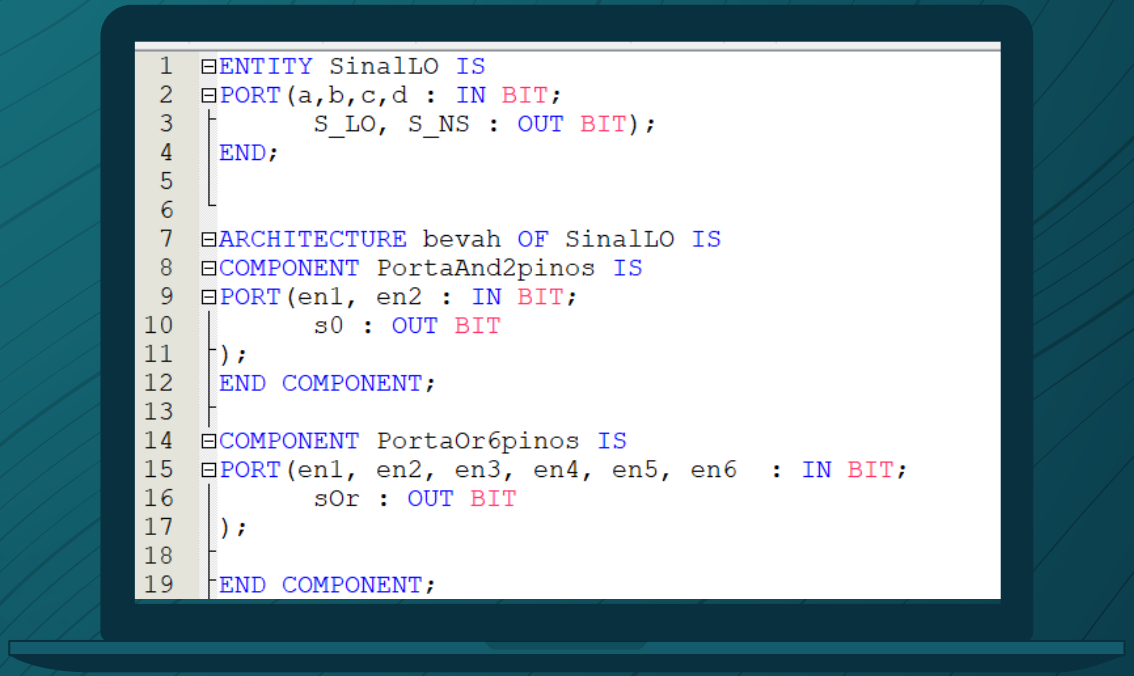
S_NS = BC'[(A+A'](A+D)] + ABD′ + AC'D'

S_NS = BC′A + BC′D + ABD′ + AC'D'

DIAGRAMA DOS CIRCUITOS

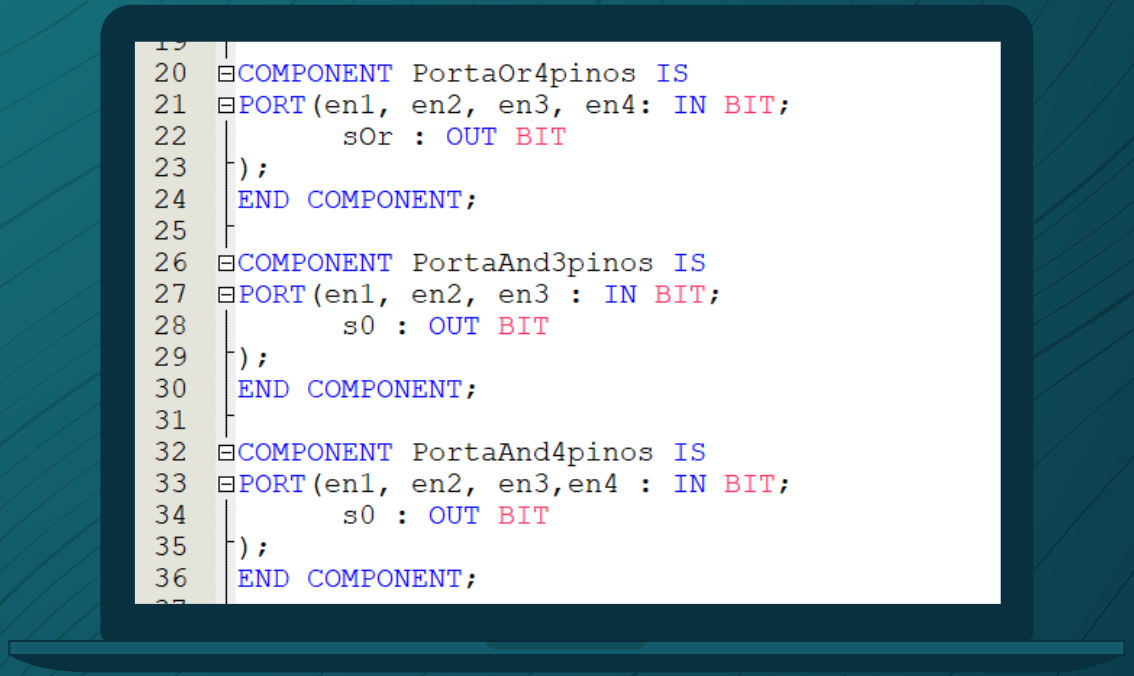


Implementação do Circuito



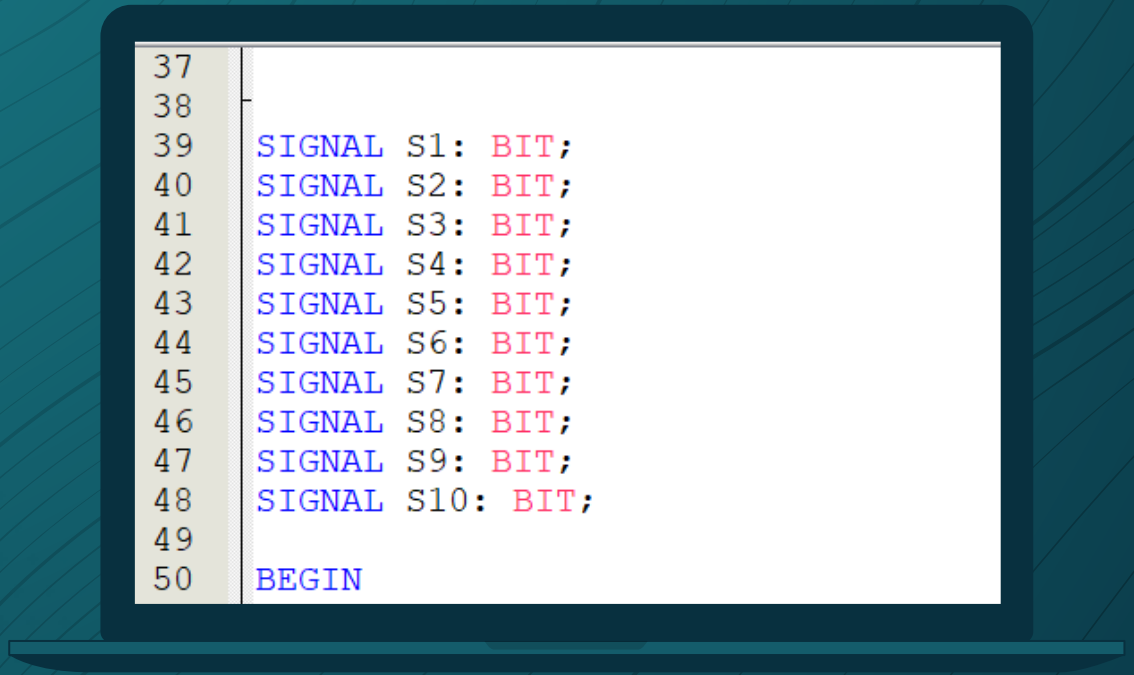
```
1  ENTITY SinalLO IS
2  PORT(a,b,c,d : IN BIT;
3        S_LO, S_NS : OUT BIT);
4  END;
5
6
7  ARCHITECTURE bevah OF SinalLO IS
8  COMPONENT PortaAnd2pinos IS
9  PORT(en1, en2 : IN BIT;
10       s0 : OUT BIT
11 );
12 END COMPONENT;
13
14 COMPONENT PortaOr6pinos IS
15 PORT(en1, en2, en3, en4, en5, en6  : IN BIT;
16       sOr : OUT BIT
17 );
18
19 END COMPONENT;
```

Implementação do Circuito



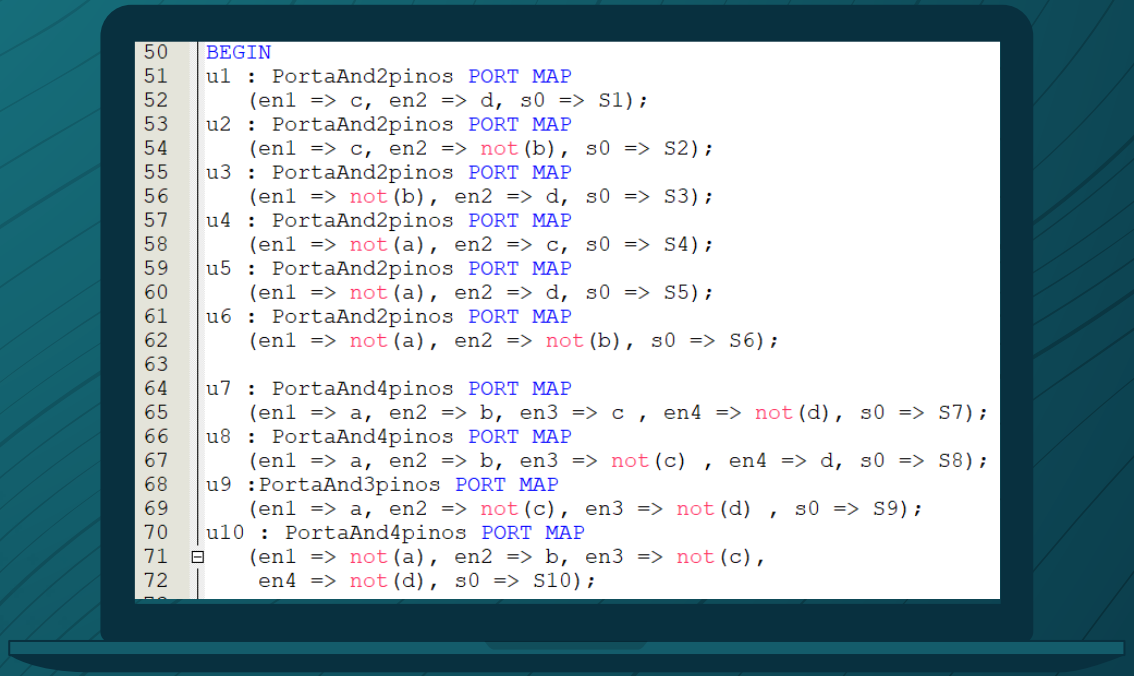
```
20  COMPONENT PortaOr4pinos IS
21  PORT(en1, en2, en3, en4: IN BIT;
22         sOr : OUT BIT
23  );
24  END COMPONENT;
25
26  COMPONENT PortaAnd3pinos IS
27  PORT(en1, en2, en3 : IN BIT;
28         s0 : OUT BIT
29  );
30  END COMPONENT;
31
32  COMPONENT PortaAnd4pinos IS
33  PORT(en1, en2, en3,en4 : IN BIT;
34         s0 : OUT BIT
35  );
36  END COMPONENT;
```

Implementação do Circuito



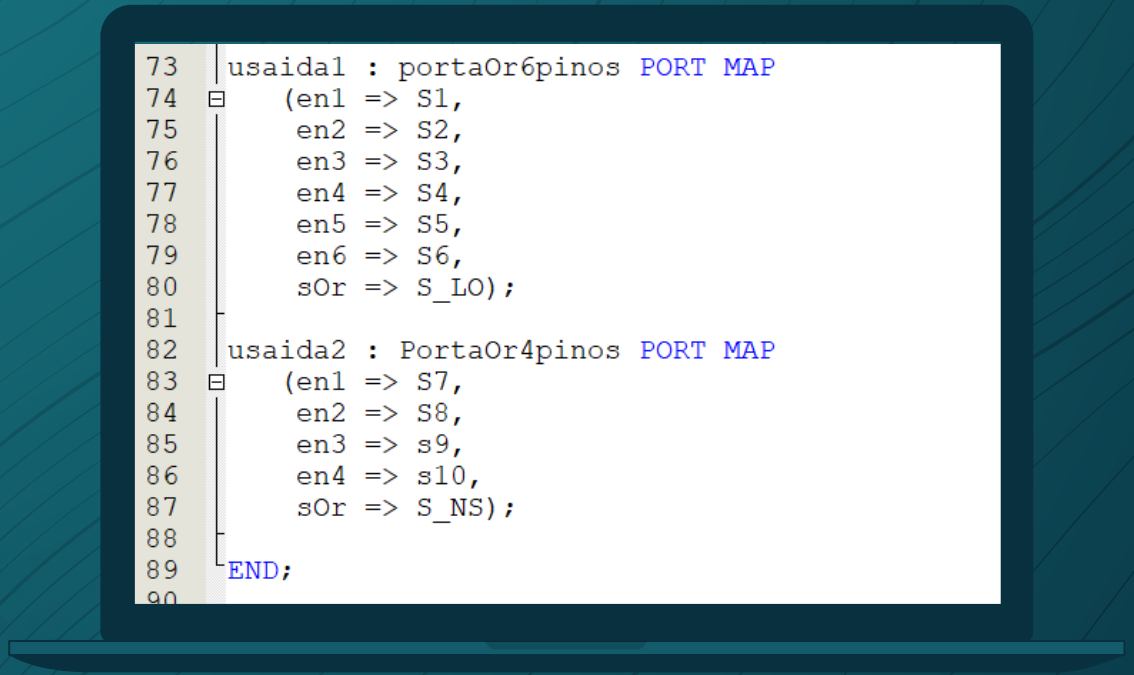
```
37
38
39  SIGNAL S1: BIT;
40  SIGNAL S2: BIT;
41  SIGNAL S3: BIT;
42  SIGNAL S4: BIT;
43  SIGNAL S5: BIT;
44  SIGNAL S6: BIT;
45  SIGNAL S7: BIT;
46  SIGNAL S8: BIT;
47  SIGNAL S9: BIT;
48  SIGNAL S10: BIT;
49
50  BEGIN
```

Implementação do Circuito



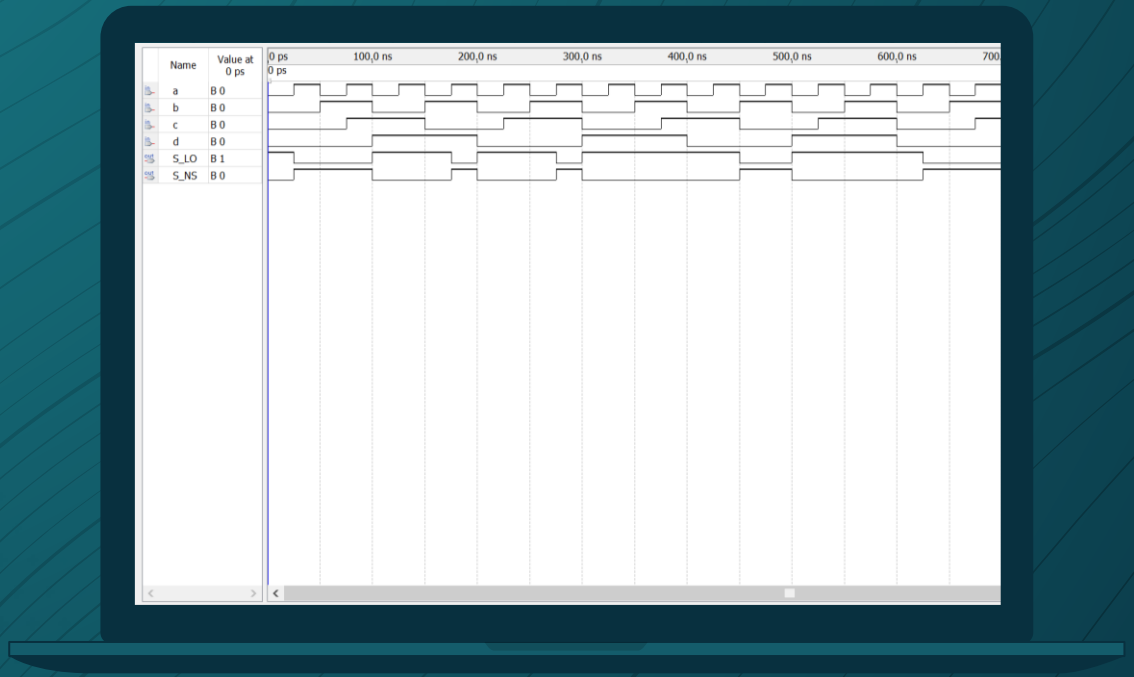
```
50  BEGIN
51  u1 : PortaAnd2pinos PORT MAP
52     (en1 => c, en2 => d, s0 => S1);
53  u2 : PortaAnd2pinos PORT MAP
54     (en1 => c, en2 => not(b), s0 => S2);
55  u3 : PortaAnd2pinos PORT MAP
56     (en1 => not(b), en2 => d, s0 => S3);
57  u4 : PortaAnd2pinos PORT MAP
58     (en1 => not(a), en2 => c, s0 => S4);
59  u5 : PortaAnd2pinos PORT MAP
60     (en1 => not(a), en2 => d, s0 => S5);
61  u6 : PortaAnd2pinos PORT MAP
62     (en1 => not(a), en2 => not(b), s0 => S6);
63
64  u7 : PortaAnd4pinos PORT MAP
65     (en1 => a, en2 => b, en3 => c , en4 => not(d), s0 => S7);
66  u8 : PortaAnd4pinos PORT MAP
67     (en1 => a, en2 => b, en3 => not(c) , en4 => d, s0 => S8);
68  u9 :PortaAnd3pinos PORT MAP
69     (en1 => a, en2 => not(c), en3 => not(d) , s0 => S9);
70  u10 : PortaAnd4pinos PORT MAP
71     (en1 => not(a), en2 => b, en3 => not(c),
72      en4 => not(d), s0 => S10);
```

Implementação do Circuito



```
73  usaida1 : portaOr6pinos PORT MAP
74     (en1 => S1,
75      en2 => S2,
76      en3 => S3,
77      en4 => S4,
78      en5 => S5,
79      en6 => S6,
80      sOr => S_LO);
81
82  usaida2 : PortaOr4pinos PORT MAP
83     (en1 => S7,
84      en2 => S8,
85      en3 => s9,
86      en4 => s10,
87      sOr => S_NS);
88
89  END;
```

Simulação


Name
Value at 0 ps
0 ps
100,0 ns
200,0 ns
300,0 ns
400,0 ns
500,0 ns
600,0 ns
a B 0
b B 0
c B 0
d B 0
S_LO B 1
S_NS B 0

Precificação

Cálculo salarial			
piso salarial	Salário CLT*:	CLT por hora**:	
R$ 6.600,00	R$ 10.084,80	R$ 84,04	Regime de 6 horas/dia
R$ 8.250,00	R$ 12.606,00	R$ 105,05	Regime 7 horas/dia
R$ 9.900,00	R$ 15.127,20	R$ 126,06	Regime 8 horas/dia

*= piso + 52,8% do piso

** = Salário CLT/4semanas/5dias/6horas

Horas trabalhadas	5
salário/hora	R$ 84,04
energia/hora	R$ 0,19
internet/hora	R$ 1,25
Lucro	10,00%
IR*	15,50%
ISS	5,00%
Valor sem imposto	R$ 470,14
Preço final:	R$ 566,52

Obrigado!

Pela atenção

Alguma Dúvida?