ELEC2104 – Week 4

PN Junction current, circuit models

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Fermi level LEVELs in equilibrium

$$w = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{bi} + V_R)}$$

$$V_{bi} = \frac{k_B T}{q} \ln \frac{N_A N_D}{n_i^2}$$

w	depletion region width
ε_s	permittivity of semiconductor
q	elementary charge
N_A, N_D	acceptor and donor density
V_{bi}	built-in potential
V_R	external bias
k_B	Boltzmann constant
n_i^2	intrinsic carrier density

pn junction currents and V_{bi}

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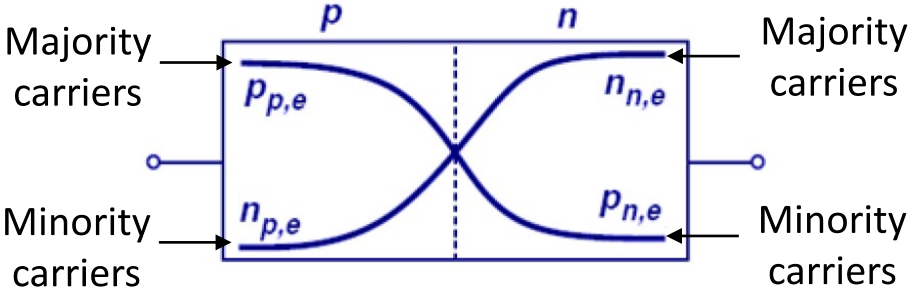
Carrier concentration in pn Junction in equilibrium

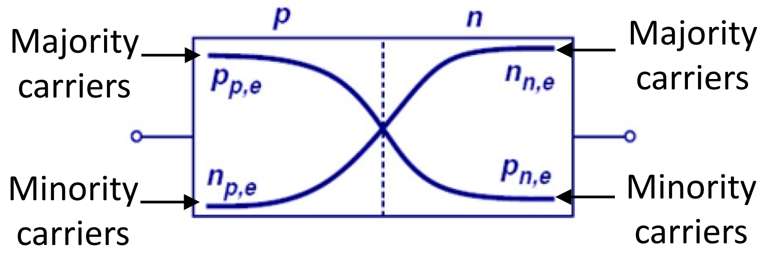
- In equilibrium
  - No external connections (open terminals)



n_n : **Concentration of electrons on n side**
p_n : **Concentration of holes on n side**
p_p : **Concentration of holes on p side**
n_p : **Concentration of electrons on p side**

- p side contains large excess of holes and n side contains large excess of electrons
  - Sharp concentration gradient (several orders of magnitude over μm)
  - Large diffusion currents
  - Electrons flow from n side to the p side
  - Holes flow from p side to the n side
  - The shape of the $p(x)$ and $n(x)$ is unknown (we don't need to know them)

PN Junction Currents



Concentration gradient (Diffusion current) ⟷ **Strong E-Field (drift current)**

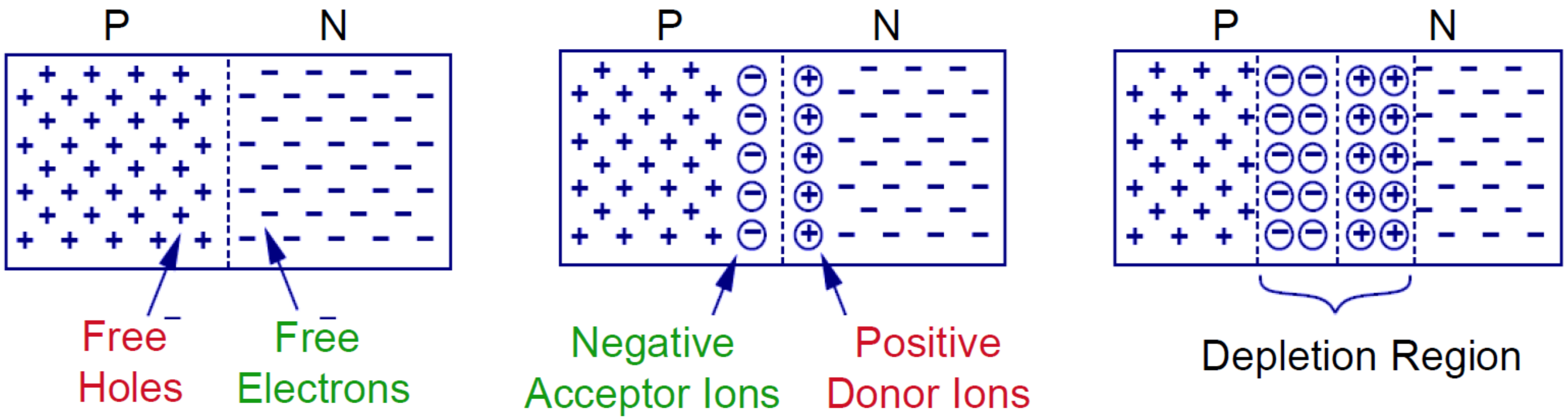
JUNCTION REACHES EQUILIBRIUM

$$I_{drift,p} = I_{diff,p} \quad \text{and} \quad I_{drift,n} = I_{diff,n}$$

Hole drift and diffusion currents must be equal and opposite at equilibrium.

Holes Diffuse →

← Holes Drift



← Electrons Diffuse

Electrons Drift →

Electron drift and diffusion currents must be equal and opposite at equilibrium.

Calculating the built-in potential by balancing currents

- We don't know $n(x), p(x)$ in the junction region
- We don't know $V(x)$
- No need to know these

E-field is defined as $E = -\dfrac{dV}{dx}$

$$I_{drift,p} = I_{diff,p}$$

$$q\mu_p pE = qD_p \frac{dp}{dx}$$

$$-q\mu_p p \frac{dV}{dx} = qD_p \frac{dp}{dx}$$

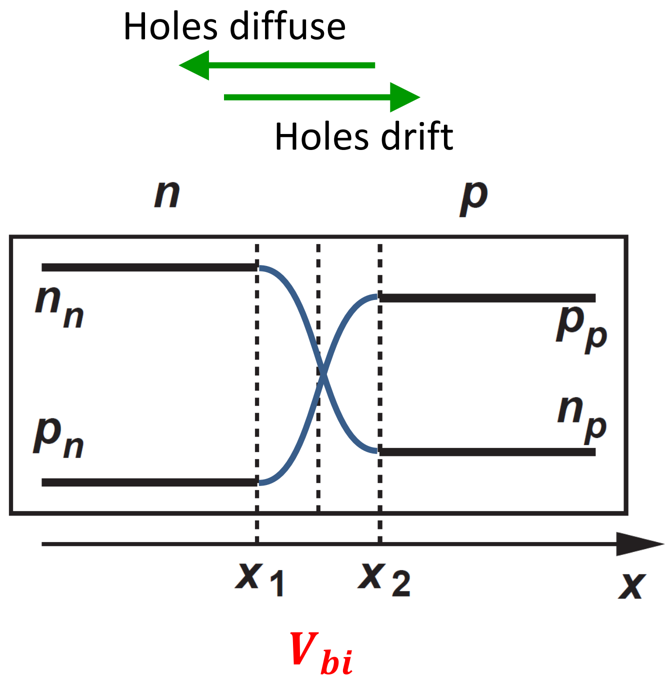
$$-\mu_p \int_{x_1}^{x_2} dV = D_p \int_{p_n}^{p_p} \frac{dp}{p}$$

$$V(x_2) - V(x_1) = -\frac{D_p}{\mu_p} \ln \frac{p_p}{p_n}$$

Einstein's relation: $\dfrac{D_p}{\mu_p} = \dfrac{kT}{q}$

$$|V_{bi}| = \frac{kT}{q} \ln \frac{p_p}{p_n}$$

$$p_p = N_A, p_n = \frac{n_i^2}{N_D}$$



$$\boxed{|V_{bi}| = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}}$$

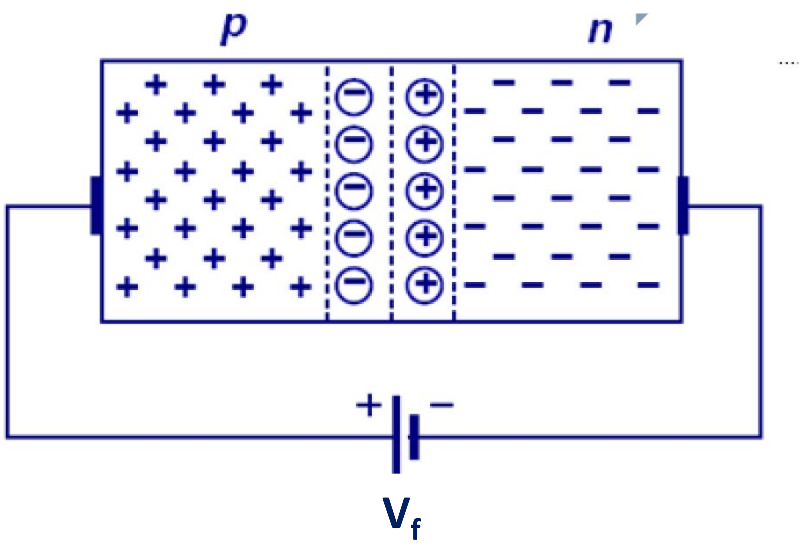
Built-in potential barrier

Recall
$np = n_i^2$

pn junction current under forward bias

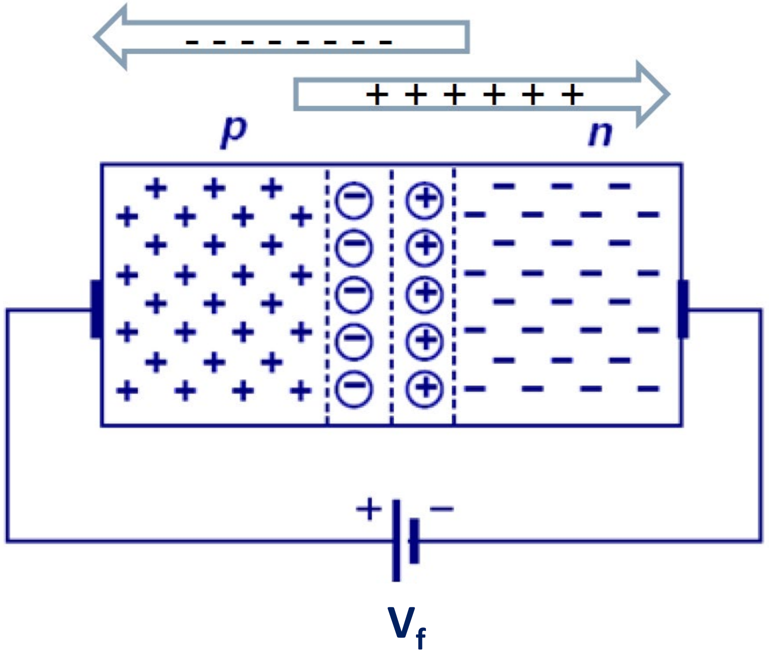
PN Junction under Forward Bias

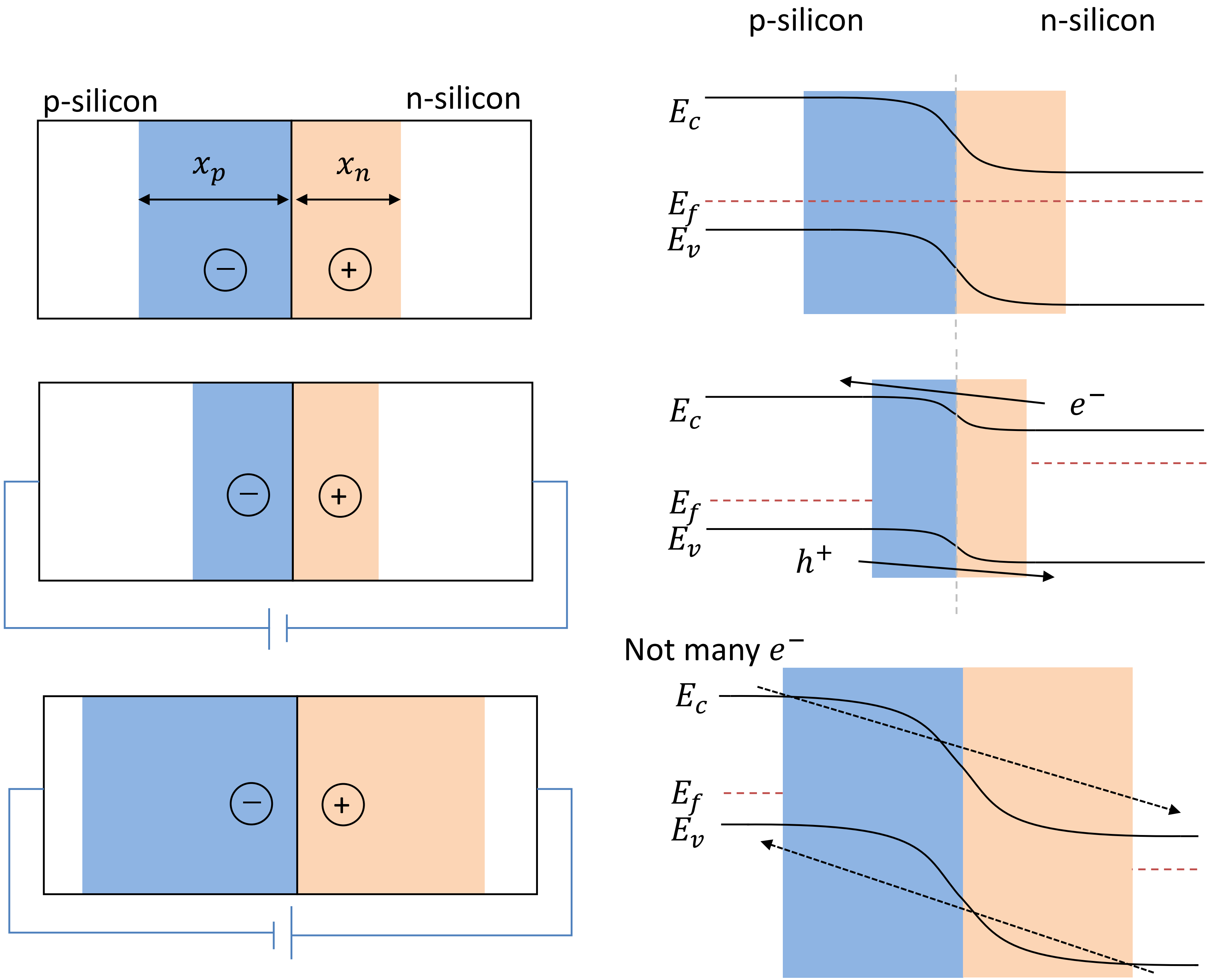
- Consider now an external voltage source V_F is applied across the junction to make *p* side more positive than the *n* side
- The connection of the positive voltage to the *p* terminal is called forward bias
- V_F creates an E-field directed from *p* to *n* side
  - Opposes the built-in field
  - Potential barrier reduces due to weakening of the field



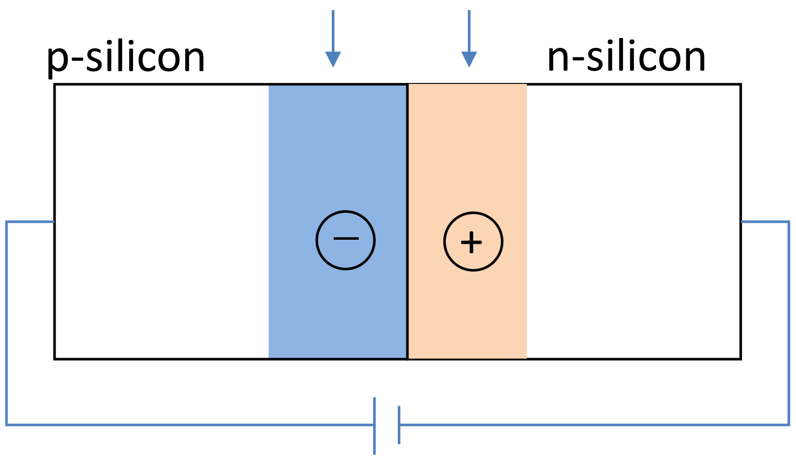
PN Junction under Forward Bias

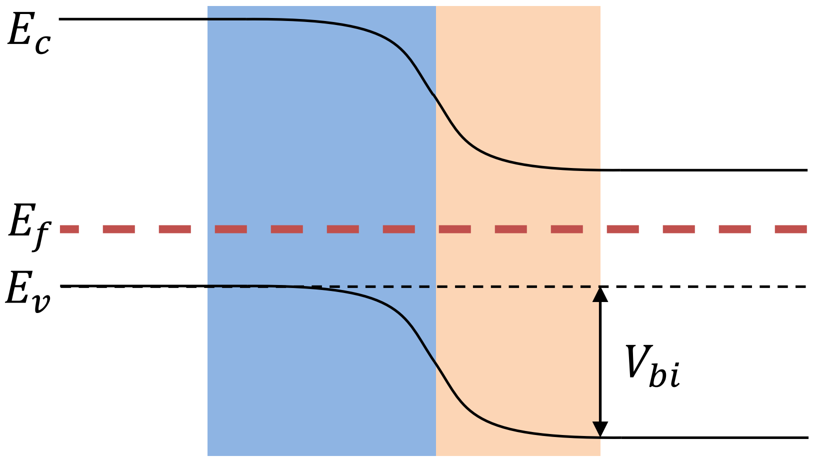
- With the built-in potential lowered, it is easier for holes to cross into the n region and electrons to cross into the p region
- This generates a forward diode current
  - Increases the diffusion current

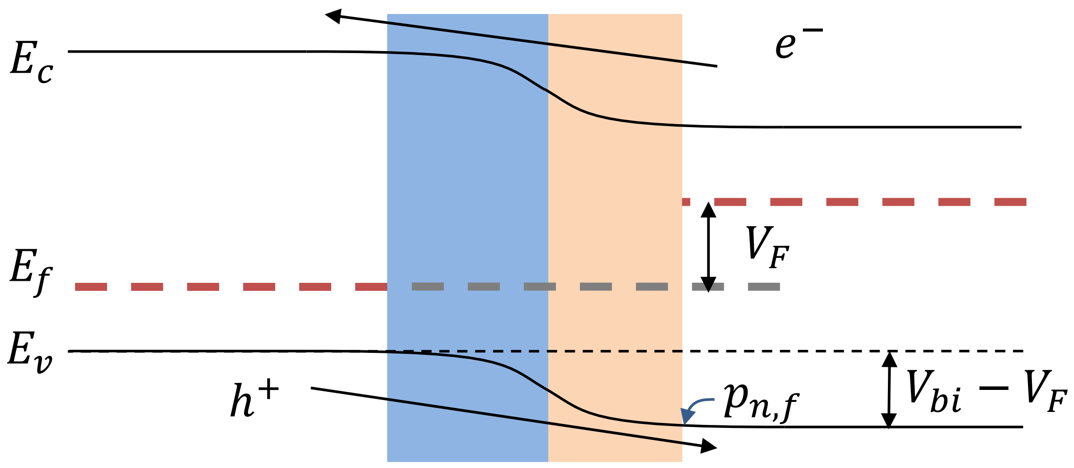



p-silicon
n-silicon
x_p
x_n
p-silicon
n-silicon
E_c
E_f
E_v
E_c
e^-
E_f
E_v
h^+
Not many e^-
E_c
E_f
E_v

- $V_T = \frac{k_B T}{q}$ thermal voltage
- N_A, N_D acceptor and donor density
- p_p hole density in p side (majority)
- $p_{n,e}$ hole density in n side (minority) in equilibrium
- $p_{n,f}$ hole density in n side (minority) under forward bias







'e' for equilibrium

'f' for forward bias

$$V_{bi} = V_T \ln \frac{N_A N_D}{n_i^2} = V_T \ln \frac{p_p}{p_n} \Rightarrow p_{n,e} = p_p \exp\left(-\frac{V_{bi}}{V_T}\right)$$

$$p_{n,f} = p_p \exp\left(-\frac{V_{bi} - V_F}{V_T}\right)$$

Minority Carriers in Forward Bias

- Minority carriers (holes) on the n-side depletion region boundary under forward bias

$$p_{n,e} = p_p \exp\left(-\frac{V_{bi}}{V_T}\right)$$

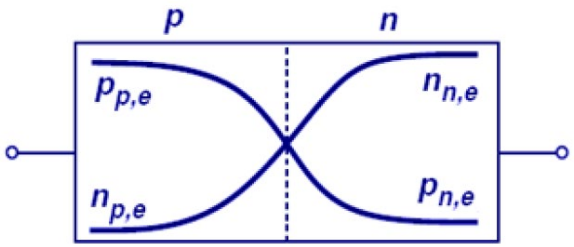
'e' for equilibrium

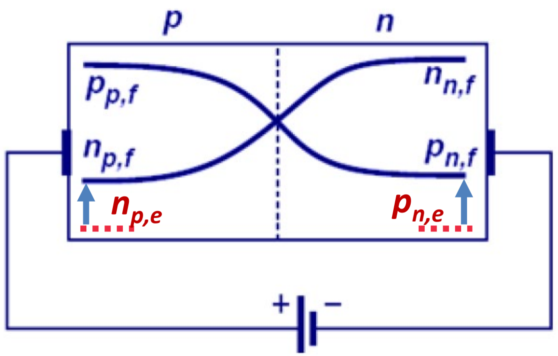
- Potential barrier is lowered by an amount equal to V_F

$$p_{n,f} = p_p \exp\left(-\frac{V_{bi} - V_F}{V_T}\right)$$

'f' for forward bias

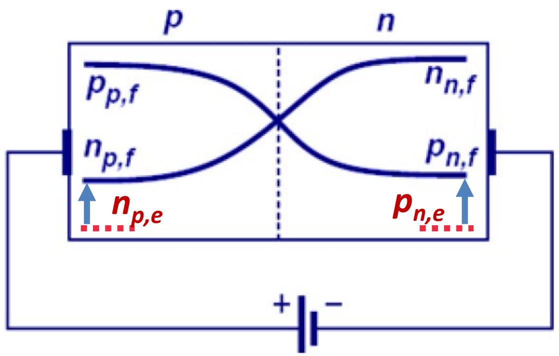
- The minority carrier concentration rises rapidly while the majority carrier concentration remains relatively constant





I/V Characteristics in Forward Bias

- Change in the hole concentration (minority carriers) on the *n* side



$$\Delta p_n = p_{n,f} - p_{n,e} = p_p e^{-\frac{V_{bi}-V_F}{V_T}} - p_p e^{-\frac{V_{bi}V_F}{V_T}}$$

$$= \frac{N_A}{\exp\frac{V_{bi}}{V_T}}\left(\exp\frac{V_F}{V_T} - 1\right)$$

$$p_p = N_A$$

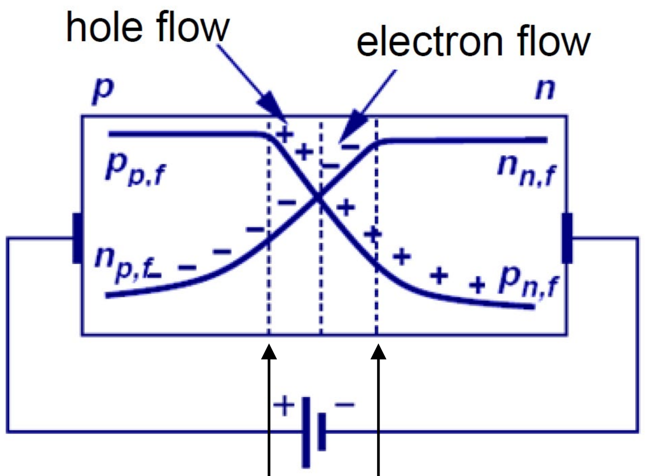
$$= \frac{n_i^2}{N_D}\left(\exp\frac{V_F}{V_T} - 1\right)$$

$$\exp\frac{V_{bi}}{V_T} = \frac{N_A N_D}{n_i^2}$$

- Change in the electron concentration (minority carriers) on the *p* side

$$\Delta n_p = \frac{n_i^2}{N_A}\left(\exp\frac{V_F}{V_T} - 1\right)$$

- These changes of minority carrier concentration is calculated at the depletion region boundary



$$\Delta n_p = \frac{n_i^2}{N_A}\left(\exp\frac{V_F}{V_T} - 1\right) \qquad \Delta p_n = \frac{n_i^2}{N_D}\left(\exp\frac{V_F}{V_T} - 1\right)$$

(At the depletion region boundary)

In the bulk, minority carrier concentration gradually returns to the original

Since current is proportional to gradient in carrier concentration

$$I_{hole} \propto \frac{n_i^2}{N_D}\left(\exp\frac{V_F}{V_T} - 1\right), \qquad I_{elec} \propto \frac{n_i^2}{N_A}\left(\exp\frac{V_F}{V_T} - 1\right)$$

I/V Characteristics in Forward Bias

$$I_{hole} \propto \frac{n_i^2}{N_D}\left(\exp\frac{V_F}{V_T} - 1\right), \qquad I_{elec} \propto \frac{n_i^2}{N_A}\left(\exp\frac{V_F}{V_T} - 1\right)$$

- It can be proved that $$I_{tot} = I_S\left(\exp\frac{V_F}{V_T} - 1\right)$$

Derivation is not required; need to understand what each term means.

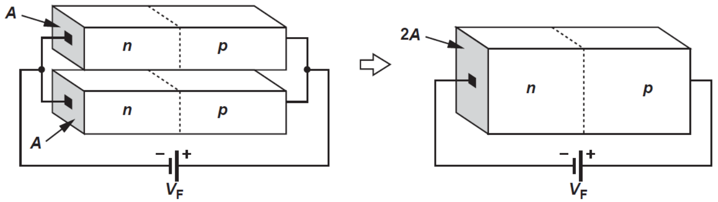
  - I_S is called the “reverse saturation current and given by

$$I_S = Aqn_i^2\left(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right)$$

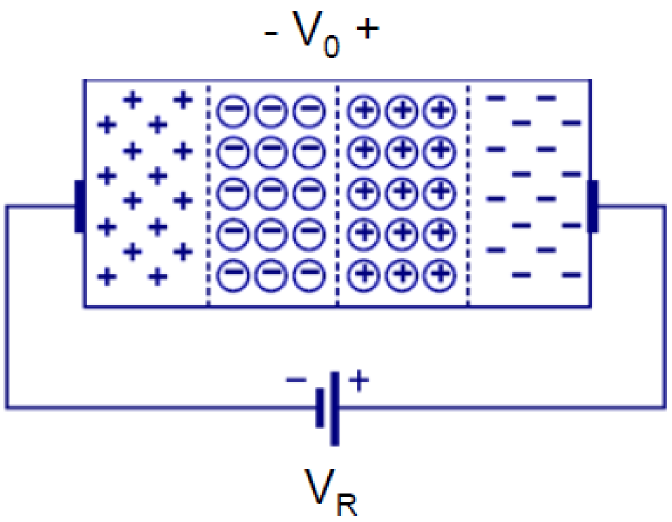
D_n, D_p: diffusion constants

flow of electrons flow of holes

  - $L_{n,p}$ = electron and hole diffusion lengths
    - average length travelled before they recombine with the majority carriers
  - A = cross section area of the device



Reverse saturation current



Reverse saturation current:

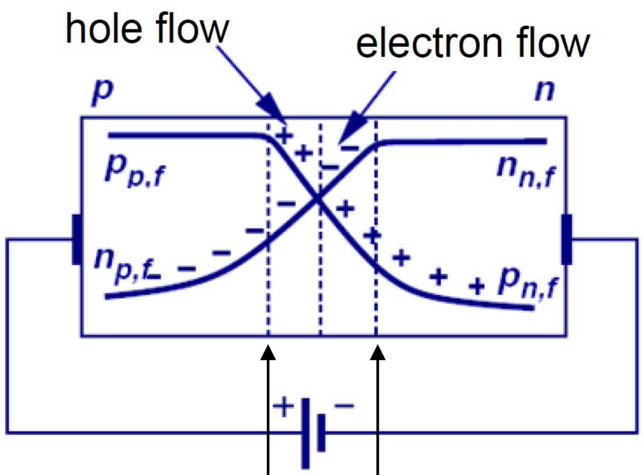
$$I_s = Aqn_i^2 \left(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right)$$

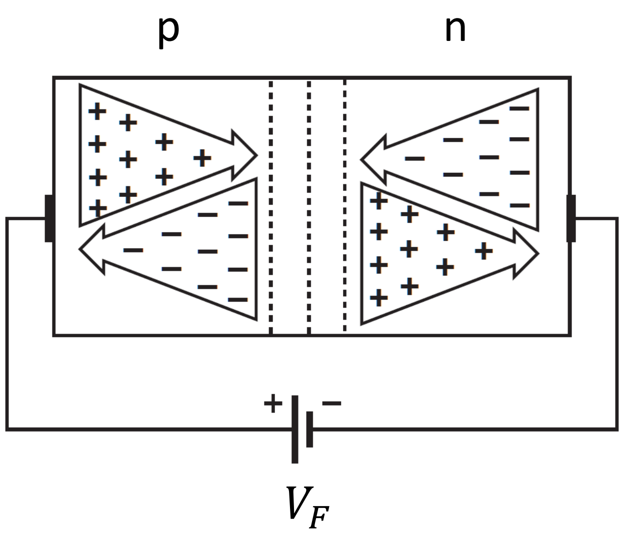
Remember:

$$D_n = \mu_n \frac{U_T}{q}, \quad D_p = \mu_p \frac{U_T}{q}$$

$$U_T = \text{Thermal Energy}$$

- This reverse saturation current is the **drift current** of thermally generated minority holes and electrons near the junction
  - Does not depend on the potential barrier
  - The reverse saturation current is quite small but it increases with temperature.





$$\Delta n_p \approx \frac{n_i^2}{N_A}\left(\exp\frac{V_F}{V_T} - 1\right) \qquad \Delta p_n = \frac{n_i^2}{N_D}\left(\exp\frac{V_F}{V_T} - 1\right)$$

(At the depletion region boundary)

In the bulk, minority carrier concentration gradually returns to the original levels

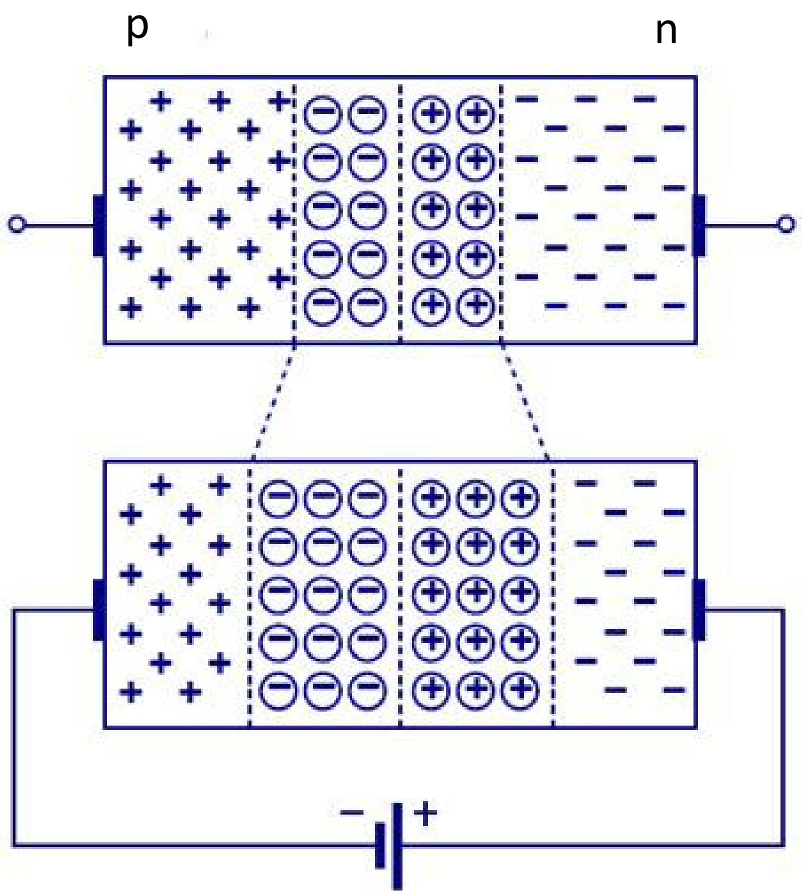
Minority carriers recombine with majority carriers as they diffuse in to the bulk

The majority carrier current and the minority carrier add to the same I_{tot} at any point

pn junction under reverse bias, capacitance

PN Junction under Reverse Bias

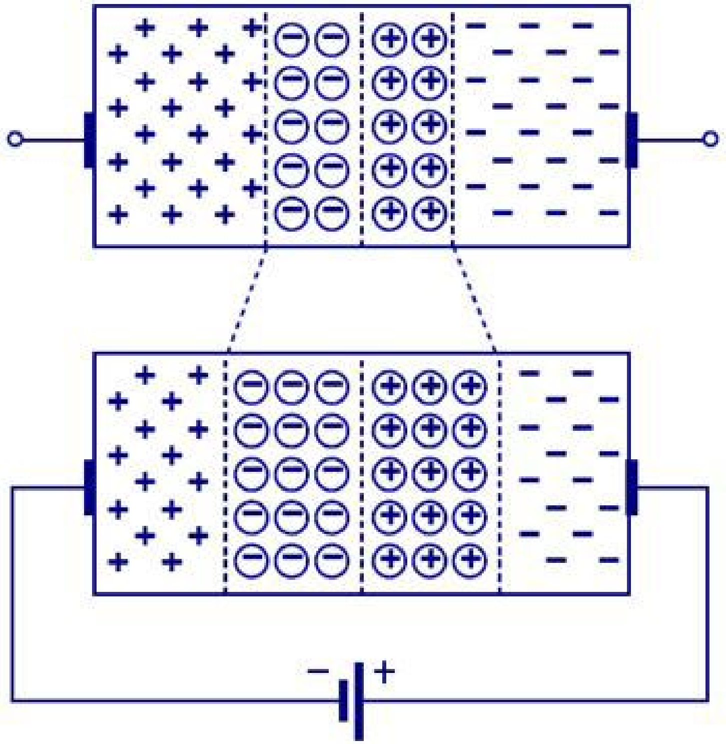
- An external voltage source V_R is now applied across the junction where the *n* side is made more positive than the *p* side
- The connection of the positive voltage to the n terminal is called reverse bias

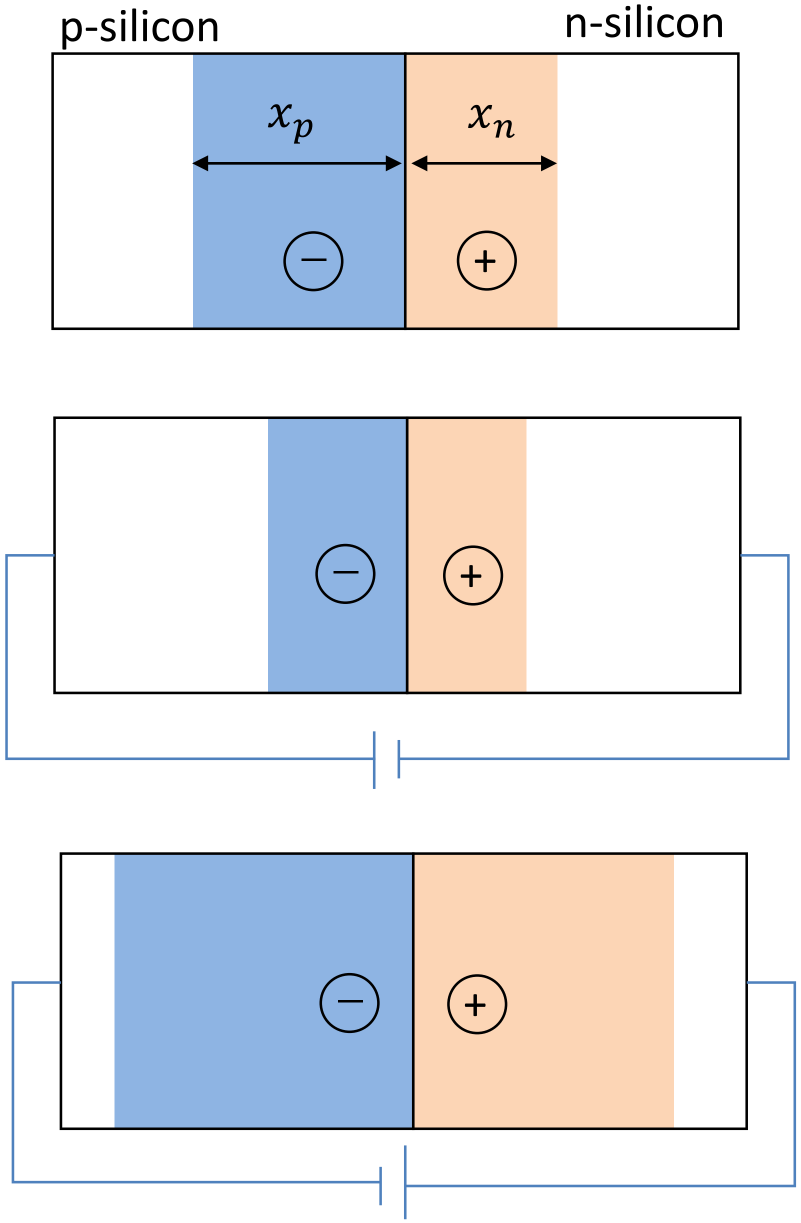


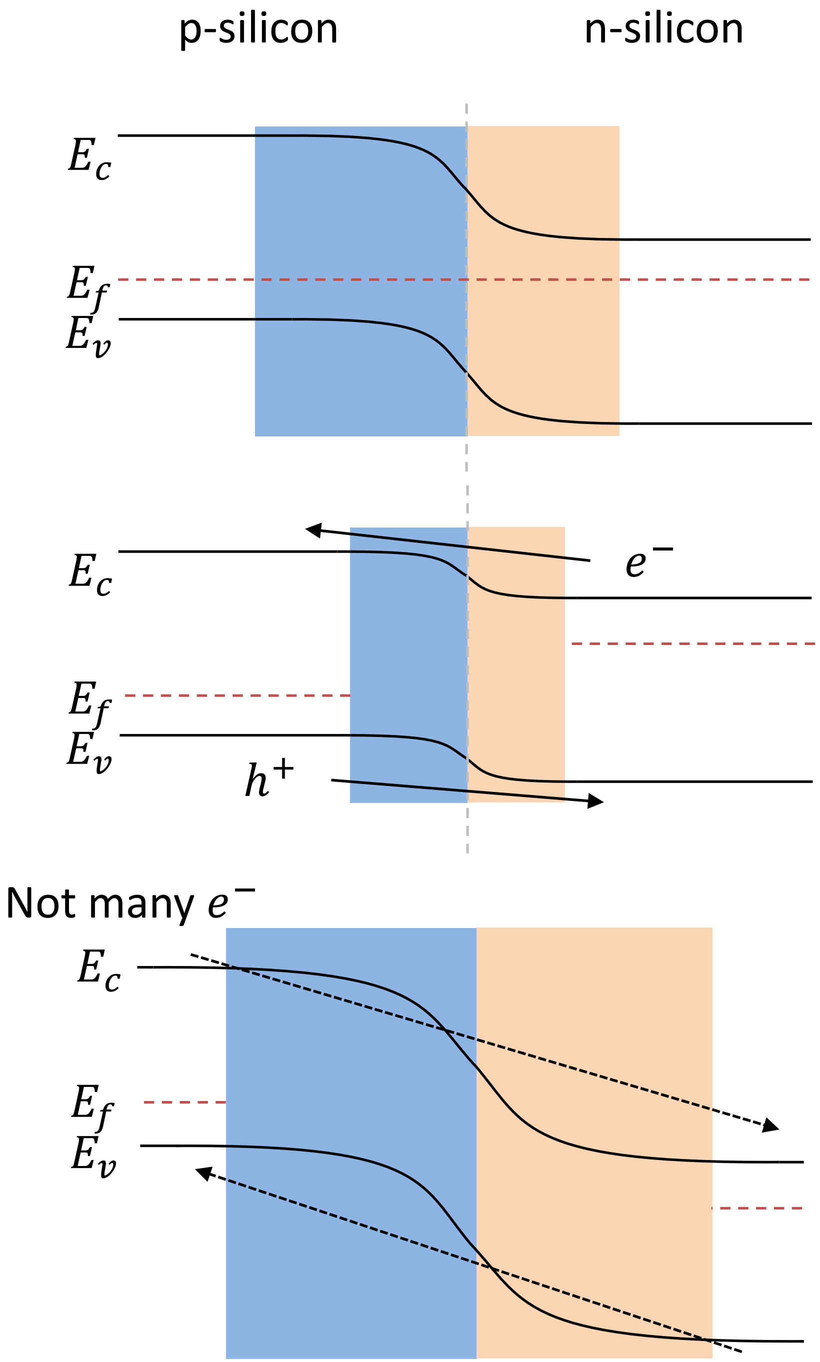
How is this useful?

PN Junction under Reverse Bias

- This reverse bias is magnifying the built-in potential of the diode
- It draws holes away on the p side, electrons away on the n side
- The depletion width is widened and the built-in electric field increased.

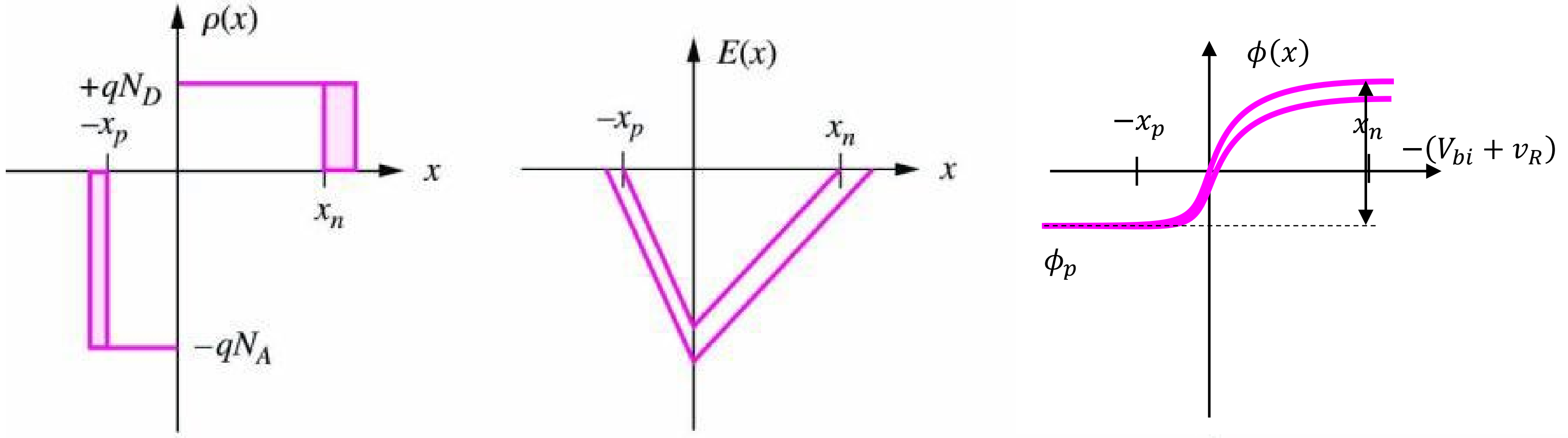



p-silicon
n-silicon
x_p
x_n
−
+


p-silicon
n-silicon
E_c
E_f
E_v
e^-
h^+
Not many e^-

PN Junction under Reverse Bias

- External reverse bias adds to the built-in potential of the pn junction. The shaded regions below illustrate the increase in the characteristics of the space charge region due to an externally applied reverse bias, V_R



(a) Space charge density (b) Electric field (c) Electrostatic potential

PN Junction under Reverse Bias

$$V_{bi} = \frac{k_B T}{q} \ln \frac{N_A N_D}{n_i^2}$$

- External reverse bias increases the width of the depletion region
- The larger electric field must be supported by additional charge.

$$w_d = x_n + x_p = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{bi} + V_R)}$$

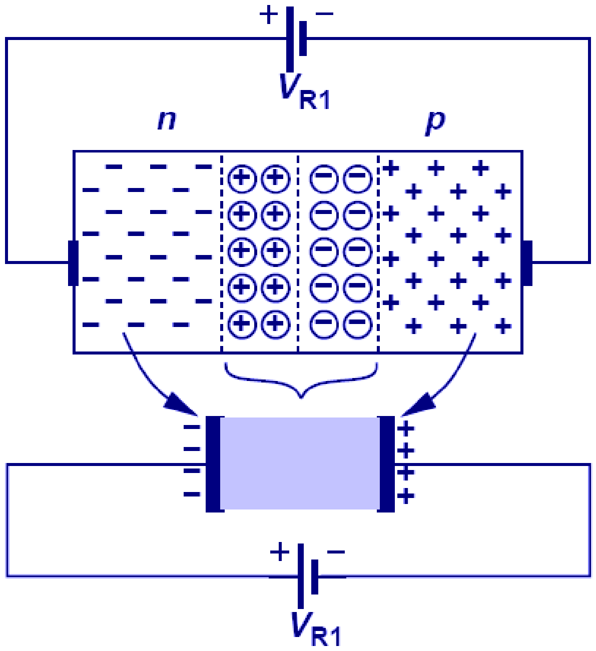
$$w_{d0} = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_{bi}}$$

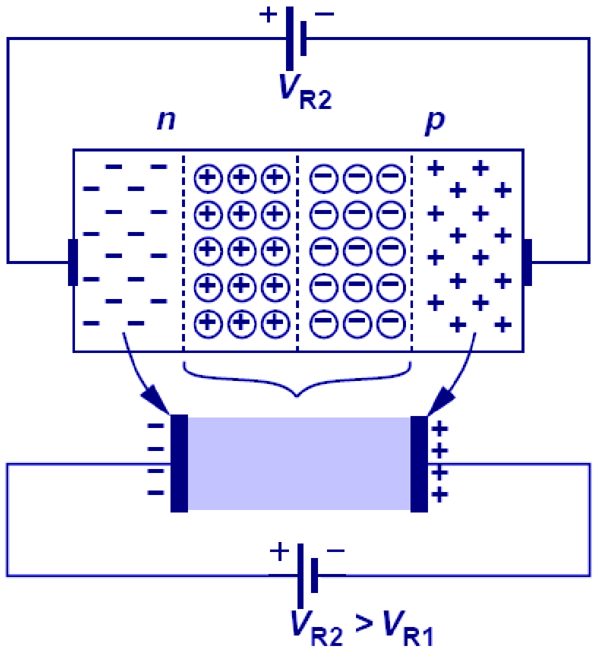
$$w_d = w_{d0}\sqrt{1 + \frac{v_R}{V_{bi}}}$$

w	depletion region width
ε_s	permittivity of semiconductor
q	elementary charge
N_A, N_D	acceptor and donor density
V_{bi}	built-in potential
V_R	external bias
k_B	Boltzmann constant
n_i^2	intrinsic carrier density

Junction capacitance

- The *n* and *p* sections can be viewed as two plates of a capacitor





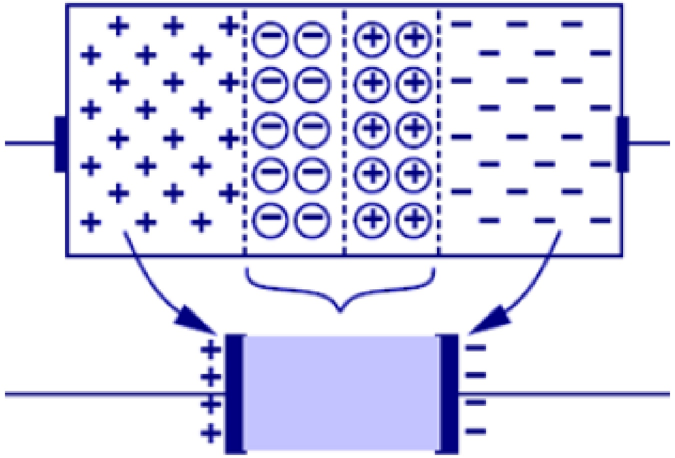
- As V_R increases, the width of the depletion region increases
- Capacitance decreases as the two plates move away from each other

$$C = \frac{\varepsilon A}{d}$$

ε	permittivity
A	area
d	width

Junction capacitance

C_{j0} is the zero bias junction capacitance per unit area in equilibrium



$$C_{j0} = \frac{\varepsilon_s}{w_{d0}} \text{ F/cm}^2$$

$$= \sqrt{\frac{\varepsilon_s q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{V_{\text{bi}}}} \text{ F/cm}^2$$

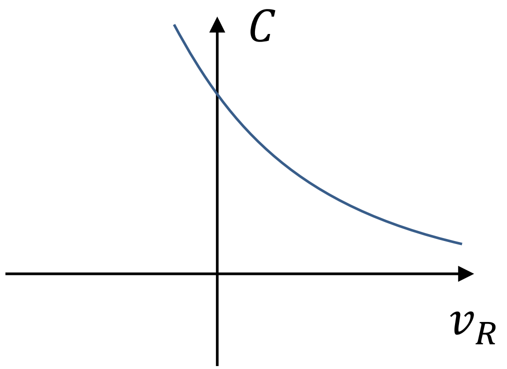
Junction capacitance

- By varying V_R, the depletion width changes, changing its capacitance value
- The PN junction is therefore, actually a voltage-dependent capacitor

Capacitance vs. bias voltage:

$$C_j = \frac{\varepsilon_s}{w_d} \text{ F/cm}^2$$

$$C_j = \frac{\varepsilon_s}{w_{d0}\sqrt{1+\frac{v_R}{V_{\text{bi}}}}} = \frac{C_{j0}}{\sqrt{1+\frac{v_R}{V_{\text{bi}}}}} \text{ F/cm}^2$$



Junction capacitance

- Capacitance of the junction per unit area (F/cm^2)

$$C_j = \frac{C_{j0}}{\sqrt{1+\frac{v_R}{V_{bi}}}}$$ ← Important to remember

where V_{bi} = built-in potential

v_R = reverse bias voltage

C_{j0} = capacitance at zero bias (V_R=0)

$$C_{j0} = \sqrt{\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{V_{bi}}}$$

where ε_{si} = dielectric constant of Si $(11.7 \times 8.85 \times 10^{-14} F/cm^{10})$

Example

A *pn* junction is doped with $N_A = 2 \times 10^{16}$ cm^{-3} and $N_D = 9 \times 10^{15}$ cm^{-3}. Determine the capacitance of the device with (a) $V_R = 0$ and $V_R = 1$V.

① Obtain the built-in potential

$$V_{bi} = \frac{kT}{q} ln \frac{N_A N_D}{n_i^2} = 0.73\ V$$

② For $V_R = 0$, solve for C_{j0}

$$C_{j0} = \sqrt{\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{V_{bi}}}$$

$$= 2.65 \times 10^{-8} F/cm^2 = 0.265\ fF/\mu m^2$$

③ For $V_R = 1$V,

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_{bi}}}}$$

$$= 0.172\ fF/\mu m^2$$

Diode I-V characteristics

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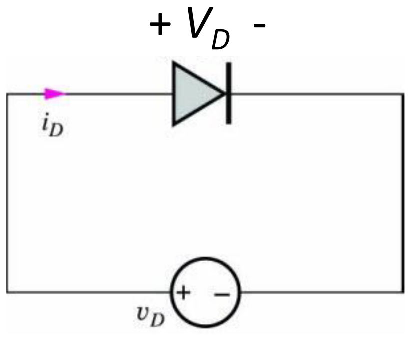
Diode I-V Characteristics

- PN Junction is a diode
  - For both forward and backward



$$i_D = I_S\left[\exp\left(\frac{qv_D}{kT}\right)-1\right] = I_S\left[\exp\left(\frac{v_D}{V_T}\right)-1\right]$$

U_T = Thermal Energy

$V_T = \frac{U_T}{q}$ = Thermal Voltage

where

	I_S	=	reverse saturation current (A)
	V_D	=	voltage applied to diode (V)
	q	=	electronic charge (1.60×10^{-19} C)
	k	=	Boltzmann's constant (1.38×10^{-23} J/K)
	T	=	absolute temperature (Kelvins)
	V_T	=	kT/q = thermal voltage (V) (25 mV at room temp.)

I_S is typically between 10^{-18} and 10^{-9} A, and is strongly temperature dependent due to its dependence on n_i^2.

Diode I-V Characteristics

- Reverse bias:

$$i_D = I_S\left[\exp\left(\frac{v_D}{V_T}\right)-1\right] \cong I_S[0-1] \cong -I_S$$

- Zero bias:

$$i_D = I_S\left[\exp\left(\frac{v_D}{V_T}\right)-1\right] \cong I_S[1-1] \cong 0$$

- Forward bias:

$$i_D = I_S\left[\exp\left(\frac{v_D}{V_T}\right)-1\right] \cong I_S \exp\left(\frac{v_D}{V_T}\right)$$

PN Junction Summary

› **Junction equation**

$$\boxed{I_D = I_S\left(\exp\frac{V_D}{V_T} - 1\right)} \qquad \boxed{I_S = Aqn_i^2\left(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right)}$$

where I_D = diode current

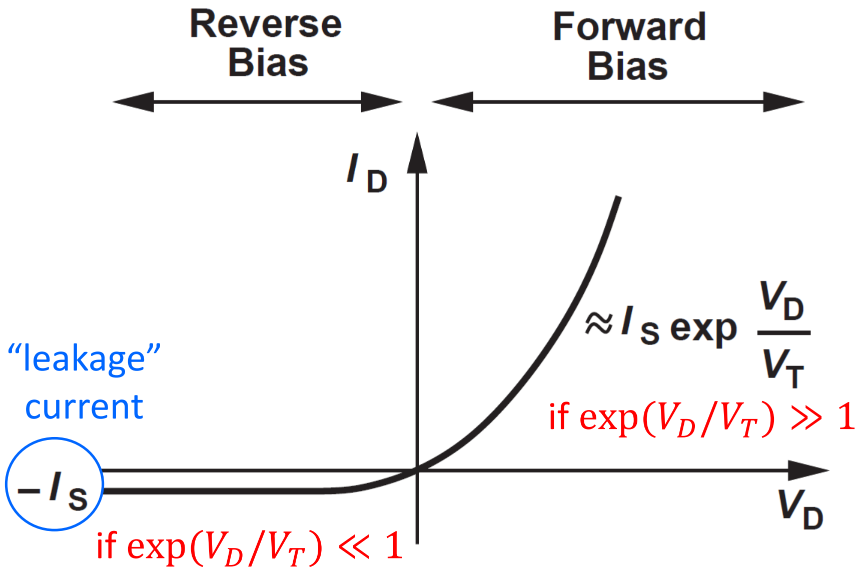
V_D = diode voltage

› **Forward bias**

- Applied voltage opposes the built-in potential
- Diffusion current is raised substantially

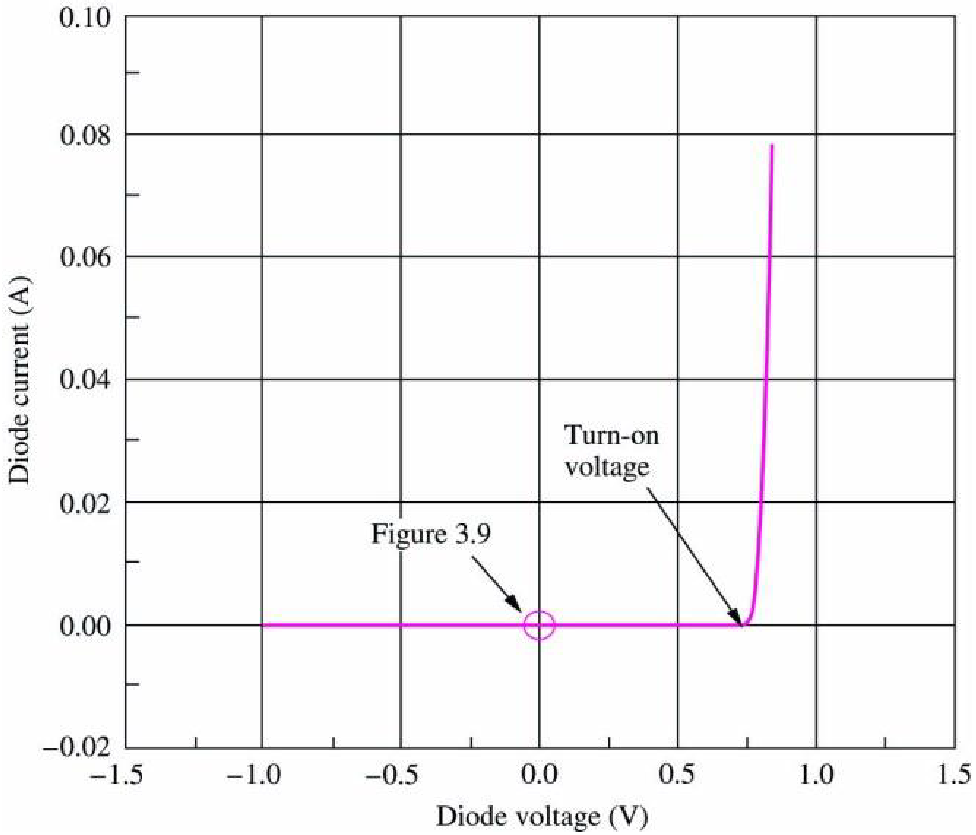
› **Reverse bias**

- Applied voltage enhances the field
- Current flow is prohibited



Diode I-V Characteristics

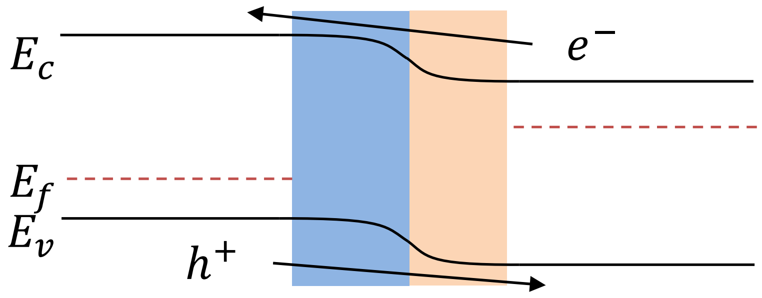
- We can plot the flow of current in response to the applied voltage
  - This is called an I-V curve

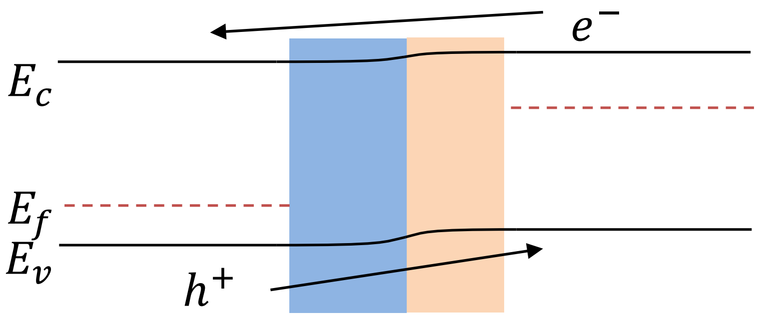


Note that the applied voltage must exceed the built-in potential before significant diffusion current can flow

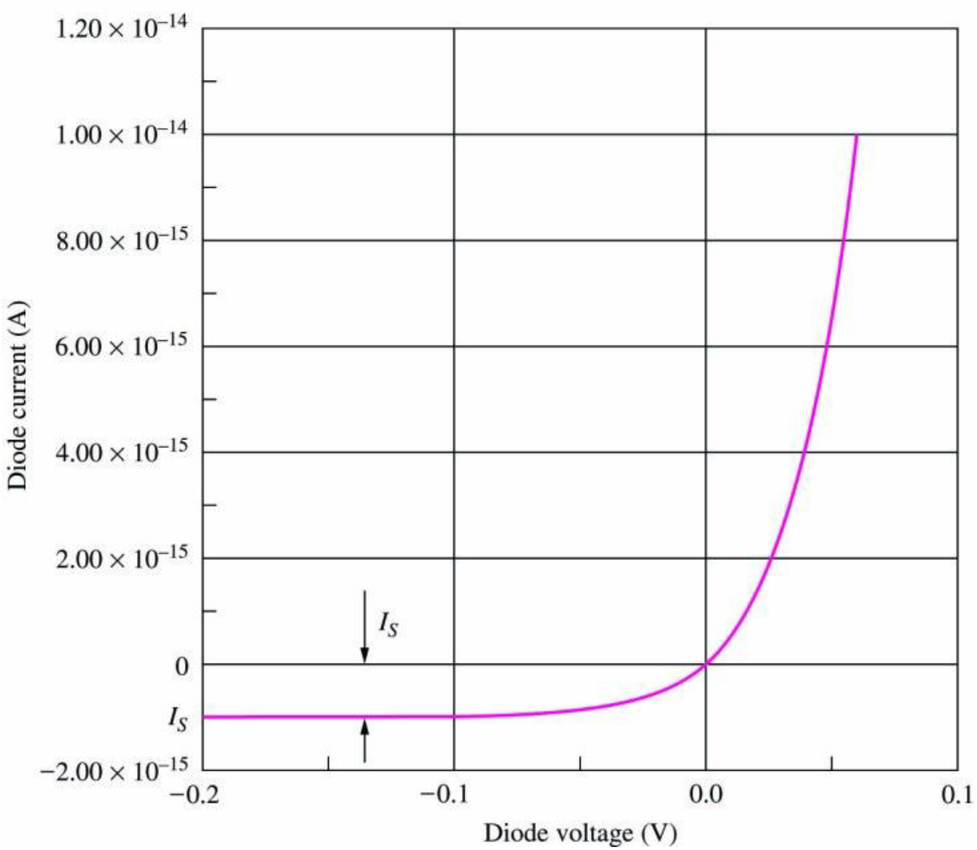
This is called the "**turn-on voltage**"

Turn-on



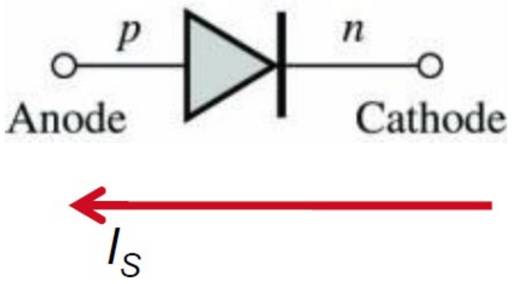


Diode I-V Characteristics



A very small amount of current I_S does flow across the diode in the reverse direction when the diode is reverse biased.

This is called the
“**reverse saturation current**”



Example

- A diode operates in the forward bias region with a typical current level. Suppose we wish to increase the current by a factor of 10. How much change in diode voltage is required?

① Express diode voltage as a function of its current

$$V_D = V_T \ln(\frac{I_D}{I_S})$$

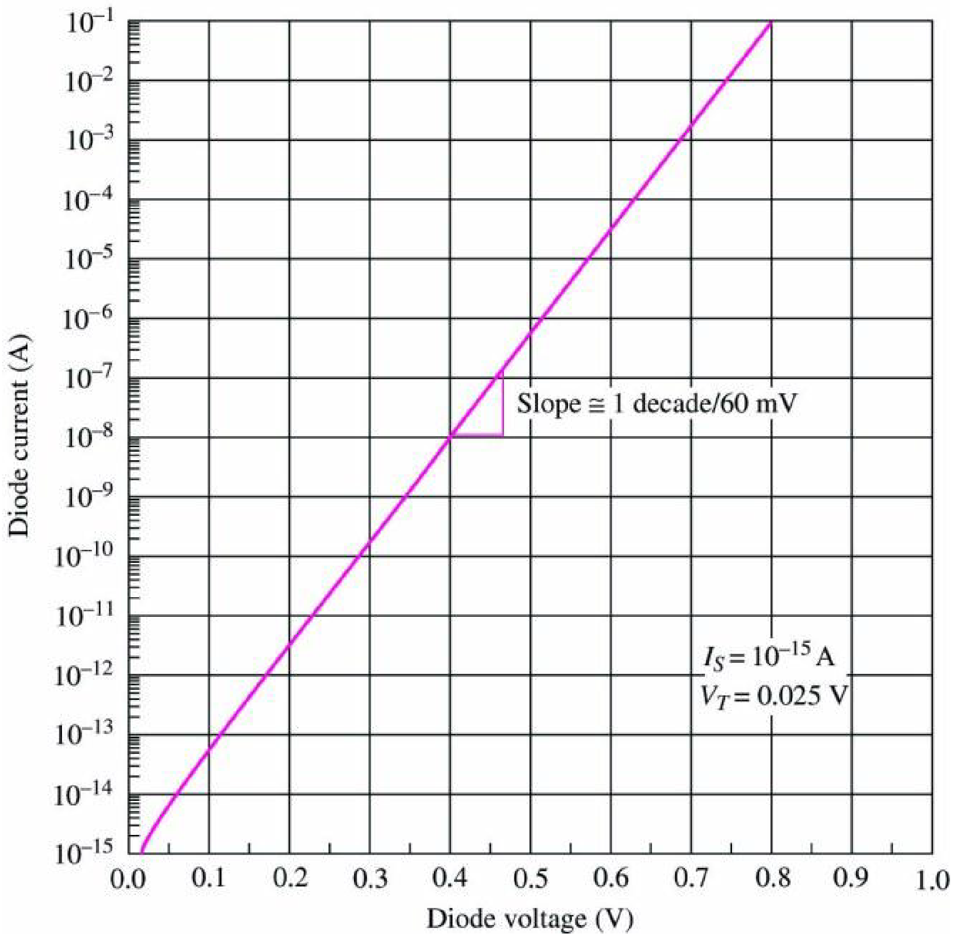
② Define $I_1 = 10\ I_D$

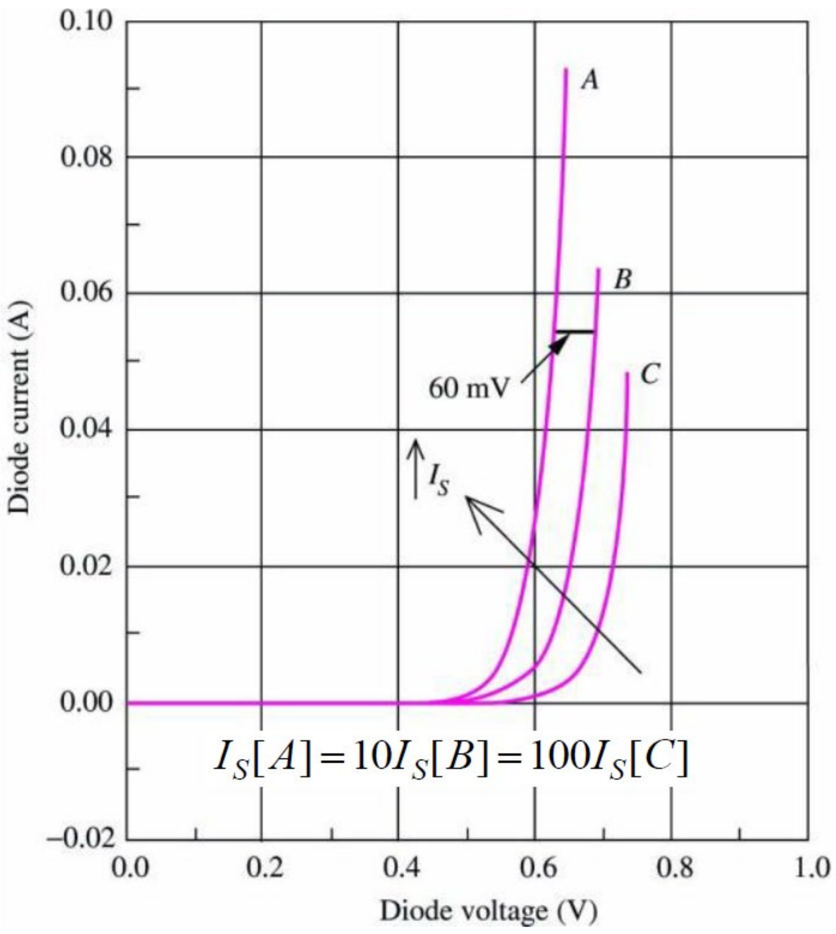
$$V_{D1} = V_T \ln(\frac{10 I_D}{I_S})$$
$$= V_D + V_T \ln(10)$$

Thus, the diode voltage must rise by V_T ln 10 ≈ 60mV (at T = 300 K)

Diode I-V Characteristics

I_S effect on diode current $\quad i_D = I_S \left[\exp\left(\frac{v_D}{V_T}\right) - \overset{\text{negligible}}{\cancel{1}}\right] \cong I_S \exp\left(\frac{v_D}{V_T}\right)$





Example

Find diode voltage for diode with given specifications, assuming the diode is operating at room temperature with V_T = 0.025 V

$$(I_S, I_D) = (0.1\text{ fA}, 300\ \mu\text{A}), (10\text{ fA}, 300\ \mu\text{A}), (0.1\text{ fA}, 1\text{ mA})$$

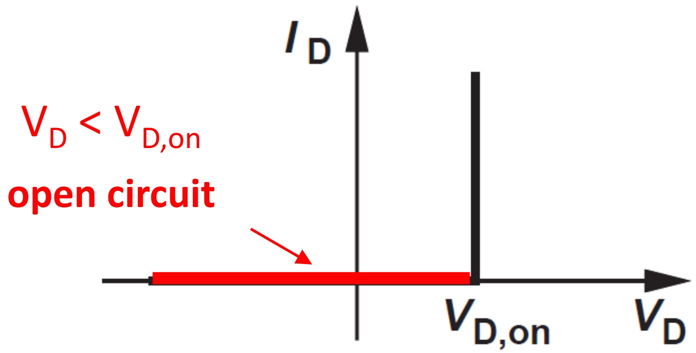
$$\text{With } I_S = 0.1\text{ fA}: \ V_D = nV_T \ln\left(1+\frac{I_D}{I_S}\right) = 1(0.025V)\ln\left(1+\frac{3x10^{-4}A}{10^{-16}A}\right) = 0.718V$$

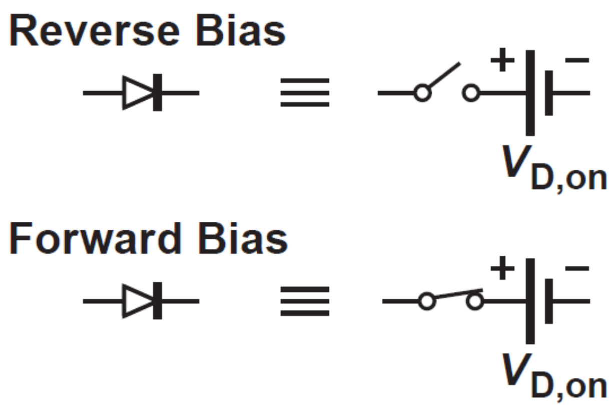
$$\text{With } I_S = 10\text{ fA}: \ V_D = (0.025V)\ln\left(1+\frac{3x10^{-4}A}{10^{-14}A}\right) = 0.603V$$

$$\text{With } I_S = 0.1\text{ fA}, I_D = 1\text{ mA}: \ V_D = (0.025V)\ln\left(1+\frac{10^{-3}A}{10^{-16}A}\right) = 0.748V$$

Constant-Voltage Model

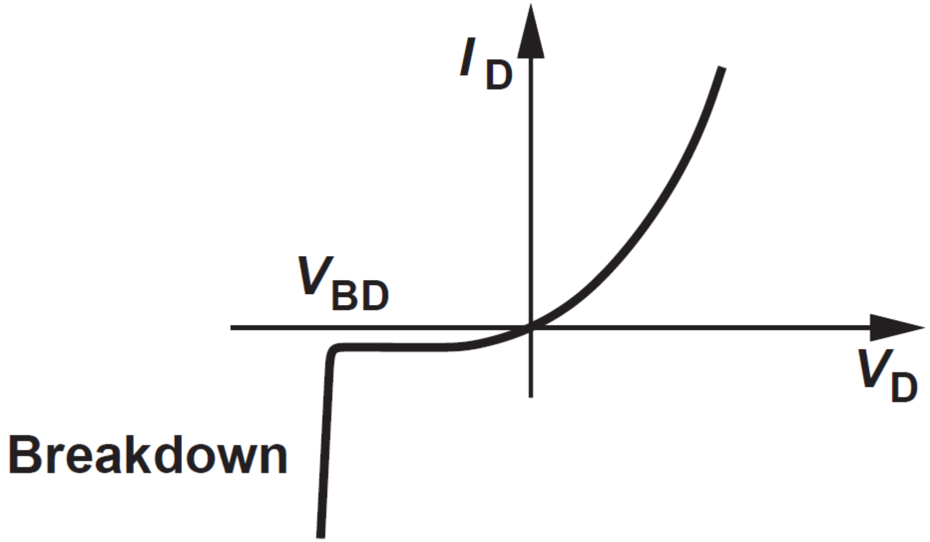
- Nonlinear equation of the exponential I/V diode model makes the analysis of circuits difficult
- Approximate forward bias voltage by a constant value
- Device is considered fully off if below this constant value
- Acts as an ideal voltage source
- $V_D < V_{D,on}$
  - open circuit





Reverse breakdown

- As the reverse bias increases, “breakdown” occurs
- A sudden enormous current is observed

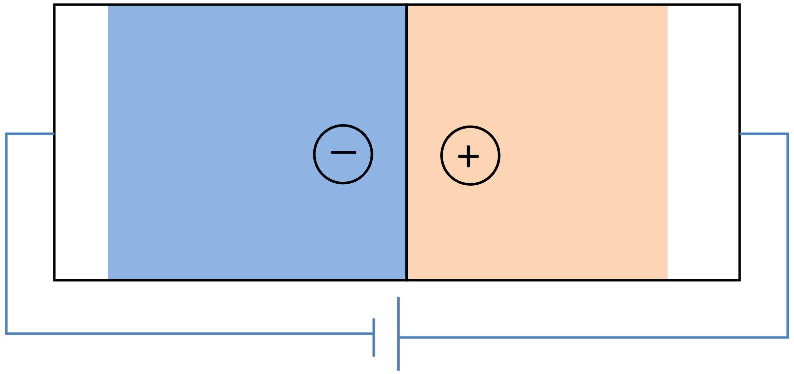


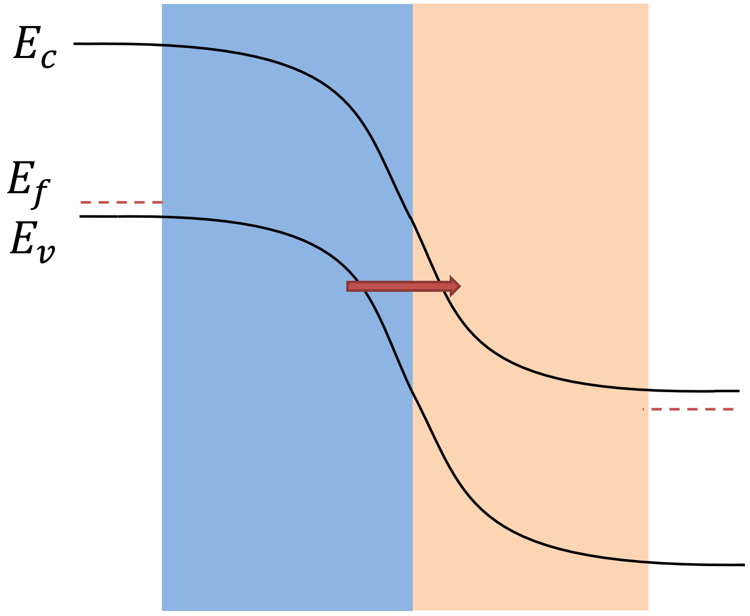
- Breakdown resulting from high voltage (high E-field) can occur in any material
- The voltage at which this occurs is the **breakdown voltage**, V_{BD}

Zener breakdown

- Occurs in heavily doped diodes
- A high E-field (10^6 V/cm) may impart enough energy to the remaining covalent electrons to tear them from their bonds
- Freed electrons are accelerated by the field and swept to the *n* side

Zener breakdown

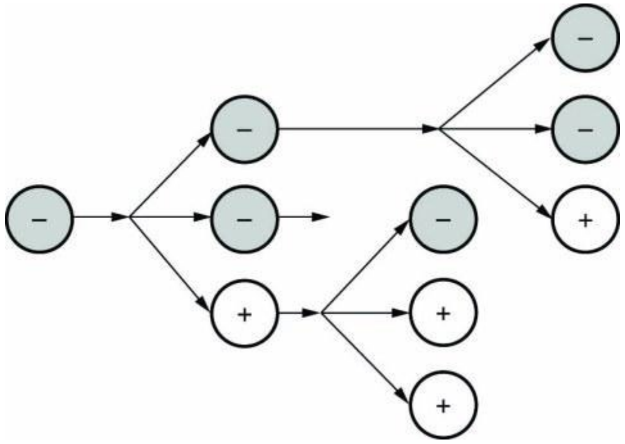




Quantum
tunnelling

Avalanche breakdown

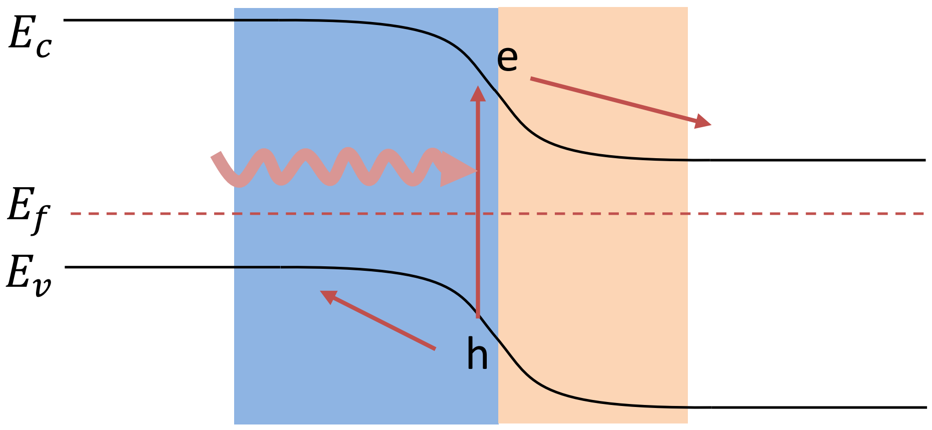
- Each carrier entering the depletion region experiences high E-field
- Large acceleration causes the carriers to gain enough energy to break the electrons from their covalent bonds
    - IMPACT IONISATION
- Each freed electron by the impact may speed itself up so much in the field as to collide with another atom with sufficient energy, thereby freeing one more covalent bond electron
    - More ionising collisions, rapidly raising the number of free carriers
- Application:
    - Avalanche photodetector (APD) for single photons (SAPD) in quantum optics



Diode optoelectronic devices

Diode photodetector

- If the depletion region of a *pn* junction diode is illuminated with light with sufficiently high frequency, photons can provide enough energy to cause electrons to jump the semiconductor bandgap to generate electron-hole pairs

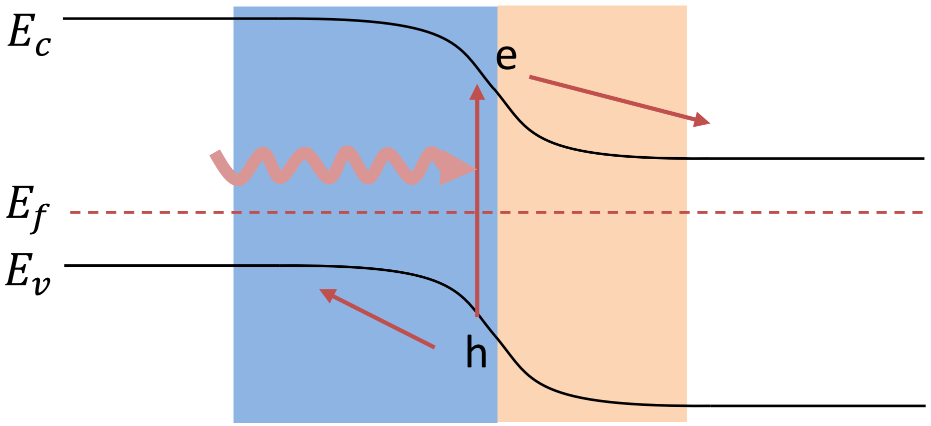


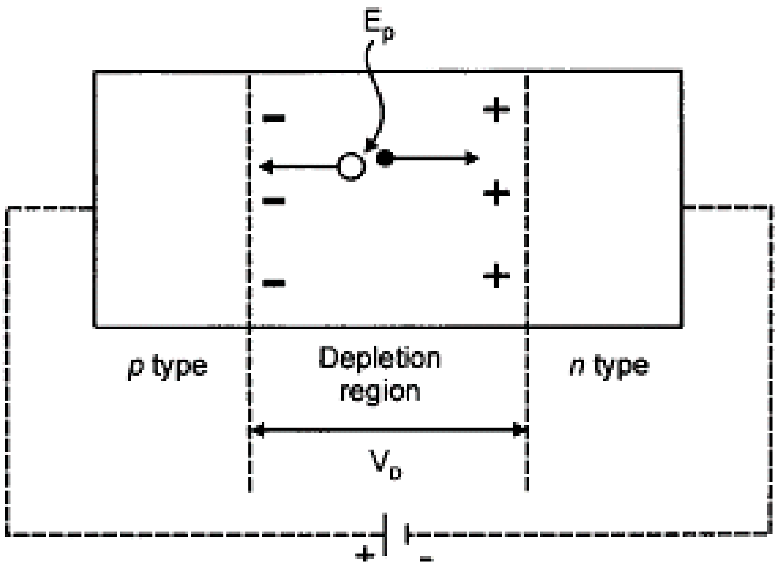
Diode photodetector

- Light absorption and emission in a semiconductor is heavily dependent on the detailed band structure of the semiconductor.
- Semiconductors for which the minimum of the conduction band occurs at the same wavevector as the maximum of the valence band have a stronger absorption of light (known as a direct band-gap versus an in-direct band-gap: Si has an indirect band-gap).

Light and Diodes

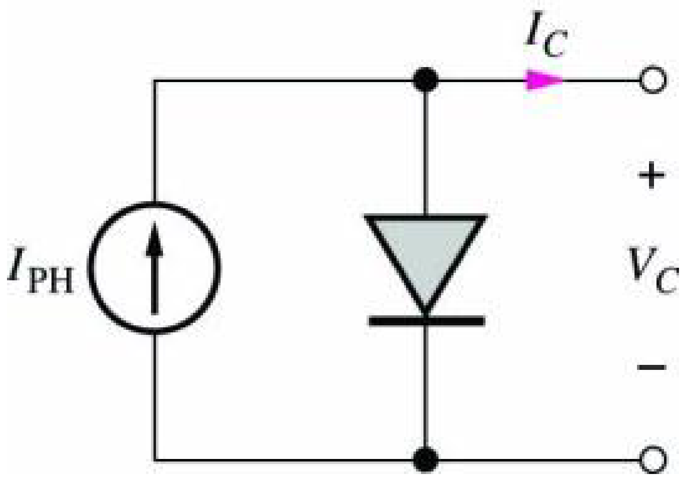
- When electron-hole pairs are generated in the depletion region, this creates a reverse current



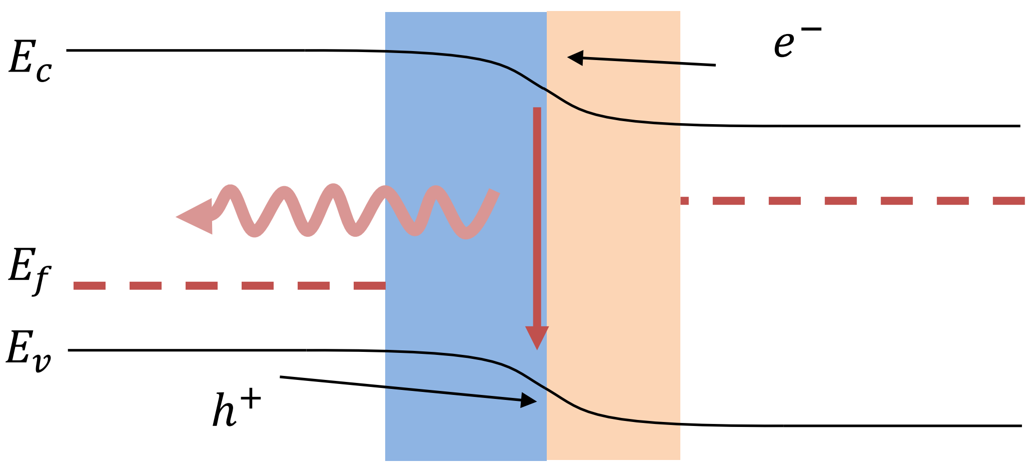


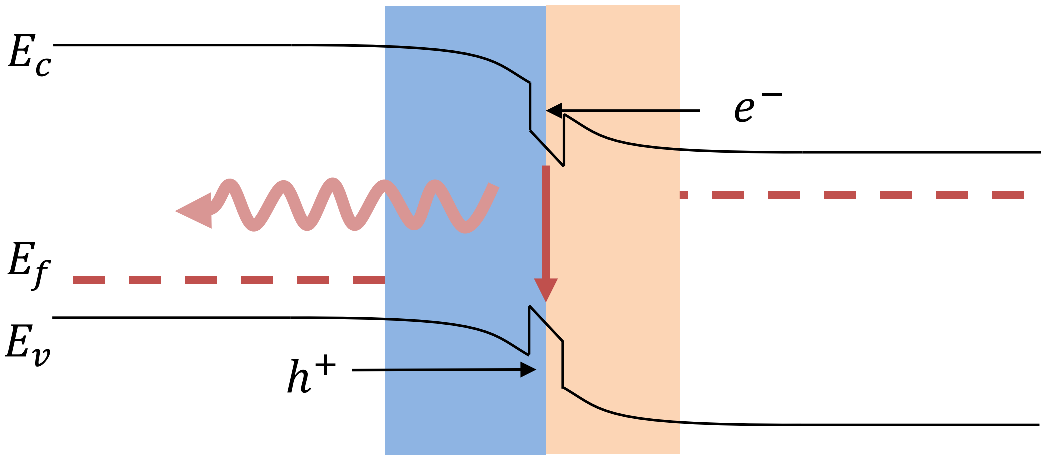
Photodiodes

- Photodiodes are operated in reverse bias because the hole-electron pairs are generated in the depletion region.
- In photodiode applications, a dc current is generated through the diode
- Photodiodes are used for cameras, remote control receivers, CD players, solar cells, pulse oximeters, and many other applications



Light-emitting Diodes



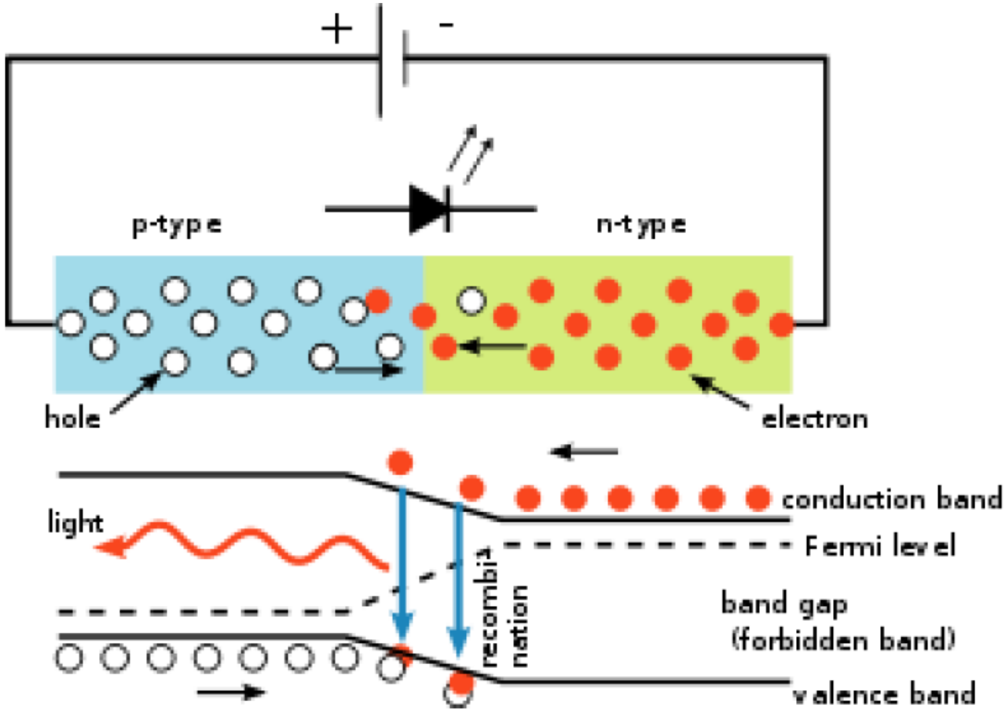


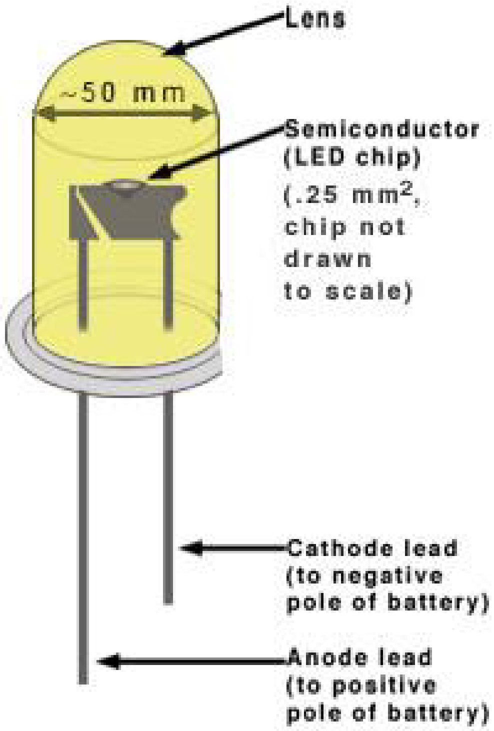
Forward biased pn-junction
Electrons and holes flow into the junction region
They can recombine to emit light

Efficiency is much improved by engineering quantum wells
Nowadays they usually have ~ 5 quantum wells

Light-Emitting Diodes (LEDs)

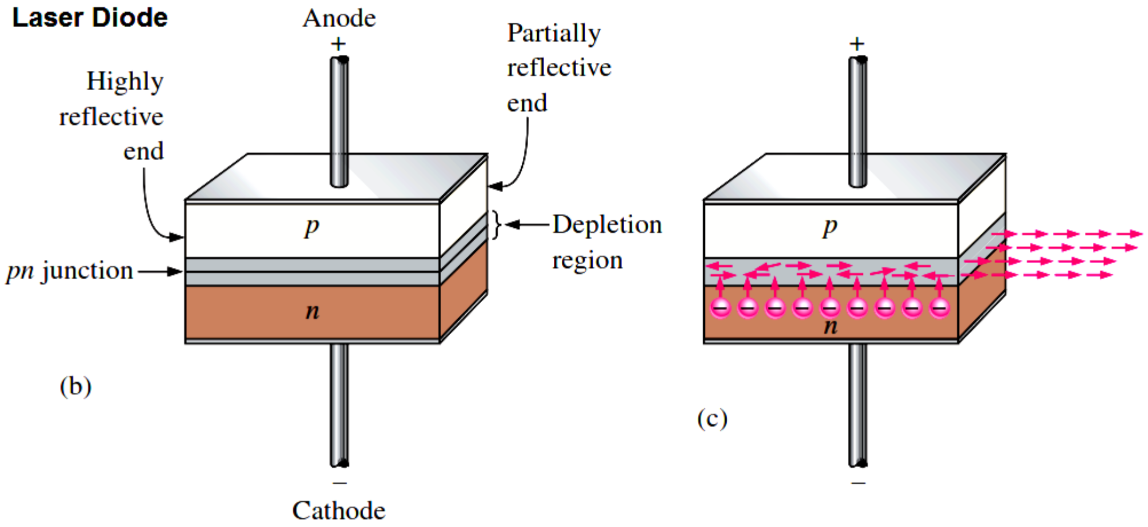
- Light-Emitting Diodes (LEDs) use recombination processes in the forward-biased *pn* junction diode to produce light.
- When a hole and electron recombine, an energy equal to the bandgap of the semiconductor is released as a photon.





Lasers

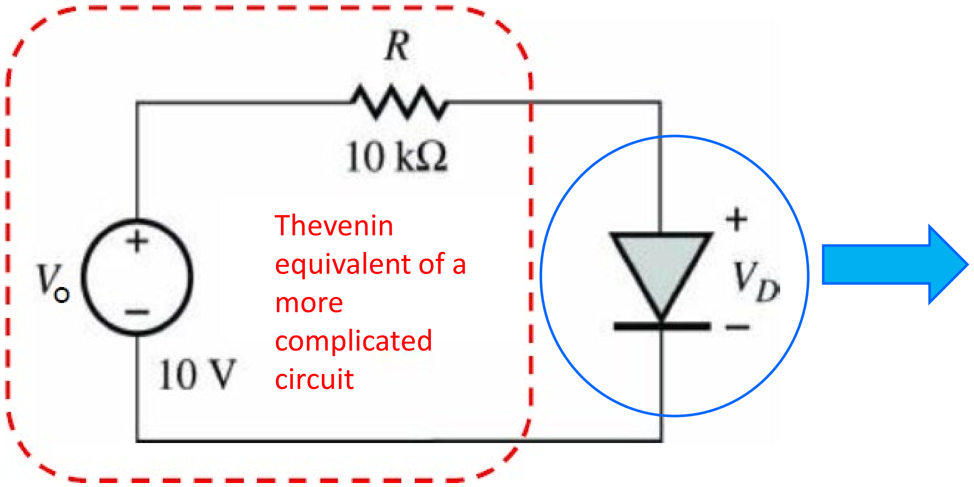
- Laser diodes also consist of a p-n diode with an active region where electrons and holes recombine resulting in light emission.
- However, a laser diode also contains an optical cavity
- The laser cavity consists of a waveguide terminated on each end by a mirror.
- Photons, which are emitted into the waveguide, can travel back and forth in this waveguide provided they are reflected at the mirrors.

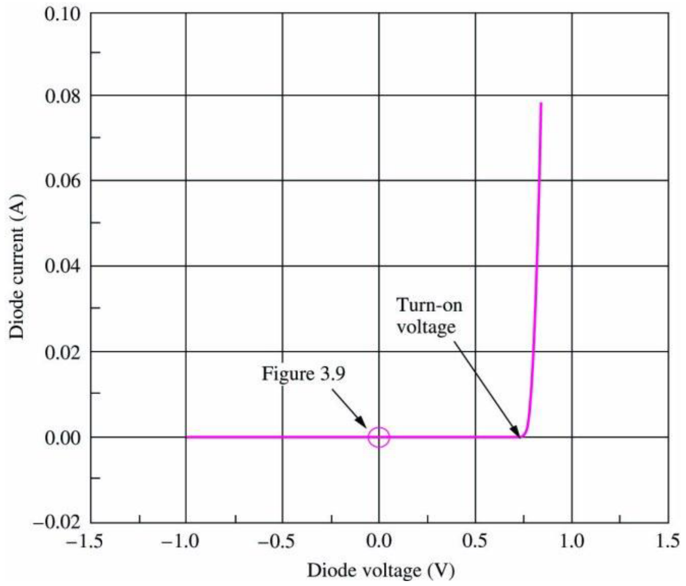


Diode circuit models

Diode Circuit Analysis

- Consider the following simplified circuit model:





Diode I-V characteristic

- Analyse loop equation:

$$V = I_D R + V_D$$

- Goal - to find the **quiescent operating point** (**Q-point**) or **bias point** for the diode
- Solving these equations gives us the Q-Point = (I_D, V_D)

Diode Circuit Analysis

- Several techniques can be used to solve for I_D and V_D
  - Mathematical Analysis using Exponential Model
  - Graphical Analysis using Load Line Approach
  - Ideal Diode Model
  - Constant-Voltage Model

Mathematical Analysis

- It is difficult to solve exponential equations by hand

$$V_0 = I_D R + V_D \qquad\qquad I_D = I_S\left[\exp\left(\frac{V_D}{V_T}\right) - 1\right]$$

$$V_0 = I_S\left[\exp\left(\frac{V_D}{V_T}\right) - 1\right] R + V_D$$

- We now need to find the zero point solution of the function

$$f = V_0 - I_S\left[\exp\left(\frac{V_D}{V_T}\right) - 1\right] R - V_D$$

- A numerical answer can be found by using Newton’s iterative method

Newton's Iterative Method

- Iterative solutions

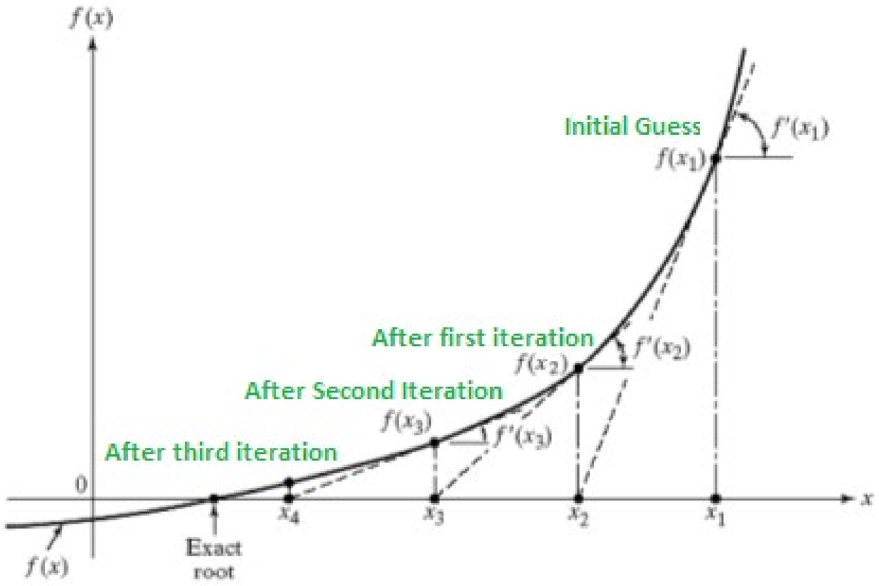
$$f = V_0 - I_S\left[\exp\left(\frac{V_D}{V_T}\right) - 1\right]R - V_D$$

Steps

1. Make an initial guess ${V_D}^0$
2. Evaluate f and its derivative f' for this value of V_D
3. Calculate new guess for V_D using

$${V_D}^1 = {V_D}^0 - \frac{f({V_D}^0)}{f\prime {V_D}^0}$$

4. Repeat steps 2 and 3 till convergence

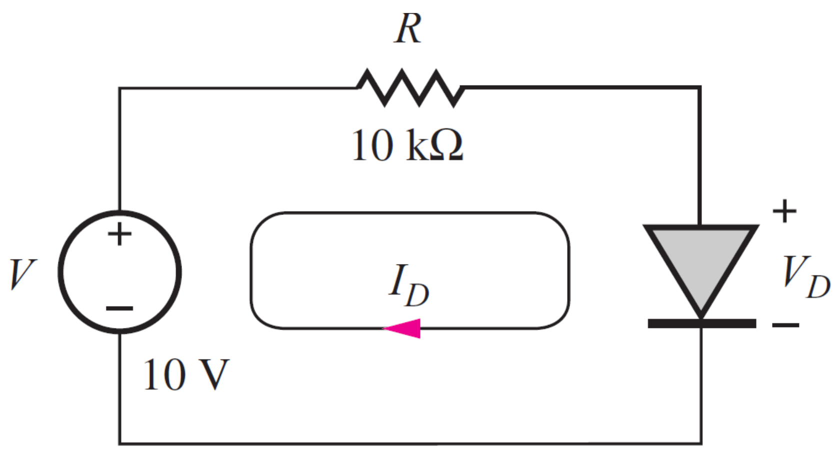


- Numerically compute using MATLAB to make things easier

Load-line Analysis

- When the I-V characteristics is given in graphical form
  - Use load-line analysis (graphical approach) to solve

$$V = I_D R + V_D$$ (**load line** for the diode)

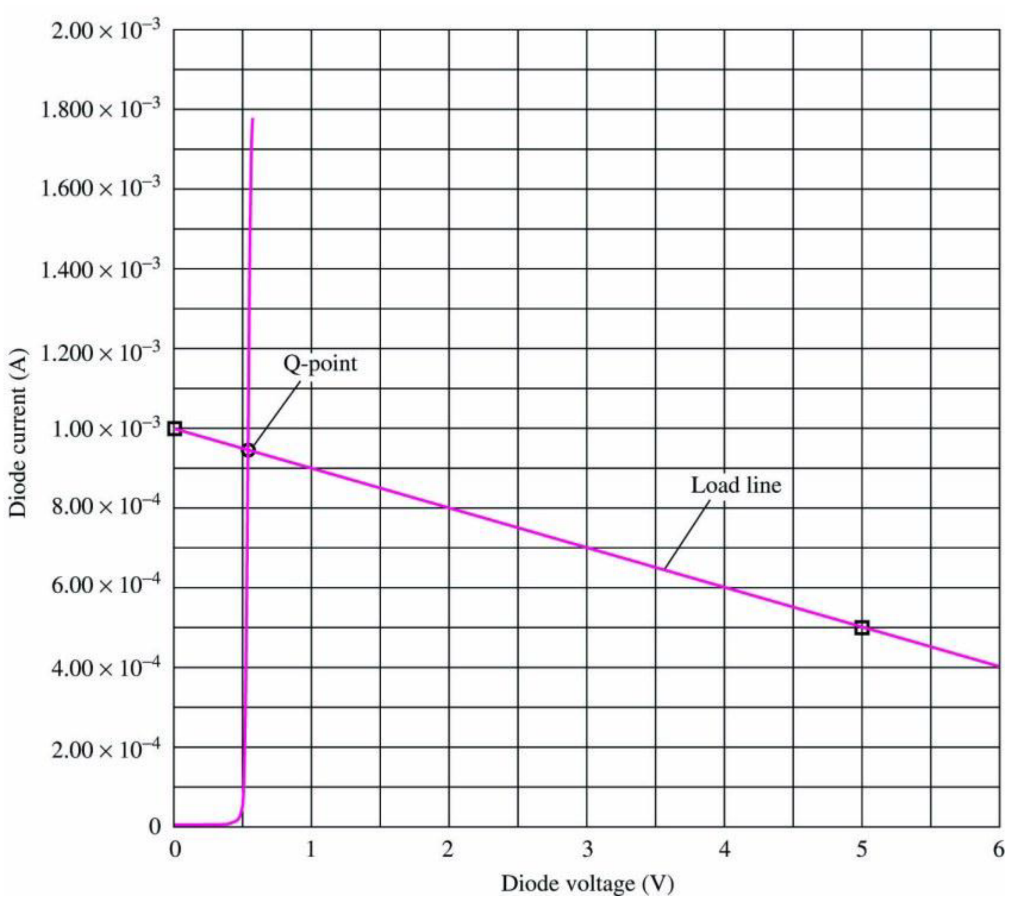


Step 1:
Transform circuit to a Thévenin equivalent with the diode as the output load

Step 2:
Write the load line equation for V_D in terms of I_D

$$V_D = V - I_D R$$

Load-line Analysis



Q-point = (0.95 mA, 0.6V)

Step 3:

Find 2 points to plot the load line

Step 4:

Plot the diode I-V curve

$$I_D = I_S\left[\exp\left(\frac{V_D}{V_T}\right) - 1\right]$$

Step 5:

The Q-point is the intersection of the load line and I-V curve

Ideal Diode Model

- Significant tolerances exist for sources and passive components.
  - We need answers precise to only 2 or 3 significant digits
- Many circuits can be analyzed using a simpler model
- We can simplify the model further to just a switch

Ideal diode model

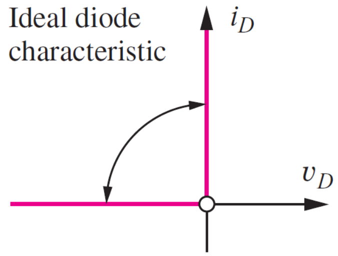
- The *I-V* characteristic for the **ideal diode** consists of two straight-line segments
- Forward biased
  - Positive current, V_D is zero

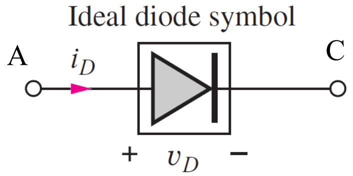
$$V_D = 0 \quad for\ I_D > 0$$

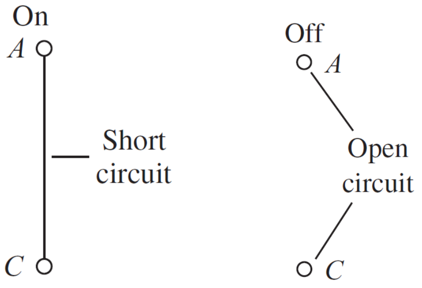
- Reverse biased
  - $V_D < 0$, then the current I_D is zero

$$I_D = 0 \quad for\ V_D \leq 0$$

- Two states
  - Conducting – ON – short circuit
  - Non-conducting – OFF – open circuit



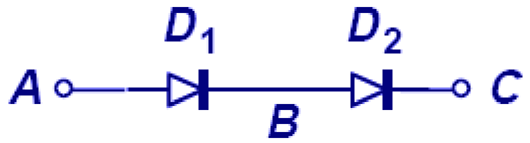




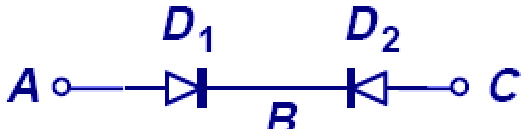
Exercise

- Diodes can be placed in series (or in parallel). Determine which one of the configurations in Fig. 3.4 can conduct current

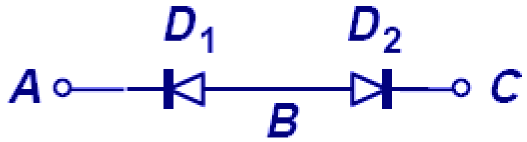
I



II

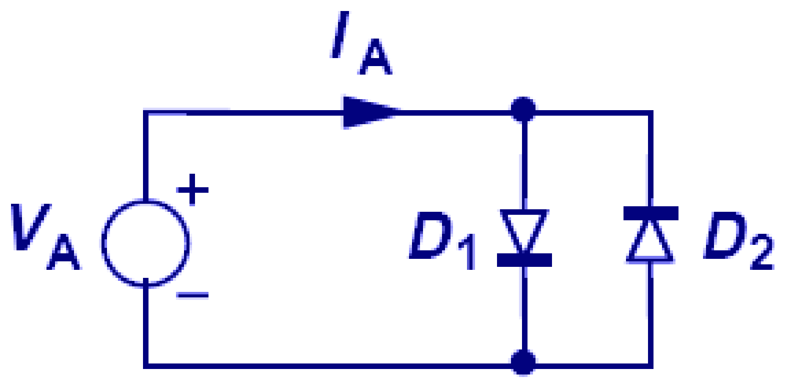


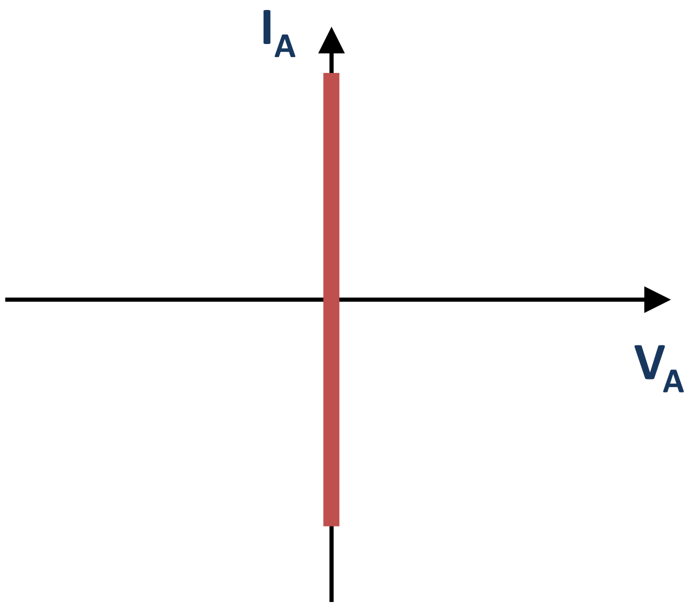
III



Exercise

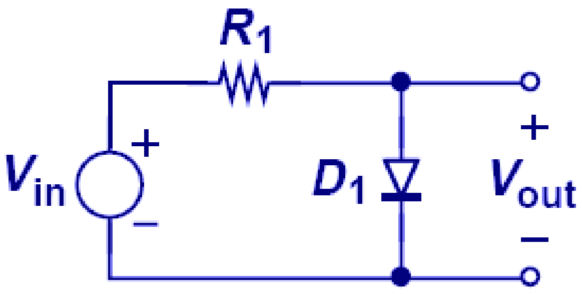
- Plot the I/V characteristic for the following diode configuration





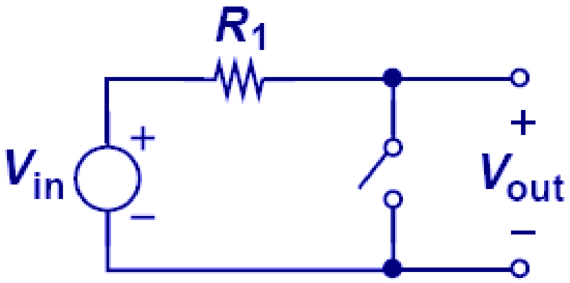
Ideal Diodes in Resistor Circuits

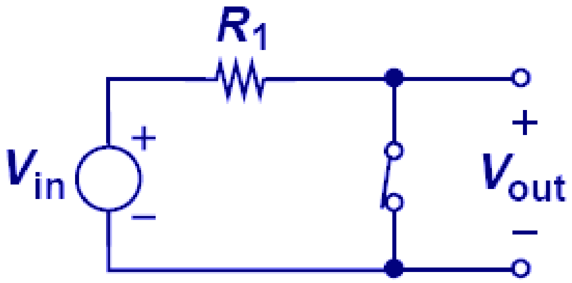
- The ideal diode model assumes zero voltage drop across the diode when it is on, and zero current through the diode when it is off



- When V_{in} is less than zero, the diode opens, so $V_{out} = V_{in}$
- When V_{in} is greater than zero, the diode shorts, so $V_{out} = 0$

$V_{in} < 0$

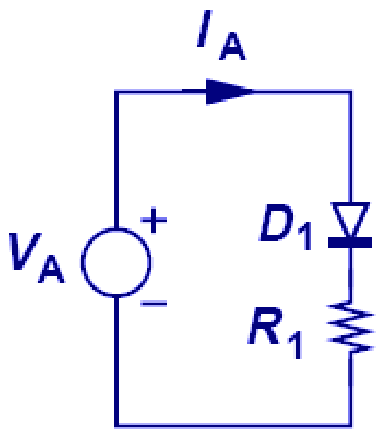


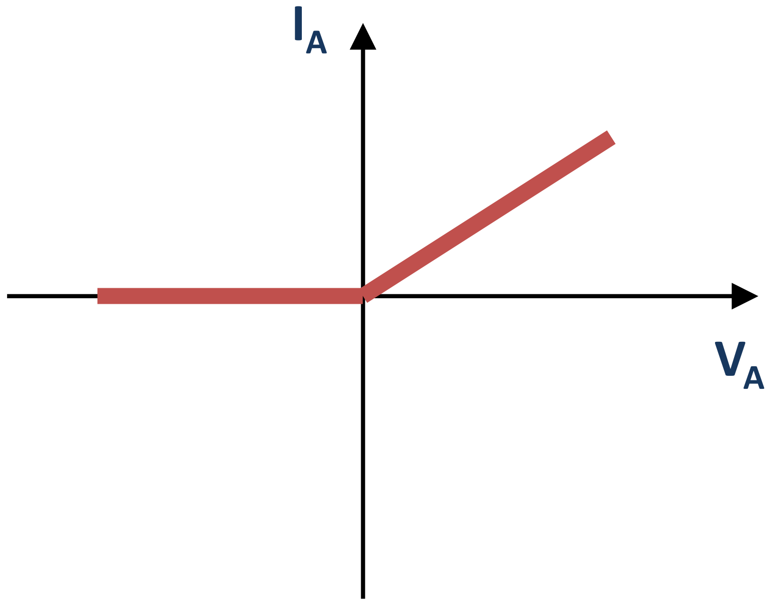


$V_{in} > 0$

Exercise

- Plot the I/V characteristic for the following diode-resistor configuration





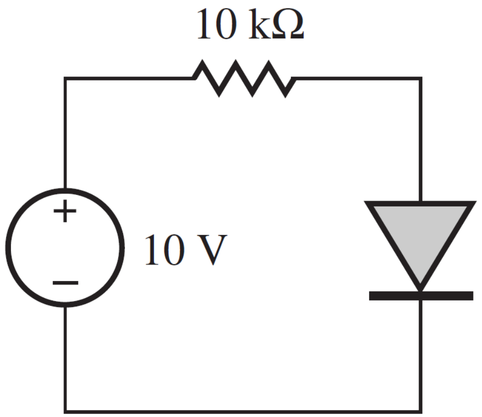
Analysis using Ideal Diode Model

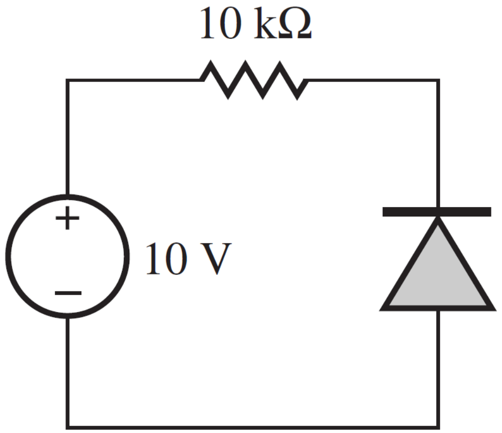
Steps

1. Identify anode and cathode of the diode and label V_D and I_D
2. Guess diode's region of operation from circuit.
    - Which diode is forward or reverse biased?
3. Analyze circuit using ideal diode model to verify assumed region of operation.
    - Redraw the circuit diagram based on assumption
4. Check results to check consistency with assumptions.
    - Does your assumption makes sense? If not, go back to Step 2.
5. Calculate Q-point using the constant-voltage or exponential diode models.

Example

- Find the Q-point for the following circuits by assuming an ideal diode model.





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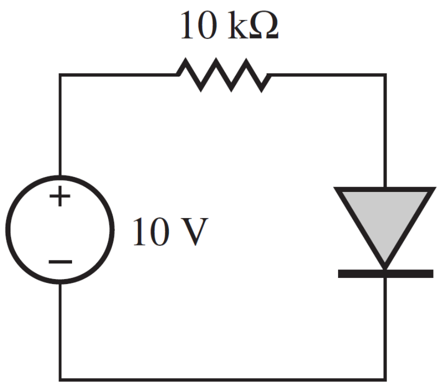
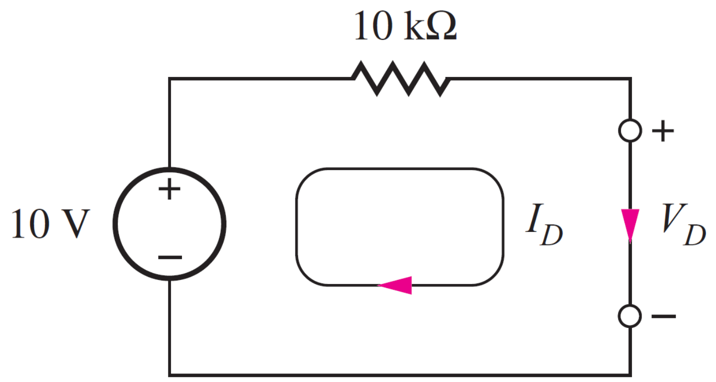




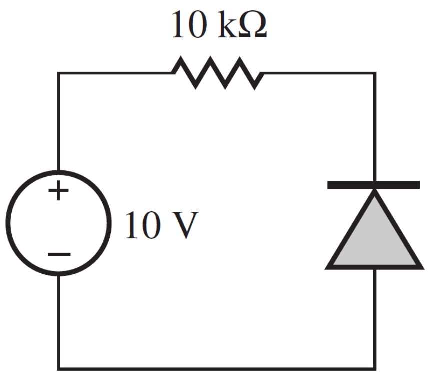
- Since source appears to force positive current through diode, assume diode is on

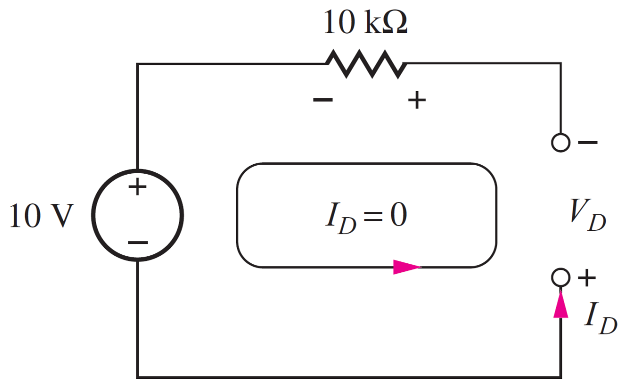
$$I_D = \frac{(10-0)V}{10k\Omega} = 1mA$$

- Because I_D is greater than 0, the assumption was correct
- Q-point = (1mA, 0V)

Example

- Find the Q-point for the following circuits by assuming an ideal diode model.





- Since source is forcing current backward through diode, assume diode is off

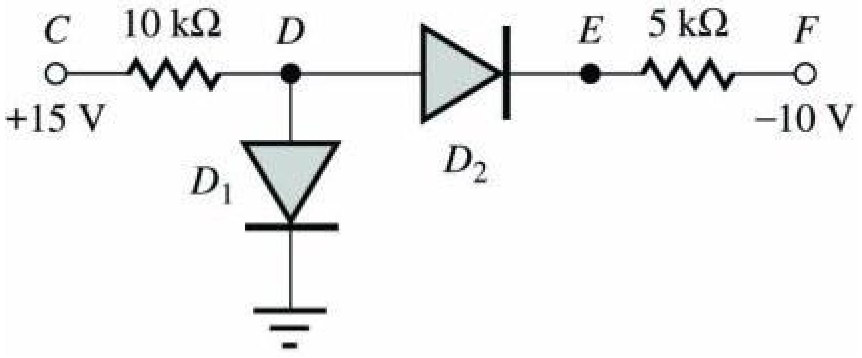
$$10 + V_D + 10^4 I_D = 0$$
$$V_D = -10V$$

- Because $V_D < 0$, the assumption was correct
- Q-point = (0, -10V)

Two-Diode Analysis

- The ideal diode model can be used to analyze circuits with more than one diode

Example: The 15-V source appears to force positive current through *D*1 and *D*2, and the -10-V source is forcing positive current through *D*2. Assume both diodes are on.



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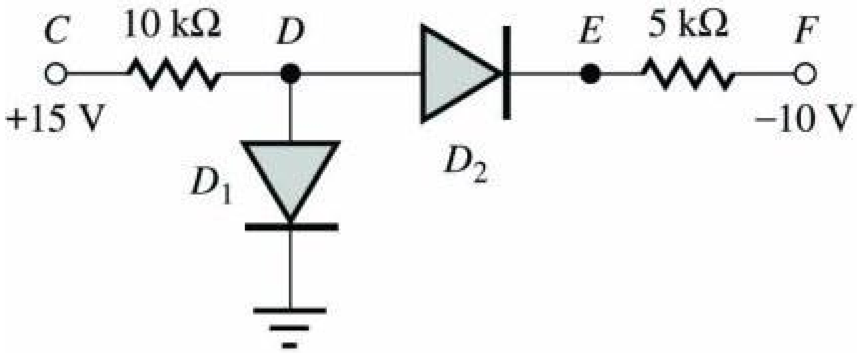
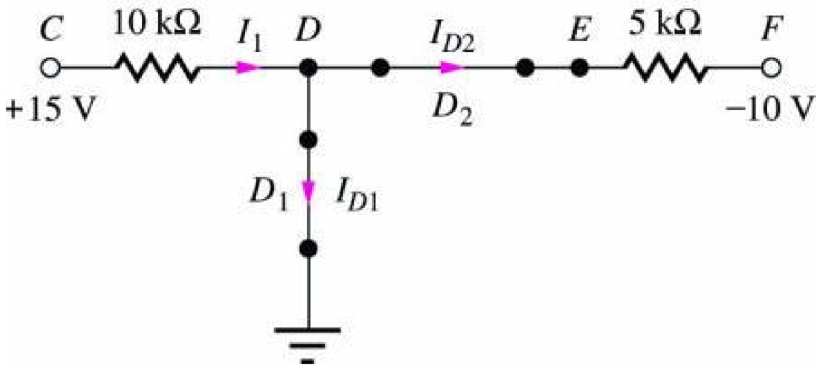




$$I_1 = I_{D1} + I_{D2}$$

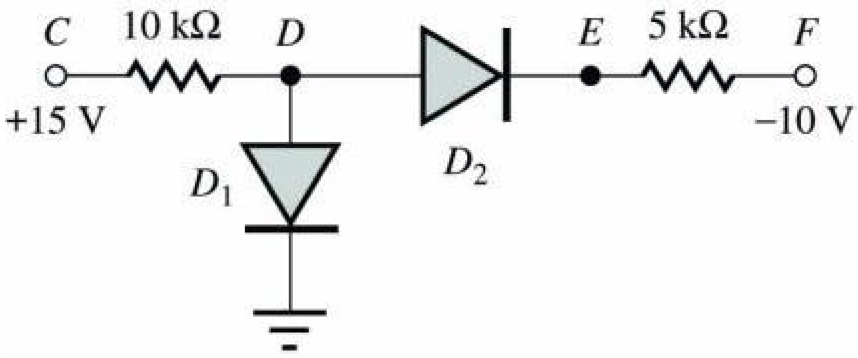
$$I_1 = \frac{(15-0)V}{10k\Omega} = 1.50\,mA$$

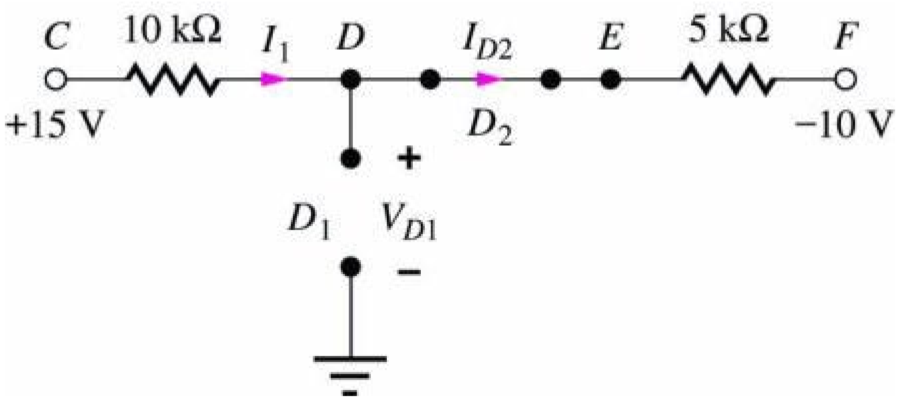
$$I_{D2} = \frac{0-(-10V)}{5k\Omega} = 2.00\,mA$$

$$I_{D1} = 1.50 - 2.00 = -0.500\,mA$$

Two-diode Analysis

Let’s try again!
ID1 < 0 is not allowed. Thus, assume *D*1 off and *D*2 on.





Then, $I_{D2} = I_1$.

$$15 - 10{,}000 I_1 - 5{,}000 I_{D2} - (-10) = 0$$

$$I_1 = \frac{25V}{15{,}000\Omega} = 1.67\ mA$$

$$V_{D1} = 15 - 10{,}000 I_1 = 15 - 16.7 = -1.67\ V$$

Q-Points
D_1 : (0 mA, -1.67 V): off
D_2 : (1.67 mA, 0 V): on

Results are consistent with the assumptions.