Lab 5: MOSFETS

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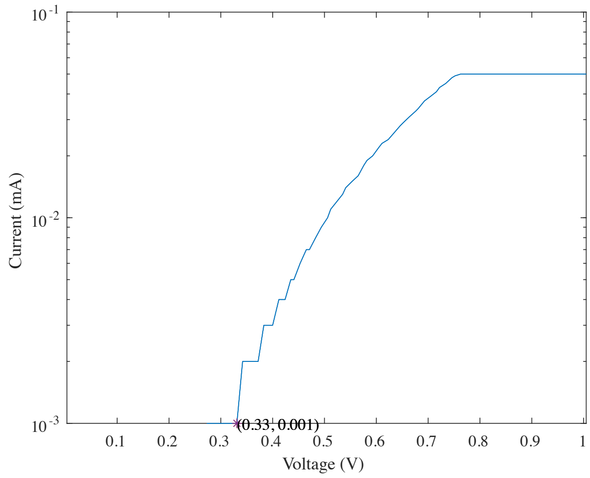
Part 1

According to the data sheet of the ALD1105, V_{GS} is when $I_D = 1\mu A$.
The transistor is forced into saturation by connecting the drain and gate.
When $I_D = 1\mu A$:

$$V = 0.33V$$

From the data sheet the ALD1105 has a low threshold voltage of 0.7V. Therefore, falling within the range specified.



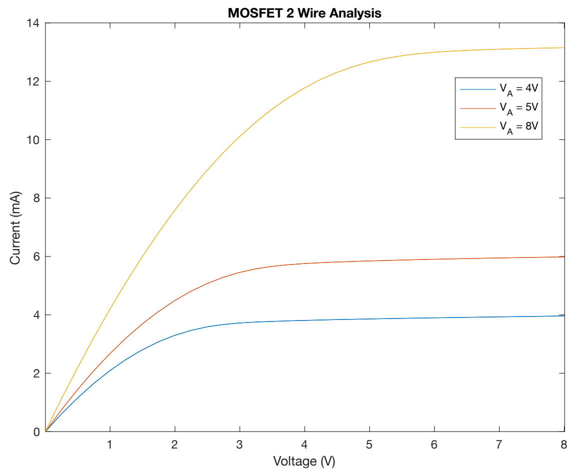
Part 2

Values of V_{PS} tried: $5V, 4V, 8V$

For the triode region: $V_{DS} < V_{GS} - V_m$

For the saturation region: $V_{DS} > V_{GS} - V_{TH}$

Regions of MOSFET:
Amplifier: Occurs during saturation region as only region with linear I-V characteristics that can be used for amplification.
Switch: Occurs during the triode region.



Part 3

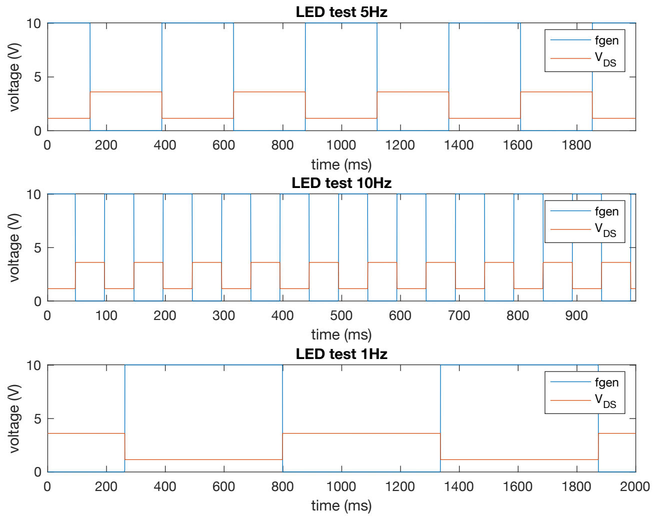
With the given circuit, the MOSFET acts as a switch as it is in the triode region.
V_{GS} is used to control I_D which in turn controls the LED.
$V_{in} = V_{FG}$
$V_{out} = V_D$

Via KVL:

$$V_D = V_{dc} - I_D - R_D - V_{LED}$$

If V_{in} is low, $V_{GS} < V_{TH}$. This results in the MOSFET being turned off, I_D is almost zero.
If V_{in} is high, $V_{GS} > V_{TH}$. This results in the MOSFET being turned on, as I_D increases, V_D decreases.

The LED is on during the triode region and off during the saturation region according to the obtained graph.



Part 4

Assuming $V_{DD1} = V_{DD2} = 5V$, $I_{ref} = 0.25mA$, $I_{ref} = \frac{V_{DD1} - V_{GS}}{R_{ref}}$, $V_t = 0.7V$ and $K_n \frac{W}{L} = 1mA/V^2$. V_{GS} can be calculated from:

$$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_t)^2$$

Which can then be used to calculate R_{ref}:

$$R_{ref} = 14.4kOhms$$

For the circuit we used

$$R_{ref} = 15kOhms$$

as it was the closest resistor available.

The I_0 current measured:

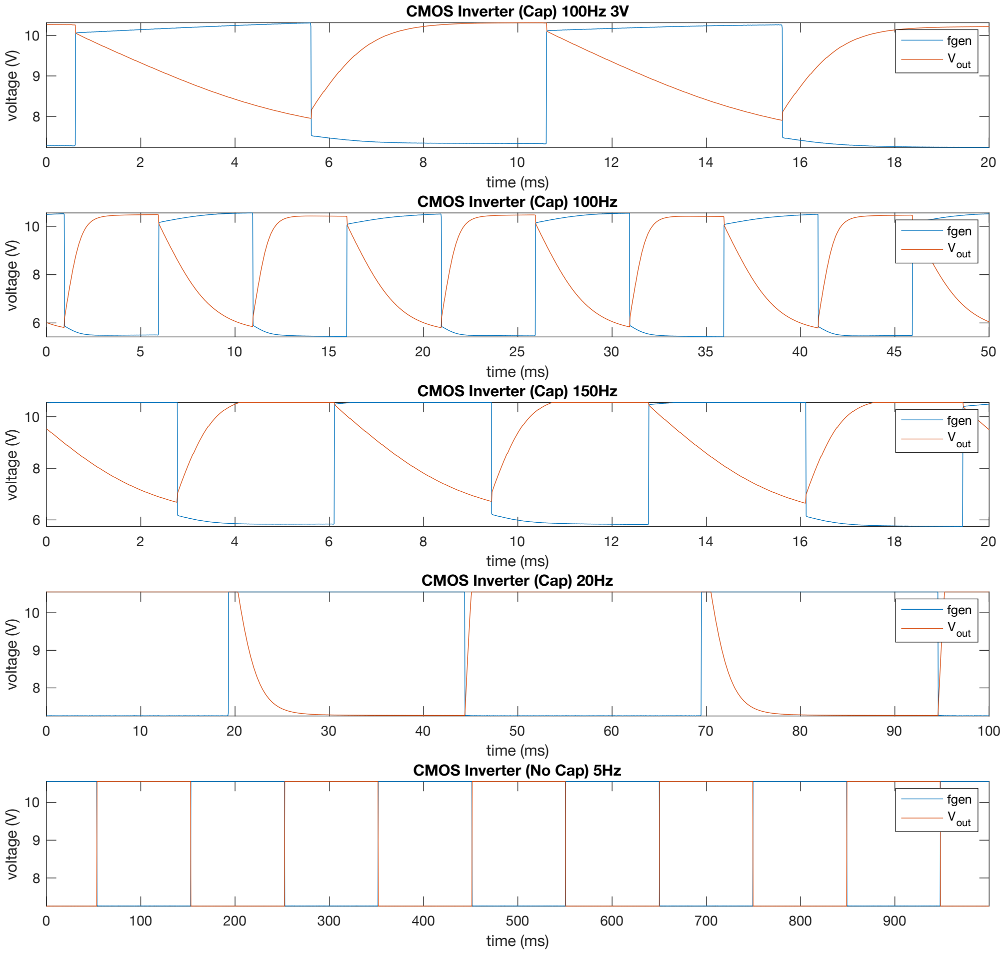
$$I_0 = 0.19mA$$

The voltage and hence current measured across the resistor:

$$V_{ref} = 4.24V$$

$$i_{ref} = 0.28mA$$

Part 5



The inverter has trouble completing high to low and low to high transitions when the frequency increases to around 100Hz. The happens due to the added capacitor, the capacitor does not have adequate time to charge and discharge as the frequency is too fast. V_{DD} determines the low-to-high delay and high-to-low delay of the inverter as it determines the value of V_{out} according to the following theory:
If V_{in} is V_{high}, $V_{in} = V_{DD}$, therefore:

$$V_{SG} = V_{DD} - V_{DD} = 0$$

$$V_{GS} = V_{DD} - 0 = V_{DD} > V_{TH}$$

Therefore N-MOS is turned on, P-MOS is off. Therefore:

$$V_{out} \rightarrow zero$$

If V_{in} is V_{low}, $V_{in} = 0$, therefore:

$$V_{SG} = V_{DD} - 0 = V_{DD} > V_{TH}$$

$$V_{GS} = V_D - GND = 0 < V_T$$

Therefore P-MOS is turned on, N-MOS is off. Therefore:

$$V_{out} \rightarrow V_{pp}$$