ELEC2104 – Lecture 08

BJT Amplifiers, MOSFET

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4-resistor biasing: example

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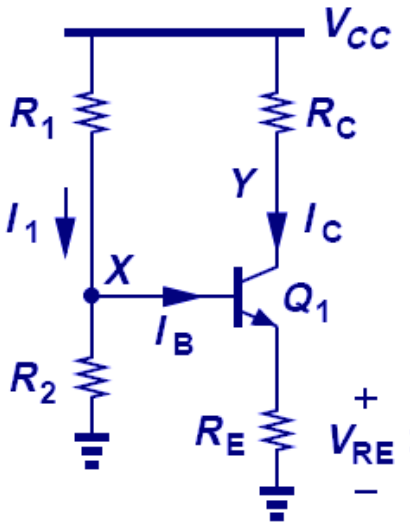
Design of Four-Resistor Bias Network: Example

- Design 4-resistor bias circuit with given parameters: I_C = 750 µA, β_F = 100, V_{CC} = 15 V, V_{CE} = 5 V. Assume we need to operate in forward-active region, V_{BE} = 0.7V
  - Let V_E = 5 V, V_C = 10 V
  - Divide (V_{CC} - V_{CE}) between R_E and R_C.

$$\alpha = \frac{\beta_F}{\beta_F + 1} = 0.99 \longrightarrow I_E = \frac{I_C}{\alpha} = 757\ \mu A$$

$$R_E = \frac{V_E}{I_E} = 6.60\ k\Omega$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = 6.67\ k\Omega$$



Design of Four-Resistor Bias Network: Example

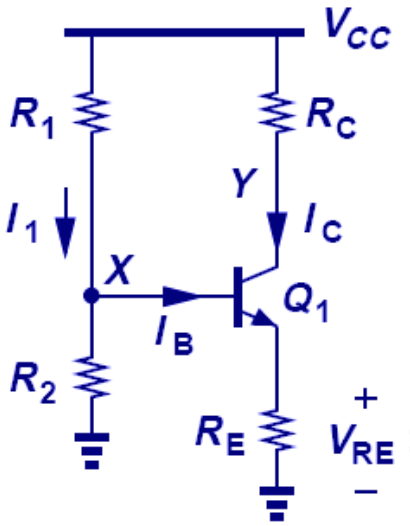
- Design 4-resistor bias circuit with given parameters: I_C = 750 µA, β_F = 100, V_{CC} = 15 V, V_{CE} = 5 V. Assume we need to operate in forward-active region, V_{BE} = 0.7V
  - Set $I_1 = 10I_B$ and $I_2 = 9I_B$

$$I_B = \frac{I_C}{\beta_F} = 7.5\mu A$$

$$V_B = V_E + V_{BE} = 5.7\ V$$

$$I_1 = 10I_B = 75\ \mu A \longrightarrow R_2 = \frac{V_B}{I_2} = 84.4\ k\Omega$$

$$I_2 = 9I_B = 67.5\ \mu A \longrightarrow R_1 = \frac{V_{CC} - V_B}{I_1} = 124\ k\Omega$$



Two-resistor biasing

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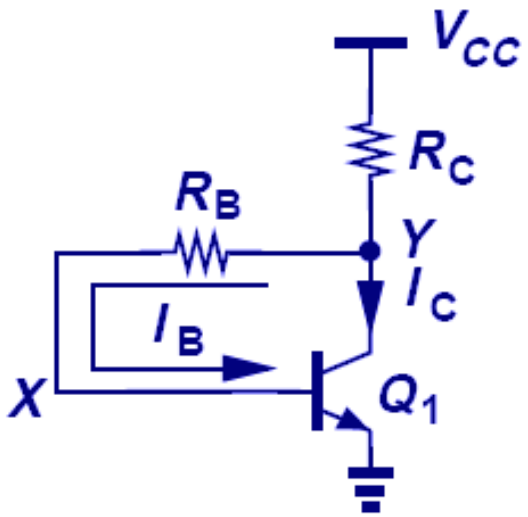
Two-resistor biasing (with collector-to-base feedback resistor)

- We can self-bias a transistor to force it into forward-active operation (guaranteed)
  - With R_B, the collector must be at a higher potential than the base
  - If BE junction is off (hence BJT is in cutoff), then $V_X = V_Y = V_{CC}$, hence $V_{BE} = V_X > V_{on}$
  - The transistor hence must be in forward-active operation.
- The collector voltage provides the necessary V_x and I_B.



$$V_Y = V_{CC} - I_E R_C = V_{CC} - I_C(1 + 1/\beta)R_C$$
$$V_Y = I_B R_B + V_{BE} = \frac{R_B I_C}{\beta} + V_{BE}$$

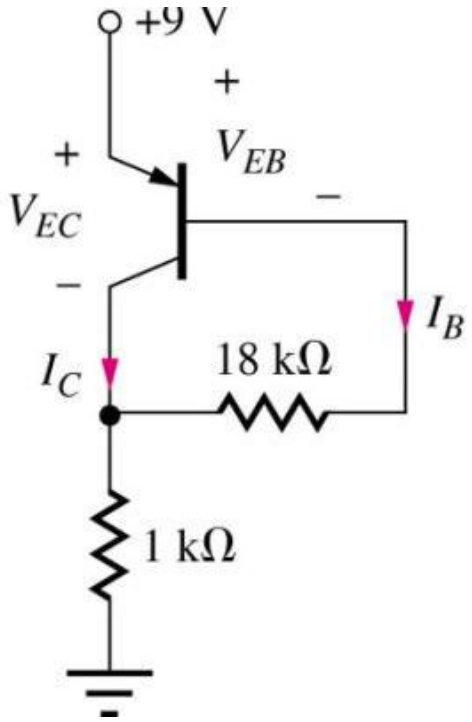
$$\Rightarrow I_C = \frac{V_{CC} - V_{BE}}{(1 + 1/\beta)R_C + R_B/\beta}$$

$R_C \gg \frac{R_B}{\beta}$ provides insensitivity of Q-point (I_C) to β

$\Delta V_{BE} \ll V_{CC} - V_{BE}$ provides insensitivity of Q-point (I_C) to variation in ΔV_{BE}

Two-Resistor Bias Network Analysis: Example

- Find Q-point for pnp transistor in a two-resistor bias circuit with β_F= 50, V_{CC}= 9 V. Assume it is in forward-active operation, so V_{EB} = 0.7 V.



Analysis is the same as for a npn transistor

Apply Kirchoff's Voltage Law:

$$-V_{CC} + V_{EB} + V_{BC} + V_C = 0$$

$$V_{EB} + 18\,000 I_B + 1000(I_C + I_B) = 9$$

$$V_{EB} + 18\,000 I_B + 1000(51) I_B = 9$$

Two-Resistor Bias Network Analysis: Example

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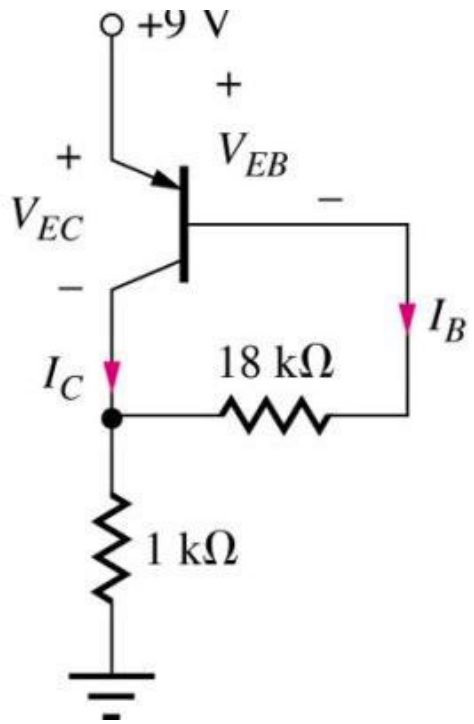


$$V_{EB} + 18\,000 I_B + 1000(51) I_B = 9$$

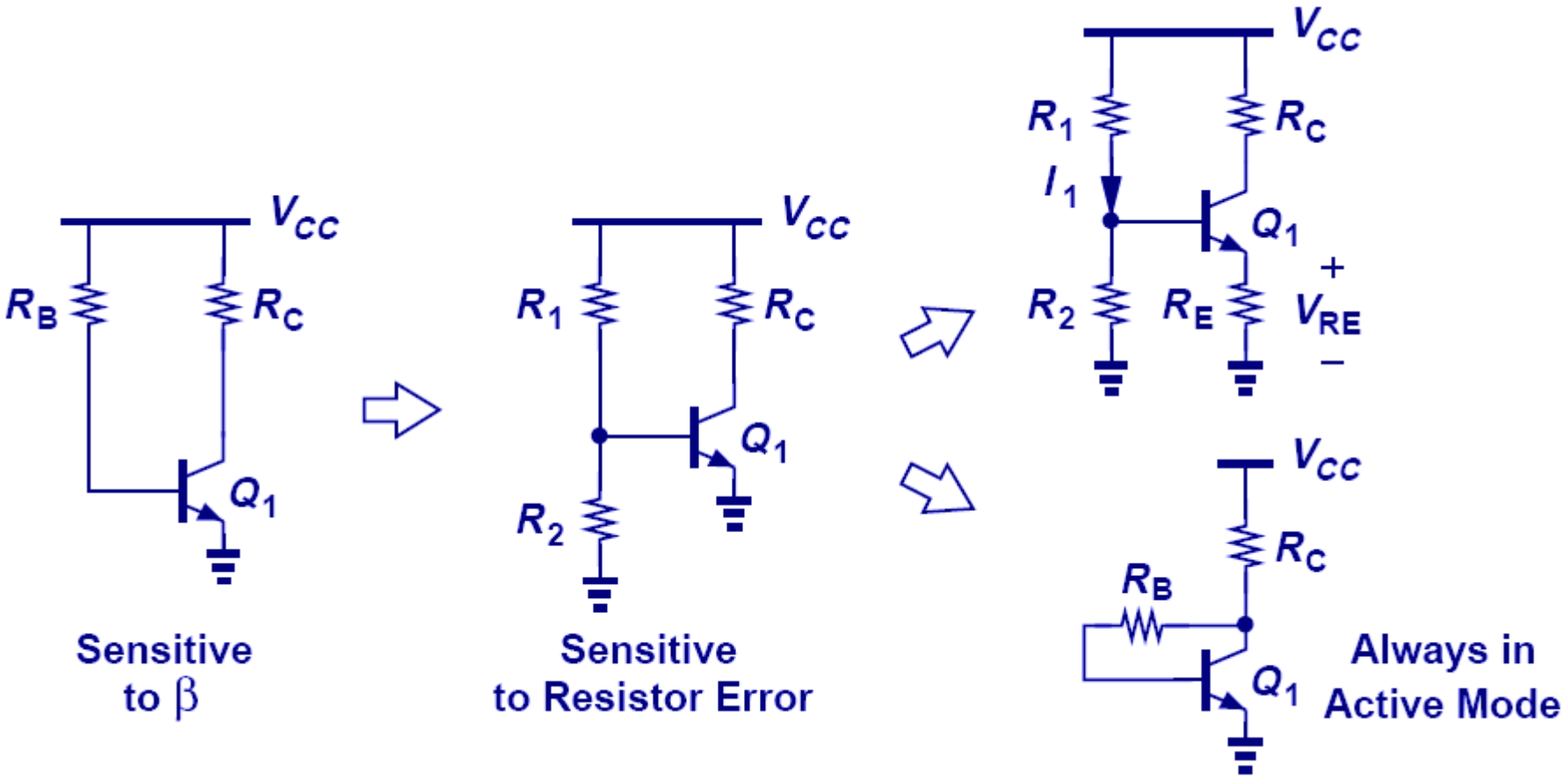
$$I_B = \frac{9\ V - 0.7\ V}{69\,000\ \Omega} = 120\ \mu A$$

$$I_C = 50 I_B = 6.01\ mA$$

$$V_{EC} = 9 - 1000(I_C + I_B) = 2.88\ V$$

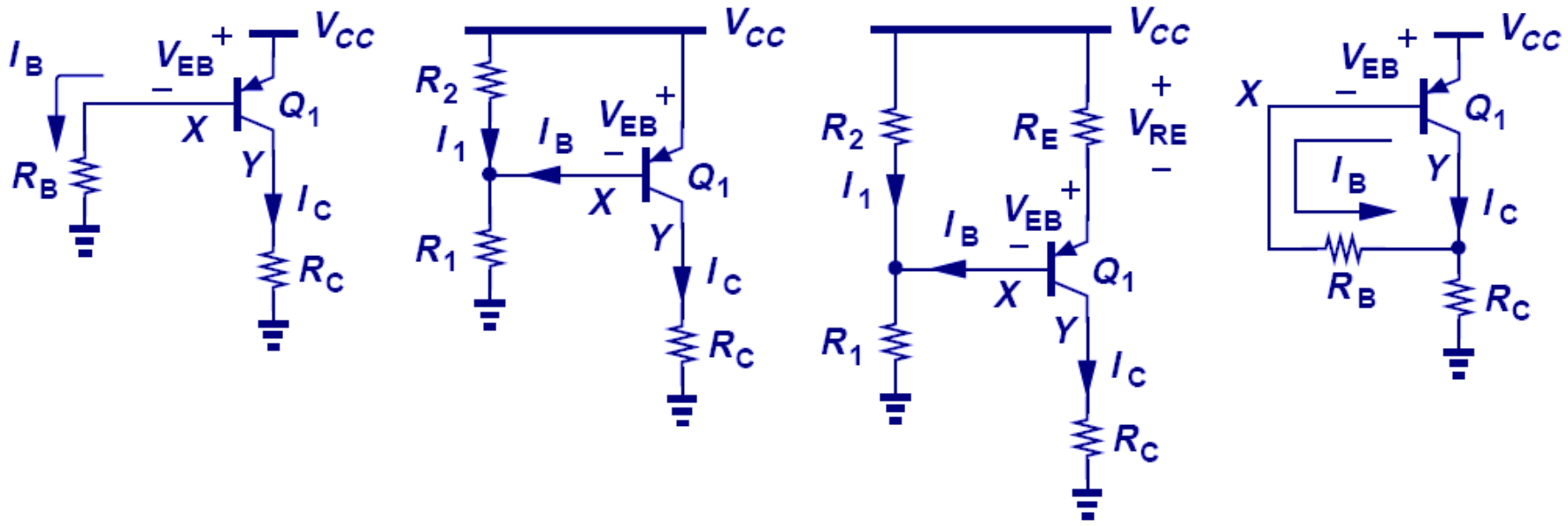
Q-point is : (6.01 mA, 2.88 V)

Summary of Biasing Techniques



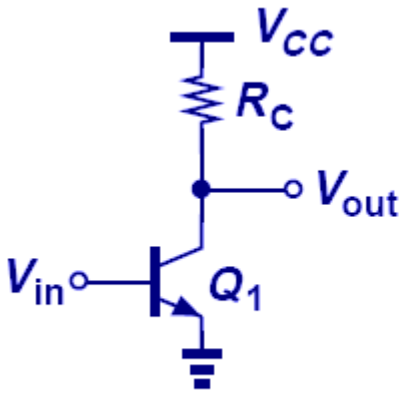
PNP Transistor Biasing

- Exact same principles, exact same design techniques
- Pay attention to direction of voltage and current

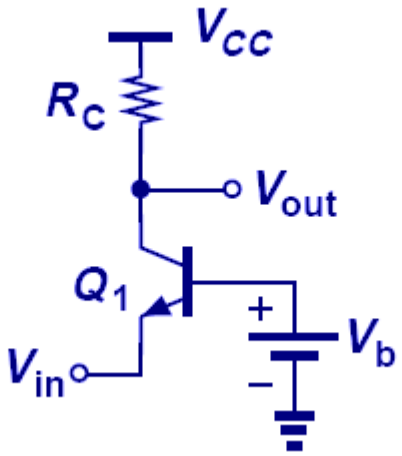


BJT amplifier topologies

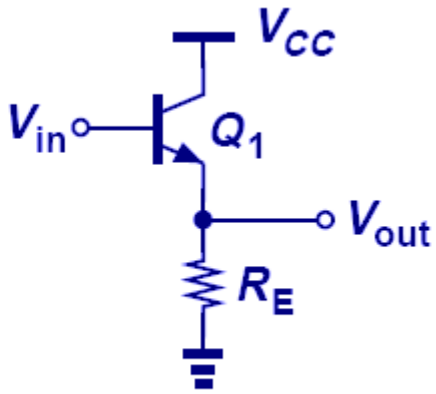
BJT Amplifier Topologies



Common-Emitter



Common-Base



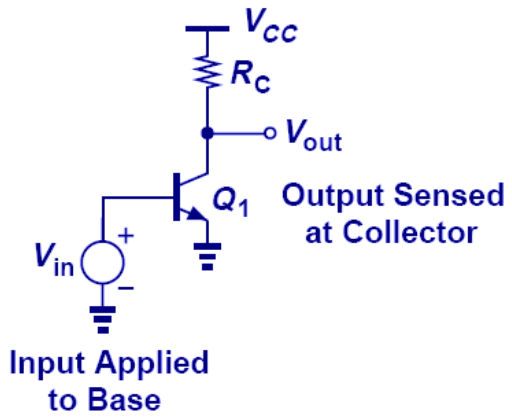
Emitter-Follower

- These are the most useful configurations
- All of v_{out}, v_{in} are small signals (on top of V_C, V_B etc.). Assuming we have biased the BJT correctly.

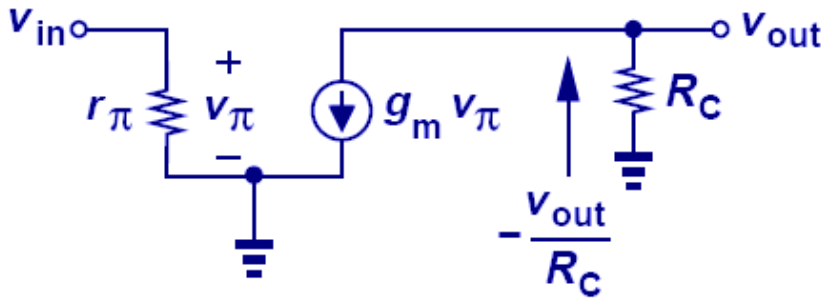
"Common": which terminal is common between input and output signals

Common-Emitter Amplifier

- Gain of amplifier – Voltage gain



$$r_\pi = \frac{\beta}{g_m} \qquad g_m = \frac{I_c}{V_T}$$



$$A_V = \frac{v_{out}}{v_{in}}$$

$$-\frac{v_{out}}{R_C} = g_m v_\pi = g_m v_{in}$$

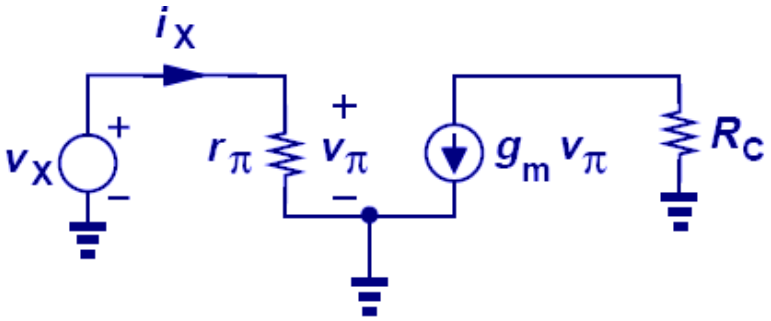
$$\boxed{A_V = -g_m R_C}$$

Common-Emitter Amplifier

- Input/Output Impedance
  - Determines the capability to interface with preceding and following stages
  - When measuring the output impedance, the input port has to be grounded so that V_{in} is grounded, i.e. we don't care whatever circuit was connected to B. (again, this is the small signal circuit)

Input Impedance

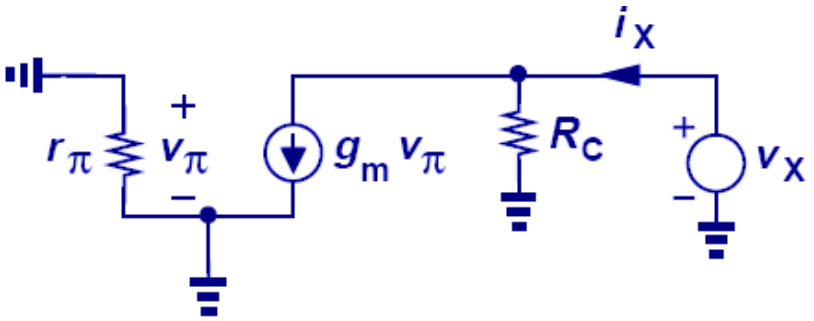
(Ideally infinite)



$$R_{in} = \frac{v_x}{i_x} = r_\pi = \frac{\beta V_T}{I_C}$$

Output Impedance

(Ideally zero)

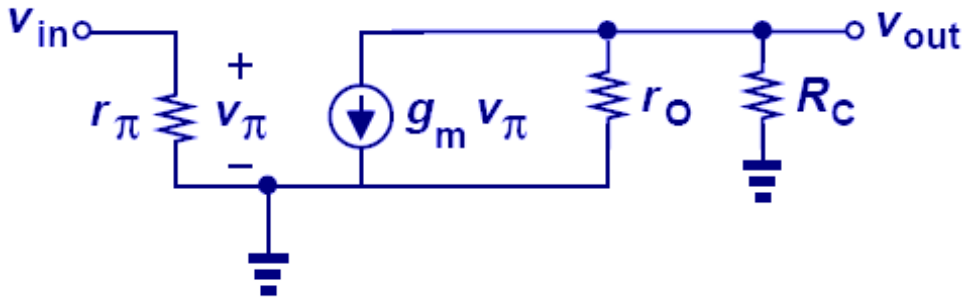


$$R_{out} = \frac{v_x}{i_x} = R_C \quad \text{(since } v_\pi = 0\text{)}$$

Tradeoff between output impedance and voltage gain

Common-Emitter Amplifier with Early effect

- Early effect will lower the gain of the CE amplifier, as it appears in parallel with R_C.



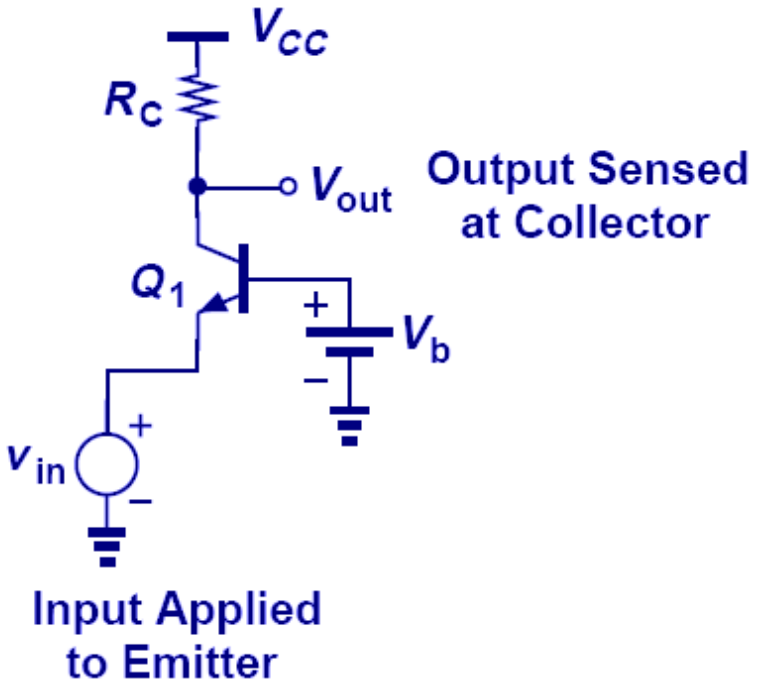
$$r_o = \frac{V_A}{I_C}$$ V_A: Early voltage

$$A_V = -g_m(R_C||r_0)$$

$$R_{out} = R_C||r_0$$

Common-Base Amplifier

- In common base topology, where the base terminal is biased with a fixed voltage, emitter is fed with a signal, and collector is the output.

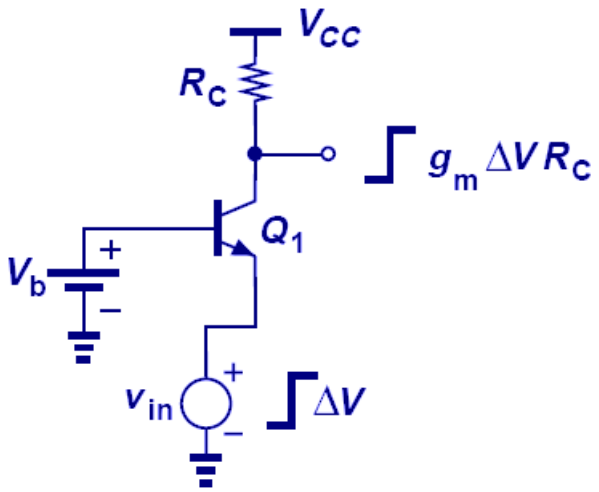


Why does this work?

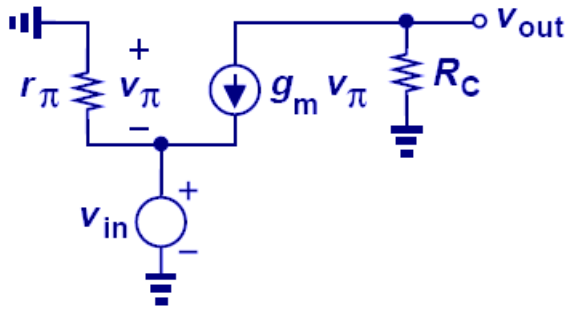
Change in V_E changes V_{BE}, hence I_C

Common-Base Amplifier

- Voltage gain
  - The voltage gain of CB stage is $g_m R_C$, which is identical to that of CE stage in magnitude and opposite in phase (positive V_{in} means negative V_{BE}).



$$r_\pi = \frac{\beta}{g_m} \qquad g_m = \frac{I_c}{V_T}$$



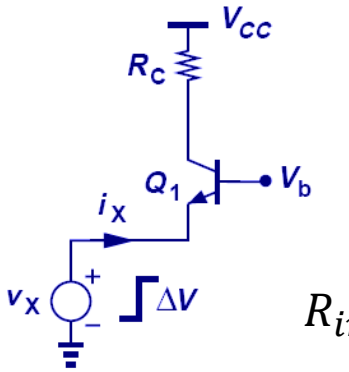
$$A_V = \frac{v_{out}}{v_{in}}$$

$$v_\pi = -v_{in} \qquad -\frac{v_{out}}{R_C} = g_m v_\pi = -g_m v_{in}$$

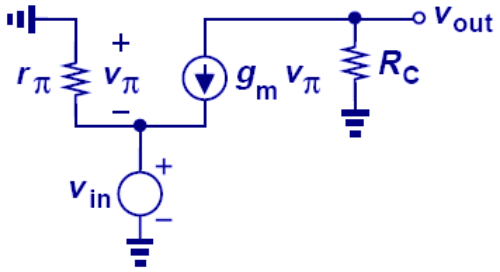
$$\boxed{A_V = g_m R_C}$$

Common-Base Amplifier

- The input impedance of CB stage is much smaller than that of the CE stage.



$$R_{in} = \frac{v_x}{i_x}$$



$$i_x = -\left(g_m v_\pi + \frac{v_\pi}{r_\pi}\right)$$

$$v_\pi = -v_{in}$$

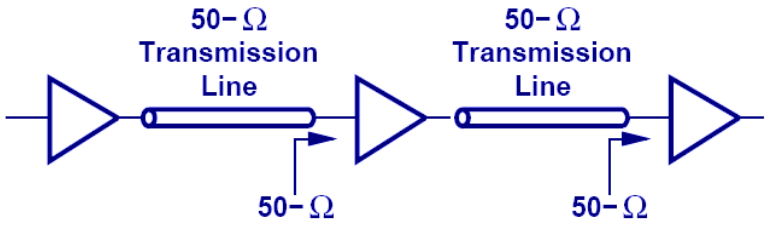
$$R_{in} = \frac{1}{g_m}$$

$$\left(R_{in} = r_\pi = \frac{\beta}{g_m} \text{ for CE}\right)$$

- CB stage's low input impedance can be used to create a match with $50\ \Omega$ transmission line (no reflection to the transmission line)
  - However, low input impedance could mean input signal is attenuated

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{sig} + R_{in}}$$

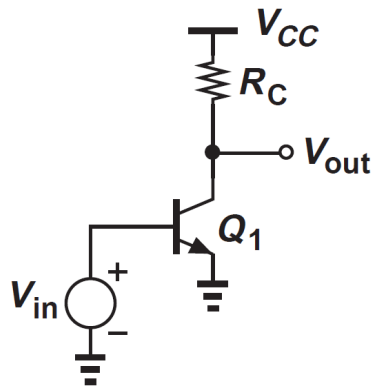
v_{sig}: incoming signal
v_{in}: input received by the circuit
R_{sig}: impedance of the signal (output impedance from previous stage)

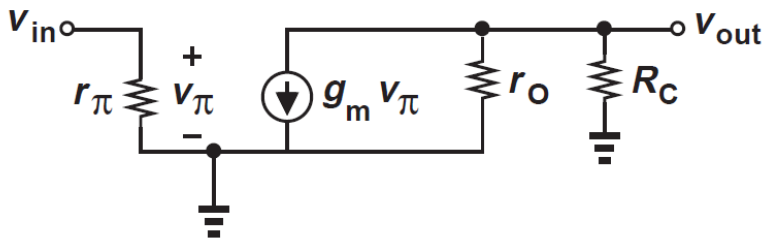


- Output impedance:
  - Same as CE stage

BJT Amplifier: Example

- The circuit below is biased with a collector current of 1 mA and R_C = 1 kΩ. If β = 100, V_T = 26 mV, and V_A = 10 V, determine the small-signal voltage gain and the I/O impedances.





Early effect reduces the voltage gain

$$g_m = \frac{I_c}{V_T} = \frac{1 \times 10^{-3}}{26 \times 10^{-3}} = (26\ \Omega)^{-1}$$

$$r_\pi = \frac{\beta}{g_m} = 100(26) = 2.6k\Omega$$

$$r_0 = \frac{V_A}{I_C} = \frac{10\ V}{1\ mA} = 10k\Omega$$

$$A_V = -g_m(R_C||r_o)$$

$$= -\frac{1}{26}\ (1k\Omega||10k\Omega) \approx -35$$

If no early effect: $A_V \approx -38$

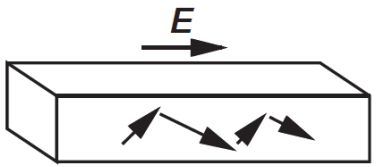
$$R_{in} = r_\pi = 2.6k\Omega$$

$$R_{out} = (R_C||r_o) = 909\Omega$$

Recap

- P-type and N-type semiconductors

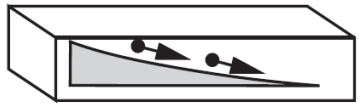
Drift Current



$$J_n = q\,n\,\mu_n E$$

$$J_p = q\,p\,\mu_p E$$

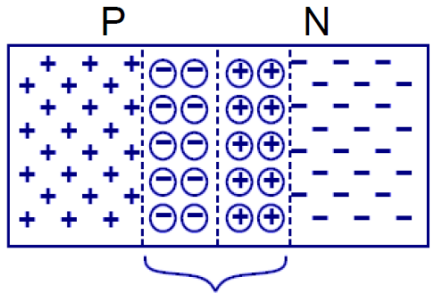
Diffusion Current



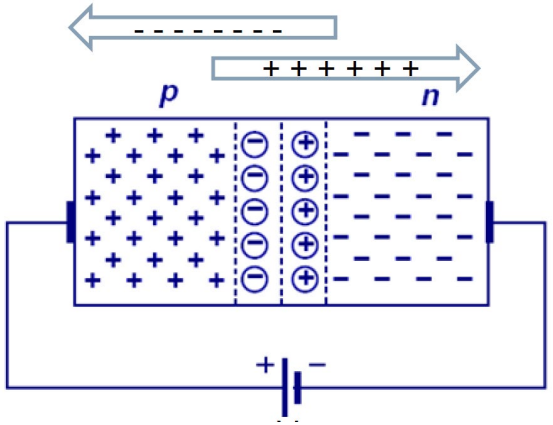
$$J_n = q\,D_n \frac{dn}{dx}$$

$$J_p = -q\,D_p \frac{dp}{dx}$$

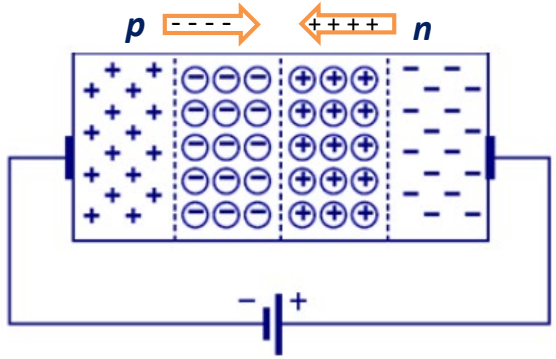
- PN Junctions as Diodes



Depletion Region



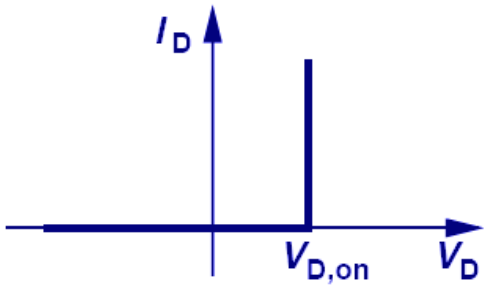
Forward bias

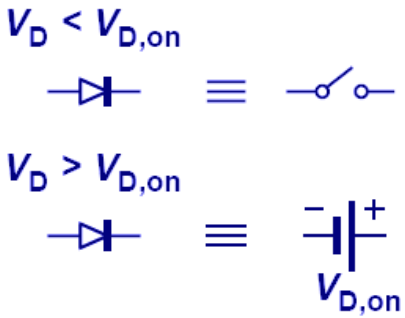


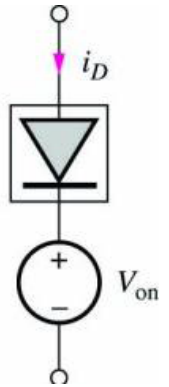
Reverse bias

Recap

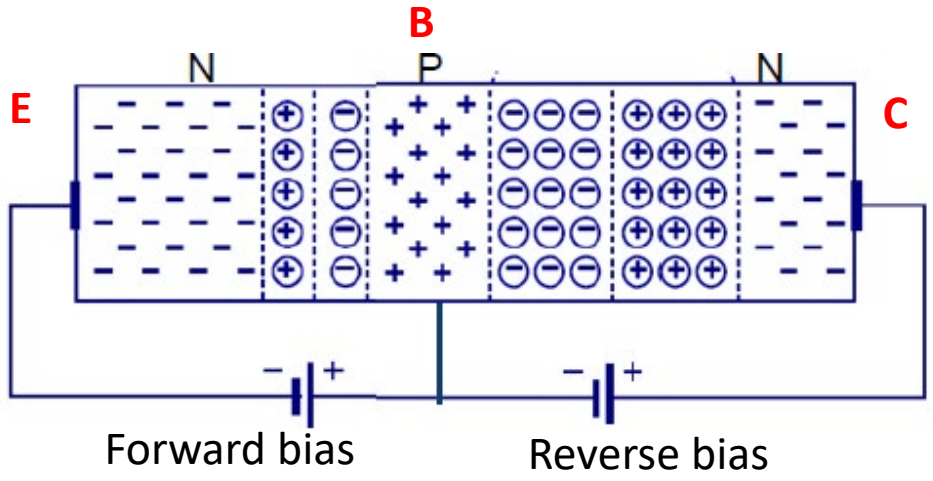
- Diode Models

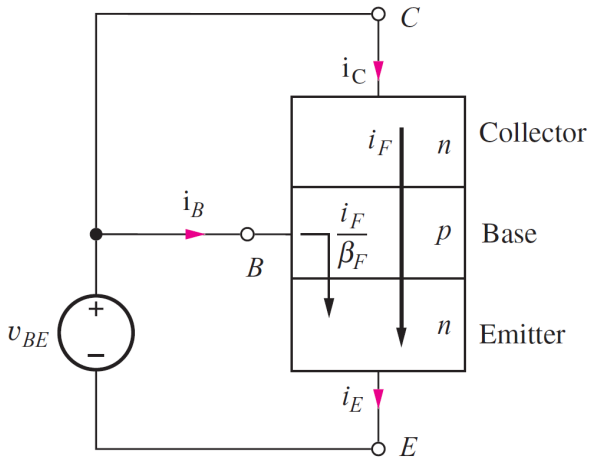






- Append two PN junctions together to create BJT





Active mode of operation

ELEC2104 – Week 8: Part II

MOSFET – Theory of Operation

Textbook Chapter Reading:
Chapter 4.1 – 4.4

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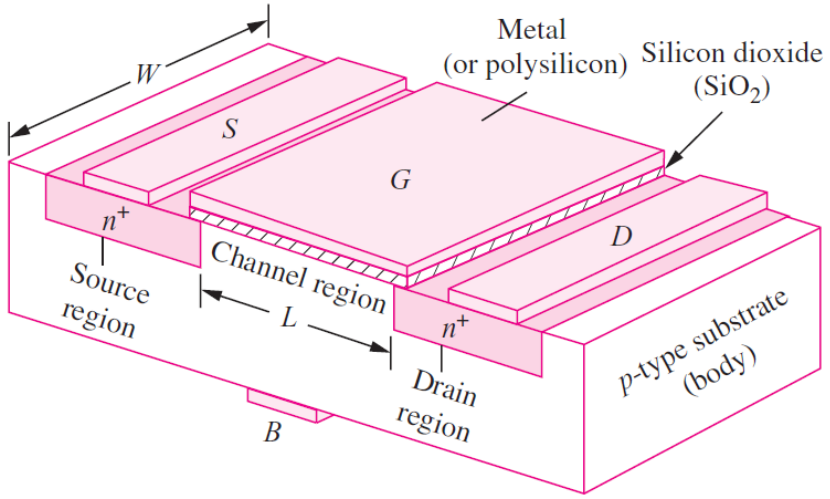
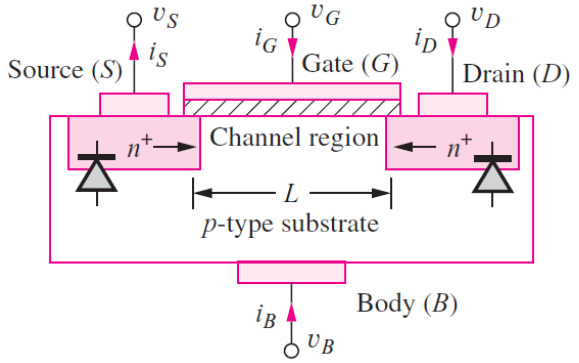
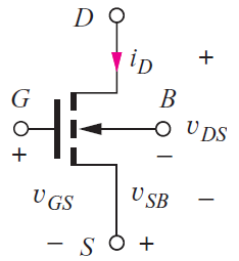
Metal-Oxide Semiconductor

- **MOSFET:** Metal-oxide-semiconductor Field Effect Transistor
- **Four** terminals device
- **Gate (G)**: Top conductive plate (e.g. metal) residing on a thin dielectric (oxide insulator) layer
- Two heavily doped regions (n^+ or p^+ type):
  - **Source (S)** – provides carriers
  - **Drain (D)** – receive carriers
- **Substrate or Body**: p- or n-type semiconductor
- NMOS or PMOS transistors
  - NMOS: electrons flow in the channel







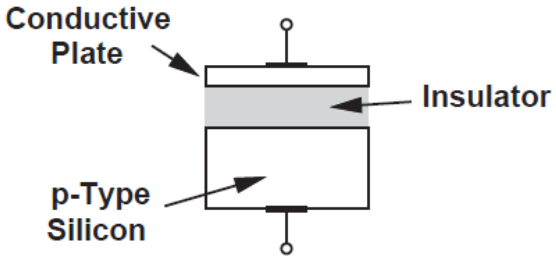
i_G usually 0

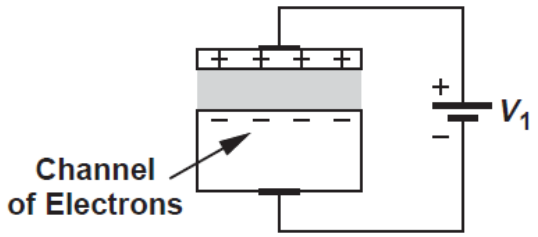
MOS Capacitor Operation

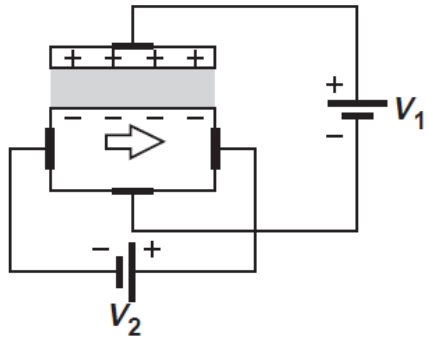
- First, understand the MOS operation
- Consider a simple geometry consisting of a conductive plate (**M**etal), an insulator (**O**xide insulator) and a lightly doped piece of silicon (**S**emiconductor)
- Apply V_1 on the top plate
  - Attracts negative charges (electrons)
  - Creates a channel of free electrons

$$Q = CV_1$$

  - Forms a good conductive path with least resistance
- Apply V_2 across the silicon
  - Electrons drift from left to right
  - Current flows through the channel

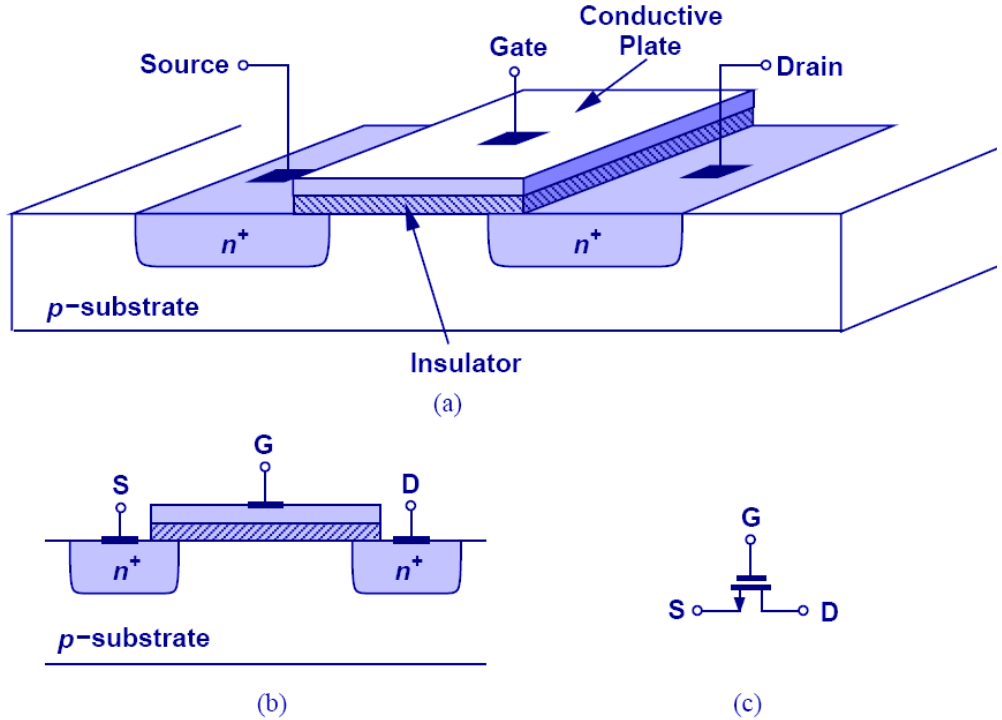






MOSFET Structure

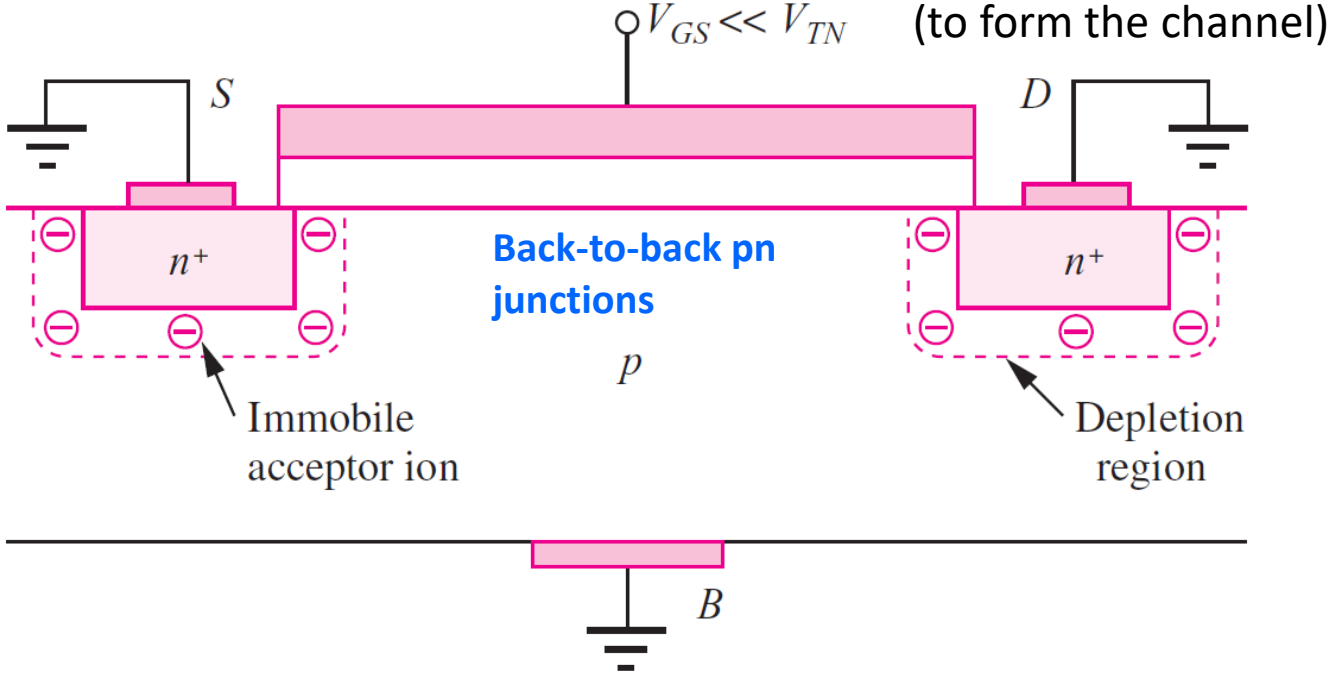
- N-type MOS (NMOS) Transistor
- Central region is the MOS cap
- N-type source/drain and p-type substrate
- Two n-well regions on either side of the MOS capacitor can supply electrons
    - Symmetric. Unlike BJT



N MOSFET Operation

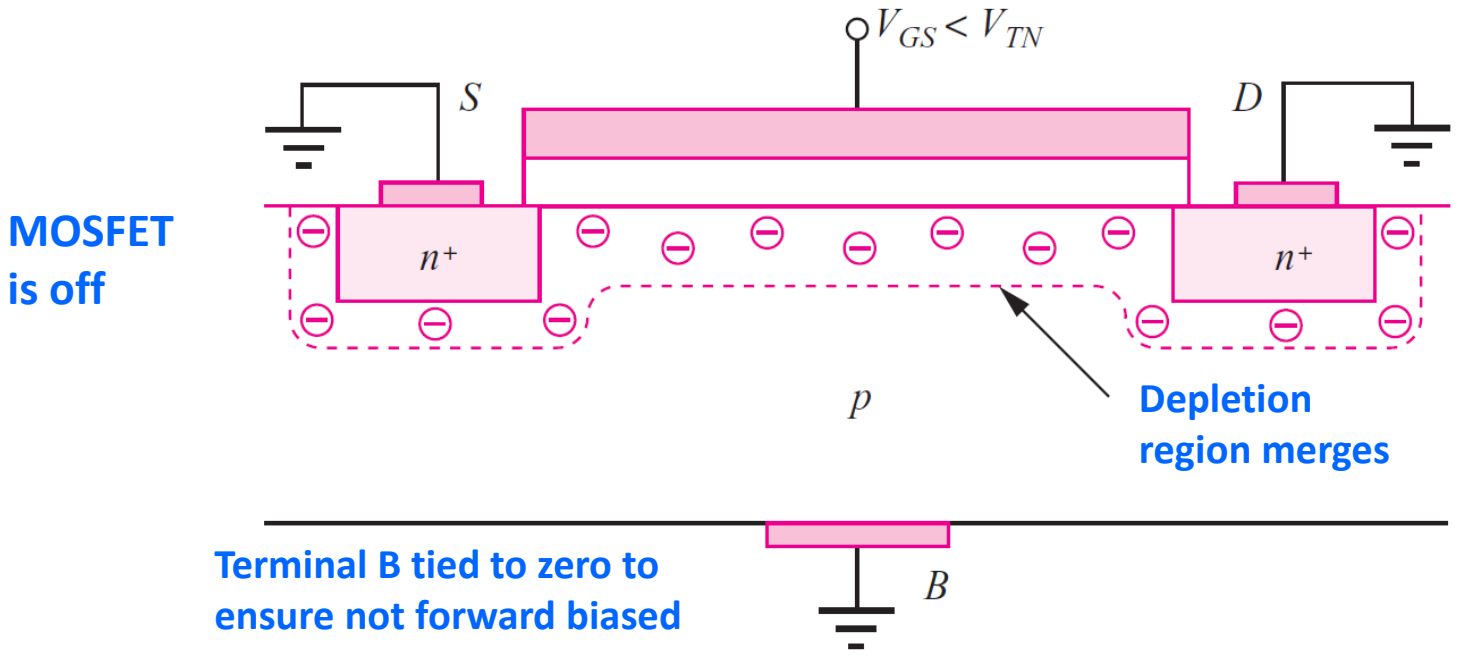
- First, consider the arrangement where:
  - Source (S) and Drain (D) are grounded
  - Gate (G) voltage is near zero
  - No current can flow

V_{TN}: threshold voltage (to form the channel)



N MOSFET Operation

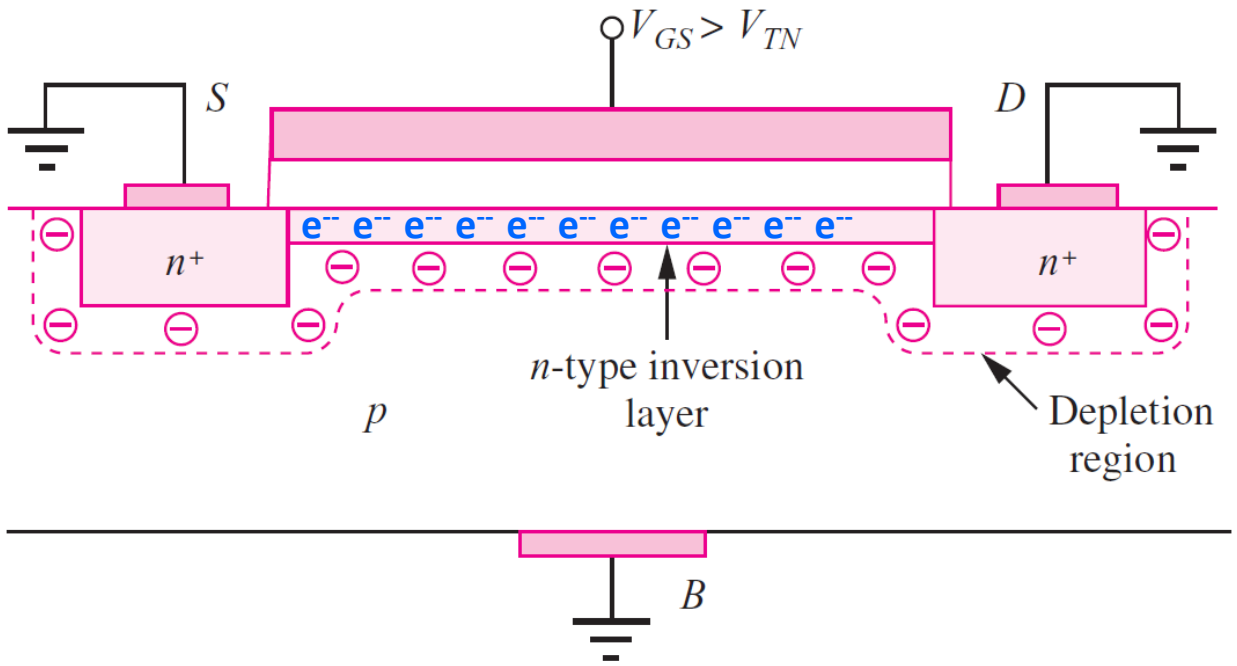
- $\boldsymbol{V_{GS} < V_{TN}}$
  - As V_G rises, positive charge on the gate repels the holes in the substrate, exposes negative ions, and creates depletion region
  - Depletion region is devoid of free carriers,
  - No channel of mobile charges formed yet, sill no current



N MOSFET Operation

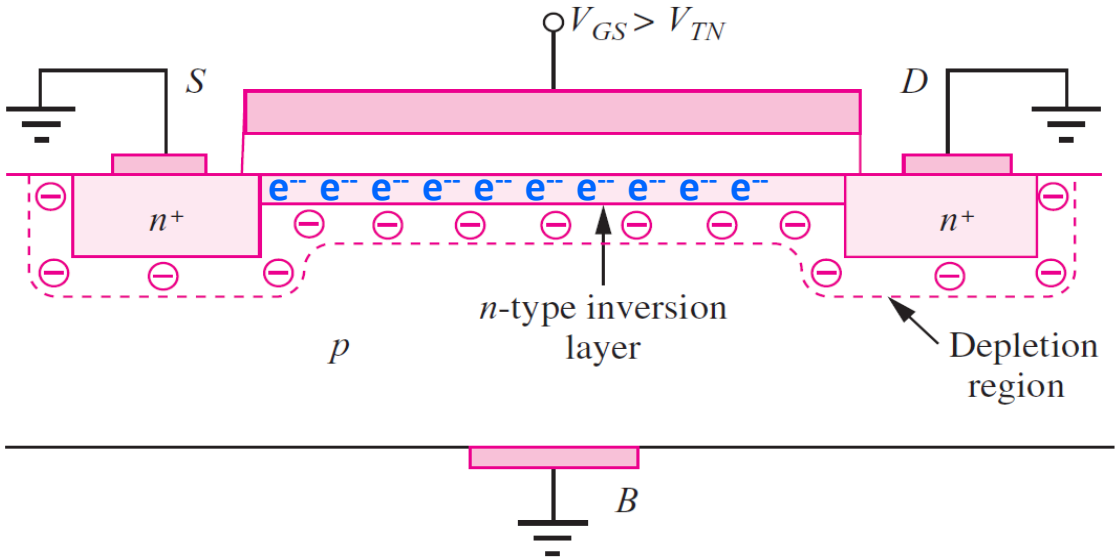
- $\boldsymbol{V_{GS} > V_{TN}}$
  - V_G becomes sufficiently positive, free electrons are attracted to the oxide-silicon interface
  - An inversion layer is formed, a conductive channel connecting S to D
  - The voltage at which this layer just forms -> “threshold voltage” V_{TN}

MOSFET is on



N MOSFET Operation

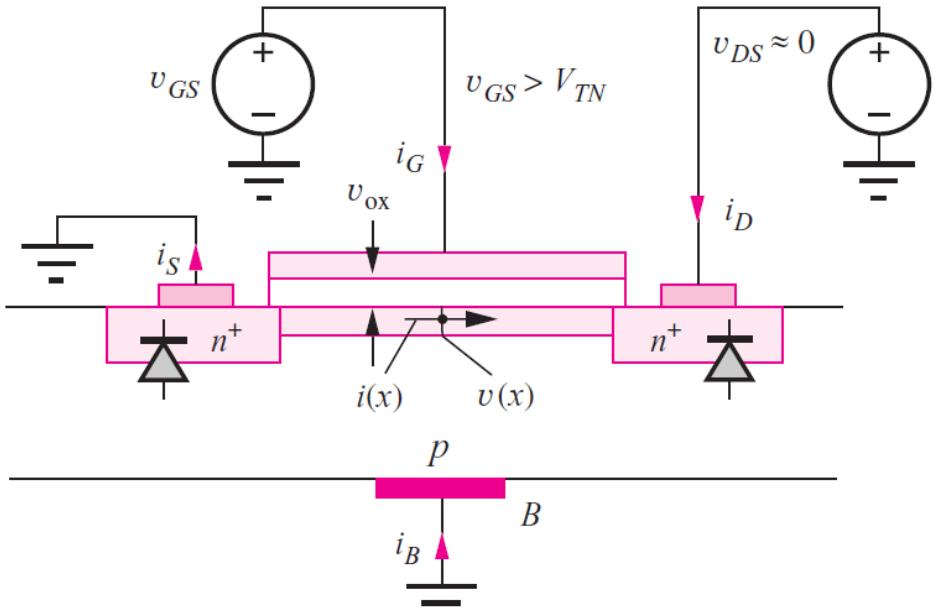
- The conductive channel between S and D can be viewed as a voltage-dependent resistor



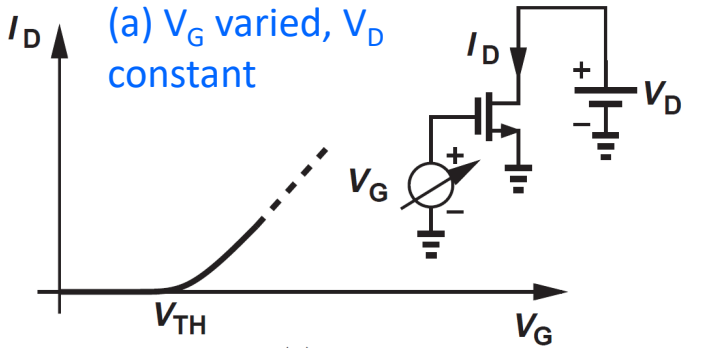
Now, with a voltage applied between S and D, current can flow.

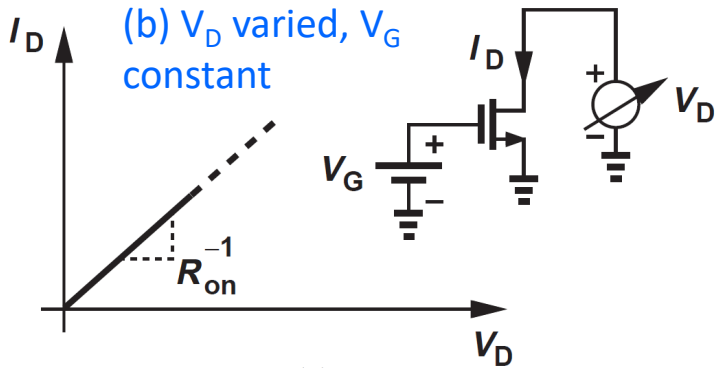
N MOSFET Operation

- If positive voltage is applied between D and S, electrons in the channel inversion layer will flow -> $I_D > 0$
- Gate terminal is insulated from the channel, $i_G = 0$.



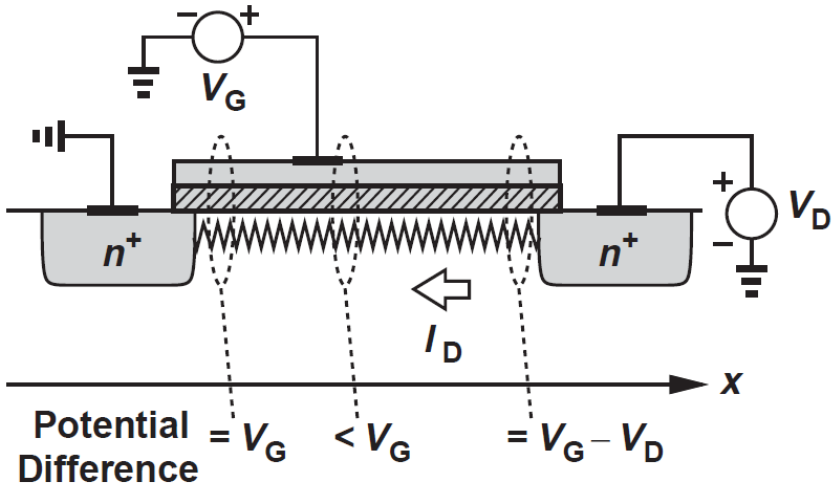
What is the current transport mechanism in a MOSFET?
Drift.

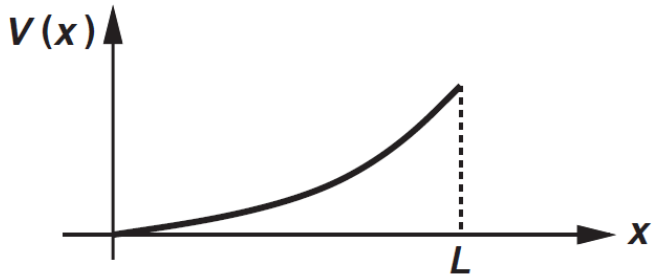


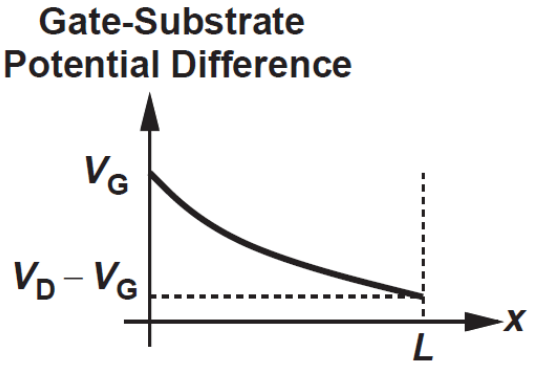


Channel Pinch-Off

- If the drain voltage (V_D) remains higher than source voltage (V_S), the voltage at each point along the channel with respect to ground increases as we go from S to D
- Potential difference between gate and substrate is reduced close to drain
- Density of electrons falls to minimum at x = L.

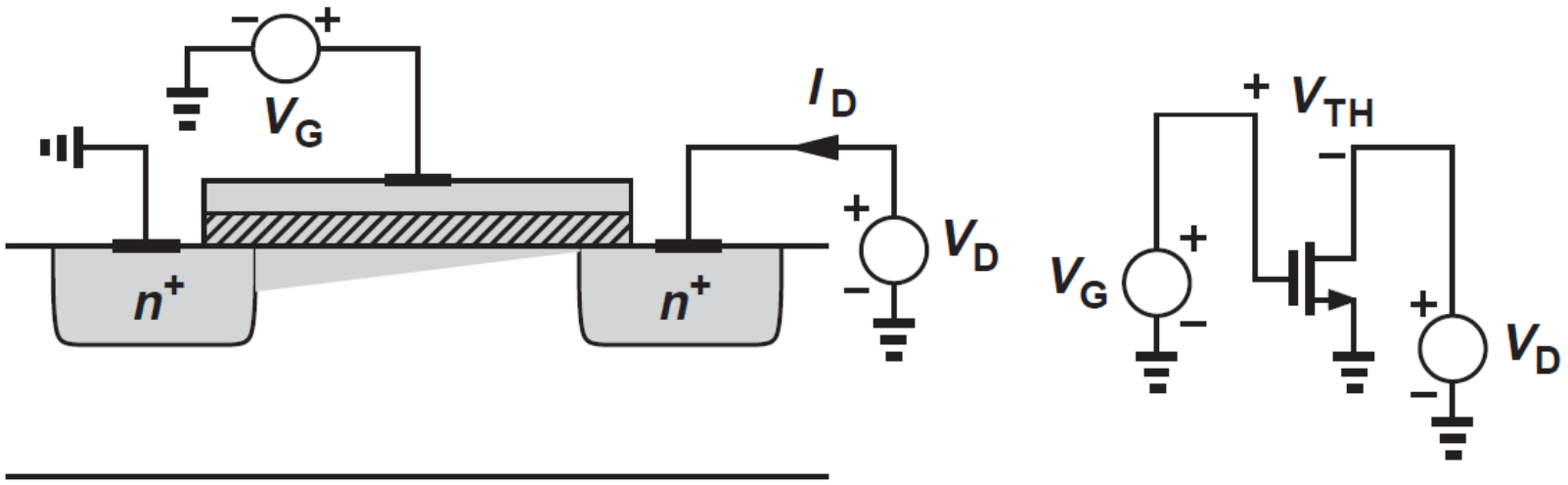






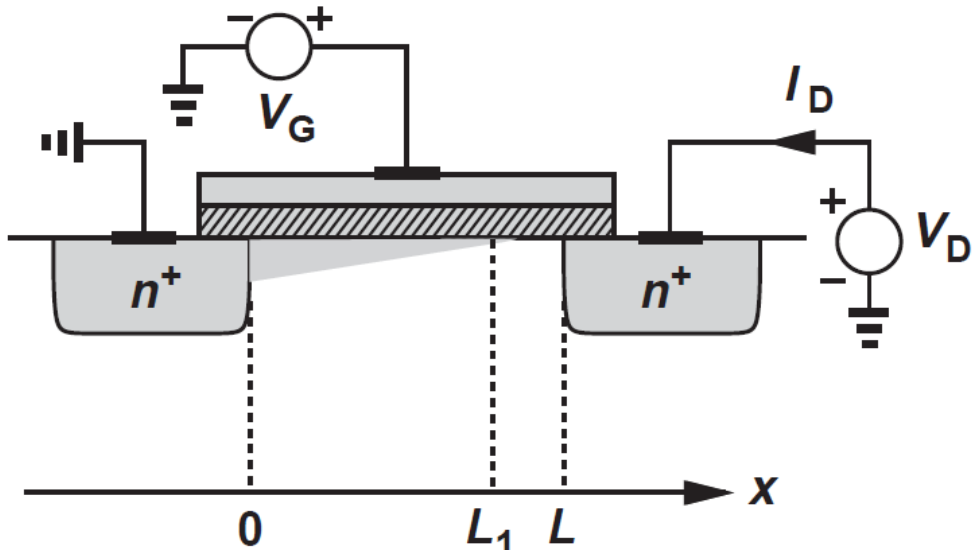
Channel Pinch-Off

- If V_D is high enough, $V_G - V_D \leq V_{TN}$, the channel ceases to exist near the drain.
  - Gate-substrate potential difference is not sufficient to attract electrons
- Channel is pinched off



Channel Pinch-Off

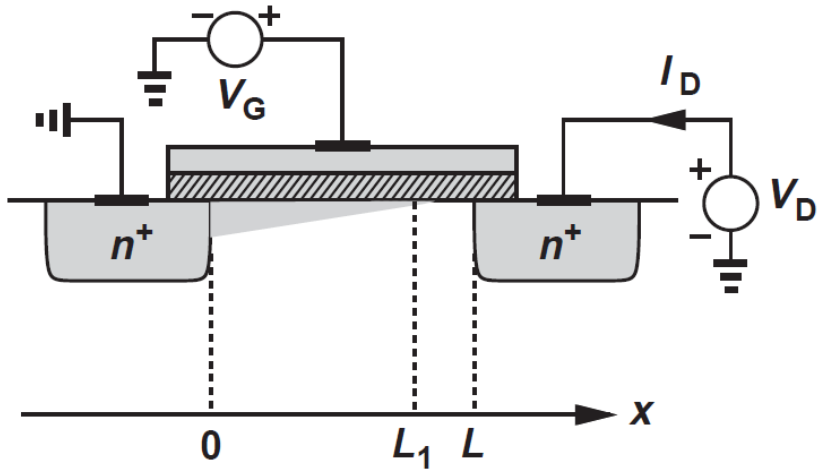
- If V_D rises further, $V_D > V_G - V_{TN}$ at x = L
- Voltage difference between gate and substrate falls to V_{TN} at $L_1 < L$
- Device contains no channel between L_1 and L.

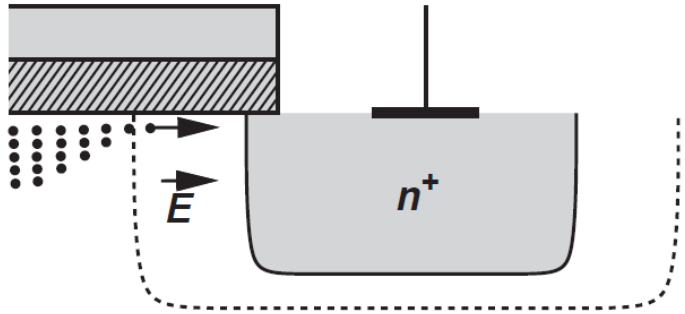


Can the device still conduct?

Channel Pinch-Off

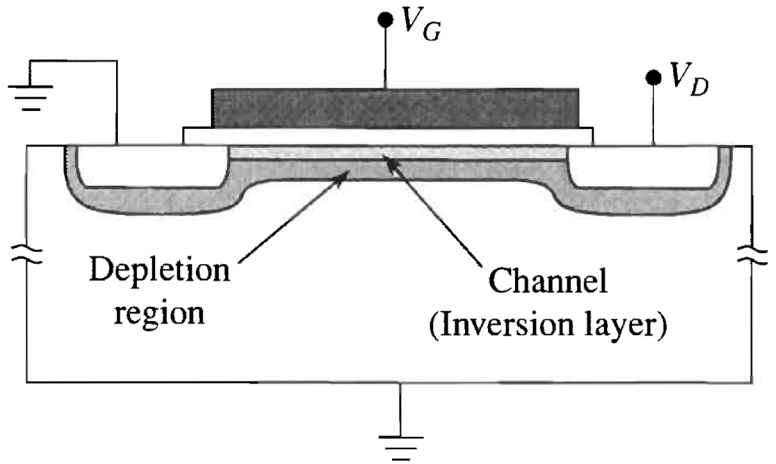
- The end of the channel at L_1 is in the depletion region.
- Electrons are rapidly swept to D due to the built-in E field in depletion region.
- When $V_D > V_G - V_{TN}$, V_D no longer affects current significantly
- MOSFET acts as a constant current source independent of V_{DS}



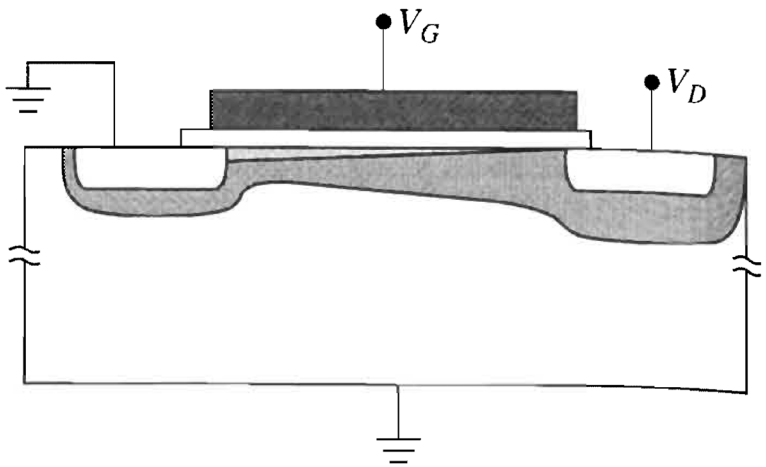


Electrons injected into depleted region gets swept onto the drain

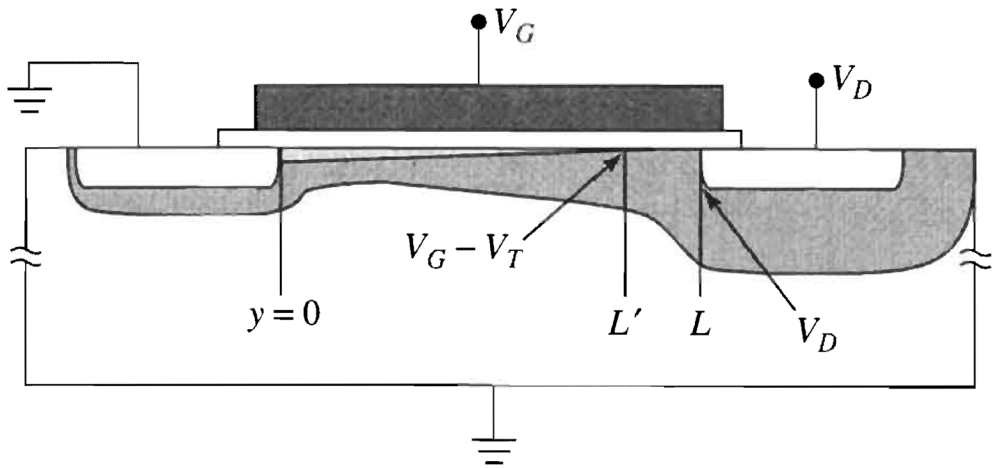
Channel pinch-off (with depletion region shown)



(a) $V_G > V_T, V_D \approx 0$

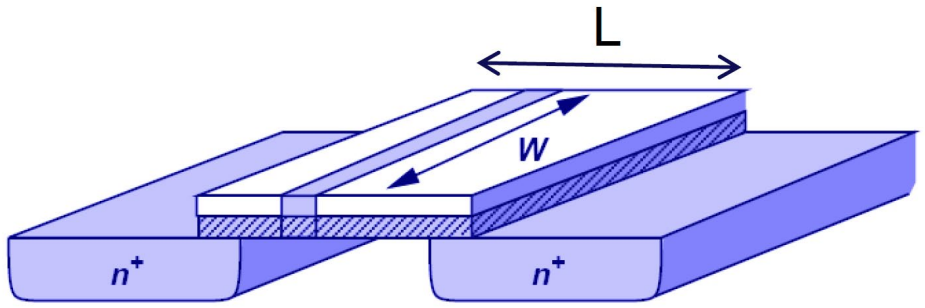


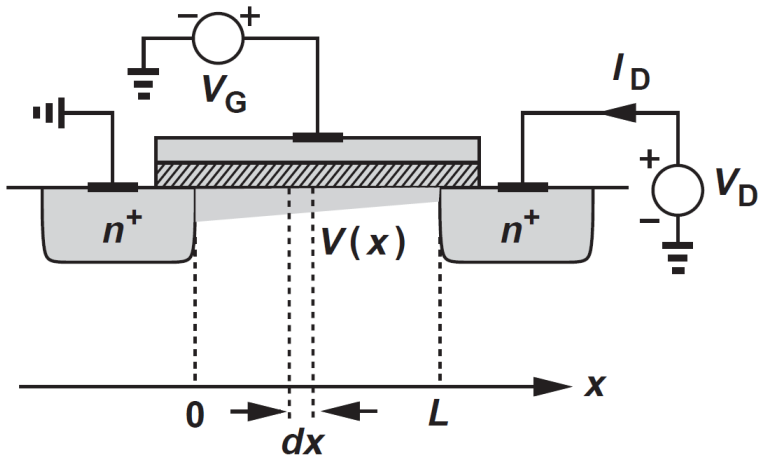
(b) $V_G > V_T, V_D < V_G - V_T$



(c) $V_G > V_T, V_D > V_G - V_T$

Channel current related to channel charge





Starting out with $Q = CV$, as channel voltage varies along x:

Q: charge density in the channel per area
W: width of the channel
C_{ox}: capacitance in the oxide per area

$$Q(x) = C_{ox}\left(V_{GS} - V_{TN} - V(x)\right)$$

$$I_{drift} = -WQ(x)\mu_n E = WQ(x)\mu_n \frac{dV}{dx}$$

$$\int_0^L I_D dx = WC_{ox}\mu_n \int_{V_S}^{V_D} \left(V_{GS} - V_{TN} - V(x)\right)dV$$

$$= WC_{ox}\mu_n \left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$$

On the other hand, I_D should be constant because of current conservation, hence $\int_0^L I_D dx = I_D L$

$$I_D = \beta\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS} = \frac{1}{2}\beta[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

where $\beta = \mu_n C_{ox}\frac{W}{L}$

MOSFET Regions of operations

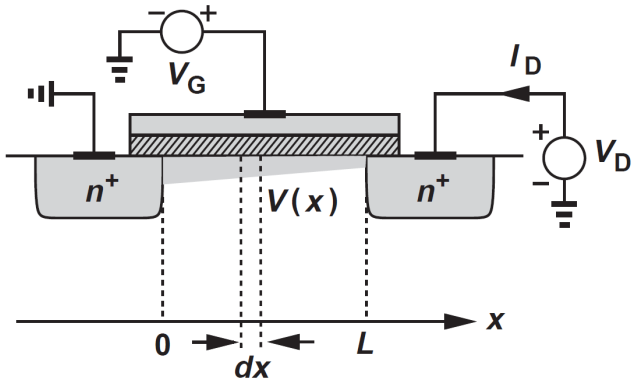
THE UNIVERSITY OF SYDNEY

Regions of Operations

- Linear or Triode Region

$$V_{GS} - V(x) \geq V_{TN} \text{ for } 0 \leq x \leq L$$

  - Resistive channel directly connects the source and drain



$$I_{D,\text{tri}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

  - For small drain voltages: $\frac{V_{DS}}{2} \ll (V_{GS} - V_{TN})$

$$I_D \approx \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TN})V_{DS}$$

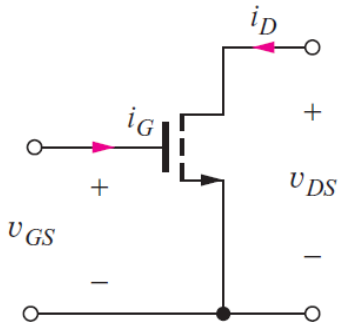
Acts like a resistor connected between drain and source

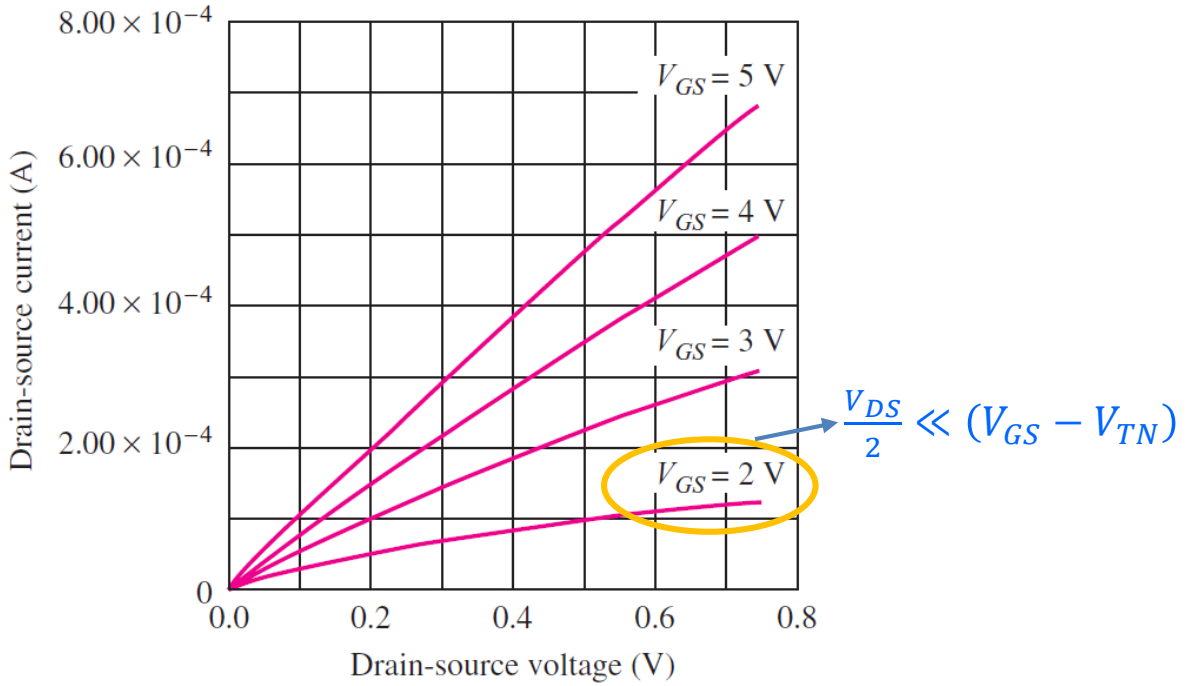
On Resistance

- Resistor value can be controlled by the gate-source voltage

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TN})}$$

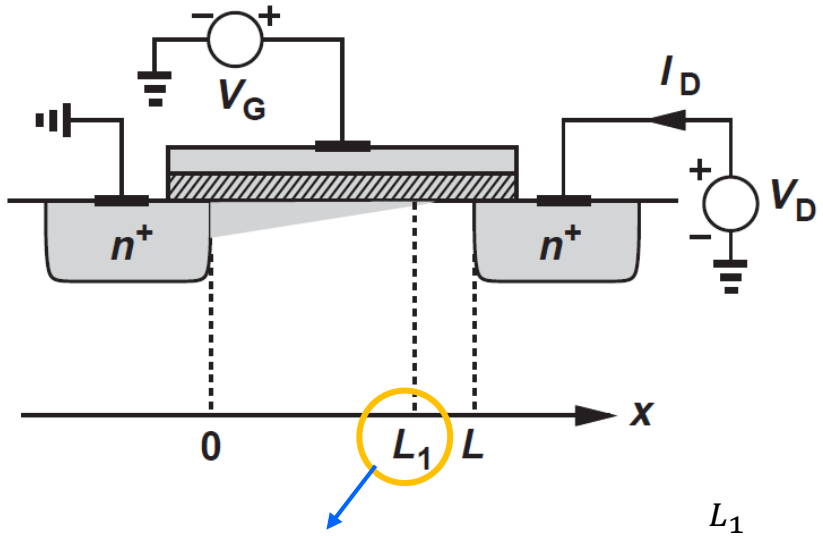
- Near the origin, the i-v curves can be approximated by straight lines having different slopes

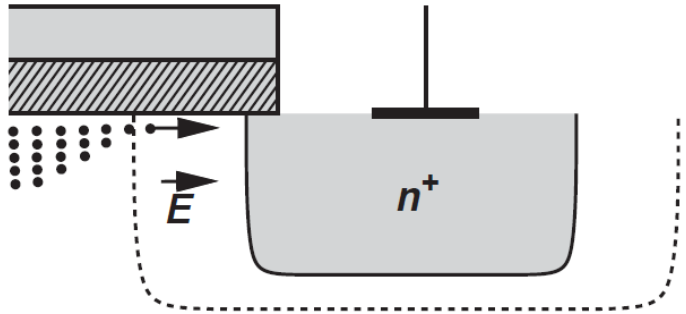




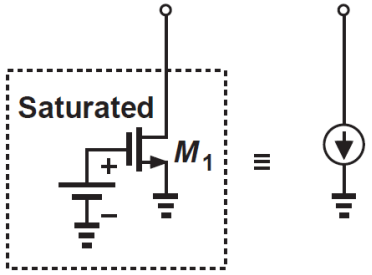
Regions of Operations

- Saturation Region
  - Drain current saturates at a constant value for $V_{DS} > V_{GS} - V_{TN}$





Pinch-off: $V_{DS} = V_{GS} - V_{TN}$

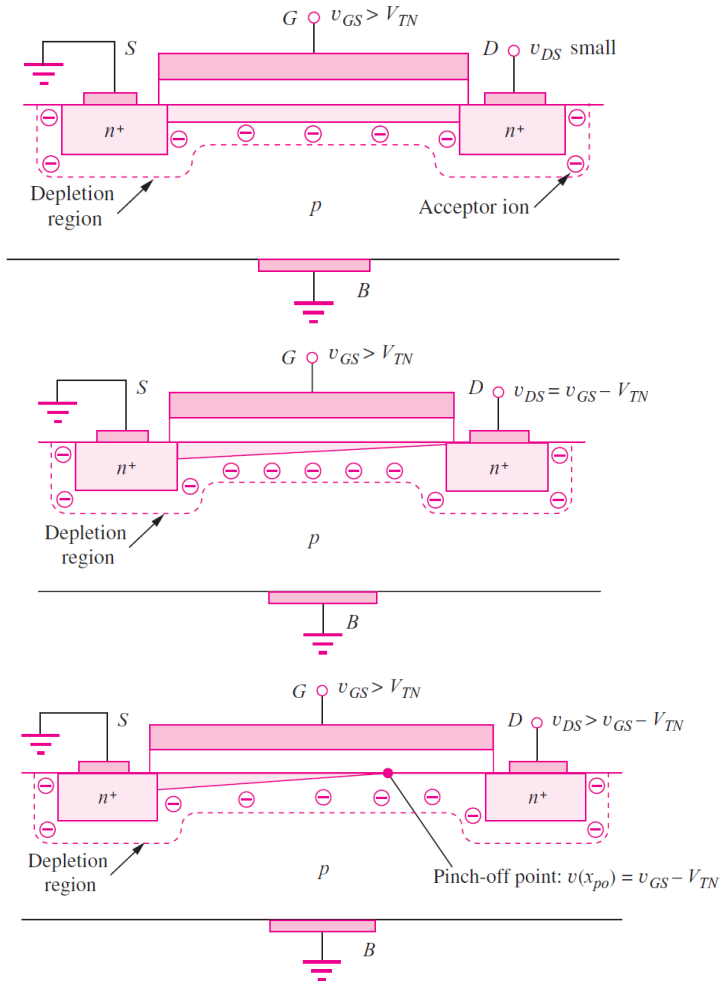


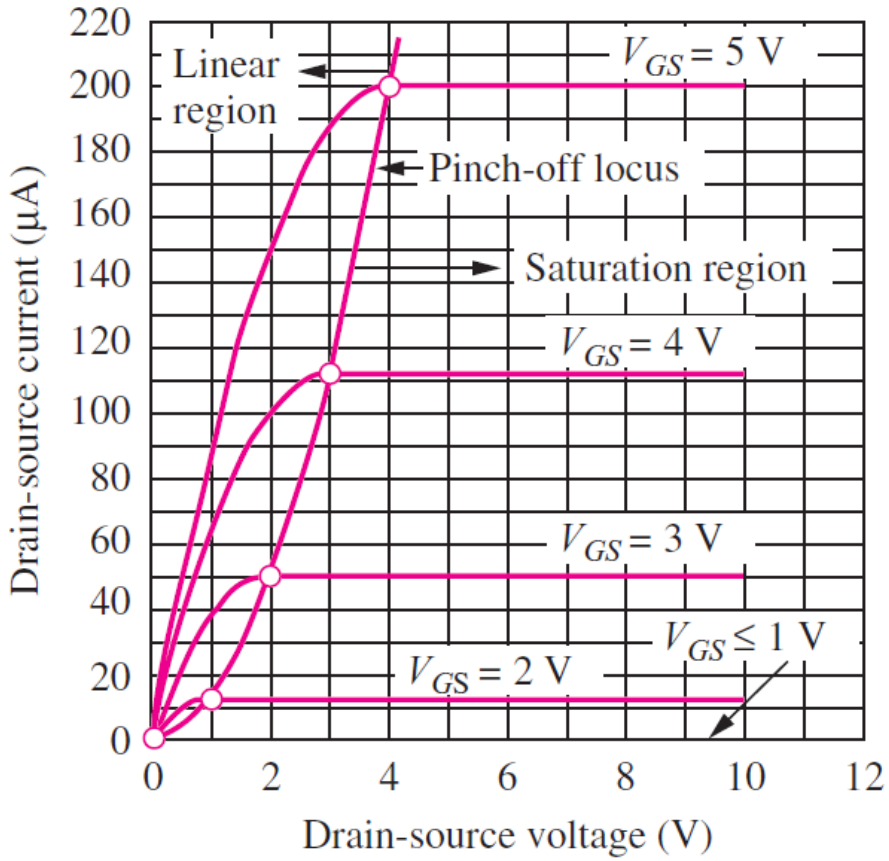
$$\int_0^{L_1} I_D dx = \int_{V_S}^{V_{GS}-V_{TN}} W C_{ox} \mu_n (V_{GS} - V(x) - V_{TN}) dV$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_1} (V_{GS} - V_{TN})^2$$ **Independent of** V_{DS}

Regions of Operations

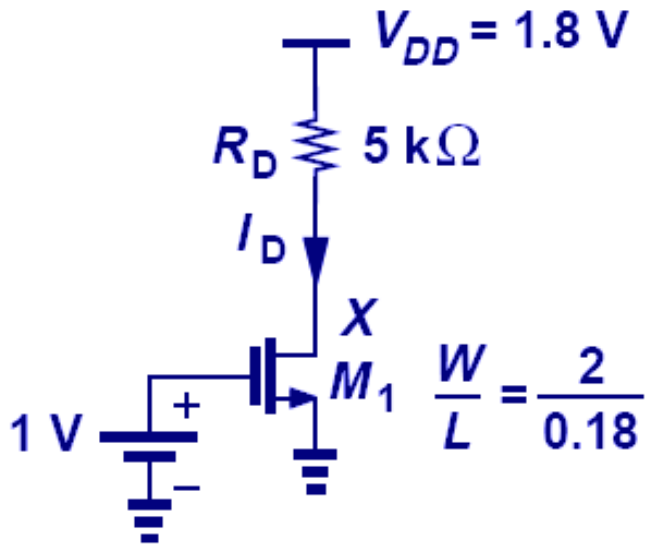
- Linear/Triode and Saturation Regions





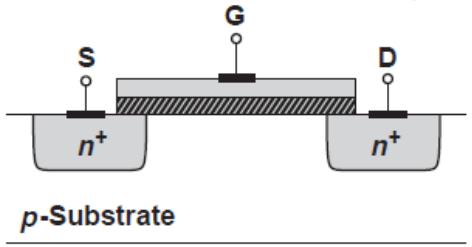
Determining Region of Operation

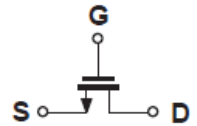
- What region of operation is this transistor operating in?
- Circuit analysis is much easier than with BJTs, because current can only go in one direction
- For the example below, it's triode or saturation: plug numbers into equations to verify



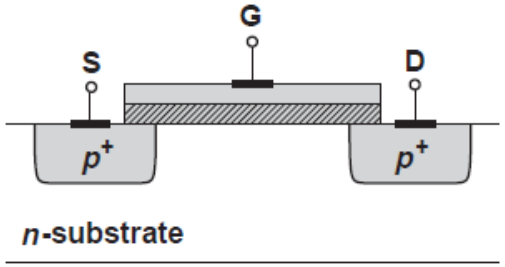
MOSFET Regions Of Operation

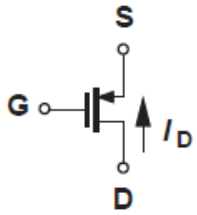
- NMOS:
  - Cut-off :: $V_{GS} = 0$
  - Saturation :: $V_{GS} > V_{TH}$ & $V_{DS} > V_{GS} - V_{TH}$
  - Triode :: $V_{GS} > V_{TH}$ & $V_{DS} < V_{GS} - V_{TH}$





- For PMOS, all values are negative:
  - Cut-off :: $V_{GS} = 0$
  - Saturation :: $V_{GS} < V_{TH}$ & $V_{DS} < V_{GS} - V_{TH}$
  - Triode :: $V_{GS} < V_{TH}$ & $V_{DS} > V_{GS} - V_{TH}$





- Equations end up being the same

$$I_{D,\text{sat}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS}) \qquad I_{D,\text{tri}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

Bipolar Transistor versus MOSFET Summary

- Comparison of Bipolar Transistor and MOSFET characteristics:

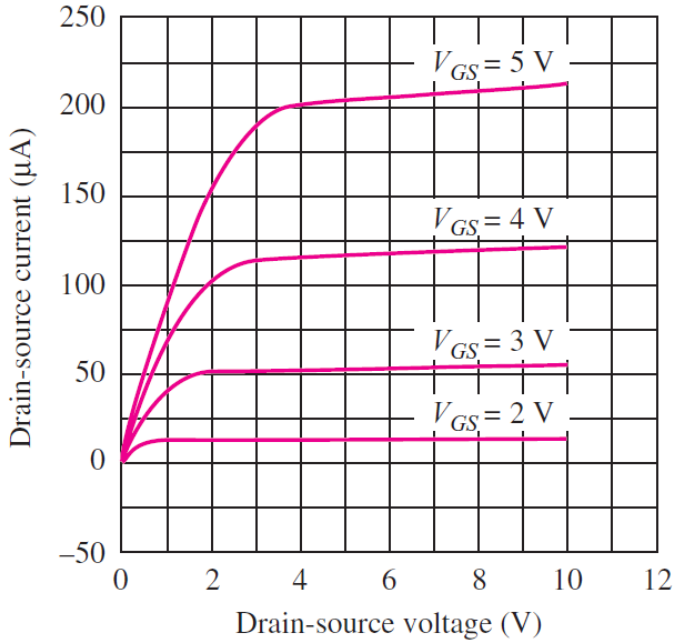
Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$
Finite Base Current	Zero Gate Current
Early Effect	Channel−Length Modulation
Diffusion Current	Drift Current
–	Voltage−Dependent Resistor

- Bipolar devices have a higher g_m than MOSFETs for a given bias current due to its exponential IV characteristics

MOSFET channel-length modulation

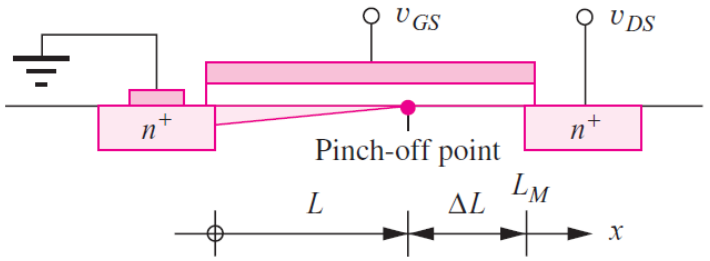
Channel-Length Modulation

- Drain current is not quite constant in the saturation region
- Drain current does increase slightly as drain-source voltage increase



$$L = L_M - \Delta L$$

Actual length L of resistive channel decreases as ΔL increases with V_{DS}

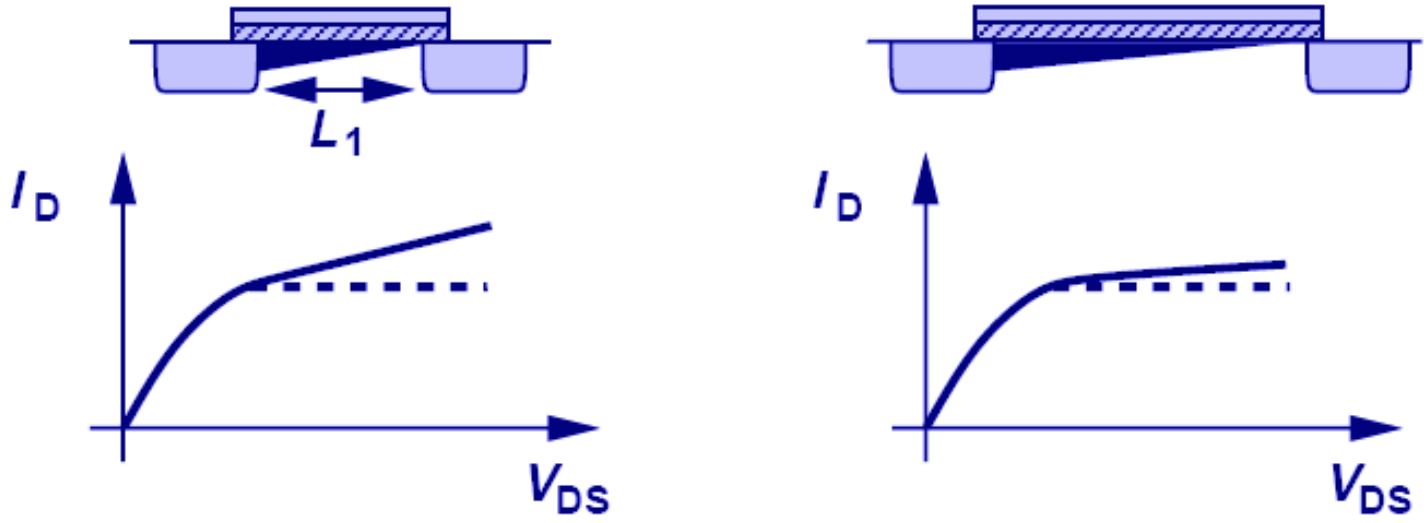


$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_1}(V_{GS} - V_{TN})^2 \quad \Rightarrow \quad I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

λ: Channel-length modulation parameter

Channel Length Modulation

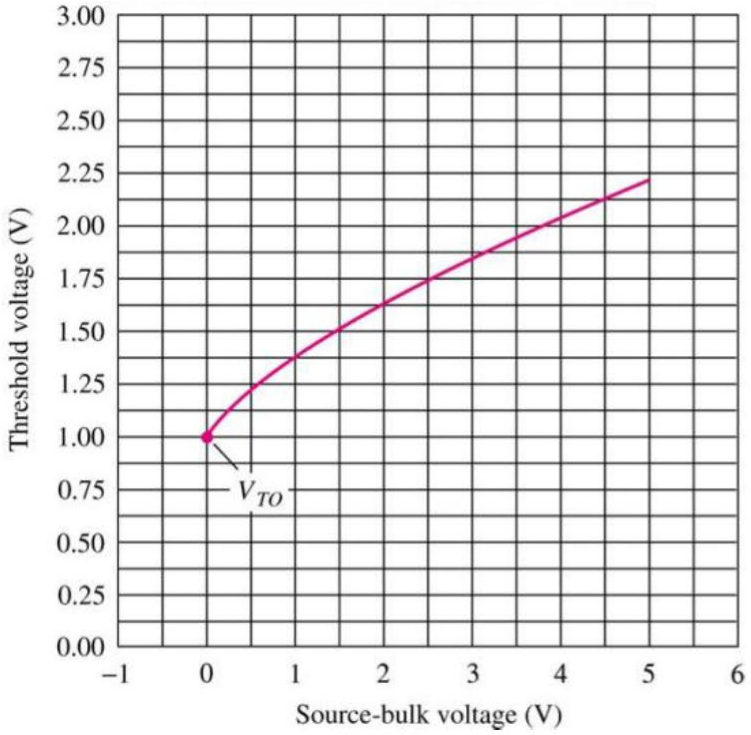
- Unlike the Early voltage in BJT, the channel- length modulation factor can be controlled by the circuit designer.
  - We cannot control base width in a BJT, but we can control gate length of a MOSFET
  - For long L, the channel-length modulation effect is less than that of short L.



Body effect

Body Effect in Strong Inversion

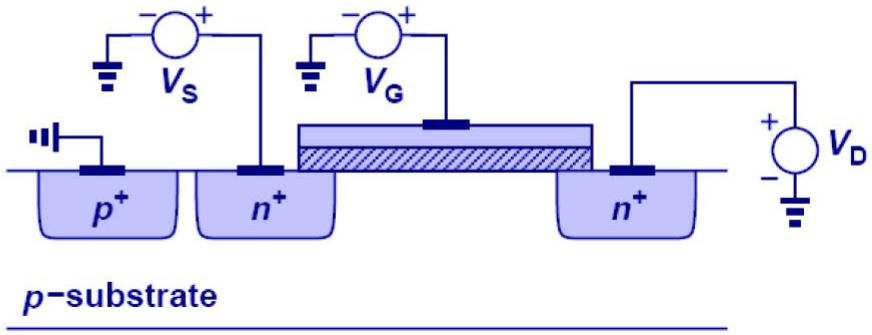
- So far, we have assumed both source and substrate are tied to ground.
- What happens if the substrate is at a different voltage from the source?
- Threshold voltage can change: $V_{Th} = V_{Th0} + \gamma\left(\sqrt{V_{SB} + 2\psi_B} - \sqrt{2\psi_B}\right)$



V_{Th0} = threshold voltage for $V_{SB} = 0$

γ = body-effect parameter = $\dfrac{\sqrt{qN_A 2\varepsilon_s}}{C_{ox}}$ $\left(\sqrt{\text{V}}\right)$

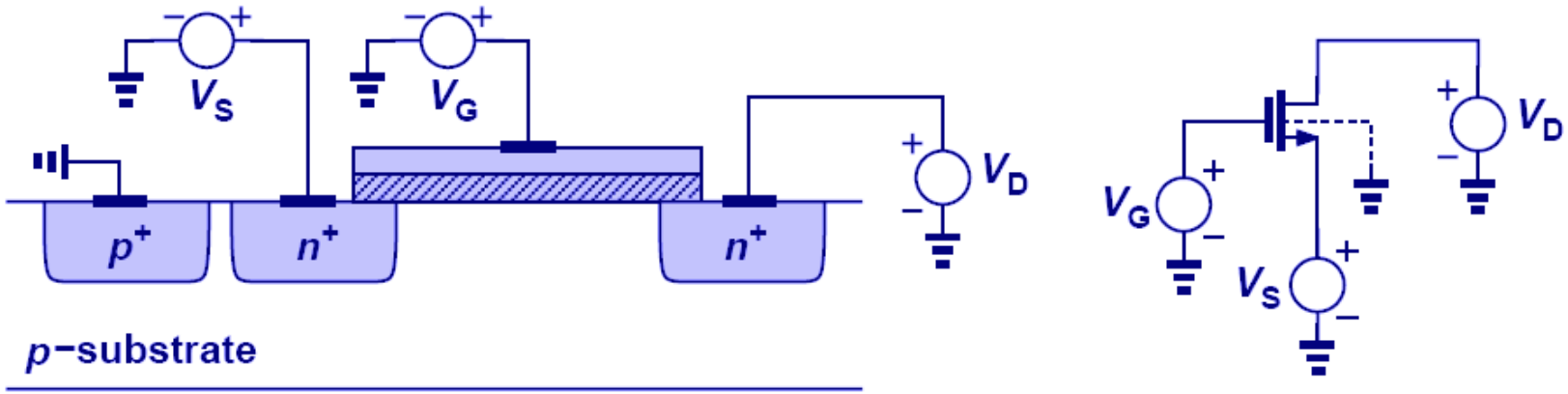
$2\psi_B$ = surface potential (V)



Body Effect

- For most circuits in this course, the substrate will be connected to the same potential as the source.
- Then, no effect.

$$V_{Th} = V_{Th0} + \gamma\left(\sqrt{V_{SB} + 2\psi_B} - \sqrt{2\psi_B}\right)$$

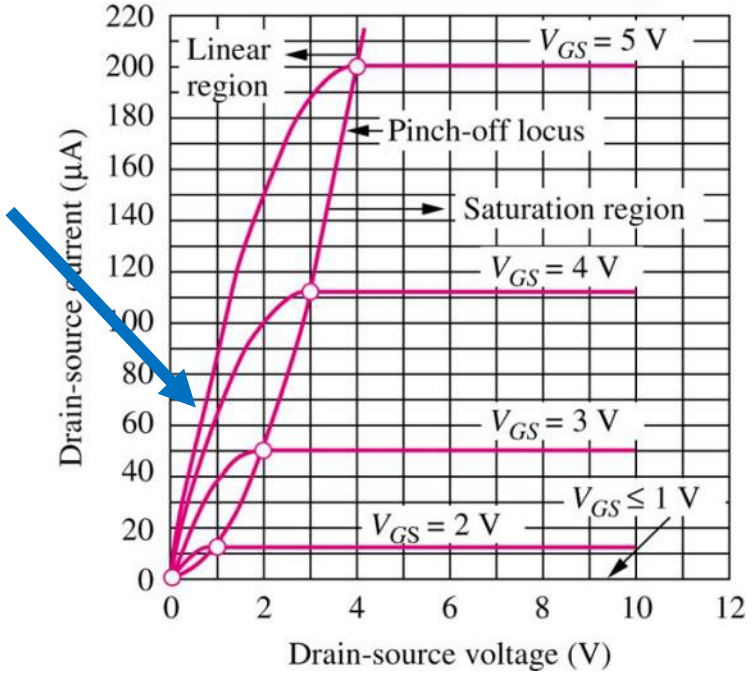


MOSFET circuit models

THE UNIVERSITY OF SYDNEY

MOSFET Circuit Models

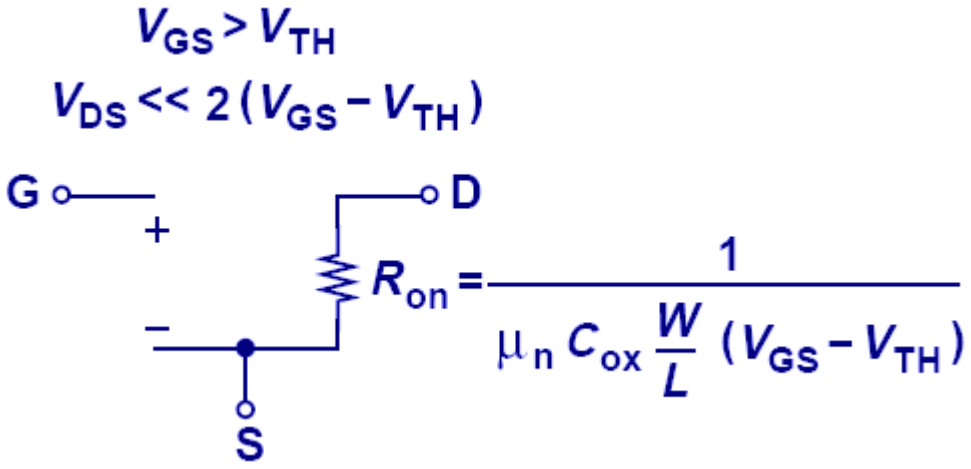
- A MOSFET can be represented using different circuit models depending on its region of operation
- When it is operating in the triode region, but V_{DS} is much smaller than ($V_{GS} - V_{Th}$), the I-V curve is linear
- The MOSFET is a resistor independent of V_{DS}

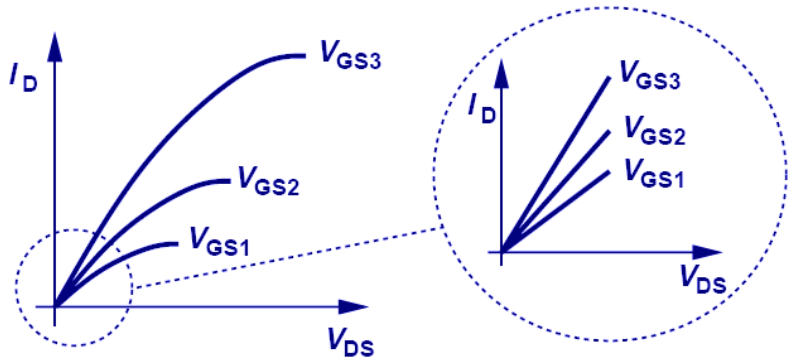


$$I_{D,\text{tri}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$
$$\approx \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TN})V_{DS}$$

Linear Triode Circuit Model

- When it is operating in the triode region, but V_{DS} is much smaller than ($V_{GS} - V_{Th}$), the I-V curve is linear



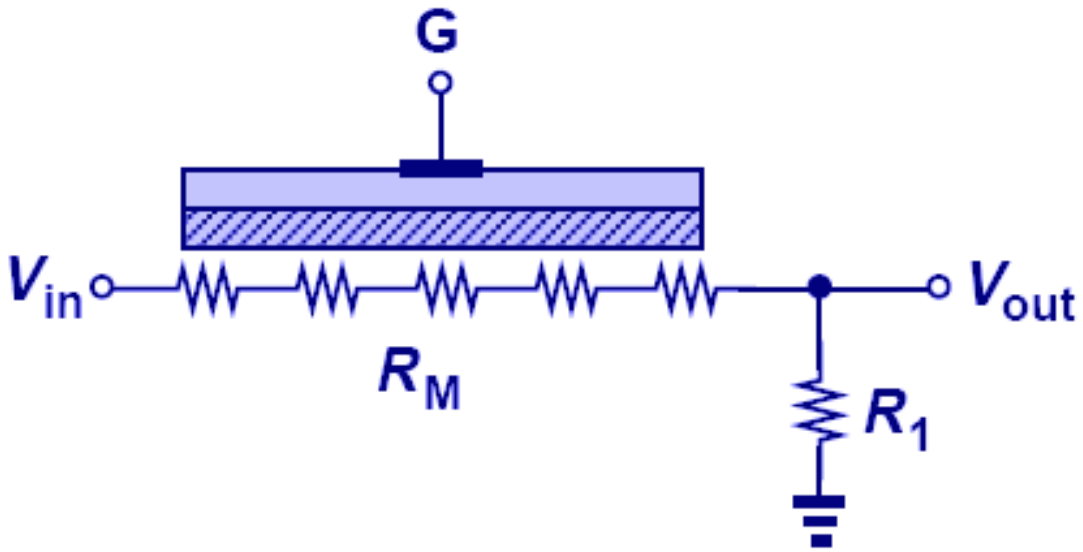


$$I_{D,\text{tri}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN}) V_{DS}$$

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})}$$

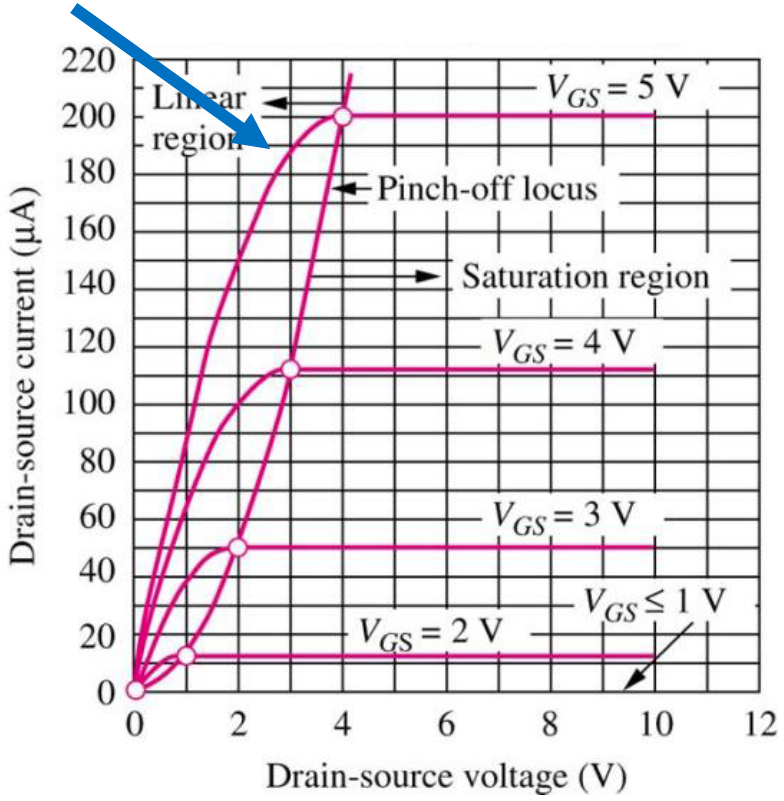
Triode Operation

- This type of gain control finds application in cell phones to avoid saturation near base stations



Non-linear Triode Circuit Model

- When operating in the triode region, and V_{DS} approaches ($V_{GS} - V_{Th}$), the I-V curve is non-linear
- The MOSFET is a voltage-controlled current source.



$$I_{D,\text{tri}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

Non-linear Triode Circuit Model

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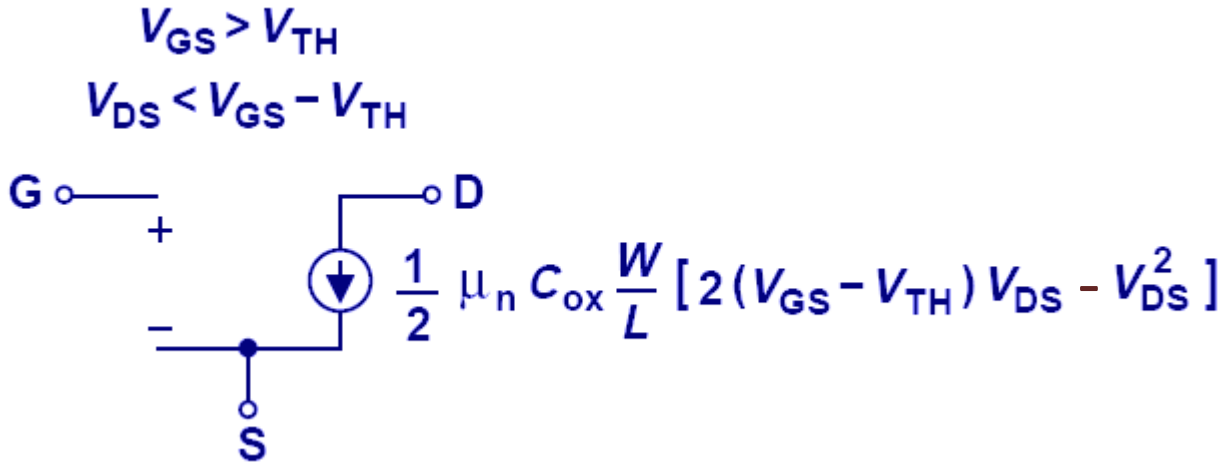
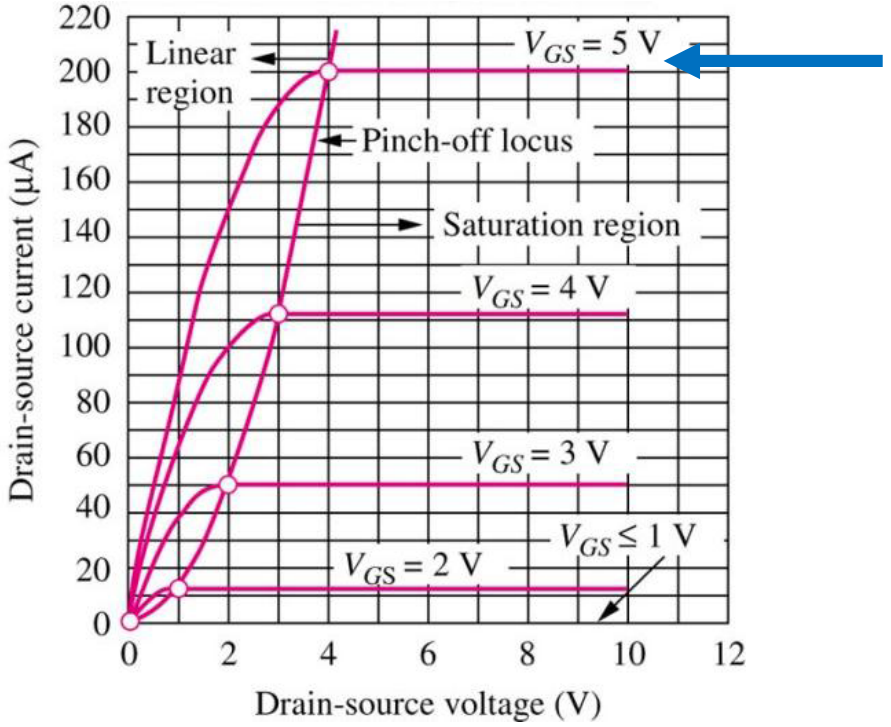


Saturation Circuit Model

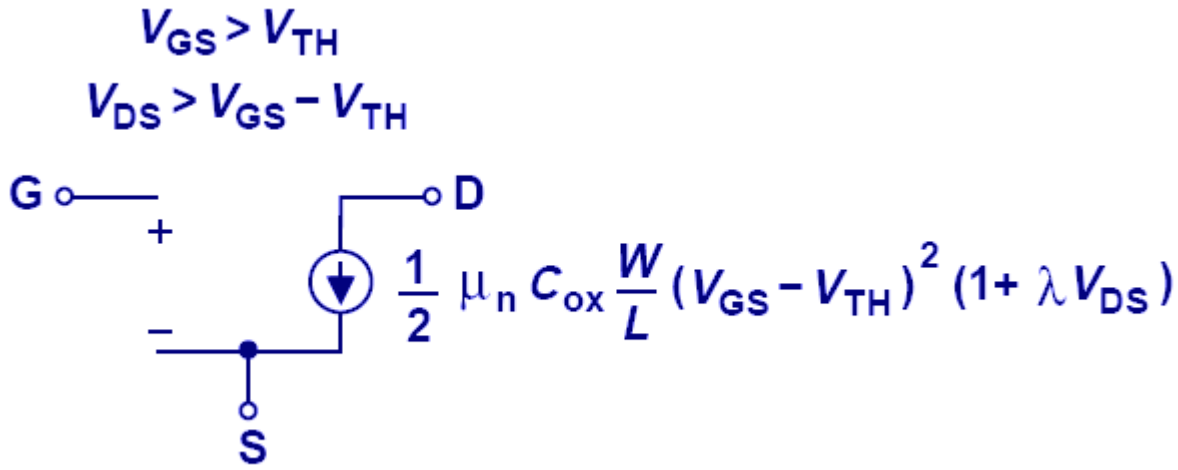
- When operating in saturation, $V_{GS} > V_{TH}$ and $V_{DS} > V_{GS} - V_{TH}$
- Ideally the drain current would be only dependent on V_{GS}
- If we want to take channel-length modulation into account, it must be a voltage-controlled current source as well

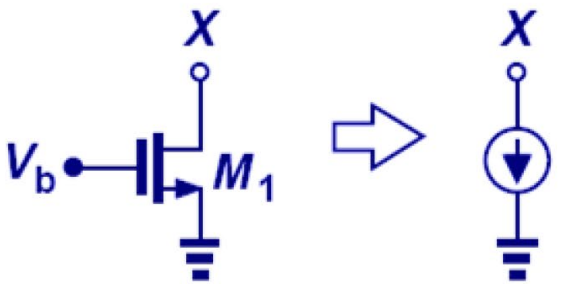


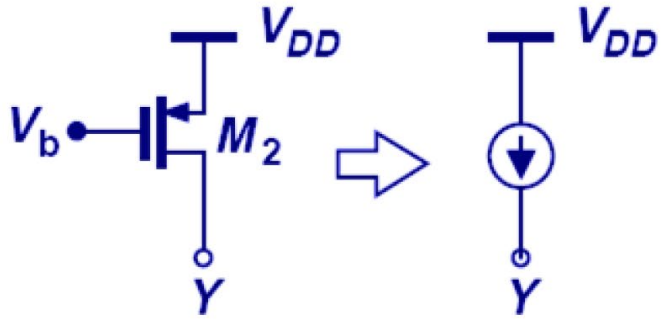
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

Saturation Circuit Model

- The MOSFET in saturation is a voltage-controlled current source

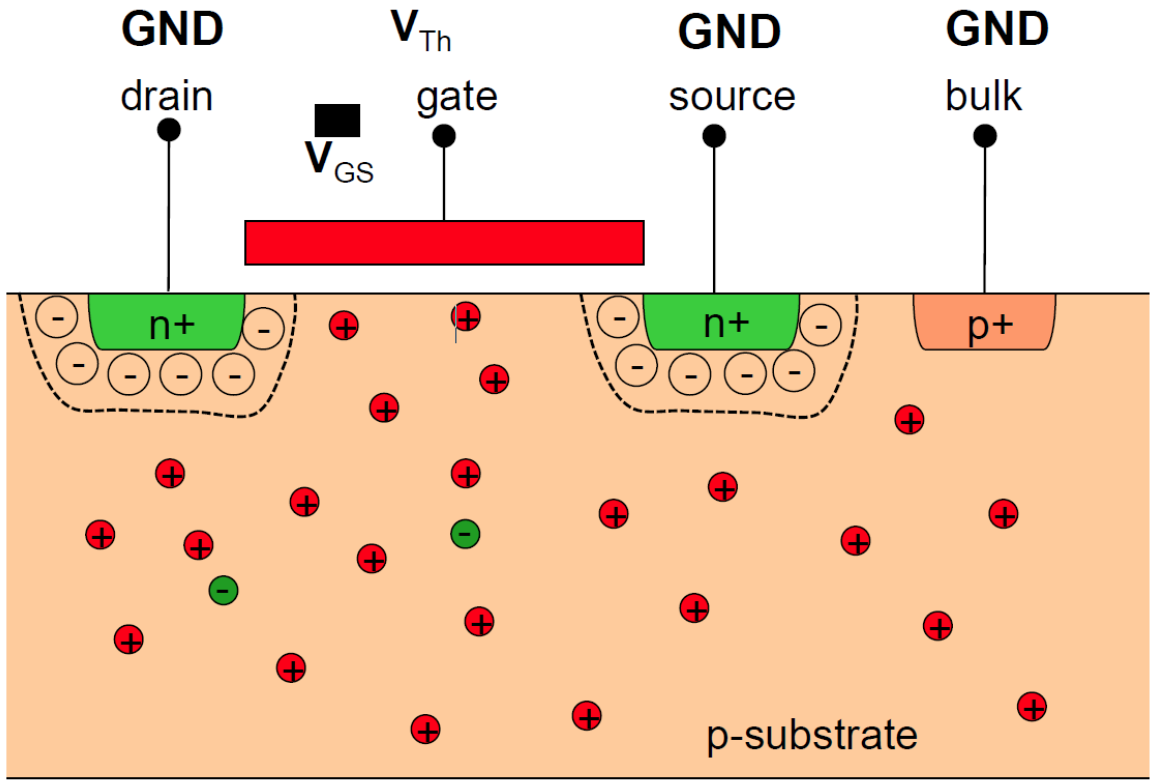




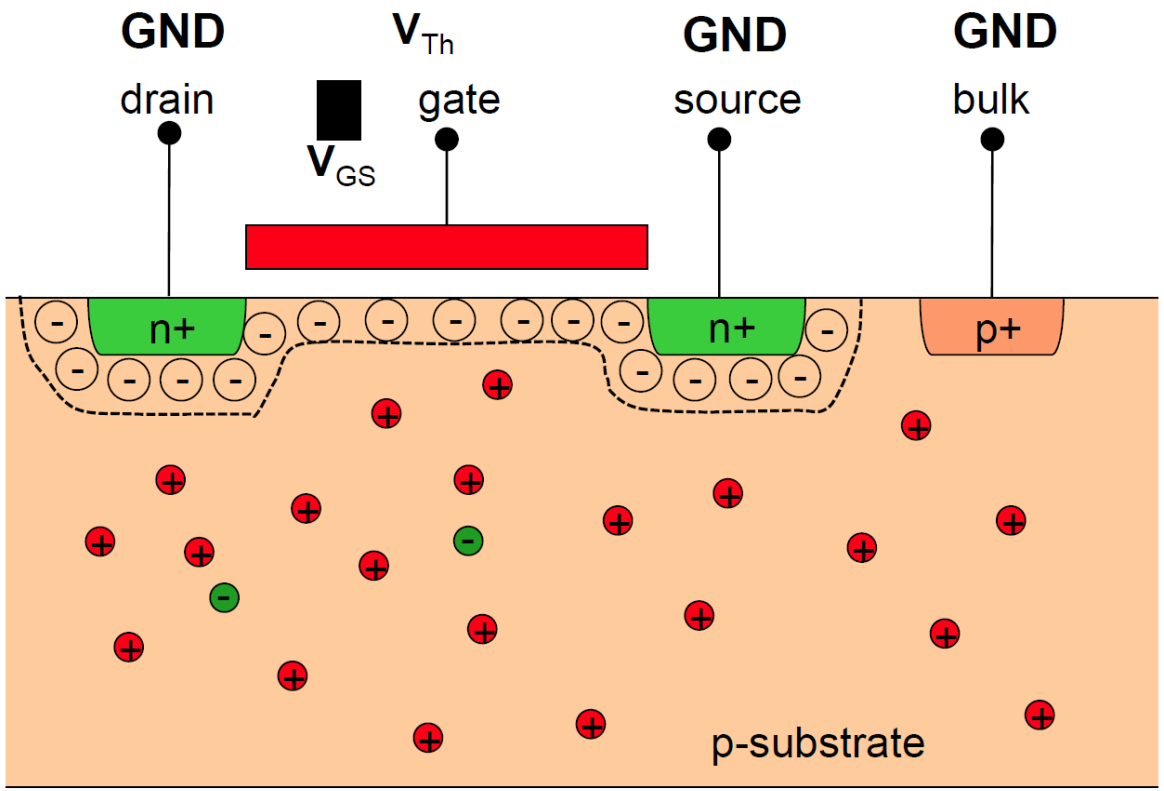


Backup slides - MOSFET

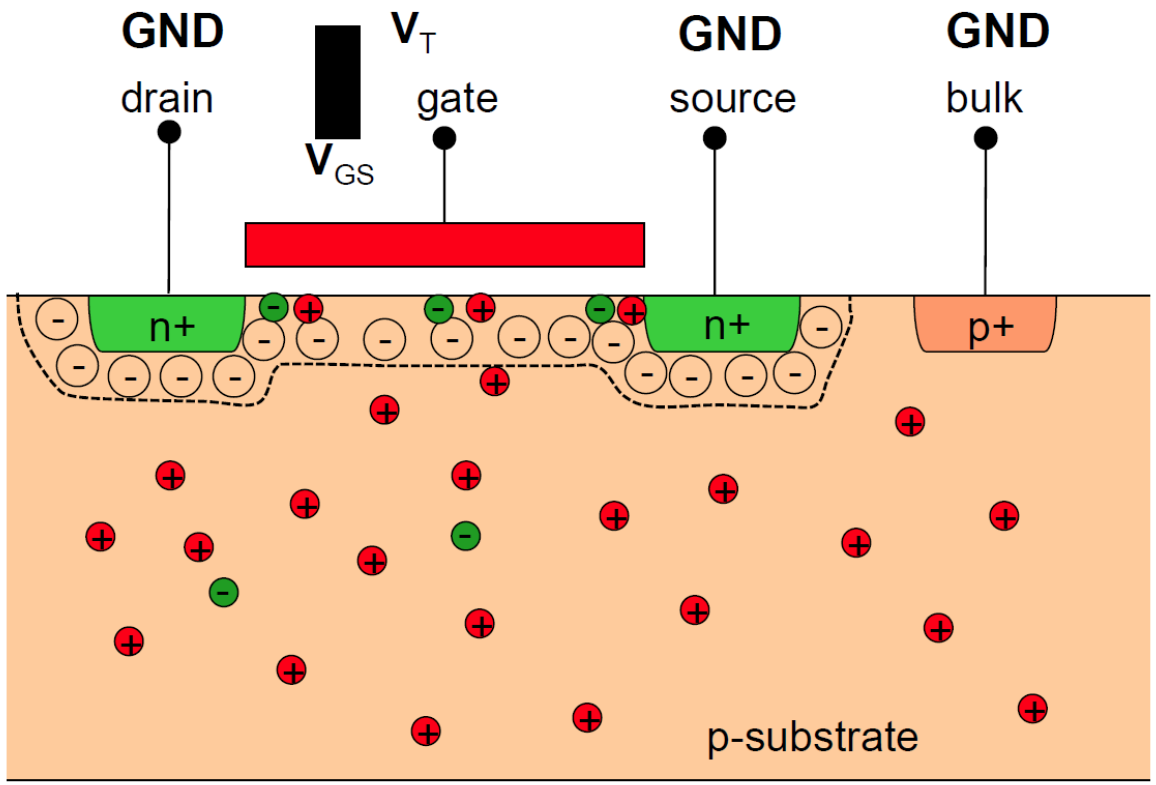
Inversion Channel And Gate Voltage



Inversion Channel And Gate Voltage

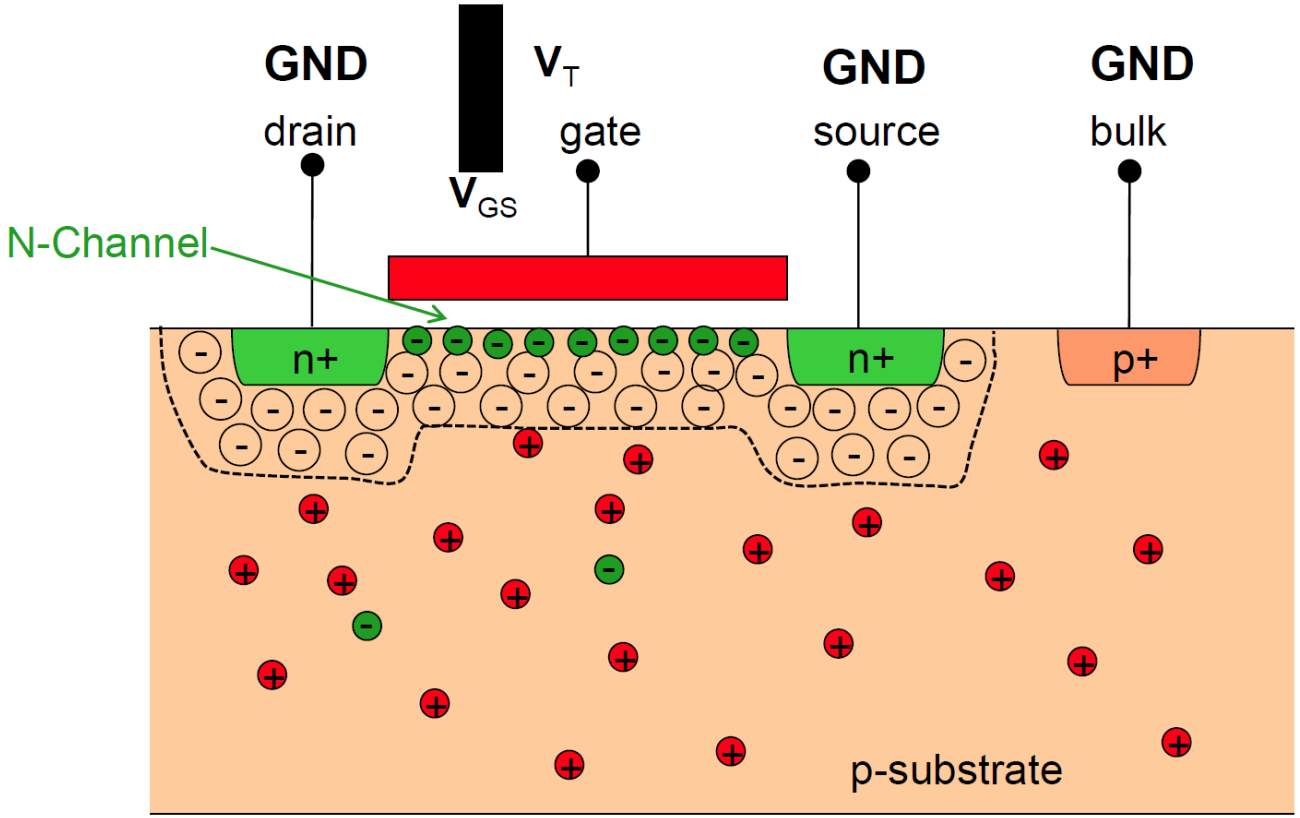


Inversion Channel at Threshold



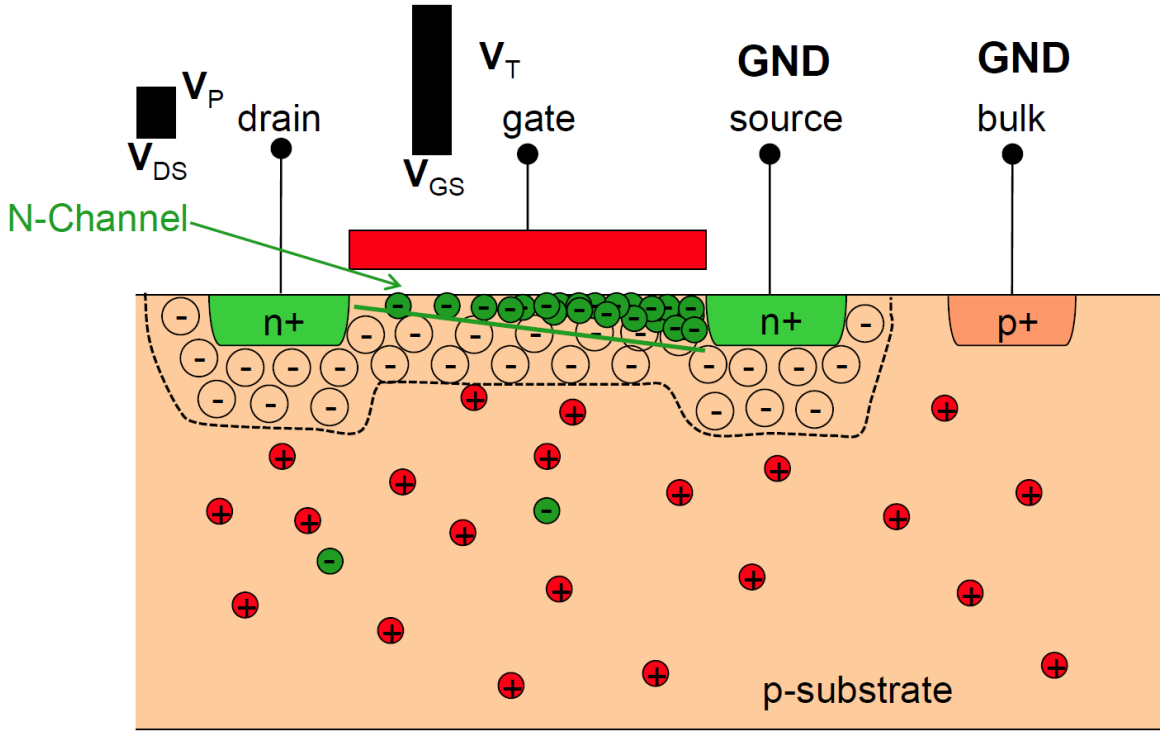
$V_G = V_{Th}$ => #electrons = #holes in the channel

Inversion Channel



Channel Current

- $V_{DS} > 0$, potential at oxide silicon interface rises from S to D
- Potential difference between gate and oxide silicon interface decreases as it approaches the drain ($V_{GS} - V_{DS}$), electron density decreases accordingly



Channel Pinch-Off

- At $V_{GS} - V_{DS} \leq V_{TN}$ -> channel ceases to exist
- Pinch-off voltage: $V_P = V_{GS} - V_{TN}$