

Power Electronics and Applications

Analysis, Design, and Simulation of Buck Converter

School of Electrical and Information Engineering

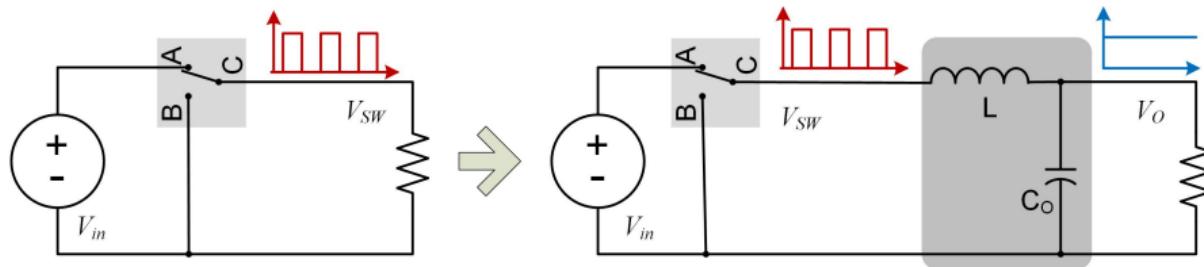
Faculty of Engineering

University of Sydney



- 1 Power train circuits of buck converter
- 2 Fundamental of pulse width modulation (PWM) and switching
- 3 Steady-state analysis of power train circuits
- 4 Continuous conduction mode (CCM)
- 5 Discontinuous conduction mode (DCM)
- 6 Circuit specification and design of buck converter for CCM
- 7 Case study of buck converter
- 8 Simulation of buck converter
- 9 Recommended design procedure of DC/DC converter
- 10 Summary
- 11 Problems to Practice

- Loss-free concept \implies switching!
- ON/OFF switching produces **pulsed voltage waveform** that is useful for **controlling power flow** from source to load.
- Most electrical loads prefer to be supplied by **constant voltage**.
- A **low pass filter or smoothing circuit**, formed by LC, can be added, to stop high-frequency pulsed signal and output smooth voltage.

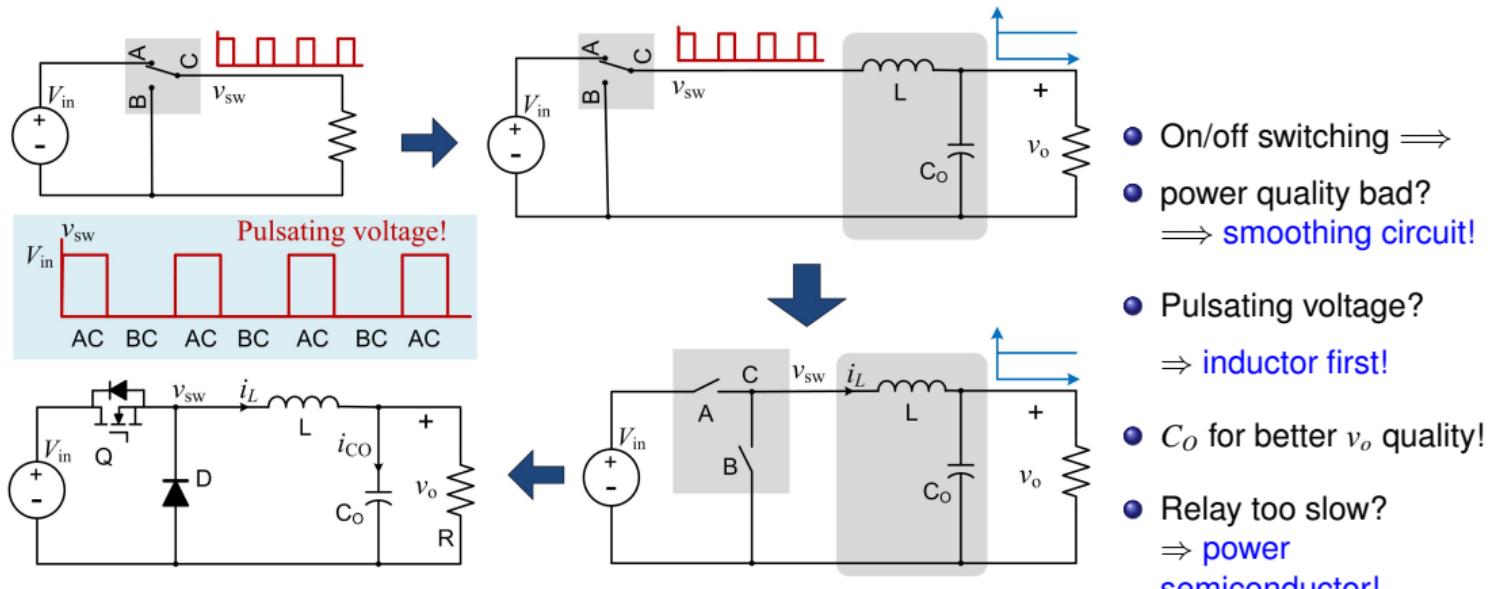


- The circuit becomes the schematic of **non-isolated buck converter**.

Section 1

Power train circuits of buck converter

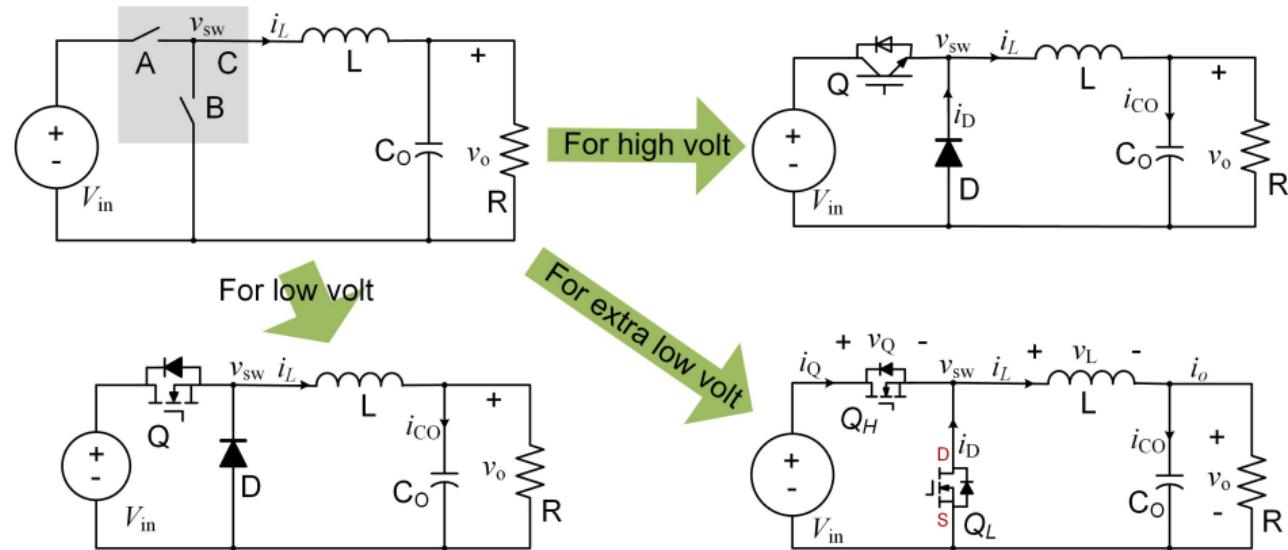
Section 1 Power train circuits of buck converter



Full-time connection (100%) of 'AC' leads to full power flow and $v_{sw} = V_{in} = v_o$

- The **active switching** controls the **pulse width** during 'AC' connection period to achieve **part-time power flow and desired output voltage**, v_o .
- The **freewheeling diode (D)** is a passive switch but effective to support the BC connection.

Section 1 Power train circuits of buck converter



- Power flow is controlled by timing the on-state of the active switch, Q or Q_H .
- Voltage step-down due to $v_o \leq V_{in} \implies$ 'Buck!'
- Synchronous rectifier: two-quadrant characteristics of MOSFETs used to replace and simulate diode for low loss in ELV applications. short-circuit risk!

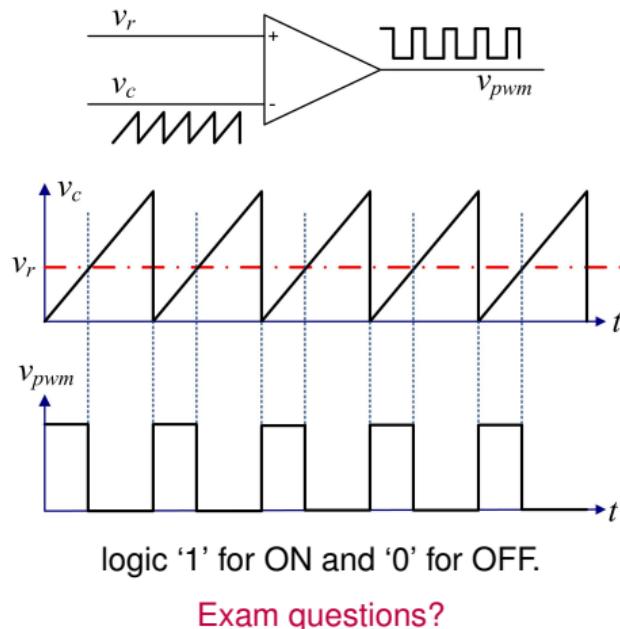
Section 2

Fundamental of pulse width modulation (PWM) and switching

PWM \Rightarrow proper timing to control power follow!

Section 2 Fundamental of pulse width modulation (PWM) and switching

- Pulse-width modulation (PWM) is a systematic way to regulate switching sequence and level of power flow.
- The PWM signal can be formed either **digitally** or by analog circuit, which follows the same mechanism by **comparing carrier (v_c) and reference v_r** :



Exam questions?

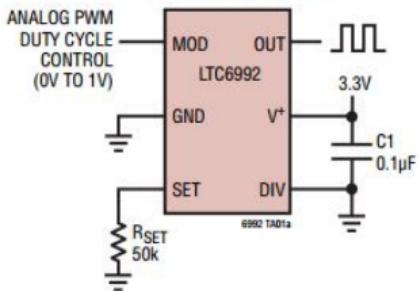
- Carrier signal: either sawtooth or triangle signal carrying the **switching frequency, f_{sw}** .
- Reference, v_r , is the control variable adjustable high or low for modulation.
- Comparator produces and outputs **different pulse width** by adjusting v_r .
- PWM signal shows controllable pulse width and control the active switch:
- Key parameters** of PWM signal:
 - Duty ratio**: percentage of ON or OFF
⇒ on-state duty or off-state duty;
 - switching frequency**

Section 2 Analog implementation of pulse width modulation (PWM)

- For experimental test, PWM signal can be generated by a **function generator** for **programmable frequency and duty cycle**.
- The 555 timer is an integrated circuit that **used to be popular** in electronics for pulse generation, time delay generation, and PWM.



1MHz Pulse Width Modulator

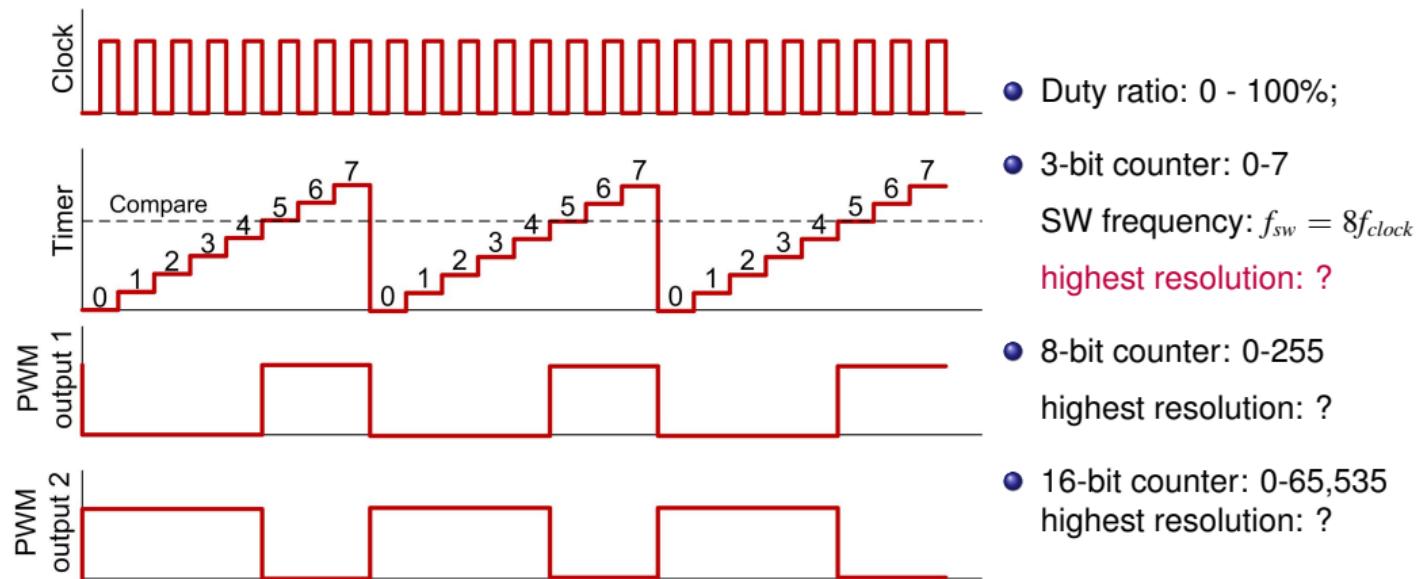


www.linear.com

- The latest IC, e.g. Linear LTC6992, makes the circuit for PWM **even easier**.
- Carrier signal produced **inside** the IC with the **switching frequency programmed** by R_{set} .
- Operation follows the same principle comparing carrier signal with reference.
- Duty cycle or pulse width can be varied by the voltage level (v_r) at "MOD".

Section 2 Digital implementation of pulse width modulation (PWM)

- Digitally counting clock pulses and reset when saturation \Rightarrow carrier.
- When a **digital number** is used for the reference to compare with the **counter output**, the duty cycle of pulses can be assigned and varied.
- Clock frequency and counter setting** in micro-controller \Rightarrow **PWM frequency and its resolution**.

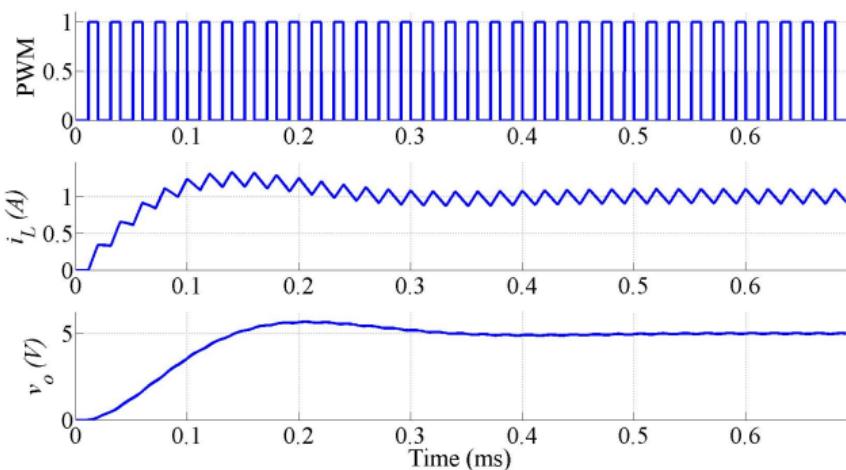


Section 3

Steady-state analysis of power train circuits

VERY IMPORTANT!

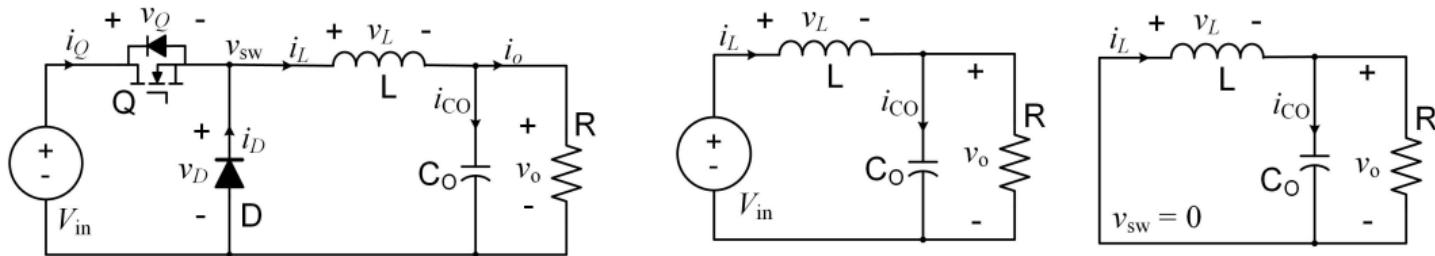
- Different from some steady-state definitions, the converter variables always include **periodic ripples due to ON/OFF switching operation**.
- How to identify the **transient state or steady state**?
- The ripples follow **uniform patterns** in steady state (SS) for converter specification and analysis.



- Steady-state: 0.4-0.8 ms:
 $\text{AVG}(i_L)$ constant!
 $\text{AVG}(v_o)$ constant!
- SS analysis is mainly based on
ripples of:
 current through inductor, i_L
 or/and
 voltage across capacitor, v_o
- Exam question?**
 SS in power converters?
 SS analysis, why? what?

Section 3 ON/OFF switching operation of buck converter

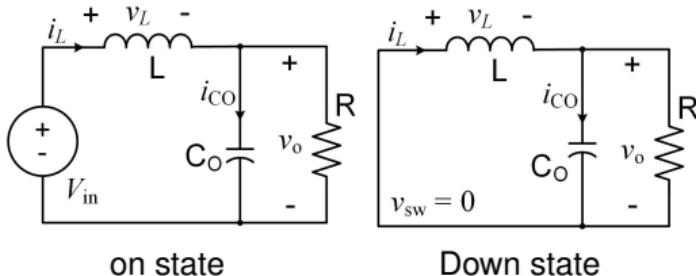
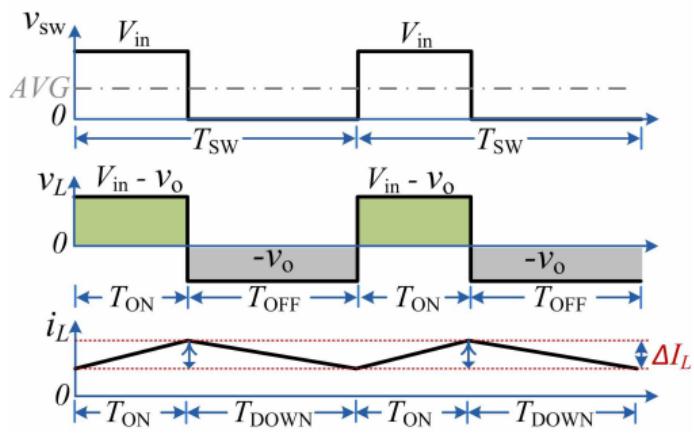
- Active switch, Q, is periodically turned ON/OFF controlled by assigned PWM signal.
- When Q is conducting, D is reversed biased due to $v_{sw} = V_{in} > 0$.



- At the on state, Q is conducting, and the **inductor current rises**, $i_L \uparrow$, since $v_L > 0$ & $v_L = V_{in} - v_o$.
- When Q is turned off, unstoppable inductor current (i_L) force the **diode forward-biased** to form a conducting loop and lease storaged energy.
- Without source, $i_L \downarrow$ due to the **discharge from the load**, R, at the down state.

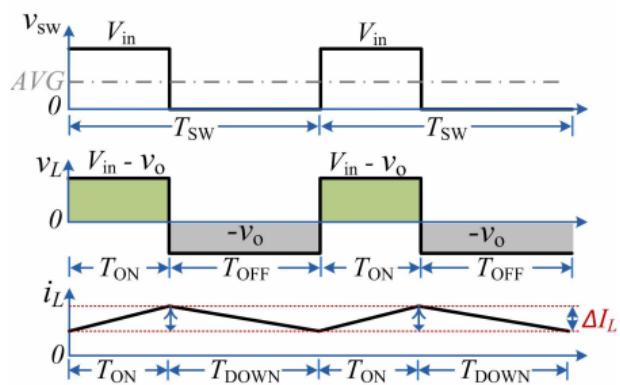
$$v_L = -v_o, \text{ negative in value!} \quad L \frac{di_L}{dt} = v_L = -v_o \implies i_L \downarrow$$

Section 3 Periodic steady state of inductor current



- The principle of **inductor volt-second balance** is defined in Ericson book (P.20).
 - In the textbook, the SS condition can be simply explained as the **averaged value of i_L becomes constant**.
 - The rising ripple of i_L is equal to dropping value to maintain a constant average value.
- In SS, integration of voltage across inductor is zero: $0 = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_L(t) dt$.

Section 3 Periodic steady-state analysis based on ON/OFF operation

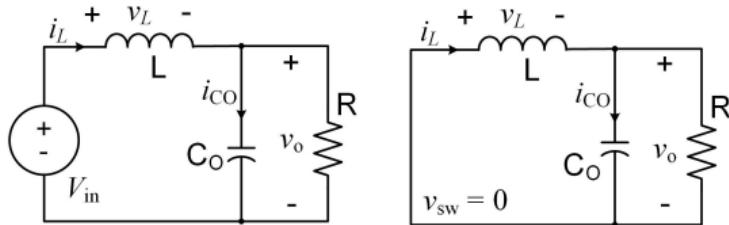


- Rising in continuous time:

$$L \frac{di_L}{dt} = V_{in} - V_o > 0$$

- Rising ΔI_L in discrete time:

$$L \frac{\Delta I_L}{T_{ON}} = V_{in} - V_o \Rightarrow \Delta I_L = \frac{V_{in} - V_o}{L} T_{ON}$$



- Down-state in continuous time: $L \frac{di_L}{dt} = -V_o$
- Dropping ΔI_L in discrete time: $-\Delta I_L = \frac{-V_o}{L} T_{DOWN}$
- V_o is averaged v_o , and constant in SS.
- Peak-to-peak ripple, ΔI_L , repeats.

$$\frac{V_{in} - V_o}{L} T_{ON} = -\frac{-V_o}{L} T_{DOWN}$$

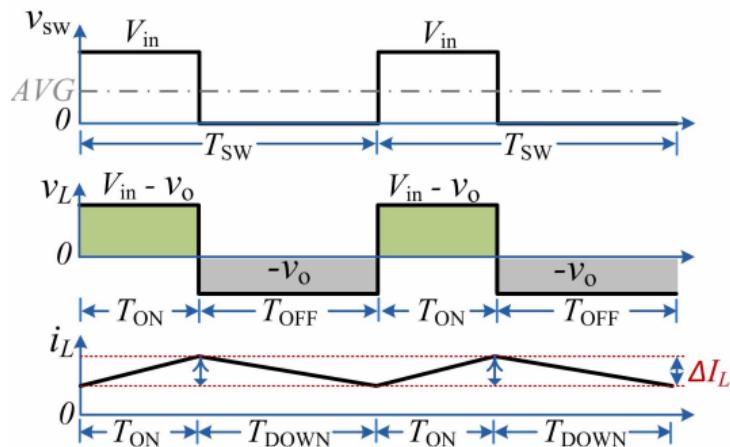
$$\Rightarrow \frac{V_o}{V_{in}} = \frac{T_{ON}}{T_{ON} + T_{DOWN}} \underbrace{\leq 1}_{buck}$$

Section 4

Continuous conduction mode (CCM)

Section 4 Continuous conduction mode (CCM) of the inductor current

- Continuous conduction mode (CCM) is defined that the inductor current is **never saturated at the zero level in SS** when diode is used as the lower switch.



- Fixed switching cycle: $T_{SW} = 1/f_{sw}$

- f_{sw} : switching frequency

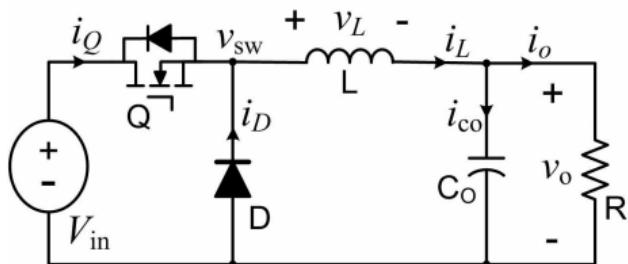
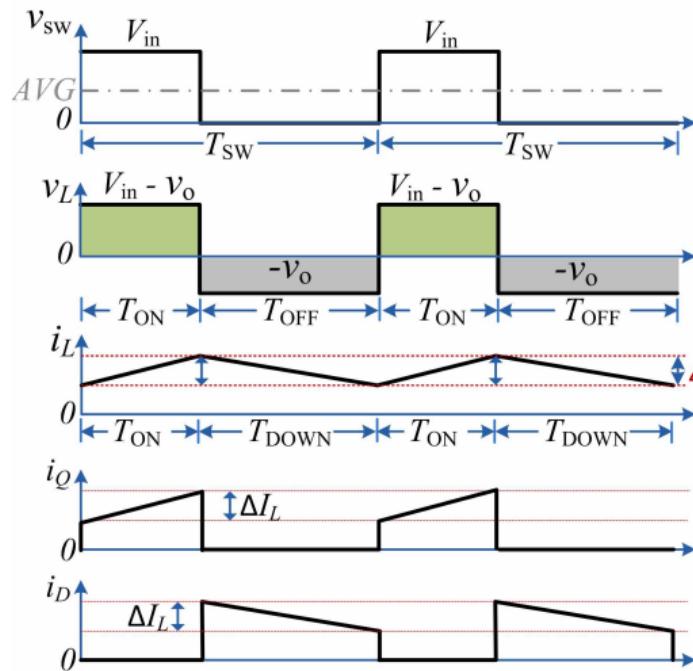
- One switching cycle: $T_{SW} = T_{ON} + T_{OFF}$

- At CCM, $T_{ON} + T_{DOWN} = T_{SW}$.

- The modulation index of CCM can be represented by the value of T_{ON} .
- The **duty ratio** of the on-state is defined by: $D_{ON} = \frac{T_{ON}}{T_{SW}}$ for the PWM.
- At CCM, $\frac{V_o}{V_{in}} = \frac{T_{ON}}{T_{ON} + T_{DOWN}} = D_{ON}$, proportional and independent of load condition.

Section 4 Continuous conduction mode (CCM) of the inductor current

- i_Q is a pulsed waveform representing current through the active switch, Q.
- i_D is a pulsed waveform representing current through the passive switch, D;

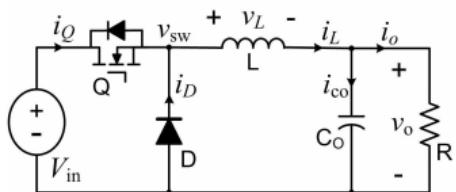


- $i_L = i_Q$ during T_{ON} .
- $i_L = i_D$ during T_{DOWN} .
- Input power: $P_{in} = V_{in} \times AVG(i_Q)$.
- Output power? η ? **Exam question?**

Section 5

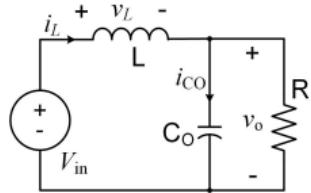
Discontinuous conduction mode (DCM)

Section 5 Discontinuous conduction mode (DCM) of the inductor current

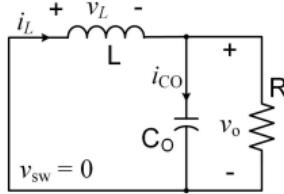


- The discontinuous conduction mode (DCM) happens since the freewheel diode only allows current to conduct at one direction.
- DCM is defined that the inductor current is down to the zero level for a certain time period (T_{ZERO}) during each periodic cycle at SS.

- On state: $i_L \uparrow$



- Down state: $i_L \downarrow$

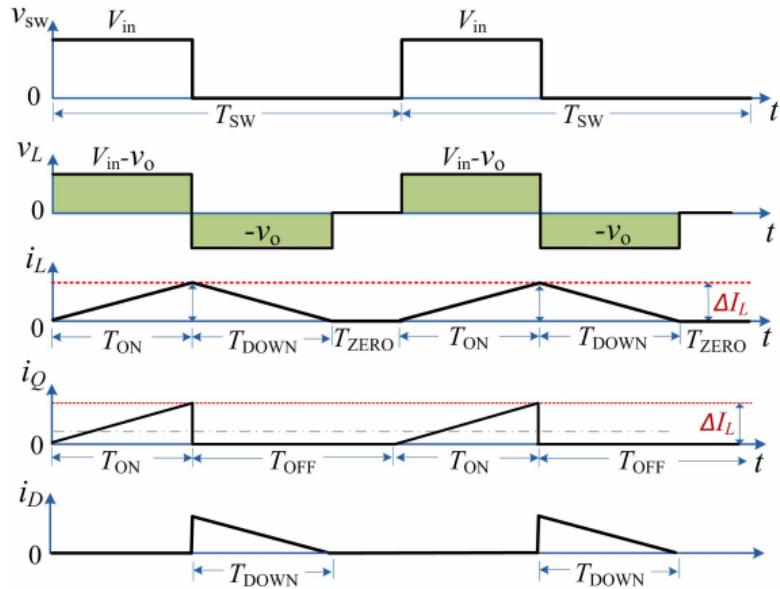
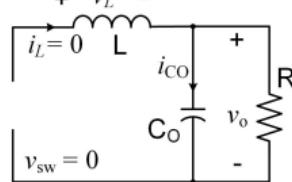


- Zero state: D stops

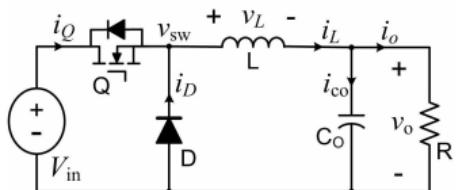
$$\Rightarrow i_L = 0:$$

$$T_{DOWN} \neq T_{OFF}$$

$$T_{SW} > T_{ON} + T_{DOWN}$$

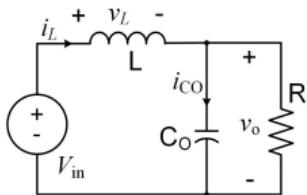


Section 5 Discontinuous conduction mode (DCM) of the inductor current

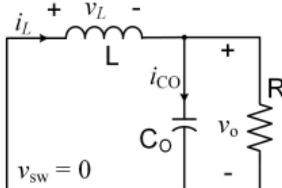


- DCM is caused by insufficient energy stored inside L released during the off state, T_{OFF} .
- DCM is caused by low level of $AVG(i_L)$ or low $AVG(i_o)$ in comparison with ripple amplitude, ΔI_L .

- On state: $i_L \uparrow$



- Down state: $i_L \downarrow$

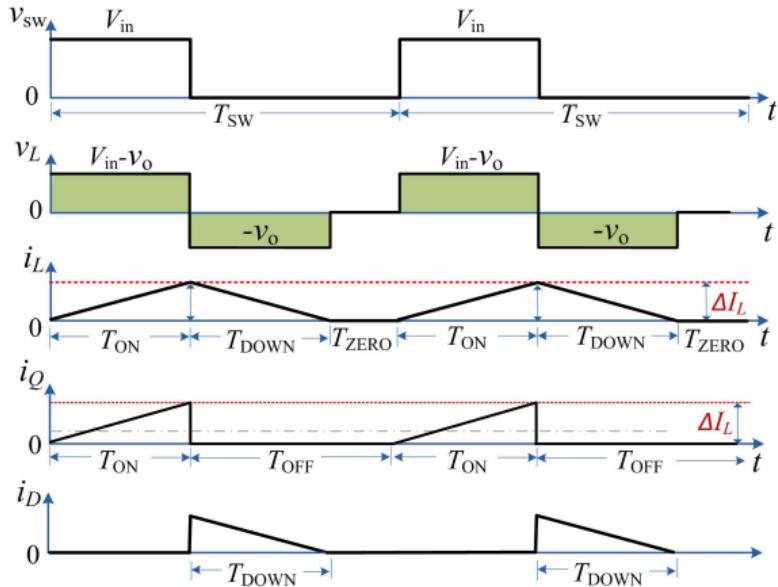
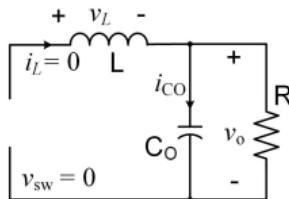


- Zero state: D stops

$$AVG(i_L) < \frac{\Delta I_L}{2}$$

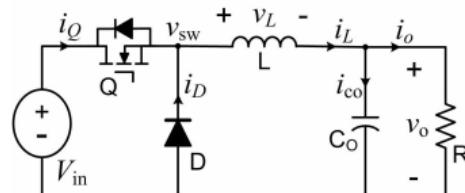
$$T_{OFF} > T_{DOWN}$$

$$\Rightarrow i_L = 0:$$



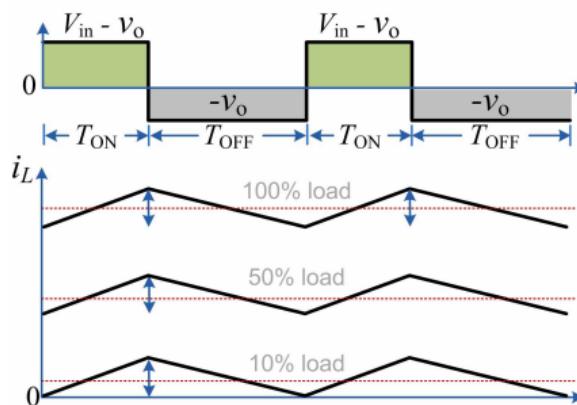
Section 5 Transition between CCM and DCM of the inductor current

- CCM is preferred for high power density, but DCM happens when the **load current is significantly low**.
- Case study: $\Delta I_L = 20\% \text{AVG}(i_L)$ in nominal steady-state $\Rightarrow i_L$ floating high above zero \Rightarrow CCM!
- When load is down to 10% of the nominal condition, i_L enters **boundary conduction mode (BCM)**!



- Critical condition or **boundary conduction mode (BCM)**:

$$\text{AVG}(i_L) = \frac{\Delta I_L}{2} \quad \text{or} \quad \frac{V_o}{R} = \frac{\Delta I_L}{2}$$



- BCM shows i_L touches zero at the end of T_{OFF} ;

- BCM is a special condition of CCM!

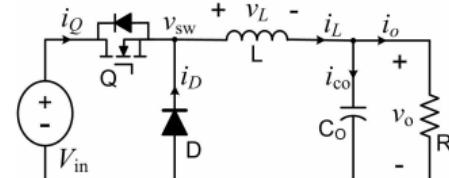
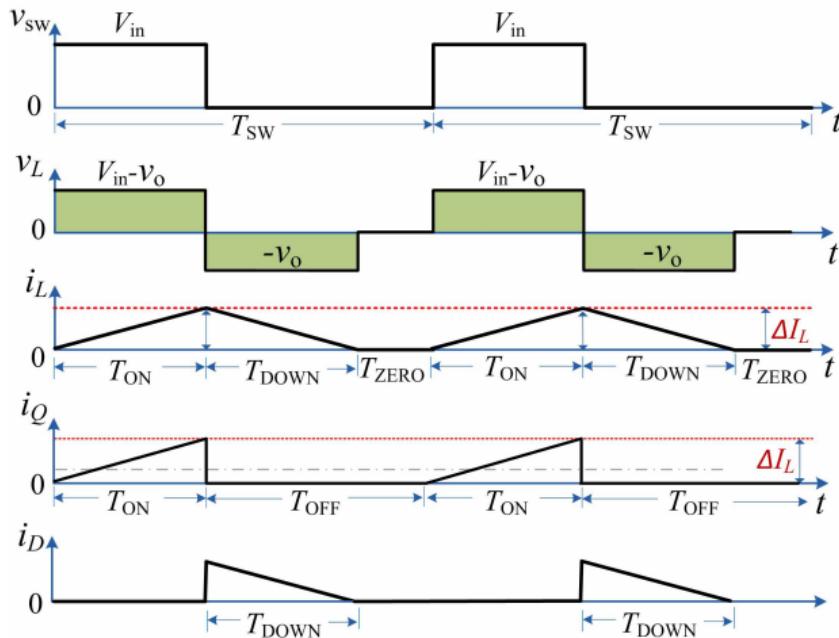
- Operation enters DCM when $\text{AVG}(i_L) < \frac{\Delta I_L}{2}$ or $\frac{V_o}{R} < \frac{\Delta I_L}{2}$;

- Exam questions:**

- explain BCM?
- voltage conversion ratio of BCM at SS?
- $R \Rightarrow$ BCM
- cause of DCM

Section 5 Discontinuous conduction mode (DCM) of the inductor current

- Based on the constant AVG(i_L) in SS, the analysis try to derive the output voltage level, V_o .



Rising ΔI_L in discrete time:

$$\Delta I_L = \frac{V_{in} - V_o}{L} T_{ON}$$

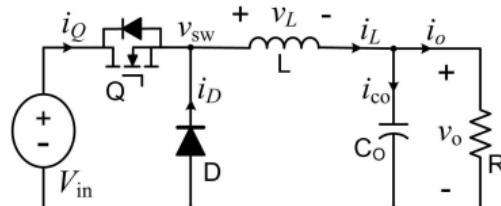
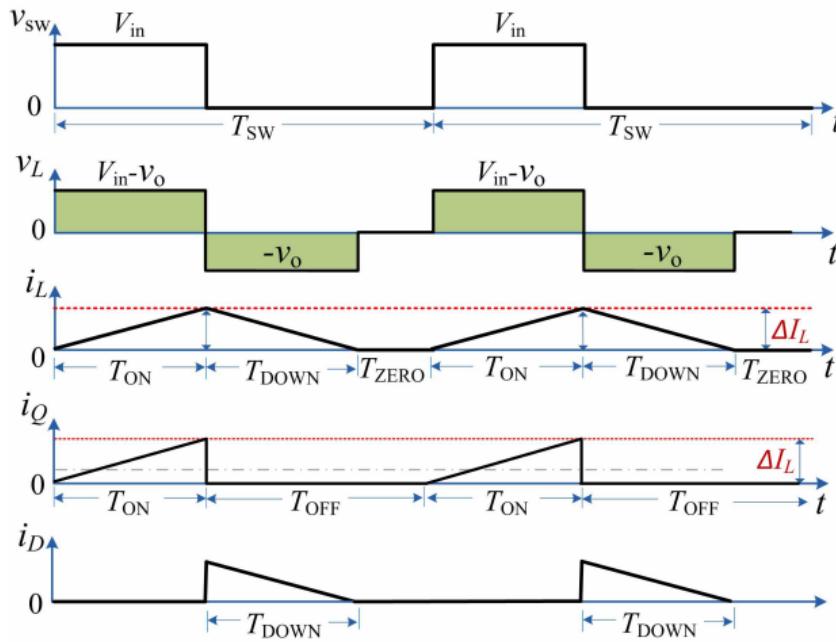
Dropping ΔI_L in discrete time:

$$-\Delta I_L = \frac{-V_o}{L} T_{DOWN}$$

- Voltage conversion ratio in steady state is derived: $\frac{V_o}{V_{in}} = \frac{T_{ON}}{T_{ON} + T_{DOWN}}$.
- T_{ON} is known! but T_{DOWN} unknown!

Section 5 Periodic steady-state analysis of DCM through current equivalence

- Find out the three unknowns: ΔI_L , V_o and T_{DOWN} !



- On state $i_L \uparrow$

$$\Delta I_L = \frac{V_{in} - V_o}{L} T_{ON} \quad (1)$$

- Down state $i_L \downarrow$

$$-\Delta I_L = \frac{-V_o}{L} T_{DOWN} \quad (2)$$

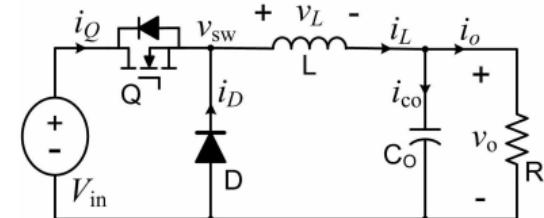
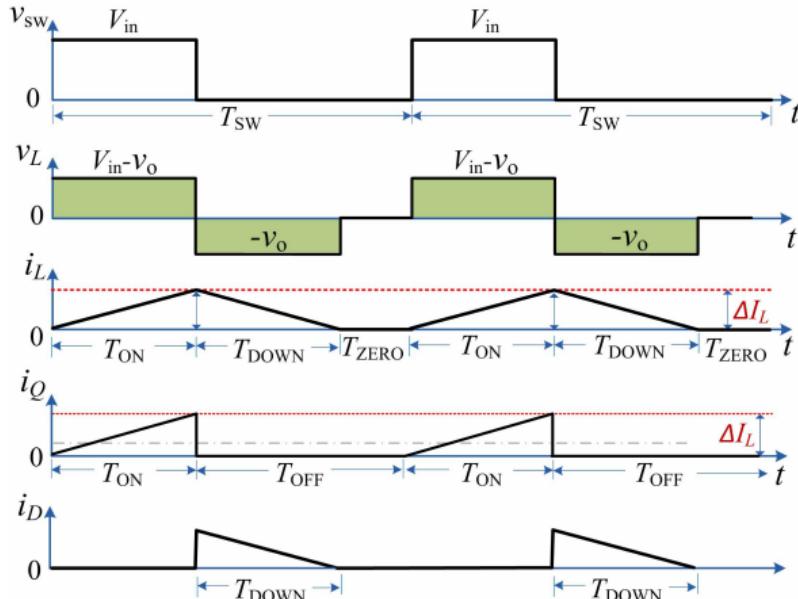
- Averaging: $\text{AVG}(i_L) \equiv \frac{V_o}{R}$

$$\frac{V_o}{R} = \frac{\Delta I_L (T_{ON} + T_{DOWN})}{2T_{SW}} \quad (3)$$

- Combining (1)-(3), V_o in SS, can be determined by: $(\underbrace{2T_{SW}L}_{a})V_o^2 + (\underbrace{V_{in}RT_{ON}^2}_{b})V_o + (\underbrace{-V_{in}RT_{ON}^2}_{c}) = 0$

Section 5 Periodic steady-state analysis of DCM through power balance

- At DCM, the initial value of i_Q is zero, and increases to the peak, ΔI_L at the end of T_{ON} .



- Peak of i_Q determined by:

$$\Delta I_L = \frac{V_{in} - V_o}{L} T_{ON}$$

- Power balance in steady state:

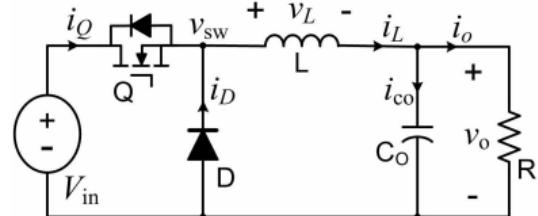
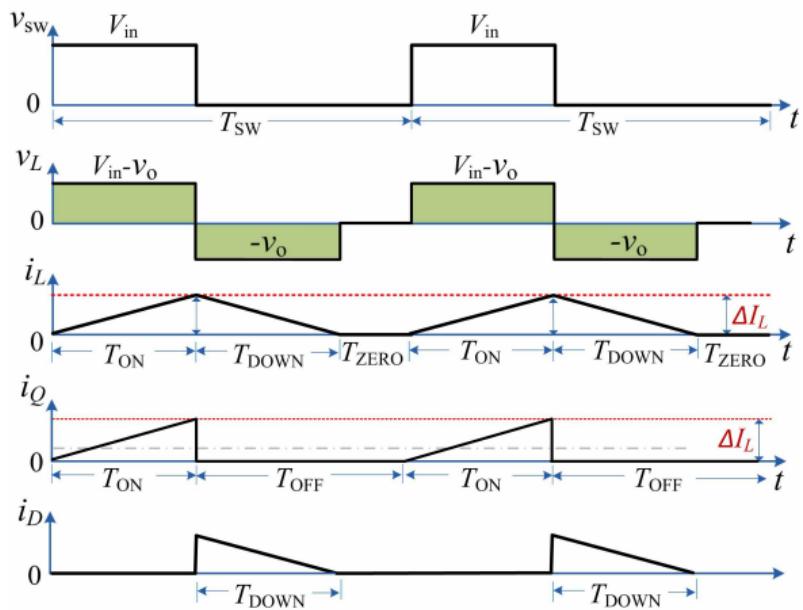
$$V_{in} \times AVG(i_Q) = \frac{V_o^2}{R}$$

$$(2T_{SW}L)V_o^2 + (V_{in}RT_{ON}^2)V_o + (-V_{in}^2RT_{ON}^2) = 0$$

a b c

$$AVG(i_Q) = \frac{\Delta I_L \times T_{ON}}{2} \times \frac{1}{T_{SW}} = \frac{(V_{in} - V_o) \times T_{ON}^2}{2LT_{SW}}$$

Section 5 Periodic steady-state analysis of DCM through power balance



$$(2T_{SW}L)V_o^2 + (V_{in}RT_{ON}^2)V_o + (-V_{in}^2RT_{ON}^2) = 0$$

a *b* *c*

- One unknown, V_o can be determined by

$$V_o = \frac{-b + \sqrt{b^2 - 4ac}}{2a}$$

- In DCM, the value of V_o is related to the **load condition**, R .
- Always determine the BCM and evaluate the conduction mode before jumping to computation since DCM is different from CCM!
- Universal expression for both CCM and DCM: $\frac{V_o}{V_{in}} = \frac{T_{ON}}{T_{ON} + T_{DOWN}}$.

Section 6

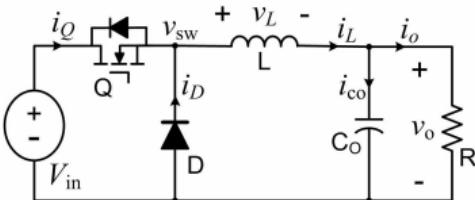
Circuit specification and design of buck converter for CCM

- Specification of buck converter

- Power rating (W) or load resistance (Ω)
- Nominal input voltage in average: V_{in}
- Nominal output voltage in SS: V_o
- Switching frequency: $f_{sw} = 1/T_{sw}$
- Nominal peak-to-peak ripple of inductor current: ΔI_L
- Nominal peak-to-peak ripple of output voltage: ΔV_o

- Design of buck converter circuit

- Calculate duty cycle, D_{ON} , mostly in CCM
- Calculate the inductance: L
- Calculate the capacitance: C_o
- Select power semiconductors based on voltage and power rating.



- Duty cycle of on state in CCM:

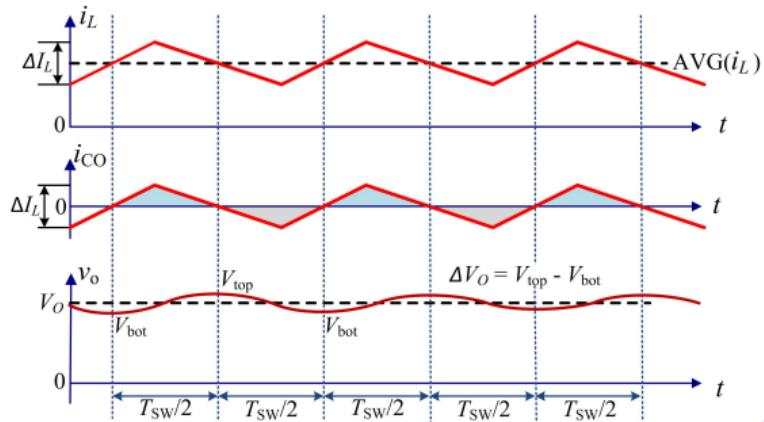
$$D_{ON} = \frac{V_o}{V_{in}} \implies T_{ON} = D_{ON} T_{sw}$$

Inductance rating:

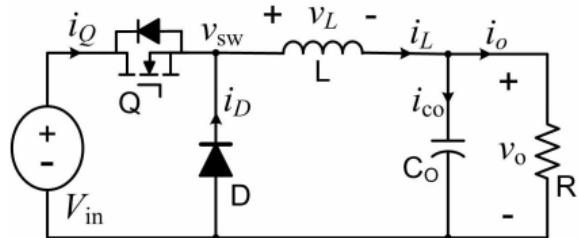
$$\Delta I_L = \frac{V_{in} - V_o}{L} T_{ON}$$

$$\Rightarrow L = \frac{V_{in} - V_o}{\Delta I_L} T_{ON}$$

- At SS, assume v_o is ideal DC and low in ripple, and the waveform of $i_o = \text{AVG}(i_L)$ can estimated as a straight line in steady state.



- Exam question: Role of C_o ?



$$i_{CO} = i_L - i_o = i_L - \frac{v_o}{R}$$

AC signal! Peak-to-peak ripple of $i_{CO} = \Delta I_{CO}$

$i_L > i_o \implies i_{CO} > 0 \implies C_o$ is charged by the surplus half cycle $\implies v_o \uparrow \quad V_{bot} \implies V_{top}$

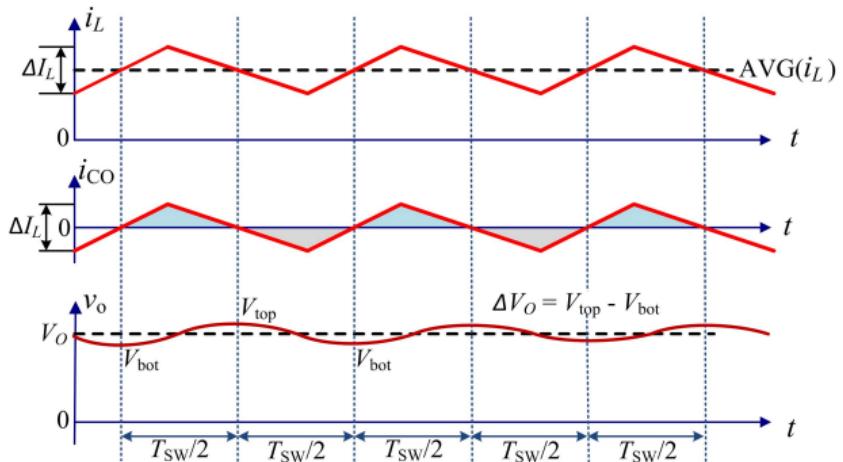
$i_L < i_o \implies i_{CO} < 0 \implies C_o$ is discharged by the deficient half cycle $\implies v_o \downarrow \quad V_{top} \implies V_{bot}$

- The two sections are equally distributed within T_{SW} in steady state; $\frac{T_{SW}}{2} + \frac{T_{SW}}{2}$.

- During charging of the **surplus half cycle**, the voltage, v_o increases by ΔV_O , from the lowest $v_o(\text{low})$ to the highest $v_o(\text{high})$, $\Delta V_O = v_o(\text{high}) - v_o(\text{low})$.

$$C_O \frac{dv_o}{dt} = i_{co} \implies v_o = \frac{1}{C_O} \int i_{co}(t) dt$$

Surplus cycle ($T_{SW}/2$):



$$v_o(\text{high}) = v_o(\text{low}) + \frac{1}{C_O} \int_0^{T_{SW}/2} i_{co}(t) dt$$

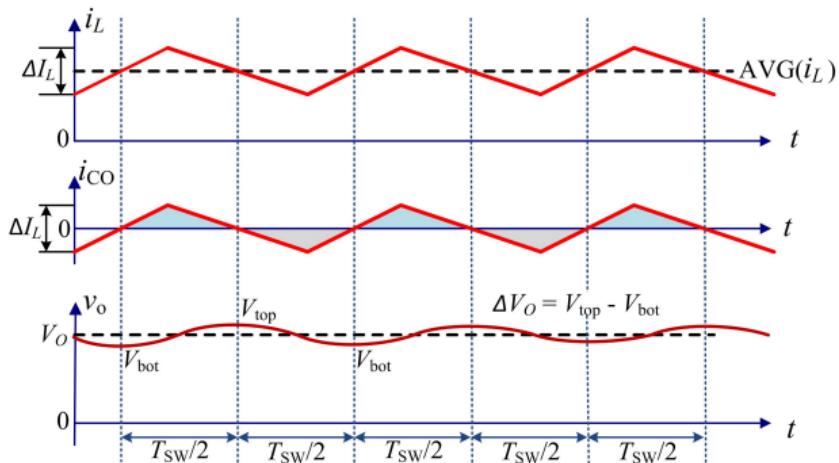
$$\Delta V_O = \frac{1}{C_O} \int_0^{T_{SW}/2} i_{co}(t) dt$$

$$\Delta V_O = \frac{1}{C_O} \underbrace{\left(\frac{1}{2} \frac{\Delta I_L}{2} \frac{T_{SW}}{2} \right)}_{\text{triangle-area}}$$

$$C_O =$$

- During charging of the **surplus half cycle**, the voltage, v_o increases by ΔV_O , from the lowest $v_o(\text{low})$ to the highest $v_o(\text{high})$, $\Delta V_O = v_o(\text{high}) - v_o(\text{low})$.

$$C_O \frac{dv_o}{dt} = i_{co} \implies v_o = \frac{1}{C_O} \int i_{co}(t) dt$$



Surplus cycle ($T_{SW}/2$):

$$v_o(\text{high}) = v_o(\text{low}) + \frac{1}{C_O} \int_0^{T_{SW}/2} i_{co}(t) dt$$

$$\Delta V_O = \frac{1}{C_O} \int_0^{T_{SW}/2} i_{co}(t) dt$$

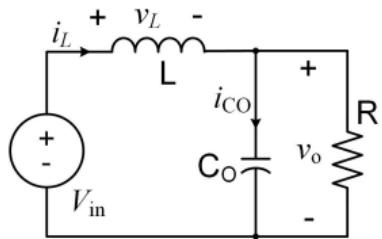
$$\Delta V_O = \frac{1}{C_O} \underbrace{\left(\frac{1}{2} \frac{\Delta I_L}{2} \frac{T_{SW}}{2} \right)}_{\text{triangle-area}}$$

$$C_O = \frac{\Delta I_L T_{SW}}{8 \Delta V_O} \quad \text{or} \quad \frac{\Delta I_L}{8 f_{sw} \Delta V_O}$$

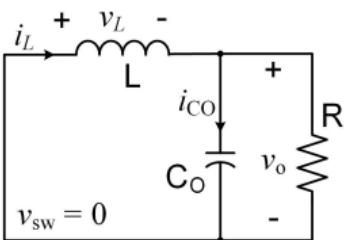
- Specification of buck converter
 - Power rating (W): 5 W
 - Nominal input voltage: $V_{in} = 12 \text{ V}$
 - Nominal output voltage: $V_o = 5 \text{ V}$ for USB charger
 - Switching frequency: $f_{SW} = 50 \text{ kHz}$
 - Nominal peak-to-peak ripple of inductor current: $\Delta I_L = 0.2 \text{ A}$
 - Nominal peak-to-peak ripple of output voltage: $\Delta V_O = 0.05 \text{ V}$
- Design of buck converter circuit
 - Calculate duty cycle, $D_{ON} = 0.42$ at CCM
 - Calculate the inductance: $L = 292\mu$
 - Calculate the capacitance: $C_O = 10\mu$
- Simulation study for concept proof
 - $v_o = V_O$ in steady state?
 - ΔI_L is correct in steady state?
 - ΔV_O is correct in steady state?
- Component selection
 - off-the-shelf inductor? if impossible, build your own!
 - off-the-shelf capacitor
 - MOSFET and driver?
 - Schottky diode?
- Draw a schematic.
- Provide specification of key components.
- Experimental evaluation

Section 8

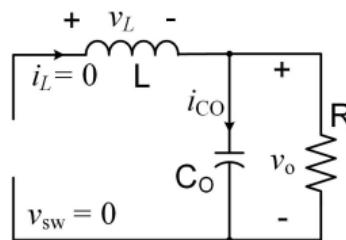
Simulation of buck converter



On state



Down state



Zero state

- on state: $L \frac{di_L}{dt} = V_{in} - v_o$ and $C_O \frac{dv_o}{dt} = i_L - \frac{v_o}{R}$.
- Down state: $L \frac{di_L}{dt} = -v_o$ and $C_O \frac{dv_o}{dt} = i_L - \frac{v_o}{R}$.
- Zero state: $i_L = 0$ and $C_O \frac{dv_o}{dt} = i_L - \frac{v_o}{R}$.
- Simulation model can be built and based on the three states and their dynamic expression.

Section 8 Simulink model of buck converter

on state

$$v_{sw} = V_{in}$$

$$i_L = \frac{1}{L} \int (V_{in} - v_o) dt$$

Down state

$$v_{sw} = 0$$

$$i_L = \frac{1}{L} \int (-v_o) dt$$

Zero state

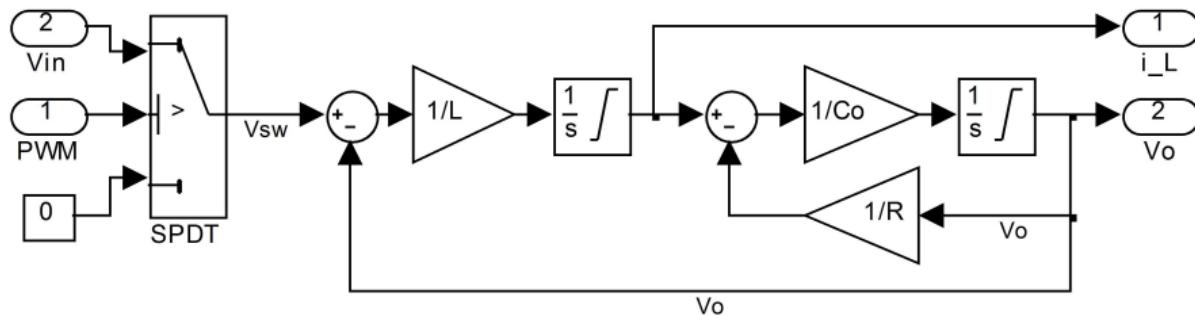
$$v_{sw} = 0;$$

$$i_L = 0$$

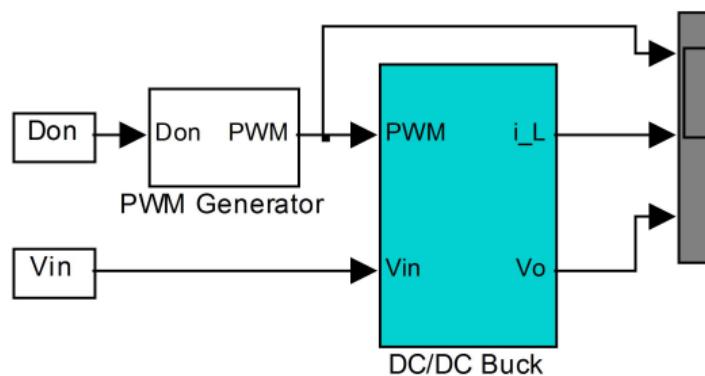
Output voltage

$$v_o = \frac{1}{C_o} \int (i_L - \frac{v_o}{R}) dt$$

- Zero state ($i_L = 0$) share the same as the down state that can be implemented by limiting $i_L \geq 0$ in the simulation block.
- A switch is used to represent the ON/OFF operation and produce the pulsed signal, v_{sw} .



- Based on the comparison mechanism, the PWM generator produces the pulse according to the on-state duty cycle, D_{ON} .
- The output variables include the inductor current and output voltage.
- Simulation time: 1 ms
- Simulation sampling time in discrete mode: $T_{SW}/1000$

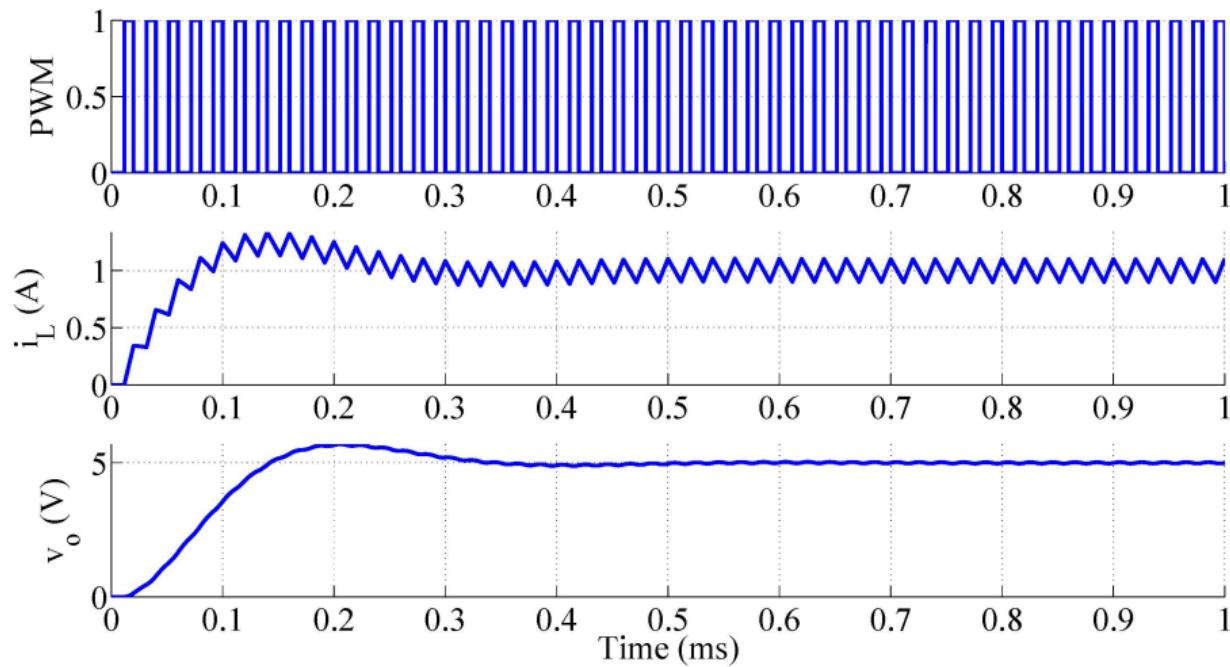


find your way or ask tutors to build the PWM generator model!

Section 8 Simulation result of inductor current and output voltage

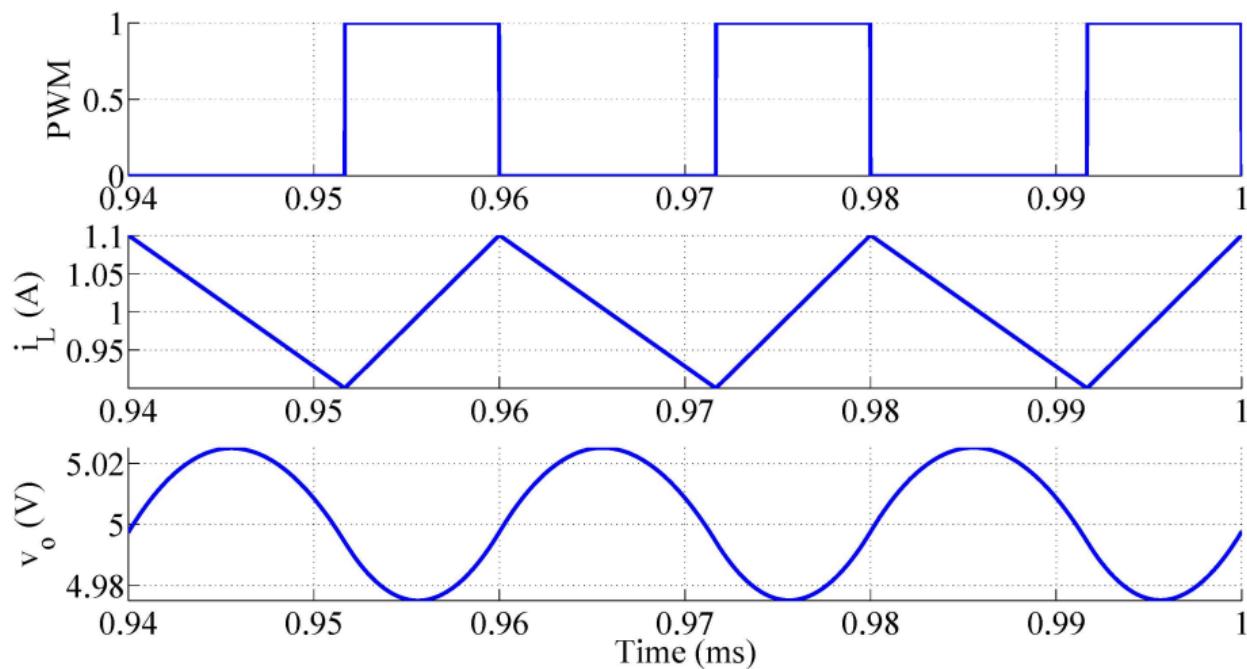
Identify the transient and steady states!

$D_{ON} = 42\% \Rightarrow$ Average of v_o and i_L at SS?? meeting the expectation?? 5W/5V?



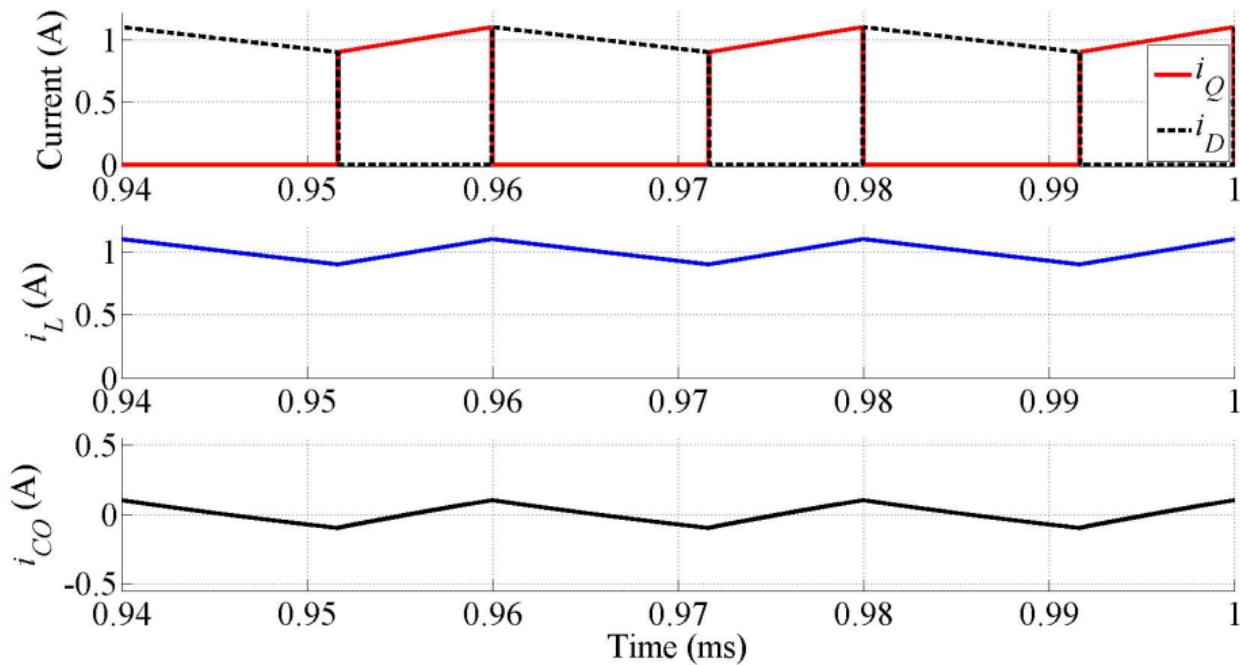
Section 8 Simulation result: zoom-in steady state

$\Delta I_L = ?$; $\Delta V_O = ?$ meeting the expectation?? Nominal: $\Delta I_L = 0.2 \text{ A}$; $\Delta V_O = 0.05 \text{ V}$



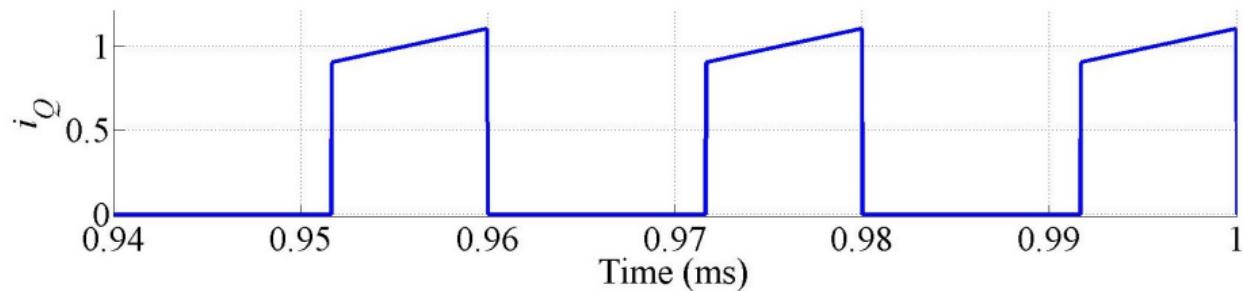
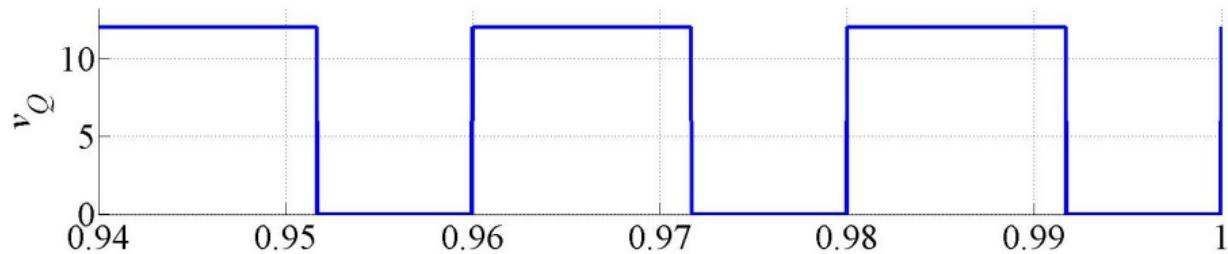
Section 8 Other current signal

- Pulsed waveforms of i_Q and i_D representing current through Q and D;
- i_Q also represents the current drawn from the source according to buck topology.

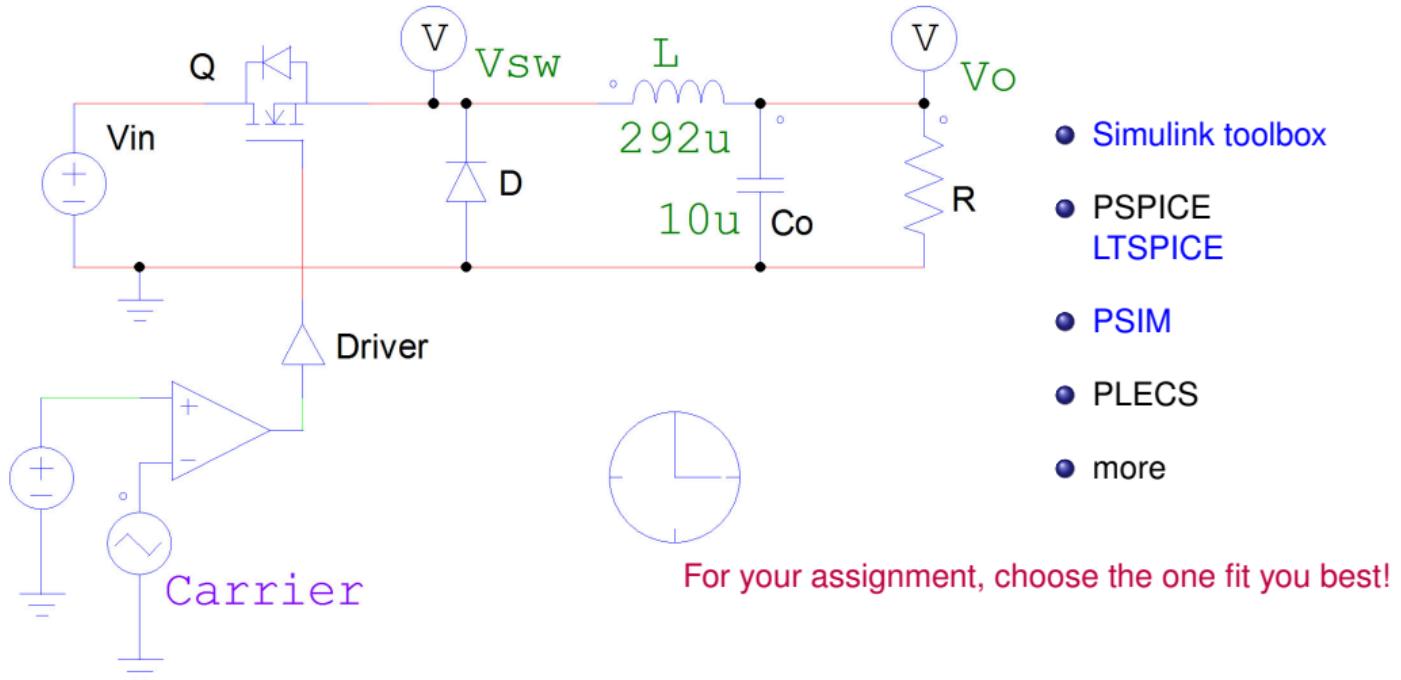


Section 8 Demonstration of hard switching

- Significant voltage across the switch, Q, at the moment of turn-on.
- Significant current through the switch, Q, at the moment of turn-off.
- Hard switching introduce switching loss in proportional to switching frequency.



- Circuit-based platforms are widely used to simulate power electronics.



- Two important simulation parameters:
 - Total simulation time, T_{total}
 - Sampling time or time step, T_{sample}
- T_{total} should be set to meet the simulation requirement, but show no overlength.
- Lower $T_{sample} \Rightarrow$ better simulation resolution and accuracy.
- $T_{sample} = \frac{T_{SW}}{100}$ or $T_{sample} = \frac{T_{SW}}{1000}$ to catch switching details, but not overcook.

Simulation time

Start time: 0.0

Stop time: Ttotal

Solver options

Type: Fixed-step

Solver: ode3 (Bogacki-Shampine)

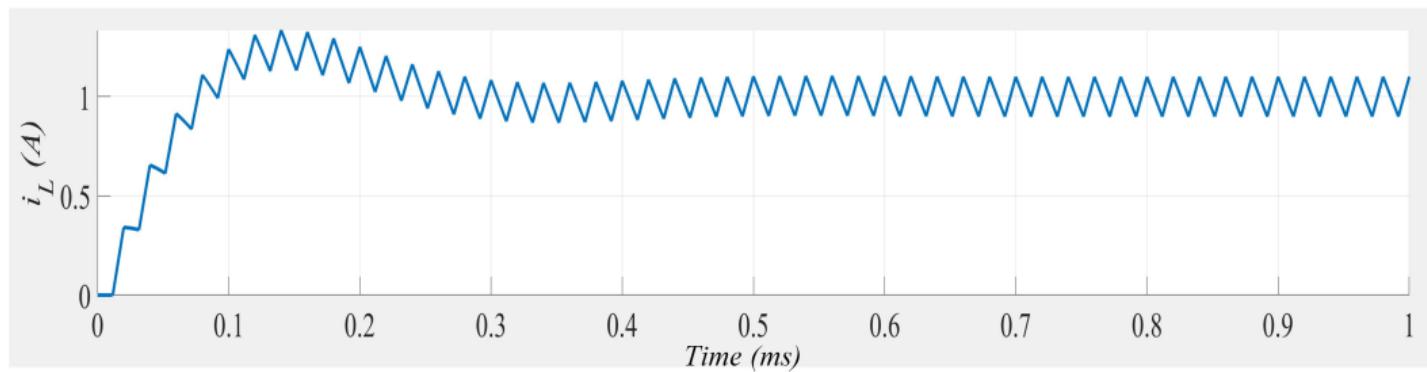
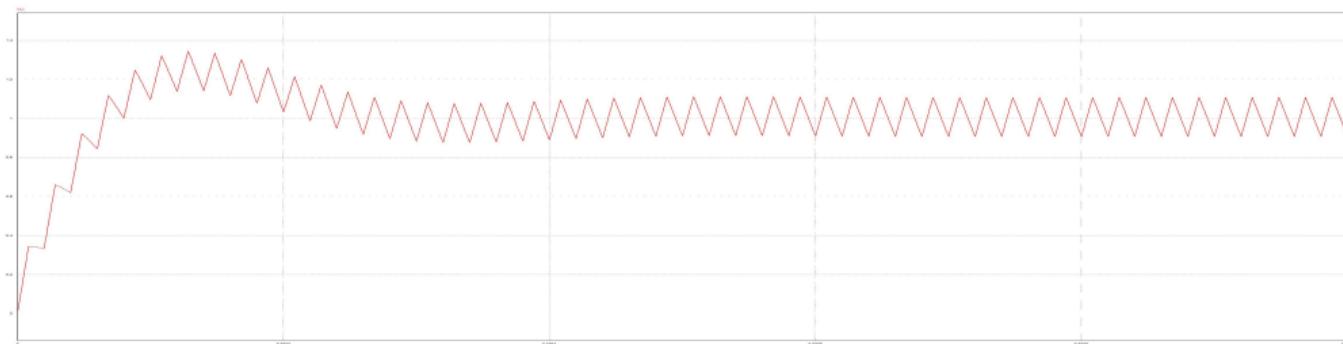
▼ Additional options

Fixed-step size (fundamental sample time):

Tsample

- For $f_{sw} = 50$ kHz,
 $T_{sample} = \frac{T_{SW}}{1000} = 20$ ns.

Section 8 Importance of re-plotting simulation result for high-quality presentation

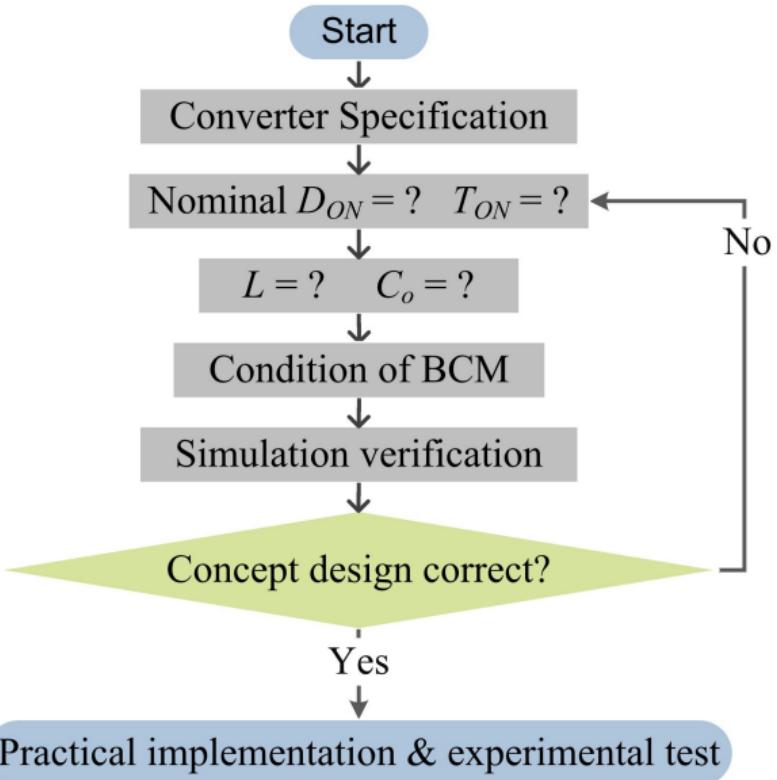


All figures presented in report should be readable! Poor figure \Rightarrow mark deduction!

Section 9

Recommended design procedure of DC/DC converter

Section 9 Recommended design procedure of DC/DC converter



Section 10

Summary

- Non-isolated buck converter are **widely used** in industry for various applications, especially in DC systems, e.g. IT and telecommunication.
- The **ON/OFF switching** operation of power converter cannot change the signal amplitude directly, but can control the pulse width in a certain time period, in order to manipulate the degree of energy transfer.
- **Steady-State (SS) Analysis** computes the periodic steady-state response of a circuit at a fundamental frequency, which is the switching frequency.
- SS analysis is commonly based on the **inductor current** during the on state and off state, which shows a constant averaged value.
- **Definition** of continuous and discontinuous conduction modes (**CCM and DCM**) is also based on the inductor current.

- The theoretical value of **voltage conversion ratio in CCM** is known since it is only correspondent to the duty cycle and independent of load.
- CCM is also preferred in buck converter design due to the high power density and predictable conversion ratio of voltage.
- Light load condition and reverse-biased diode lead the **transition from CCM to DCM**.
- The output voltage cannot be directly calculated if the load condition is **unknown in DCM**.
- **Low-pass filtering** is generally required to recover the smooth waveform in term of either DC and AC for practical implementation.
- Steady-state analysis theoretically reveals the **voltage conversion ratio** and is used to **size the passive components**, L and C filter.

- To reduce the size of inductor and capacitor and maintain the same ripple for the capacitor voltage and inductor current, **high switching frequency** is desirable since it shortens the time period in term of rising and dropping.
- Constraints for high switching frequency lie in the **physical limit** of power semiconductor and switching losses.
- **DC/DC converter design procedure** is proposed in this presentation.
- Simulation is used for a **quick concept proof** to meet the design specification.
- Case study is based on a practical design of DC/DC converter that can be used for USB charger.
- Part of discussion can be found in Section 3.3 of the textbook.

- Industry trend to standardize the package size for DC/DC converters, which is easy for installation and competing **power density and conversion efficiency**.



- DC/DC modules with standard size:
 - Full brick: 117 x 55.9 x 12.7mm
 - Half brick: 57.9 x 55.9 x 12.7mm
 - Quarter brick: 57.9 x 36.8 x 12.7mm
- Selection from the output voltage from 2 to 54 V.
- Power rating:
 - Full brick up to 600 W
 - Half brick up to 300 W
 - Quarter brick up to 150 W

<http://www.vicorpowers.com>

- New challenge: extra low voltage and extra high current for ICT components!

You first assignment can be done this weekend!

You can search support from tutors next week!

Highly recommend you finish the assignment before the lab session on Week 5!

- ① A digital counter is based on the 16-bit register with the 10 MHz clock. When the counter is used to produce 100 kHz PWM signals, determine the best resolution of the duty ratio.
- ② Build your own models for the buck converter. Use the example in this lecture to verify the model accuracy and limit.
- ③ Based on the case study in this lecture, determine the output voltage when the load resistance become 100Ω , when the specified duty ratio is applied without any loss consideration. Verify the computation by simulation.