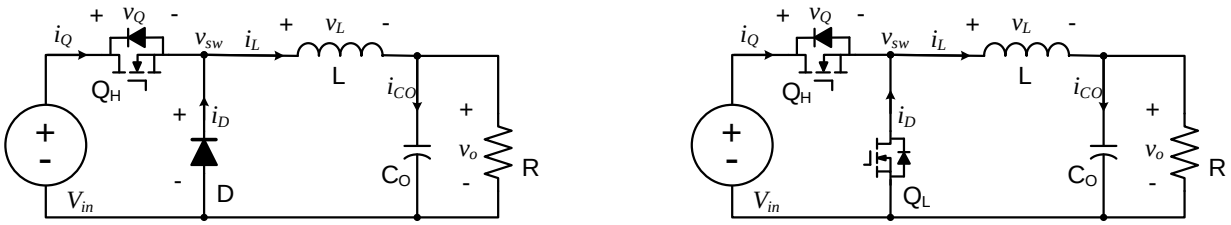
1 Scope

The purpose of the project is to analyze, simulate, prototype, and test a non-isolated DC/DC buck converter. The schematics are shown in Figure 1 including the standard version (a) and synchronous version (b). The operational principle of both is considered the same in CCM. The synchronous buck converter is widely used for low-voltage applications, such as computer, tablet, and cell, since the conduction loss caused by diode voltage drop can be minimized.



(a) Standard version (b) Synchronous version

Figure 1 Schematic of Buck Converters

2 Converter Specifications

The converter shall be designed to supply 5 V DC.

Input voltage	Switching frequency	Inductor	Output capacitor	Load resistor
V_{in} = 12V	f_{sw} = 100 kHz	L = 100 µH	Co = 3.3 µF	R = 10 Ω

3 Periodic Steady-state Analysis

When **42%** on-state duty cycle is applied to switch the MOSFET Q_H, the low-side MOSFET acts like the flywheel diode in the buck converter. The following question should be answered without considering any loss in the circuit

- Assume CCM, the average of the output voltage in steady state AVG(v_o) = ?
- Assume CCM, the peak-to-peak ripple value of the inductor current in steady state: ΔI_L = ?
- Assume CCM, the RMS value of the inductor current in steady state: RMS(i_L) = ?
- Assume CCM, the average value of the inductor current in steady state: AVG(i_L) = ?

- Is the converter operated at continuous conduction mode (CCM) in steady state?
- What is the critical value of the load resistance, R, between the CCM and the discontinuous conduction mode (DCM)?
- Peak-to-peak ripple value of the voltage across the load and output capacitor: ΔV_O = ?

4 Simulation

- Build the simulation model by your development. You are flexible to choose Simulink, PSIM, or LTSPICE as your simulation tool.
- Specify the parameters of sampling frequency and simulation time of the simulation model. The sampling frequency of the simulation should be at least 100 times of the switching frequency. The simulation time should cover the transient time and steady state with the best resolution.
- Simulate and demonstrate the following simulated waveforms:
  1) Voltage at the switching node: $\boldsymbol{v_{SW}}$, indicating the upper and lower voltage level;
  2) Voltage across MOSFET Q: $\boldsymbol{v_Q}$, indicating the upper and lower voltage level;
  3) Voltage across the inductor, $\boldsymbol{v_L}$, indicating the upper and lower voltage level;
  4) Inductor current, $\boldsymbol{i_L}$, indicating the average value, $AVG(I_L)$, and the peak-to-peak ripple value (ΔI_L);
  5) Current through the diode, D: $\boldsymbol{i_D}$, indicating the upper and lower current level;
  6) Current through MOSFET Q: $\boldsymbol{i_Q}$, indicating the upper and lower current level;
  7) Output capacitor current: $\boldsymbol{i_{co}}$, indicating the upper and lower current level;
  8) Output voltage, $\boldsymbol{v_o}$, indicating the average value, $V_O(AVG)$, the peak-to-peak ripple value (ΔV_O).

5 Report (5%)

- Following the requirement of Section 3, show the steady-state analysis.
- Following the requirement of Section 4, present your work in terms of simulation model, simulation parameters, and simulation waveforms.

- Make sure all fonts in figures in your report are proper in size and readable directly. Mark reduction is expected if font size is too small to read.
- Comment based on comparing your simulation waveforms to your steady state analysis in term of average value and ripple levels.
- Justify if the simulation matches your analysis. If not, tell the reason.
- Due date: follow Canvas submission site.

6 Warning

- Please don’t copy any plot from the lecture slides and modify for your homework!
- Please don’t copy others drawing and use as yours!
- All figures and tables shall show high quality and resolution!
- Serious offense will be reported to the school and discipline committee!