Signal Quality in Multi Stage Sample Rate Converters

Matthieu Guerquin-Kern, ENSEA

June 27, 2018

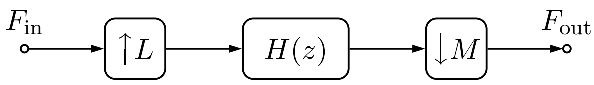
Abstract

The purpose of this document is to evaluate the impact that the multi-stage implementation of a sample rate converter might have on signal quality.

1 Context

1.1 Single Stage Sample Rate Converter

A synchronous sample rate converter (SRC) can be described by the cascade of an upsampler, a filter, and a downsampler.



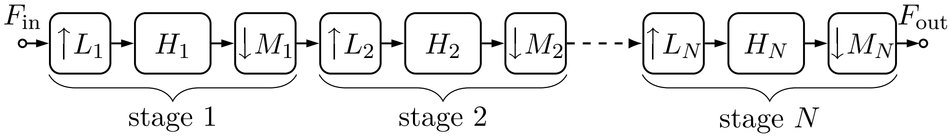
In the above block diagram, the SRC will change the signal from a rate F_{in} to a rate F_{out} under the constraint that $L \cdot F_{\text{in}} = M \cdot F_{\text{out}}$ with L and M integers. The linear shift invariant filter H plays two roles: interpolating and anti-aliasing (sensible only if $M > L$). Therefore, in order to ensure a minimal distortion on the signal, one wants the filter as close as possible to a low-pass with cutoff pulsation $\omega_c = \pi / \max(L, M)$ and $H(1) = M$.

1.2 Multi Stage Sample Rate Converter

Let us consider the following factorizations

$$L = \prod_{i=1}^{N} L_i \text{ and } M = \prod_{i=1}^{N} M_i,$$

where some L_i or M_i might equal 1 but with M_i ad L_j relatively prime $\forall i, j$. Then, we can consider decomposing the SRC into N multiple stages of the same form.



Since the L_i and M_j are relatively prime, the two structures are equivalent provided that

$$H(z) = \prod_{i=1}^{N} H_i\left(z^{\tilde{L}_i \cdot \tilde{M}_{N-i+1}}\right), \tag{1}$$

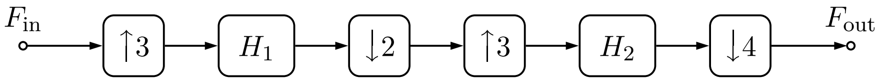
with the notations $\tilde{L}_i$ and $\tilde{M}_i$ stand for $\prod_{k=i+1}^{N} L_k$ and $\prod_{k=i+1}^{N} M_k$ if $i < N$, and $\tilde{L}_N = \tilde{M}_N = 1$.

For the design of the filters H_i, one can apply the constraints previously seen: low-pass with cutoff pulsation $\omega_c = \pi/\max(L_i, M_i)$ and $H_i(1) = M_i$. Then, the question is "how should organize the stages in order to have a minimal impact on signal quality?" In other words, "How to sort the sequences L_i and M_i in order to have H be the closest to a low-pass with cutoff pulsation $\omega_c = \pi/\max(L, M)$"? [1]

2 Simple Example

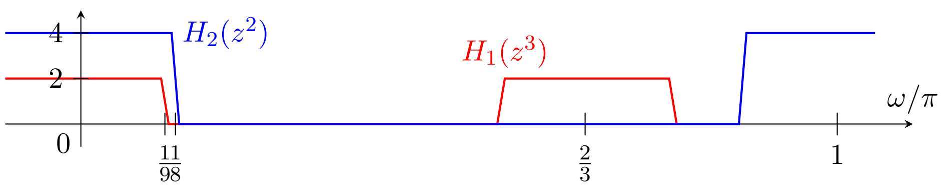
In this example, we consider the case where $L = 9$, $M = 8$ and $N = 2$. Since, $L_1 = L_2 = 3$, we result in two possible implementations of a dual stage SRC.

2.1 Case $M_1 = 2$ and $M_2 = 4$



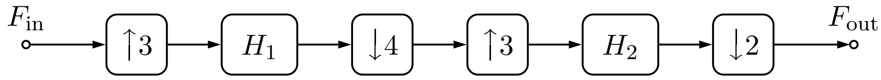
The cutoff frequencies of H_1 and H_2 are $\pi/3$ and $\pi/4$, respectively. We have $H(z) = H_1(z^3)H_2(z^2)$. As the following plot shows, there should be no problem :

- outside of low frequencies, the filters act on different frequency bands,
- the resulting cutoff pulsation is $\pi/9$ as expected.



[1] From (1), one sees that $H(1) = M$ is not a big deal.

2.2 Case $M_1 = 4$ and $M_2 = 2$



The cutoff frequencies of H_1 and H_2 are $\pi/4$ and $\pi/3$, respectively. We have $H(z) = H_1(z^3)H_2(z^4)$. As the following plot shows, the situation is now more complicated because

- the filters share common frequency intervals in high frequencies.
- the resulting cutoff pulsation $\pi/12$ is lower than expected.