On Digital Single-Sideband Modulators

SIDNEY DARLINGTON, FELLOW, IEEE

Abstract—This paper concerns digital single-sideband modulators with analog inputs and outputs. A group of 12 modulators is treated as a single system, with analog-to-digital converters at 12 input ports and a digital-to-analog converter at a single output port. Tradeoffs are obtained between computational parameters.

Substitution of digital counterparts for the phase shifters and product modulators in 12 analog Hartley modulators gives a simple program. However, operation in real time requires quite a large number of multiplications per second. A similar digitalization of 12 Weaver modulators requires even more multiplications. However, the 12 Weaver modulators can be transformed *as a system*, to reduce the multiplication rate for the Hartley system by a factor > 4. The cost is an increase in scratch pad storage and a more complex program.

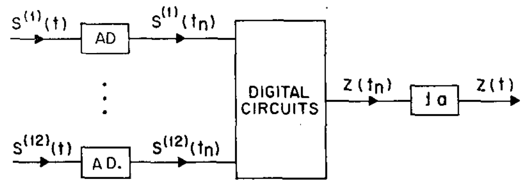

Fig. 1. Representation of 12 modulators as a system.

I. Introduction

When input and output signals are band limited, analog circuits can be replaced by digital signal processors, preceded and followed by analog-to-digital (A–D) and digital-to-analog (D–A) converters. The possibility of obtaining substantially the same external characteristics with such digital counterparts of analog circuits has been recognized for a long time. With the coming of large-scale integrated circuitry, it appears that the digital counterparts may soon compete economically in applications where analog circuitry used to be taken for granted.

This paper concerns the digitalization of single-sideband modulators for analog input and output signals. More specifically, it considers a group of 12 single-sideband modulators as a single system, as illustrated in Fig. 1. A–D converters, at 12 input ports convert analog voice-band signals $s^{(i)}(t)$ into sequences of numbers $s^{(i)}(t_n)$, digital circuitry converts the 12 inputs into a single output sequence $z(t_n)$, and a D–A converter, converts the output sequence into the sum $z(t)$ of 12 single-sideband translations of the analog inputs (with suitably spaced carrier frequencies). Twelve-channel analog subsystems are a usual part of even large carrier systems, in which later modulations combine groups of 12-channel groups to form super groups, etc.

The work described here was motivated by digital single-sideband modulators proposed previously, notably by McDonald and Jackson. The purpose of this paper is to illustrate how a system point of view can yield tradeoffs between important computational parameters.

Analog single-sideband modulation is usually accomplished by a combination of time-invariant linear circuits and product modulators. Several different such combinations are known, notably conventional modulators using bandpass filters, Hartley modulators using phase shifts, and Weaver modulators using low-pass filters [1], [2]. Digital counterparts of each of these can be obtained by simply substituting digital counterparts of each of the subsystems (circuits and product modulators). Under certain assumptions; the Hartley modulator gives the simplest direct digital counterpart, but the required multiplication rate is quite high, perhaps 13 000 000 multiplications per second. The direct digital counterpart of the Weaver modulator requires an even higher multiplication rate. However, the computations required in a group of 12 digital Weaver modulators can be transformed in a way that drastically reduces the multiplication rate (to perhaps a quarter or a fifth of the rate for the Hartley modulator).

The primary purpose of this paper is to point out the potential saving in multiplication rate and how it can be accomplished. For practical applications, of course, one must also consider changes in other computational parameters. In terms of bits per second, the computation rate depends also on the number of bits to which the multiplications must be carried, and the number of bits depends on sensitivities to roundoff errors. According to qualitative arguments, which will be noted at the end of the paper, the transformed Weaver modulator is almost surely no more sensitive to roundoff than the Hartley modulator, and probably less so. A quantitative determination of roundoff errors is a large task, requires many more assumptions regarding programming details, and is not likely to be undertaken for this specific system without prior knowledge of the saving in multiplication rate. The principal cost of the saving in multiplication rate is an increase in scratch pad storage (which will be estimated) and a more complex program.

II. Carrier Frequencies and Sample Intervals

We will assume that the voice-band signals are band limited and also have a low-frequency cutoff > 0 (as required for all single-sideband systems). Let f_0 be a frequency (in hertz) a little higher than the highest voice-band frequency, such that: first, spacing carrier frequencies at intervals f_0 leaves practical guardbands

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The author is with Bell Telephone Laboratories, Inc., Murray Hill, N. J.

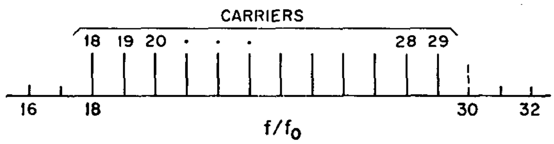

Fig. 2. Carrier frequency assignments.

between single sidebands; second, $2f_0$ samples per second is a practical sampling frequency for individual voice-band signals. We shall call the corresponding sample interval T the baseband Nyquist interval:

$$T = \frac{1}{2f_0} = \text{baseband Nyquist interval.} \quad (1)$$

We shall find it convenient to choose the 12 carrier frequencies indicated in Fig. 2, that is

$$18f_0, 19f_0, \cdots, 29f_0. \quad (2)$$

Then, assuming upper sidebands, the highest frequency of the highest sideband is a little below $30f_0$. Note that $18f_0$ is two channel widths above $16f_0$ and $30f_0$ is two below $32f_0$. We will use f_c to represent any carrier frequency, and also $\omega_c = 2\pi f_c$ and $\omega_0 = 2\pi f_0$.

For definiteness we will assume

$$f_0 = 4000 \text{ Hz}, \quad (3)$$

and that the filters in single-sideband modulators must meet requirements appropriate for high-quality large carrier systems.

Since the bandwidth of the group of 12 single sidebands is approximately $12f_0$, the digital circuitry of Fig. 1 must produce more than $2f_0$ samples per second. In principle, $12 \times 2f_0$ is sufficient, but this requires sharp cutoff analog filters associated with the D–A conversion (to eliminate extraneous frequencies due to foldover). For our purposes we shall find it convenient to assume $16 \times 2f_0$ output samples per second. Then, in contrast to (1),

$$\frac{T}{16} = \text{output sample interval.} \quad (4)$$

With carrier frequencies (2) and sample interval (4), true signal frequencies and extraneous frequencies are separated by guardbands of approximately four channel widths.

III. Difference Equations

We are going to examine digital counterparts of analog modulators that include filters or phase shifters defined by differential equations. Digital counterparts (operating on discrete signal samples) are described by difference equations. We shall have occasion to use all three of the following well-known forms of difference equations, in which x_η is the input sample at sample time η and y_n is the output sample at sample time n:

$$\sum_{\sigma=0}^{\rho} a_\sigma y_{n-\sigma} = x_n \quad (5a)$$

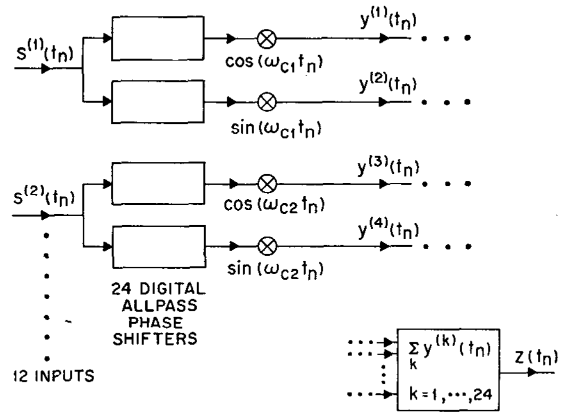

Fig. 3. A system using digital Hartley modulators.

$$y_n = \sum_{\eta=n-N}^{n} W_{n-\eta} x_\eta \quad (5b)$$

$$\sum_{\sigma=0}^{\rho_1} a_\sigma y_{n-\sigma} = \sum_{\sigma=0}^{\rho_2} b_\sigma x_{n-\sigma}. \quad (5c)$$

These may be described, respectively, as recursive, nonrecursive or convolutionary, and general. It is well known that the general form is most efficient (in terms of orders ρ, N, ρ_1, ρ_2) for mechanization of individual sharp cutoff filters and phase shifters, but we shall find the other forms useful for our 12-channel systems.

IV. Hartley Modulators

Fig. 3 illustrates a group of 12 digital Hartley modulators. There are 24 transmission paths through the system (2 per channel). In each path, the signal is operated on by a difference equation and then by a product modulation. The output sample rate is $16 \times 2f_0$ samples per second. For this, the difference equations and modulation factors are formulated for, and computed at $16 \times 2f_0$ computation cycles per second. The (digital) all-pass circuits can not eliminate foldover frequencies due to lower input sample rate. Hence, the input sample rate must be $16 \times 2f_0$ samples per second (for each of the 12 inputs), even though the original analog input can be reconstructed from $2f_0$ samples per second.

The economy of the circuit of Fig. 3 depends critically on an assumption that $16 \times 2f_0$ samples per second can be supplied to each input almost as easily as $2f_0$ samples per second. This may well be true of practical applications, because the preferred D–A converters are likely to start with delta modulation, entailing many increments per baseband Nyquist interval.

Simple computations [3] indicate the following. If each of the phase shifters in a Hartley modulator is described by a frequency function with four poles, a 60-dB suppression of the unwanted sideband can be achieved with a ratio of maximum-to-minimum voice-band frequencies of about 15. Corresponding difference equations have the general form (5c), with $\rho_1 = \rho_2 = 4$, the coefficients on the right the same as those on the left written in reverse order, and one coefficient equal

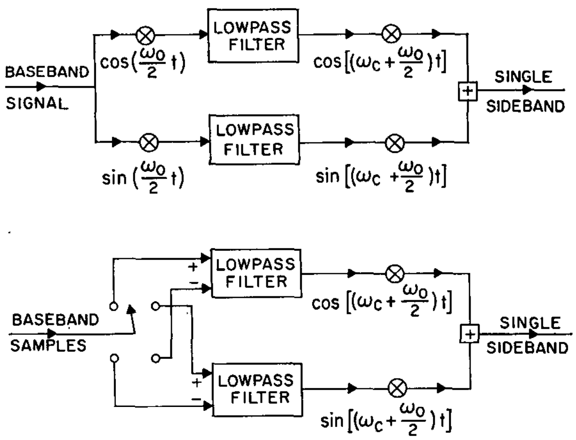

Fig. 4. Analog Weaver modulators.

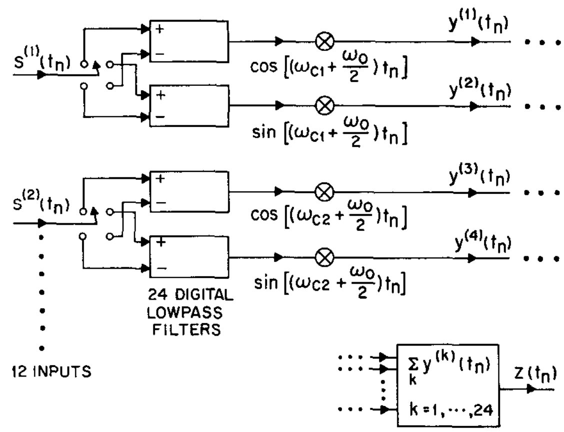

Fig. 5. A system using digital Weaver modulators.

to unity.[1] If input and output samples multiplied by identical constants are first combined (by subtraction), only four multiplications are needed per computation cycle per phase shifter. But this is 24×4 multiplications per computation cycle for the 24 phase shifters, or $16 \times 24 \times 4$ multiplications per baseband Nyquist interval. This comes to $1536 \times 8000 > 12 \times 10^6$ multiplication per second for the phase shifters. Adding the multiplications required for the product modulations raises the figure to $> 13 \times 10^6$ multiplications per second for the system of Fig. 3.

Storing the previous input and output samples that appear in the 24 difference equations uses 8×24 or 192 words of scratch pad memory.

V. Weaver Modulators

Fig. 4(a) illustrates the original Weaver modulator [1]. Fig. 4(b) illustrates a modification using a sampled input [2]. A minus sign at a filter input indicates that a sample is to be reversed in sign before it enters the filter. Fig. 5 illustrates a corresponding direct digitalization of our 12-channel group. The two filters in each modulator, and hence the 24 in the 12-channel group are all identical.

There are again 24 transmission paths through the system, and in each path the signal is operated by a difference equation and then by a product modulation. The same difference equation is used in each path, but with a different modulation factor. The output sample rate is again $16 \times 2f_0$, and the difference equations and modulation factors are again formulated for, and computed at $16 \times 2f_0$ computation cycles per second. Now, however, because the difference equations apply filtering, baseband samples are needed only at the Nyquist rate. (One effect of the filtering is interpolation between baseband samples.)

Fig. 23 in [4] indicates that, for comparable quality, the low-pass filters in the Weaver modulator need some eight poles each, as opposed to the four poles of the Hartley phase shifters. (The reason more poles are needed has not been definitely established. A probable reason is the fact that Weaver modulators discriminate against frequencies on both sides of the used sideband, not just on the side toward the carrier.) Corresponding difference equations have the general form (5c), with $\rho_1 = 8$, $\rho_2 \leq 8$. The fact that each filter receives only f_0 input samples per second (every other sample of a voice-band signal) can be taken into account by using $x_\eta = 0$ except at every 32nd sample time η of the $16 \times 2f_0$ samples per second sequence.

Because of the eight poles per filter, compared with four poles per phase shifter, the Weaver modulator as illustrated in Fig. 5 requires about twice as many multiplications per second as the Hartley modulator of Fig. 3. However, it can be modified and transformed to obtain an even lower multiplication rate.

As a first step in reducing the multiplication rate, we separate each digital filter into two filters in cascade, as illustrated in Fig. 6. The difference equation for the first is designed for only $2f_0$ computation cycles per second and supplies only $2f_0$ samples per second to the second filter. The difference equation for the second filter is designed for $16 \times 2f_0$ computation cycles per second and produces the required filter output at $16 \times 2f_0$ samples per second. The first filter produces the sharp cutoff needed for a Weaver modulator. It is characterized by eight poles, but the multiplications per second are relatively few because of the fewer computation cycles per second. The second filter eliminates extraneous frequencies due to the low sample rate of the first. It can be relatively simple (characterized by fewer poles) because its frequency function can cut off quite slowly. Fig. 7 indicates frequency intervals occupied by the true signal frequencies and the nearest extraneous frequencies. (Recall that the first product modulators in the Weaver modulator of Fig. 4(a) reduce the voice-band frequencies by $f_0/2$ so that they lie in the interval $-f_0/2$ to $+f_0/2$.) The two filters need not have flat passbands, individually, provided their variations in loss over the passbands are complementary.

The simple expedient described above reduces the

[1] The relation between coefficients can be derived by applying the well-known z transform $s = (1 - z)/(1 + z)$ to a rational all-pass frequency function.

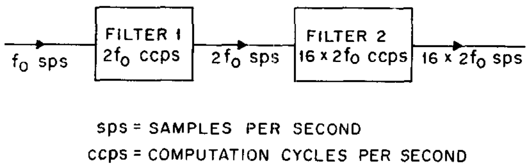

Fig. 6. Slow and fast filters in cascade.

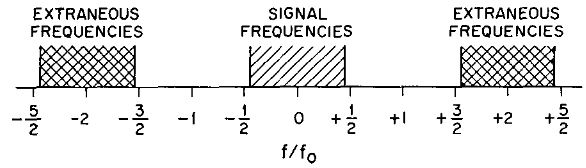

Fig. 7. Frequencies at the inputs of the fast filters.

multiplication rate, but not to where the Weaver modulator becomes competitive with the Hartley modulator (under the conditions assumed in Section IV). To obtain further reductions in the multiplication rate, we now assume that the first "slow" filter in Fig. 6 is purely recursive and the second "fast" filter is nonrecursive (slow and fast refer to the computation cycles per second). Section VI describes how the 24 nonrecursive filters in a corresponding 12-channel modulator system can be manipulated to obtain a drastic reduction in the overall multiplication rate. Then Section VII shows how a recursive slow and nonrecursive fast pair of filters can be derived from a general difference equation appropriate to the direct digitalization of a Weaver modulator as in Fig. 5.

VI. Transfer of the Nonrecursive Filters to the System Output

In this section we are concerned with the part of the 12-channel system indicated in Fig. 8—the 24 nonrecursive filters, the subsequent product modulators, and the summation that yields the digital system output. Let superscripts (k), $k = 1, \cdots, 24$, designate the individual transmission paths through the system and recall that the output sample interval is $T/16$, where T is the baseband Nyquist interval. Let

$$\begin{aligned} x_\eta^{(k)} &= \text{input to filter } (k) \text{ at sample time } \eta(T/16) \\ y_n^{(k)} &= \text{output of filter } (k) \text{ at sample time } n(T/16) \\ M_n^{(k)} &= \text{product modulation factor applied to } y_n^{(k)} \\ z_n &= \text{digital system output at sample time } n(T/16). \end{aligned} \tag{6}$$

To account for the lower sample rate at the inputs requires

$$x_\eta = 0 \qquad \text{except when } \eta = 16\,\mu \tag{7}$$

where μ is an integer.

The nonrecursive filters relate $y_n^{(k)}$ to $x_\eta^{(k)}$ by a difference equation of the form

$$y_n^{(k)} = \sum_{\eta=n-N}^{n} W_{n-\eta} x_\eta^{(k)} \qquad x_\eta^{(k)} = 0, \quad \eta \neq 16\,\mu. \tag{8}$$

Then the digital system output z_n is

$$z_n = \sum_{k=1}^{24} M_n^{(k)} y_n^{(k)} = \sum_{k=1}^{24} M_n^{(k)} \sum_{\eta=n-N}^{n} W_{n-\eta} x_\eta^{(k)}. \tag{9}$$

Note that $W_{n-\eta}$ does not depend on index (k). This suggests reversing the order of the summation, which gives

$$\begin{aligned} z_n &= \sum_{\eta=n-N}^{N} W_{n-\eta} B_{n,\eta} \\ B_{n,\eta} &= \sum_{k=1}^{24} M_n^{(k)} x_\eta^{(k)}. \end{aligned} \tag{10}$$

If (10) is mechanized instead of (9) the summation with weight factor $W_{n-\eta}$ need be computed only once per computation cycle, instead of separately for each of 24 filters. With general input samples $x_\eta^{(k)}$ and general coefficients $M_n^{(k)}$, this economy is more than offset by extra computations required for $B_{n,\eta}$. However, in our special case (10) offers a very substantial reduction in the multiplications per second.

First, because of (7),

$$B_{n,\eta} = 0 \qquad \text{except when } \eta = 16\,\mu. \tag{11}$$

Second, with the carrier frequencies (2) and sample intervals (1), (4),

$$|B_{n,\eta}| \text{ is periodic in } n \text{ with period } 32 \tag{12}$$

(and changes in sign with n can be taken care of by adjusting the sign of $W_{n-\eta}$). Thus, it is sufficient to compute and store 32 $B_{n,\eta}$ once each baseband sample interval (once every 16 output sample intervals). Third, when the phases of the carriers are suitably related to the sampling instants, the factors $N_n^{(k)}$ belong to the set

$$\left.\begin{matrix} \cos\left[\pm\left(q\,\dfrac{n\pi}{8} \pm \dfrac{n\pi}{32}\right) + n\,\dfrac{3\pi}{2}\right] \\ \sin\left[\pm\left(q\,\dfrac{n\pi}{8} \pm \dfrac{n\pi}{32}\right) + n\,\dfrac{3\pi}{2}\right] \end{matrix}\right. \qquad q = 1, 2, 3. \tag{13}$$

(Recall that the product modulators apply frequencies $f_c + f_0/2$, where f_c is a carrier frequency, as in Fig. 4.) As a result, procedures at least reminiscent of fast Fourier transforms can be used to compute the 32 $B_{n,\eta}$ using only 76 multiplications.

Fig. 9 is a block diagram of a corresponding 12-channel modulator system.

VII. Design of Slow and Fast Filter Pairs

This section describes how digital filters with difference equations of the form (5c), appropriate for the system of Fig. 5, can be decomposed into exactly equivalent pairs of recursive slow and nonrecursive fast filters, appropriate for the purposes described in the previous two sections, leading to a reduction in multiplication rate as in (10) and Fig. 9.

Let the original filter be described by

$$\sum_{\sigma=0}^{p} a_\sigma y_{n-\sigma} = \sum_{\sigma=0}^{p} b_\sigma s_{n-\sigma} \qquad s_\eta = 0, \quad \eta \neq 16\,\mu. \tag{14}$$

The frequency function corresponding to the difference equation can be written in the following factored form (using $p = i\omega$):

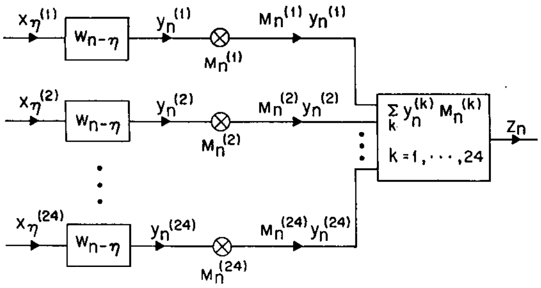

Fig. 8. The fast filters and subsequent operations.

$$Y(p) = K \prod_{\sigma=1}^{\rho} \left(\frac{1 - \lambda_\sigma e^{-(T/16)p}}{1 - \gamma_\sigma e^{-(T/16)p}} \right). \tag{15}$$

Multiplying numerator and denominator of the typical factor by common factors gives

$$\frac{1 - \lambda_\sigma e^{-(T/16)p}}{1 - \gamma_\sigma e^{-(T/16)p}} = \frac{(1 - \lambda_\sigma e^{-(T/16)p})(1 - \gamma_\sigma^{16} e^{-Tp})}{(1 - \gamma_\sigma^{16} e^{-Tp})(1 - \gamma_\sigma e^{-(T/16)p})}. \tag{16}$$

But the second denominator factor can be divided into the second numerator factor, after which

$$\frac{1 - \lambda_\sigma e^{-(T/16)p}}{1 - \gamma_\sigma e^{-(T/16)p}} = \frac{A_\sigma(e^{-(T/16)p})}{1 - \gamma_\sigma^{16} e^{-Tp}} \tag{17}$$

in which $A_\sigma(\cdot)$ is a polynomial of degree 16.

Transforming all factors of (15) in the same way transforms (15) into

$$Y(p) = \frac{A(e^{-(T/16)p})}{B(e^{-Tp})} \tag{18}$$

in which $B(\cdot)$ is a polynomial of degree ρ but $A(\cdot)$ is a polynomial of degree 16ρ. This can be mechanized as a recursive digital circuit defined by the denominator followed by a nonrecursive digital circuit defined by the numerator. In terms of corresponding difference equations:

$$\sum_{\sigma=0}^{\rho} \hat{a}_\sigma x_{n-16\sigma} = s_n \qquad s_n = 0, \quad x_n = 0, \quad n \neq 16\,\mu \tag{19a}$$

$$y_n = \sum_{\eta=n-16\rho}^{n} W_{n-\eta} x_\eta \qquad x_\eta = 0, \quad \eta \neq 16\,\mu. \tag{19b}$$

The large number of terms in (19b) is offset by the condition on x_η, which makes all terms zero except every 16th (but the coefficients of nonzero terms vary cyclically with n). Actually, (19a) and (19b) require the same number of multiplications per second as does (14).

If the difference equation (14) defines a filter appropriate to the Weaver modulators of Fig. 5, (19) defines recursive slow and nonrecursive fast digital circuits appropriate for the purposes described in the last two sections, leading to a reduction in multiplication rate as in (10) and Fig. 9.

Suppose the overall filter function has eight poles, as before, and assume that y_n in (19a) is so scaled that one of the coefficients is unity. Then the 24 recursive slow filters require 24×8 multiplications per baseband Nyquist interval. The single convolution in the system

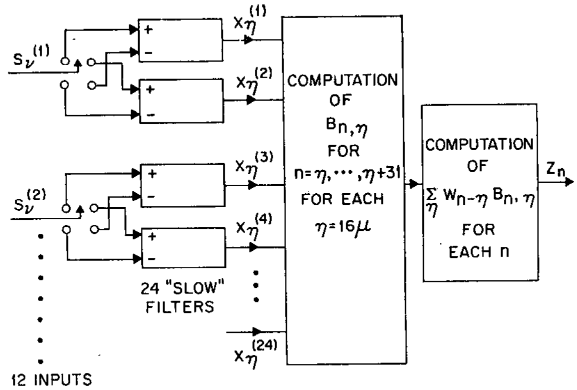

Fig. 9. The transformed system.

output in (19b) and Fig. 8 requires 9 multiplications per output sample interval, or 16×9 per baseband Nyquist interval. Finally, computation of the quantities $B_{n,\eta}$ in (10) requires no more than 76 multiplications per baseband Nyquist interval. The sum of these multiplication rates is $412 \times 8000 < 3\,300\,000$ multiplications per second. Relatively minor rearrangements of the computations, which need not concern us here, can be used to reduce the multiplications by another 10 percent or more [for example, by exchanging scale factors between $W_{n-\eta}$ and $B_{n,\eta}$ in (10)].

Numbers that must be stored for at least one computation cycle now use a scratch pad memory of approximately 450 words. Other numbers may have to be stored more briefly, for example in the computation of $B_{n,\eta}$, but will depend strongly on details of the computation program.

VIII. Roundoff Sensitivities

Suppose the recursive difference equation (5a) represents a filter with a flat passband and sharp cutoff at 2000 Hz. Because of the flat passband and sharp cutoff it will accumulate roundoff errors during an impulse response time that lasts for many of our sample intervals T. In other words, even at 8000 computation cycles per second, the net roundoff error at any one time will be a weighted sum of errors committed during many computation cycles. At 16×8000 computational cycles per second, 16 times as many roundoff errors will be accumulated.

The same remarks apply, at least qualitatively, to the recursive part of the general difference equation considered in Section VII. Thus, replacing the recursive part of (14) at 16×8000 computational cycles per second by a recursive equation at 8000 computational cycles per second reduces the effects of corresponding roundoff errors. This is further supported by the denominators in (17) in which $|\gamma_\sigma| < 1$, and then $|\gamma_\sigma|^{16} < |\gamma_\sigma|$ (which reduces by 16 to 1 the effective memory time in terms of computation cycles).

A purely nonrecursive representation of a filter with a flat passband and sharp cutoff requires many terms and may be as sensitive to roundoff as a recursive counterpart, but this does not apply to the nonrecursive part of (14). It produces the transmission zeros needed for high loss in the attenuation band. By itself, it produces neither a flat passband nor a sharp cutoff. This kind of equation is generally less sensitive to roundoff. With $\rho < 16$, the right-hand side of (14) contains only one *nonzero* term in each computing cycle. In (19b), there are only ρ, or about 8 nonzero terms. The ρ signal samples are separated by baseband Nyquist intervals T; thus (19a) will not exaggerate roundoff by small differences between true terms under usual signal statistics.

IX. Concluding Remarks

The previous sections have shown how a group of 12 digital single-sideband modulators, treated as a single system, can be transformed in a way that drastically reduces the required multiplications per second. The cost is an increase in scratch pad storage and a much more complicated program.

Whether the transformed system will compete economically with, for example, the digital Hartley modulators of Fig. 3, will depend on many factors not discussed here. These include relative costs of multiplications per second and scratch pad memory, the possibility of common program control for many groups of 12-channel modulators, and the word lengths required by various schemes for roundoff control.

References

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[4] S. Darlington, "Synthesis of reactance 4-poles," *J. Math. and Phys.*, vol. 18, pp. 257–353, September 1939. (See Fig. 23, p. 331, and note that n in the figure is related to number of poles ρ by $\rho = 2n + 1$.)

Correspondence

One-Pole Admittance Functions

Abstract—**Necessary and sufficient conditions are obtained that a set of admittance functions having a single finite pole be realizable as an RC three-terminal network. The necessary conditions are more restrictive than the familiar residue and coefficient conditions.**

Preliminaries

We outline the theory required below, basing ourselves on [4], [5], but using a slightly different notation. Let Γ be a general RC three-terminal network having $t + 1$ nodes, whose external nodes are numbered 1, 2, 3. The nodes are identified so that each branch consists of resistor and capacitor in parallel. Hence the admittance y_{ij} $(i \neq j)$ of the branch between nodes i and j is of the form $a + bs$ where $a \geq 0$, $b \geq 0$. Write

$$y_{ii} = \sum_{\substack{j=1 \\ j \neq i}}^{t+1} y_{ij} \qquad (ii) = y_{ii}; \quad (ij) = -y_{ij} (i \neq j).$$

The network determinant $\mathfrak{D}$ is the $(t + 1) \times (t + 1)$ determinant whose element in row i, column j, is (ij). Let $\mathfrak{D}_{ij}$ be the cofactor of (ij) in $\mathfrak{D}$, $\mathfrak{D}_{ijkl}$ be the cofactor of (kl) in $\mathfrak{D}_{ij}$, etc. It is known that all the $\mathfrak{D}_{ij}$ are equal. We write their common value as Δ.

The external behavior of Γ is usually characterized by the impedance functions

$$Z_{22} = \mathfrak{D}_{1122}/\Delta \qquad Z_{33} = \mathfrak{D}_{1133}/\Delta \qquad Z_{23} = \mathfrak{D}_{1123}/\Delta$$

or alternatively, by the admittance functions

$$Y_{22} = \mathfrak{D}_{1133}/\mathfrak{D}_{112233} \qquad Y_{33} = \mathfrak{D}_{1122}/\mathfrak{D}_{112233}$$
$$-Y_{23} = \mathfrak{D}_{1123}/\mathfrak{D}_{112233}. \qquad (1)$$

We shall find it convenient to use a symmetric formulation by means of the triplet of transfer impedances

$$\begin{aligned} Z_1 &= Z_{23} = \mathfrak{D}_{1123}/\Delta \\ Z_2 &= Z_{31} = \mathfrak{D}_{2231}/\Delta \\ Z_3 &= Z_{12} = \mathfrak{D}_{3312}/\Delta \end{aligned} \qquad (2)$$

and the triplet of transfer admittances

$$\begin{aligned} Y_1 &= -Y_{23} = \mathfrak{D}_{1123}/\mathfrak{D}_{112233} \\ Y_2 &= -Y_{31} = \mathfrak{D}_{2231}/\mathfrak{D}_{112233} \\ Y_3 &= -Y_{31} = \mathfrak{D}_{3312}/\mathfrak{D}_{112233}. \end{aligned} \qquad (3)$$

Since the cofactors satisfy the equation

$$\mathfrak{D}_{1123}\,\mathfrak{D}_{2231} + \mathfrak{D}_{2231}\,\mathfrak{D}_{3312} + \mathfrak{D}_{3312}\,\mathfrak{D}_{1123} = \Delta\,\mathfrak{D}_{112233}$$

the transfer impedances and admittances are related by the equations

$$\begin{aligned} Z_1 &= Y_1/Y \qquad Z_2 = Y_2/Y \qquad Z_3 = Y_3/Y \\ Y_1 &= Z_1/Z \qquad Y_2 = Z_2/Z \qquad Y_3 = Z_3/Z \end{aligned} \qquad (4)$$

where

$$Y = Y_1 Y_2 + Y_2 Y_3 + Y_3 Y_1$$
$$Z = Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1.$$

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