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EECE.2650 Logic Design

Assignment 5

## Design of Arithmetic Logic Unit

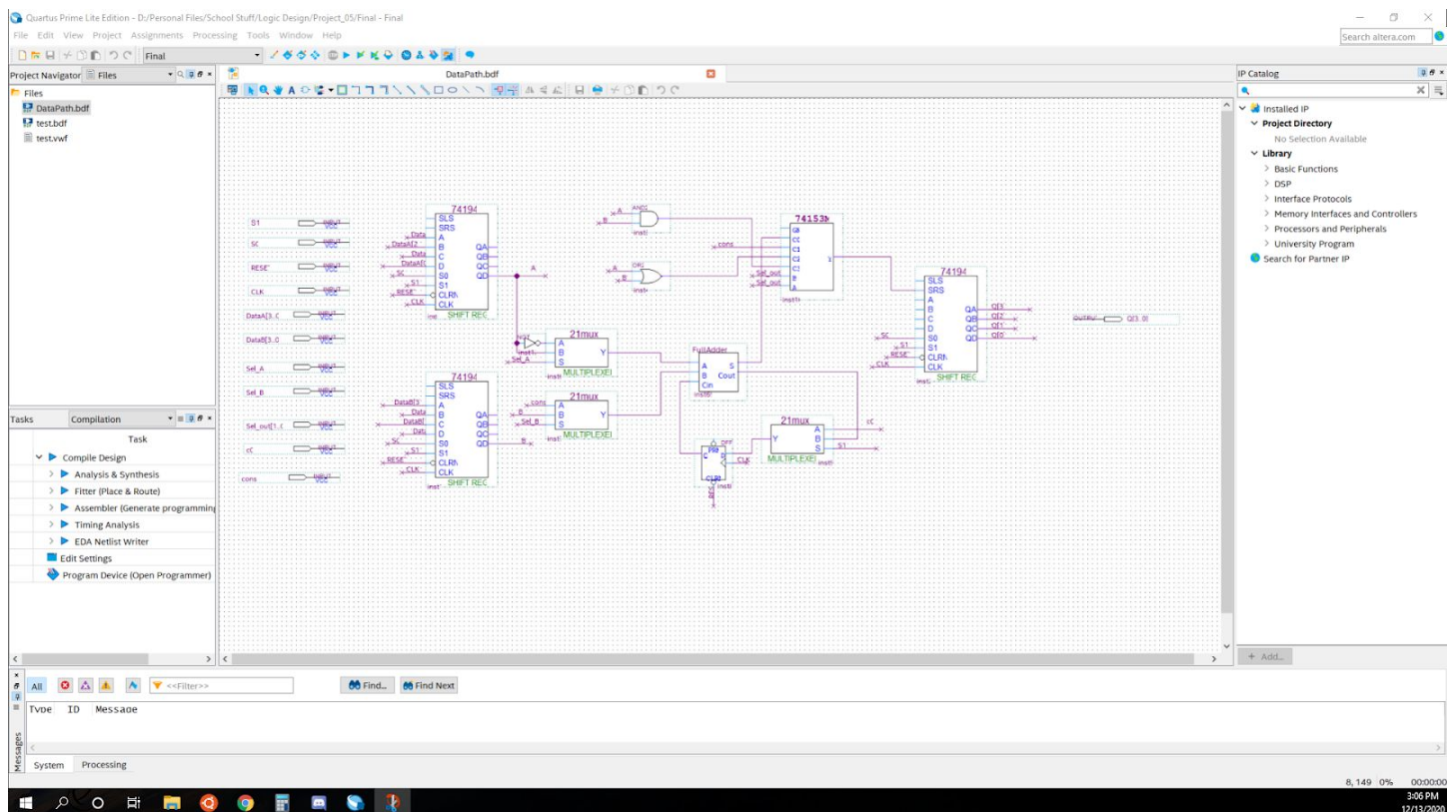
### Datapath Module

**Data Path Table:** Use this table to determine which signals go where for each instruction. You can then use this table to wire your datapath so that the muxes route the correct signals

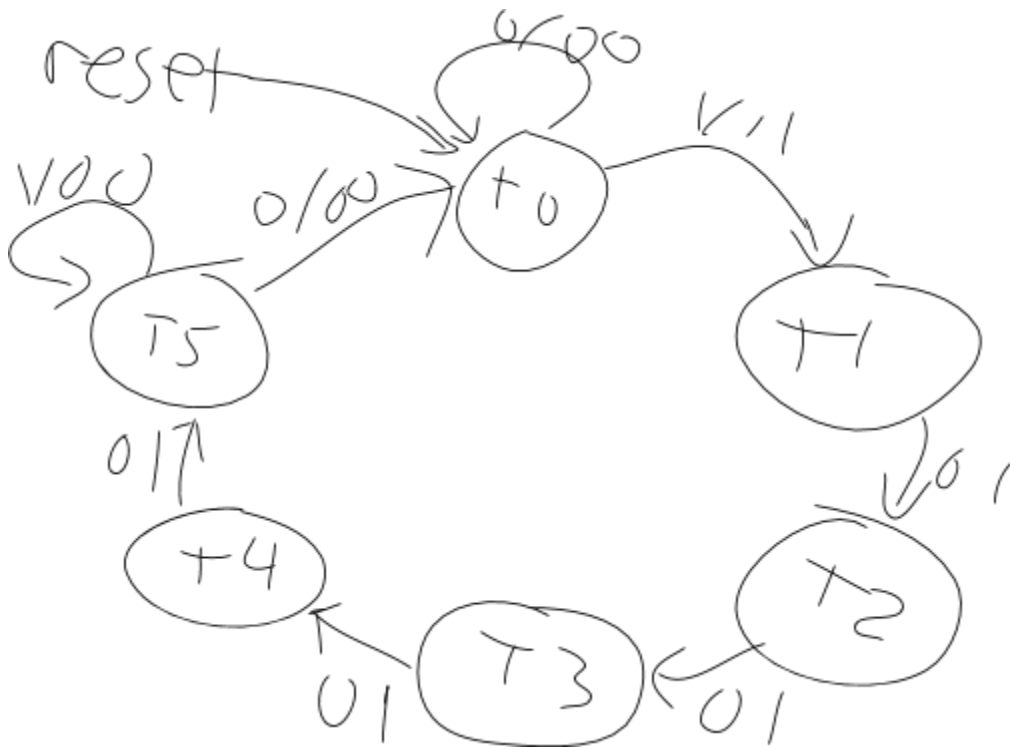
The first instruction is filled out for you.  $A + B$  uses the full adder for addition ( $c0 = 0$ ) the inputs to the full adder  $xi$  and  $yi$  get  $Ai$  and  $Bi$  respectively.

OpCode	Instruction	xi	yi	c0	Output Selector
0 0 0	Add A + B	Ai	Bi	0	Full Adder
0 0 1	Increment A	Ai	0	1	Full Adder
0 1 0	Invert A	$\sim Ai$	0	0	Full Adder
0 1 1	Subtract B - A	$\sim Ai$	Bi	1	Full Adder
1 0 0	Decrement A	Ai	1	0	Full Adder
1 0 1	$A \mid B$	Ai	Bi	D	OR Gate
1 1 0	$A \& B$	Ai	Bi	D	AND Gate
1 1 1	Negative A	$\sim Ai$	0	1	Full Adder

### Completed Datapath:



**State Diagram for the State Generator:**



**Transition Table for the State Generator:**

Present State	START	Next State	s1 s0
T0	0	T0	00
T0	1	T1	11
T1	d	T2	01
T2	d	T3	01
T3	d	T4	01
T4	d	T5	01
T5	0	T0	00
T5	1	T5	00

Using the table above, find the Next State Equations for T0-T5 and equations for s1 and s0:

$$T0+ = (T0 * !start) + (T5 * !start)$$

$$S1 = T0 * start$$

$$T1+ = (T0 * start)$$

$$S0 = !T5 * !(T0 * !start)$$

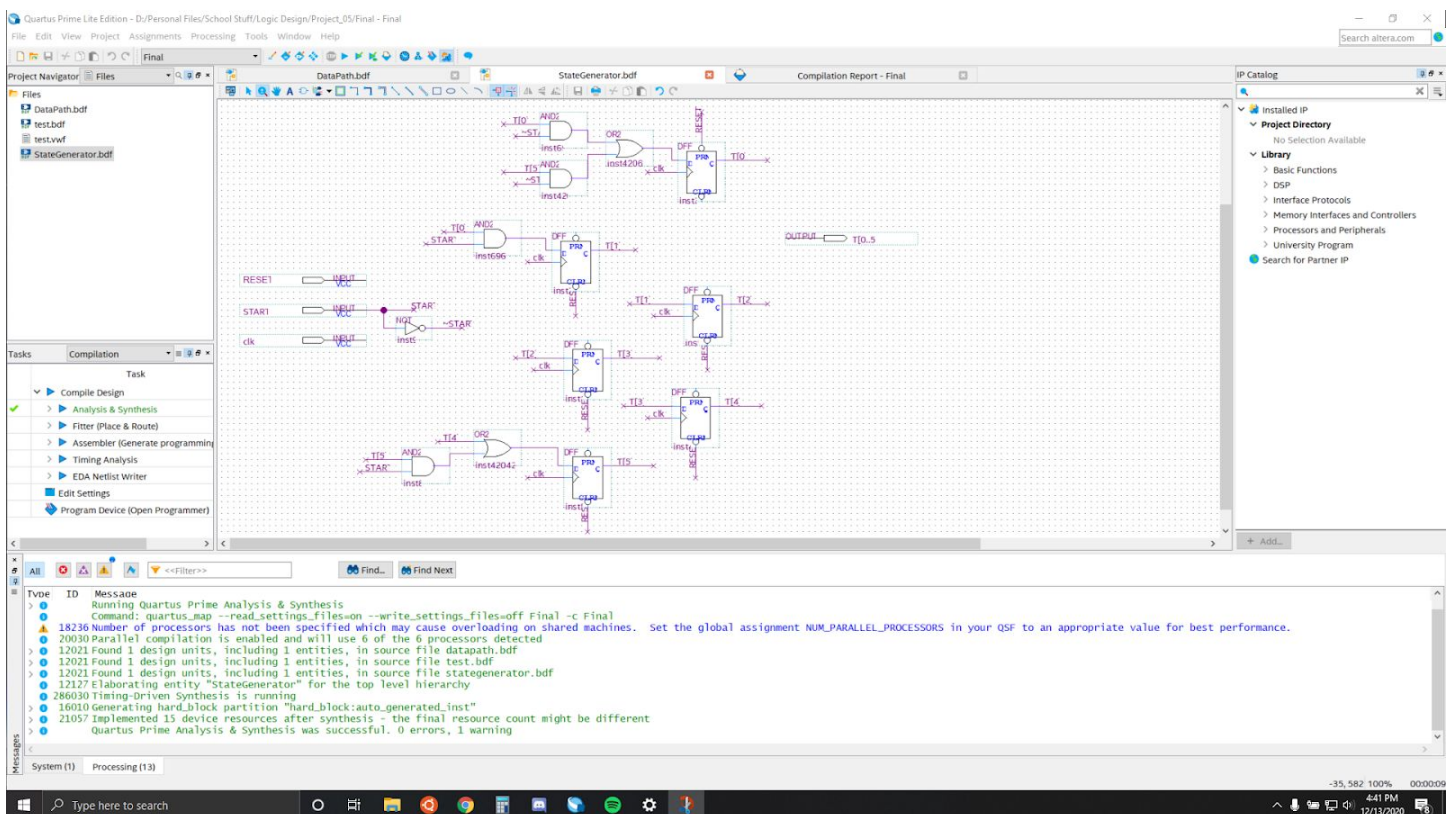
$$T2+ = T1$$

$$T3+ = T2$$

$$T4+ = T3$$

$$T5+ = T4 + (T5 * start)$$

Block Diagram for state generator:



# Control Circuit Truth Table:

OpCode	Instruction	Sel_A	Sel_B	Sel_out[1..0]	c0	Const
0 0 0	Add A + B	0	0	00	0	d
0 0 1	Increment A	0	1	00	1	0
0 1 0	Invert A	1	1	00	0	0
0 1 1	Subtract B - A	1	0	00	1	d
1 0 0	Decrement A	0	1	00	0	1
1 0 1	A   B	d	d	10	D	d
1 1 0	A & B	d	d	11	D	d
1 1 1	Negative A	1	1	00	1	0

Equations for each control signal: (You may choose to use a KMAP for each signal)

OP1 = A, OP2 = B, OP3 = C

Sel\_A

OP1/ OP2,3	00	01	11	10
0	0	0	1	1
1	0	1	1	0

Sel\_B

OP1/ OP2,3	00	01	11	10
0	0	1	0	1
1	1	1	1	0

c0

OP1/ OP2,3	00	01	11	10
0	0	1	1	0
1	0	1	1	1

Sel\_A = B

Sel\_B =  $A \oplus B \oplus C$

c0 = C

const

OP1/ OP2,3	00	01	11	10
0	d	0	d	0
1	1	d	0	d

Sel\_out[0]

OP1/ OP2,3	00	01	11	10
0	0	0	0	0
1	0	0	0	1

Sel\_out[1]

OP1/ OP2,3	00	01	11	10
0	0	0	0	0
1	0	1	0	1

const =  $A!B$

Sel\_out[0] =  $AB!C$

Sel\_out[1] =  $A!BC + AB!C$

$A(B \oplus C)$

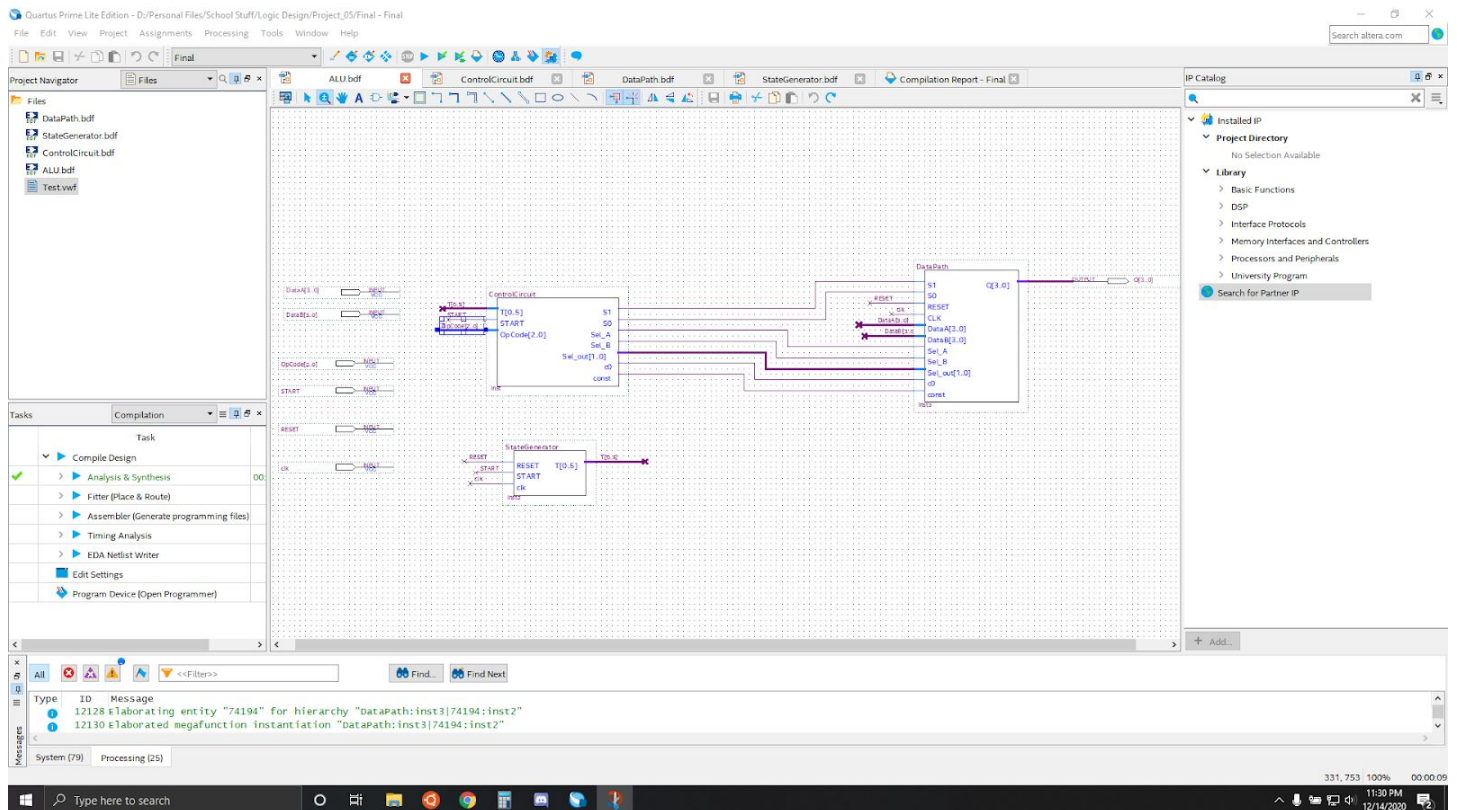
The screenshot shows the Quartus Prime IDE interface. The main workspace displays a logic diagram for a control circuit. The diagram includes several logic gates (AND, OR, NOT, XOR) and input/output signals. The left pane shows the Project Navigator with files like DataPath.bdf, StateGenerator.bdf, ControlCircuit.bdf, and ALU.bdf. The right pane shows the IP Catalog. The bottom pane shows the Messages window with a warning message about a hierarchy path.

Messages:

```

Type ID Message
12128 E Laborating entity "74194" for hierarchy "datapath:inst3[74194:inst2]"
12130 E Laborated megafuction instantiation "datapath:inst3[74194:inst2]"
System (79) Processing (25)
  
```

## Block Diagram for Completed Circuit:

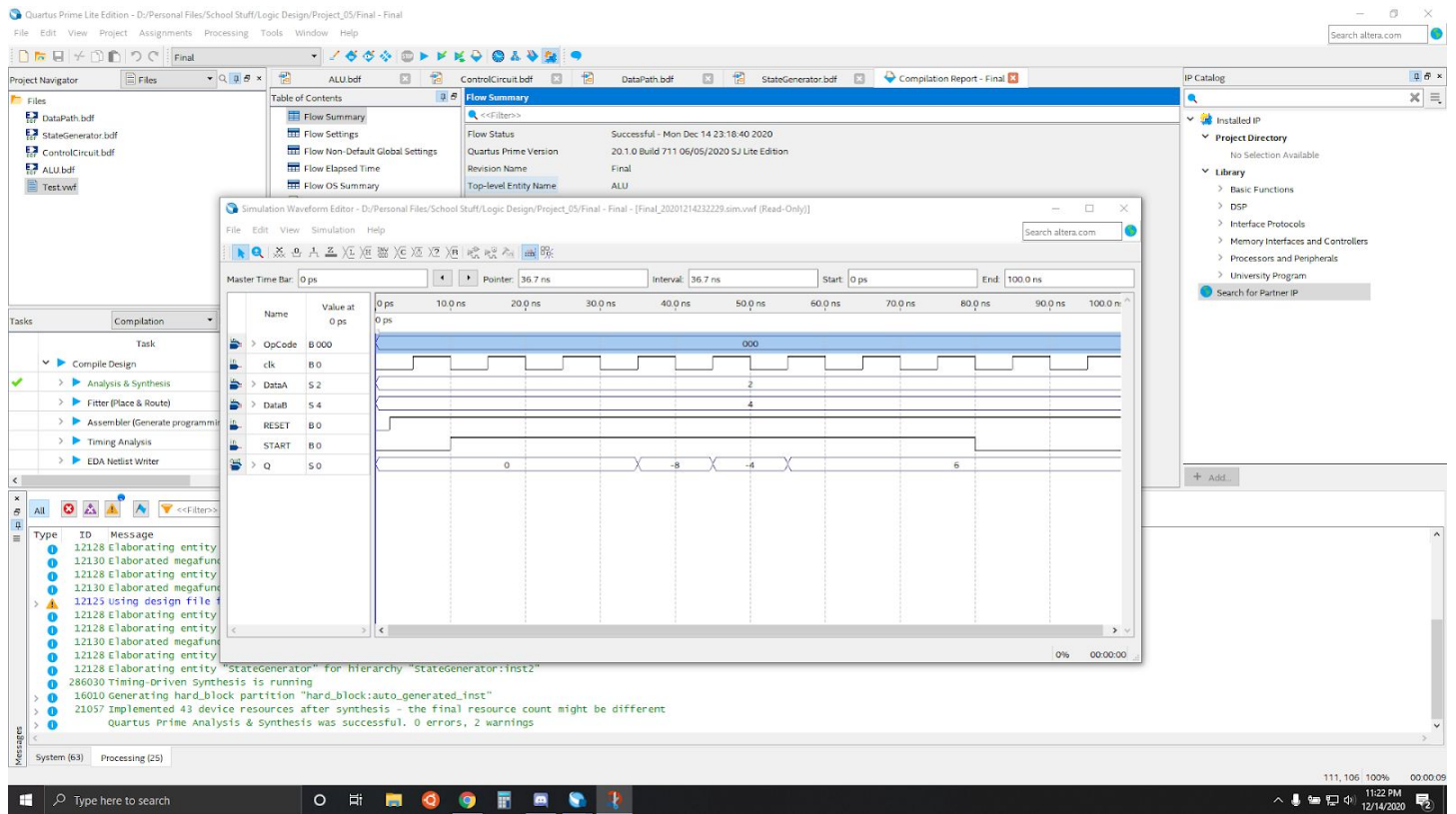


## Testing of ALU:

Paste images showing each OpCode being performed successfully below. Be sure to label each image with the Opcode being used and its instruction.

### Example:

Simulation for OpCode 000, A+B:





The screenshot displays the Quartus Prime Lite Edition software interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The main workspace is divided into several panels:

- Project Navigator:** Shows the project files, including DataPath.bdf, StateGenerator.bdf, ControlCircuit.bdf, ALU.bdf, and Testvdf.
- Table of Contents:** Lists the project's structure, including Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow OS Summary, and Flow OS Summary.
- Flow Summary:** Displays the project's status and settings. The Flow Status is "Successful - Mon Dec 14 23:10:40 2020". The Quartus Prime Version is "20.1.0 Build 711 06/05/2020 SJ Lite Edition". The Revision Name is "Final", and the Top-level Entity Name is "ALU".
- Simulation Waveform Editor:** Shows the timing diagram for the project. The Master Time Bar is set to 0 ps. The waveform displays signals for OpCode (001), clk (clock), DataA (2), DataB (4), RESET (0), START (0), and Q (0). The Q signal is shown with a value of 0 at 0 ps and a value of 3 at 100.0 ns.
- Messages:** Displays the compilation and simulation results. The messages indicate that the compilation was successful, with 0 errors and 2 warnings. The messages also show the timing analysis results, including the timing-driven synthesis and the final resource count.

The bottom status bar shows the system and processing status, indicating 65 systems and 25 processing units.

The screenshot displays the Quartus Prime Lite Edition interface during a compilation process. The top window, titled 'Flow Summary', shows the compilation status as 'Successful - Mon Dec 14 23:18:40 2020'. The bottom window, 'Simulation Waveform Editor', shows a timing diagram for various signals. The Q signal is highlighted, showing a sequence of values: 0000, 1000, 0100, 1010, and 1101. The Messages pane at the bottom indicates that the compilation was successful with 0 errors and 2 warnings.



The screenshot displays the Quartus Prime Lite Edition software interface. The main window is the Simulation Waveform Editor, showing a timing diagram for a circuit. The waveform is titled "Simulation Waveform Editor - D:\Personal Files\School Stuff\Logic Design\Project\_05\Final - [Final\_20201214232446.sim.vwf (Read-Only)]". The waveform shows signals for OpCode, clk, DataA, DataB, RESET, START, and Q over a time range from 0 ps to 100.0 ns. The Master Time Bar is set to 0 ps, and the Pointer is at 29.6 ns. The Interval is 29.6 ns. The Start and End times are blank.

The Messages window at the bottom shows the following messages:

```

12128 Elaborating entity
12130 elaborated megafunc
12128 elaborating entity
12130 elaborated megafunc
12125 Using design file
12128 elaborating entity
12128 elaborating entity
12130 elaborated megafunc
12128 elaborating entity
12128 elaborating entity
12128 elaborating entity "StateGenerator" for hierarchy "StateGenerator:inst2"
286030 Timing-driven Synthesis is running
16010 Generating hard_block partition "hard_block:auto_generated_instn"
21057 Implemented 43 device resources after synthesis - the final resource count might be different
Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 warnings

```

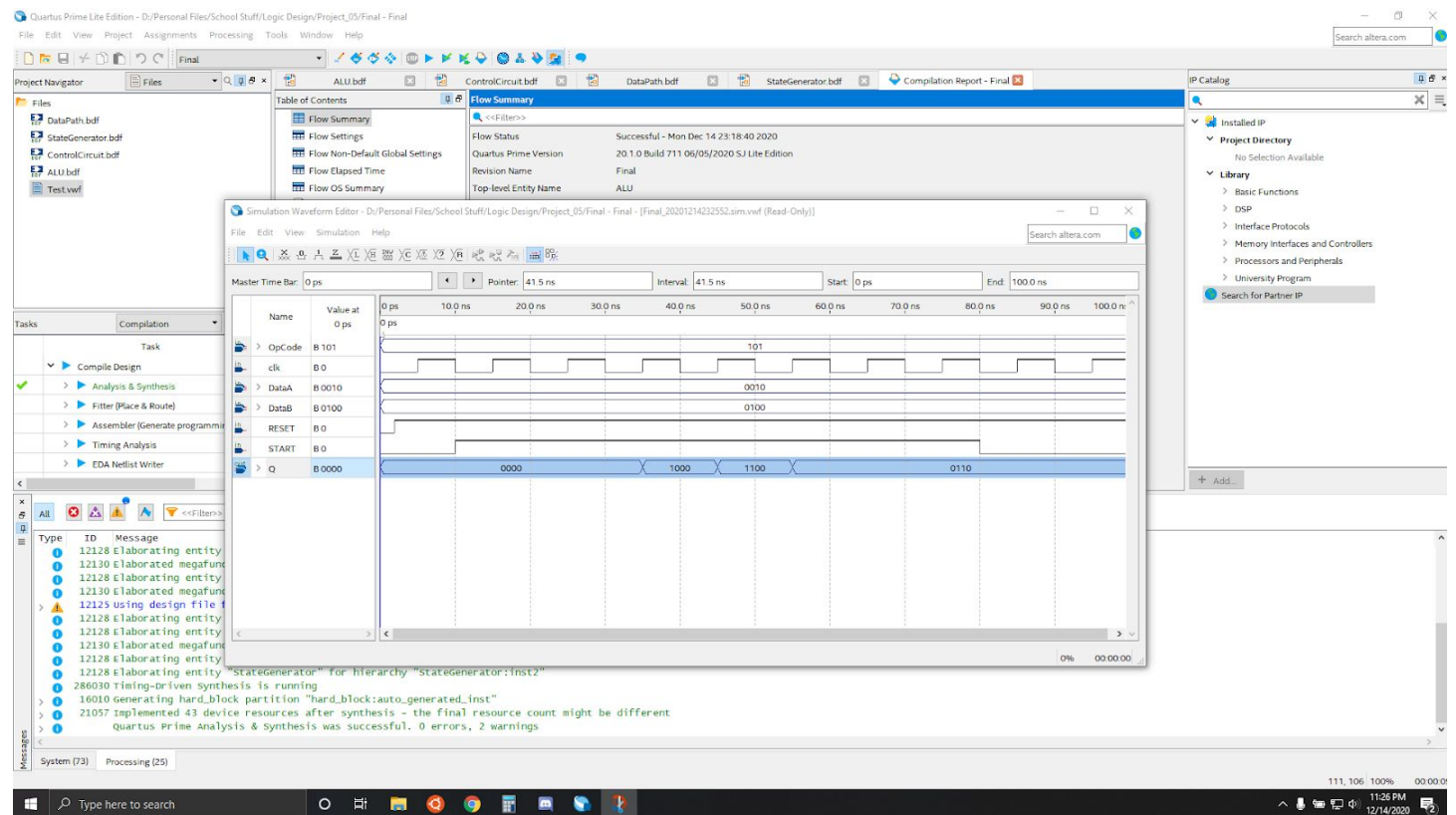
The Project Navigator on the left shows the project files: DataPath.bdf, StateGenerator.bdf, ControlCircuit.bdf, ALU.bdf, and Testwrf. The Table of Contents on the right shows the project structure: Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, and Flow OS Summary. The IP Catalog on the far right shows the installed IP and project directory.

The screenshot displays the Quartus Prime Lite Edition software interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The main workspace is divided into several panes:

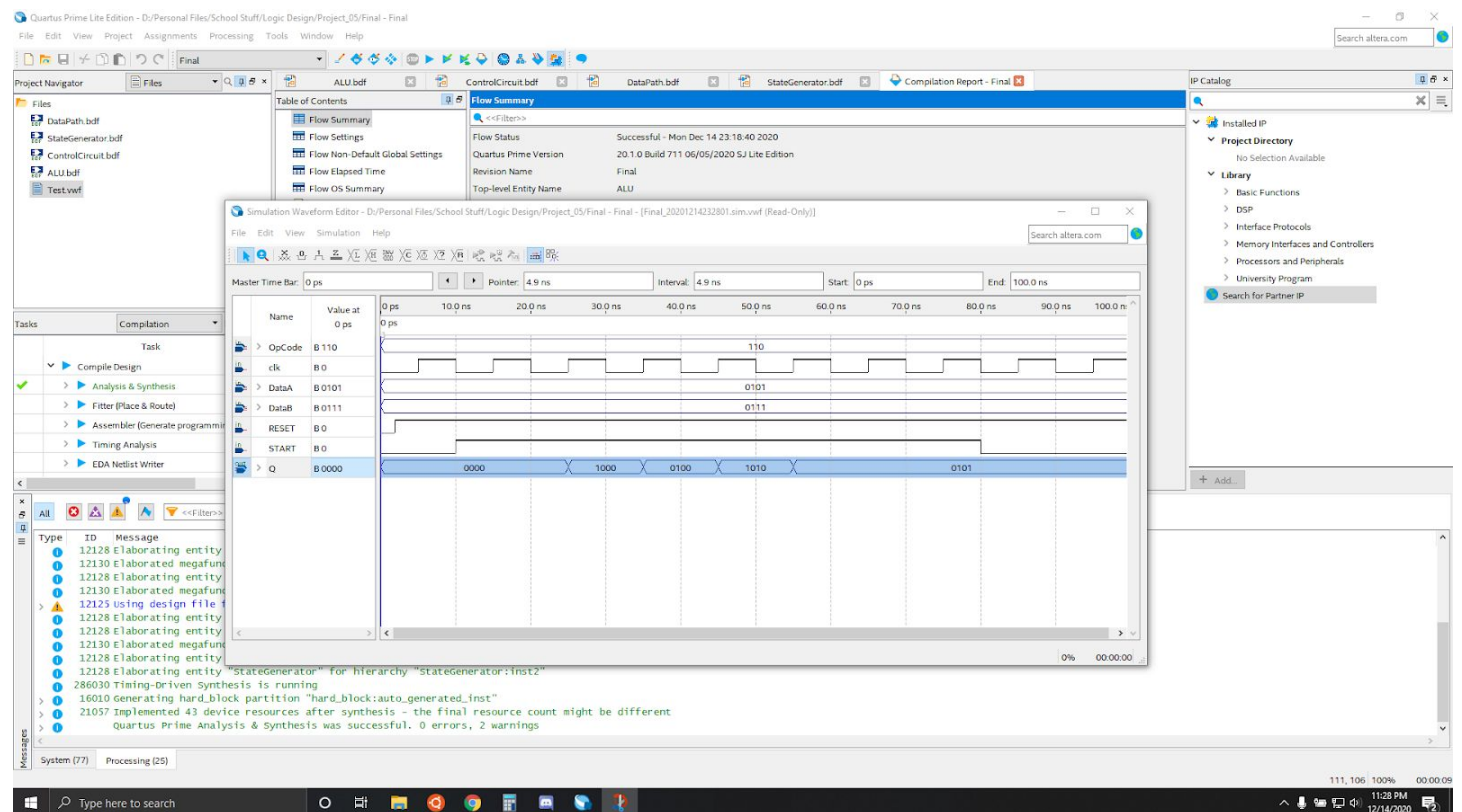
- Project Navigator:** Shows the project files, including DataPath.bdf, StateGenerator.bdf, ControlCircuit.bdf, ALU.bdf, and Testvwr.
- Table of Contents:** Lists the project's components, such as Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, and Flow OS Summary.
- Flow Summary:** Displays the project's status, including the flow status (Successful - Mon Dec 14 23:18:40 2020), Quartus Prime Version (20.1.0 Build 711 06/05/2020 SJ Lite Edition), Revision Name (Final), and Top-level Entity Name (ALU).
- Simulation Waveform Editor:** Shows the timing diagram for the project. The Master Time Bar is set to 0 ps. The waveform displays signals for OpCode, clk, DataA, DataB, RESET, START, and Q. The Q signal is shown as a sequence of values: 0, -8, 4, 2, 1.
- Messages:** Displays the compilation and simulation results. The messages indicate that the project was successfully compiled and simulated, with 0 errors and 2 warnings.

The bottom status bar shows the system (71) and processing (25) status.

## Simulation for OpCode 101, A | B:



## Simulation for OpCode 110, A & B:



## Simulation for OpCode 111, Negative A:

