

WEIGHING SCALE DESIGN

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A digital weight scale is one of the most precise analog instruments. It uses force sensors to measure the load offered by an object. Weigh scales are used in a multitude of applications ranging from point of sales terminals to industrial measurement equipment.

The most common method for implementing weigh scale designs uses a resistive load cell configured as wheat stone bridge. However, the sensor interface is complex due to precision requirements. In the load cells, the signal levels are low and the effect of noise is prominent. This article discusses how to measure this signal accurately to meet the requirements of precision measurement for weighing scales. It will discuss the different parameters of a load cell and their contribution to its inaccuracies. A weighing scale system is not just about the analog front end (AFE) for high accuracy measurement. It also needs many other things like a clear user interface and boost circuitry to deal with low battery conditions. Also, in some weighing scales, some kind of communication protocol may be needed to communicate with a host controller. Other considerations include managing cost and integrating a weighing scale design to implement all the features mentioned above.

Analog Front End

Let us begin with the analog front end of the weighing scales. Figure 1 shows the basic arrangement of analog front end for weighing scale applications.

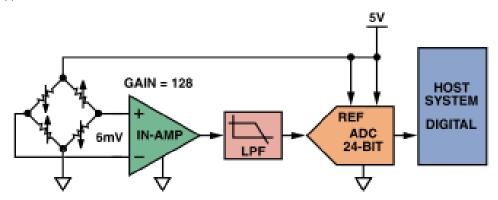


Figure 1. Analog front end for weighing scale

In this arrangement, the output of the transducer is first amplified, followed by a filtering stage to remove noise due to power supply and mechanical vibrations. Then this filtered output is sampled by a high resolution ADC. Load cells are nothing but resistive sensors which provide a ratio metric voltage corresponding to the load applied to them. Most commonly used load cells have strain gauges connected as a wheat stone bridge. Figure 2 shows the basic arrangement of strain gauges connected in wheat stone bridge to compose a load cell.

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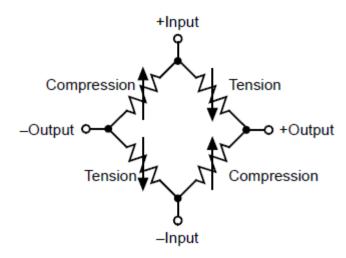


Figure 2. Full bridge load cell configuration

This is a full bridge arrangement for a load cell (also known as fully active as all the arms have strain gauges and contribute towards the change in output) in which two strain gauges have a positive change to tension whereas the other two have a positive change to compression. Thus, when a load is applied on the sensor, two of the sensors increase their resistance while the other two decrease. This change in resistance causes an unbalance in the bridge, thus providing a differential output corresponding to the weight placed.

Based on its construction, material, and design, load cells tend to have certain parameters associated with them. It is absolutely necessary to understand these parameters before designing a load cell interface.

Sensitivity (Rated Output)

This is one of the most important parameters of a load cell. The sensitivity of a load cell is defined as full load output voltage in relation to the excitation voltage. It is generally expressed in mV/V. This value corresponds to the voltage deviation caused by the load cell at full load when excited by a 1V source. The sensitivity of load cells is very low (generally about 2mV/V). If a system has a 3.3V excitation voltage then at full load, the output voltage will be 6.6mV. It makes the requirement for a high precision ADC mandatory while dealing with load cells.

Non-linearity

Load cells being mechanical devices, they have their own non-linearity based on their construction. A typical non-linearity of a load cell is about 0.015% of the rated output, which is approximately one bit when the ADC is sampling at 13 bits. However, one has to bear in mind that this is just one of component of non-linearity which is contributed by the load cell in the complete system. The measurement system and analog front end would have their own contributions into the systems' total non-linearity as well.

Hysteresis

Hysteresis error is seen as the change in load cell output when a known load is reached from a lesser weight as compared to when it is reached from a higher weight. This is caused due to deformation properties of the material used in construction of the load cell. A higher weight may temporarily deform the load cell which effectively adds a small offset which would show up when the target was reached from a higher weight.

Repeatability

This specification defines the change in the load measured by the load cell when the same weight is placed multiple times on the same load cell.

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Creep and creep recovery

Creep is the measure of change in measured weight over time, such as when a weight is placed on a scale for a long period of time. For example, output counts will be different when the weight is just placed and 30 minutes after. This effect is based on the elastic property of the material used in the load cell. Cheaper materials can result in very large creep values and it may take a long time for the load cell to recover from the deformation.

System Precision

Most weigh scale designers would have two different resolutions – the display resolution and the internal resolution. The display resolution is the resolution of the end result displayed by the weigh scale. The internal resolution is the actual resolution on the internal analog front end.

Now let us consider a weighing scale in which the load cell excitation voltage is 5V. In this case, its output voltage will be 0-10mV with a 2mV/V sensitivity. If the weighing scale has to be designed for a resolution of 5 gram and a total range of 10 Kg, the weigh scale's display resolution will be 1:2000. As mentioned earlier, in weighing scales display resolution is different from internal resolution, and it is standard practice to have internal resolution about 20-30 times of display resolution. So, for this weighing scale, the internal counts needed will be 1: 60000. This corresponds to a 16-bit internal resolution.

There are multiple means of induced error in the load cell interface starting with errors in the sensor itself, as discussed earlier. For this reason, the internal resolution is kept higher than the display resolution so that the design can compensate using some of the extra resolution.

The design would have to resolve the 10mV range of input with a 16-bit resolution. To measure this 10 mV full range output, the most commonly used method is to implement a gain stage to gain the input signal to fit the ADC's input range, as shown in figure 1, thus resolving more bits inside a smaller range. For example, to have a measurement range of 10mV as discussed earlier using an ADC that has a 1V range, the user can resort to getting close to 100x gain on the signal using an amplifier-based gain stage.

Consider an ADC with 20-bit resolution and an input range of 1V. The minimum input change this ADC can is resolve is 1uV. When we use a gain stage to amplify the signal prior to applying the signal to the ADC to improve the range to 0-10mV, the lowest resolved voltage would be as small as 10nV. This kind of resolution would place us deep inside the noise domain. The gain stage amplifies the noise as much as it amplifies the signal. This noise renders a considerable number of bits of the ADC as unusable and thus reduces the effective number of bits (ENOB). Thus, designers have to pick an ADC which gives an optimum ENOB for the required gain settings.

The most commonly used ADC to measure load cell's output is a Delta Sigma (DelSig) ADC. This ADC relies on the technique of oversampling the signal and later decimating it to achieve high resolution. This architecture makes the ADC have an inherent low pass nature which helps in reducing the effects of noise.

Having a very good ADC only solves one half of the puzzle. The gain stage is another requirement. Most designs use an external low noise amplifier for this purpose. But there are some devices in the market now like the Cypress's PSoC®3 and PSoC®5 that implement this gain stage in the ADCs input stage itself. The way this is achieved in the PSoC is by having an integrated input Buffer in the ADC's input that can achieve up to 8x gain. The ADC itself is capable of having a gain of up to 16x in its modulator stage.

As no external amplification stage is needed, such ADCs can provide about 18 effective number of bits since noise due to external amplifiers does not come into picture. But for a weigh scale application, resolution requirements are generally defined in terms of peak-to-peak resolution. This is the effective resolution calculated for a system after taking out the effect of the noise as a peak-to-peak value.

The general requirement for a commercial market space is 16-bit peak-to-peak resolution. This resolution would have to be achieved while measuring a full range of 10mV. The major concern would be dealing with system noise, thus bringing down the effective resolution.

Another major concern in a load cell interface is that it is prone to gain error because of how the output signal range is dependent upon the excitation voltage. Any variation in the excitation voltage can cause a similar percentage of gain error in the measurements. This can be avoided if the signal measurements are made as a ratio against the excitation voltage. This can be achieved by two means:

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- 1. One can measure the signal and excitation voltage separately and then calculate the ratio, thus taking out the gain error. However, this method requires multiplexing of the ADC between the two signals. The other problem with this approach is that the signal we are measuring is in the 10mV range and the excitation voltage would be the Volts range. This would mean dynamically changing gain settings and ADC range parameters, something which might not be advisable in most analog systems. In addition, changing these parameters dynamically would raise questions of mismatch of the two independent measurements made.
- 2. As shown in figure 3, the other means of achieving this is by using the reference to the ADC itself. ADCs generally have a reference pin to connect to an external reference. The input range of the ADC is defined as a factor of the reference voltage. Thus, every measurement made in the ADC is made with respect to the reference. If we provide the excitation voltage or a divided derivative of it as a reference to the ADC, we can achieve a ratio-metric measurement for the signal. Since load measurement in the load cell is a ratio of resistors, this approach fits the picture the best. Also, any variations in the excitation voltage would be unnoticed in the measurements since the ADC reference is also affected in the same way.

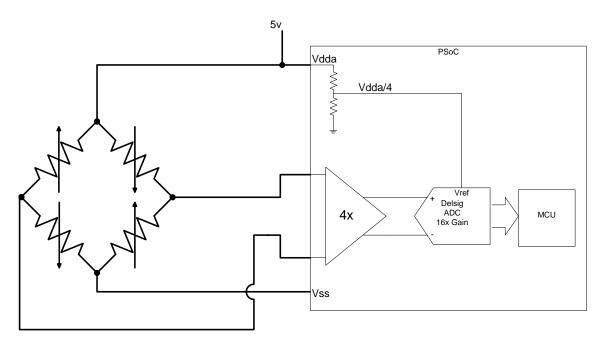


Figure 3. Load Cell interface Circuit for ratio-metric measurement

Noise reduction by Delta Sigma ADCs

There are some redundant characteristics of the frequency response of DelSig ADCs that can be made use of to reduce noise. Being a primarily averaging ADC, DelSig ADCs have a low pass nature which provides considerable noise reduction, as discussed earlier. Howver, most DelSig ADCs have a specific frequency response like a Sinc response on the PSoC3 and PSoC5 ADCs. This response has specific nulls in certain frequencies that are multiples of the sampling frequency.

Hence we can align the ADCs sampling rate to a specific value and thus eliminate a specific noise band. This can be particularly helpful when trying to eliminate noises sources like 50/60Hz noise.

More about filtering – Moving average filter

We have discussed means to avoid noise and other sources of error in the analog signal chain for a weigh scale design. One of the final steps to achieving a noise-free output resides in using a firmware-based mathematical filter to average out noise. An easy filter to implement is a moving average filter (Figure 4). It uses an array where the input values keep getting streamed in from one side and the oldest values fall off the array from the other side. At any given time, the output of the filter is the average of all of the elements in the array.

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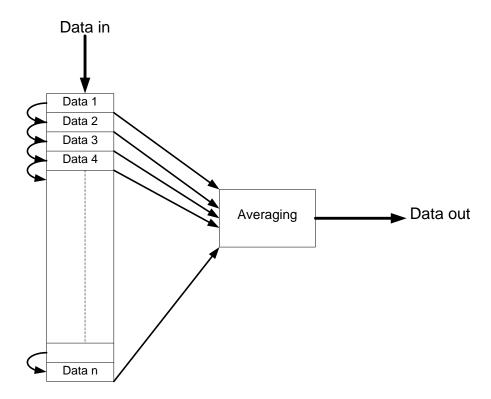


Figure 4. Moving average filter

The moving average filter is one of the easiest yet most effective filters to achieving higher noise-free bits from the measurement system. Note that there is a constant delay this filter imposes which is proportional to the depth of the array used. That means for an 'n' element moving average filter, every change is going to take 'n' cycles to reflect itself in the output. This can be a bit misleading if there are larger variations and the output slowly catches up. This condition can be avoided by having a threshold condition check on variations. For example, if the input varies more than a threshold at a specific point of time, the whole filter is flushed and new data is copied in the filter and also into the output, thus reducing the latency for larger variations. Filter size needs to be selected dependent on the required resolution, ADC's sample rate, and response time specification of the weigh scale.

System design and Integration

Until now, we have been discussing analog front end design and different considerations to improve performance. However, an entire weigh scale solution is more than just the analog front end. Based on the application segment, every weigh scale design could have varying integral components ranging from communication interfaces to user interfaces. Figure 5 shows a typical implementation of a weigh scale solution.

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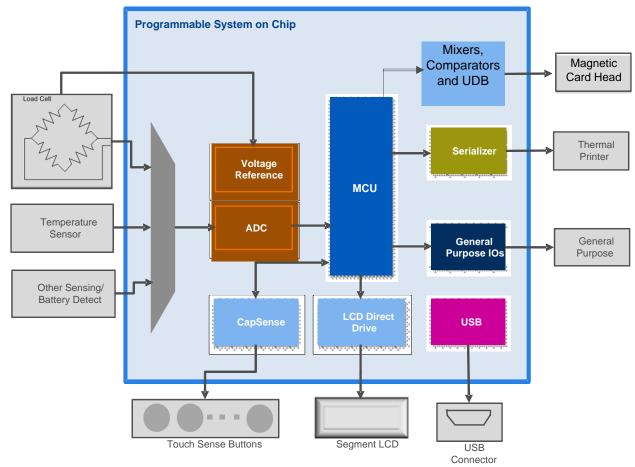


Figure 5. Integrated Weigh scale solution based on a Cypress PSoC 3 device

Apart from implementing the analog front end for load cell, the system might be also measuring other analog sensors. Some high precision weigh scales may require temperature monitoring to compensate for drifts in the load cell parameters with temperature. This could mean implementing a thermistor interface. If the entire assembly is expected to be portable, then the design might also need a battery charger interface. This would require an ADC for voltage and current monitoring and separate comparators for over voltage and current protection circuits. There are application-specific devices available in the market that implements battery charging, but the same could be integrated into the SOC with a programmable device like the PSoC3.

As far as user interfaces are concerned, inputs can be simple tactile buttons. With current touch technology, some designs might be good candidates for a capacitive sensing interface. Also, the outputs would be LCDs and due to extreme cost pressure, most designs resort to direct drive for LCDs thus avoiding the cost of LCD drivers.

Communication interfaces could range from a simple USB link to the host processor to an SPI/I2C to another wireless communication device. Having these interfaces integrated can reduce a lot of cost of the system.

Until now, we were talking about the basic components needed in most of the designs. But some weigh scales like the ones in point of sales terminals might also have an opportunity of integrating a thermal printer and a magnetic card reader interface. The thermal printer is built using nothing but a serializer similar to an SPI interface, a motor driver circuit, a little more analog to measure the head's temperature, and a paper sensor. A lot of programmable SoCs have a programmable digital array that can be programmed to integrate a Thermal printer interface.

A magnetic card is another complicated analog function that is mostly implemented in an ASIC platform. But when one can have the capability to also integrate this in the same SOC like the Cypress's PSoC3, the result can be significant BOM

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savings. Programmability of SoCs allows different resources to be reconfigured at runtime i.e. ADC's specification (input range, resolution etc), connections between different peripheral etc. In weighing scale applications, all the operations – measurement, printing and card reading are not done at the same time. So, all the resources on the chip can be used in a time-shared basis to provide an highly compact and cost effective approach.

Weighing scale systems are one of the most precise measurement systems. Their reliable design needs designers to understand the basics of load cells to be aware of different sources of errors in the system and to find out the specifications needed from the analog front end i.e. the specifications for the ADC, amplifiers, and filter. Delta Sigma ADCs are the best type of ADC to be use in these applications because of their ability to deal with high frequency noise due to their inherent LFP response and to deal with power supply noise by adjusting the sample rate. An inbuilt gain stage in ADC can help in reducing the overall noise in the system and provide a greater ENOB compared to what could be given when an external gain stage is used. A firmware based filter (i.e. moving average filter) is needed to further reduce noise. Need of other components in the system, i.e. user interface (buttons. LCDs etc), communication interface like USB, UARTv etc, temperature sensing makes SoCs the best fit for these applications to provide a highly integrated and cost effective solution in today's competitive market. SoCs also allow other solutions to be integrated on the same chip i.e. thermal printer and magnetic card reader.

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