Exploring Machine Learning for Electrical Behavior Prediction: **The CMOS Inverter Case Study**

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Structure

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Context


IBM Creates First 2nm Chip
by Dr. Ian Cutress on May 6, 2021 6:00 AM EST
Posted in CPUs GPUs SoCs IBM GAAFET 2nm
117 Comments
+ Add A Comment

The Problem

↑ Technology Complexity ∴ ↑ Design Process Variability

Affects

- Delay
- Power Consumption

In order to avoid

Simulations
(can take very long)

Possible Solution

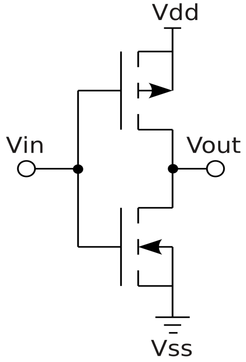
Machine Learning
Thus, reducing cost of production

- More corner cases must be considered during the electrical characterization
- Machine learning can assist digital design in many levels

Goal

Regression Task!

CMOS INVERTER CIRCUIT



https://pt.wikipedia.org/wiki/CMOS

SIMULATION DATA

(temperature, voltage, process variability...)

SUPERVISED ALGORITHMS

MACHINE LEARNING MODELS

Multiple Linear Regression
Support Vector Regression
Decision Trees
Random Forest

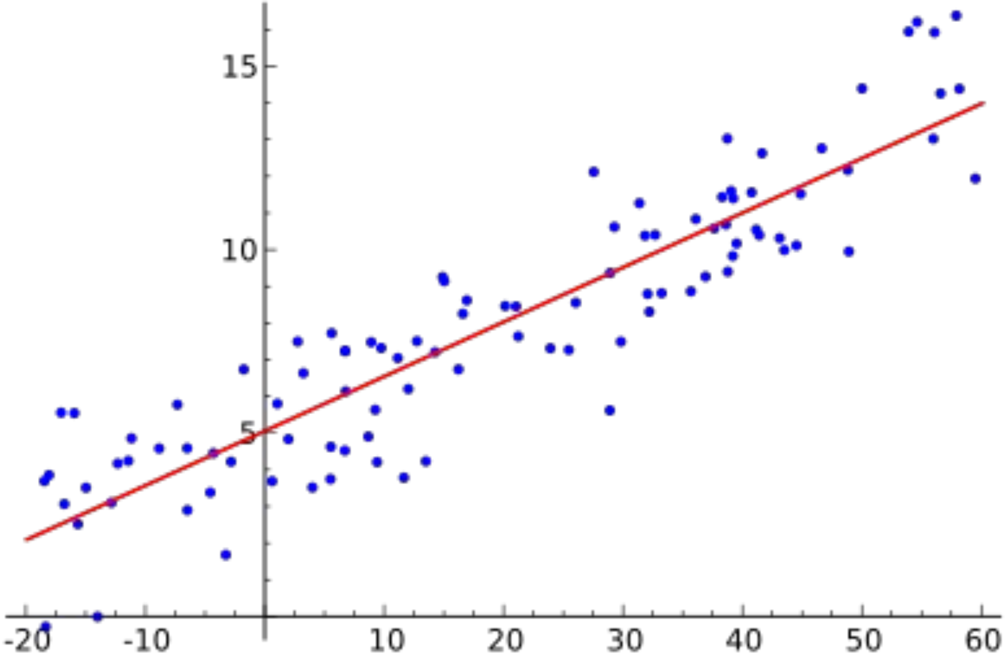
PREDICTION

TARGETS

- **$Tp_{L}H$**
- **$Tp_{H}L$**
- **Energy**

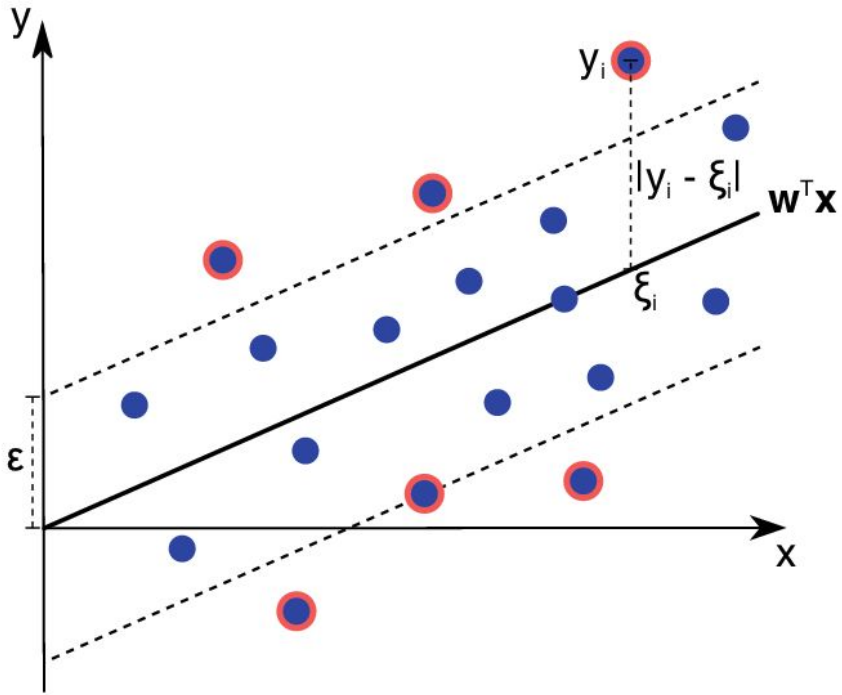
SYNOPSYS HSPICE® | pandas | NumPy

Multiple Linear Regression (MLR)



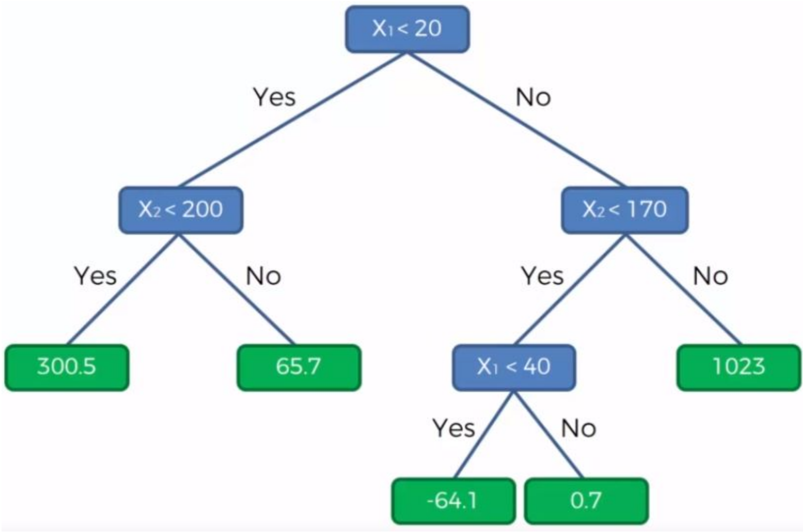
$$\hat{y} = \theta_0 + \theta_1 x_1 + \theta_2 x_2 + \ldots + \theta_n x_n$$

Support Vector Regression

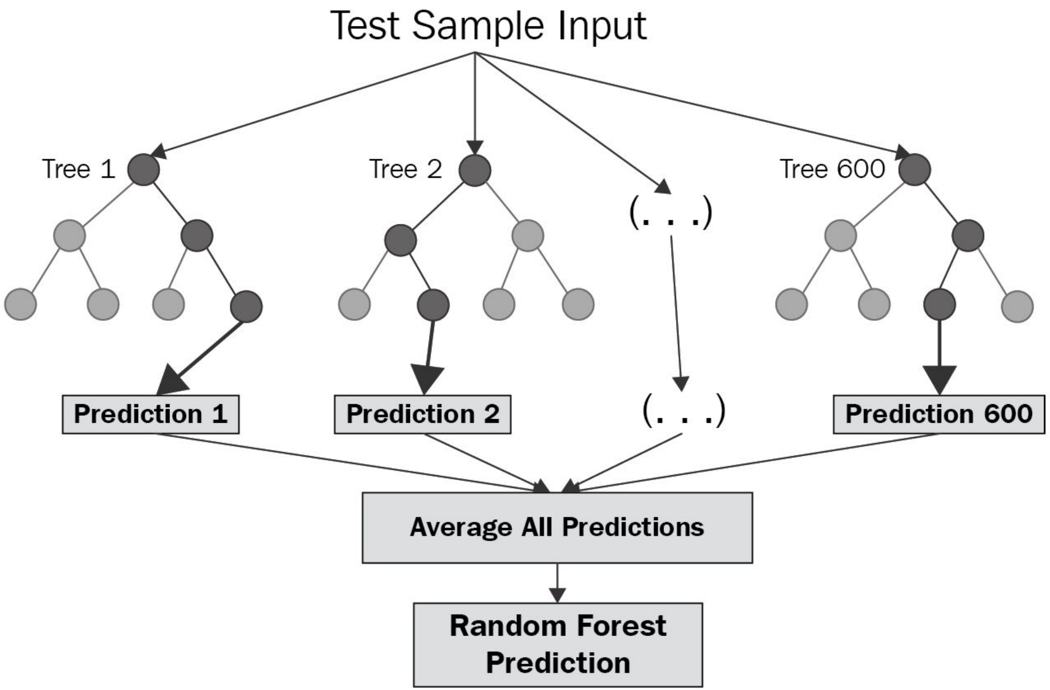


$$\hat{y} = w^{T} x + b$$

Decision Tree

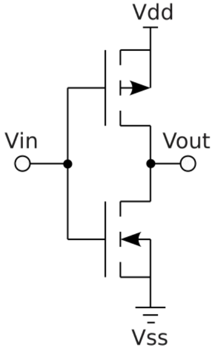


Random Forest



Training Flow - Overview

I. Simulation



II. Feature Extraction → **III. Data Processing** → **IV. Algorithms** → **V. Evaluation**

↓

VI. Results

↓

VII. Model Deployment

Feature Extraction

1000 Monte Carlo transient simulations of 20ns with step of 0.1ns in HSPICE

Features

NMOS Vth0
PMOS Vth0 (threshold voltage)
Temperature (-25, 0, 50, 75, 100°C)
Voltage (0.6, 0.7, 0.8, 0.9V)
Width PMOS (70, 140, 280, 350, 420nm)
Width NMOS (70, 140nm)
Length (20, 32, 40nm)

Targets

High-Low Propagation (Tp_HL)
Low-High Propagation (TP_LH)
Energy

Data processing (Scaling)

$$x' = \frac{x - \min(x)}{\max(x) - \min(x)}$$

MIN-MAX Scaler

Algorithms (Cross Validation)

Values & Best Hyperparameters

- DT - **Max Depth**: 1, 5, 10, 25, 50
- RF - **Max Depth**: 1, 5, 10, 25, 50
- RF - **N Estimators**: 5, 25, 50, 100, 150

	DT - **Max Depth**	RF - **Max Depth**	RF - **N Estimators**
Tp_HL	5	5	25
Tp_LH	10	10	150
Energy	10	10	150

50%
Training Set

25%
Validation Set

25%
Test Set

Evaluation Metrics

$$\sqrt{\frac{1}{m}\sum_{i=1}^{m}(h(x^{(i)}) - y^{(i)})^2}$$

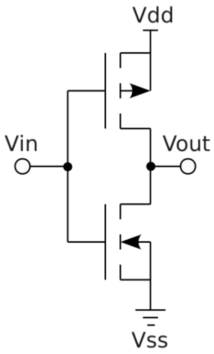
Root Mean Square Error (RMSE)

$$R^2 = 1 - \frac{\sum_i (y_i - \hat{y}_i)^2}{\sum_i (y_i - \bar{y}_i)^2}$$

Coefficient of Determination (R^2)

Training Flow

I. Simulation



II. Targets

Energy
TPHL
TPLH

II. Features

Voltage
Temperature
Width PMOS
Width NMOS
Length
Nmos Vth0
Pmos Vth0

III. Data Processing

Min-Max Scaler

$$x' = \frac{x - \min(x)}{\max(x) - \min(x)}$$

50% Training Set

25% Validation Set

25% Test Set

IV. Algorithms

Multiple Linear Regression
Support Vector Machine
Decision Trees
Random Forest

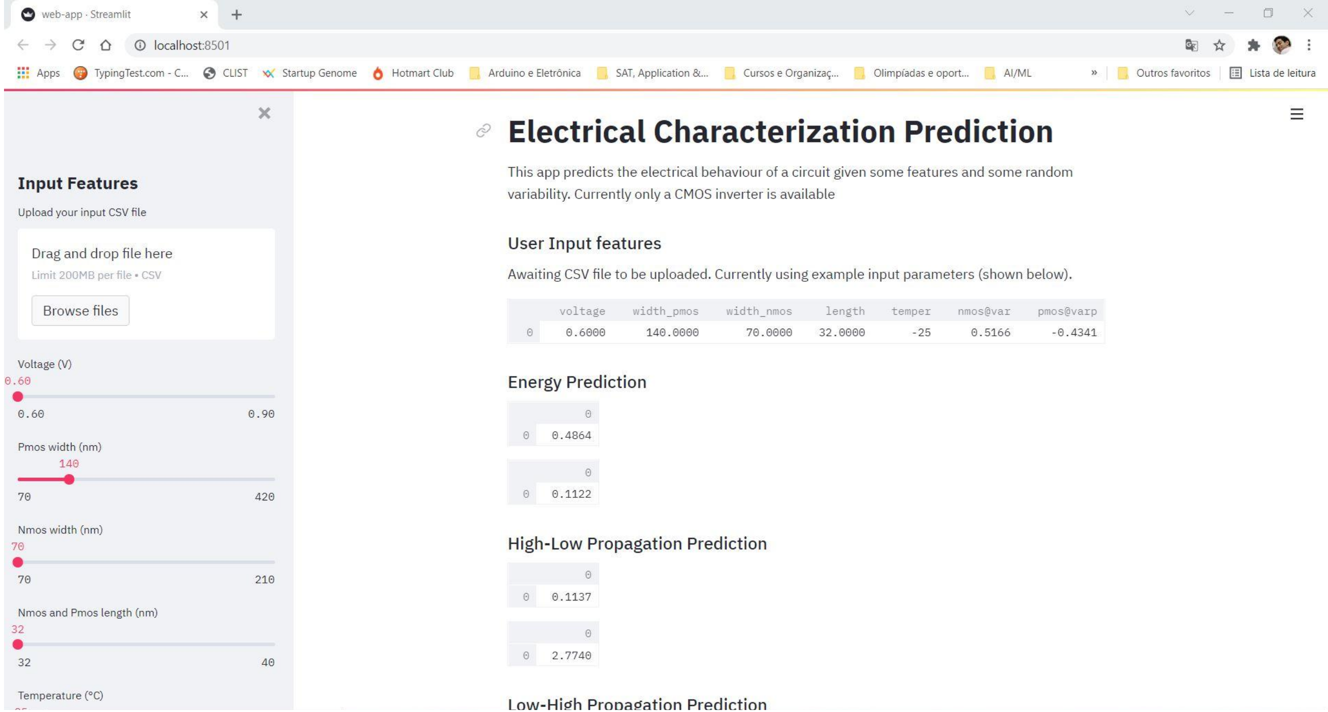
V. Evaluation

$$\sqrt{\frac{\sum_{t=1}^{T}(\hat{y}_t - y_t)^2}{T}}.$$

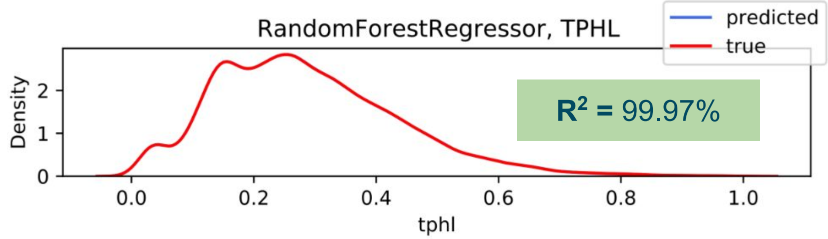
VI. Results

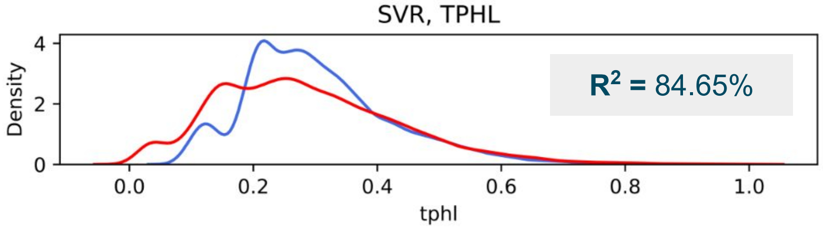
VII. Model Deployment

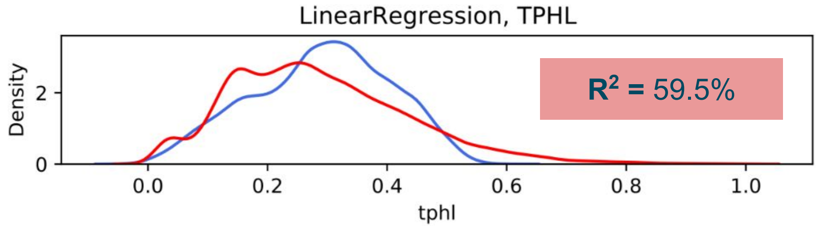
Model Deployment

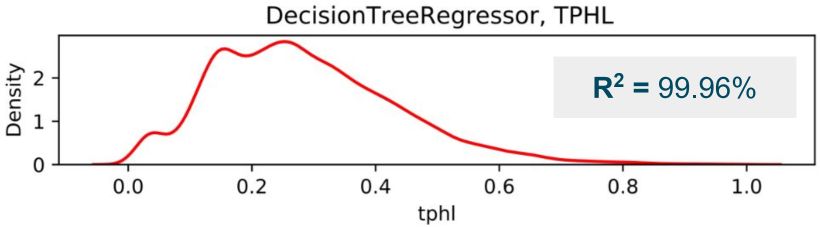


Tp_HL Prediction

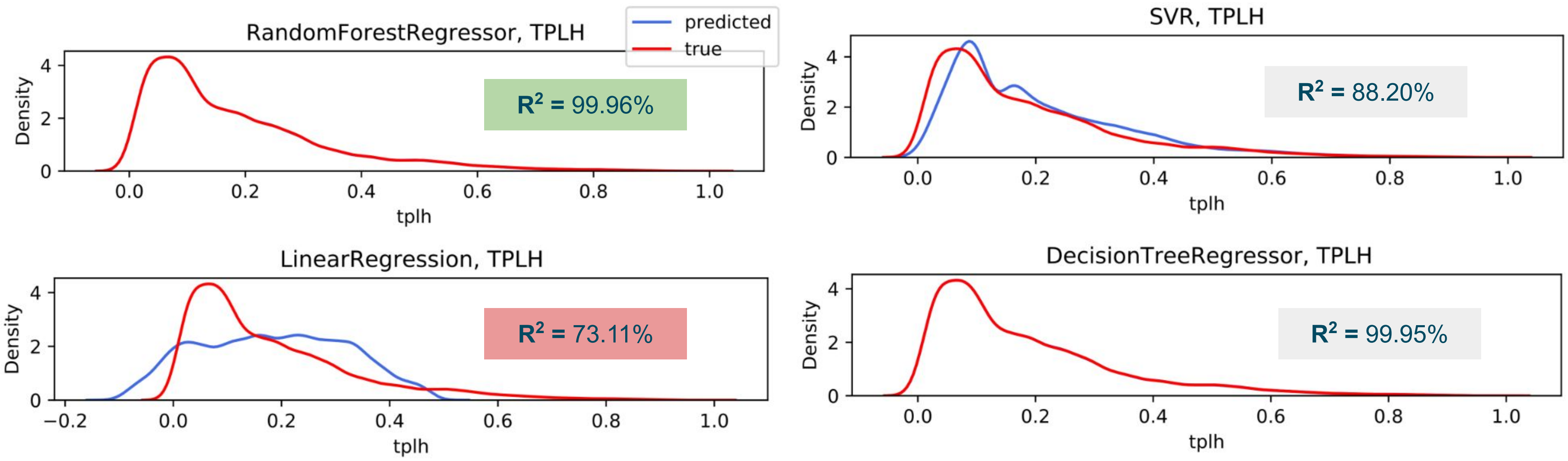




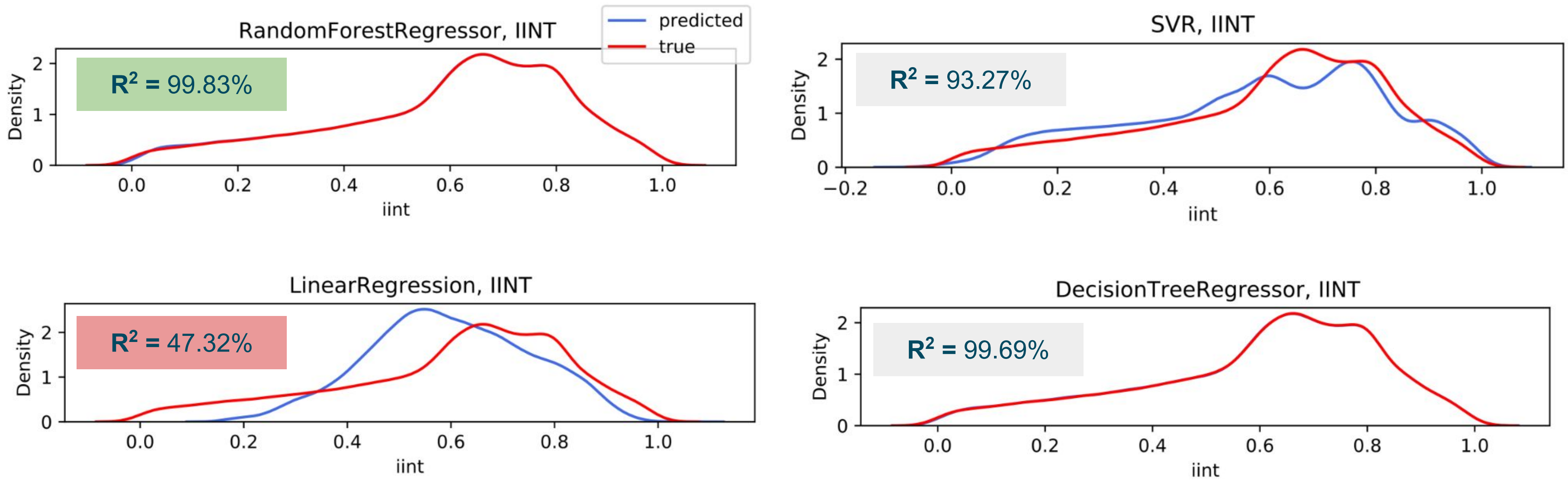




Tp_LH Prediction



Energy Prediction



Simulation vs Inference Time

Single Hspice electrical simulation = 0.069 s
DT = 0.0006 s (115×)
RF = 0.0432 s (1.59×)

Best Algorithm

Random Forest

Worst Algorithm

Multiple Linear Regression

Possible Applications

Foundries can adopt ML to cell characterization and make available the machine learning model trained, protecting the private data of the device models.

Future Works

Basic gates from a standard cell library

Investigate Neural Networks architectures

Evaluate the dependencies between the ML models and the technology node, considering FinFET devices

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Appendix

Pearson Correlation Coefficients