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Abstract
Purpose – The aim of this paper is to formulate the effect of the process variation on various leakage currents and subthreshold swing factor in FinFET devices. These variations cause a large spread in leakage power, since it is extremely sensitive to process variations, which in turn results in larger temperature variations across different dies.
Design/methodology/approach – Owing to large temperature variation within the die, the authors investigate the variation of various leakage currents with absolute die temperature.
Findings – The results obtained on the basis of the model are compared and contrasted with reported numerical and experimental results. A close match was found which validates the analytical approach.
Originality/value – The analytical modeling of subthreshold leakage current, subthreshold swing, gate leakage current and its variation with process parameters are carried out in this paper.

Keywords Electric current, Temperature measurement, Integrated circuits

Paper type Research paper

Introduction

Double gate (DG) FinFETs (Hisamoto, 2000) have emerged as a better alternative to replace the conventional bulk MOSFETs for scaling even down to a 10 nm feature size and below. FinFETs, with the physical gate length of 10 nm, have already been experimentally fabricated (Choi *et al.*, 2001; Yu *et al.*, 2002). The next essential step is the optimization of these ultrascaled devices to achieve superior performance in circuit applications. High subthreshold leakage current and rise in gate leakage current would make scaling technology invariable. DG devices such as FinFET reduce short channel effects (SCE's). Further fabrication of FinFET devices using conventional bulk technology is also possible. Therefore, without excessive change in feb-line new technology can be easily convinicated for better performance and scalability. To improve electrical characteristics, several innovative device structures such as ultra-thin-body SOI and FinFET (Hisamoto, 2000) have been proposed. However, FinFETs have confined channel, surrounded by silicon dioxide, which has lower thermal conductivity compared to bulk silicon (Su *et al.*, 1994). This results in increased self-heating and aggravated thermal issues (Pop *et al.*, 2003). Under high-frequency operation, temperatures rise due to large active power consumption. The high temperature increases the sub-threshold leakage (which is strong function of temperature), further increasing temperature. If heat cannot be dissipated effectively, a positive feedback between leakage power and temperature can result in thermal runaway (Choi *et al.*, 2006). To predict thermal runaway, it is important to account for all the components of power dissipation self-consistently with respect to temperature. Many research works have been conducted to estimate leakage power under process variation (Chang and Sapatnekar, 2005; Rao *et al.*, 2003; Choi *et al.*, 2007). In previous works, however, the temperature dependence of leakage current was not considered and the impact of dynamic power on leakage and temperature was not appropriately accounted for. CMOS with gate length of 50-70 nm needs an oxide thickness of around 1.5-2.0 nm, which corresponds to two to three layers of silicon atoms (Jeon and Burk, 1989; Lucci *et al.*, 2003; Ortiz-Conde *et al.*, 2005; Harrison *et al.*, 2004). With such a thin oxide, direct tunneling occurs, resulting in exponentially increasing gate leakage current. This gate leakage current increases power dissipation and deteriorates device performance and circuit stability for ULSI (Taur *et al.*, 1997). The key feature of multi-gate FinFET is strong gate control of the channel region suppressing effectively the SCE. Moreover, the role of quantum-mechanical (QM) effects becomes more important in these devices with an ultra-thin gate dielectric and Si body. One of such QM effects, which has been recently predicted for ultra-thin body single-gate and DG FinFET, is the reduced gate tunneling currents compared to planar bulk-Si devices due to the reduced transverse electric field and less quantum carrier confinement (Chang *et al.*, 2002; Rudenko

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et al., 2006). The above gate current reduction was predicted to be enhanced for the increased physical dielectric thickness and hence for higher-k dielectrics. This is a promising find since it may relax the restrictions on the gate oxide thickness scaling.

In this paper, we investigate the combined effect of process variation and die temperature as leakage current for FinFET devices. The analytical modeling of subthreshold leakage current, subthreshold swing and gate leakage current have been carried out in this work.

FinFET design parameters

Figure 1 shows the 3D structure of FinFET device and Figure 2 shows key geometric parameters for a FinFET. FinFET devices are built as SOI wafer and the current flows through very thin silicon body "fin" perpendicular to wafer plane. The fin-shaped body is surrounded by gate electrode to achieve a stricter container over the channel and hence current. The distance between the source and drain is referred to as the gate length, L_{gate}. H_{fin} is the fin height. The oxide thickness between the side gates and the fin is t_{ox}. The oxide thickness between the top gate and the fin is t_{ox-top}, W_{fin} is the fin width ($W_{fin} = 2H_{fin} + T_{fin}$)and T_{fin} is the fin thickness. Fin engineering (balancing height, fin thickness, oxide thickness, and channel length) is essential in minimizing the leakage current, I_{off}, and maximizing the on current, I_{on} (Huang *et al.*, 2001; Joshi *et al.*, 2004). FinFET is a symmetric DG structure. It means that both the front and back gates have the same work function and are tied to the same bias, so the two surface channels turn on at the same time. The independent control of front gate and back is possible by electrically isolated them from each other. When a potential larger than the threshold voltage, V_T, is applied between the gates of the DG FinFET device and source, current flows from the drain to the source. The DG, however, allows modulating the channel from two sides instead of one. The two gates together strongly influence the channel potential, combating the drain impact, and leading to the better ability to shut off the channel current. DIBL is thus reduced, and the swing is improved.

Figure 1 3D structure of FinFET device

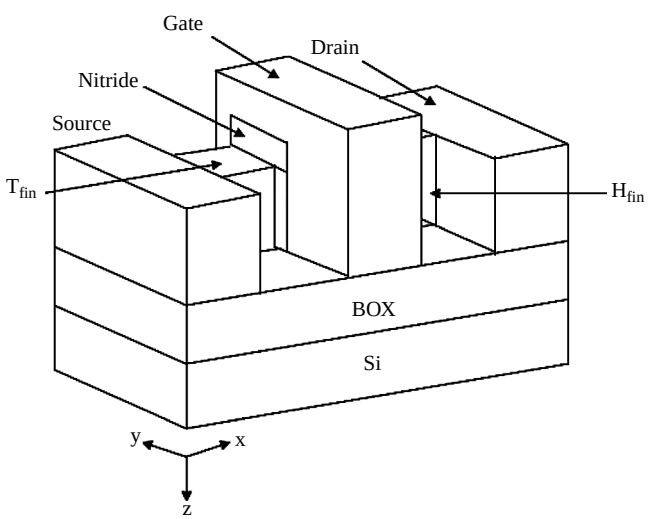
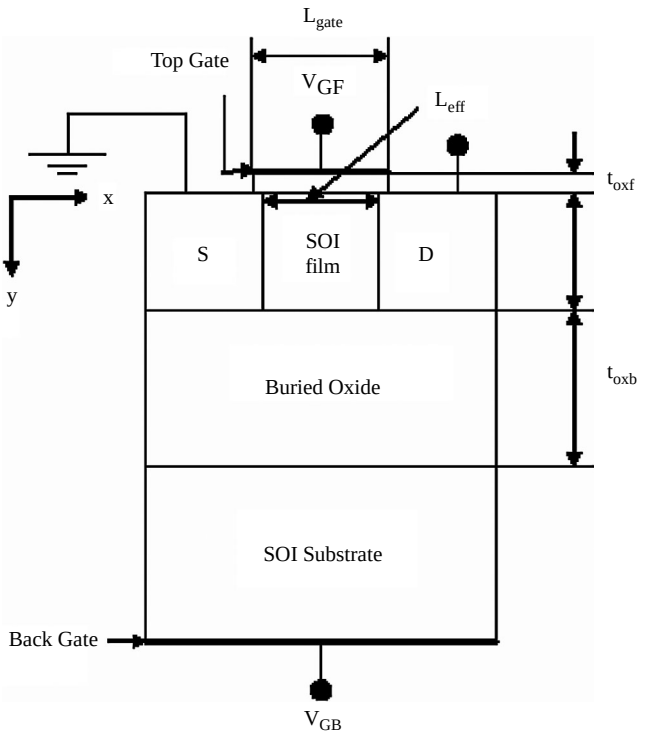


Figure 2 Cross-sectional view of FinFET along the channel length



Subthreshold swing

A commonly used parameter in characterizing leakage behavior of deep submicrometer circuit is the subthreshold swing (also called subthreshold slope). The subthreshold swing (S) is the amount of variation required in gate-to-source (V_{gs}) or threshold voltage (V_{th}) in order to vary the weak inversion current by one decade (Kursun and Friedman, 2006). Two key characteristics of a DG FinFET that are particularly important to digital applications are threshold voltage (V_{th}) and subthreshold swing. As the effective channel length (L_{eff}) of a DG FinFET is reduced, threshold voltage (V_{th}) typically decreases and subthreshold swing (S) increases, commonly known as SCE. Consequently, the ratio of the drive current to the leakage current is substantially reduced, which results in significantly increased stand-by power. The analytically evaluated subthreshold swing factor is given by Chen and Meindl (2004):

$$S = \left[1 - 2\Gamma_1 \cos\left(\frac{T_{fin}}{4\lambda_1}\right) \exp\left(-\frac{L_{gate}}{2\lambda_1}\right)\right]^{-1} \frac{kT}{q} \log 10. \quad (1)$$

The parameter λ_1 is determined by the vertical dimensions:

$$\lambda_1 = \frac{1 + (1/r)}{1 + (\pi/2)} T_{fin}, \quad (2)$$

where $r = \varepsilon_{ox} T_{fin} / \varepsilon_{Si} t_{ox}$, is the gate oxide thickness, and ϵ_{ox} and ϵ_{Si} are the permittivity of the gate oxide and silicon, respectively. The parameter Γ_1 is given as (Chen and Meindl, 2004):

$$\Gamma_1 = \frac{2\lambda_1}{T_{\text{fin}}} \frac{\sqrt{1 + (T_{\text{fin}}^2/r^2\lambda_1^2)}}{((1/r) + (1/2) + (1/2)(T_{\text{fin}}^2/r^2\lambda_1^2))}. \quad (3)$$

We define a new term subthreshold swing factor (S_f) as the ratio of subthreshold swing of device to that of ideal value of subthreshold swing (60 mV/dec).

Threshold voltage

The threshold voltage analysis methodology is applied to highly scaled DG FinFET device, by using the relation between the two coupled gates. We can derive the QM threshold voltage, V_{th} of the DG FinFET as (Chiang *et al.*, 2006):

$$V_{\text{th}} = V_{\text{FB}} + \psi_{\text{s(inv)}} - \frac{Q_{\text{b}}}{2C_{\text{ox}}} + \Delta V_{\text{th.QM}}, \quad (4)$$

where V_{FB} is the flat-band voltage, $\Psi_{\text{s(inv)}}$ is the surface potential at threshold, $\Delta V_{\text{th,QM}}$ is the threshold voltage increase due to quantum mechanical effects, which can be approximated as a function of the ratio of the carrier effective mass in the direction of confinement to the free electron mass and silicon film thickness, (Chiang *et al.*, 2006) and Q_{b} is given as:

$$Q_{\text{b}} = -qN_{\text{A}}T_{\text{fin}}. \quad (5)$$

When considering the QM confinement of inversion-layer carriers, V_{th} of equation (4) should be augmented with $\Delta V_{\text{th,QM}}$. The surface potential at threshold is given by:

$$\psi_{\text{s(inv)}} = 2\psi_{\text{b}}, \quad (6)$$

$$\psi_{\text{b}} = \frac{kT}{q} \ln\left(\frac{N_{\text{A}}}{N_{\text{i}}}\right). \quad (7)$$

Substitute the value of ψ_{b} from equations (7) into equation (6), we obtain:

$$\psi_{\text{s(inv)}} = 2\left(\frac{kT}{q} \ln\left(\frac{N_{\text{a}}}{N_{\text{i}}}\right)\right), \quad (8)$$

$\Delta V_{\text{th,QM}}$ is change in threshold voltage due to QM effects, which is given by Trivedi *et al.* (2003):

$$\Delta V_{\text{th.QM}} \cong \frac{S}{(kT/q)\ln(10)} \times \frac{0.3763}{(m_{\text{x}}/m_{\text{L}})T_{\text{fin}}^2}, \quad (9)$$

where S is the subthreshold swing, T_{fin} is fin thickness and $m_{\text{x}}/m_{\text{L}}$ is the ratio of the carrier effective mass in the direction of confinement to the free electron mass (e.g. 0.92 for electrons and 0.29 for holes).

Substitute the value of $\psi_{\text{S(inv)}}$ from equation (8), Q_{b} from equation (5) and $\Delta V_{\text{th,QM}}$ from equation (9) into threshold voltage expression equation (4). The final expression for the threshold voltage is obtained as:

$$V_{\text{th}} = V_{\text{FB}} + 2\left(\frac{kT}{q} \ln\left(\frac{N_{\text{A}}}{N_{\text{i}}}\right)\right) - \frac{(kT/q)\ln(N_{\text{A}}/N_{\text{i}})}{2C_{\text{ox}}} + \frac{S}{(kT/q)\ln(10)} \times \frac{0.3763}{(m_{\text{x}}/m_{\text{L}})T_{\text{fin}}^2}. \quad (10)$$

Subthreshold leakage current modeling

A MOSFET operates in the week inversion (subthreshold) region when the magnitude of the gate-to-source voltage is less than the magnitude of the threshold voltage. In the weak inversion mode, current conduction between the source and drain (the subthreshold leakage current) is primarily due to diffusion of the carriers (Kursun and Friedman, 2006). Subthreshold leakage current is a sensitive function of subthreshold leakage current, effective gate length and fin width. As the channel length increases, I_{sub} decreases because longer channel reduces DIBL and SCE (Taur and Ning, 1998). On the contrary, I_{sub} increases with larger fin width (W_{fin}). It is because thinner body allows gates to better control the electrostatic of the channel reducing SCE. Hence, while modeling subthreshold leakage, careful attention should be given to the combined effect of temperature as well as device parameters, effective gate length and fin width.

An empirical relationship was developed through curve fitting to estimate subthreshold leakage current variation with temperature. Subthreshold leakage current (I_{sub}) in DG FinFET devices is expressed as (Choi *et al.*, 2007):

$$I_{\text{sub}} = 2\frac{W_{\text{fin}}}{L_{\text{gate}}} C_{\text{g}}\mu_{\text{eff}}(E_{\text{y}})\left(\frac{kT}{q}\right)^2 \text{e}^{(-qV_{\text{th}}/SkT)}, \quad (11)$$

where $C_{\text{g}} = \varepsilon_{\text{ox}}/t_{\text{ox}}$ is the effective gate capacitance per unit area, $\mu_{\text{eff}}(E_{\text{y}})$ is transverse electric field dependent effective mobility, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, V_{th} is the threshold voltage of the device and S is the subthreshold swing factor. Note that the temperature dependence of I_{sub} is dominated by the exponential term and that I_{sub} has exponential dependence on threshold voltage V_{th}.

Mobility modeling

For the purpose of evaluating the field dependent mobility of the charge carriers in FinFET, the electric field in the transverse direction is to be evaluated. This can be found out from the potential variation of one gate to another. The model assumes that the channel mobility is the sum of the reciprocal mobility derived from three different scattering mechanisms. These three different scattering mechanisms are coulomb, phonon, and surface roughness scattering:

$$\frac{1}{\mu} = \frac{1}{\mu_{\text{c}}} + \frac{1}{\mu_{\text{ph}}} + \frac{1}{\mu_{\text{sr}}}. \quad (12)$$

The coulomb limited mobility term has been extensively studied (Jeon and Burk, 1989; Lucci *et al.*, 2003) based on the Boltzman transport equation (Fischetti and Laux, 1993). This includes scattering of electrons from both the repulsive coulomb potential due to ionized acceptor atoms and the attractive coulomb potential due to positive interfacial charge for electrons as charge carriers. The coulomb mobility model can be given as (Jeon and Burk, 1989):

$$\mu_{\text{c}} = a_1^{-1}T, \quad (13)$$

where a_1 is a parameter to be extracted (Annada Prasad Sarab and Dasgupta, 2005), T is absolute temperature.

The phonon scattering limited mobility is taken into consideration with dependency of crystallographic

orientation. It does not depend upon the fabrication process. This interface-state density dependent mobility shows the dependency on temperature. The mobility μ_{ph} can be given as (Jeon and Burk, 1989):

$$\mu_{ph} = a_2 T^{-n} E_y^{-1/y}, \quad (14)$$

where a_2 is a parameter to be extracted (Annada Prasad Sarab and Dasgupta, 2005) can be empirically derived constants.

Surface roughness scattering limited mobility constitutes a major cause of scattering at high-electron concentrations. At low-temperature and high-transverse electric fields, the surface roughness scattering strongly degrades the surface mobility and field effect mobility. As surface roughness scattering is independent of temperature, it will be same for both higher and lower temperature ranges and can be modeled for high-electric fields as (Jeon and Burk, 1989):

$$\mu_{s\gamma} = a_3^{-1} T^{-n} E_y^{-2}, \quad (15)$$

where a_3 is a parameter to be extracted (Annada Prasad Sarab and Dasgupta, 2005).

From these above models, the effective mobility model for electric field at room temperature can be obtained by putting the values of μ_c, μ_{ph}, μ_{sr} from equations (13)-(15) in equation (12):

$$\mu_{eff}(E_y) = \frac{1}{a_1/T + a_2 T^n E_y^{1/\gamma} + a_3 E_y^2}.$$

Gate leakage current

Gate insulator leakage current (direct tunneling current) increases with the scaling of the gate oxide thickness (t_{ox}). The scaling of the gate oxide thickness is crucial to enhance the performance of MOS devices. Reducing the thickness of the gate oxide increases the oxide capacitance per unit area, thereby enhancing the drain current of MOS devices (Kursun and Friedman, 2006). Continued reduction of t_{ox} makes accurate modeling of gate tunneling current an important aspect of compact FinFET device. As the minimum gate length of FinFET has been scaled into sub-50 nm range, substantial gate leakage current has been observed experimentally (Huang *et al.*, 2001). The tunneling current density at any point x within the channel is given by :

$$\mathcal{J}_g(x) \cong \mathcal{J}_o D(x) F_s(x), \quad (16)$$

where:

$$\mathcal{J}_o = \frac{q m^* k_B^2 T^2}{2\pi^2 h^3}, \quad (17)$$

$D(x)$ and $F(x)$ are transmission probability and supply function, respectively.

An analytical expression for $D(x)$ is given as ((Ben) Gu *et al.*, 2004):

$$D(x) = \exp[-B_0 f(z_g)], \quad (18)$$

where:

$$B_o = \frac{4 t_{ox}\sqrt{m_{ox} q\Phi_B}}{3h},$$

$$f(z_g) = \frac{1-(1-z_g)^{2/3}}{z_g} \text{ and } z_g = \frac{V_{ox}}{\Phi_B}.$$

After substituting the value of B_0 and $f(z_g)$ in equation (18), we obtained the expression for $D(x)$ as:

$$D(x) = \exp\left[-\frac{4 t_{ox}\sqrt{m_{ox} q\Phi_B}}{3h} \times \frac{1-(1-z_g)^{2/3}}{z_g}\right], \quad (19)$$

Where m_{ox} is the electron effective mass in SiO_2 in the tunneling direction, $q\Phi_B$ is the conduction band offset at the Si/SiO_2 interface and $V_{ox} = V_g - V_{fb} - \psi_s(x)$. V_g is the gate voltage, V_{fb} is the flat band voltage and $\psi_s(x)$ is the surface potential at point x.

The supply function ($F_s(x)$) in equation (16) is given by (Ben) Gu *et al.* (2004):

$$F_s(x) = \log\left\{\frac{1+\exp[(\Psi_s - \Phi_n - \alpha_b - \Psi_t)/\phi_1]}{1+\exp[(\Psi_s - V_{gb} - \alpha_b - \Psi_t)/\phi_t]}\right\}, \quad (20)$$

where ϕ_n is the channel voltage at point x, and $q\alpha_b$ is the difference between the conduction band edge and the electron in the FinFET body region. $\Psi_t = 0$ for $V_{ox} \geq 0$ and $\psi_t = -(V_{ox} - G_0\phi_t)$ for $V_{ox} < 0$, where G_0 is an adjustable parameter. $\psi_t(V_{ox})$ dependence we set as ((Ben) Gu *et al.*, 2004):

$$\psi_t = \frac{1}{2}\left[\sqrt{(V_{ox} + G_0\phi_t)^2 + 0.01} - (V_{ox} + G_0\phi_t)\right]. \quad (21)$$

Substituting the value of $\mathcal{J}_0$ from equation (17), $D(x)$ from equation (19), and $F_s(x)$ from equation (20) in equation (16). We obtain the final expression for the tunneling current density, $\mathcal{J}_g(x)$ as (Table I):

$$\mathcal{J}_g(x) = \left(\frac{q m^* k_B^2 T^2}{2\pi^2 h^3}\right) \times \left(\exp\left[-\frac{4 t_{ox}\sqrt{m_{ox} q\Phi_B}}{3h} \times \frac{1-(1-z_g)^{2/3}}{z_g}\right]\right) \times \left(\left\{\frac{1+\exp[(\Psi_s - \varphi_n - \alpha_b - \Psi_t)/\phi_t]}{1+\exp[(\Psi_s - V_{gb} - \alpha_b - \Psi_t)/\phi_t]}\right\}\right). \quad (22)$$

Results and discussion

In this paper, the analytical modeling for subthreshold leakage current and gate leakage current in the DG FinFET device has been carried out. For the purpose of validity of our approach, we compared our results with the reported numerical results. A close match was found which validate our analytical modeling approach for leakage current estimation in DG FinFET device.

Table I Value of extracted parameters

Parameters	Values
L_{eff}	28 nm (Choi *et al.*, 2006)
H_{fin}	35 nm (Choi *et al.*, 2006)
T_{fin}	7 nm (Choi *et al.*, 2006)
t_{ox}	1.2 nm (Choi *et al.*, 2006)
G_0	7.891 ((Ben) Gu *et al.*, 2004)

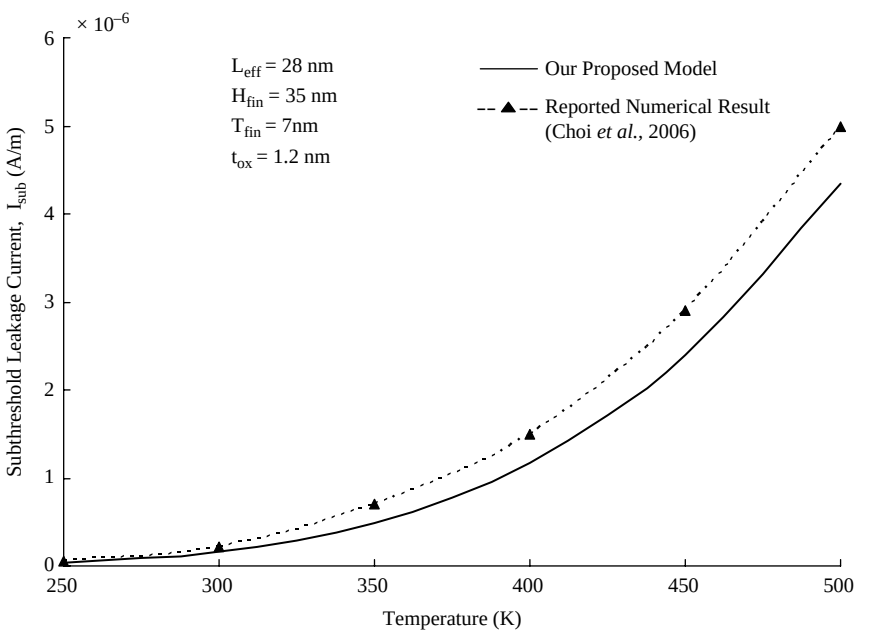
Figure 3 shows the variation of subthreshold leakage current (I_{sub}) with variation of temperature for our proposed model and reported numerical result (Choi *et al.*, 2006). The design parameter used are $L_{eff} = 28$ nm, $H_{fin} = 35$ nm, $T_{fin} = 7$ nm and $t_{ox} = 1.2$ nm. It can be seen from the figure that there is a close match between our proposed model and reported numerical model. It is known that subthreshold current and gate leakage current varying with temperature but subthreshold leakage current variation is more sensitive to temperature variation. It can be seen from the figure that subthreshold leakage current increases with increase in temperature. This is primarily because of inverse exponential function in the subthreshold current formulation given in equation (1). As the temperature increases there is a drastic rise in subthreshold leakage current at higher temperature domains. The major portion of leakage current component is through diffusion current which is primarily composed of minority carriers, whose concentration increases with increase in temperature. Because of high temperature sensitivity, subthreshold leakage current is a major component of the total static power consumption at high temperature.

Figure 4 shows the variation of direct tunneling current density with the applied gate voltage for three different values of fin thicknesses. The results has been compared and contrasted with reported numerical result (Mukhopadhyay *et al.*, 2007). A close match is found for fin thickness of 5 nm between our model and reported numerical results. The direct tunneling current is obtained from first sub-band of first valley for the potential well with in the active area of device. It is seen from the figure that the direct tunneling density is reduces to very negligible value for gate voltage of 0.6 V. This is due to the fact that the transverse direction electric field reduces drastically as the gate voltage is below 0.6 V. It is further observed that as the fin thickness is an increase there is a decrease in the direct tunneling current density. This can be attributed to lower value of quantum confinement in the transverse direction with increasing fin thickness.

The proposed analytical model is verified with reported numerical results (Mukhopadhyay *et al.*, 2007) for the purpose of validation and verification and is shown in Figure 5. The variation of direct tunneling current density with the applied gate voltage for various oxide layers thickness and its comparison with reported numerical results is shown in Figure 5. It can be seen from the figure that there is a close match between our proposed model and reported numerical model (Mukhopadhyay *et al.*, 2007). Further, it can be observed that our proposed analytical model is robust model against variation in oxide layer thickness. As the gate voltage increases the direct tunneling density increases initially in linear faction followed by non-linear faction and finally it saturates. This is because of the fact as the gate voltage increases transverse electric field also increases. There by increasing the probability of direct tunneling current.

Figure 6 shows the variation of subthreshold leakage current with absolute temperature for four effective channel lengths. It can be seen from the figure that for same temperature as the channel increases there is decrease in subthreshold leakage current. Since subthreshold currents are essential drift currents, therefore as channel length increases the longitudinal direction electric field decreases thereby decreasing the drift velocity of the of the carriers and hence the decrease in the current. At 450 K there is a decrease of 2×10^{-7} A/m for a decrease in effective channel length (L_{eff}) of 40 nm. Further the sensitivity of subthreshold leakage current for a lower channel length is more as compare to higher channel. So for the purpose of optimizing subthreshold leakage current, it is necessary to operate at higher effective channel length.

Figure 3 Variation of subthreshold leakage current (I_{sub}) with variation of absolute temperature for our proposed model and reported numerical result



Source: Choi *et al.* (2006)

Figure 4 Variation of direct tunneling current density with gate voltage for fin thickness (T_{fin}) of 5, 10, and 15 nm

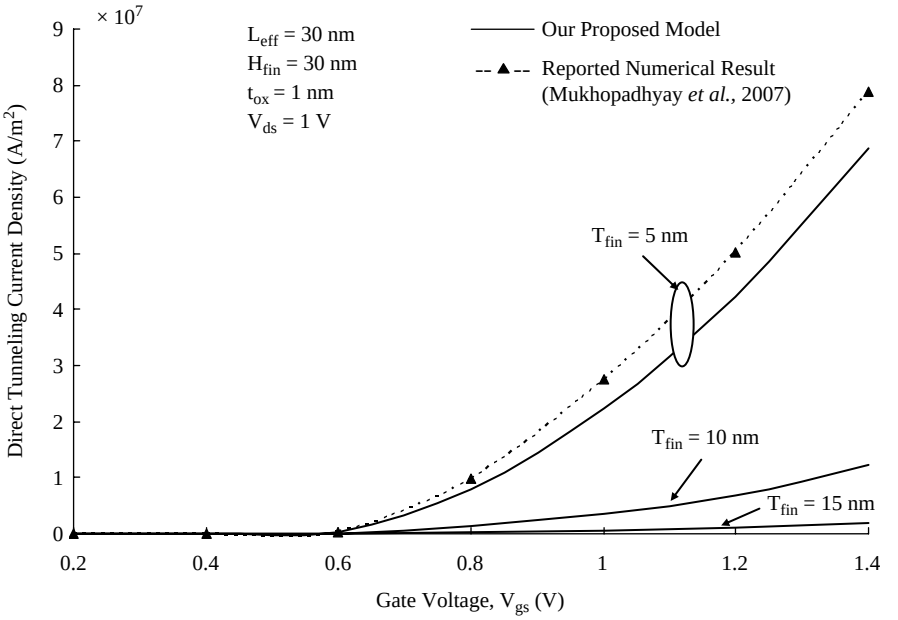
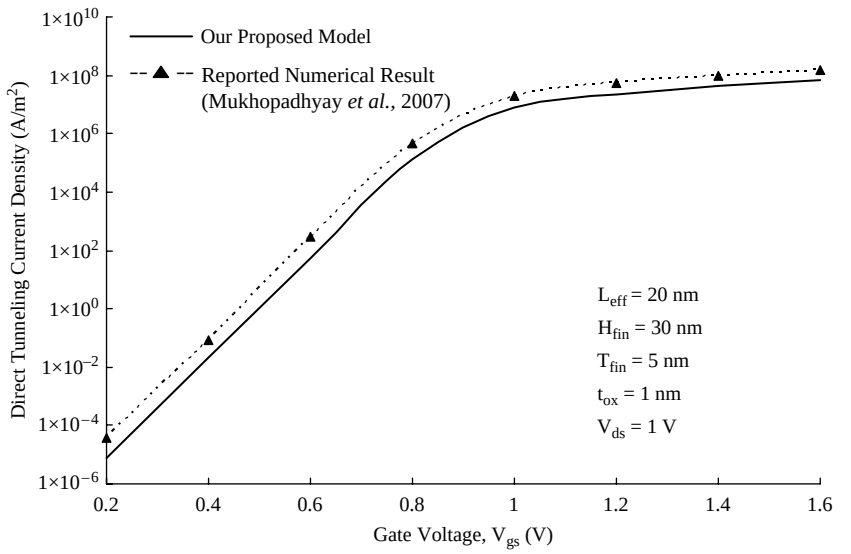


Figure 5 Variation of direct tunneling current density with gate voltage for our proposed model and reported numerical result



Source: Mukhopahyay *et al.* (2007)

Variation of subthreshold leakage current with the absolute temperature for various fin height is shown in Figure 7. For any fin height as the absolute temperature increases there is an increase in subthreshold leakage current. This can be attributed to the rise in thermal voltage and hence an increased value of minority carrier concentration which results in an enhanced in the subthreshold leakage current. Further as the fin height decreases there is a decrease in subthreshold leakage current as well. This is because of the total width of device decreases with the decrease in the value of the fin height, which results in lower subthreshold leakage current.

Figure 8 shows the variation of subthreshold leakage current with variation in absolute temperature for three values of subthreshold swing factor (S). It can be observed from the figure as the subthreshold factor increases there is increase in the subthreshold leakage current at a fixed temperature. A larger subthreshold swing factor value primarily implies a larger variation in gate voltage to change the current by one decade factor. This would primarily mean a larger effective gate voltage on drain side for FinFET structure under study. This would results larger subthreshold leakage current.

Figure 6 Variation of subthreshold leakage current (I_{sub}) with variation of absolute temperature for channel length of 20, 30, 40 and 60 nm

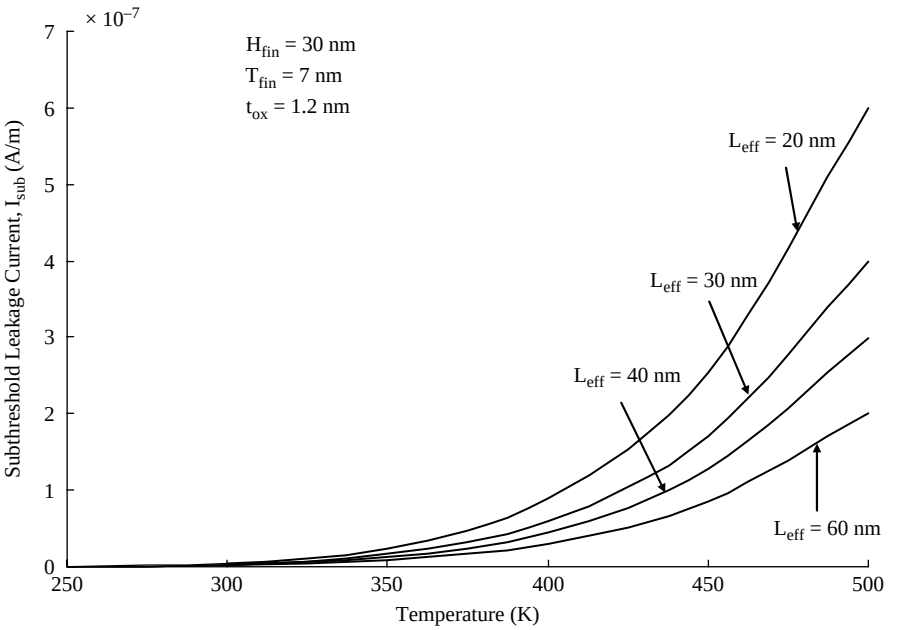
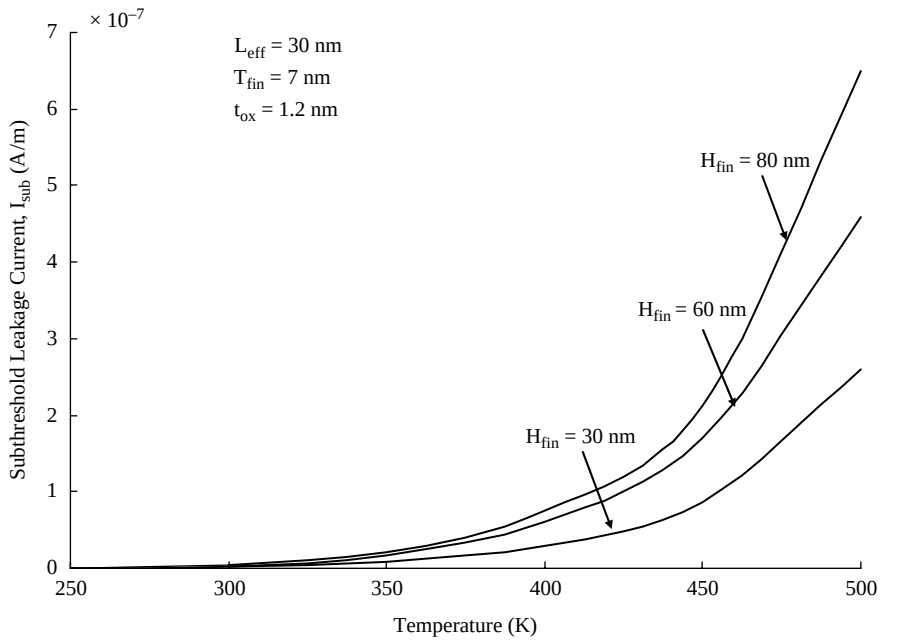


Figure 7 Variation of subthreshold leakage current (I_{sub}) with variation of absolute temperature for fin height of 20, 60 and 80 nm



Variation of direct tunneling current density with gate voltage for various oxide thicknesses is shown in Figure 9. It can be seen from the figure as the gate voltage increases there is almost exponential rise in direct tunneling current characteristics. This is because of increased value of transverse electric field through the oxide layer which increases the probability of direct tunneling current.

For the purpose of validation the results obtained on the basis of our proposed model has been compared with those obtained through reported experimental result (Yu *et al.*, 2002), for the variation of subthreshold swing factor for variation of effective channel length as shown in Figure 10. It can be seen from the figure that a close matches between the two, thus validating our approach. The variation of subthreshold swing factor with variation of channel length for various fin thickness is shown in Figure 11. It can be seen from the figure that, the minimum value of subthreshold swing factor which is asymptotically to one. Further, it can be seen from the figure that as the effective channel length reduces below 30 nm there is gradual increase in the value of subthreshold swing factor. This increase in subthreshold swing factor is primarily because of access SCEs at such

Figure 8 Variation of subthreshold leakage current (I_{sub}) with variation of absolute temperature for subthreshold swing factor of 1, 1.2 and 1.4

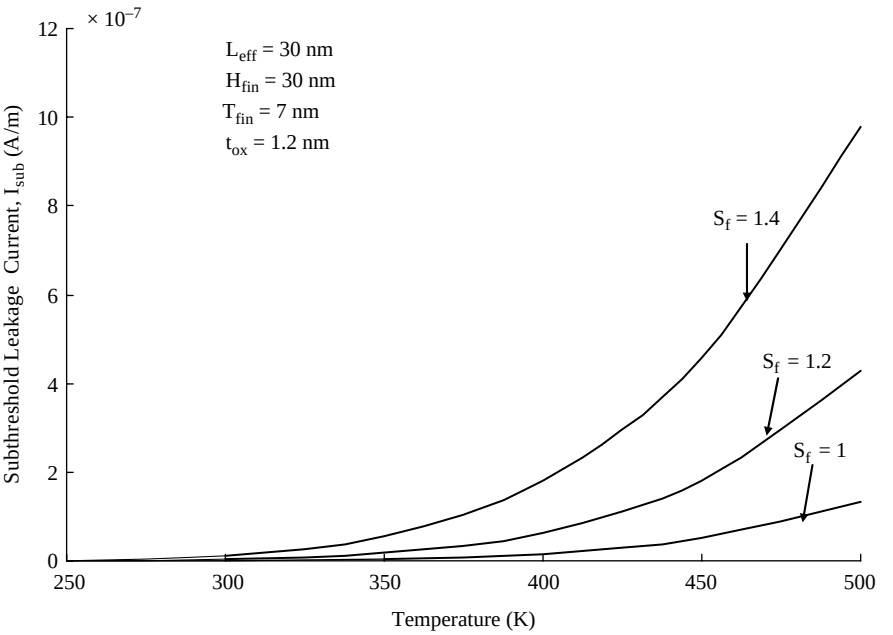
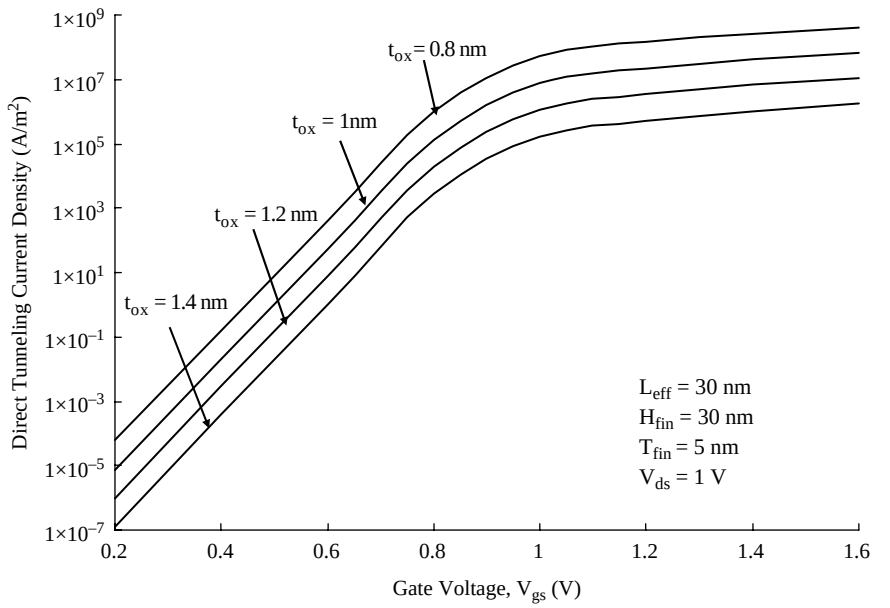


Figure 9 Variation of direct tunneling current density with gate voltage for oxide thickness (t_{ox}) of 0.8, 1, 1.2 and 1.4 nm

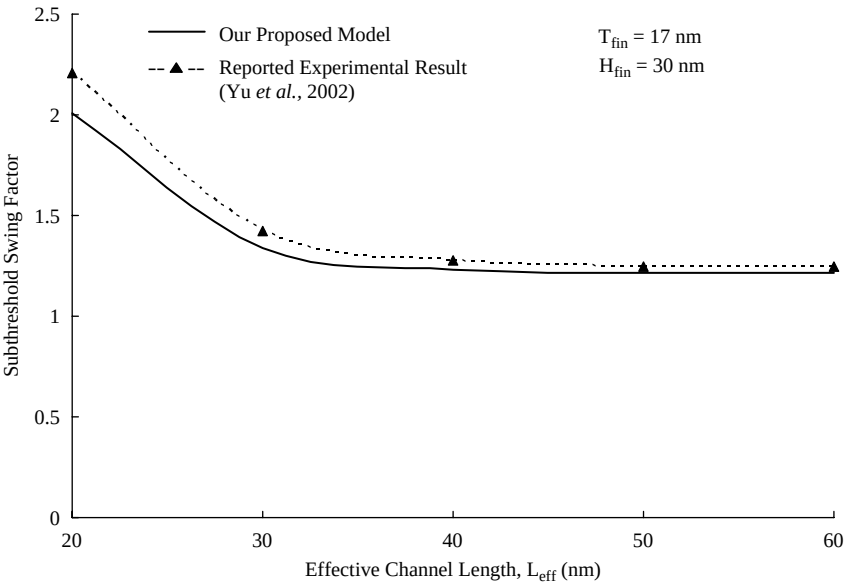


small dimensions. Further it can be observed that as the fin thickness increases there is an increase in subthreshold swing factor. This primarily due to larger cross-section area across which the channel formation has been taken place and hence a larger inversion charge requirement is needed, which results in an increased value of subthreshold swing factor.

Variation of subthreshold swing factor with fin thickness for three devices with different channel length is shown in Figure 12. It can be observed from the figure that as the fin thickness increases, there is an increase in subthreshold swing factor. As the fin thickness increases so does the area under the insulator across which the inversion charge can be founded. This requires a larger gate voltage variation in order to generate the same amount of increment/decrement of inversion charge. Further it is seen that for a shorter channel length the increase in subthreshold swing factor is more as compared to a device with larger channel length. This is due to increased SCEs for low dimension fin devices.

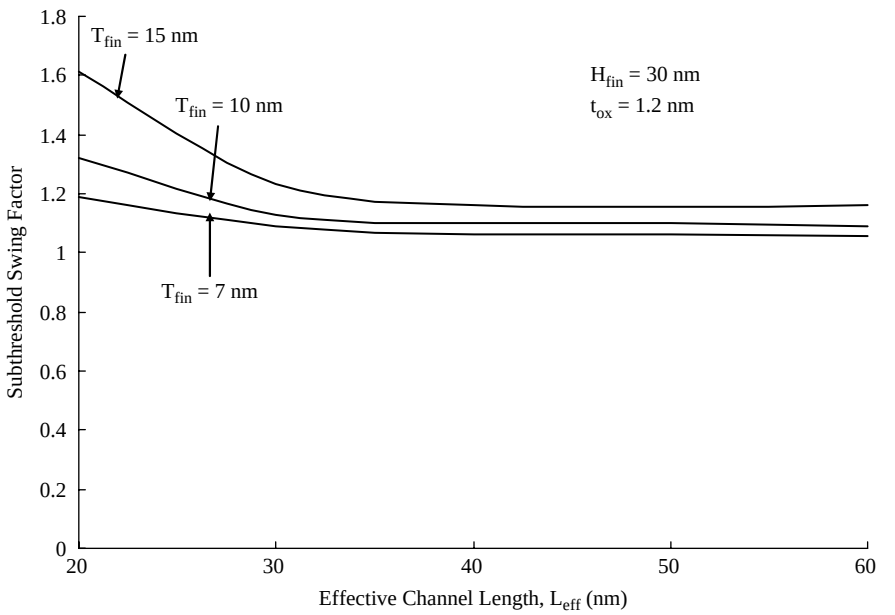
Figure 13 shows the variation of subthreshold swing factor with oxide thickness for various fin thickness. It can be seen, for any fin thickness as the oxide thickness increases so does the subthreshold swing factor. This is due to the fact that with

Figure 10 Variation of subthreshold swing factor with the variation of channel length for our proposed model and reported experimental result



Source: Yu *et al.* (2002)

Figure 11 Variation of subthreshold swing factor with the variation of channel length for fin thickness of 7, 10 and 15 nm



increasing oxide thickness an enhancement in gate voltage is required in order to generate same amount of inversion charge, which results in a larger subthreshold swing factor. Further as the oxide thickness decreases the subthreshold swing factor tries to reach its ideal value (one).

Conclusion

This paper presents the analytical modeling for estimation of leakage currents and subthreshold swing factor in DG FinFET device. We have evaluated subthreshold swing factor, subthreshold leakage current and direct tunneling current in FinFET including process parameter variations. It is seen from our study that subthreshold swing factor increases below effective gate length of 30 nm. We have considered the temperature effect variation in subthreshold leakage currents. The results obtained through our analytical model are compared with the reported numerical and experimental results. A close match between our proposed analytical model and reported results validate our approach. The study undertaken would help to design ore robust FinFET structures which are process variation tolerant and dependent less on temperature variation.

Figure 12 Variation of subthreshold swing factor with the fin thickness for channel length of 20, 30 and 40 nm

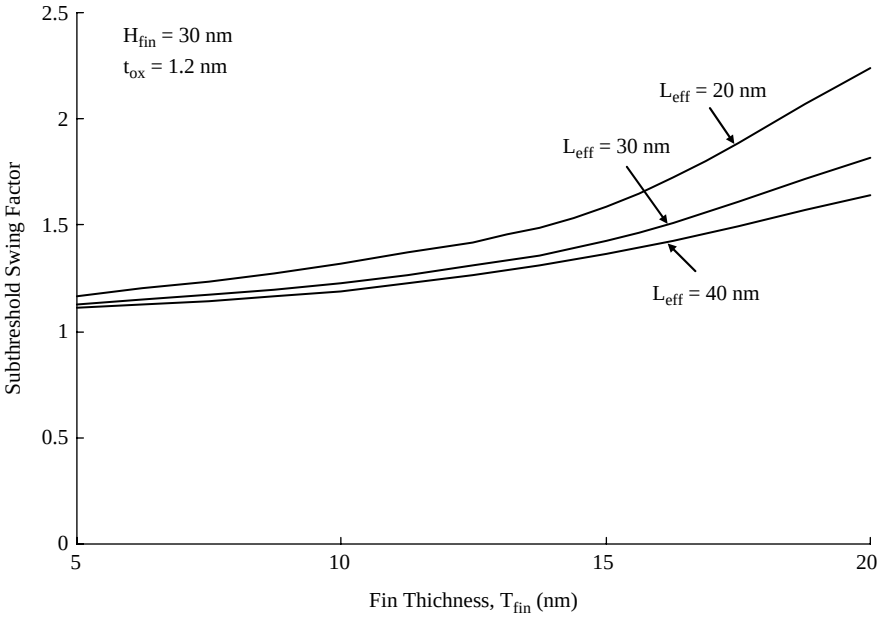
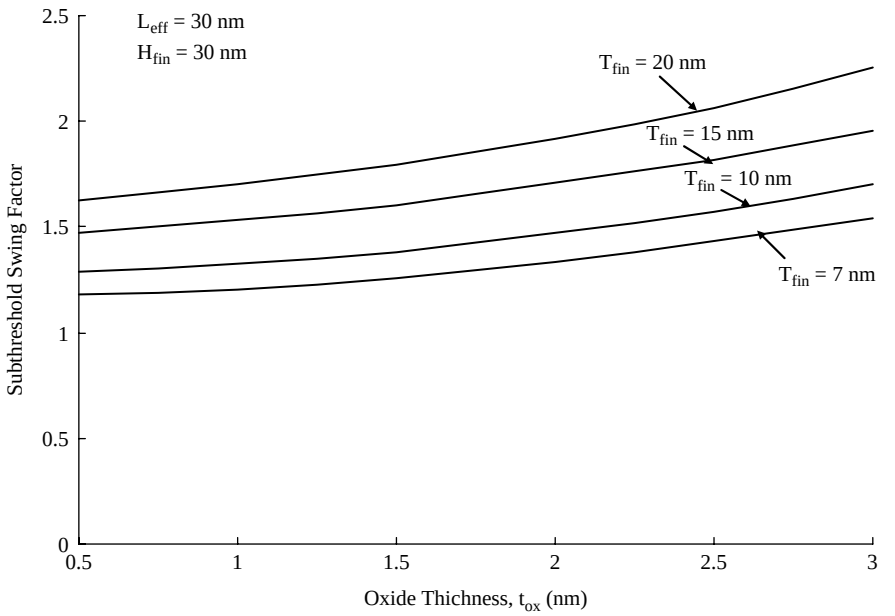


Figure 13 Variation of subthreshold swing factor with oxide thickness for fin thickness of 7, 10, 15 and 20 nm



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