

# Nanocryotron reconfigurable logic gate for superconducting nanowire single photon detector readout

Gabriel Le Guay,<sup>1</sup> Matteo Castellani,<sup>1</sup> Reed Foster,<sup>1</sup> Francesca Incalza,<sup>1</sup> Alejandro Simon,<sup>1</sup> and Karl K. Berggren<sup>1</sup>  
*Department of Electrical Engineering and Computer Science,  
Massachusetts Institute of Technology,  
77 Massachusetts Ave., Cambridge, MA 02139, USA*

(Dated: 9 December 2025)

Scaling photonic quantum-information platforms will require integrating arrays of superconducting nanowire single-photon detectors (SNSPDs) to enable low-latency feedforward control, in which optical operations are conditioned on preceding Bell-state measurements. On-chip cryogenic electronics performing coincidence or parity logic on detector outputs and accordingly driving optical modulators could improve scalability by reducing latency and room-temperature interconnects. In this work, we present a bias-programmable logic gate built from three nanocryotrons (nTrons), three-terminal superconducting devices fabricated using the same thin-film technology as SNSPDs, enabling seamless co-integration with detector arrays. By tuning the bias currents, the circuit reconfigures between AND (coincidence), XOR (odd parity), and OR operations, providing a versatile on-chip logic family. We confirm correct operation of the gate at 4.2 K with inputs from an arbitrary waveform generator, applied as sequences of three pulses with an inter-pulse delay of 200 ns. The corresponding bit-error rates was  $10^{-3}$ , with bias margins of  $\pm 11$  to  $\pm 24\%$ . Moreover, we observe operation up to 25 MHz over a narrower bias window, and we obtained bit-error rates lower than  $10^{-5}$  at 5 MHz with limited margins. We also demonstrate that the gate can perform logic functions on two SNSPD outputs in LTspice simulations. Additionally, we show that a single nTron can drive a capacitive load up to 1.2 V, possibly enabling compatibility with optical modulators in thin-film lithium niobate. The results of this proof-of-concept study demonstrate the potential of integrated nanocryotron logic for photonic applications, but its relevance extends to any other field where cryogenic signal processing can enhance system-level scalability.

## A. Introduction

Large-scale arrays of superconducting nanowire single-photon detectors (SNSPDs) have the potential to significantly advance quantum communication<sup>1</sup>, quantum computing<sup>2</sup>, imaging<sup>3</sup>, and sensing<sup>4</sup>. In particular, arrays of waveguide-integrated detectors<sup>5,6</sup> will help scale up quantum photonic platforms substantially, by enabling on-chip Bell-state measurements, a fundamental operation in many quantum protocols<sup>2?</sup>. Typically, these protocols also require feedforward control, in which photon-detection outcomes rapidly influence subsequent optical components through classical computation. Reading out arrays and performing such classical computation with room-temperature electronics requires several cryostat feedthroughs, limiting scalability and latency. Multiplexing schemes<sup>3</sup> and cryogenic processors based on cryo-CMOS<sup>7,8</sup> or rapid single-flux-quantum (RSFQ)<sup>9,10</sup> have been explored to reduce wiring in SNSPD arrays, and CMOS discrete logic elements have been used to implement feedforward control with single detectors at cryogenic temperatures<sup>11,12</sup>. However, these approaches either require additional fabrication processes, increase power dissipation, or show limited compatibility with the high impedance of nanowires, modulators, and CMOS technologies. An appealing alternative is to perform signal processing directly in the nanowire platform itself using nanocryotrons.

Nanocryotrons (nTrons) are three-terminal nanowire devices fabricated on a single thin-film superconducting layer in which an electrically coupled gate controls the switching current of the channel<sup>13</sup>. They share the fabrication process of SNSPDs, are robust to milliTesla magnetic fields<sup>14</sup>, have low-power dissipation, down to 20 aJ/pulse<sup>15</sup>, can am-

plify small signals and drive high impedances<sup>16,17</sup>, making them promising candidates for integrated cryogenic electronics. Their functionalities arise from engineering the device geometry, which in principle enables their implementation in a variety of superconducting materials used for waveguide-integrated SNSPDs, from typical polycrystalline compounds such as niobium nitride (NbN)<sup>2</sup> to amorphous materials such as molybdenum silicide (MoSi)<sup>18</sup> and tungsten silicide (WSi). As an example, multilayer heater cryotrons (hTrons), devices analogous to nTrons that operate via thermal activation<sup>19,20</sup>, have been fabricated in WSi<sup>21</sup>. Previous demonstrations have shown cryotron-based counters<sup>22</sup> and encoders<sup>23,24</sup> integrated with SNSPDs, shift-registers<sup>25</sup>, memories<sup>26?</sup>, and logic gates<sup>13,14,27</sup>. Moreover, rectifiers<sup>28</sup> and neuromorphic components<sup>29,30</sup> have been demonstrated in the same NbN nanowire platform.

Despite the wide variety of circuits proposed to date, no cryotron logic gates specifically optimized for processing SNSPD outputs have been demonstrated. In a typical Bell-state measurement setup<sup>2</sup>, a reconfigurable cryotron gate integrated with two SNSPDs would enable the selective detection of correlated and anti-correlated photon pairs through odd-parity and coincidence detection, respectively. More broadly, a single circuit capable of implementing a universal set of logic functions would allow for the realization of more complex operations, such as quantum error correction, with limited design overhead. In the cryotron gates mentioned above, certain logic functions required dedicated circuit designs, limiting flexibility, or device reset relied on external signals, potentially adding power overhead and design complexity when only combinational operations are needed. An alternative approach is to realize multiple basic logic functions (AND, OR,

NOT, MAJ) within a single cryotron (nTron or hTron) by exploiting direct input currents addition and reconfigurable biasing conditions, achieving a universal gate set<sup>31</sup>.

In this work, we present a fully reconfigurable nanocryotron logic gate that unifies three operations, AND, OR, and XOR, within the same circuit, without any change in layout or wiring. It builds on the concepts of the bias-programmable cryotron gate described above, but introduces additional nanocryotrons to amplify detector signals and directly implement XOR operations, which facilitates correlated Bell-state detection. Moreover, it operates using short current pulses comparable to SNSPD outputs, and it self-resets after each operation. The circuit is fabricated on a 10 nm thick NbN film also incorporates integrated gold resistors that enable self-resetting nTrons, ensuring controlled current diversion to the loads while eliminating parasitic circulating currents in the interconnects. The NOT operation can be implemented by supplying pulses to one input of the XOR gate, phase-aligned with the other input, enabling a universal combinational logic family with a single device. We show through LTspice simulations that the gate can perform XOR and AND operations on two SNSPD's output pulses to detect correlated and anti-correlated pairs, respectively. Additionally, we demonstrate nTrons can reach voltage levels comparable to lithium niobate electro-optic modulators, highlighting their potential for seamless integration with quantum photonic platforms and full implementation of on-chip feedforward control.

## B. Working principle

The topology of the reconfigurable gate is shown in Fig. 1. In this circuit, the two side nTrons ( $nT_1$  and  $nT_2$ ) switch when they receive independent input pulses (IN 1 and IN 2), redirecting part of their bias current ( $I_{b1}$  and  $I_{b2}$ ) toward the gate of the central nTron ( $nT_3$ ). In particular, the bias current is split between the  $nT_3$  gate, the other side nTron branch, and the shunt resistor ( $R_{sh}$ ), which ensures the two side nTrons always reset to the superconducting states without latching. Kinetic inductors ( $L_1$ ) were added to reduce the current flowing through the other branch ( $i_1$  and  $i_2$ ). The resulting output currents from  $nT_1$  and  $nT_2$  are denoted  $i_1$  and  $i_2$ , respectively, and the total current driving  $nT_3$  is  $i_3 = i_1 + i_2$ , as illustrated schematically in Fig. 1(a). The circuit can be reconfigured to perform XOR, AND, and OR logic operations by tuning the bias currents  $I_{b1}$  and  $I_{b2}$ . Figure 1(b) depicts the temporal evolution of the gate input pulses from LTspice simulations, showing the internal currents  $i_1$ ,  $i_2$ , and  $i_3$  as well, and the corresponding output voltage  $v_{out}$  for the XOR and AND configurations (OR operation shown in the supplementary material section 3). The double-spike structure observed in the simulated currents  $i_1$ ,  $i_2$ , and  $i_3$  can be understood from the dynamics of the inductor current and the gate current : when the two side nTrons switch, their bias currents are first diverted into the central branch, producing the initial peak in  $i_1$  and  $i_3$ . When the central nTron subsequently switches, the current stored in the inductor is released back into the circuit, leading to the second rise and the slow decay of these signals.

In the XOR configuration, the side nTrons ( $nT_1$  and  $nT_2$ ) are biased symmetrically near their switching currents but with opposite polarity ( $+I_b$  and  $-I_b$ ).  $I_b$  is the bias current sufficient to make  $nT_3$  fire when one of  $nT_1$  or  $nT_2$  fires. The central nTron ( $nT_3$ ) is biased close to its switching threshold. When a pulse is applied to either  $nT_1$  or  $nT_2$ , the high bias  $+I_b$  is diverted, causing  $nT_3$  to switch and generate an output pulse. However, when simultaneous pulses are applied to both  $nT_1$  and  $nT_2$ , the opposite bias contributions cancel out ( $i_1 + i_2 \approx 0$ ), preventing  $nT_3$  from switching. As a result, an output pulse is produced only for the input combinations (1,0) and (0,1), where 1 denotes the presence of a pulse and 0 its absence, implementing the XOR logic operation. To ensure stable operation under repeated XOR cycling, resistors  $R_1$  are inserted to provide a resistive path for current relaxation, thereby avoiding the buildup of circulating currents in the loop.

In the AND configuration, both side nTrons are biased symmetrically at an intermediate bias current  $I_{bAND}$ , where  $I_{b1} = I_{b2} = I_{bAND}$  and  $I_b/2 < I_{bAND} < I_b$ . When a single input pulse arrives, the smaller bias of the AND configuration, redirected to  $nT_3$ , is insufficient to trigger switching, and no output pulse is generated. When both inputs fire simultaneously, the two contributions add constructively, giving  $i_3 = i_1 + i_2 \approx 2I_{bAND}$ , which exceeds the switching threshold of  $nT_3$  and produces an output pulse. Consequently, the circuit generates an output only for the (1,1) input state, thereby realizing AND logic.

In the OR configuration, both side nTrons are biased positively at  $+I_b$ . A pulse on either input diverts enough current through the coupling branch to raise  $i_3$  above the switching threshold of  $nT_3$ , resulting in an output pulse. When both inputs fire simultaneously, the bias contributions add, and  $nT_3$  still switches normally. Consequently, output pulses appear for the input combinations (1,0), (0,1), and (1,1), implementing OR logic. The same underlying current redistribution dynamics among  $i_1$ ,  $i_2$ , and  $i_3$  therefore govern all three configurations, with the specific logic function determined by the applied biasing conditions. The NOT gate could be operated by biasing the device in the XOR configuration and fixing one of the inputs, so that the circuit effectively inverts the remaining input. Although we did not demonstrate this operation experimentally.

## C. Methods

We determined the target circuit parameters of the device designs in LTspice simulations, using the electro-thermal model of an nTron<sup>32,33</sup>. Integrated resistors were patterned through direct-write photolithography and lift-off on a 20 nm thick metal film (5 nm of titanium and 15 nm of gold), deposited through electron-beam evaporation on a 300 nm SiO<sub>2</sub>/Si substrate<sup>33</sup>. A 10 nm thick film of niobium nitride (NbN) was sputtered on the SiO<sub>2</sub> substrate and the patterned resistors, to ensure good electrical contact between the two layers. The superconducting components (nTrons, inductors, and interconnects) were patterned on the NbN layer through

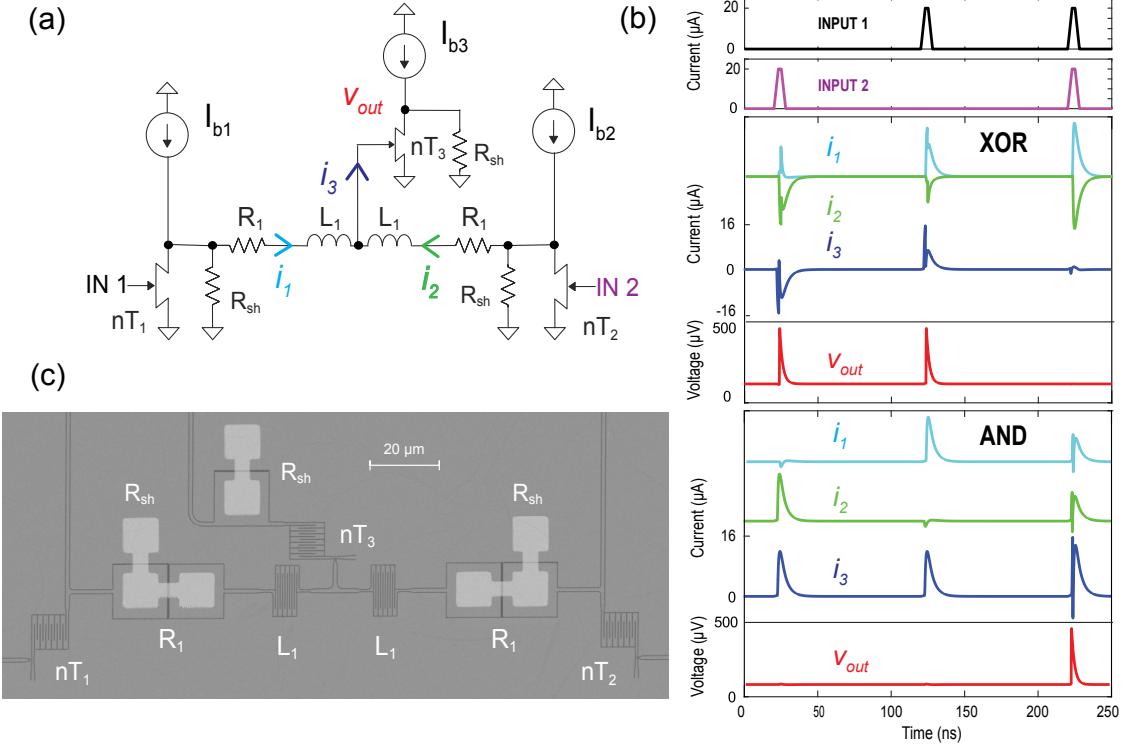


FIG. 1. (a) Schematic of the reconfigurable three-nTron logic gate. The two lateral devices ( $nT_1$  and  $nT_2$ ) receive independent input pulses, while the central nTron ( $nT_3$ ) produces the output. The bias currents  $I_{b1}$  and  $I_{b2}$  set the operating configuration (XOR, AND, or OR). For simplicity and compactness, the 8 nH series inductors connected above each nTron are not shown. The other kinetic inductors  $L_1$  have values of 10 nH. The series resistors  $R_1$  are 10 Ω, while the shunt resistors  $R_{shunt}$  are 5 Ω. (b) Time-domain representation of the gate dynamics for the XOR and AND configurations. The plots show the input pulses applied to the gates of  $nT_1$  and  $nT_2$ , the corresponding internal currents  $i_1$  and  $i_2$ , their sum  $i_3$ , and the output voltage  $V_{out}$ . For visual clarity and compactness, the current traces  $i_1$  and  $i_2$  are vertically shifted along the current axis in both the XOR and AND panels. (c) Scanning electron micrograph (SEM) of the fabricated three-nTron circuit. The image shows the layout of the lateral nTrons ( $nT_1$ ,  $nT_2$ ), the central device ( $nT_3$ ), and the bias and output connections. The meandered nanowire sections visible in the image act as kinetic inductors. The gray regions correspond to the niobium nitride (NbN) film, while the dark edges of the traces reveal the underlying SiO<sub>2</sub> substrate. A continuous ground plane surrounds all the circuit traces.

electron-beam lithography and reactive ion etching. Inductors were implemented as meandered nanowires (600 nm of wire width) with a theoretically estimated kinetic inductance of  $\sim 40$  pH/sq, yielding values of  $L_d = 8$  nH, a sheet resistance of  $60 \Omega/\square$  and  $L_1 = 10$  nH. The typical critical temperature of such films is  $T_c \approx 8.5$  K (not extracted for this particular sample). The nTrons featured a 43 nm wide choke and a 334 nm wide channel. The circuits were patterned on a 1 cm × 1 cm chip, and each circuit occupied an area of approximately  $80 \times 200 \mu\text{m}^2$ . All circuits were obtained from a single fabrication run and operated successfully on the first cooldown, without requiring design iterations or post-fabrication tuning.

The devices were mounted on a printed circuit board (PCB) using GE varnish, and electrical contact to the device pads was provided by aluminum wire bonds. Measurements were performed in a liquid-helium dewar with a custom-built cryogenic probe<sup>34</sup> at 4.2 K. 5 ns wide input current pulses applied to the devices were generated by an arbitrary waveform generator (AWG). On the PCB at 4.2 K, each bias line from the

low-noise voltage sources was connected through a 10 kΩ series resistor to the circuit input, with a 50 Ω resistor in parallel to the input node to match the coaxial cable impedance. The readout chain consisted of a bias tee with DC port capped, a fixed attenuator (3 dB), and two low-noise amplifiers in series (each 25 dB gain and 2.5 GHz bandwidth), followed by a real-time 6 GHz bandwidth oscilloscope.

#### D. Results

We experimentally verified that the device correctly implements reconfigurable logic operations. Figure 2(a) shows the time-domain output traces for the same circuit configured as an AND, XOR, and OR gate. In this figure, the input traces correspond to the AND measurement, while the XOR and OR outputs are shown together to illustrate correct logic and reconfigurable operation. The logic behavior is confirmed.

To further analyze the circuit dynamics, we investigated the role of the inter-arrival time of the input pulses. For the (1,1)

operation, AND and XOR rely on coincident input pulses. This timing dependence is particularly relevant for coincidence detection with SNSPDs, where simultaneous photon arrivals encode multi-photon correlations or Bell-state projections. In such applications, the logic gate must discriminate between coincident (AND Gate) and non-coincident (XOR Gate) detection events. The success probability was evaluated as a function of the relative delay between the two input pulses, normalized such that 1 corresponds to error-free operation over 1000 trials and 0 corresponds to all-error operation. As shown in Fig. 2(b), both gates exhibit a sharp decrease in success rate when the delay exceeds a few nanoseconds. To control the relative timing, the frequency of the input pulses was slightly detuned between the two channels to allow for measurement of operation with sub-nanosecond phase increments.

A notable difference is the width of the correct operation window: the AND gate maintains functionality over  $\sim 9$  ns at 50%, whereas the XOR window is narrower,  $\sim 5$  ns. This behavior is consistent with our simulations and can be attributed to the asymmetric shape of the nTron output pulses; the rising edge is much faster than the falling edge. In the AND configuration, the rising edge of the pulse from one input nTron (e.g.,  $i_1$ ) can overlap with the long falling edge of the other ( $i_2$ ) in Fig. 1, allowing the combined current  $i_3$  to exceed the switching threshold of nT<sub>3</sub> even for larger inter-arrival delays. However in the XOR configuration, correct operation relies on the cancellation of coincident peaks. Because the rising edge is much faster than the falling edge, the second pulse must arrive very close to the rising edge of the first to cancel it in time, making the XOR gate more sensitive to timing mismatch and resulting in a narrower operation window.

Following the timing analysis, the reliability of the reconfigurable gate was quantified by measuring the bit-error rate (BER) as a function of the two side-nTron bias currents ( $I_{b1}$ ,  $I_{b2}$ ). For each logic configuration, 1000 operations were executed, and the BER, ranging from  $10^{-3}$  to 1, was computed across the full two-dimensional bias space (Fig. 3a). The OR gates exhibit a square-symmetric window of correct operation, while the AND gate displays an L-shaped region, consistent with its requirement that both input currents contribute simultaneously to switch the central nTron. However, in the XOR configuration, the window of correct operation is rectangular, indicating a slight asymmetry between the left and right halves of the circuit. This asymmetry likely arises from two factors: (1) in the XOR configuration, the application of a positive input to the gate of the negatively biased nTron (nTron<sub>2</sub>) and a positive input to the positively biased nTron (nTron<sub>1</sub>); and (2) device-level variations such as differences in choke width, kinetic inductance, or resistance, potentially linked to the small notch observed on the right resistor R<sub>1</sub> in the SEM of Fig. 1(c).

When one branch is strongly biased, it can partially compensate for a weaker bias on the other, leading to the characteristic asymmetry of the AND mode. In contrast, the OR and XOR responses produce the expected square-shaped operation windows.

From these data, we extract the fractional bias margins, defined as the half-width of the valid bias window normal-

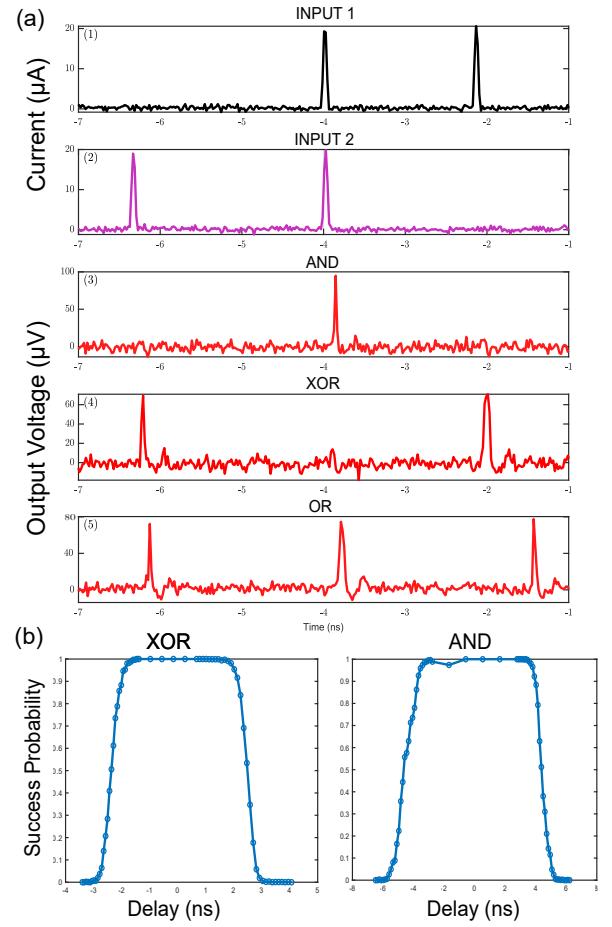


FIG. 2. Reconfigurable logic operation and timing dependence at 4.2K. (a) Time-domain output traces for the reconfigurable nTron logic gate configured as AND ( $I_{b1,2}=60\mu\text{A}$ ), XOR ( $I_{b1}=86\mu\text{A}$  and  $I_{b2}=-96\mu\text{A}$ ), and OR operations ( $I_{b1,2}=100\mu\text{A}$ ). The two input traces shown in insets 1 and 2 correspond to the signals used during the AND-gate measurement. For the XOR and OR operations, the input pulses (not shown) had slightly different relative phases, leading to different timing in output pulses between the three gate operations. The output responses for AND, XOR, and OR are shown in Insets I, II, and III, respectively. (b) Success probability as a function of the relative delay between the two input pulses for the AND and XOR Gate. The delay dependence is relevant only for them, since in the OR mode each input pulse independently generates an output.

ized to its center value. At a BER threshold of  $10^{-3}$  and 4.2 K, the XOR configuration operates for  $I_{b1} = 75\text{--}100 \mu\text{A}$  and  $I_{b2} = (-105)\text{--}(-80) \mu\text{A}$ , corresponding to  $\pm 14.3\%$  and  $\pm 13.5\%$  margins, respectively. The AND mode, with valid ranges  $I_{b1} = 55\text{--}75 \mu\text{A}$  and  $I_{b2} = 50\text{--}70 \mu\text{A}$ , yields  $\pm 15.4\%$  and  $\pm 16.0\%$  margins. Because the operating region forms an L-shaped contour in the  $(I_{b1}, I_{b2})$  map, the effective area of correct operation is larger than suggested by the individual bias margins. The OR gate exhibits the broadest window,  $I_{b1} = 70\text{--}115 \mu\text{A}$  and  $I_{b2} = 75\text{--}115 \mu\text{A}$ , corresponding to  $\pm 24.3\%$  and  $\pm 21.1\%$ . These results indicate that the OR mode is most tolerant to bias variation, whereas the AND and

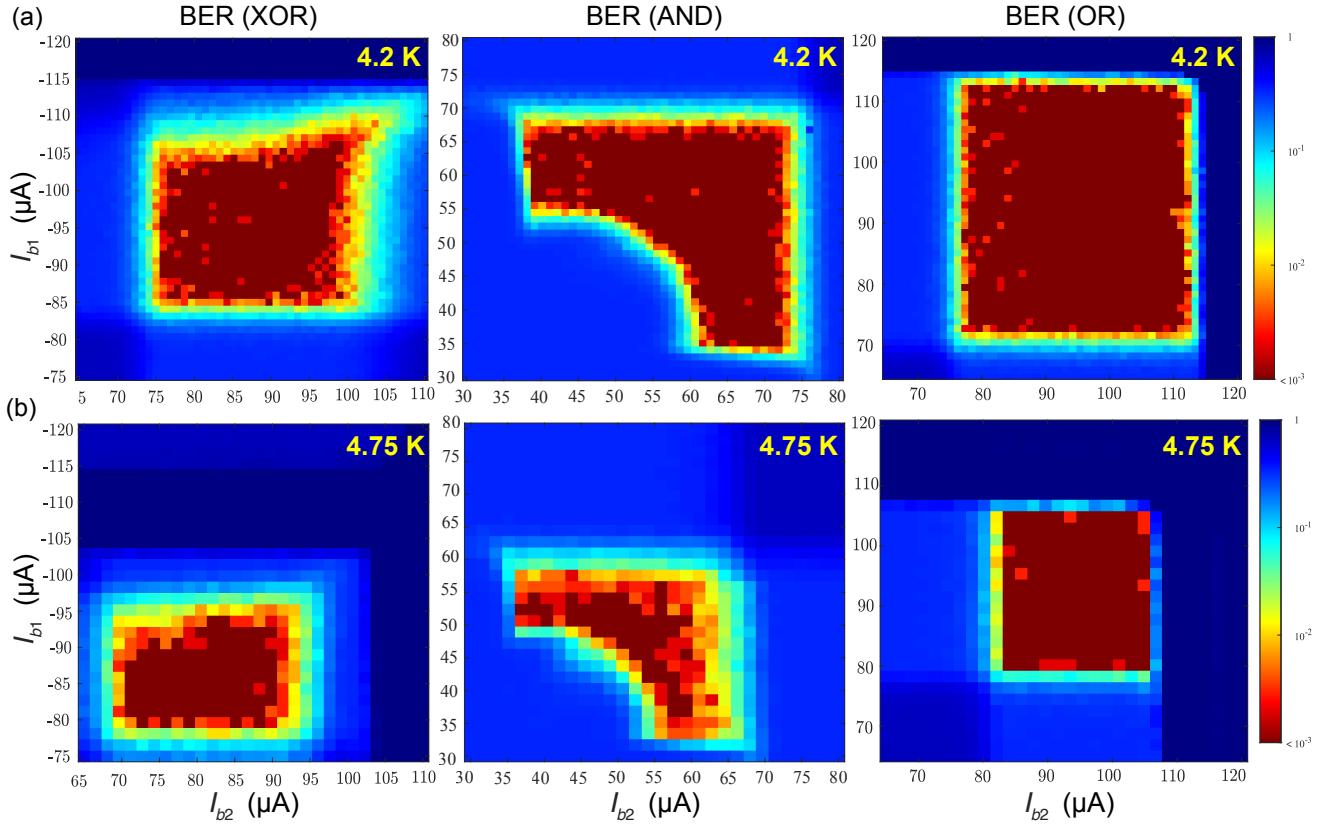


FIG. 3. Bit-error-rate (BER) maps for the XOR, AND, and OR configurations measured at 5 MHz and two temperatures. (a) Results at 4.2 K and (b) at 4.75 K. The BER is plotted as a function of the two side nTron bias currents ( $I_{b1}, I_{b2}$ ), with red regions indicating correct operation over  $10^3$  logic trials.

XOR modes require tighter bias control.

Although the present characterization uses electrical input pulses, the intended application of this reconfigurable gate is to be driven directly by superconducting nanowire single-photon detectors (SNSPDs). In such architectures, each logic input corresponds to a photon-detection event, and the logic stage therefore forms part of the front-end readout for detector arrays or feedforward quantum-photonic circuits. The lowest measured bit-error rate of approximately  $10^{-3}$  with high margins is already sufficient for practical operation in these detector-driven systems. In typical SNSPD arrays, the detectors themselves operate with detection efficiencies of 90–99% and intrinsic timing jitter on the order of tens of picoseconds<sup>35,36</sup>. Within this context, an additional logic-stage error probability  $<10^{-3}$  per event contributes negligibly to the overall system fidelity.

To assess the robustness of the bias margins with respect to temperature, we repeated the measurements at an elevated temperature of 4.75 K. The operation regions shift to lower absolute bias and become narrower, as shown in Fig. 3b. For the XOR mode, the valid range contracts to  $I_{b1} = 70$ –95  $\mu\text{A}$  and  $I_{b2} = (-95)$ –(-77)  $\mu\text{A}$ , corresponding to fractional margins of  $\pm 15.6\%$  and  $\pm 10.3\%$ . The AND mode window becomes  $I_{b1} = 50$ –63  $\mu\text{A}$  and  $I_{b2} = 45$ –60  $\mu\text{A}$ , with fractional

margins of  $\pm 11.5\%$  and  $\pm 14.3\%$ . The OR gate remains functional over  $I_{b1} = 82$ –106  $\mu\text{A}$  and  $I_{b2} = 80$ –106  $\mu\text{A}$ , but its margins decrease to  $\pm 13.2\%$  and  $\pm 13.5\%$ . Overall, the contraction observed with increasing temperature is consistent with reduced critical current and smaller thermal margins. All three modes remain bias-tunable and operational; AND and XOR retain reduced yet comparable margins, whereas the OR window shrinks most due to its higher-side biases and the additive (1,1) drive pushing the central nTron closer to its switching threshold.

As the input frequency increases from 15 MHz to 25 MHz, the operation windows of the device become noticeably narrower and the overall bit-error rate (BER) rises. This degradation is attributed to the reduced electrical recovery time between successive pulses. In particular, the finite  $L/R$  time constant, set by inductors and shunts of the circuit, slows down the nTron reset within each cycle, increasing the error probability. A frequency-induced bias asymmetry emerges in the AND and XOR configurations, where the low-BER region along  $I_{b1}$  becomes narrower than that along  $I_{b2}$ . In the XOR mode, this asymmetry likely stems from the opposite polarity between the bias and input pulse on the  $I_{b2}$  branch (negative bias with positive pulse), while both are positive on the  $I_{b1}$  side, affecting local switching dynamics and thermal re-

set. In contrast, the OR gate preserves a largely symmetric response but shows a uniform BER increase with frequency. The corresponding BER maps and frequency-dependent plots for 15 MHz and 25 MHz operation are provided in Supplementary Material, Section 2.

### Power consumption

To quantitatively assess the power consumption of the circuit, we performed a detailed power analysis using LTspice simulations under the same operating conditions as the experimental measurements. The AND, OR, and XOR configurations all exhibit highly consistent energy characteristics, with per-operation energies in the range of 7.4–7.6 fJ for an input pulse duration of approximately 7.7 ns. The average instantaneous power per operation is approximately 1  $\mu$ W, confirming that the circuit remains in a low-power regime even during active switching.

The three logic configurations present comparable results: the XOR mode shows slightly higher energy consumption (by about 2–3%) compared to the AND mode, while the OR mode yields a mean per-operation energy of 7.6 fJ, corresponding to an average power of 0.99  $\mu$ W. Overall, the results demonstrate that the energy efficiency and balance between input channels are well maintained across logic functions and bias conditions. Our values lie in the few-femtojoule regime previously reported for nTron logic<sup>14</sup>. They are also consistent with the ripple counter of Castellani *et al.*, which reports higher energy than JJ/RSFQ logic as the trade-off for native compatibility with high-impedance SNSPD and standard CMOS loads<sup>22</sup>. We note that these energy and power values refer only to the simulated on-chip gate and do not include off-chip components such as the 10 k $\Omega$  PCB bias resistors.

The bias-reconfigurable nTron gate operates at multi-MHz rates with an estimated energy dissipation of  $\sim 7 \times 10^{-15}$  J per operation in electrical mode. These values place it behind conventional RSFQ and AQFP logic: RSFQ circuits typically dissipate  $10^{-19}$ – $10^{-18}$  J per junction but require continuous DC biasing and complex distribution networks, while AQFP achieves energies below  $10^{-20}$  J at the expense of GHz clock rates<sup>37,38</sup>. Cryo-CMOS implementations, by contrast, reach  $\sim 10^{-15}$ – $10^{-14}$  J per switching event but are generally implemented in semiconductor processes that are challenging to monolithically co-fabricate with superconducting nanowires. Within this context, the nTron gate offers reasonably low energy per operation and tens-of-MHz operating speeds, even if it does not match the ultimate power-delay performance of SFQ or cryo-CMOS logic. Its main advantage lies in its fabrication simplicity and ability to share a common nanowire process with SNSPDs, enabling straightforward monolithic integration and compact detector–logic co-design.

### Integration with SNSPDs for Quantum Applications

Integrating SNSPDs with superconducting logic allows detected photon events to be processed directly on chip without

external amplification. Our goal is to demonstrate that the reconfigurable nanocryotron gate can interface with SNSPD outputs and perform logic operations under realistic detector conditions. In a typical setup for correlated or anti-correlated photon pair detection in Bell-state measurements, SNSPDs would be placed after the two output ports of optical splitters, and bouncing or coincidence counts would be recorded<sup>2</sup>. Assuming no photons are lost and no unwanted photons are introduced in this process, AND and XOR operations between the two detector’s outputs are sufficient to recognize anti-correlated and correlated pairs, respectively. Figure 4 shows the proposed integration scheme in which two SNSPDs ( $\text{SNSPD}_1$  and  $\text{SNSPD}_2$ ) directly provide input signals to  $nT_1$  and  $nT_2$  in the reconfigurable nanocryotron gate. We simulated this scheme in LTspice, where photon events were mimicked by dynamically lowering the critical current of each detector below its bias point<sup>32</sup>, through control pulses shown in the first two panels of Figure 4(b). In this simulation, we modeled a 10 nm-thick NbN layer—identical to that used in the reconfigurable gate and an SNSPD with a switching current of 22  $\mu$ A. As illustrated in panel (b), the simulated traces reproduce the expected Boolean behavior: in XOR mode, an output pulse is generated when only one SNSPD fires, but not when both detectors fire simultaneously; conversely, in AND mode, the output appears only when both inputs fire together.

These simulations confirm that the same physical circuit can reliably switch between XOR and AND operation through simple bias adjustment. Beyond reducing interconnect complexity in SNSPD arrays, this reconfigurability provides a native XOR primitive directly compatible with superconducting nanowire technology. Such functionality is particularly relevant for quantum photonic protocols, where XOR enables conditional feedforward operations and underpins Bell-state measurements essential for entanglement-based and measurement-driven architectures. In particular, the XOR configuration could be used to detect correlated Bell states, where two photons would be simultaneously detected by a single detector ( $\text{SNSPD}_1$  or  $\text{SNSPD}_2$ ). The AND configuration would detect anti-correlated states, where both detectors would fire simultaneously. Overall, the proposed gate serves as a compact cryogenic logic element and a versatile building block for scalable quantum photonic systems.

Deterministic and low-latency electrical control of optical modulators, conditional on previous photon-state detection events and logic operations, is a critical requirement for quantum feedforward protocols. Realizing a fully-integrated cryogenic circuit for this task requires logic circuits that can easily drive electro-optic modulators up to their control voltage levels. To evaluate this capability in our technology, we fabricated a wide-channel nTron (1.5  $\mu$ m channel and 200 nm choke), which could be interposed between the logic gate and the modulator as an amplifier. In our configuration the logic-gate output current is only  $\sim 1.5 \mu$ A, which is below the amplifier gate’s critical current, so the device could be further optimized to deliver a larger output current. We tested the nTron’s ability to drive a capacitive load at cryogenic temperatures<sup>16,39</sup>, where the load was a 1 pF surface-mount capacitor that approximately mimicked the impedance of a

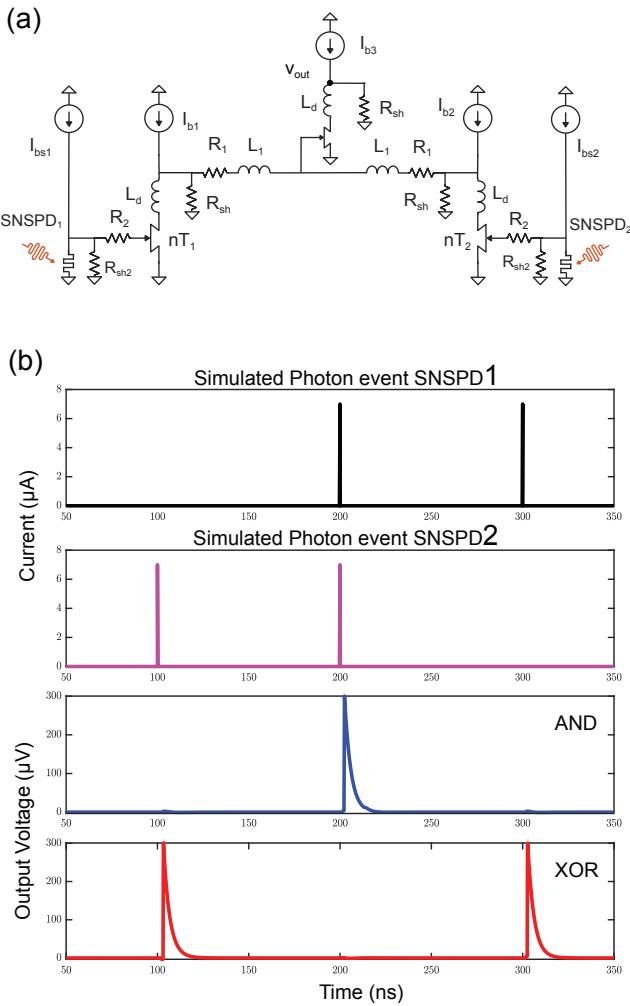


FIG. 4. (a) Circuit schematic of the reconfigurable logic gate driven by two SNSPD inputs. All nTrons have the same channel and choke dimensions as in the previous device, and are modeled using electrical models of nTrons and SNSPDs. The shunt resistor values are  $R_{shunt2} = 3 \Omega$  and  $R_2 = 5 \Omega$ . The SNSPDs are biased at  $+22 \mu\text{A}$  and  $-22 \mu\text{A}$  ( $I_{bs1}$  and  $I_{bs2}$ , respectively). (b) Simulation traces of the reconfigurable gate driven by SNSPD inputs. The first two panels correspond to the electronic current pulses applied in the simulation, which transiently lower the critical current of each SNSPD model and induce switching. The third panel shows the resulting output voltage when the gate operates in the AND configuration, while the fourth panel shows the output voltage in the XOR configuration.

gate-controlled electro-optic modulator. The device successfully charged the capacitor up to 1.2 V at a repetition rate of 200 kHz in a liquid-helium dewar at 4.2 K (see supplementary material). These results suggest that the nTron can deliver sufficient voltage to actuate cryogenic electro-optic or CMOS-compatible elements, establishing it as a viable driver for implementing quantum feedforward. Additional details are provided in Supplementary Material Section 5. We believe the relatively low 200 kHz operation rate is mainly limited by the nTron's thermal recovery time and the electrical time constants of the output circuit, which prevent the device

from fully cooling down before the next pulse. To increase speed, one could reduce parasitic inductance and resistance, improve thermal anchoring by adjusting the fabrication process and combining suitable materials, optimize film geometry for faster cooling, enabling higher repetition rates without compromising the output voltage.

## E. Discussion

Our results demonstrate that a three-nanocryotron (nTron) circuit can be bias-reconfigured to realize AND, OR, and XOR logic with bit-error rates below  $10^{-3}$  with large margins at cryogenic temperatures, addressing the long-standing need for simple, on-chip logic compatible with SNSPD technology. Compared with RSFQ or cryo-CMOS approaches, which can reduce wire count but at the cost of added process complexity or impedance mismatch, the nTron shares materials and fabrication with SNSPDs and can directly drive high impedances, simplifying co-integration.

The measured BER values down to  $10^{-3}$  already satisfy the fidelity requirements for SNSPD-based logic, where detector efficiency (90–98%) and photon statistics dominate overall system errors. Further optimization of the bias point can reduce the BER below  $10^{-5}$ , but this improvement is largely redundant for practical feedforward or coincidence-detection architectures. The corresponding bias margins of 10–25% demonstrate that reliable operation can be maintained without active feedback or bias stabilization.

The asymmetries observed in the XOR mode at higher frequencies are likely due to bias-polarity asymmetry between  $nT_{Tron1}$  and  $nT_{Tron2}$  and small device-level variations, and could be reduced with more symmetric designs and tighter fabrication control.

Measurements at 4.2 and 4.75 K indicate robust operation over this temperature range, with bias windows contracting by approximately  $\pm 30$ –50% as the thermal margin decreases. This trend reflects the reduction of the device's critical current with temperature and is mode dependent: AND and XOR preserve broadly similar relative margins at elevated  $T$ , while OR is most sensitive. In the OR regime, comparatively high side biases are chosen so that either input alone can switch the central nTron, and the two contributions add under the (1, 1) input; as  $I_c$  falls with temperature, the effective drive sits closer to threshold over a larger portion of the bias plane, making OR more susceptible to small thermal and bias fluctuations and thus compressing its valid region. Despite this contraction, all three modes remain bias-tunable and functional within the cryogenic range relevant to SNSPD systems.

The extracted energy dissipation of approximately  $7 \times 10^{-15} \text{ J}$  per electrical operation situates the nTron gate between RSFQ and cryo-CMOS logic in efficiency. While the present demonstration operates without global clocking or complex DC bias trees, large-scale implementations will require bias distribution networks. Static power dissipation in such systems can, however, be minimized through the use of inductive bias trees, which efficiently store and distribute bias currents without continuous resistive losses<sup>40</sup>.

The development of reconfigurable superconducting nanowire logic directly supports the broader effort toward scalable photonic quantum computing architectures. Recent progress demonstrated a manufacturable silicon photonics platform for large-scale quantum information processing<sup>2</sup>, highlighting the importance of integrating fast, low-power control electronics with photonic components. Our approach complements such advances by providing a native superconducting logic layer that can interface directly with single-photon detectors and modulators on the same chip. The ability to implement logic operations within the cryogenic layer eliminates the latency and interconnect complexity associated with off-chip signal routing, paving the way for tightly integrated quantum photonic circuits with ultrafast feedforward capability.

The remaining limitations such as bias asymmetry, thermal recovery, and the narrowing of bias windows at higher repetition rates arise from practical design constraints. These can be mitigated through improved layout symmetry, matched shunts, and active reset schemes. Further co-design of the detector geometry, nTron dimensions, and interconnect inductance could expand the operating margins while preserving the compact footprint and low dissipation demonstrated here.

## F. Conclusion

The demonstrated bias-configurable nanocryotron logic gate provides a compact and energy-efficient building block for on-chip superconducting logic compatible with SNSPD technology. By tuning bias currents, a single circuit can implement AND, OR, and XOR functions with sub- $10^{-3}$  error rates and femtojoule-level dissipation, offering flexible operation within the same layout. This reconfigurability simplifies cryogenic logic design and enables direct integration with superconducting detector arrays. Future work will extend this concept toward multi-gate logic circuits and co-fabricated detector-logic networks, paving the way for scalable cryogenic computing, quantum feedforward control, and low-power signal processing in extreme environments.

## ACKNOWLEDGMENTS

The initial part of this work was supported by the National Science Foundation under Grant No. OMA-2137723 and the Center for Quantum Networks (CQN) Grant No. EEC-1941583. The second stage of this work was sponsored by the U.S. Department of Energy under Award No. DE-AC02-07CH11359. Alejandro Simon acknowledges support from the NSF GRFP. We would like to thank Phillip D. Keathley for helping with the data analysis.

## DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## REFERENCES

- <sup>1</sup>J. Wang, F. Sciarrino, A. Laing, and M. G. Thompson, *Nat. Photonics* **14**, 273 (2020).
- <sup>2</sup>PsiQuantum team, *Nature* **641**, 876 (2025).
- <sup>3</sup>B. G. Oripov, D. S. Rampini, J. Allmaras, M. D. Shaw, S. W. Nam, B. Kozh, and A. N. McCaughan, *Nature* **622**, 730 (2023).
- <sup>4</sup>E. Pelucchi, G. Fagas, I. Aharonovich, D. Englund, E. Figueroa, Q. Gong, H. Hannes, J. Liu, C.-Y. Lu, N. Matsuda, J.-W. Pan, F. Schreck, F. Sciarrino, C. Silberhorn, J. Wang, and K. D. Jöns, *Nat. Rev. Phys.* **4**, 194 (2022).
- <sup>5</sup>M. Colangelo, B. Desiatov, D. Zhu, J. Holzgrafe, O. Medeiros, M. Loncar, and K. K. Berggren, in *Conference on Lasers and Electro-Optics* (Optica Publishing Group, 2020) p. SM4O.4.
- <sup>6</sup>A. A. Sayem, R. Cheng, S. Wang, and H. X. Tang, *Applied Physics Letters* **116**, 151102 (2020).
- <sup>7</sup>T. Viskova, “Cryo-CMOS ICs for Scalable Superconducting Nanowire Single Photon Detectors,” (2022).
- <sup>8</sup>J. A. Fredenburg, D. Braga, T. England, F. Fahim, A. Quinn, and H. Sun, in *2024 IEEE Nuclear Science Symposium (NSS), Medical Imaging Conference (MIC) and Room Temperature Semiconductor Detector Conference (RTSD)* (2024) pp. 1–2.
- <sup>9</sup>S. Miyajima, M. Yabuno, S. Miki, T. Yamashita, and H. Terai, *Optics Express* **26**, 29045 (2018).
- <sup>10</sup>M. Yabuno, S. Miyajima, S. Miki, and H. Terai, *Optics Express* **28**, 12047 (2020).
- <sup>11</sup>F. Thiele, N. Lamberty, T. Hummel, N. A. Lange, L. M. Procopio, A. Barua, S. Lengeling, V. Quiring, C. Eigner, C. Silberhorn, and T. J. Bartley, “Cryogenic Feedforward of a Photonic Quantum State,” (2024), \_eprint: 2410.08908.
- <sup>12</sup>N. Lamberty, F. Thiele, T. Hummel, and T. J. Bartley, “Interfacing superconducting nanowire single photon detectors with cryogenic opto-electronics for quantum photonic applications,” (2025), \_eprint: 2501.08125.
- <sup>13</sup>A. N. McCaughan and K. K. Berggren, *Nano Letters* **14**, 5748 (2014).
- <sup>14</sup>A. Buzzi, M. Castellani, R. A. Foster, O. Medeiros, M. Colangelo, and K. K. Berggren, *Applied Physics Letters* **122**, 142601 (2023), special Collection: Advances in Superconducting Logic.
- <sup>15</sup>A. Simon, R. Foster, O. Medeiros, M. Castellani, E. Batson, and K. K. Berggren, *IEEE Transactions on Applied Superconductivity* **35**, 1 (2025).
- <sup>16</sup>Q.-Y. Zhao, A. N. McCaughan, A. E. Dane, K. K. Berggren, and T. Ortlepp, *Superconductor Science and Technology* **30**, 044002 (2017).
- <sup>17</sup>D. J. Paul, T. X. Zhou, and K. K. Berggren, *Phys. Rev. Appl.* **24**, 024060 (2025), publisher: American Physical Society.
- <sup>18</sup>M. Colangelo, D. Zhu, L. Shao, J. Holzgrafe, E. K. Batson, B. Desiatov, O. Medeiros, M. Yeung, M. Lončar, and K. K. Berggren, *ACS Photonics* **11**, 356 (2024).
- <sup>19</sup>R. Baghdadi, J. P. Allmaras, B. A. Butters, A. E. Dane, S. Iqbal, A. N. McCaughan, E. A. Toomey, Q.-Y. Zhao, A. G. Kozorezov, and K. K. Berggren, *Phys. Rev. Appl.* **14**, 054011 (2020), publisher: American Physical Society.
- <sup>20</sup>V. Karam, O. Medeiros, T. El Dandachi, M. Castellani, R. Foster, M. Colangelo, and K. K. Berggren, *Physical Review Applied* **24**, 024020 (2025).
- <sup>21</sup>A. N. McCaughan, V. B. Verma, S. M. Buckley, J. P. Allmaras, A. G. Kozorezov, A. N. Tait, S. W. Nam, and J. M. Shainline, *Nature Electronics* **2**, 451 (2019).
- <sup>22</sup>M. Castellani, M. Colangelo, O. Medeiros, J. C. Bienfang, R. A. Foster, A. Buzzi, A. Restelli, and K. K. Berggren, *Physical Review Applied* **22**, 024020 (2024).
- <sup>23</sup>Y.-H. Huang, Q.-Y. Zhao, H. Hao, N.-T. Liu, Z. Liu, J. Deng, F. Yang, S.-Y. Ru, X.-C. Tu, L.-B. Zhang, X.-Q. Jia, J. Chen, L. Kang, and P.-H. Wu, *Applied Physics Letters* **124**, 192601 (2024), editor’s Pick, Special Collection: 2024 Rising Stars Collection.
- <sup>24</sup>K. Zheng, Q.-Y. Zhao, H.-Y.-B. Lu, L.-D. Kong, S. Chen, H. Hao, H. Wang, D.-F. Pan, X.-C. Tu, L.-B. Zhang, X.-Q. Jia, J. Chen, L. Kang, and P.-H. Wu, *Nano Letters* **20**, 3553 (2020).
- <sup>25</sup>R. A. Foster, M. Castellani, A. Buzzi, O. Medeiros, M. Colangelo, and K. K. Berggren, *Applied Physics Letters* **122**, 152601 (2023).
- <sup>26</sup>B. A. Butters, R. Baghdadi, M. Onen, E. A. Toomey, O. Medeiros, and K. K. Berggren, *Superconductor Science and Technology* **34**, 035003 (2021), publisher: IOP Publishing.

- <sup>27</sup>H. Wang, N. Noordzij, M. Mikhailov, S. Steinhauer, T. Descamps, E. Ok-senberg, V. Zwiller, and I. E. Zadeh, *Nano Letters* **25**, 4401 (2025).
- <sup>28</sup>M. Castellani, O. Medeiros, A. Buzzi, R. A. Foster, M. Colangelo, and K. K. Berggren, *Nature Electronics* **8**, 417 (2025).
- <sup>29</sup>E. Toomey, K. Segall, M. Castellani, M. Colangelo, N. Lynch, and K. K. Berggren, *Nano Letters* **20**, 8059 (2020).
- <sup>30</sup>A. E. Lombo, J. Lares, M. Castellani, C.-N. Chou, N. Lynch, and K. K. Berggren, *Neuromorphic Computing and Engineering* **2**, 034011 (2022), publisher: IOP Publishing.
- <sup>31</sup>S. Alam, D. S. Rampini, B. G. Oripov, A. N. McCaughan, and A. Aziz, *Applied Physics Letters* **123**, 152603 (2023).
- <sup>32</sup>K. K. Berggren, Q.-Y. Zhao, N. Abebe, M. Chen, P. Ravindran, A. McCaughan, and J. C. Bardin, *Superconductor Science and Technology* **31**, 055010 (2018).
- <sup>33</sup>M. Castellani, *Design of superconducting nanowire-based neurons and synapses for power-efficient spiking neural networks*, Ph.D. thesis, Politecnico di Torino (2020).
- <sup>34</sup>B. A. Butters, *Digital and microwave superconducting electronics and experimental apparatus*, Ph.D. thesis, Massachusetts Institute of Technology (2022).
- <sup>35</sup>J. Chang, J. W. N. Los, J. O. Tenorio-Pearl, N. Noordzij, R. Gourgues, A. Guardiani, J. R. Zichi, S. F. Pereira, H. P. Urbach, V. Zwiller, S. N. Dorenbos, and I. Esmaeil Zadeh, *APL Photonics* **6**, 036114 (2021).
- <sup>36</sup>B. Korzh, Q.-Y. Zhao, J. P. Allmaras, S. Frasca, T. M. Autry, E. A. Bersin, A. D. Beyer, R. M. Briggs, B. Bumble, M. Colangelo, G. M. Crouch, A. E. Dane, T. Gerrits, A. E. Lita, F. Marsili, G. Moody, C. Peña, E. Ramirez, J. D. Rezac, N. Sinclair, M. J. Stevens, A. E. Velasco, V. B. Verma, E. E. Wollman, M. D. Shaw, R. P. Mirin, S. W. Nam, and K. K. Berggren, *Nature Photonics* **14**, 250 (2020).
- <sup>37</sup>A. Bairamkulov, A. Bozbey, O. A. Mukhanov, M. A. Manheimer, A. Di Michele, F. Giazotto, G. N. Goltsman, and G. De Micheli, *IEEE Circuits and Systems Magazine* **24**, 16 (2024), comprehensive review comparing RSFQ, AQFP, cryo-CMOS, and emerging nanowire-based superconducting logics.
- <sup>38</sup>C. L. Ayala, T. Tanaka, R. Saito, M. Nozoe, N. Takeuchi, and N. Yoshikawa, *IEEE Journal of Solid-State Circuits* **56**, 496 (2021).
- <sup>39</sup>D. J. Paul, T. X. Zhou, and K. K. Berggren, *Physical Review Applied* **24**, 024060 (2025), arXiv:2504.16314 [cond-mat.supr-con].
- <sup>40</sup>D. E. Kirichenko, S. Sarwana, and A. F. Kirichenko, *IEEE Transactions on Applied Superconductivity* **21**, 776 (2011).
- <sup>41</sup>A. N. McCaughan, D. M. Oh, and S. W. Nam, *IEEE Transactions on Applied Superconductivity* **30**, 2400505 (2020).
- <sup>42</sup>Q.-Y. Zhao, A. N. McCaughan, A. E. Dane, K. K. Berggren, and T. Ortlepp, *Superconductor Science and Technology* **30**, 044002 (2017).
- <sup>43</sup>D. Zhu, L. Shao, M. Yu, R. Cheng, B. Desiatov, C. J. Xin, Y. Hu, J. Holzgrafe, S. Ghosh, A. Shams-Ansari, E. Puma, N. Sinclair, C. Reimer, M. Zhang, and M. Lončar, *Advances in Optics and Photonics* **13**, 242 (2021).
- <sup>44</sup>S. Bogdanov, M. Y. Shalaginov, A. Boltasseva, and V. M. Shalaev, *Opt. Mater. Express* **7**, 111 (2017).
- <sup>45</sup>M. de Cea, E. E. Wollman, A. H. Atabaki, D. J. Gray, M. D. Shaw, and R. J. Ram, *Sci. Rep.* **10**, 9470 (2020).
- <sup>46</sup>Q.-Y. Zhao, A. N. McCaughan, A. E. Dane, K. K. Berggren, and T. Ortlepp, *Superconductor Science and Technology* **30**, 044002 (2017), publisher: IOP Publishing.
- <sup>47</sup>K. Alexander, A. Benyamin, D. Black, D. Bonneau, S. Burgos, B. Burridge, H. Cable, G. Campbell, G. Catalano, A. Ceballos, C.-M. Chang, S. S. Choudhury, C. Chung, F. Danesh, T. Dauer, M. Davis, E. Dudley, P. Er-Xuan, J. Fargas, A. Farsi, C. Fenrich, J. Frazer, M. Fukami, Y. Ganesan, G. Gibson, M. Gimeno-Segovia, S. Goeldi, P. Goley, R. Haislmaier, S. Halimi, P. Hansen, S. Hardy, J. Horng, M. House, H. Hu, M. Jadidi, V. Jain, H. Johansson, T. Jones, V. Kamineni, N. Kelez, R. Koustuban, G. Kovall, P. Krogen, N. Kumar, Y. Liang, N. LiCausi, D. Llewellyn, K. Lokovic, M. Lovelady, V. R. Manfrinato, A. Melnichek, G. Mendoza, B. Moores, S. Mukherjee, J. Munns, F.-X. Musalem, F. Najafi, J. L. O'Brien, J. E. Ortmann, S. Pai, B. Park, H.-T. Peng, N. Penthorn, B. Peterson, G. Peterson, M. Poush, G. J. Pryde, T. Ramprasad, G. Ray, A. V. Rodriguez, B. Roxworthy, T. Rudolph, D. J. Saunders, P. Shadbolt, D. Shah, A. Bahgat Shehata, H. Shin, J. Sinsky, J. Smith, B. Sohn, Y.-I. Sohn, G. Son, M. C. M. M. Souza, C. Sparrow, M. Staffaroni, C. Stavrakas, V. Sukumaran, D. Tamborini, M. G. Thompson, K. Tran, M. Triplett, M. Tung, A. Veitia, A. Vert, M. D. Vidrighin, I. Vorobeichik, P. Weigel, M. Wingert, J. Wooding, X. Zhou, and PsiQuantum Team, *Nature* (2025), 10.1038/s41586-025-08820-7.
- <sup>48</sup>M. de Cea, E. E. Wollman, A. H. Atabaki, D. J. Gray, M. D. Shaw, and R. J. Ram, *Scientific Reports* **10**, 9470 (2020).