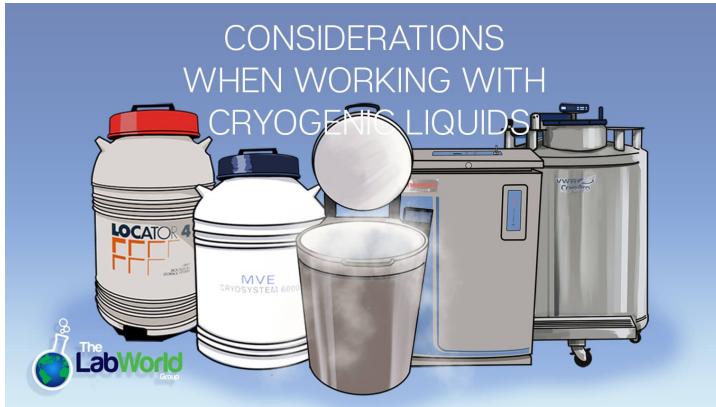


Reconfigurable Superconducting Logic Gate: From Photon-Driven Operation to Electro-Optic Modulation

QNN Group Meeting
October 20th, 2025

Gabriel Le Guay - gablg@mit.edu

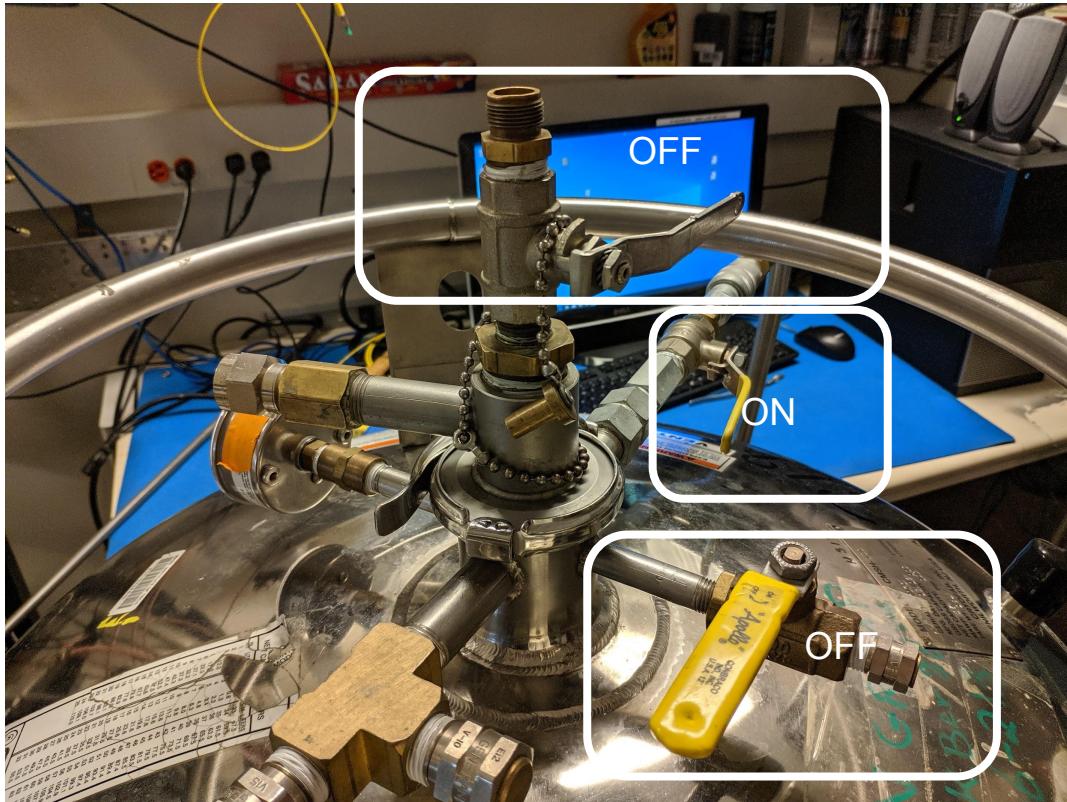
Safety Slides



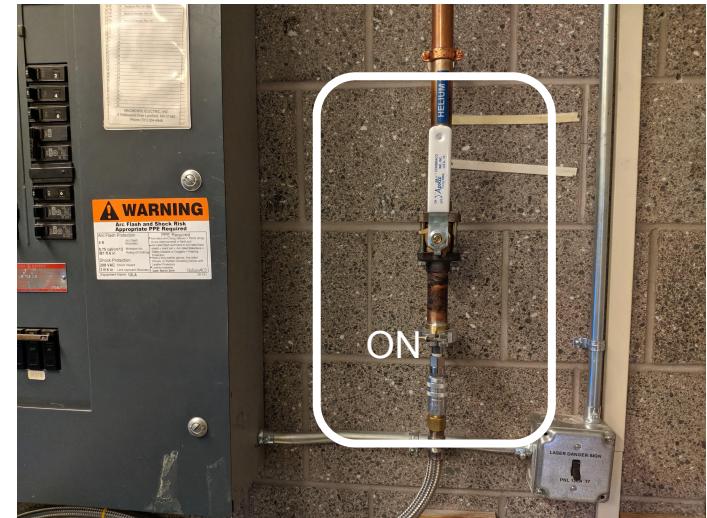
- Gloves and clothing
- Glasses
- Warn people in the room
- Avoid incompatible materials



Safety slide - dewar's valves

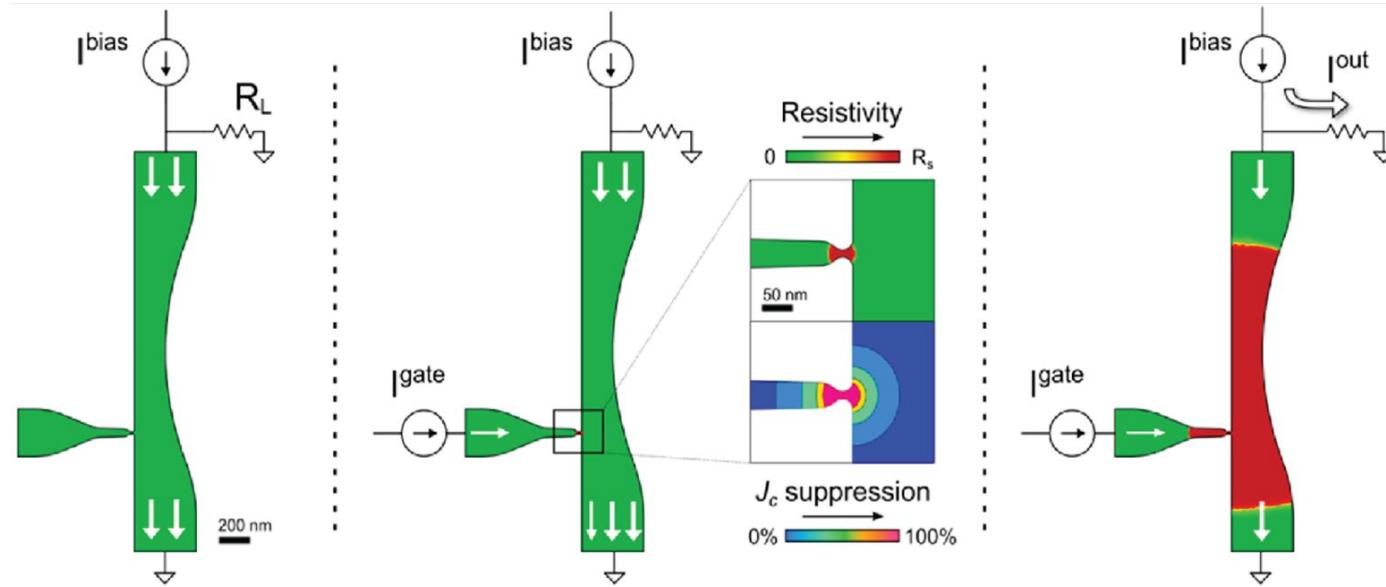


standard valves positions

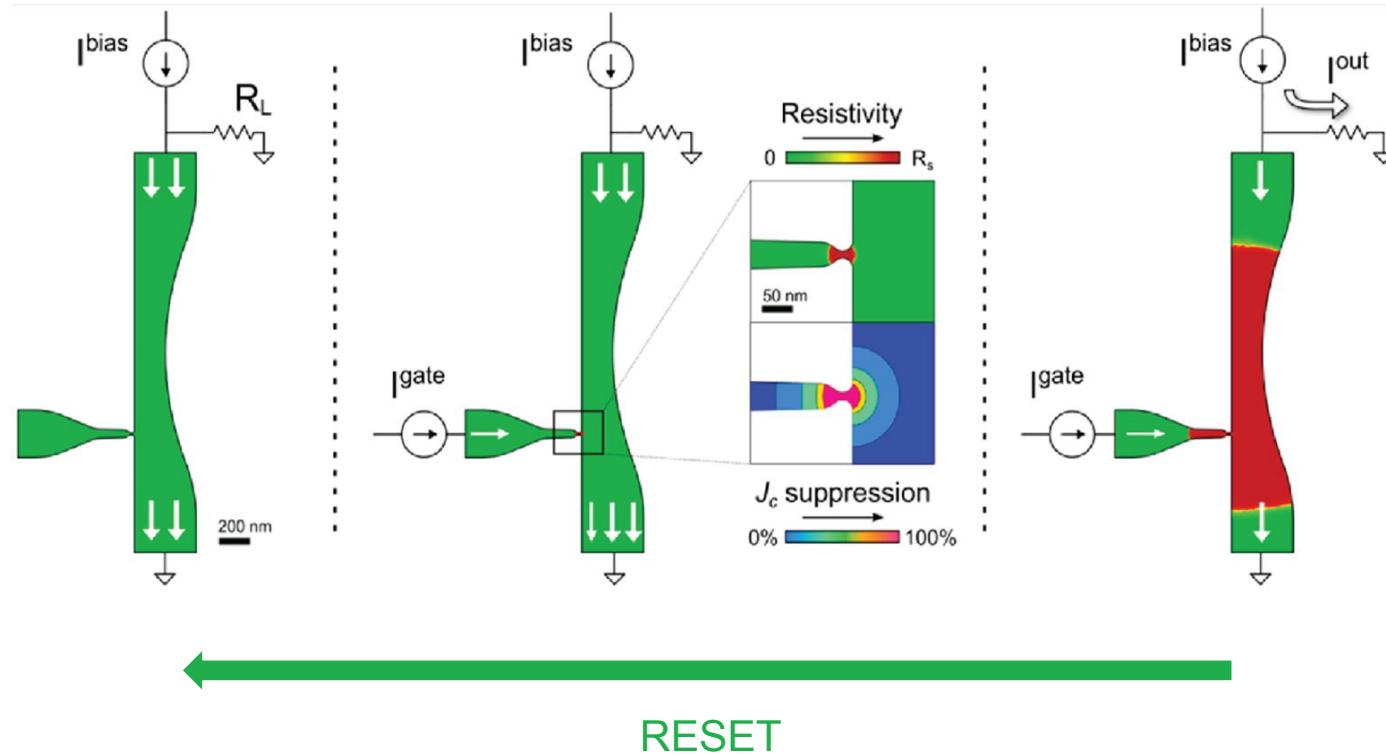


Background nTrons behavior

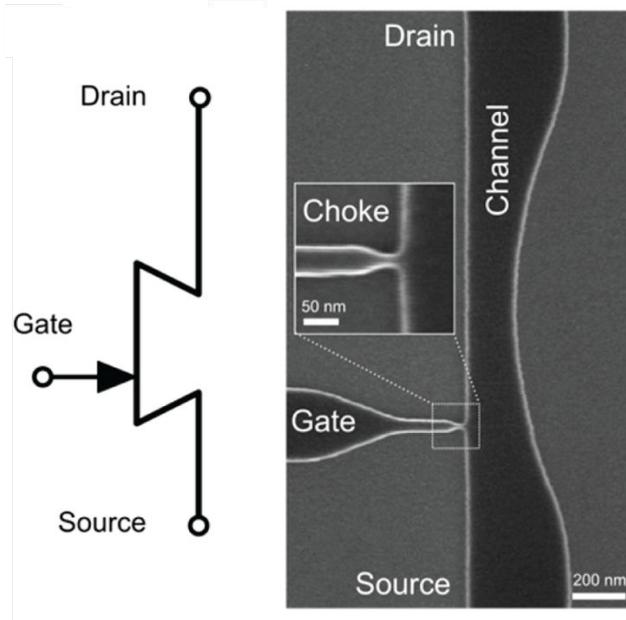
What is a Nanocryotron ?



What is a Nanocryotron ?

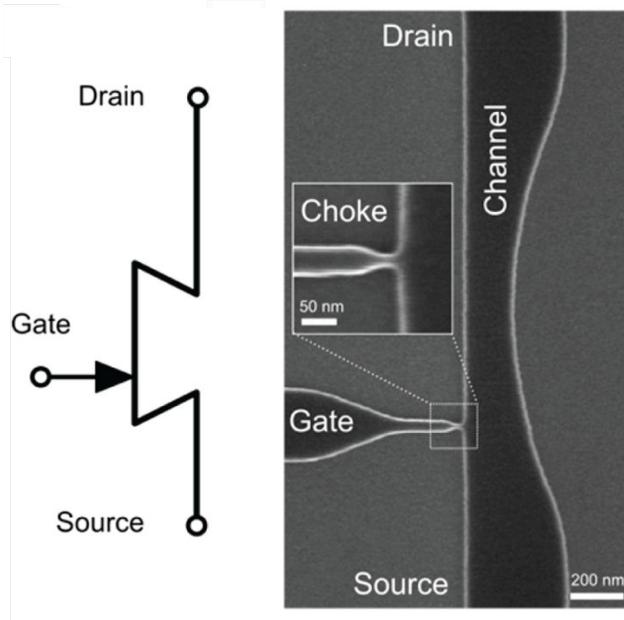


Why using Nanocryotrons ?



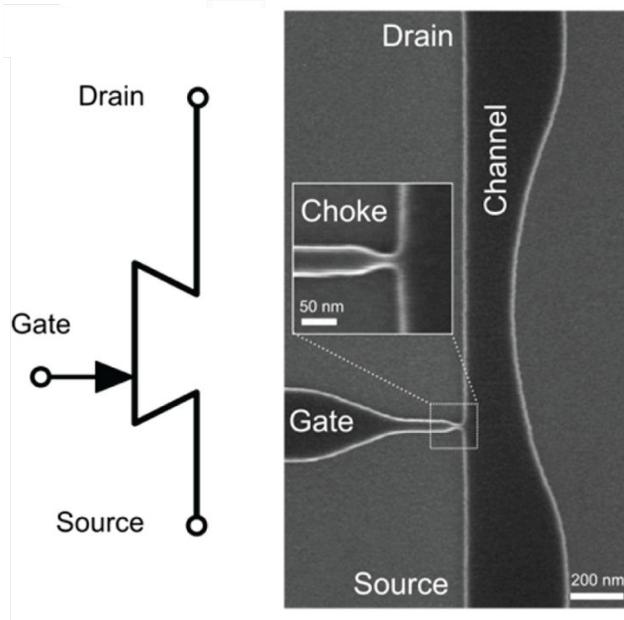
- **Simple structure**
- Magnetic field robustness
- High load driving
- Coupling with SNSPDs

Why using Nanocryotrons ?



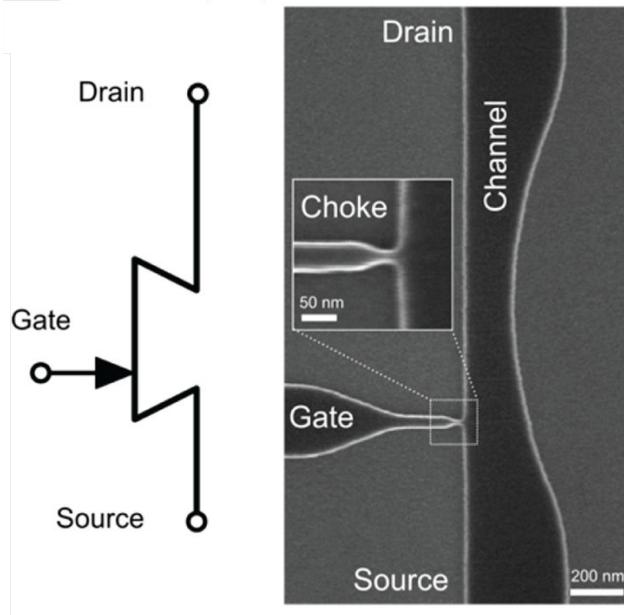
- Simple structure
- **Magnetic field robustness**
- High load driving
- Coupling with SNSPDs

Why using Nanocryotrons ?



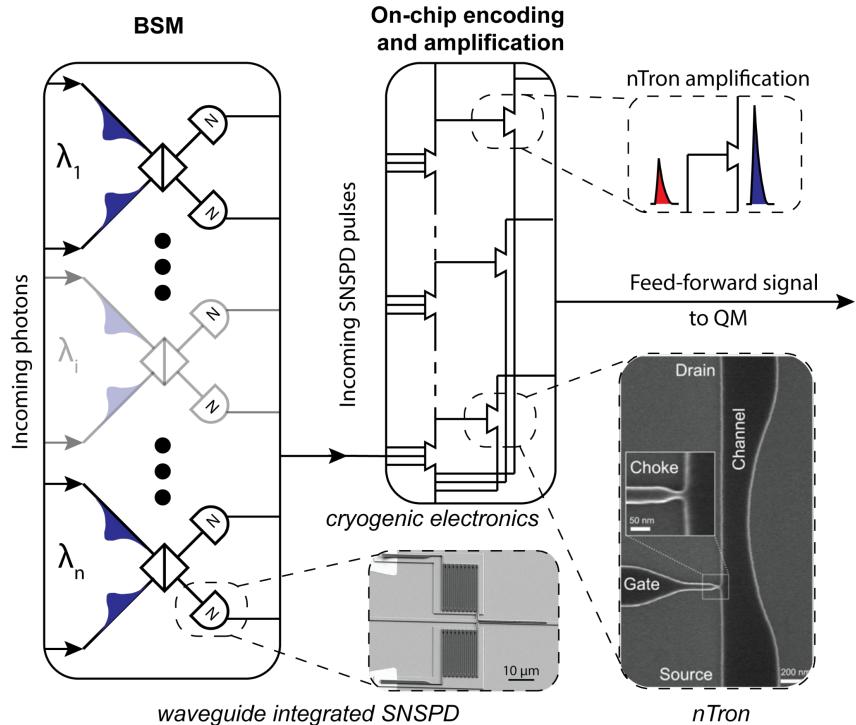
- Simple structure
- Magnetic field robustness
- **High load driving**
- Coupling with SNSPDs

Why using Nanocryotrons ?



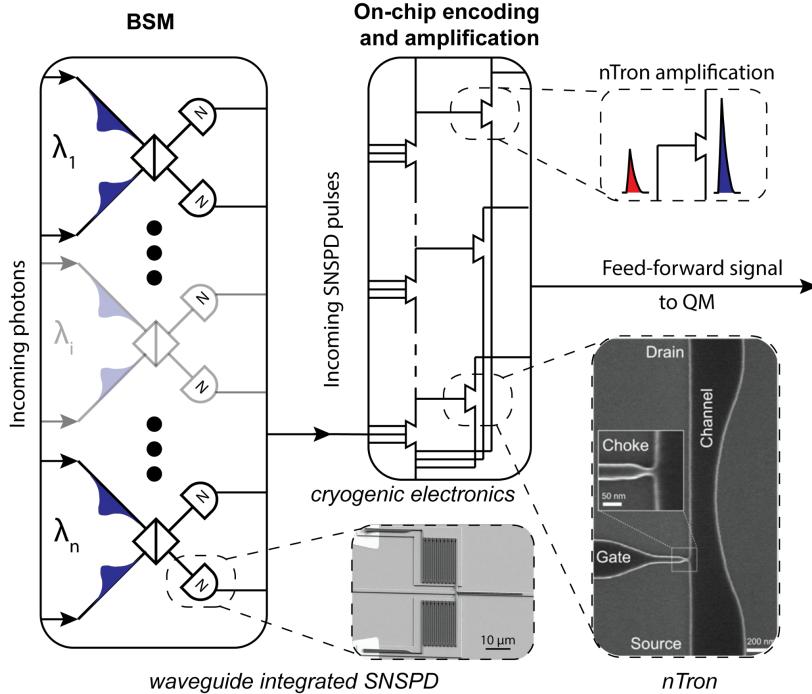
- Simple structure
- Magnetic field robustness
- High load driving
- **Coupling with SNSPDs**

Feedforward electronics with nTrons



- Can we implement any logic function with nTrons?
(e.g. logic for coincidence detection)
- Can logic operations be driven directly by SNSPDs and nTrons?
- Can we drive an optical modulator with nTrons?

For Bell-state measurements

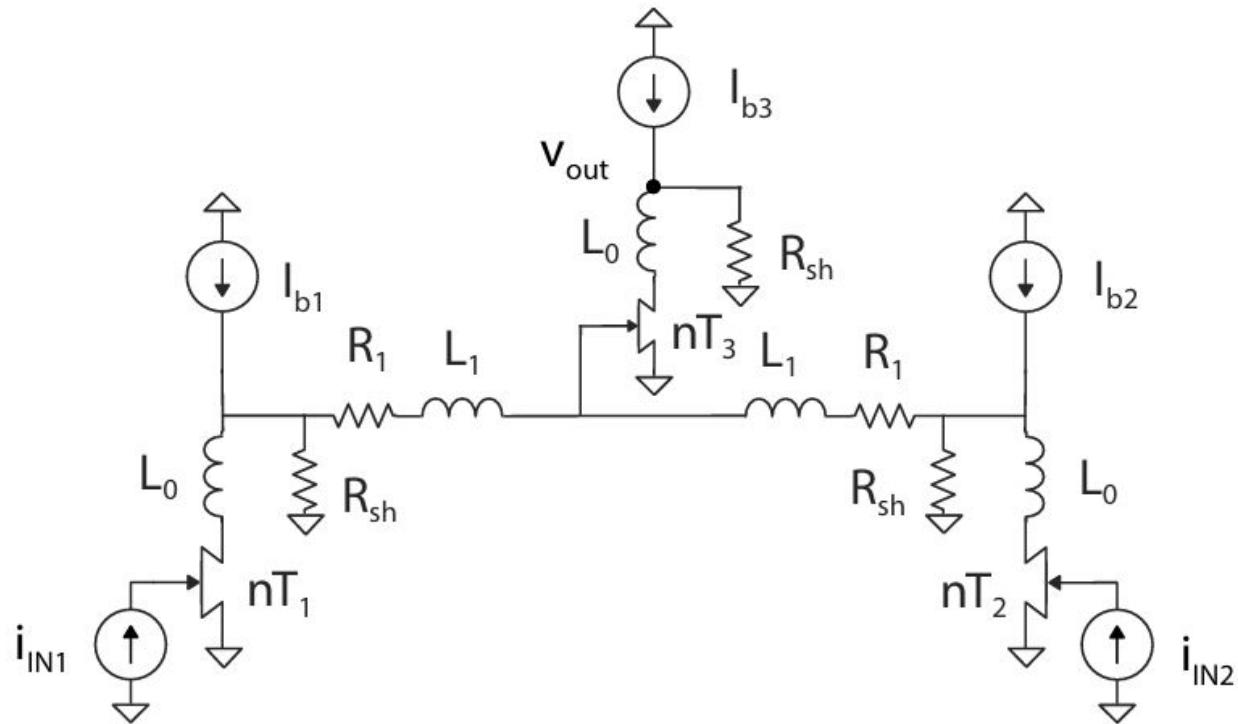


- The accuracy of Bell-state measurements increases if the photon number per detector in a SNSPD pair is known
- Depending on the state, we want to see:
 - 1 photon on both detectors,
 - or 2 photons on one and 0 on the other.

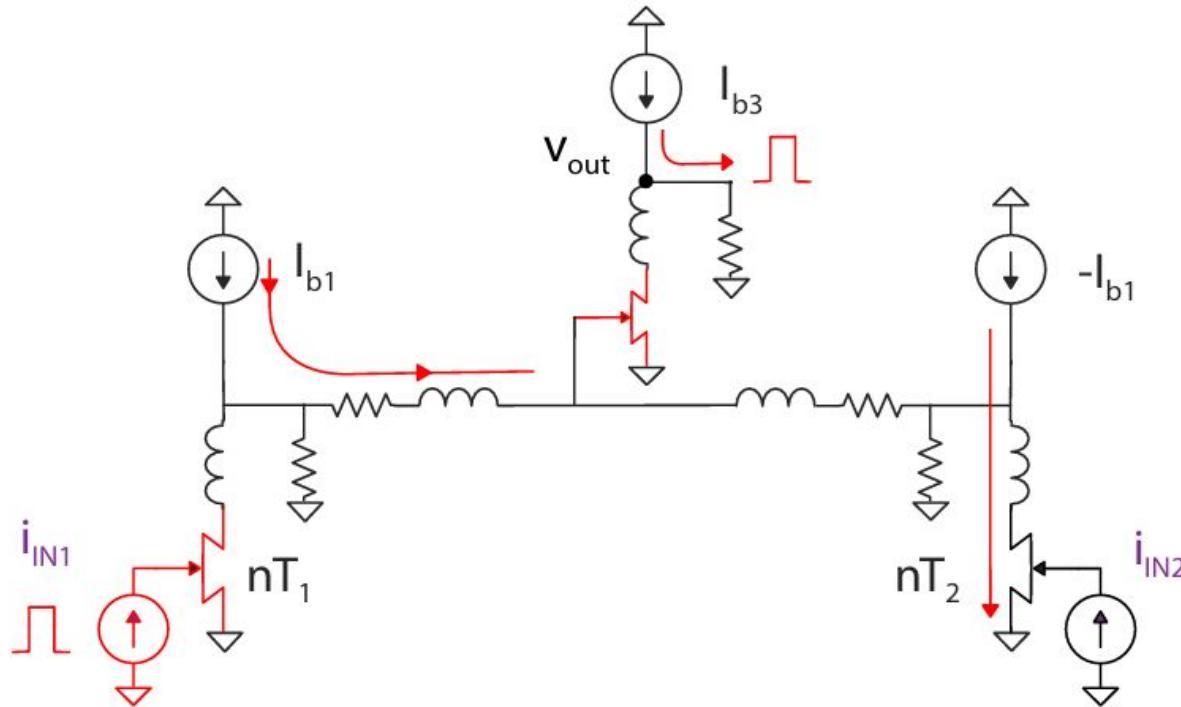
Reconfigurable Gate

From XOR to AND to OR Gate

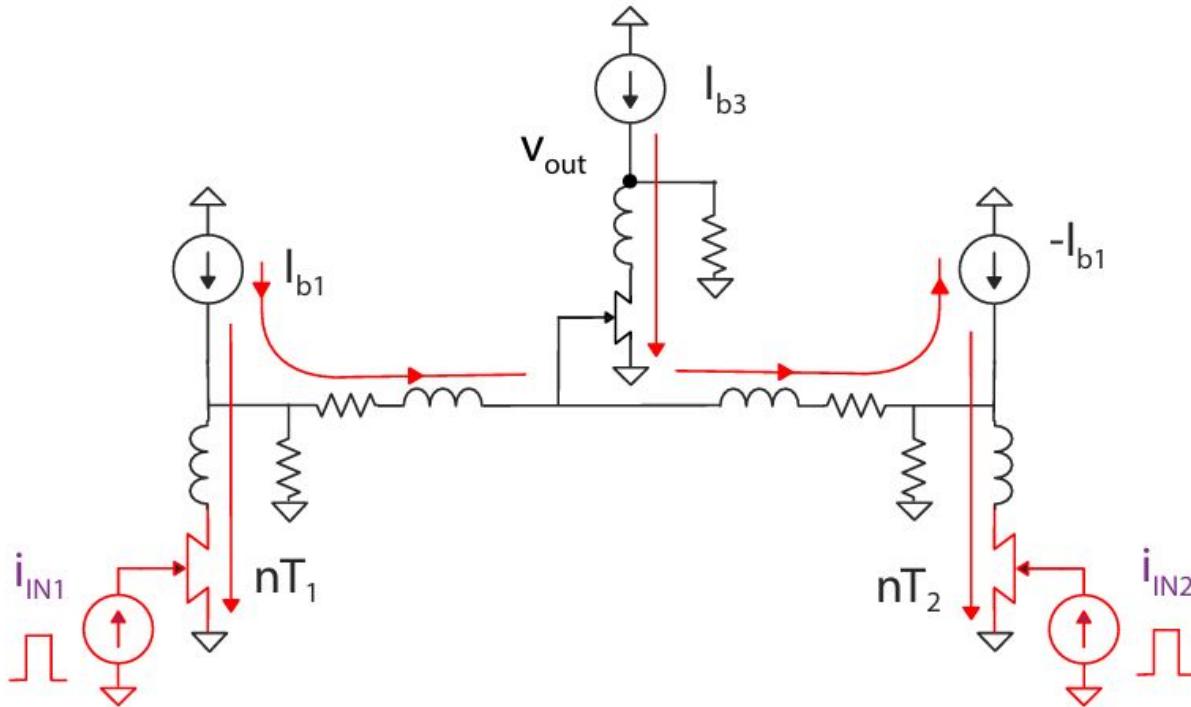
Circuit layout



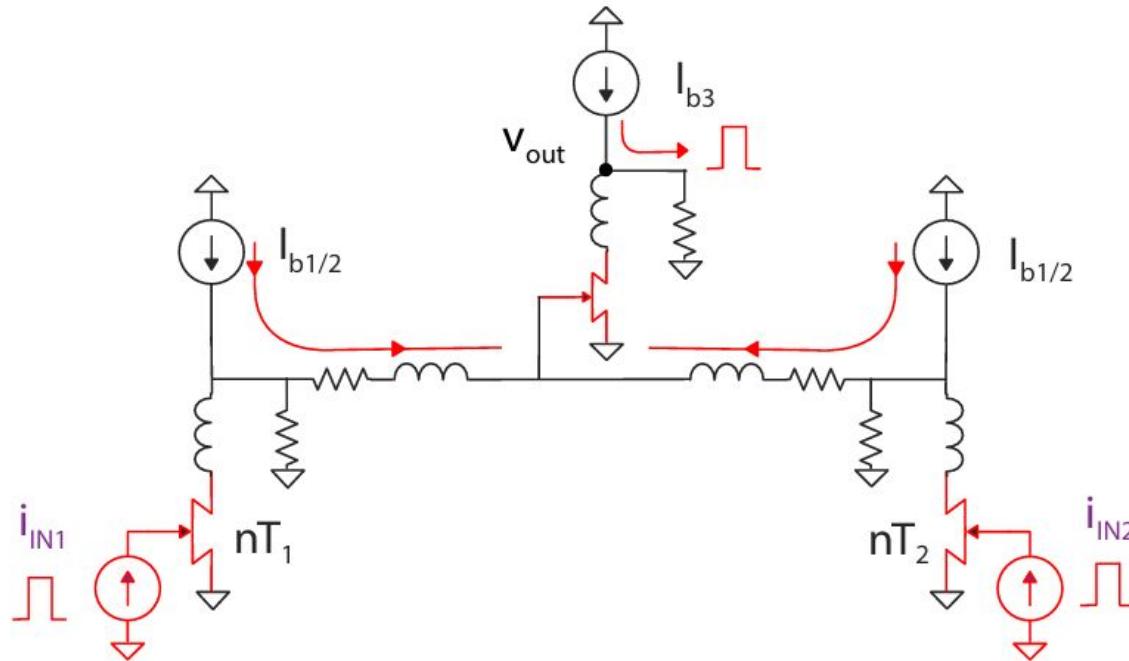
XOR mode - (1,0)



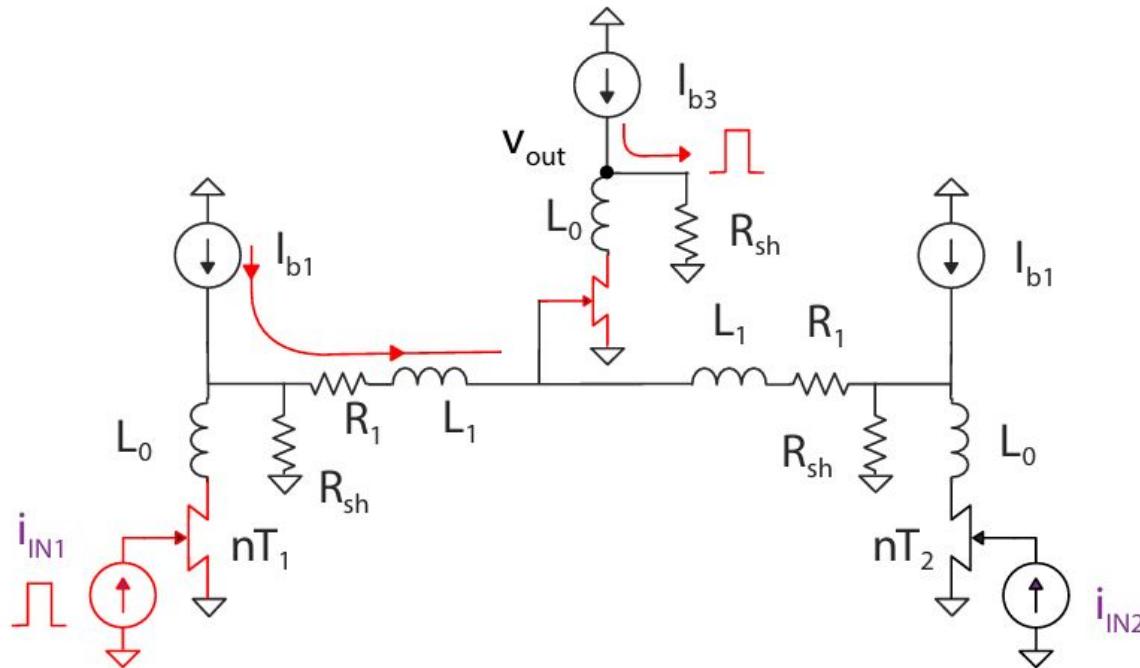
XOR mode - (1,1)



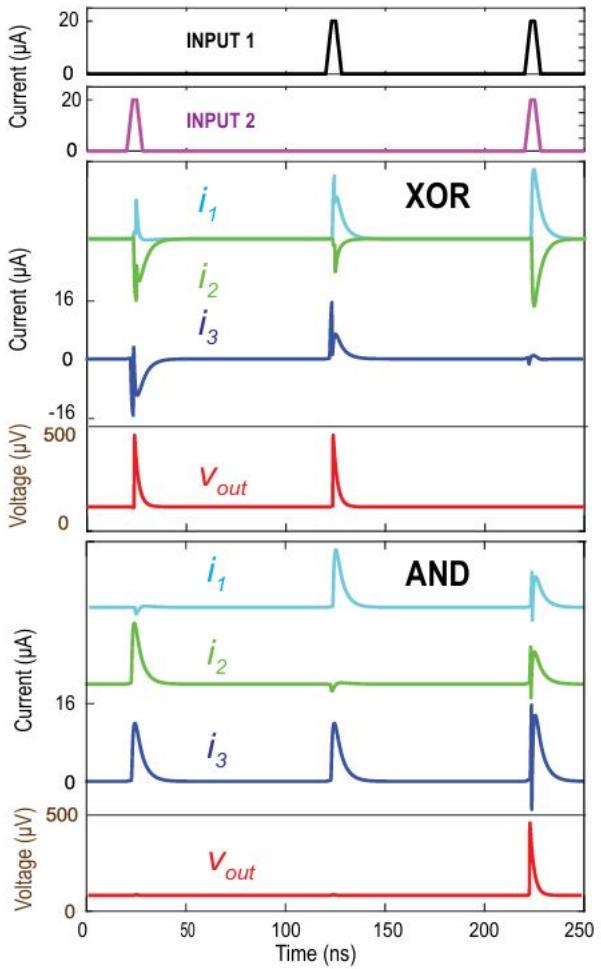
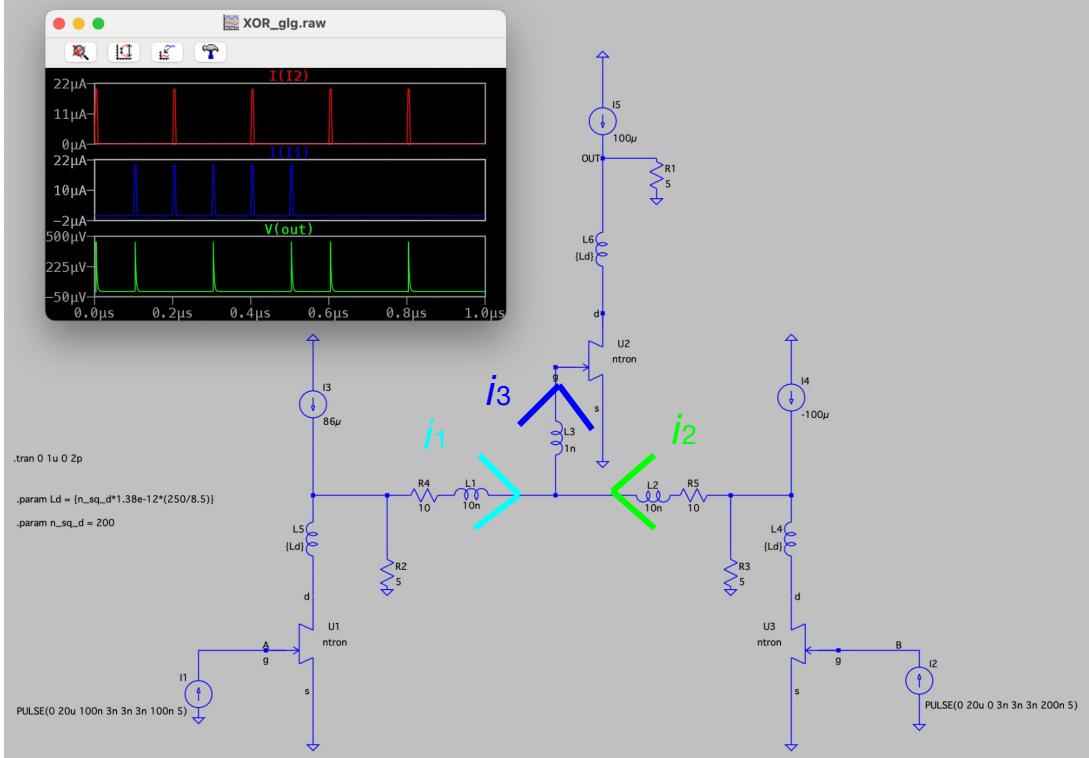
AND mode



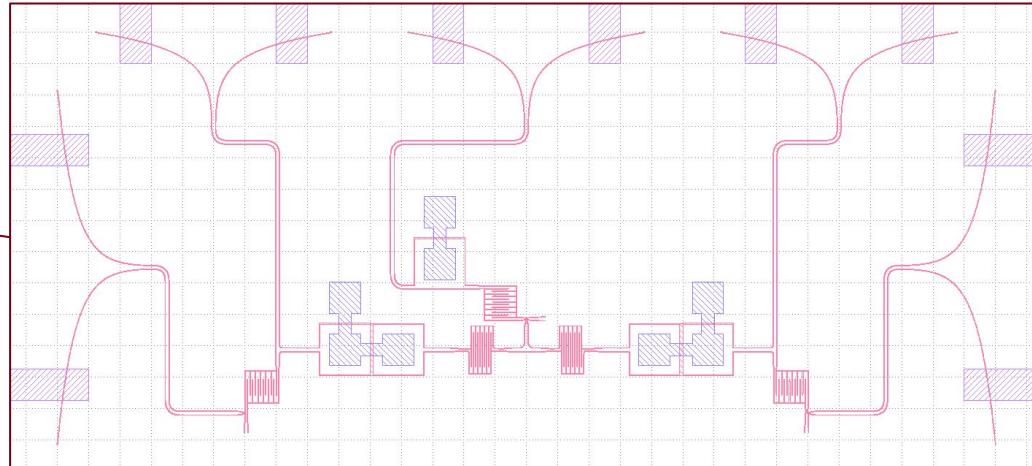
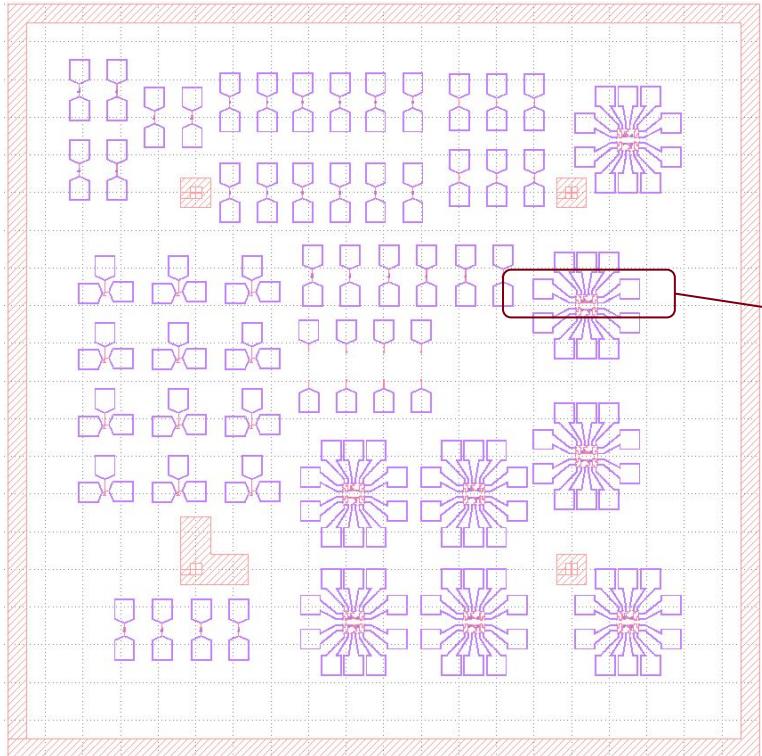
OR mode



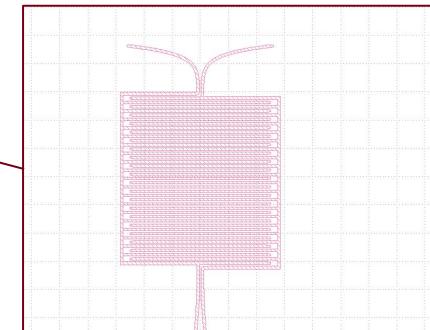
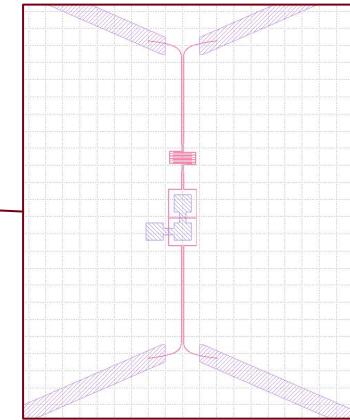
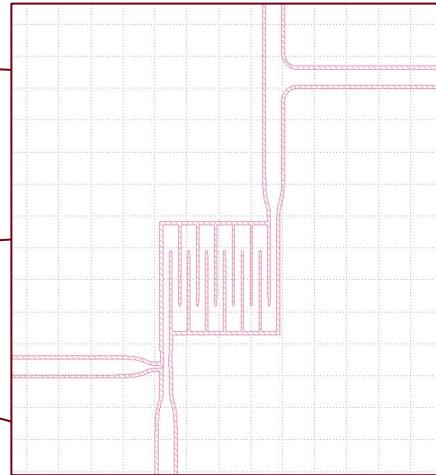
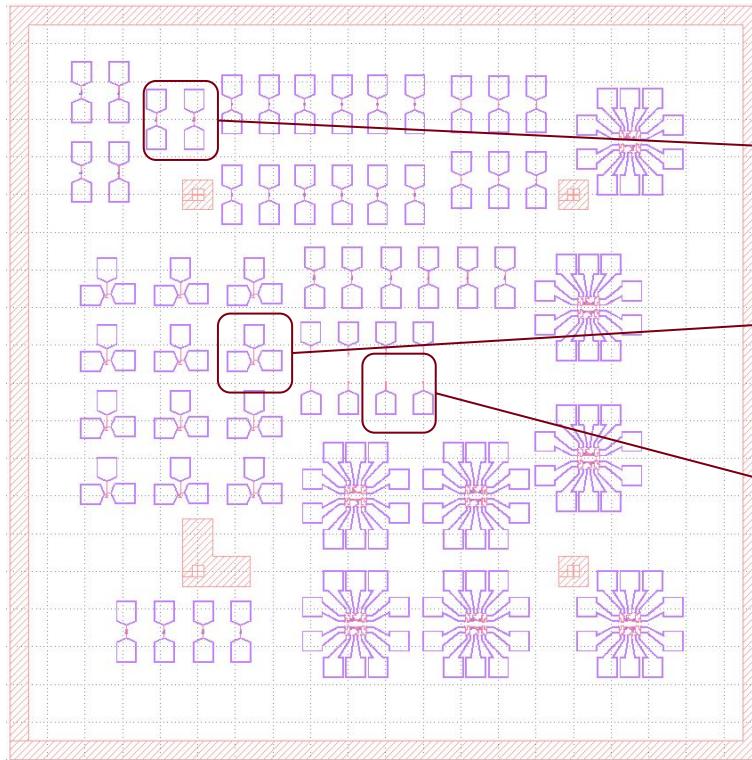
Spice Simulation



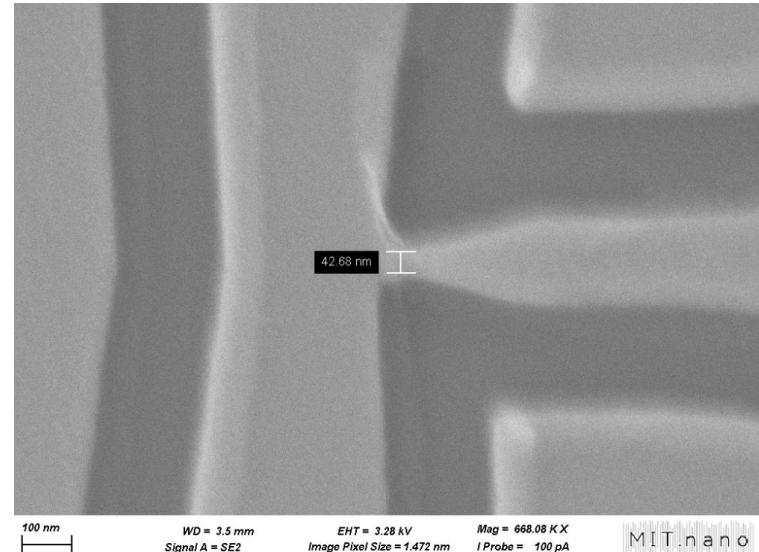
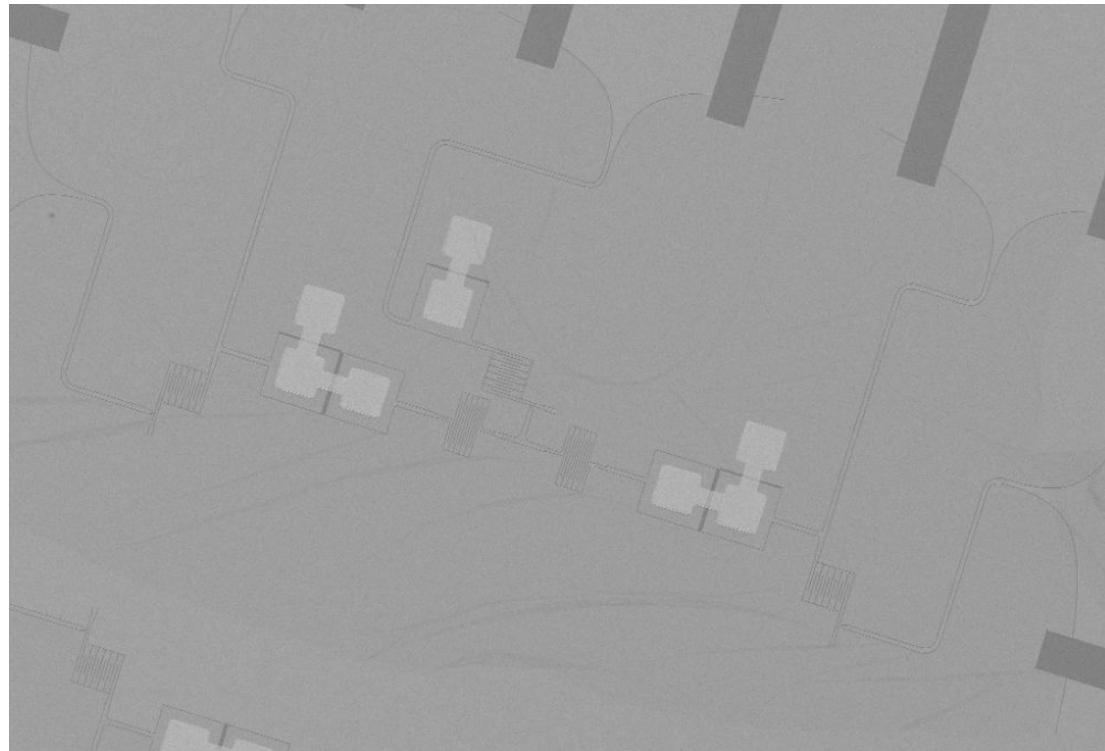
layout



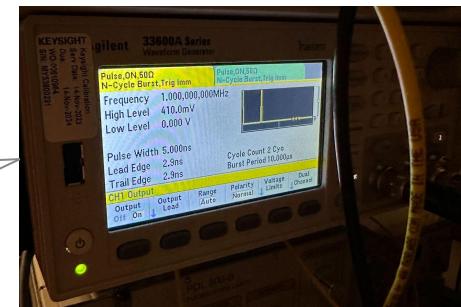
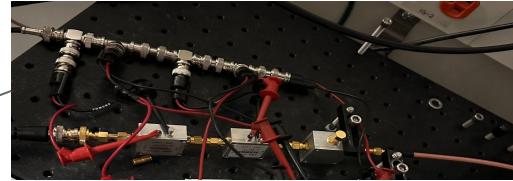
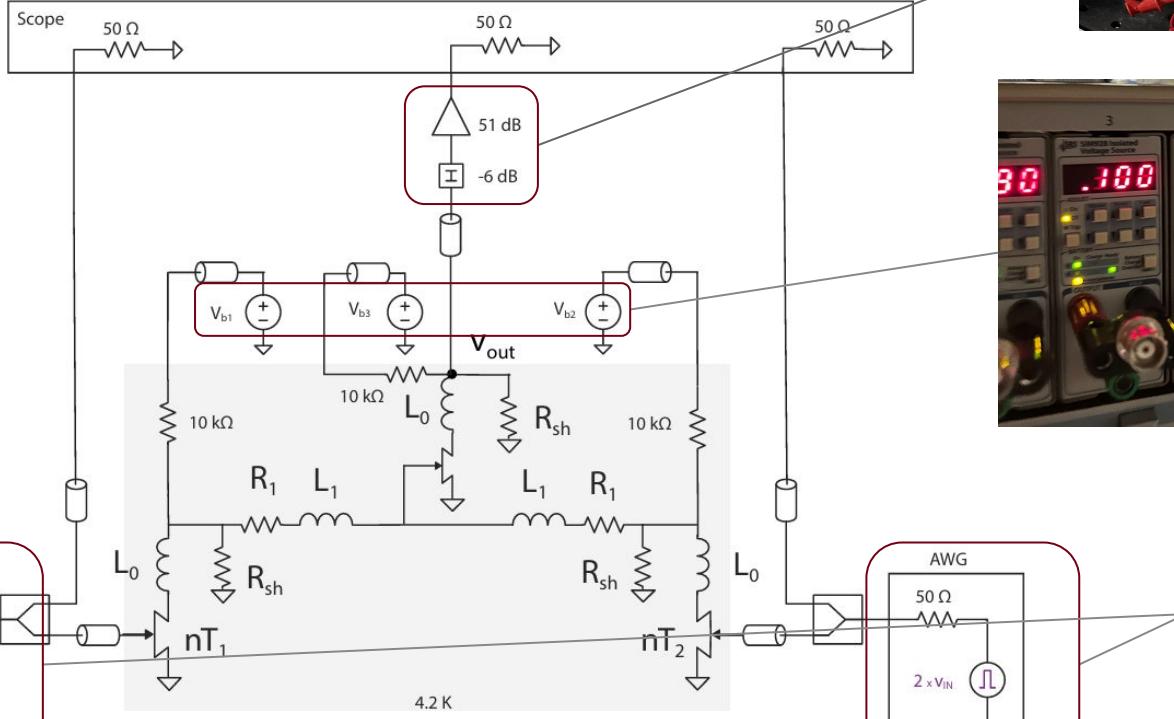
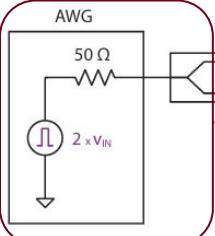
Spice Simulation, layout and fabrication



Spice Simulation, layout and fabrication



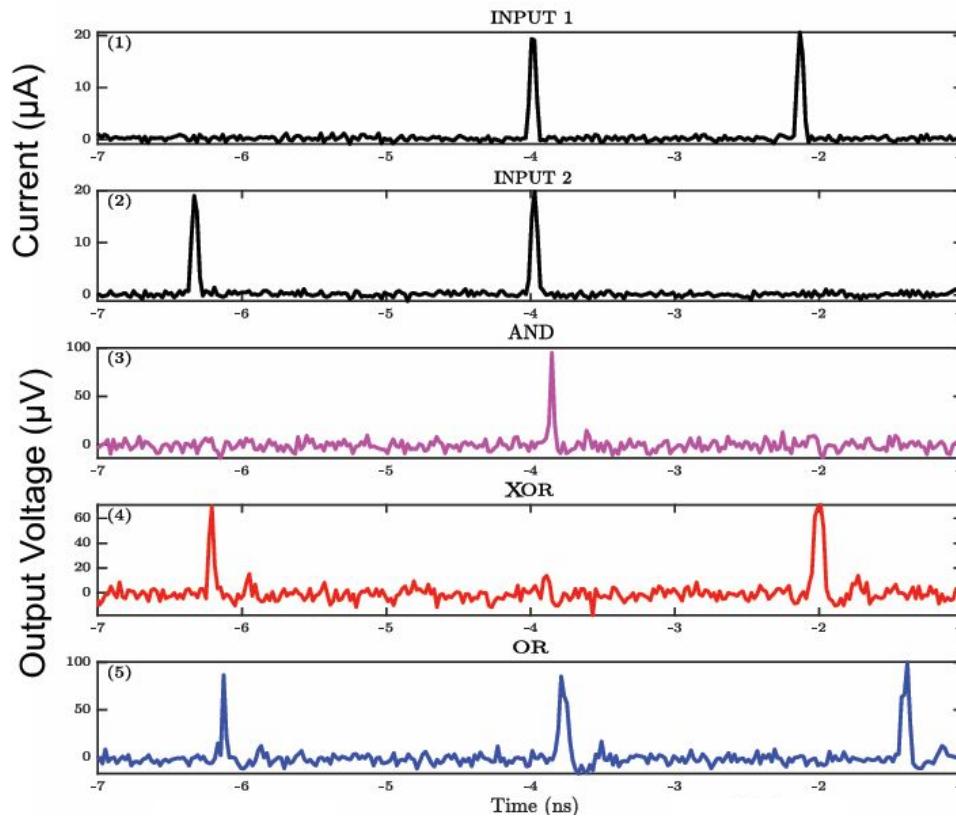
Setup methods



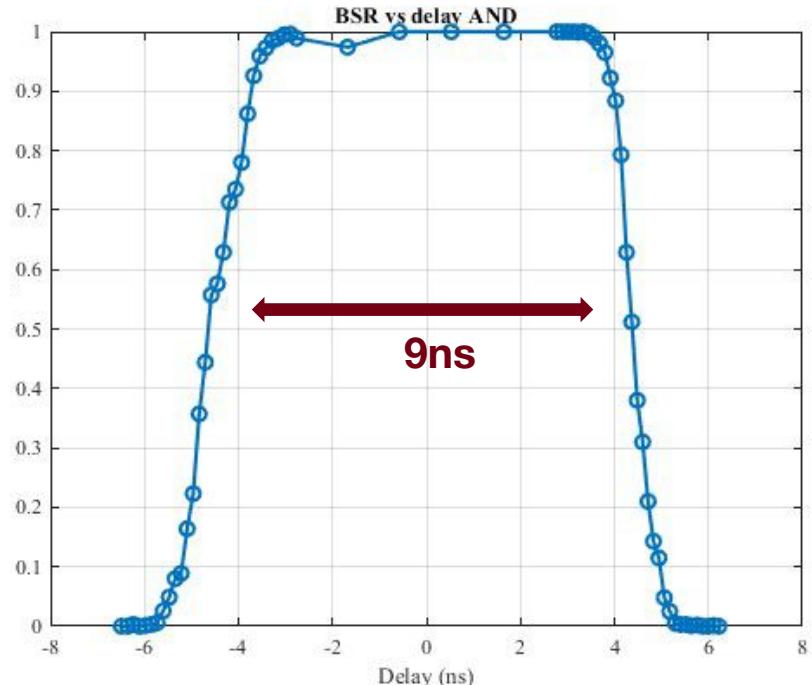
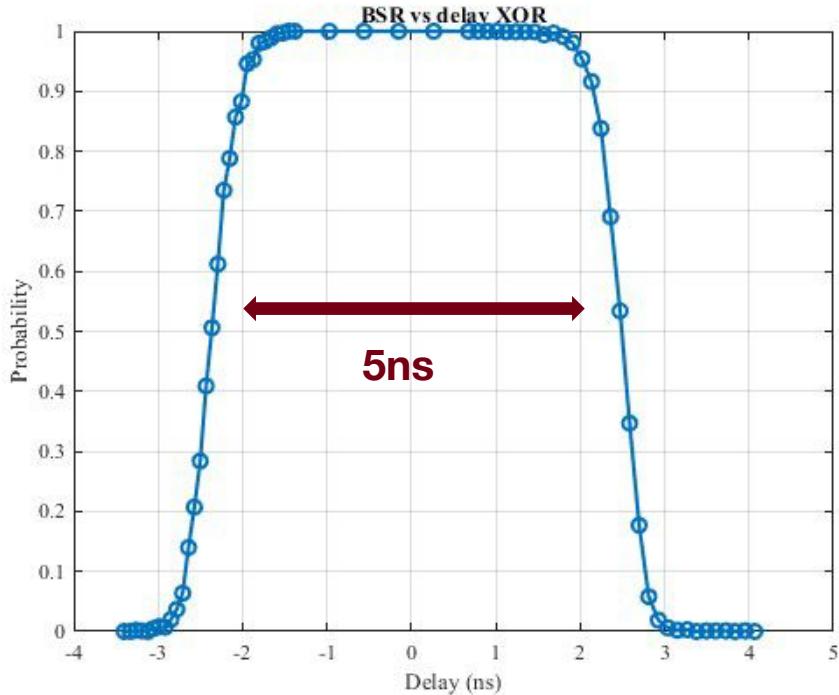
Results

Pulse alignment and Bit Error Rate

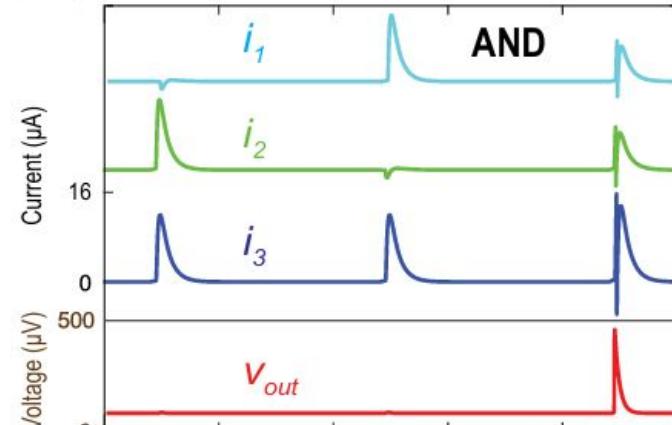
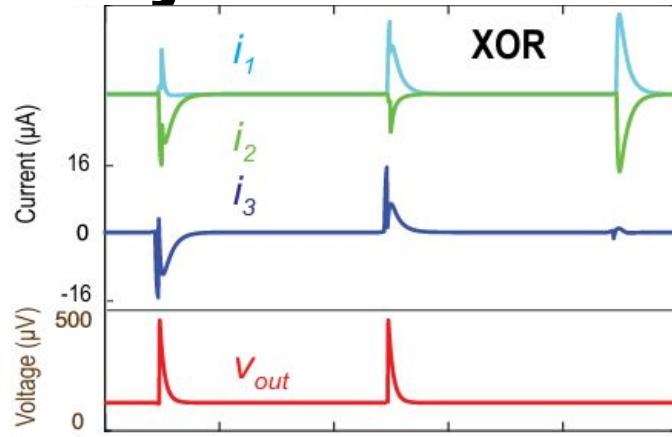
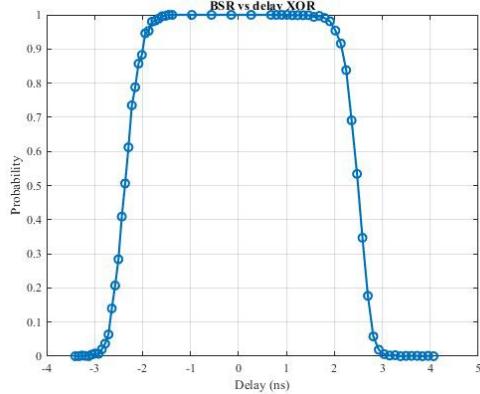
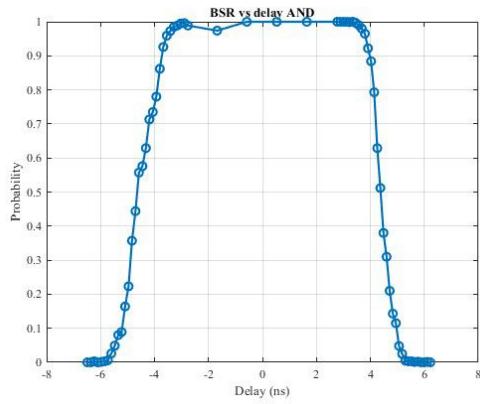
Pulse Alignment



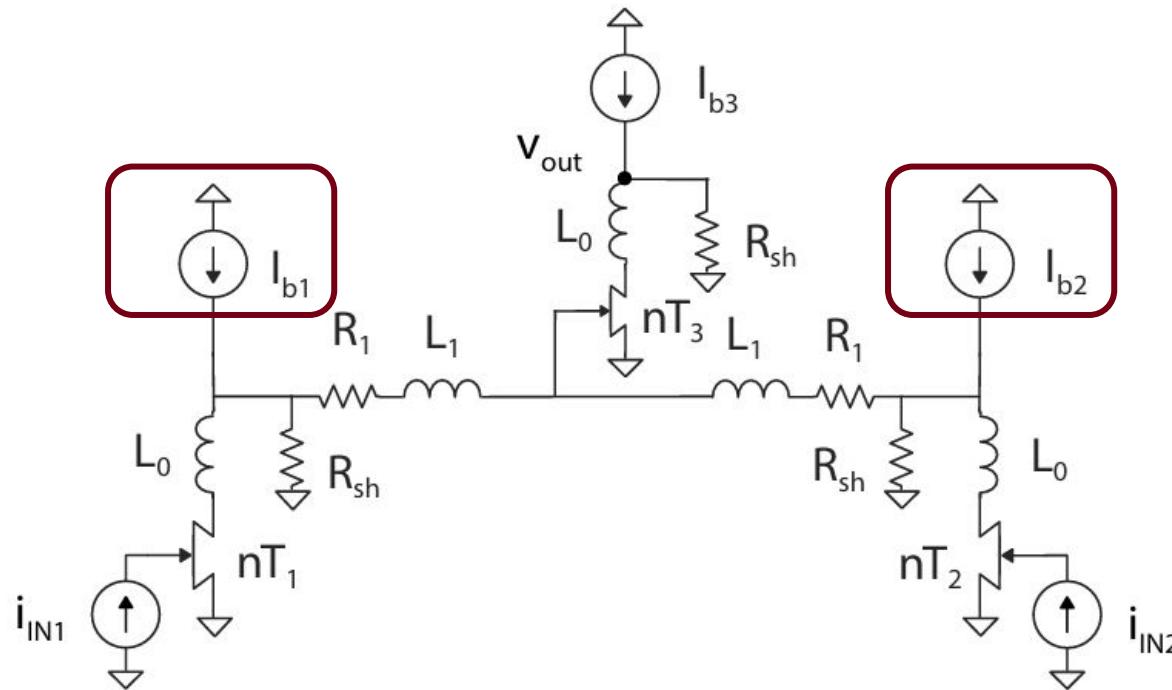
Success probability vs Delay



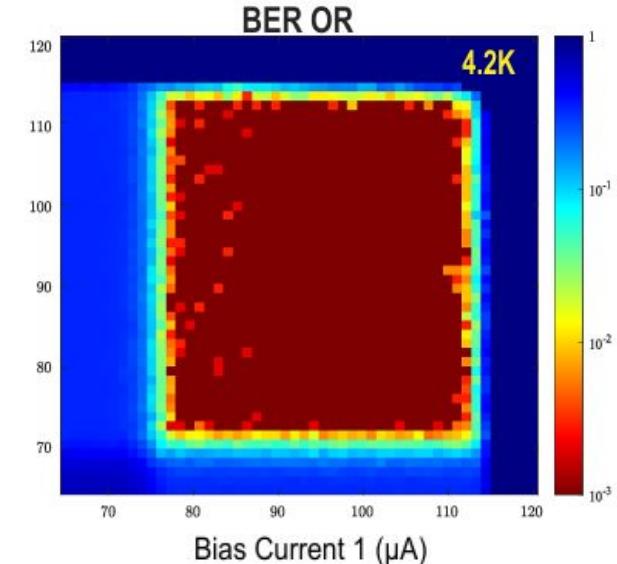
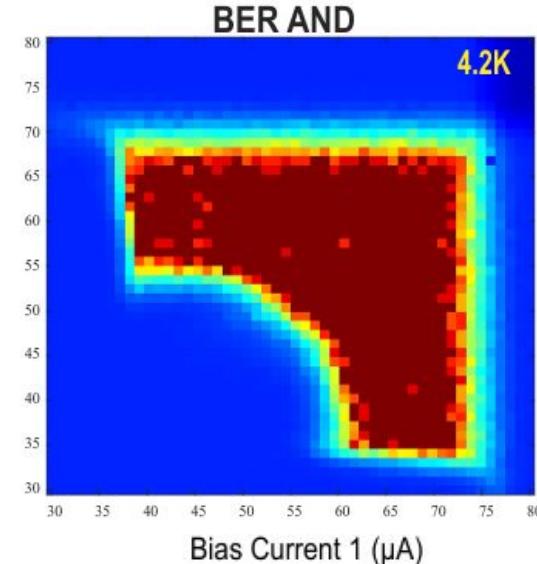
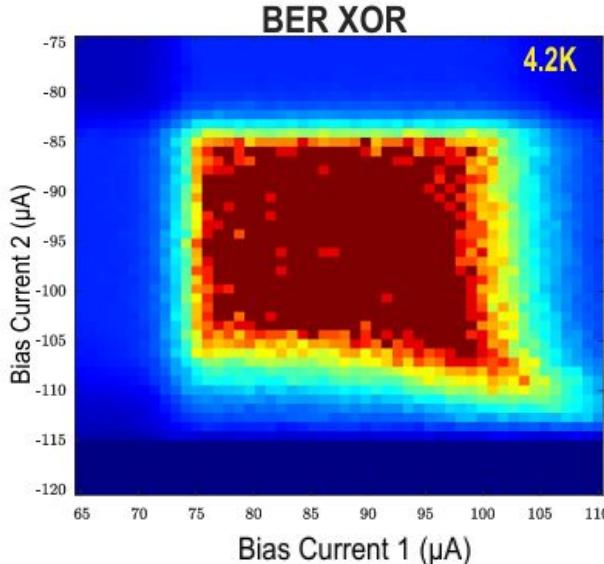
Success probability vs Delay



Bit Error Rate - Ib1 and Ib2 sweep



Bit Error Rate - Ib1 and Ib2 sweep



Operating Margins

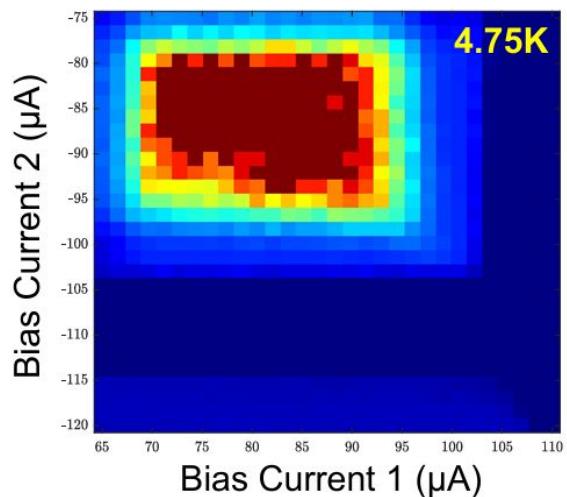
14%

16%

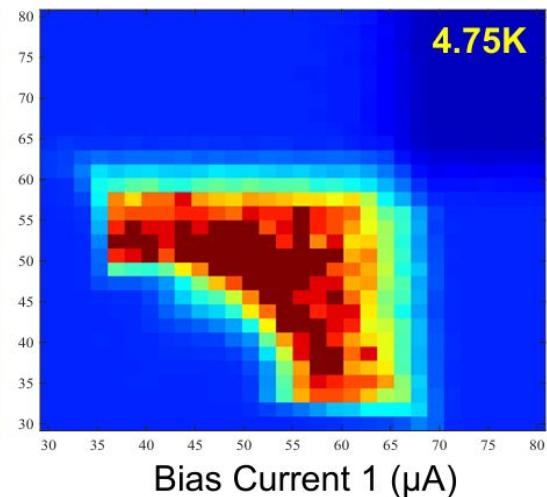
22%

Bit Error Rate - higher temperature : 4.75K

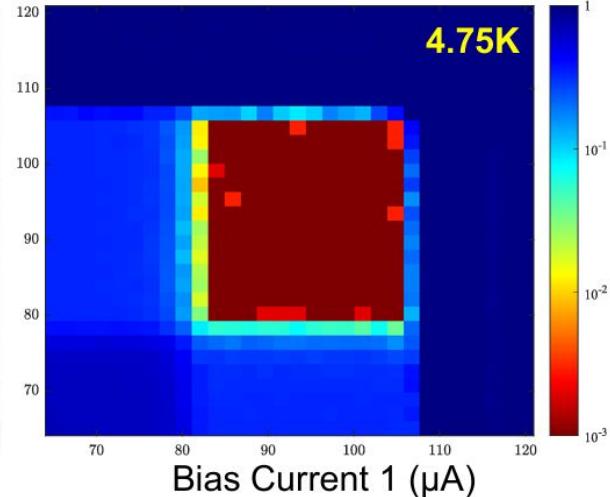
BER XOR



BER AND



BER OR



Operating Margins

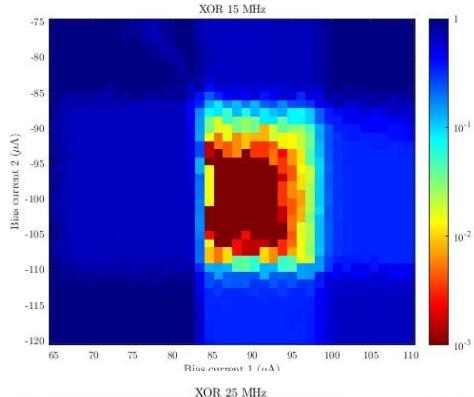
12%

13%

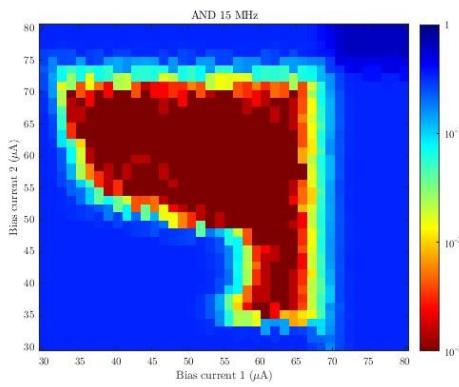
13%

Bit Error Rate - higher frequencies

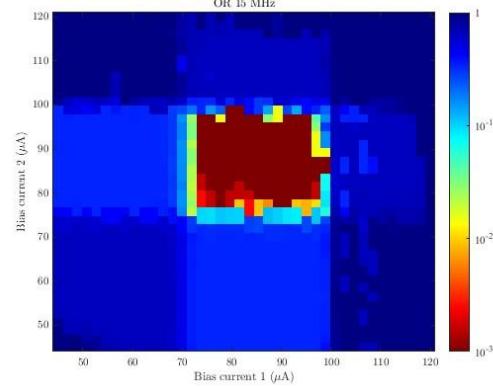
XOR



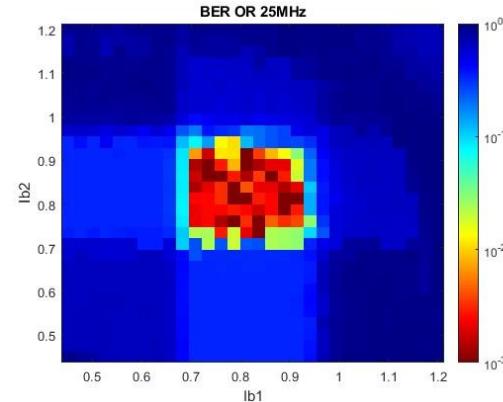
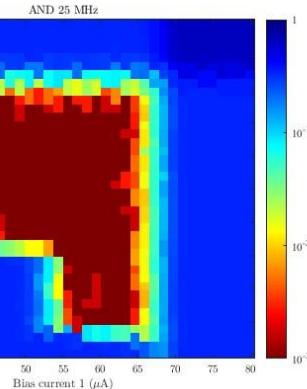
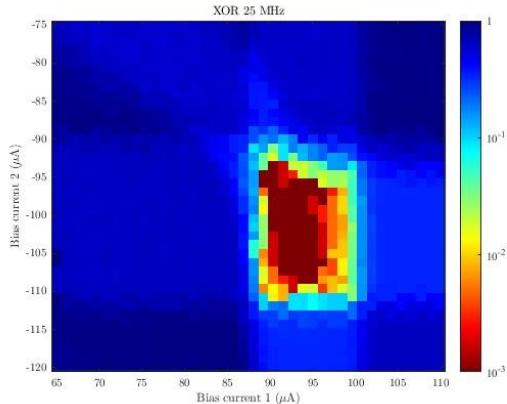
AND



OR



15MHz



25MHz

Energy consumption

$$p_i(t) = V_i(t) I_i(t), \quad E_i = \int_{t_1}^{t_2} V_i(t) I_i(t) dt, \quad E_{\text{total}} = \sum_i E_i$$

Logic mode	Mean energy per op E_{op} (J)	Mean power per op P_{op} (W)
AND	7.42×10^{-15}	9.6×10^{-7}
XOR	7.59×10^{-15}	9.9×10^{-7}
OR	7.62×10^{-15}	9.9×10^{-7}
Average	7.54×10^{-15}	9.8×10^{-7}

Technology	Typical energy per operation (J)
CMOS (room temp., 14–7 nm)	$10^{-13}\text{--}10^{-12}$
Cryo-CMOS (4 K operation)	$10^{-15}\text{--}10^{-14}$
RSFQ / ERSFQ / RQL	$10^{-18}\text{--}10^{-17}$ per Josephson junction
AQFP	$10^{-19}\text{--}10^{-18}$ per junction
nTron Reconfigurable Gate (this work)	7.5×10^{-15} ($= 7.5 \text{ fJ/op}$)

B. Bairamkulov *et al.*, “Superconducting Electronics for Energy-Efficient Computing,” *IEEE Circuits and Systems Magazine*, vol. 25, no. 1, pp. 16–32, 2025.

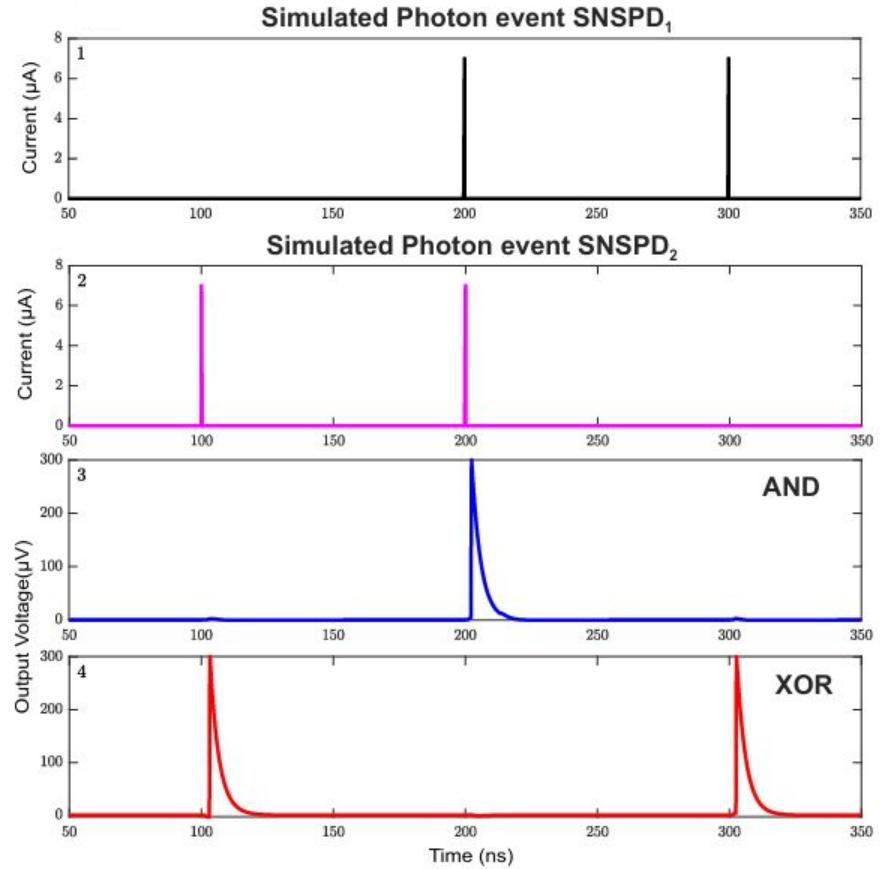
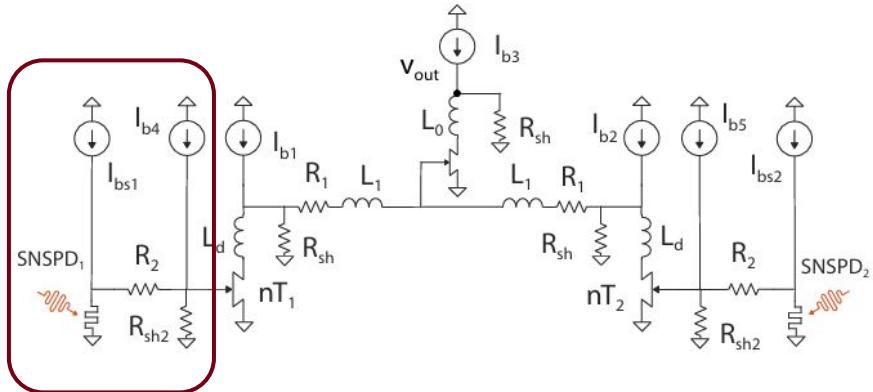
Integration with SNSPDs

Simulations and layout

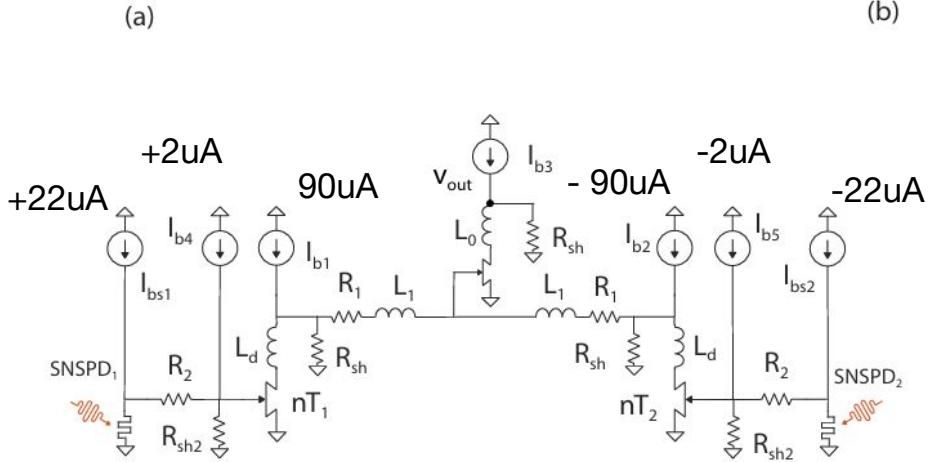
Motivation

- Enable on-chip Bell-state measurements
- Support quantum feedforward operations
- Demonstrate circuit compatibility
- Reduce latency and wiring overhead
- Pave the way for integrated quantum photonic processors

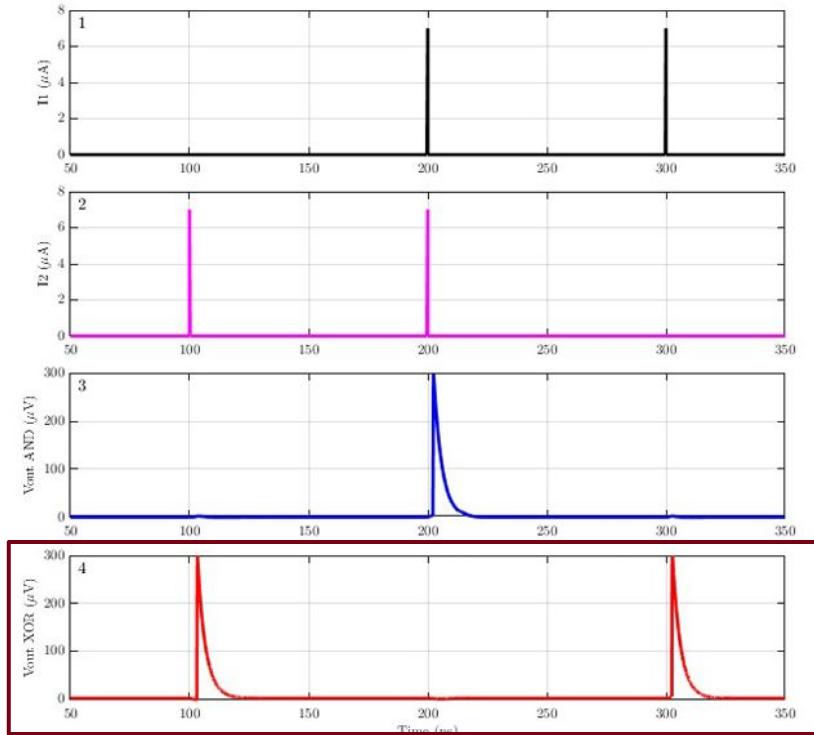
Circuit and simulation



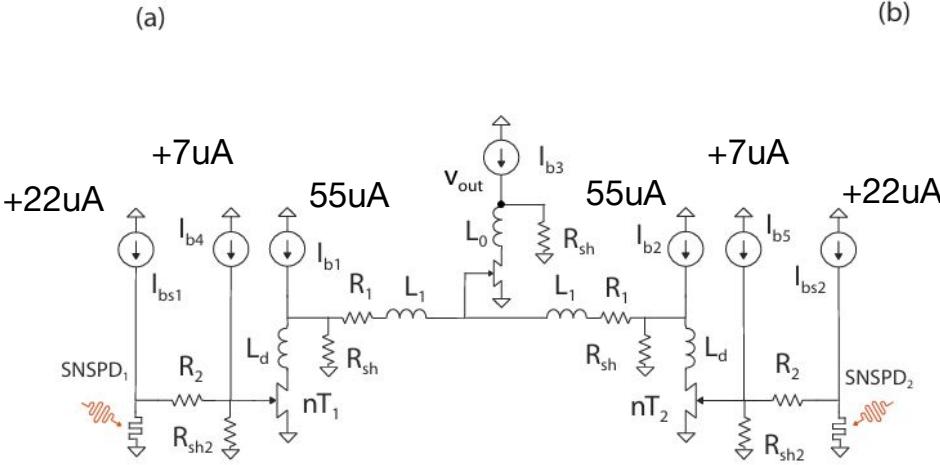
Circuit and simulation - XOR



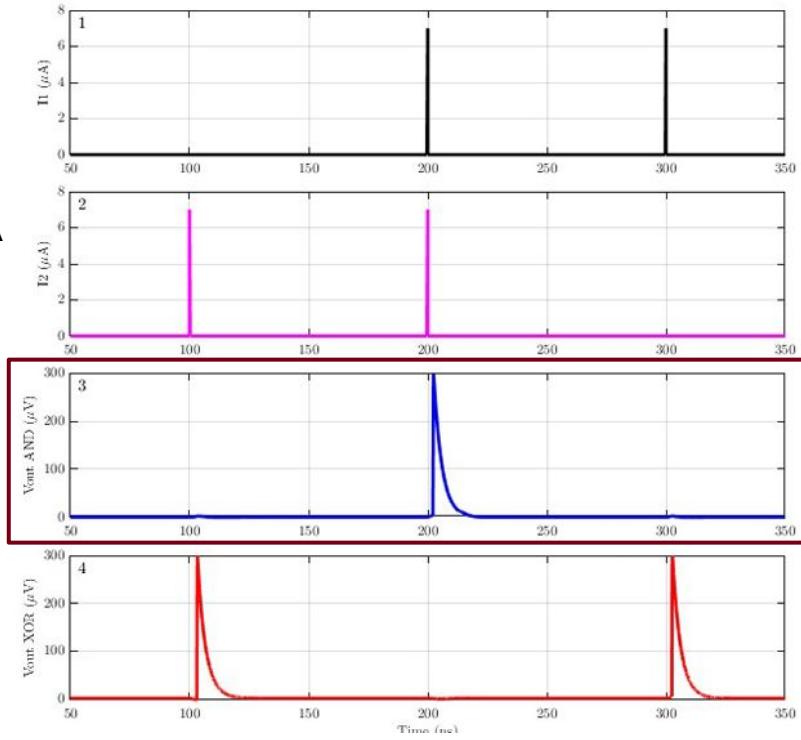
(b)



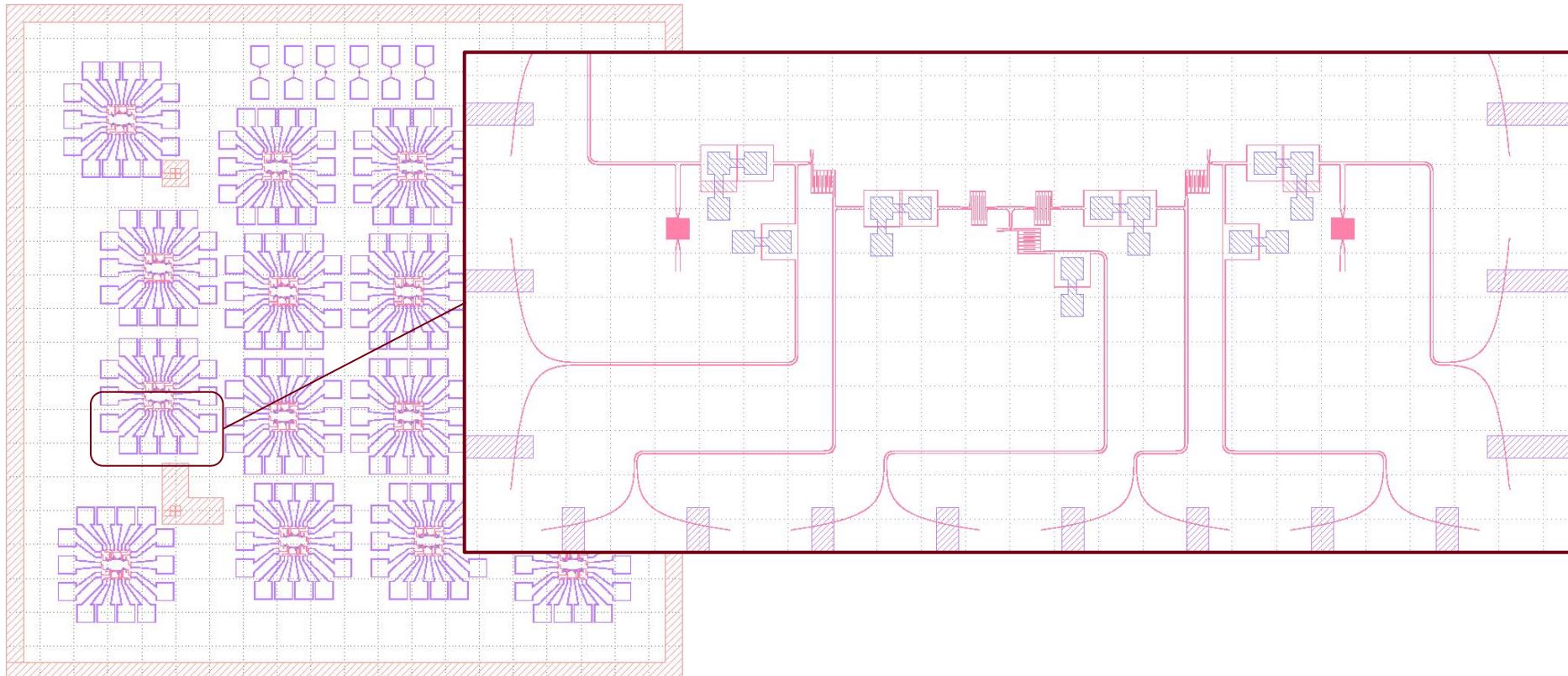
Circuit and simulation - AND



(b)



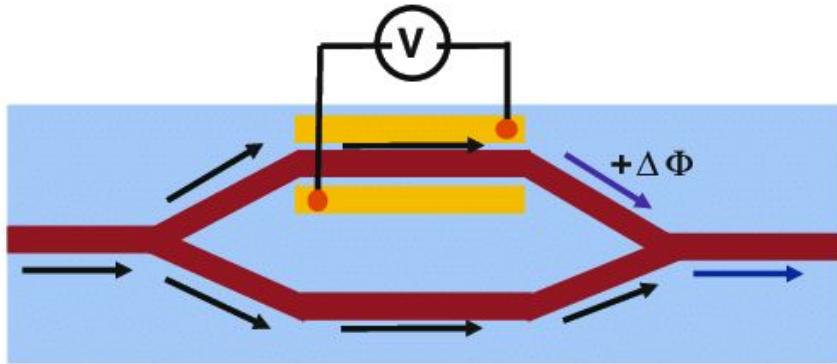
Layout



Photonic Output Interface

nTron driving an E/O Mach-Zehnder modulator

Mach-Zehnder modulator

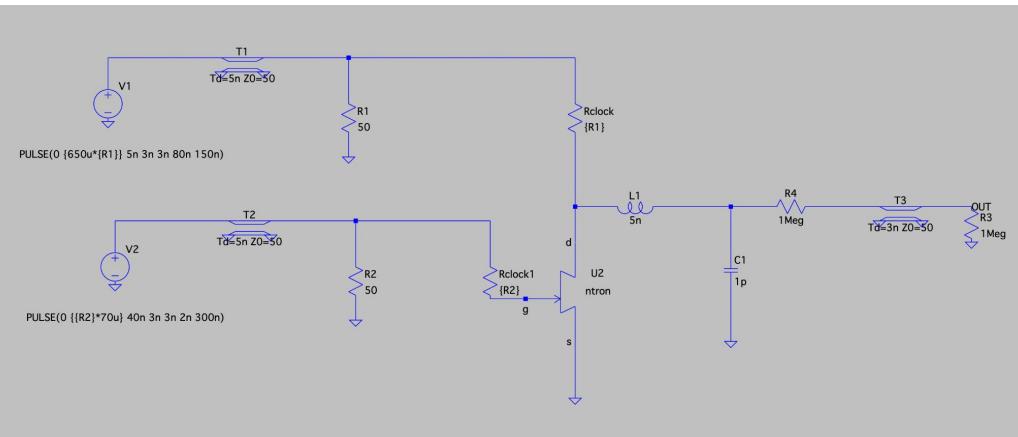


The MZI modulator

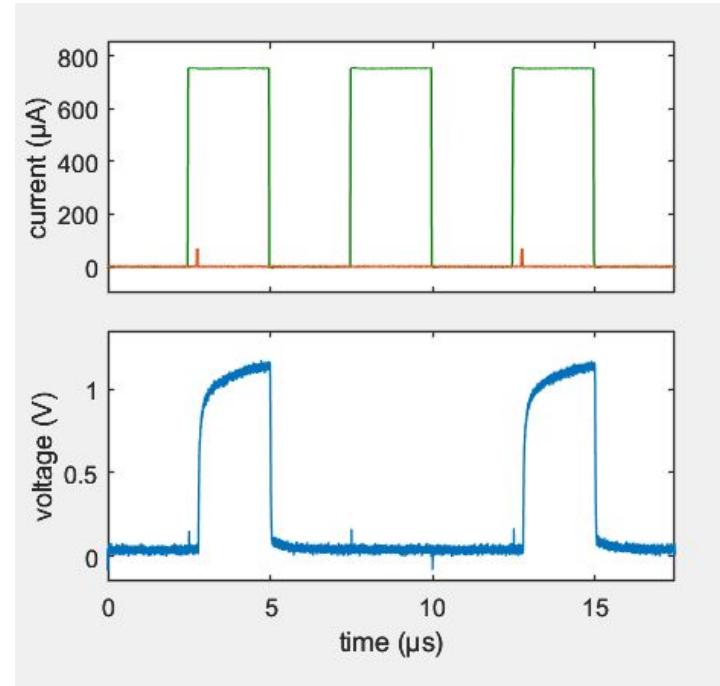
1. Voltage pulse → index change in upper arm
2. Phase delay between arms
3. Interference at output → optical modulation

Objective: The output voltage of the nTron should be large enough to shift the two optical signals by a phase difference of π , causing destructive interference and very low output. This voltage is referred to as $V\pi$.

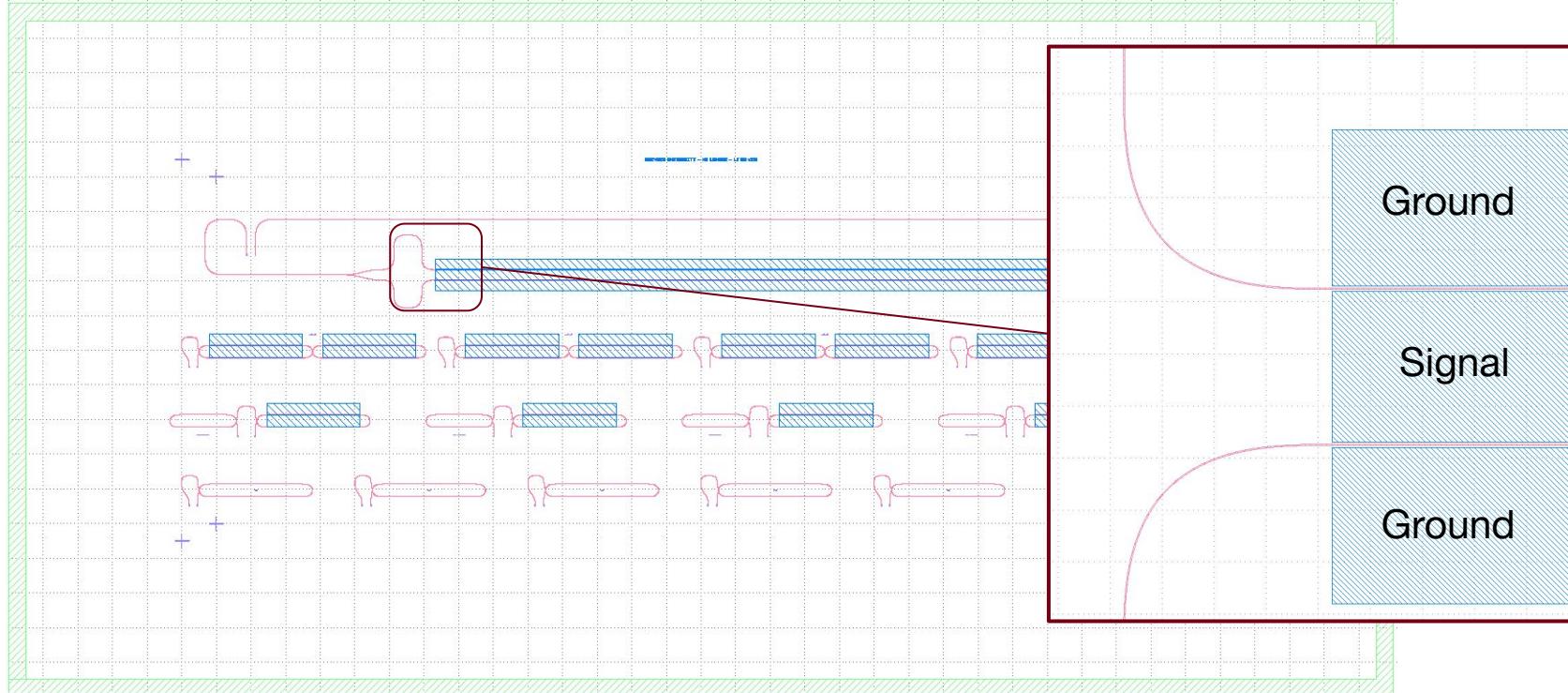
nTron driving a capacitor : simulation and results



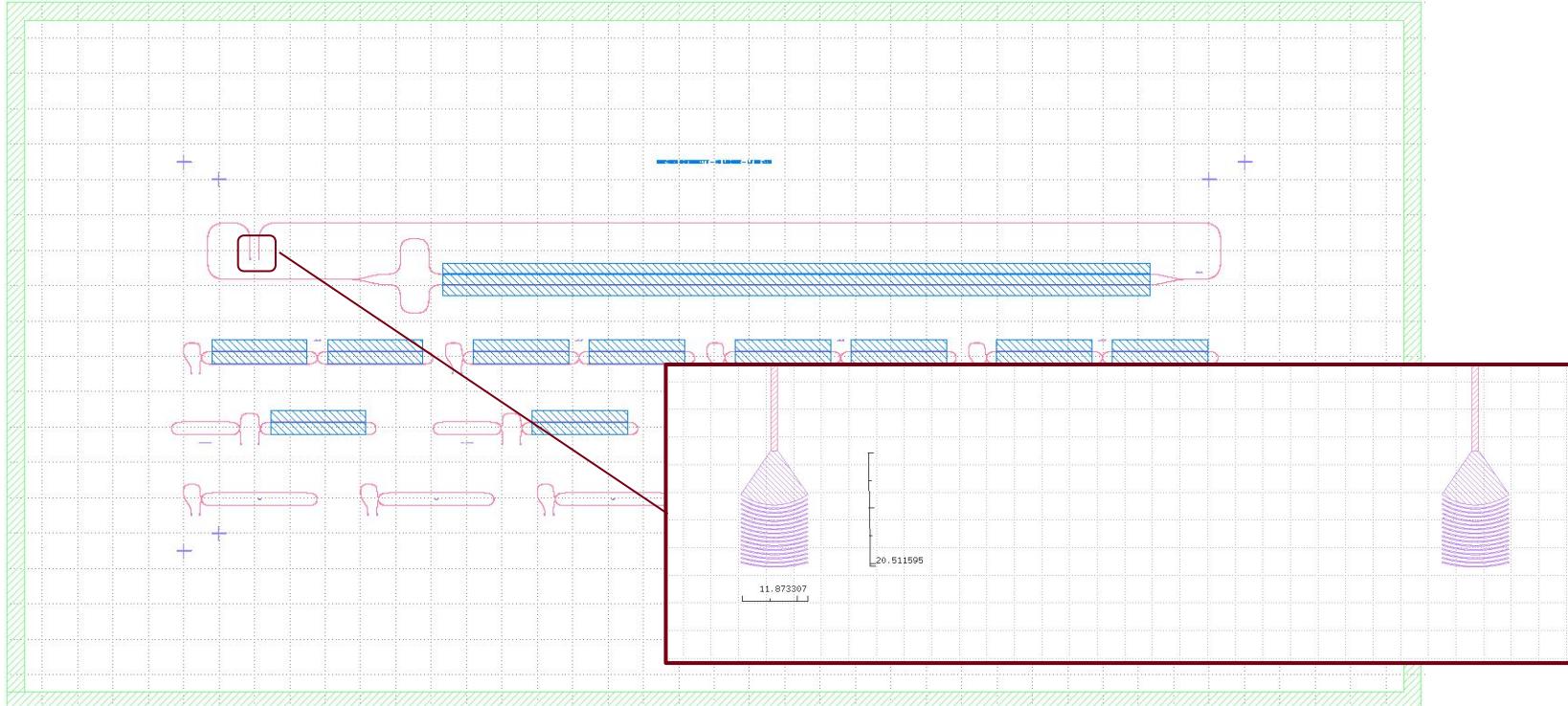
- nTron with a $1.5 \mu\text{m}$ channel and a 200 nm choke
- Capacitor of 1pF to reproduce the modulator electrodes



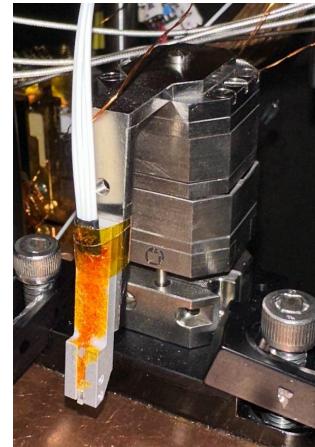
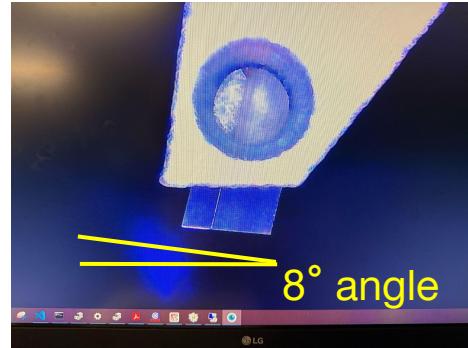
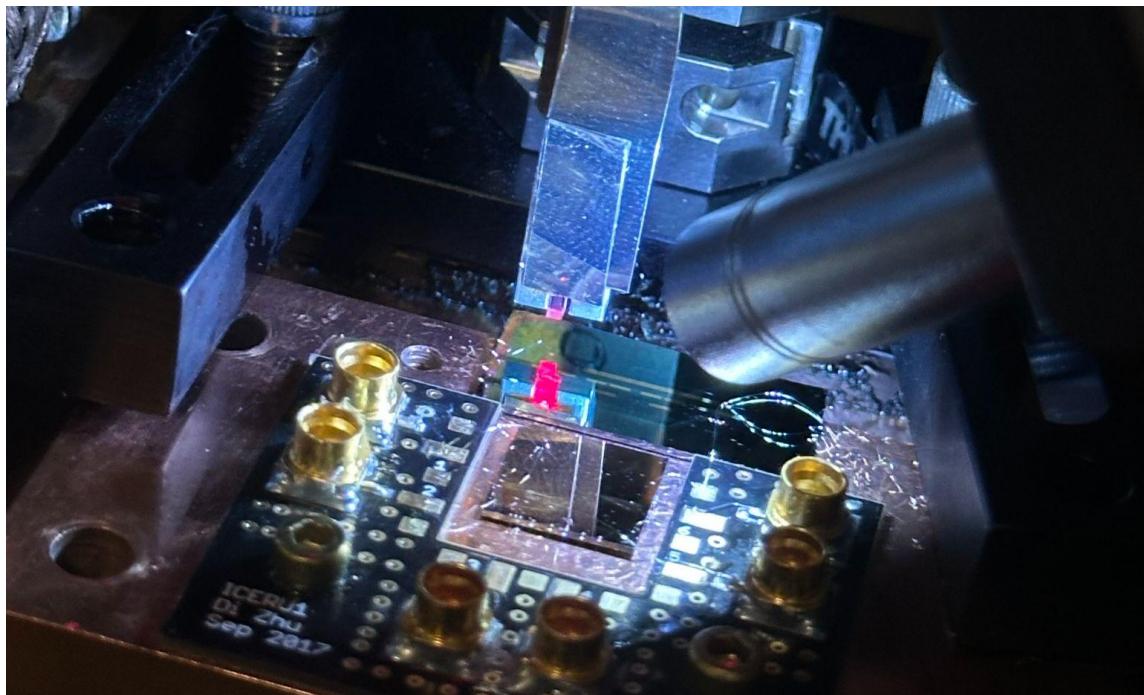
Mach-Zehnder Modulator with GSG electrode configuration



Travelling-Wave Mach-Zehnder Modulator with GSG electrode configuration



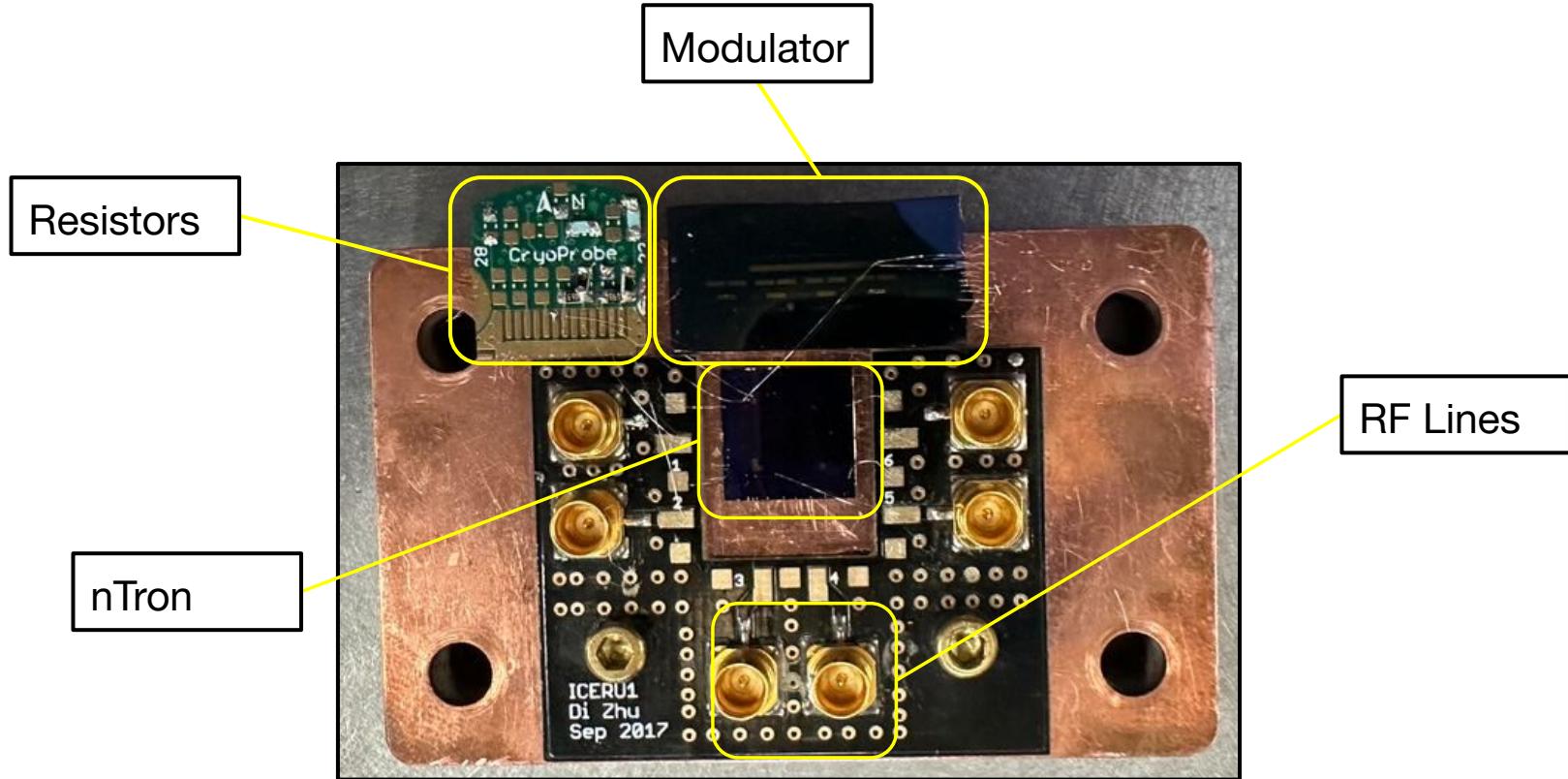
Set-up



Attocube
(x, y, z)

Fiber array

Set-up - ICE



Results - room Temperature

1. $V\pi = 2.4V$ at 1kHz

$$ER(\text{dB}) = 10 \log_{10} \left(\frac{P_{\text{on}}}{P_{\text{off}}} \right)$$

2. Extinction Ratio = 15dB

$$\frac{P_{\text{on}}}{P_{\text{off}}} = 10^{15/10} \approx 31.6$$

Alignment : Fiber array - Grating coupler

The attocube had :

- Big step size
- Different step size depending on the direction, voltage, position
- No absolute position available

→ Algorithm to align the fiber to the coupler

→ Algorithm to keep the fiber aligned while cooling down

Future Work



- Test the chip with SNSPD's
- Try the modulation of an nTron's OUTPUT
- Directly connect the output of the logic Gate to the modulator

Acknowledgements



Quantum Nanostructures and Nanofabrication Group

Thanks for your attention !

Questions are welcome