Design of Micro Power CMOS LNA for Healthcare Applications

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Abstract - **The need for radio frequency (RF) integrated circuits with low power consumption is increasing in wearable devices in healthcare applications. In this paper, it is proposed to design a Low Noise Amplifier (LNA) at 2.4GHz using TSMC 0.13µm CMOS process for RF receiver front-end for ultra low power consumption. Simulation results show 15 dB gain,-13dB return loss,3.6 dB Noise Figure and -24 dBm input 1 dB compression point while consuming 800µW power at a supply voltage of 0.8V. The proposed LNA design saves power, area and cost.**

Keywords: wearable devices, LNA, Power Consumption, RF receiver and CMOS.

I.INTRODUCTION

With the advance in wireless technology, the demand of wearable devices such as biosensor is growing in medical applications like ECG monitoring system. The IEEE 802.15.4 standard supports 2.4 GHz industrial, scientific and Medical (ISM) band for RF transceiver of wearable sensors [1]. As the scaling-down of CMOS technology continues, which extends the operation limit of CMOS circuits for wireless applications and also due to its high integration capability nanoscale CMOS technologies remain a prime candidate for the future developments of ultra-low power (ULP) integrated circuits. Therefore, strong demand for ultra low power RFICs to extend the battery life of the wireless applications has arisen. Being a crucial part in a frontend receiver, the low noise amplifier (LNA) is recognized as one of the most power-consuming components. Traditionally, CMOS LNAs have been designed with MOS transistors operating in strong inversion regime rather than sub-threshold because MOSFETs do not have enough gain, high noise contribution at sub-threshold region and also noise characteristics are very much saturates and not properly modeled for sub-threshold region [2]. The most common topologies of LNA are common source topology and common gate topology. To alleviate shortcomings of common source such as poor isolation between input and output and performance degradation as CMOS technology scales, cascode topology is often used. For sub-mW power consumption, the cascode topology is more suitable with high gain [3]. The proposed LNA is designed using cascode topology using TSMC 0.13µm CMOS technology The proposed LNA operates in moderate inversion region and achieves low power consumption, less area and low cost.

II.MOSFET INVERSION REGIONS

The operation of the MOSFET is typically classified into three modes based on the gate-to-source voltage (V_{GS}): weak, moderate and strong inversion. With various levels of inversion, the I-V characteristics of the MOSFETs are strongly influenced by the bias condition. Typically, distinct expressions of the drain current are required for weak, moderate, and strong inversion to characterize the transistor behavior [4].In subthreshold or weak inversion mode, the gate-source voltage is lower than threshold voltage of the device ($V_{GS}<V_{th}$).The subthreshold current varies exponentially with gate to source voltage V_{GS} as given approximately by

$$I_D = I_{Do} exp\left(\frac{V_{GS}-V_{th}}{nV_T}\right) \quad (1)$$

I_{DO} is the current at $V_{GS}=V_{th}$ and n is the slope factor. V_T is the thermal voltage $V_T = KT/q$

As V_{GS} slightly increases above the threshold voltage V_{th}, it is called as moderate inversion region.As Vgs increases more above the threshold voltage, the drain current is dominated by the carrier drift which leading to strong inversion operation. The saturation current of a MOSFET in strong inversion region is given by [4]

$$I_D = I_{D0}\left\{\ln\left[1+\exp\left(\frac{V_{GS}-V_{th}}{2nV_T}\right)\right]\right\}^2 \quad (2)$$

with

$$I_{D0} = 2\mu_0 C_{0X} n {V_T}^2 \left(\frac{W}{L}\right) \quad (3)$$

For a MOS transistor operating in strong inversion,the drain current as in (2) can be approximated by

$$I_D = \mu_0 C_{0X}\left(\frac{W}{L}\right)\frac{(V_{GS}-V_{th})^2}{2n} \quad (4)$$

To determine the gate-to-source voltage (V_{GS}) range in moderate inversion region, the effective voltage or overdrive voltage (V_{GS}-V_{th}) can be approximated by [5]

$$V_{GS} - V_{th} = 4.6nV_T \quad (5)$$

where n is the weak inversion slope factor with a typical value from 1 to 2. Fig. 1 shows the simulated result of gate-source voltage (V_{GS}) Vs drain current. It is noticed that, gate-to-source voltage (V_{GS}) range in moderate inversion region is from

0.35V to 0.55V. It is observed that drain current of the MOSFET operating from weak to strong inversion with sufficient accuracy. In this paper, moderate inversion region is demonstrated.

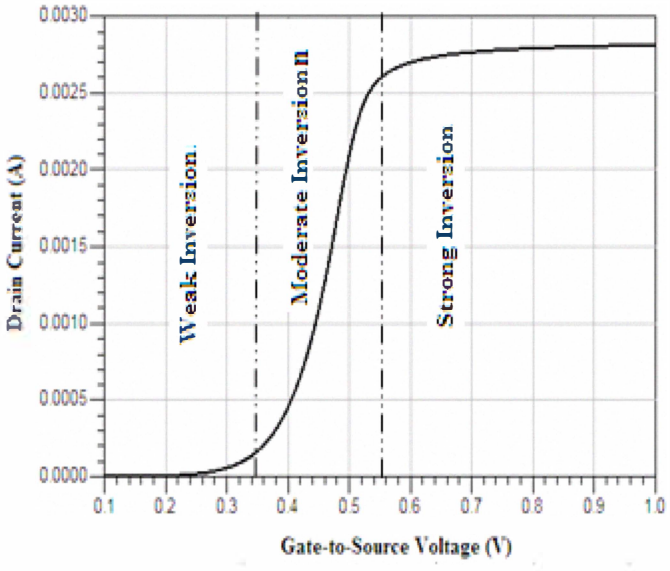

Figure 1. Simulated drain currents of 0.13µm cascode structure of n-channel MOSFET with a fixed V_{DS}

III.CIRCUIT DESIGN

A.Conventional LNA:

The original topology considered is the well-known inductively source degenerated cascode LNA as shown in Fig. 2 [5].In this, L_s adds a real part to the input impedance, while (L_g+L_s) resonates with C_{gs} (gate-source capacitance) of M_1 to provide impedance matching at the operating frequency. Ideally, L_s adds no noise to the system, making this input matching method highly attractive.

The input impedance of the LNA is well known to be [5]

$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega(L_g + L_s) + \left(\frac{g_m}{C_{gs}}\right)L_s \qquad (5)$$

From (5), the input impedance matching to a 50-Ω system can be achieved by

$$\frac{g_m}{C_{gs}}L_s = 50 \qquad (6)$$

and

$$\omega_0 = \frac{1}{\sqrt{(L_s+L_g)C_{gs}}} \qquad (7)$$

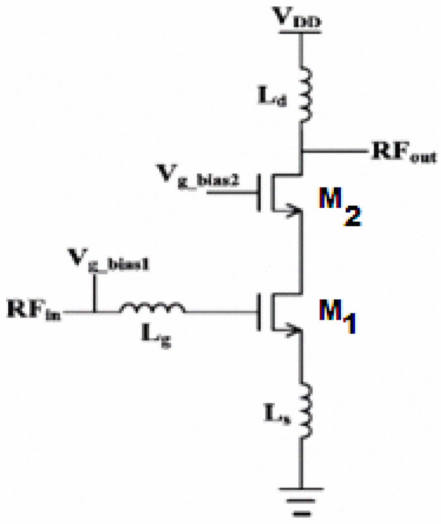

Figure 2.Source Degenerated Cascode LNA

B.Proposed LNA :

Fig.3 shows the proposed LNA.The proposed LNA is designed for low power consumption by making three modifications in the inductively source degenerated cascode LNA. The three main changes are the removal of L_s ,replacing L_d with a resistor and biasing M_1 in the moderate inversion region with a bias voltage of 0.45V and M_2 is biased in the saturation region to take advantage of the low parasitic output capacitance associated with the smaller device size.

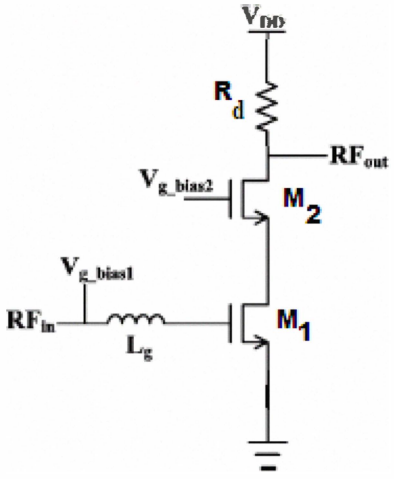

Figure 3. Proposed LNA

For the proposed LNA, the source is matched to the parasitic resistance of L_g. Inductor Lg is used to resonate at a frequency of 2.4GHz and match the input impedance. If this resistance is insufficient, an extra resistor can be added in series with L_g as shown in Fig. 4.

Figure 4. Input Matching Network

In some cases, the spiral inductor is designed to have an equivalent series resistance of 50Ω at the operating frequency, thus achieving input impedance match at the cost of higher noise figure. In this, the IEEE 802.15.4 does not require a low LNA noise figure.

In proposed LNA, the low Q value of six is assumed. L_d is replaced with a load resistor Rd .This is possible because small amount of dc current through the LNA.

The voltage gain is calculated by

$$Gain = g_m Q R_L \tag{8}$$

where

R_L is the load resistance

g_m is the transconductance of the device

Q factor is normally between 4 to 7

C.Small Signal Characteristics :

To have a better understanding on the noise matching , the small signal equivalent circuit of input stage of proposed LNA is depicted in Fig 4.where v_{ns} and Z_s indicate the Thevenin's equivalent circuit seen from the MOS transistor to the source terminal, and $\overline{i_{ng}^2}$ and $\overline{i_{nd}^2}$ represent the mean-square values of the gate-induced and channel noise currents, respectively.

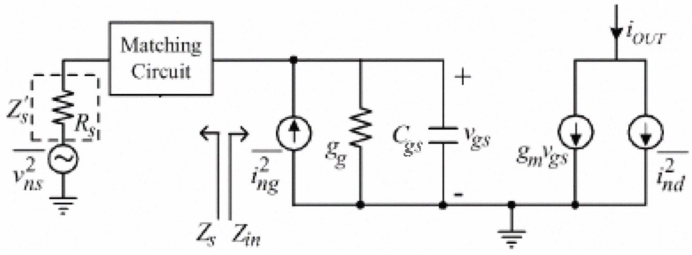

Figure 5. Small signal equivalent circuit of a proposed LNA

The expressions of the noise currents are given by

$$\overline{i_{ng}^2} = 4kT\,\delta g_g \Delta f \tag{10}$$

$$\overline{i_{nd}^2} = 4kT\,\gamma g_{d0} \Delta f \tag{11}$$

where δ and γ have typical values of 4/3 and 2/3 respectively. Note that g_g is given by

$$g_g = \frac{\omega^2 C_{gs1}^2}{5 g_{d0}} \tag{12}$$

where g_{d0} is the zero-bias drain conductance.

Since the gate-induced noise current has a correlation with the channel noise current, a correlation coefficient is defined as follows

$$C = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}} \cdot \sqrt{\overline{i_{nd}^2}}} \tag{13}$$

The minimum noise factor F_{min} are expressed as [6],[7]

$$F_{min} = 1 + \frac{2\omega_0}{\sqrt{5}\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \tag{14}$$

Using this formula ,minimum noise figure F_{min} can be found.

IV.SIMULATION RESULTS

The proposed LNA is simulated in ADS (Advanced Design System) using TSMC 0.13µm CMOS technology and Fig. 6 shows the voltage gain ,S21 of 15dB in the 2.4GHz band and S11 of -13dB provides a good input impedance matching to 50Ω Fig. 7 shows the Noise Figure nf(2) is 3.6dB. 1dB compression point of -24dBm is calculated using gain compression which is available in the simulator ADS as shown in Fig 8. This circuit consumes 800µW power from a 0.8V supply as shown in Fig. 9.

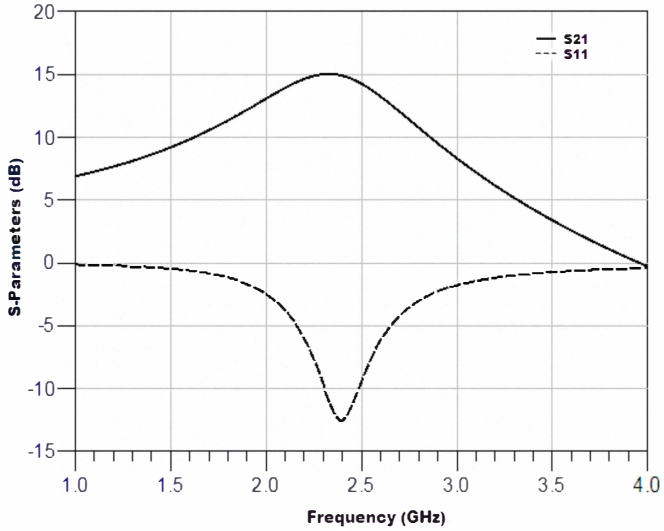

Figure 6. S-Parameters

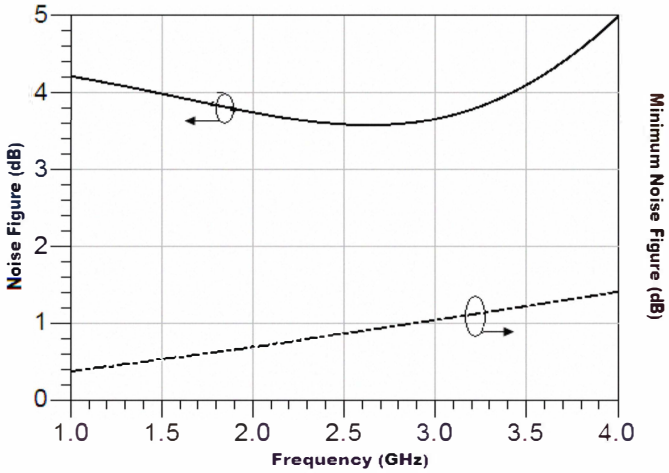

Figure 7.Noise Figure and Minimum Noise Figure

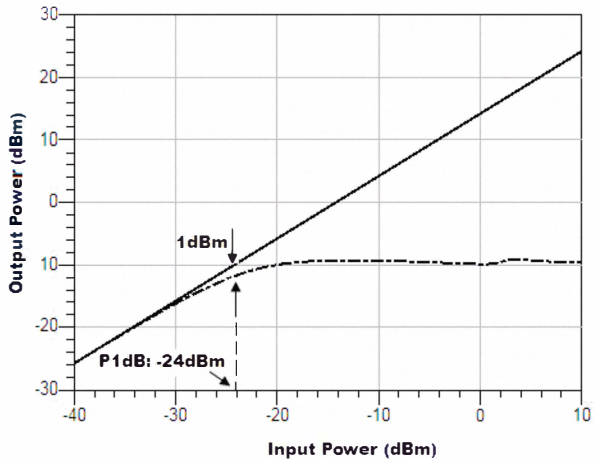

Figure 8. Simulated 1-dB Compression Point

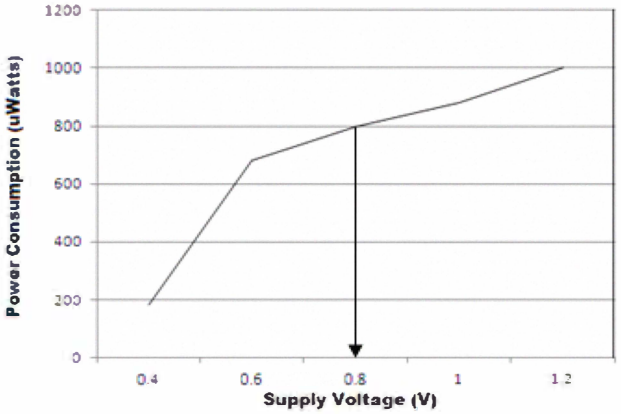

Figure 9.Power Consumption variation with supply voltage and bias current is maintained at 1mA

Table 1. shows the performance comparison of proposed LNA with the Previous works.

TABLE1

PERFORMANCE COMPARISON OF LNAS

	Units	Proposed work	[11]	[12]	[13]*
Technology	µm	0.13	0.35	0.18	.13
Supply Voltage	V	.8	3	1	.6
S(2,1)	dB	15	18	33	9.1
S(1,1)	dB	-14	-	-	-13
Noise Figure	dB	3.6	3.5	5.7	4.7
Pin1dB	dBm	-24	-13	-	-25
Power Consumption	mW	0.8	13.2	1.2	0.4

* subthreshold LNA

Weak inversion region achieved high noise figure and moderate gain and also noise model is not properly modeled in this region. So many circuit designers were not preferred weak inversion region. Strong inversion region attained good gain but is not suitable for low power consumption. It is inferred that, moderate inversion have the best trade-offs between gain, noise figure, frequency response and power consumption.

V.CONCLUSION

The design of LNA with microwatts power consumption based on moderate inversion region is presented with tradeoff between gain, noise, linearity and power consumption. The moderate inversion region is achieved low power consumption with high gain. The designed LNA gives required performance for the application with 800uW power consumption. It occupies very less area because of using only one inductor and low cost by using CMOS technology.

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