



## 1. Description

### 1.1. Project

Project Name	dash
Board Name	custom
Generated with:	STM32CubeMX 6.14.0
Date	08/31/2025

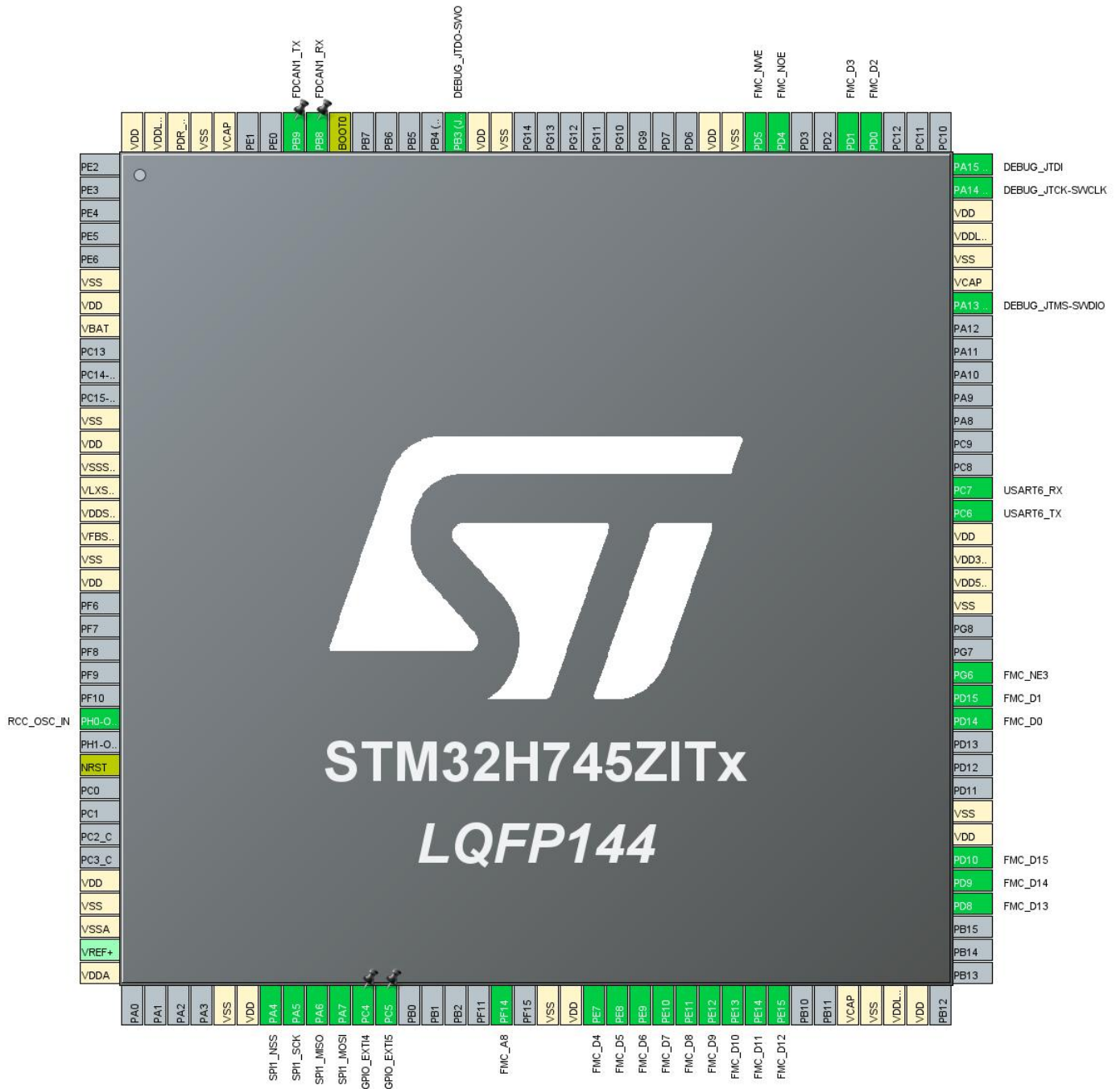
### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H745ZITx
MCU Package	LQFP144
MCU Pin number	144

### 1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4
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## 2. Pinout Configuration



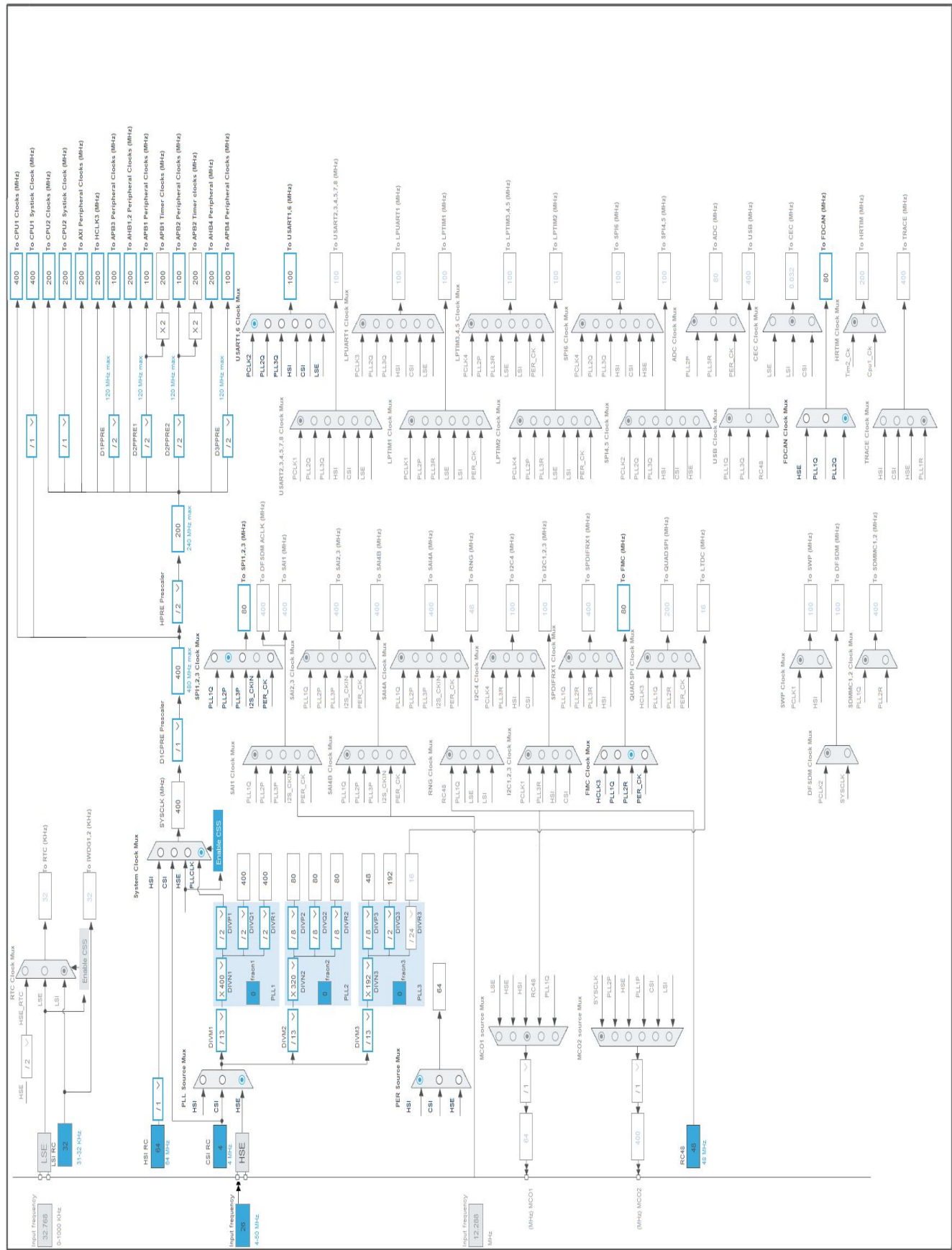
### 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VSS	Power		
7	VDD	Power		
8	VBAT	Power		
12	VSS	Power		
13	VDD	Power		
14	VSSSMPS	Power		
15	VLXSMPS	Power		
16	VDDSMPS	Power		
17	VFBSMPS	Power		
18	VSS	Power		
19	VDD	Power		
25	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
27	NRST	Reset		
32	VDD	Power		
33	VSS	Power		
34	VSSA	Power		
36	VDDA	Power		
41	VSS	Power		
42	VDD	Power		
43	PA4	I/O	SPI1_NSS	
44	PA5	I/O	SPI1_SCK	
45	PA6	I/O	SPI1_MISO	
46	PA7	I/O	SPI1_MOSI	
47	PC4	I/O	GPIO_EXTI4	
48	PC5	I/O	GPIO_EXTI5	
53	PF14	I/O	FMC_A8	
55	VSS	Power		
56	VDD	Power		
57	PE7	I/O	FMC_D4	
58	PE8	I/O	FMC_D5	
59	PE9	I/O	FMC_D6	
60	PE10	I/O	FMC_D7	
61	PE11	I/O	FMC_D8	
62	PE12	I/O	FMC_D9	
63	PE13	I/O	FMC_D10	
64	PE14	I/O	FMC_D11	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
65	PE15	I/O	FMC_D12	
68	VCAP	Power		
69	VSS	Power		
70	VDDLDO	Power		
71	VDD	Power		
76	PD8	I/O	FMC_D13	
77	PD9	I/O	FMC_D14	
78	PD10	I/O	FMC_D15	
79	VDD	Power		
80	VSS	Power		
84	PD14	I/O	FMC_D0	
85	PD15	I/O	FMC_D1	
86	PG6	I/O	FMC_NE3	
89	VSS	Power		
90	VDD50_USB	Power		
91	VDD33_USB	Power		
92	VDD	Power		
93	PC6	I/O	USART6_TX	
94	PC7	I/O	USART6_RX	
102	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
103	VCAP	Power		
104	VSS	Power		
105	VDDLDO	Power		
106	VDD	Power		
107	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
108	PA15 (JTDI)	I/O	DEBUG_JTDI	
112	PD0	I/O	FMC_D2	
113	PD1	I/O	FMC_D3	
116	PD4	I/O	FMC_NOE	
117	PD5	I/O	FMC_NWE	
118	VSS	Power		
119	VDD	Power		
128	VSS	Power		
129	VDD	Power		
130	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
135	BOOT0	Boot		
136	PB8	I/O	FDCAN1_RX	
137	PB9	I/O	FDCAN1_TX	
140	VCAP	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
141	VSS	Power		
142	PDR_ON	Power		
143	VDDLDO	Power		
144	VDD	Power		

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H745ZITx
Datasheet	DS12923_Rev1

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1



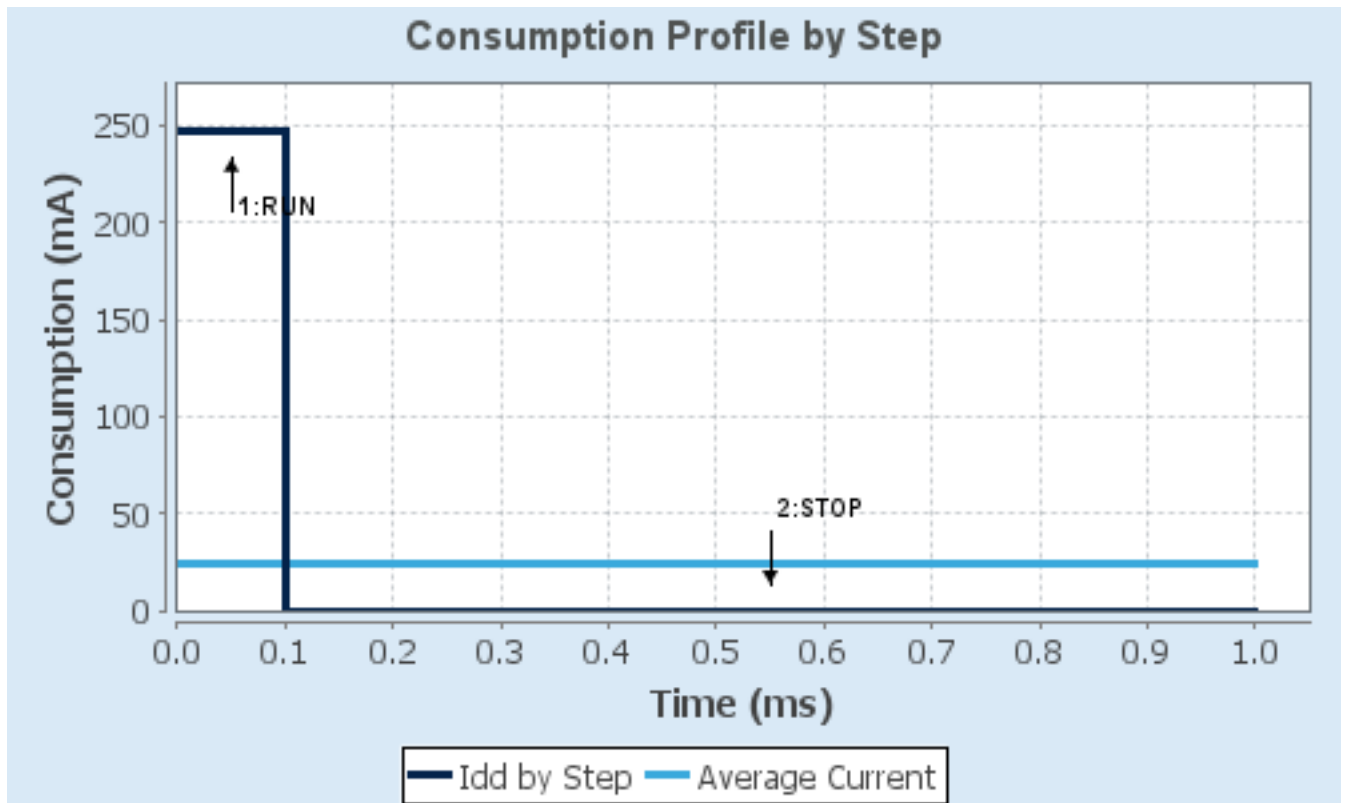
## 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0	SVOS5: System-Scale5
<b>D1 Mode</b>	DRUN/CRUN	DSTANDBY
<b>D2 Mode</b>	DRUN/CRUN	DSTANDBY
<b>D3 Mode</b>	DRUN	DSTOP
<b>Fetch Type</b>	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
<b>CM7 Frequency</b>	480 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL ALL IPs ON	LSE Flash-ON
<b>CM4 Frequency</b>	240 MHz	0 Hz
<b>Clock Source Frequency</b>	25 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	247 mA	145 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	1027.0	0.0
<b>Category</b>	In DS Table	In DS Table

## 1.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

## 1.6. Chart



## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	dash
Project Folder	C:\Users\ramga\Desktop\projects\dash
Toolchain / IDE	EWARM V8.50
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	M4-0x200
Minimum Stack Size	M4-0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_CRC_Init	CRC
4	MX_DMA2D_Init	DMA2D
5	MX_FMC_Init	FMC

### 2.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO

Rank	Function Name	Peripheral Instance Name
2	MX_FDCAN1_Init	FDCAN1
3	MX_SPI1_Init	SPI1
4	MX_USART6_UART_Init	USART6

## 3. Peripherals and Middlewares Configuration

### 3.1. CORTEX\_M4

#### 3.1.1. Parameter Settings:

##### Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

##### Cortex Memory Protection Unit Control Settings:

MPU Control Mode	Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers *
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##### Cortex Memory Protection Unit Region 0 Settings:

MPU Region	Disabled
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##### Cortex Memory Protection Unit Region 1 Settings:

MPU Region	Disabled
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##### Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled
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##### Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled
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##### Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled
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##### Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled
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##### Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled
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##### Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled
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### 3.2. CORTEX\_M7

#### 3.2.1. Parameter Settings:

##### Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

### Speculation default mode Settings:

Speculation default mode **Enabled \***

### Cortex Interface Settings:

CPU ICache Disabled

CPU DCache Disabled

### Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers

### Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled

MPU Region Base Address **0x0 \***

MPU Region Size 4GB

MPU SubRegion Disable **0x87 \***

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE

MPU Shareability Permission ENABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

### Cortex Memory Protection Unit Region 1 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 2 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 10 Settings:

MPU Region Disabled

### Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

**Cortex Memory Protection Unit Region 12 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 13 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 14 Settings:**

MPU Region Disabled

**Cortex Memory Protection Unit Region 15 Settings:**

MPU Region Disabled

### 3.3. CRC

**mode: Activated**

#### 3.3.1. Parameter Settings:

**Core(s) Settings:**

Context(s): Cortex-M7

Initialized Context: Cortex-M7

Power Domain: D3

**Basic Parameters:**

Default Polynomial State Enable

Default Init Value State Enable

**Advanced Parameters:**

Input Data Inversion Mode None

Output Data Inversion Mode Disable

Input Data Format Bytes

### 3.4. DEBUG

**Debug: JTAG (4 pins)**

#### 3.4.1. Core(s) Settings:

Context(s): Cortex-M4

Initialized Context: Cortex-M4

Power Domain:

### 3.5. DMA2D

**mode: Activated**

#### 3.5.1. Parameter Settings:

##### **Core(s) Settings:**

Context(s): Cortex-M7  
 Initialized Context: Cortex-M7  
 Power Domain: D1

##### **Basic Parameters:**

Transfer Mode Memory to Memory  
 Color Mode ARGB8888  
 Output Offset 0

##### **Foreground layer Configuration:**

DMA2D Input Color Mode ARGB8888  
 DMA2D ALPHA MODE No modification of the alpha channel value  
 Input Alpha 0  
 Input Offset 0  
 DMA2D ALPHA Inversion Regular Alpha  
 DMA2D Red and Blue swap Regular mode (RGB or ARGB)  
 DMA2D Chroma Sub-Sampling Mode No chroma sub-sampling 4:4:4

### 3.6. FDCAN1

**mode: Activated**

#### 3.6.1. Parameter Settings:

##### **Core(s) Settings:**

Context(s): Cortex-M4  
 Initialized Context: Cortex-M4  
 Power Domain: D2

##### **Basic Parameters:**

Frame Format **FD mode without BitRate Switching \***  
 Mode Normal mode  
 Auto Retransmission Disable  
 Transmit Pause Disable  
 Protocol Exception Disable



Nominal Sync Jump Width	1
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0
Std Filters Nbr	0
Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

#### **Clock Calibration Unit:**

Clock Calibration	Disable
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#### **Bit Timings Parameters:**

Nominal Prescaler	16
Nominal Time Quantum	<b>200.0 *</b>
Nominal Time Seg1	1
Nominal Time Seg2	1
Nominal Time for one Bit	<b>600 *</b>
Nominal Baud Rate	<b>1666666 *</b>

### **3.7. FMC**

NOR Flash/PSRAM/SRAM/ROM/LCD 1

**Chip Select: NE3**

**Memory type: LCD Interface**

**LCD Register Select: A8**

**Data: 16 bits**

3.7.1. NOR/PSRAM 1:

#### **Core(s) Settings:**

Context(s):

	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1
<b>NOR/PSRAM control:</b>	
Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 3
Write operation	Enabled
Write FIFO	Enabled
Extended mode	Disabled
<b>NOR/PSRAM timing:</b>	
Address setup time in FMC clock cycles	15
Data setup time in FMC clock cycles	255
Bus turn around time in FMC clock cycles	15

### 3.7.2. Bank Mapping:

<b>Core(s) Settings:</b>	
Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1
<b>Mapping parameters:</b>	
FMC bank mapping	Default mapping

## 3.8. RCC

### High Speed Clock (HSE): BYPASS Clock Source

#### 3.8.1. Parameter Settings:

<b>Core(s) Settings:</b>	
Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3
<b>Power Parameters:</b>	
SupplySource	<b>PWR_LDO_SUPPLY *</b>
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

#### RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

#### System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Product revision	rev.V

#### PLL range Parameters:

PLL1 clock Input range	Between 2 and 4 MHz
PLL2 input frequency range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

### 3.9. SPI1

#### Mode: Full-Duplex Master

#### Hardware NSS Signal: Hardware NSS Input Signal

##### 3.9.1. Parameter Settings:

#### Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

#### Basic Parameters:

Frame Format	Motorola
Data Size	<b>8 Bits *</b>
First Bit	MSB First

#### Clock Parameters:

Prescaler (for Baud Rate)	<b>16 *</b>
Baud Rate	<b>5.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

#### Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled

NSS Signal Type	Input Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.10. SYS\_M4

**Timebase Source: SysTick**

#### 3.10.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

### 3.11. SYS

**Timebase Source: SysTick**

#### 3.11.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

### 3.12. USART6

**Mode: Asynchronous**

#### 3.12.1. Parameter Settings:

##### **Core(s) Settings:**

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4

Power Domain:

D2

**Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

**Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a		Cortex-M4	Cortex-M4
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a		Cortex-M4	Cortex-M4
	PA15 (JTDI)	DEBUG_JTDI	n/a	n/a	n/a		Cortex-M4	Cortex-M4
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a		Cortex-M4	Cortex-M4
FDCAN1	PB8	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
	PB9	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
FMC	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PG6	FMC_NE3	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7	D1
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
SPI1	PA4	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M4	D2
GPIO	PC4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PC5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4

\* Initialized context

## 4.2. DMA configuration

nothing configured in DMA service

## 4.3. BDMA configuration

nothing configured in DMA service

#### **4.4. MDMA configuration**

nothing configured in DMA service



## 4.5. NVIC configuration

### 4.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line4 interrupt	unused		
EXTI line[9:5] interrupts	unused		
CM4 send event interrupt for CM7	unused		
FPU global interrupt	unused		
DMA2D global interrupt	unused		
HSEM1 global interrupt	unused		
Hold core interrupt	unused		

### 4.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

### 4.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0

Interrupt Table	Enable	Preenmption Priority	SubPriority
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
EXTI line4 interrupt	unused		
FDCAN1 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
EXTI line[9:5] interrupts	unused		
SPI1 global interrupt	unused		
FDCAN calibration unit interrupt	unused		
CM7 send event interrupt for CM4	unused		
USART6 global interrupt	unused		
FPU global interrupt	unused		
HSEM2 global interrupt	unused		
Hold core interrupt	unused		

#### 4.5.4. NVIC2 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

\* User modified value

## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

**Category view**   Context Execution view   Context Initialization view   Power Domain view

Choose filters ...

... by Context Execution: ☐ Cortex-M7 ☐ Cortex-M4

... by Context Initialization: ☐ Cortex-M7 ☐ Cortex-M4 ☒ None

... by Power Domain: ☐ D1 ☐ D2 ☐ D3 ☒ None

Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Utilities	Other
BDMA			FDCAH1 ✓	DMA2D ✓		CRC ✓	DEBUG ✓			
CORTEX_M4 ✓			FMC ✓							
CORTEX_M7 ✓			SP11 ✓							
DMA			USART6 ✓							
GPIO ✓										
MDMA										
IVVIC1 ✓										
IVVIC2 ✓										
RCC ✓										
SYS_M4 ✓										
SYS_M7 ✓										

### 5.1.2. Without filters

**Category view**   Context Execution view   Context Initialization view   Power Domain view

Choose filters ...

... by Context Execution: ☐ Cortex-M7 ☐ Cortex-M4

... by Context Initialization: ☐ Cortex-M7 ☐ Cortex-M4 ☒ None

... by Power Domain: ☐ D1 ☐ D2 ☐ D3 ☒ None

#### Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Utilities	Other
BDMA			FDCAH1 ✓	DMA2D ✓		CRC ✓	DEBUG ✓			
CORTEX_M4 ✓			FMC ✓							
CORTEX_M7 ✓			SP11 ✓							
DMA			USART6 ✓							
GPIO ✓										
MDMA										
IVVIC1 ✓										
IVVIC2 ✓										
RCC ✓										
SYS_M4 ✓										
SYS_M7 ✓										

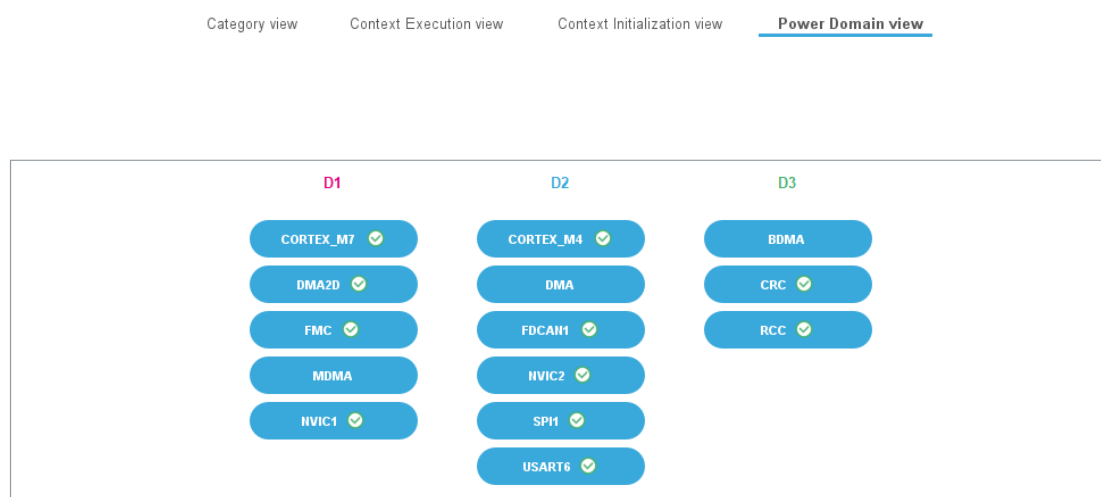
## 5.2. Context Execution view



### 5.3. Context Initialization view



## 5.4. Power Domain view



## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h7_bsdI.zip">https://www.st.com/resource/en/bsdl_model/stm32h7_bsdI.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32h7-svd.zip">https://www.st.com/resource/en/svd/stm32h7-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
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Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/brstm32h7.pdf">https://www.st.com/resource/en/brochure/brstm32h7.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32h7rs.pdf">https://www.st.com/resource/en/flyer/flstm32h7rs.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf">https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-">https://www.st.com/resource/en/application_note/an1709-emc-design-</a>



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- Application Notes [https://www.st.com/resource/en/application\\_note/an5690-how-to-use-vrefbuf-peripheral-on-stm32-mcus-and-mpus-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an5690-how-to-use-vrefbuf-peripheral-on-stm32-mcus-and-mpus-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an4230-introduction-to-random-number-generation-validation-using-the-nist-statistical-test-suite-for-stm32-mcus-and-mpus-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4230-introduction-to-random-number-generation-validation-using-the-nist-statistical-test-suite-for-stm32-mcus-and-mpus-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an2867-guidelines-for-oscillator-design-on-stm8afals-and-stm32-mcus-mpus-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an2867-guidelines-for-oscillator-design-on-stm8afals-and-stm32-mcus-mpus-stmicroelectronics.pdf)
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- Application Notes [https://www.st.com/resource/en/application\\_note/an4277-how-to-use-pwm-shutdown-for-motor-control-and-digital-power-conversion-on-stm32-mcus-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4277-how-to-use-pwm-shutdown-for-motor-control-and-digital-power-conversion-on-stm32-mcus-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an4635-how-to-optimize-lpuart-power-consumption-on-stm32-mcus-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4635-how-to-optimize-lpuart-power-consumption-on-stm32-mcus-stmicroelectronics.pdf)
- Application Notes [https://www.st.com/resource/en/application\\_note/an4759-introduction-to-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-mcus-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4759-introduction-to-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-mcus-stmicroelectronics.pdf)

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