PRESENTATION

on

INPUT/OUTPUT PORT

BY-:

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INPUT/OUTPUT PORT

I/O port are basically interface needed for communication between processor and I/O device.

- These are of two types:-

1. Non programmable
2. programmable

NON-PROGRAMMABLE I/O PORT

These are fixed port which work either as input or output port only and there function cannot be changed and its example is Intel 8212

PROGRAMMABLE I/O PORT

Programmable I/O port is a multi port device which can be programmed to work in variety of ways as user likes. e.g. Intel 8255

INTEL 8255

The Intel 8255 Programmable Peripheral Interface (PPI) chip is a peripheral chip originally developed for the Intel 8085 microprocessor. It contains Three programmable port Ports-> Port A, Port B, Port C. The port C can be further divided into two ports of 4-bits each :- Port C_{UPPER}, Port C_{LOWER}
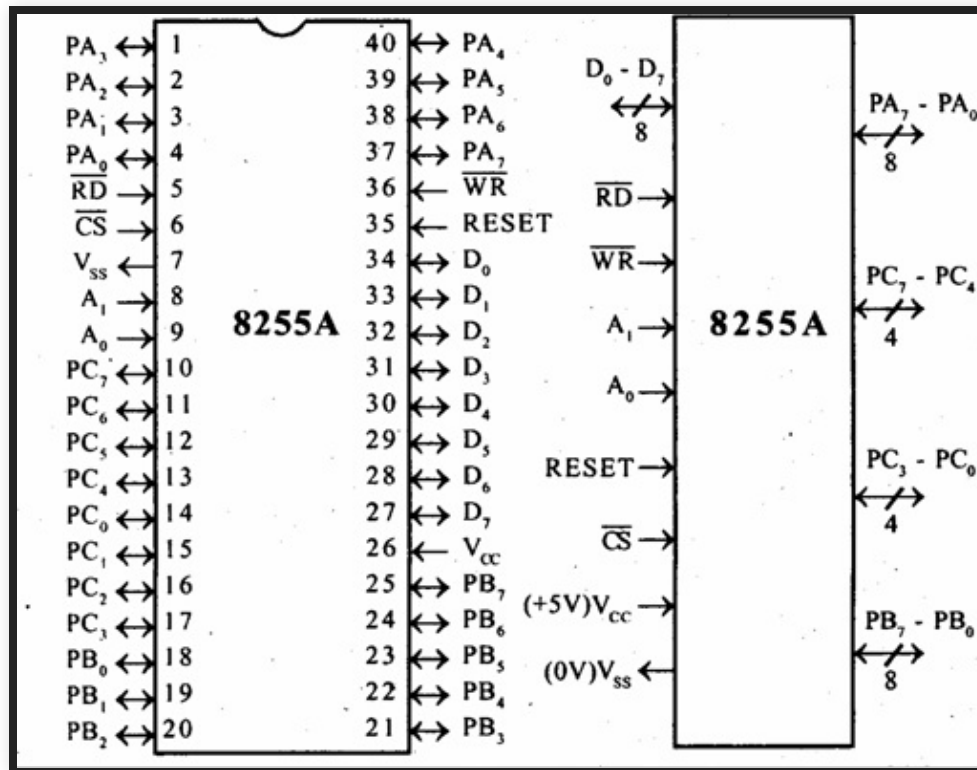
MODES

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The 8255 operates in three modes -:
Mode 0 -: all operate as simple I/O port
Mode 1 -: Port A,B operate as strobed I/O Port and Port C
          act as control word.
Mode 2 -: Port A operates as strobed bi-directional Port
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8255A

Left side (pins 1–20):
- PA3 ↔ 1
- PA2 ↔ 2
- PA1 ↔ 3
- PA0 ↔ 4
- $\overline{RD}$ → 5
- $\overline{CS}$ → 6
- Vss ← 7
- A1 → 8
- A0 → 9
- PC7 ↔ 10
- PC6 ↔ 11
- PC5 ↔ 12
- PC4 ↔ 13
- PC0 ↔ 14
- PC1 ↔ 15
- PC2 ↔ 16
- PC3 ↔ 17
- PB0 ↔ 18
- PB1 ↔ 19
- PB2 ↔ 20

Right side (pins 40–21):
- 40 ↔ PA4
- 39 ↔ PA5
- 38 ↔ PA6
- 37 ↔ PA7
- 36 ← $\overline{WR}$
- 35 ← RESET
- 34 ↔ D0
- 33 ↔ D1
- 32 ↔ D2
- 31 ↔ D3
- 30 ↔ D4
- 29 ↔ D5
- 28 ↔ D6
- 27 ↔ D7
- 26 ← Vcc
- 25 ↔ PB7
- 24 ↔ PB6
- 23 ↔ PB5
- 22 ↔ PB4
- 21 ↔ PB3

8255A (block diagram)
- D0 - D7 ↔ /8
- $\overline{RD}$ →
- $\overline{WR}$ →
- A1 →
- A0 →
- RESET →
- $\overline{CS}$ →
- (+5V)Vcc →
- (0V)Vss ←
- PA7 - PA0 ↔ /8
- PC7 - PC4 ↔ /4
- PC3 - PC0 ↔ /4
- PB7 - PB0 ↔ /8

```
Programmer make use of control word that defines which
port will act as an input or output.
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SERIAL DATA TRANSFER

Serial data transfer refers to the transfer of only one bit at a time. This is done for cost efficiency. Serial data can be transmitted in two modes:

1 Asynchronous Mode

2 Synchronous Mode

Synchronous Data Transmission

- The transmitter and receiver are synchronized.
  - A sequence of synchronization signals is sent before the communication begins.

- Usually used for high speed transmission.
  - More than 20 K bits/sec.

- Message based.
  - Synchronization occurs at the beginning of a long message.

Asynchronous Data Transmission

- Transmission occurs at any time.

- Character based.
  - Each character is sent separately.

- Generally used for low speed transmission.
  - Less the 20 K bits/sec.

Asynchronous Data Transmission

- Follows agreed upon standards:
  - The line is normally at logic one (mark).
    - Logic 0 is known as space.
  - The transmission begins with a start bit (low).
  - Then the seven or eight bits representing the character are transmitted.
  - The transmission is concluded with one or two stop bits.
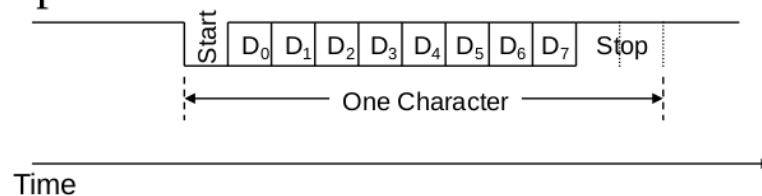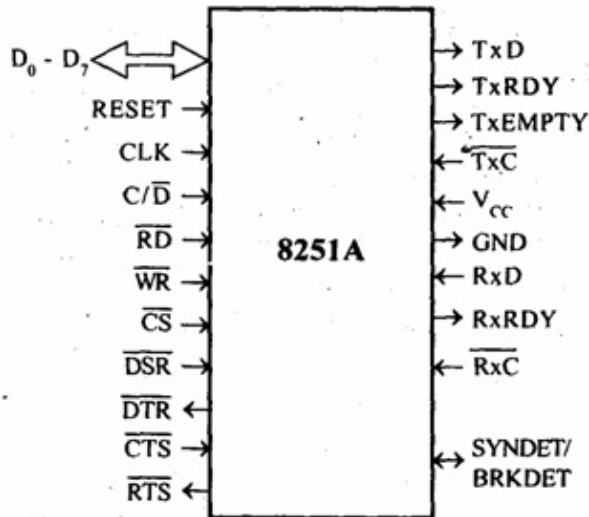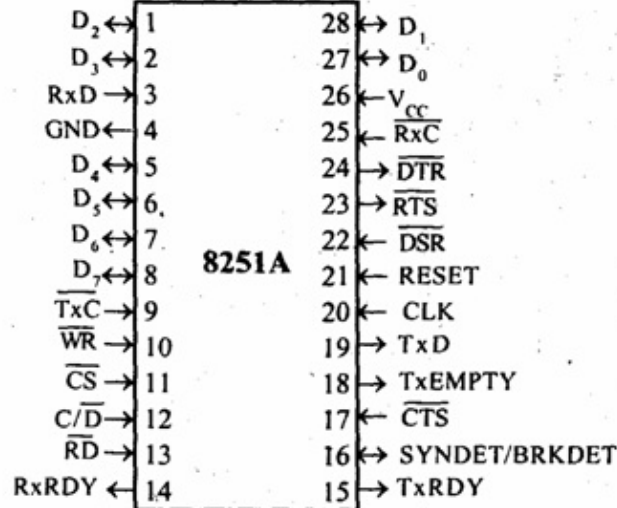
Simplex and Duplex Transmission

- Simplex.
  - One-way transmission.
  - Only one wire is needed to connect the two devices
  - Like communication from computer to a printer.

- Half-Duplex.
  - Two-way transmission but one way at a time.
  - One wire is sufficient.

- Full-Duplex.
  - Data flows both ways at the same time.
  - Two wires are needed.
  - Like transmission between two computers.

USART

USART stands for Universal Synchronous Receiver-Transmitter. It is an IC used to convert serial data into parallel data so that the computer can process it and vice-versa. It also has an acknowledgement mechanism to make sure that the sender does not transmit at a rate higher than the receiver can handle.

INTEL 8251A

The 8251A is a programmable communication interface for serial data transmission. Its a type of USART. It accepts data in parallel format from the CPU and converts them into a continuous serial stream for transmission. Simultaneously, it can receive serial data streams and converts them into parallel data. The data so converted into parallel format are sent to the CPU for processing.

8251A

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D₂ ↔ |1          28| ↔ D₁
D₃ ↔ |2          27| ↔ D₀
RxD → |3          26| ← Vcc
GND ← |4          25| ← RxC
D₄ ↔ |5          24| → DTR
D₅ ↔ |6.         23| → RTS
D₆ ↔ |7    8251A 22| ← DSR
D₇ ↔ |8          21| ← RESET
TxC → |9          20| ← CLK
WR → |10         19| → TxD
CS → |11         18| → TxEMPTY
C/D → |12         17| ← CTS
RD → |13         16| ↔ SYNDET/BRKDET
RxRDY ← |14      15| → TxRDY
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D₀ - D₇ ⟺           → TxD
RESET →             → TxRDY
CLK →               → TxEMPTY
C/D →               ← TxC
RD →         8251A  ← Vcc
WR →                → GND
CS →                ← RxD
DSR →               → RxRDY
DTR ←               ← RxC
CTS →
RTS ←               ↔ SYNDET/
                      BRKDET
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Pin	Description
D₀-D₇	Parallel data
C/D	Control register or Data buffer select
RD	Read control
WR	Write control
CS	Chip Select
CLK	Clock pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready
TxRDY	Transmitter Ready
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/ BRKDET	Synchronous Detect / Break Detect
RTS	Request To Send Data
CTS	Clear To Send Data
TxEMPTY	Transmitter Empty
Vcc	Supply (+5V)
GND	Ground (0 V)

TYPES OF CONTROL WORDS-:

1. mode word

2. command word

3. status word

Before starting data transmission, control words are loaded into Intel 8251

STEPS FOR SENDING DATA TO CPU

1. TX RDY is connected to interrupt pin

2. When TX RDY is high it can accept data

3. When data is received it goes low

Then data is converted in serial form through TXD li

5. Rate of data is controlled by TXC pin

STEPS FOR RECEIVING DATA FROM I/O DEVICE

1. when RX RDY is low it can accept data

2. when data is received it goes high

hen data is converted in parallel form through RXD

4. Rate of data is controlled by RXC pin

THE END .