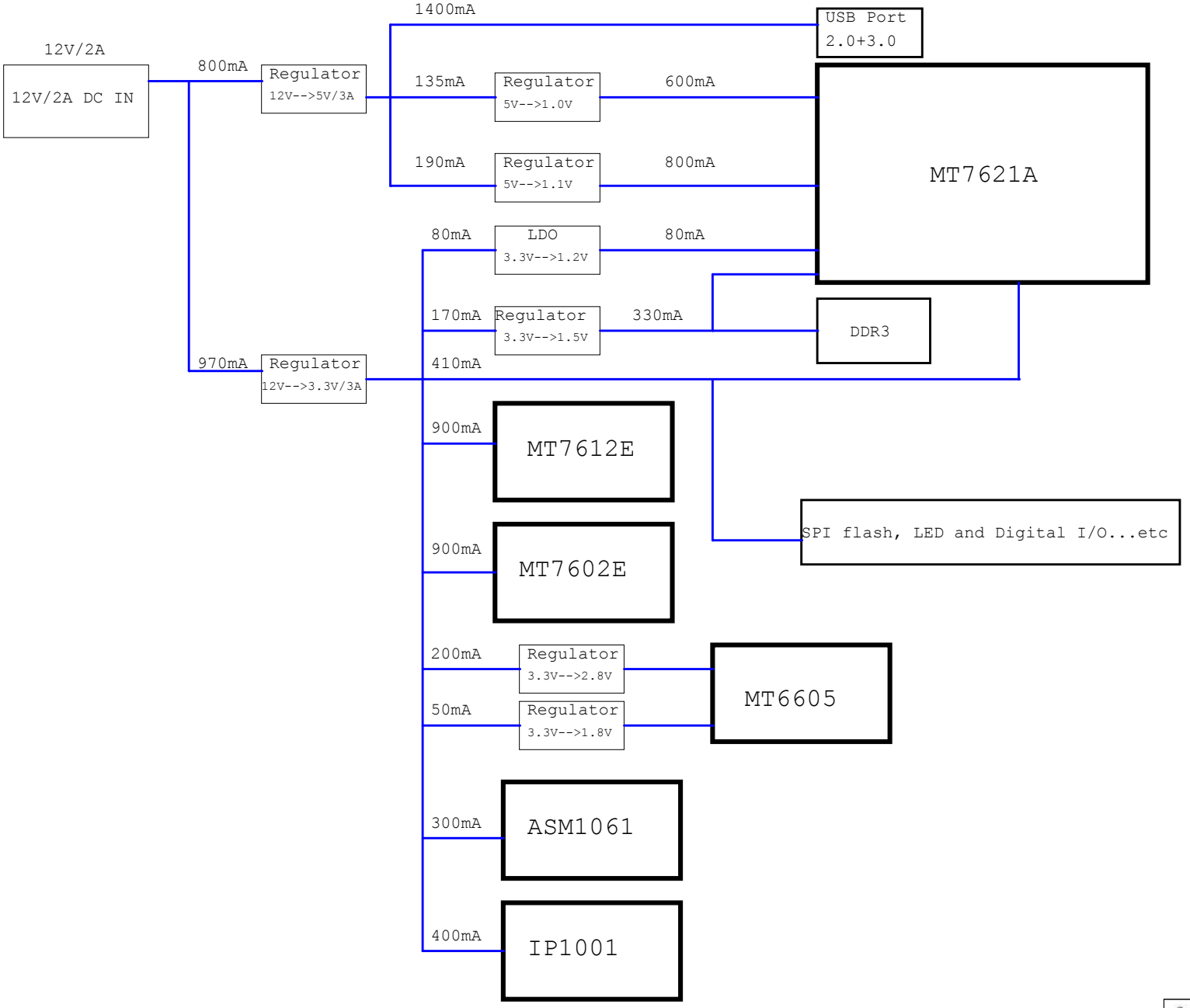

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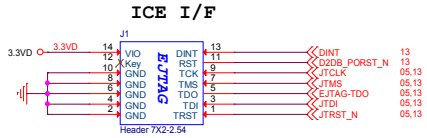
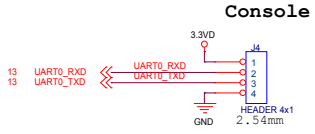
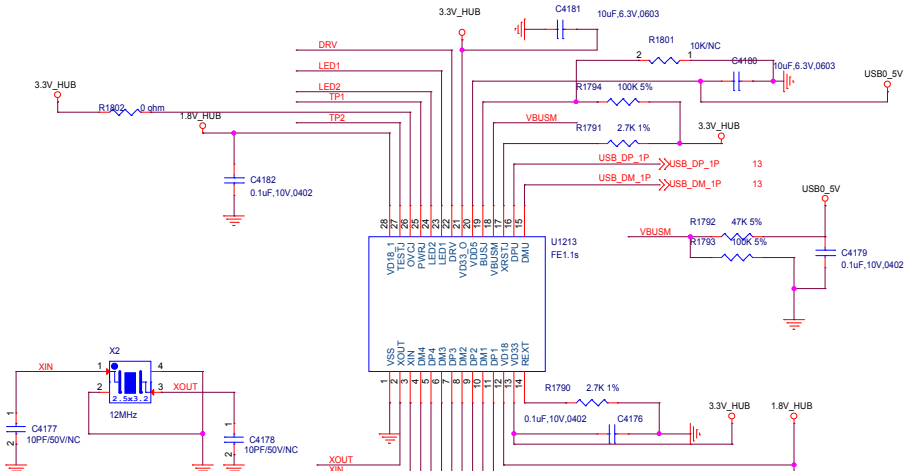
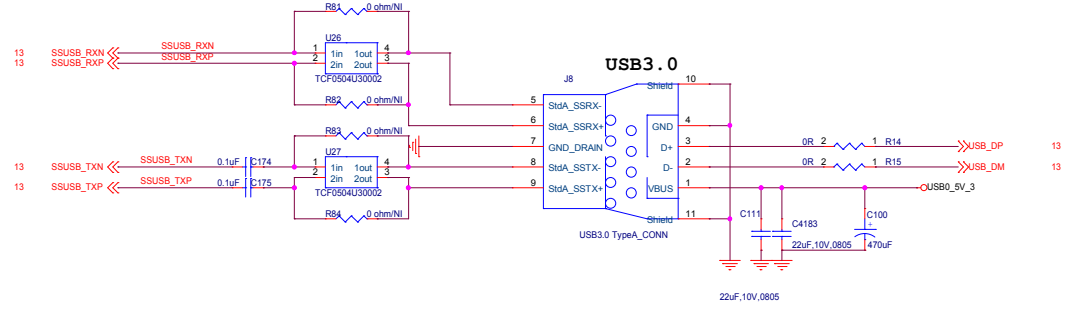
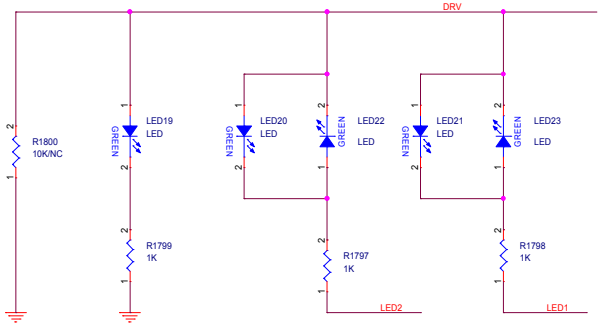


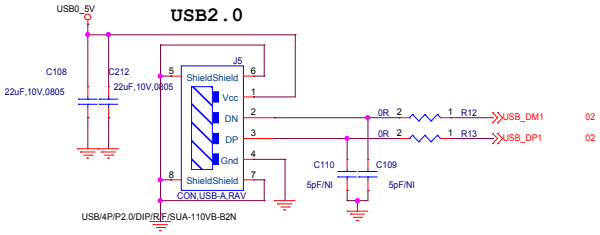
rts3_n (O)	i2s_sdo (O)
cts3_n (I)	i2s_clk (I/O)
txd3 (O)	i2s_ws (I/O)
rxd3 (I)	i2s_sdi (I)

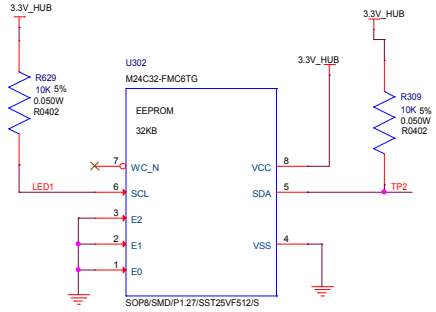












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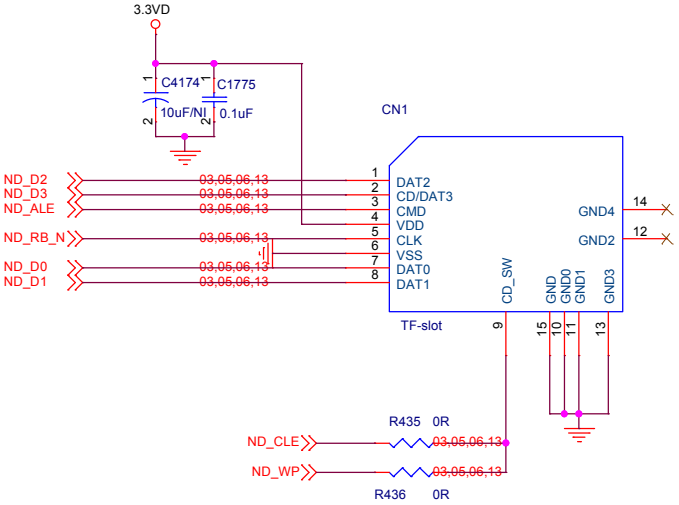

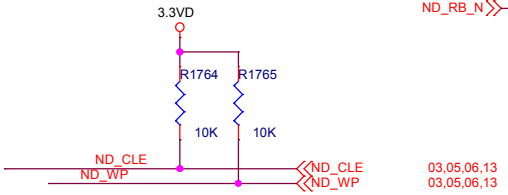

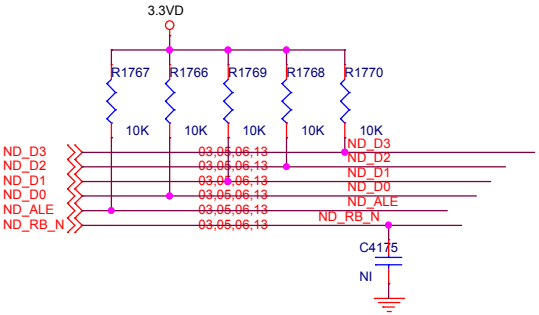

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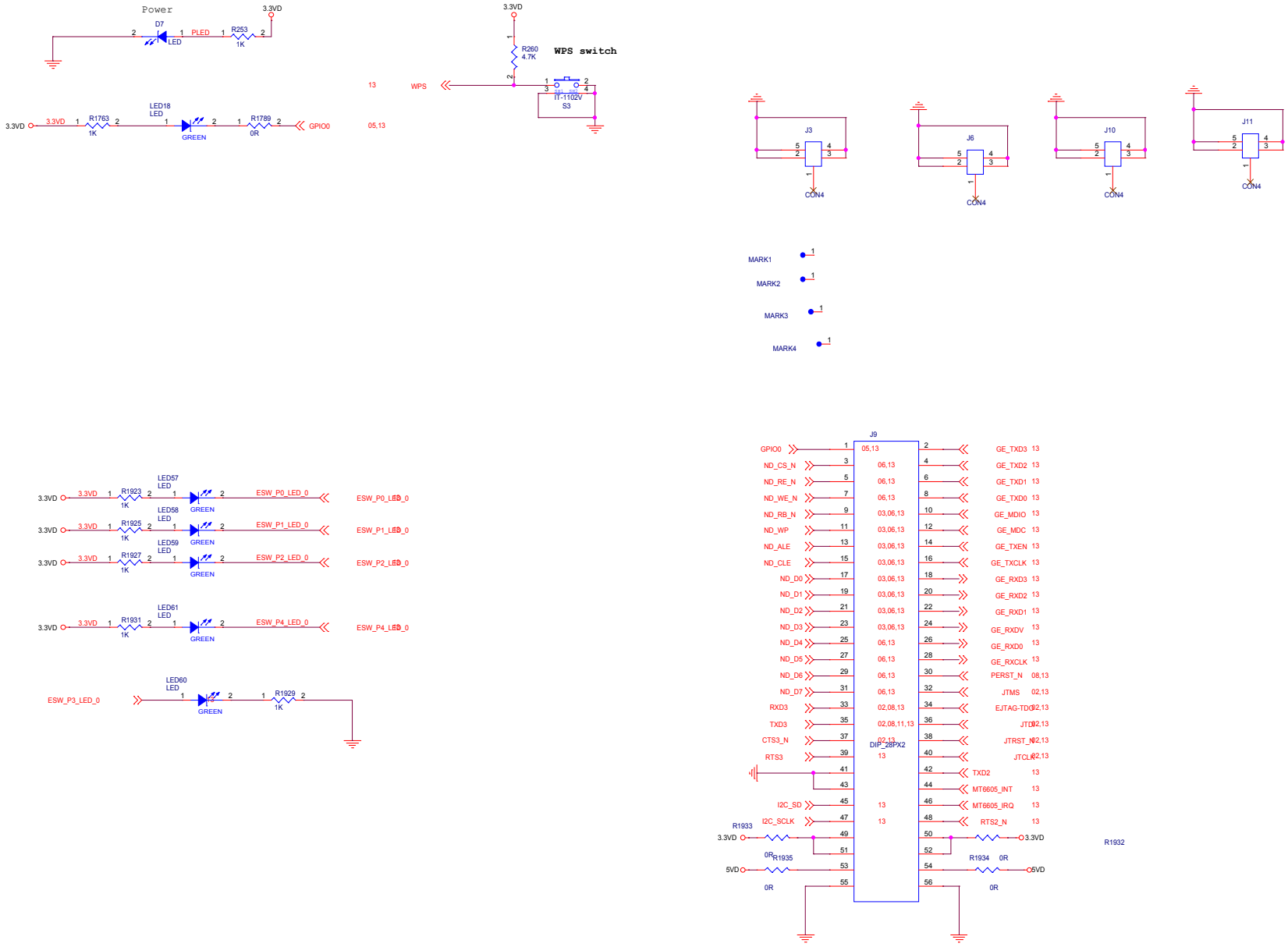
LED



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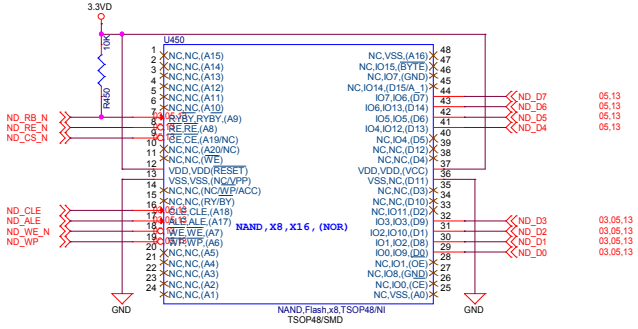

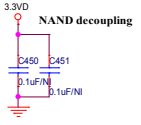

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Boot Strapping

Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input **011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

Giga Switch Hardware Trap

Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		

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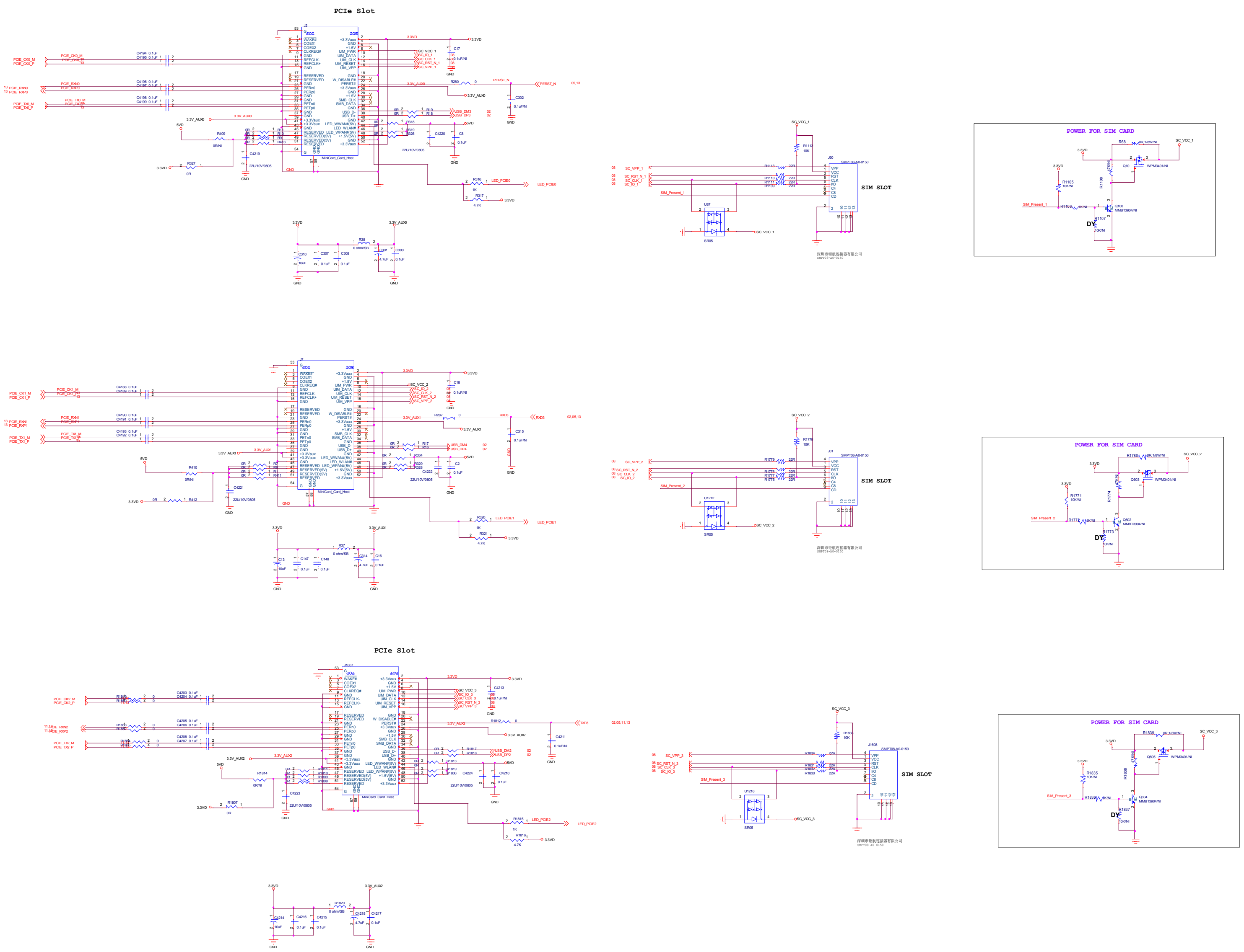

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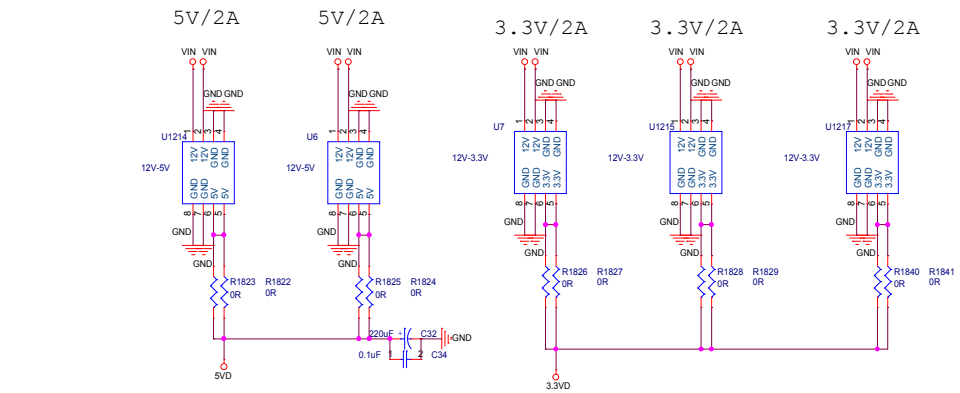
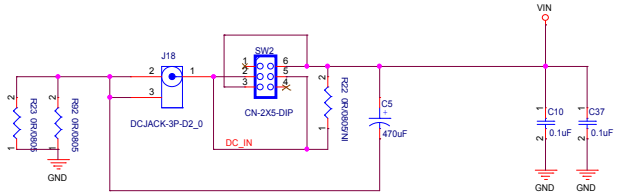
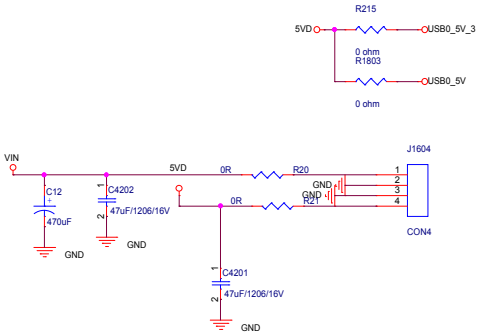
USB 5V Power





5-12V DC ADAPTER



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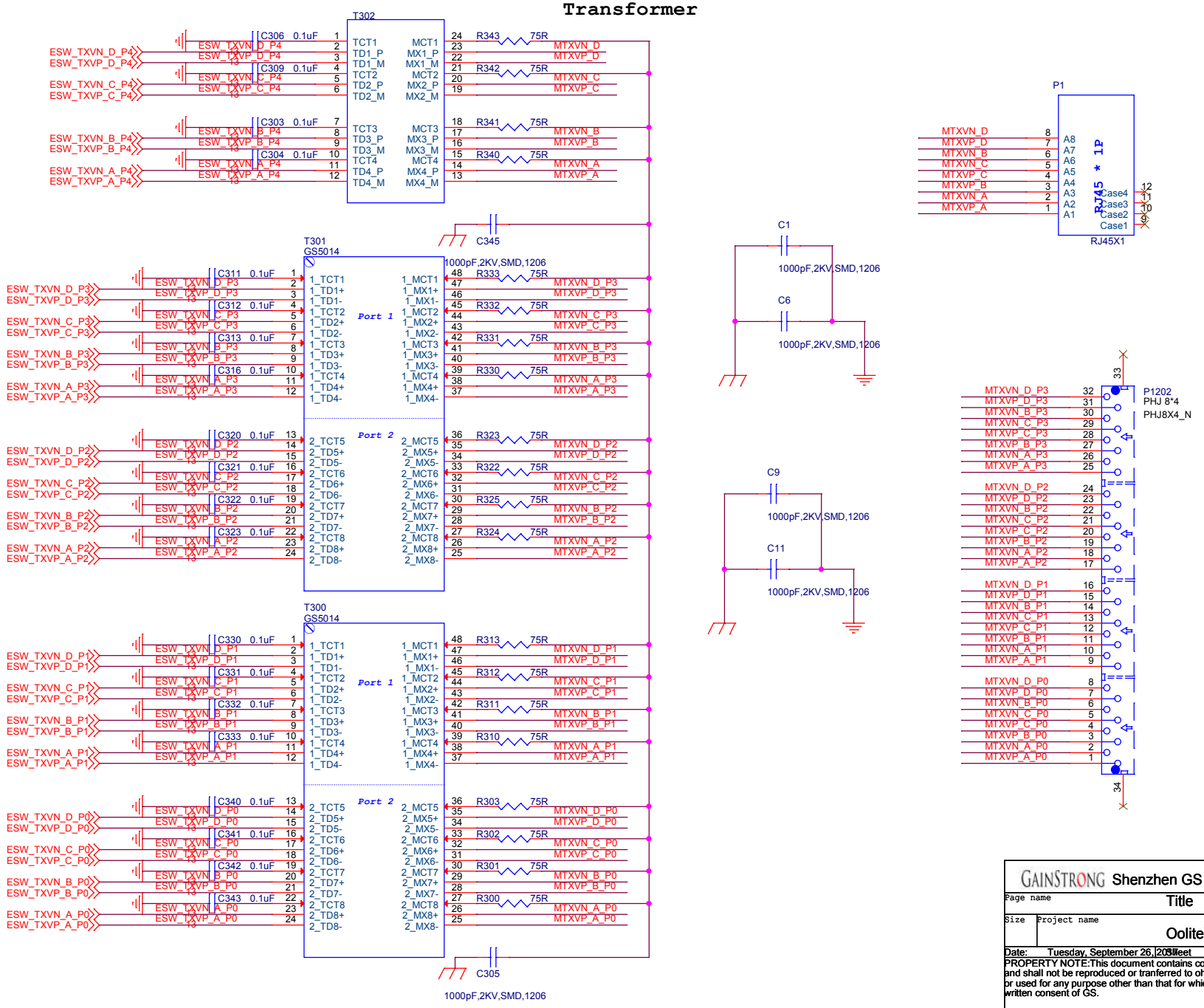
Transformer



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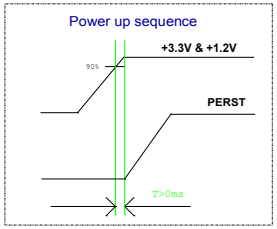
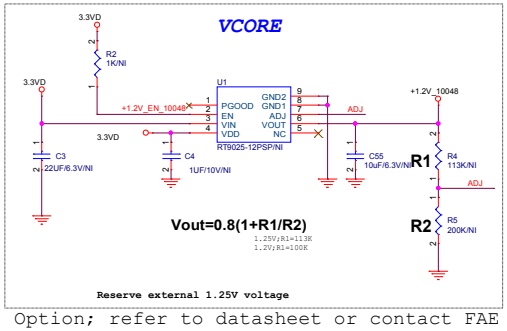
PCIe to SATA

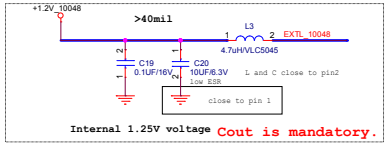




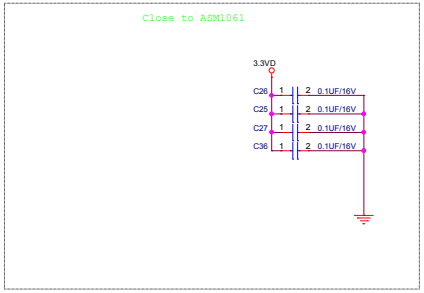
Option; refer to datasheet or contact FAE

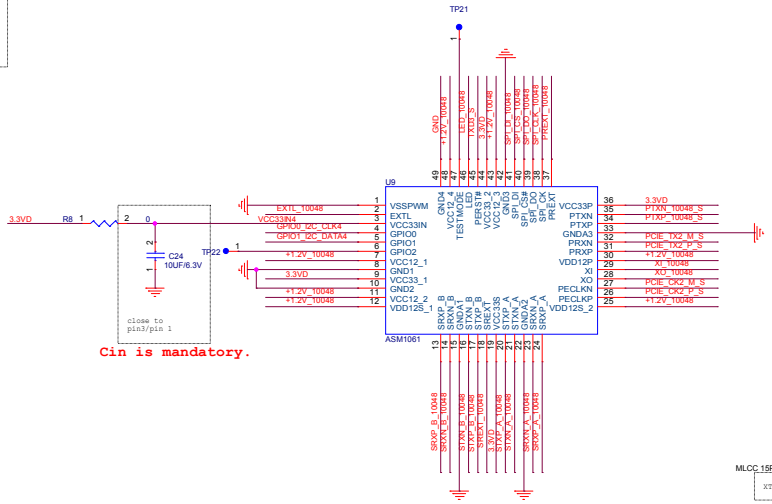
PCIE_TX2_P
PCIE_TX2_M
PCIE_TX2_P_S
PCIE_TX2_M_S
TXD3
TXD3_S
PCIE_CK2_P
PCIE_CK2_M
PCIE_CK2_P_S
PCIE_CK2_M_S
PTXN_10048_S
PTXP_10048_S
C14
C23
MLCC 0.1UF/16V (0402) X7R 10%
Close to PCIe Slot
X7R/0402 type

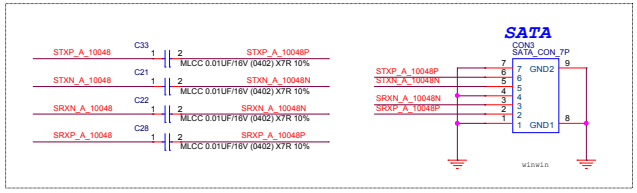
SREXT_10048 R48 12.1K 1%
PREXT_10048 R49 12.1K 1%
Close to IC

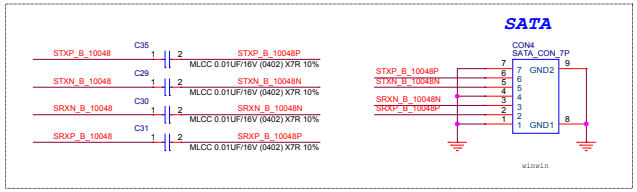


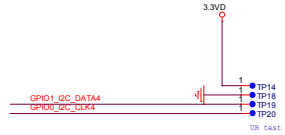
Internal 1.25V voltage **Cout is mandatory.**

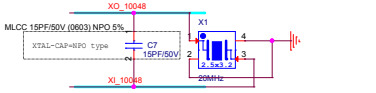




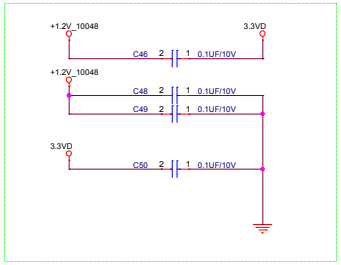








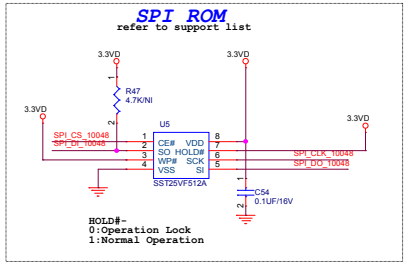
XI & XO follow differential layout rule for Min. jitter



H/W Strapping

refer to datasheet:

SPI_DO
0: Spin up by H/W
1: Spin up by S/W



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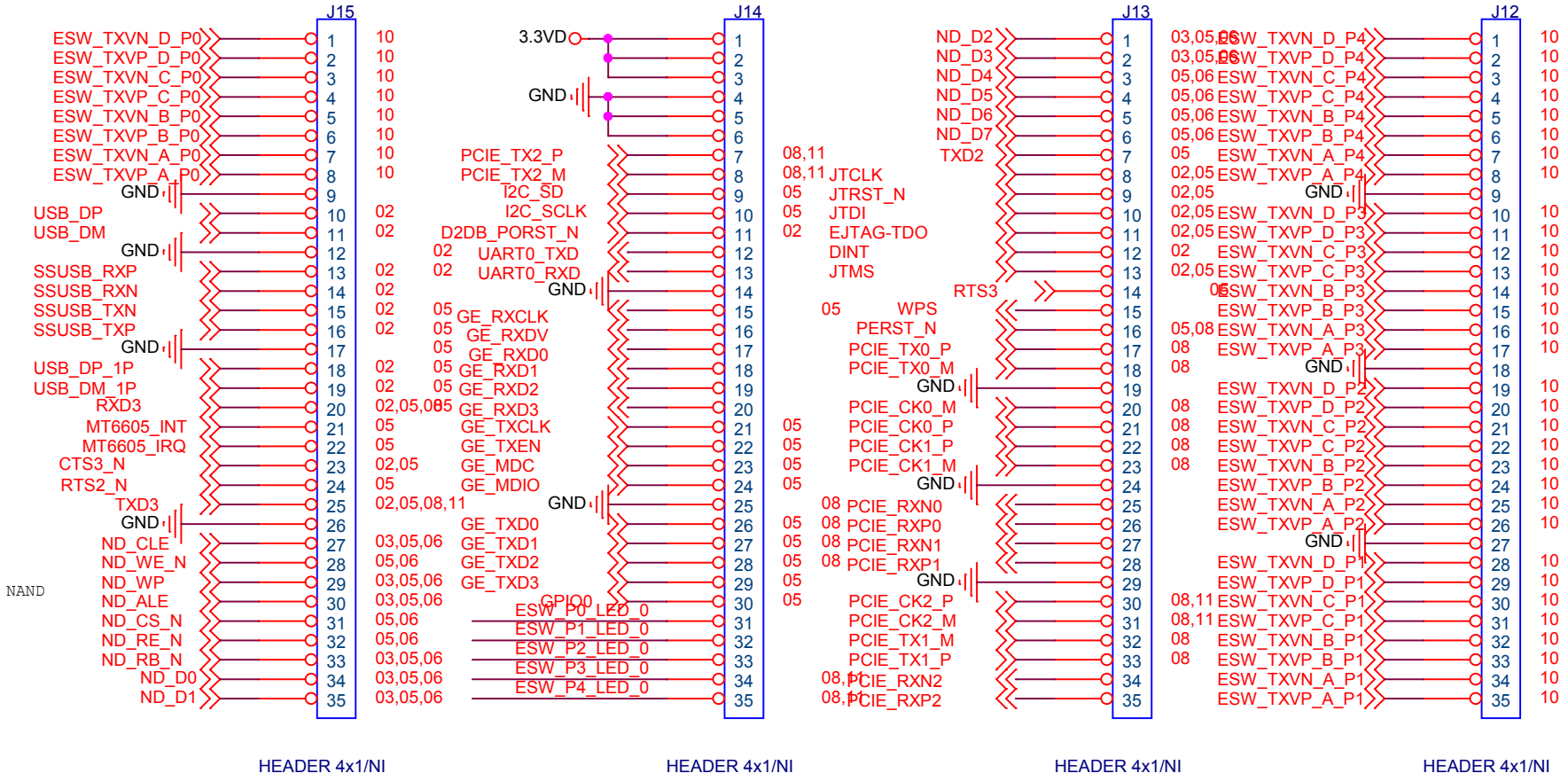

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