

GAINSTRONG

MT7688AN/MT7628AN Core Module

# OoliteV3.3 SPEC

*Specification Version V1.0.1*

Author : River

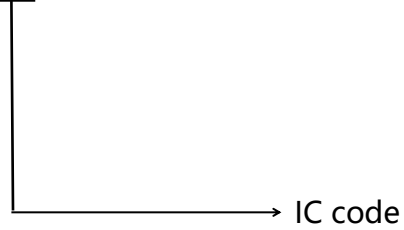
*May 17, 2017*

Revision	Date	Contents of Revision Change	Remark
1.0.0	2017-5-10	First release	
1.0.1	2017-5-17	supplementary information	

## MODULE CODE

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Oolite -V3.2-S/D



IC code	IC
S	MT7688AN
D	MT7628AN

# 1 INTRODUCTION

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The Oolite V3.3 module can use the MT7688AN chipset or MT7628AN chipset.

## 1.1 Oolite V3.3D

The Oolite V3.3D module use the MT7628AN chipset. The MT7628AN includes a high performance 580/575 MHz MIPS 24KEc CPU core and high speed USB2.0/PCIe interfaces, which is designed to enable a multitude of high performance, cost-effective IEEE 802.11n applications with a MediaTek WiFi client card. There are several masters (MIPS 24KEc, USB, PCI Express, SDXC, FE) in the MT7628 SoC on a high performance, low latency Rbus. In addition, the MT7628 SoC supports lower speed peripherals such as UART Lite, GPIO, I2C and SPI via a low speed peripheral bus (Pbus). The DDR/DDR2 controller is the only bus slave on the Rbus. It includes an Advanced Memory Scheduler to arbitrate the requests from bus masters, enhancing the performance of memory access intensive tasks.

### Features:

- CPU: MT7628AN with 580/575 MHz MIPS 24KEc
- RAM: 64MB DDR2 RAM (maximum 256MB optional)
- Flash: 64MB SPI NOR Flash ROM(8/16/32/64M option)
- Wireless speed: 300Mbps
- GPIO: 42 (total), High-speed UART for console support
- USB: Usb 2.0 master interface, support USB hub extension
- Power supply voltage: 3.3V.
- Port: 1×WAN+ 4×LAN ( IOT mode 1×port)
- 1×PCIE interface
- Antenna: 2× IPeX external antenna.
- Debug: serial debugging interface has lead out.
- Supports 16 DMA channels and 32 bit address.
- 8 channel QoS Arbiter with Configurable Bandwidth and Duedate for each agent.
- Supports the Synchronous Inter-Integrated Circuits (I2C) serial protocol
- Supports up to 2 SPI master operations and Extends the addressable range from 24 bits to 32 bits for memory size
- larger than 128 Mb.

## 1.2 Oolite V3.3S

The Oolite V3.3S module use the MT7688AN chipset. The MT7688AN integrates a 1T1R 802.11n Wi-Fi radio, a 580MHz MIPS® 24KEc™ CPU, 1-port fast Ethernet PHY, USB2.0 host, PCIe, SD-XC, I2S/PCM and multiple slow IOs. The MT7688AN provides two operation modes – IoT gateway mode and IoT device mode. In IoT gateway mode, the PCI Express interface can connect to 802.11ac chipset for 11ac dual-band concurrent gateway. The high performance USB 2.0 allows the MT7688AN to add 3G/LTE modem support or add a H.264 ISP for wireless IP camera. For the IoT device mode, the MT7688AN supports eMMC, SD-XC and USB 2.0. The MT7688AN can support the WiFi high quality audio via 192Kbps/24bits I2S interface and VoIP application through PCM. In IoT device mode, it further supports PWM, SPI slave, 3rd UART and more GPIOs. For IoT gateway, it can connect to touch panel and BLE, Zigbee/Z-Wave and sub-1G RF for smart home control.

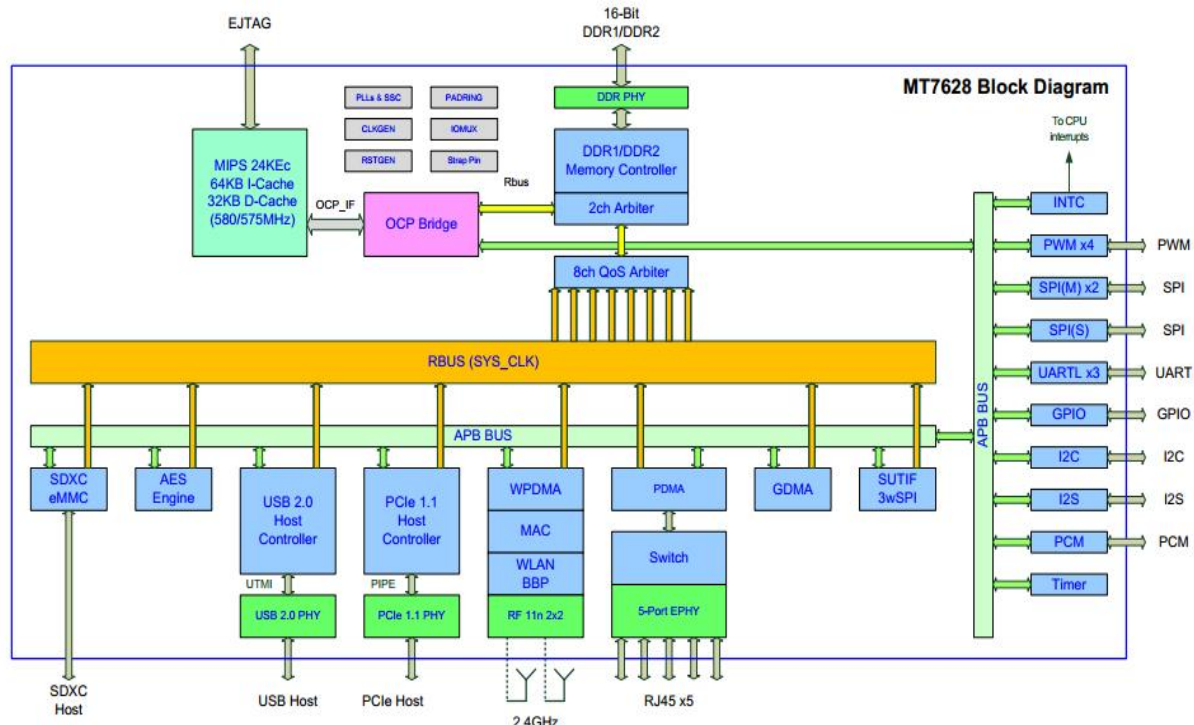
### Features:

- CPU: MT7688AN with 580/575 MHz MIPS 24KEc
- RAM: 64MB DDR2 RAM (256MB optional)
- Flash: 64MB SPI NOR Flash ROM(8/16/32/64M option)
- Wireless speed: 150Mbps
- GPIO:46(total), High-speed UART for console support
- USB: Usb 2.0 master interface, support USB hub extension
- Power supply voltage: 3.3V
- Port: 1×port (IOT Device Mode)
- 1×PCIe interface
- Antenna:1× IPeX external antenna.
- 20/40 MHz channel bandwidth
- Supports Legacy 802.11b/g ,HT 802.11n and 802.11vmodes
- Supports WEP64/128, TKIP, AES, WPA, WPA2, WAPI
- Green AP/STA
  - Intelligent Clock Scaling (exclusive)
  - DDRII: ODT off, Self-refresh mode
- iPA/iLNA and ePA/eLNA
- Embedded PMU

## 2 FUNCTIONAL BLOCK DIAGRAM

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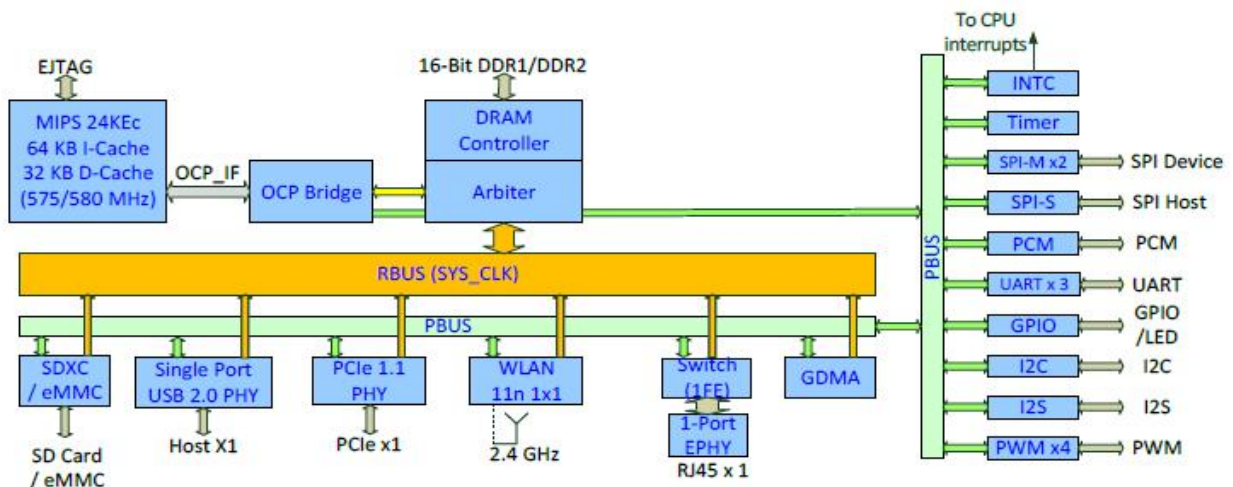
### 2.1 Oolite V3.3D

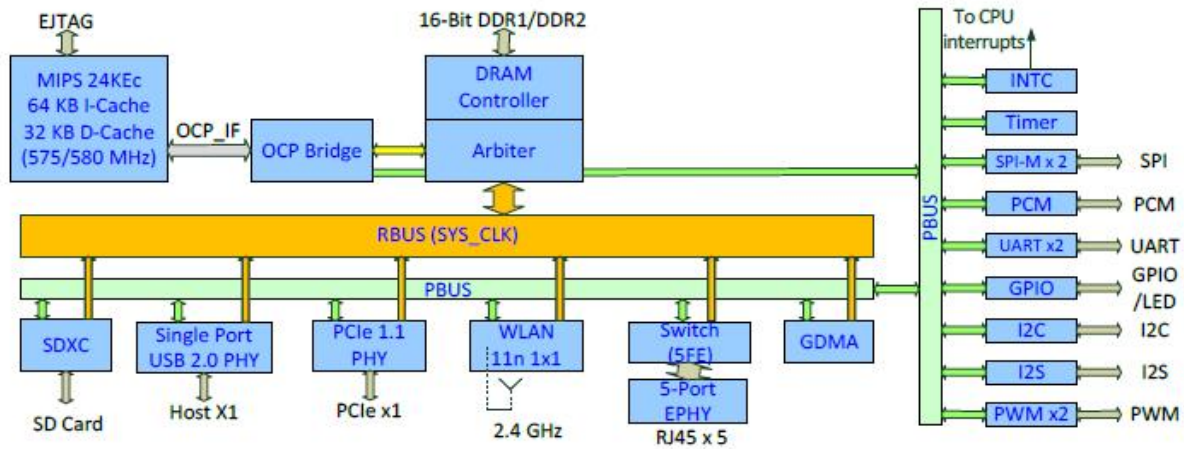


TBD

## 2.2 Oolite V3.3S

### IoT Device Mode

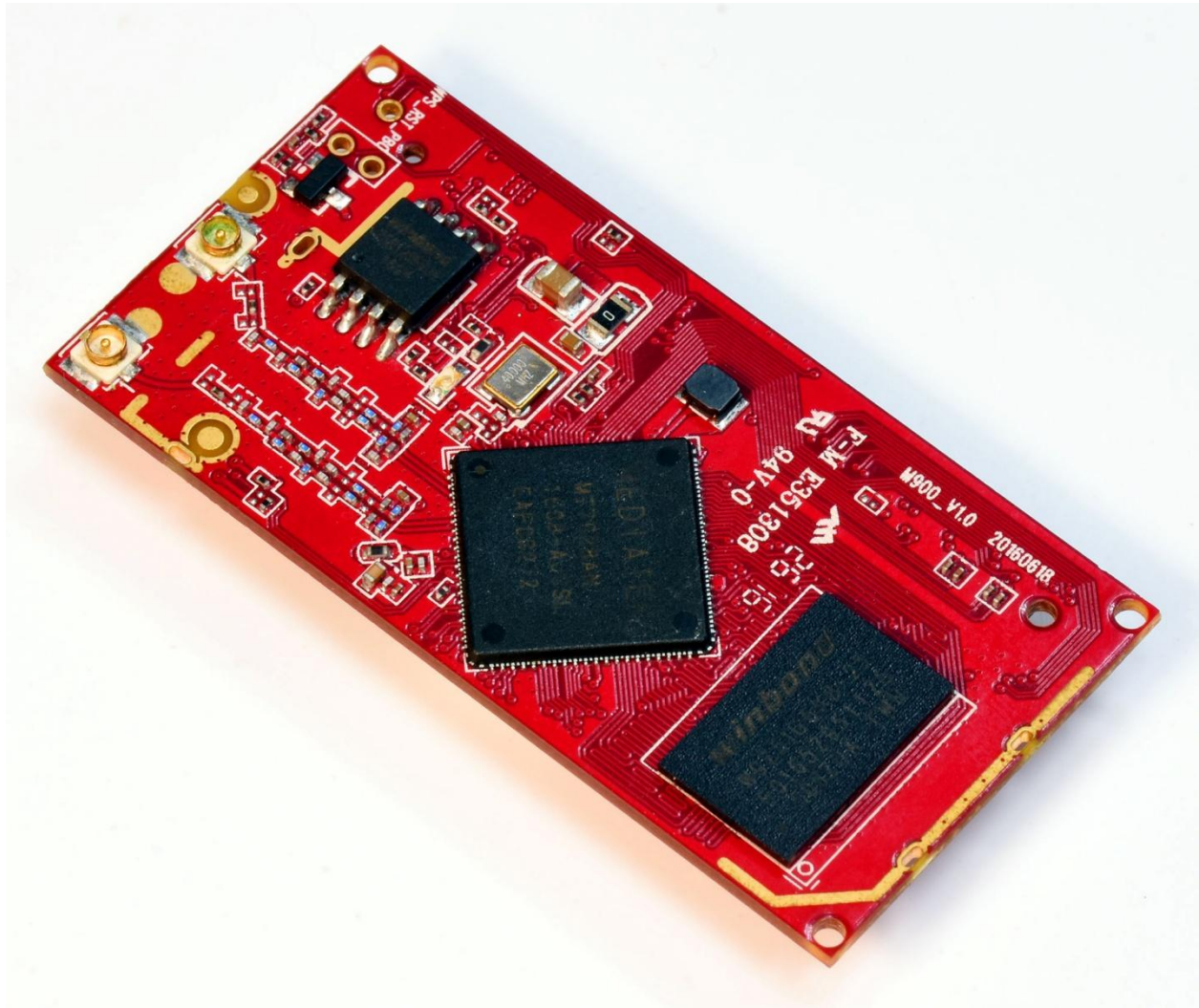


**IoT Gateway Mode**

## 3 PICTURES

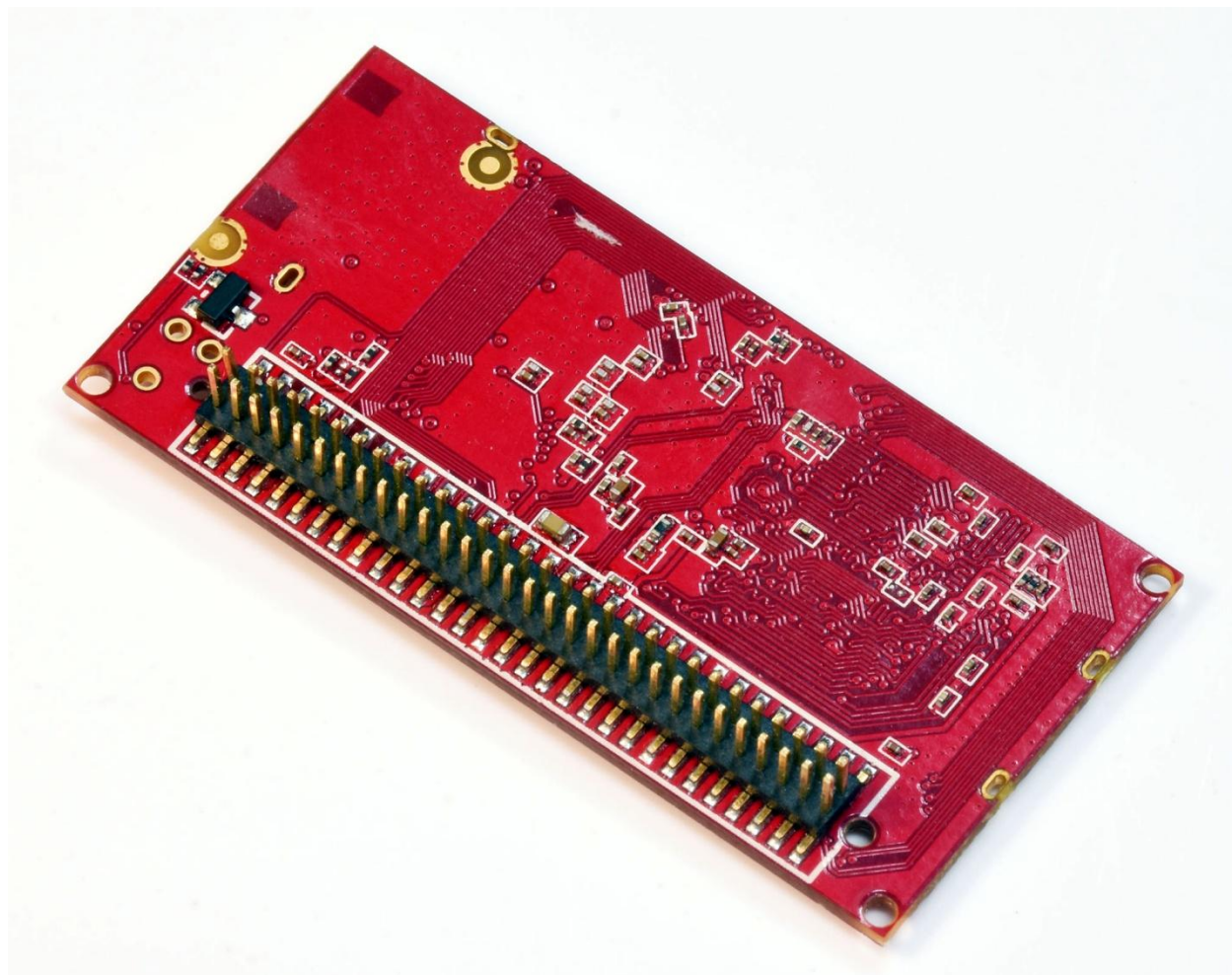
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TOP:





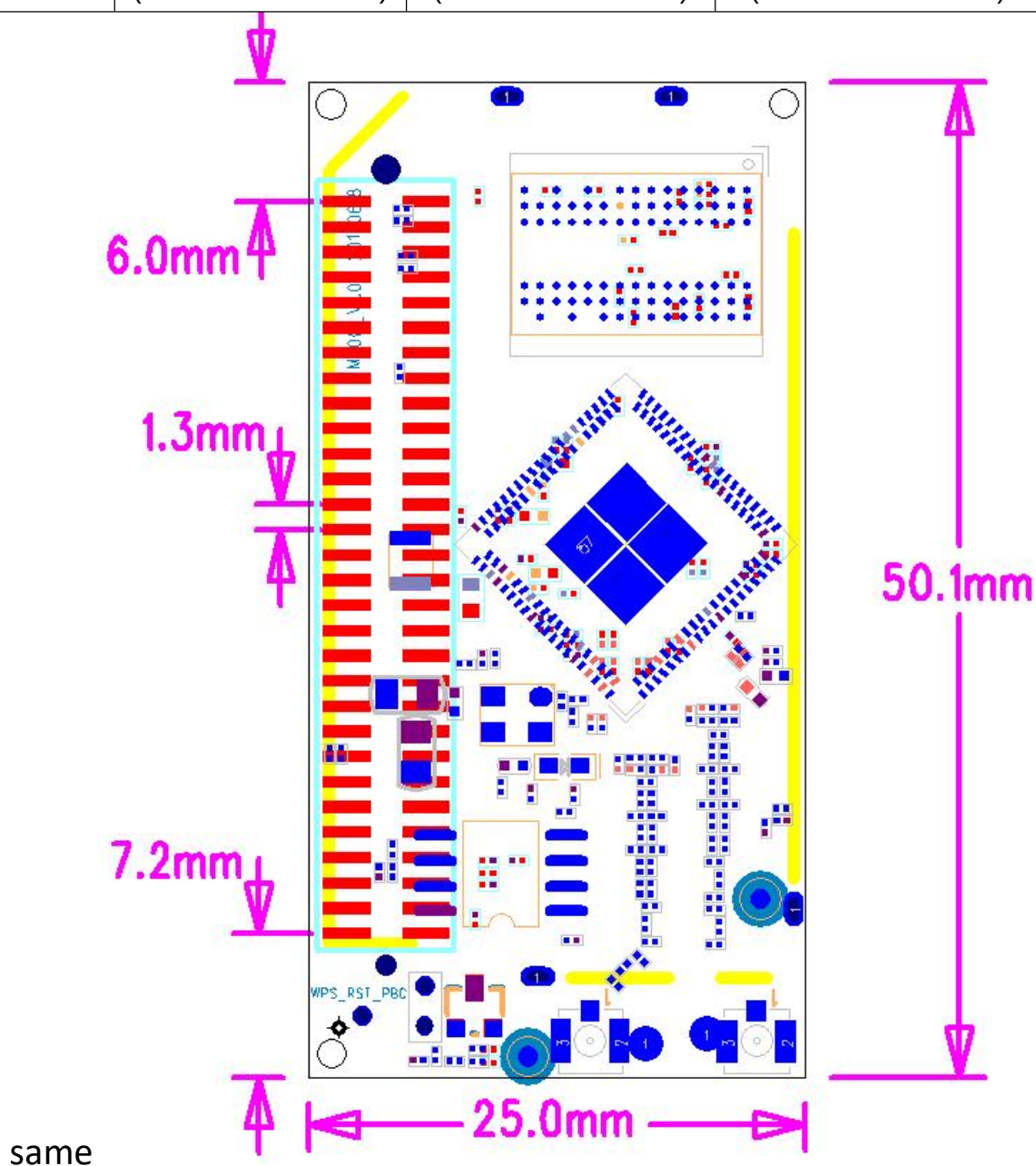
BOTTOM:



## 4 MECHANICAL

Oolite V3.3D and Oolite V3.3S are the

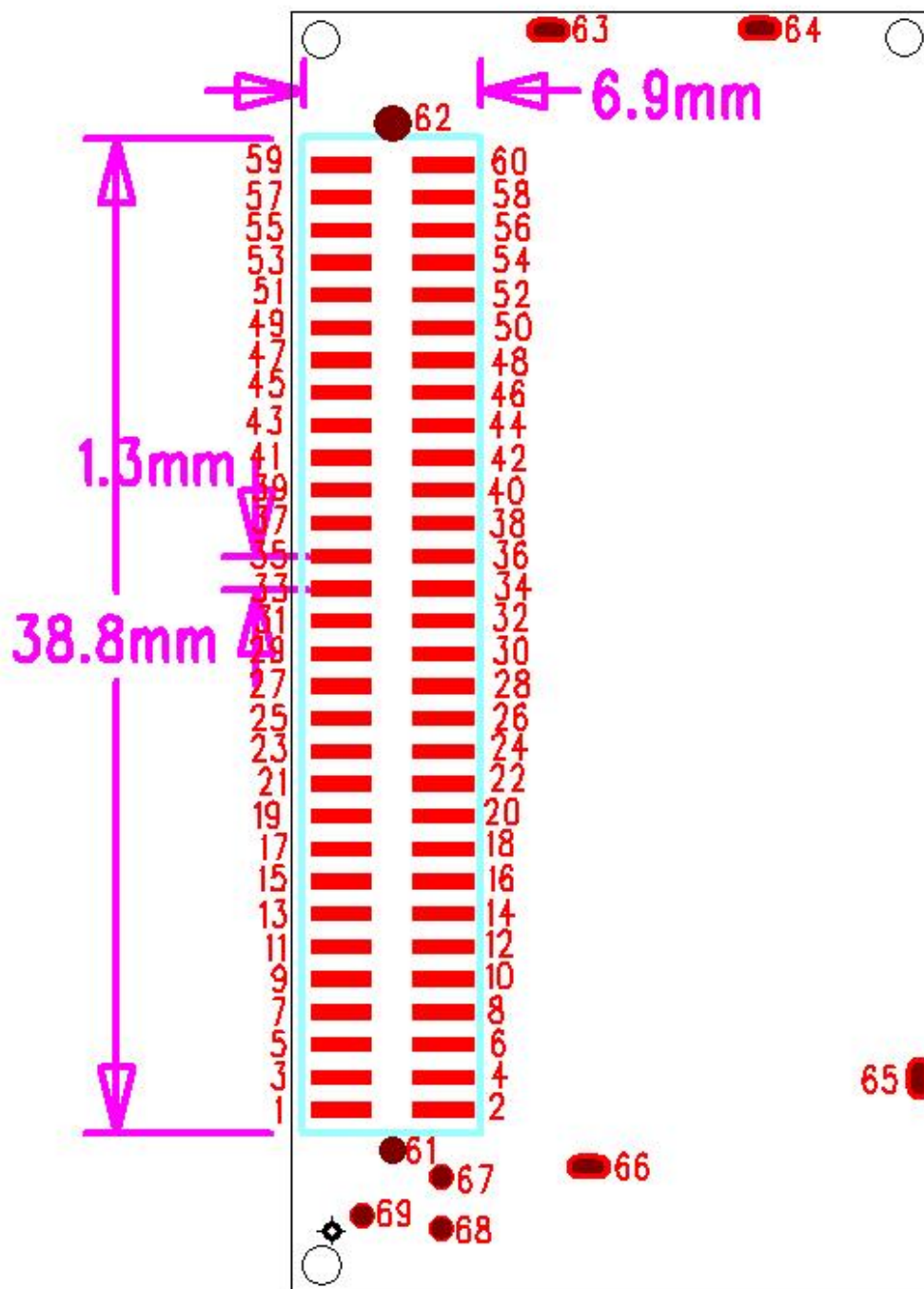
Dimensions (mm)	Length	Width	Height (without shield)
	50.1 (Tolerance:±0.2mm)	25.0 (Tolerance:±0.2mm)	1.0 (Tolerance:±0.2mm)



## **5 PACKAGE STRUCTURE FOR CONNECTING MODULE ON FLOOR PLATE**

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Oolite V3.3D and Oolite V3.3S are the same



## 6 PINS DESCRIPTION

Oolite V3.3D and Oolite V3.3S are the same

Pin No.	Name	Description
1	SPI_CS1	SPI chip select1
2	UART_TXD1	UART1 Lite TXD1
3	LINK4	10/100 PHY Port #4 activity LED
4	SPI_CLK	SPI clock
5	SPI_MOSI	SPI Master output
6	UART_RXD1	UART0 Lite RXD
7	3.3V	POWER
8	3.3V	POWER
9	UART_RXD0	UART0 Lite RXD
10	UART_TXD0	UART0 Lite TXD
11	I2S_DO	I2S data output
12	LINK0	10/100 PHY Port #0 activity LED
13	I2S_CLK	I2S clock
14	I2S_WS	I2S word select
15	REFCLK0_OUT	Reference Clock Ouptut
16	I2S_DI	I2S data input
17	GND	GROUND
18	GND	GROUND
19	RXIN0	10/100 PHY Port #0 RXN
20	RXIP0	10/100 PHY Port #0 RXP
21	TXON0	10/100 PHY Port #0 TXN
22	TXOP0	10/100 PHY Port #0 TXP
23	3.3V	
24	USB_D+	USB Port0 data pin Data+
25	I2C_SCLK	I2C clock
26	USB_D-	USB Port0 data pin Data-
27	I2C_SD	I2C Data
28	WLED_N	WLAN Activity LED

29	GND	GROUND
30	GND	GROUND
31	GPIO20	General Purpose I/O
32	GPIO18	General Purpose I/O
33	GPIO21	General Purpose I/O
34	GPIO19	General Purpose I/O
35	GPIO0	General Purpose I/O
36	CPURST_N	Power on reset
37	GPIO29	General Purpose I/O
38	GPIO28	General Purpose I/O
39	GPIO27	General Purpose I/O
40	GPIO26	General Purpose I/O
41	GPIO25	General Purpose I/O
42	GPIO24	General Purpose I/O
43	GPIO23	General Purpose I/O
44	GPIO22	General Purpose I/O
45	GND	GROUND
46	GND	GROUND
47	TXOP1	10/100 PHY Port #1 TXP
48	PERST_IN	PCIe device reset
49	TXON1	10/100 PHY Port #1 TXN
50	PCIE_CKP0	External reference clock output
51	RXIP1	10/100 PHY Port #1 RXP
52	PCIE_CKN0	External reference clock output
53	RXIN1	10/100 PHY Port #1 RXN
54	PCIE_RXN0	PCIe0 differential transmit RX-
55	LINK1	10/100 PHY Port #1 activity LED
56	PCIE_RXP0	PCIe0 differential transmit RX +
57	LINK2	10/100 PHY Port #2 activity LED
58	PCIE_TXP0	PCIe0 differential transmit TX +

59	LINK3	10/100 PHY Port #4 activity LED
60	PCIE_TXN0	PCIE0 differential transmit TX -
61	Floating	
62	Floating	
63	GND	GROUND
64	GND	GROUND
65	GND	GROUND
66	GND	GROUND
67	POWER_ON	3.3V
68	CPURST_N	Power on reset
69	WPS_RST_PBC	Watchdog timeout reset

**NOTE:**

1. Power supply pin 7,8,23 can input 3.3V,
2. Unused GPIOs can floating, no need pull-up or pull-down.
3. I/O supply voltage is 3.3V
4. Input,Output,or I/O Voltage allow GND-0.3 V to Vcc +0.3V

**7 PIN SHARE SCHEME**



Oolite V3.3D and Oolite V3.3S are the same

#### UART1 pin share scheme

Controlled by the UART1\_MODE register.

Pin Name	2'b00 UART-Lite #1	2'b01 GPIO	2'b10 PWM	2'b11 TRX_SW
UART1_RXD	UART1_RXD	GPIO#46	PWM_CH1	
UART1_TXD	UART1_TXD	GPIO#45	PWM_CH0	

#### MT7688AN EPHY LED pin share scheme

Controlled by the P#\_LED\_AN\_MODE registers

Pin Name	Bootstrapping (DBG_JTAG_MODE=1)	Bootstrapping (DBG_JTAG_MODE=0)	
		P4_LED_AN_MODE =2'b00	P4_LED_AN_MODE =2'b01
EPHY_LED4_N_JTRST_N	JTAG_RST_N	EPHY_LED4_N	GPIO#39
		P3_LED_AN_MODE =2'b00	P3_LED_AN_MODE =2'b01
EPHY_LED3_N_JTCLK	JTAG_CLK	EPHY_LED3_N	GPIO#40
		P2_LED_AN_MODE =2'b00	P2_LED_AN_MODE =2'b01
EPHY_LED2_N_JTMS	JTAG_TMS	EPHY_LED2_N	GPIO#41
		P1_LED_AN_MODE =2'b00	P1_LED_AN_MODE =2'b01
EPHY_LED1_N_JTDI	JTAG_TDI	EPHY_LED1_N	GPIO#42
		P0_LED_AN_MODE =2'b00	P0_LED_AN_MODE =2'b01
EPHY_LED0_N_JTDO	JTAG_TDO	EPHY_LED0_N	GPIO#43

#### MT7688AN WLAN LED pin share scheme

Controlled by the WLED\_AN\_MODE registers

Pin Name	2'b00	2'b01
WLED_N	WLED_N	GPIO#44



**PERST\_N pin share scheme**

Controlled by the PERST\_MODE register.

Pin Name	1'b0	1'b1
PERST_N	PERST_N	GPIO#36

**WDT\_RST\_N pin share scheme**

Controlled by the WDT\_MODE register.

Pin Name	1'b0	1'b1
WDT_RST_N	WDT_RST_N	GPIO#37

**REF\_CLKO pin share scheme**

Controlled by the REFCLK\_MODE register.

Pin Name	1'b0	1'b1
REF_CLKO	REF_CLKO	GPIO#38

**UART0 pin share scheme**

Controlled by the UART0\_MODE register.

Pin Name	1'b0	1'b1
UART_TXD0	UART_TXD0	GPIO#12
UART_TXD0	UART_RXD0	GPIO#13

**GPIO0 pin share scheme**

Controlled by GPIO\_MODE register.

Pin Name	2'b00	2'b01	2'b10	2'b11
GPIO0	GPIO#11	GPIO#11	REF_CLKO	PERST_N

**SPI pin share scheme**

Controlled by SPI\_MODE register.

Pin Name	1'b0	1'b1
SPI_CLK	SPI_CLK	GPO#7
SPI_MOSI	SPI_MOSI	GPO#8
SPI_MISO	SPI_MISO	GPIO#9
SPI_CS0	SPI_CS0	GPIO#10

**SPI\_CS1 pin share scheme**

Controlled by SPI\_CS1\_MODE register.

Pin Name	2'b00	2'b01	2'b10
SPI_CS1	SPI_CS1	GPIO#6	REF_CLKO

**I2C pin share scheme**

Controlled by I2C\_MODE register.

Pin Name	2'b00	2'b01
I2C_SCLK	I2C_SCLK	GPIO#4
I2C_SD	I2C_SD	GPIO#5

**I2S pin share scheme**

Controlled by I2S\_MODE register.

Pin Name	2'b00	2'b01	2'b10
I2S_SDI	I2C_SCLK	GPIO#0	PCMDRX
I2S_SDO	I2C_SD	GPIO#1	PCMDTX
I2S_WS	I2C_SCLK	GPIO#2	PCMCLK
I2S_CLK	I2C_SD	GPIO#3	PCMFS

**SD pin share scheme**

Controlled by the EPHY\_APGIO\_AIO\_EN[4:1] and SD\_MODE registers

Pin Name	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	SD_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	SD_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	SD_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	SD_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	SD_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	SD_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	SD_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	SD_D3	GPIO#29

**eMMC pin share scheme**

Controlled by the EPHY\_APGIO\_AIO\_EN[4:1] and SD\_MODE registers

Pin Name	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	eMMC_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	eMMC_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	eMMC_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	eMMC_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	eMMC_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	eMMC_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	eMMC_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	eMMC_D3	GPIO#29

**UART2 pin share scheme**

Controlled by the EPHY\_APGIO\_AIO\_EN[4:1] and UART2\_MODE registers

Pin Name	4'b0000	4'b1111			
		2'b00	2'b01	2'b10	2'b11
MDI_TP_P2	MDI_TP_P2	UART_TXD2	GPIO#20	PWM_CH2	eMMC_D5
MDI_TN_P2	MDI_TN_P2	UART_RXD2	GPIO#21	PWM_CH3	eMMC_D4

**PWM\_CH1 pin share scheme**

Controlled by the EPHY\_APGIO\_AIO\_EN[4:1] and PWM1\_MODE registers

Pin Name	4'b0000	4'b1111			
		2'b00	2'b01	2'b10	2'b11
MDI_RN_P2	MDI_RN_P2	PWM_CH1	GPIO#19		eMMC_D6

**PWM\_CH0 pin share scheme**

Controlled by the EPHY\_APGIO\_AIO\_EN[4:1] and PWM0\_MODE registers

Pin Name	4'b0000	4'b1111			
		2'b00	2'b01	2'b10	2'b11
MDI_RP_P2	MDI_RP_P2	PWM_CH0	GPIO#18		eMMC_D7

**SPIS pin share scheme**

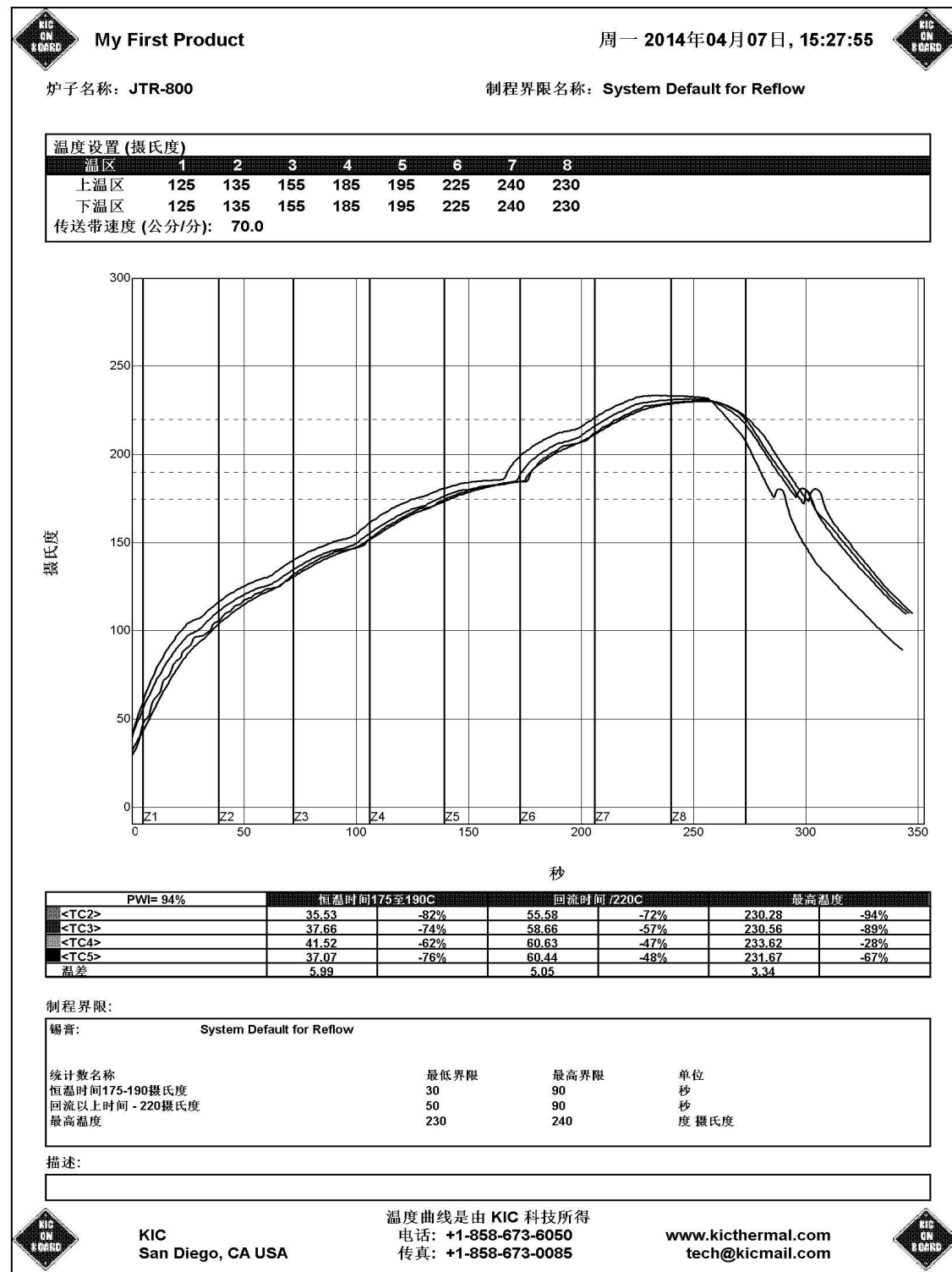
Controlled by the EPHY\_APGIO\_AIO\_EN[4:1] and SPIS\_MODE registers

Pin Name	4'b0000	4'b1111			
		2'b00	2'b01	2'b10	2'b11
MDI_TP_P1	MDI_TP_P1	SPIS_CS	GPIO#14		PWM_CH0
MDI_TN_P1	MDI_TN_P1	SPIS_CLK	GPIO#15		PWM_CH1
MDI_RP_P1	MDI_RP_P1	SPIS_MISO	GPIO#16		UART_TXD2
MDI_RN_P1	MDI_RN_P1	SPIS_MOSI	GPIO#17		UART_RXD2

**Bootstrapping Pins Description**

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7688AN only. It needs to be pull-low for 7688KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

## 8 REFLOW SOLDERING TEMPERATURE CURVE





## 9 MODULE OTHER CONTENT

### 8.1 RF hardware performance

#### 8.1.1 Oolite V3.3D

Item	type	real target
Antenna 0	Frequency error	-5.0ppm
	power	CCK 11M 18.0dbm OFDM 54M 16.0dbm MCS7(HT20) 16.0dbm MCS7(HT40) 15.0dbm
	EVM	CCK 11M -18.0db OFDM 54M -25.0db MCS7(HT20) -27.0db MCS7(HT40) -28db
	Reception Sensitivity	CCK 11M -85dbm OFDM 54M -63dbm MCS7(HT20) -61dbm MCS7(HT40) -59dbm

Item	type	real target
	Frequency error	-5.0ppm
	power	CCK 11M 18.0dbm OFDM 54M 16.0dbm MCS7(HT20) 16.0dbm MCS7(HT40) 15.0dbm
	EVM	CCK 11M 26.0db OFDM 54M -25.0db

Antenna 1		MCS7(HT20) -27.0db MCS7(HT40) -28db
	Reception Sensitivity	CCK 11M -85dbm OFDM 54M -63dbm MCS7(HT20) -61dbm MCS7(HT40) -59dbm

### 8.1.2 Oolite V3.3S

Item	type	real target
Antenna 0	Frequency error	-5.0ppm
	power	CCK 11M 18.0dbm OFDM 54M 16.0dbm MCS7(HT20) 16.0dbm MCS7(HT40) 15.0dbm
	EVM	CCK 11M -18.0db OFDM 54M -25.0db MCS7(HT20) -27.0db MCS7(HT40) -28db
	Reception Sensitivity	CCK 11M -85dbm OFDM 54M -63dbm MCS7(HT20) -61dbm MCS7(HT40) -59dbm

### 8.2 Installed matters needing attention

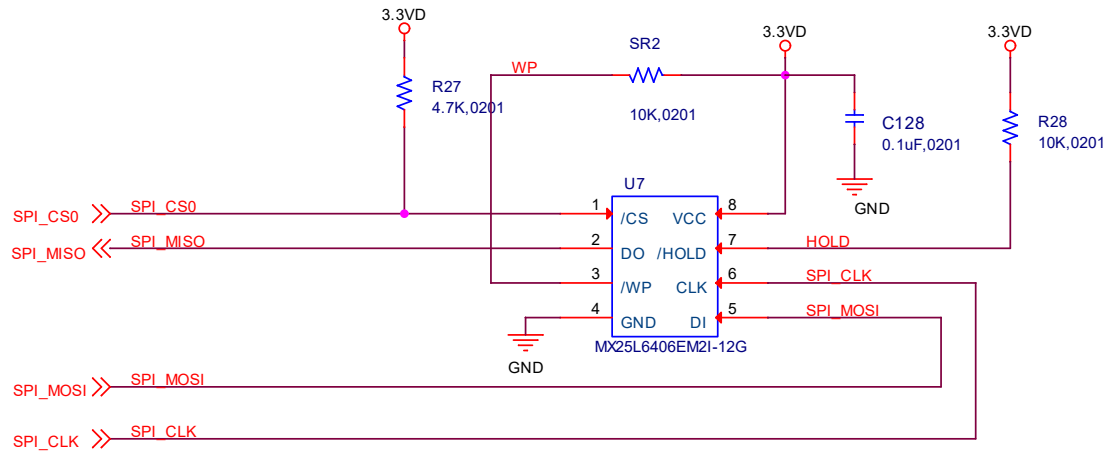
- In the opening of the steel mesh, the module of the pad hole in a ratio of 1:1 to expand 0.7mm and thickness of 0.12 mm.
- Putting the module to the oven at 120 °C ( $\pm 5^{\circ}\text{C}$ ) baking for 12 hours, and then on the basis of how much per hour can stick taking out the corresponding number of modules.
- Bring gloves and electrostatic ring to get the module.

d. The furnace temperature on the basis of main board size .

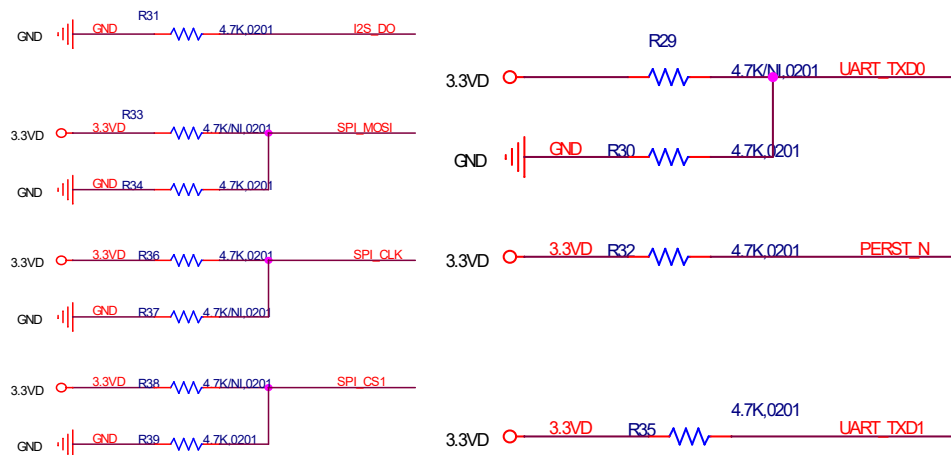
## 9 ENCLOSURE

Oolite V3.2D and Oolite V3.2S are the same

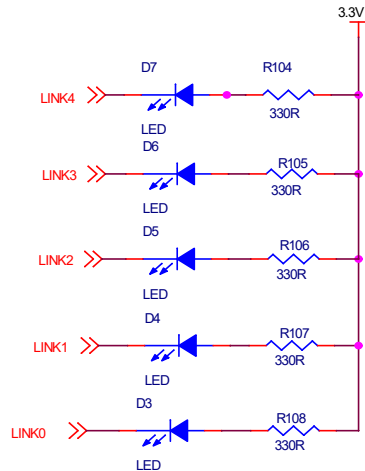
### (1) SPI Flash Schematic



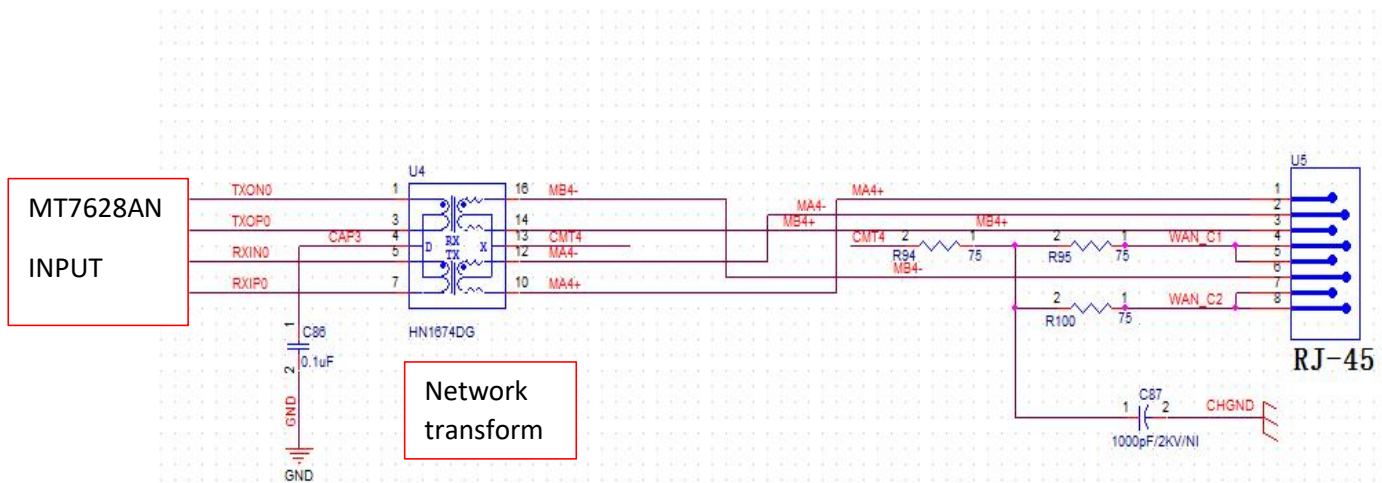
### (2) Bootstrap CONFIG Schematic



### (3) External mode of module



### (4) Net port connection



## 10 MODULE OPERATING ENVIRONMENT

Working temperature: 0 °C to 40 °C;

Storage temperature: -40 °C to 70 °C;



Humidity: 10% to 90% RH no condensation;

Storage humidity: 5% to 90% RH no condensation.