

GAINSTRONG Oolite-MT7620A_SPEC

Specification Version 1.0.4

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Rev.	Date	Contents of Revision Change	Remark
1.0.0	2016-02-30	Initial release	
1.0.1	2018-02-09	Revise	James
1.0.2	2018-04-18	Supplementary specification	Bruce Lee
1.0.3	2018-08-27	Fixed Error:GE1_RXD0 GE1_RXCLK inverted!	James
1.0.4	2018-11-13	Fixed Module Pins Map Error	James



1 OVERVIEW

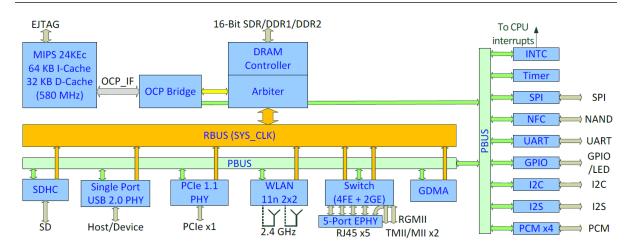
The MT7620 router-on-a-chip includes an 802.11n MAC and baseband, a 2.4 GHz radio and FEM, a 580 MHz MIPS® 24K™ CPU core, a 5-port 10/100 switch and two RGMII. The MT7620 includes everything needed to build an AP router from a single chip. The embedded high performance CPU can process advanced applications effortlessly, such as routing, security and VoIP. The MT7620 also includes a selection of interfaces to support a variety of applications, such as a USB port for accessing external storage.

2 FEATURES

- CPU:7620A Embedded MIPS24KEc (580 MHz) with 64 KB I-Cache and 32 KB D-Cache
- 802.11 b/g/n 2T2R 2.4 GHz with 300Mbps data rate.
- 16-bit DDR2 up to 256 Mbyte (optional: 64Mbyte/128Mbyte/256Mbyte)
- SPI Flash:16MByte(optional: 16Mbyte/32Mbyte/64Mbyte)
- Nand Flash:512Byte page(max 64Mbyte), 2KByte page(max 1Gbyte),need teternal extend.
- 1x USB 2.0, 1x PCle host/device
- 5-port 10/100 SW and two RGMII
- I2C, I2S, SPI, PCM, UART, JTAG, MDC, MDIO, GPIO
- Hardware NAT with IPv6 and 2 Gbps wired speed
- 16 Multiple BSSID
- WEP64/128, TKIP, AES, WPA, WPA2, WAPI
- QoS: WMM, WMM-PS
- WPS: PBC, PIN
- Voice Enterprise: 802.11k+r
- Firmware: Linux 2.6 SDK, Openwrt/Lede
- Size:40mm*40mm*4.25mm



3 FUNCTIONAL BLOCK DIAGRAM



4 MAIN FEATURES

Features	MT7620N	MT7620A	
CPU	MIPS24KEc (600/580 MHz)	MIPS24KEc (580 MHz)	
Total DMIPs 580 x 1.6 DMIPs 580 x 1.6 DMIPs		580 x 1.6 DMIPs	
I-Cache, D-Cache 64 KB, 32 KB 64 KB, 32 KB		64 KB, 32 KB	
L2 Cache n/a n/a		n/a	
HNAT/HQoS	HNAT	HNAT 2 Gbps forwarding	
Memory			
DRAM Controller	16 b	16 b	
SDRAM	512 Mb, 120 MHz	n/a	
DDR1	512 Mb, 193 MHz	n/a	
DDR2	512 Mb, 193 MHz	2 Gb, 193 MHz	
NAND	n/a	Small page 512Byte (max 512M bit) Large page 2Kbyte (max 8G bit)	
SPI Flash	3B addr mode (max 128Mbit) 4B addr mode (max 512Mbit)	3B addr mode (max 128Mbit) 4B addr mode (max 512Mbit)	
SD	n/a	SD-XC (class 10)	
RF	2T2R 802.11n 2.4 GHz	2T2R 802.11n 2.4 GHz	
PCIe	n/a	1	
USB 2.0	1	1	
Switch	5p FE SW	5p FE SW + RGMII(1) 4p FE SW + RGMII(2)	
125	n/a	1	
PCM	n/a	1	
I2C	1	1	
UART	1 (Lite)	2 (Lite/Full)	
JTAG	1	1	
Package	DRQFN148- 12 mm x 12 mm	TFBGA265- 11 mm x 11 mm	

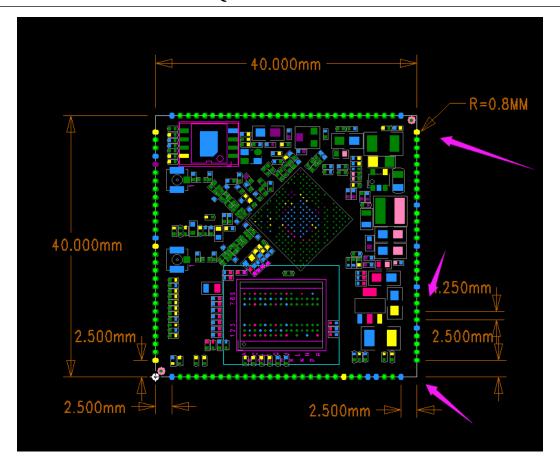


5 MOUDLE PICTURE



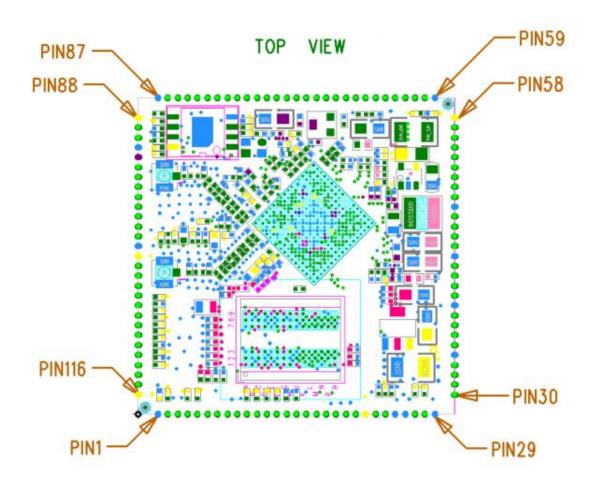


6 PHYSICAL DEMENSIONS (REFERENCE FOR MAINBOARD DESIGN)





7 MODULE PINS DESCRIPTION



Pin No.	Out Name	description			
1	ND_GND				
These pin shared with Nand and SD interface					
2	ND_WP/SD_WP				
3	ND_RB_N/SD_CLK				
4	ND_CLE/SD_CD				
5	ND_ALE/SD_CMD				
6	ND_D7/BT_ANT				
7	ND_D6/BT_WACT				



8	ND_D5/BT_AUX	
9	ND_D4/BT_STAT	
10	ND_D3/SD_D3	
11	ND_D2/SD_D2	
12	ND_D1/SD_D1	
13	ND_D0/SD_D0	
14	TXD Uart Full	
15	RXD	
16	DSR_N	
17	DCD_N	
18	DTR_N	
19	RIN	
20	CTS_N	
21	RTS_N	
22	UART_3.3V Uart Lite	
23	UART_TXD2	
24	UART_RXD2	
25	UART_GND	
26	I2C_GND	
27	I2C_SCLK I2C	
28	I2C_SD	
29	MDI_GND Ethernet Port 0	
30	MDI_RP_P0	
31	MDI_RN_P0	
32	MDI_TP_P0	
33	MDI_TN_P0	
34	MDI_GND Ethernet Port 1	
35	MDI_RP_P1	



	-	
MDI_RN_P1		
MDI_TP_P1		
MDI_TN_P1		
MDI_GND Ethernet Port2		
MDI_RP_P2		
MDI_RN_P2		
MDI_TP_P2		
MDI_TN_P2		
MDI_GND		
MDI_RP_P3 Ethernet Port3		
MDI_RN_P3		
46 MDI_RN_P3 47 MDI_TP_P3		
MDI_TN_P3		
MDI_GND Ethernet Port4		
MDI_RP_P4		
MDI_RN_P4		
MDI_TP_P4		
MDI_TN_P4		
VIN_GND Power		
VIN_GND Power		
VIN_3.3V		
VIN_3.3V		
GE_3.3V		
RGMII 1000M/Ethernet		
GE_GND		
GE_MDIO		
GE_MDC		
GE2_TXD3		
	MDI_TP_P1 MDI_TN_P1 MDI_GND Ethernet Port2 MDI_RP_P2 MDI_RN_P2 MDI_TP_P2 MDI_TN_P2 MDI_GND MDI_RP_P3 Ethernet Port3 MDI_RP_P3 MDI_TP_P3 MDI_TN_P3 MDI_TN_P3 MDI_TN_P4 MDI_RP_P4 MDI_RP_P4 MDI_RP_P4 MDI_TP_P4 MDI_TP_P4 MDI_TP_P4 MDI_TP_P4 MDI_TP_P4 MDI_TP_P4 MDI_TP_P4 MDI_TN_P5 MDI_TN_P6 VIN_GND Power VIN_GND Power VIN_3.3V VIN_3.3V GE_3.3V RGMII 1000M/Ethernet GE_GND GE_MDIO GE_MDIO	



63	GE2_TXD2	
64	GE2_TXD1	
65	GE2_TXD0	
66	GE2_TXEN	
67	GE2_TXCLK	
68	GE1_TXD3	
69	GE1_TXD2	
70	GE1_TXD1	
71	GE1_TXD0	
72	GE1_TXEN	
73	GE1_TXCLK	
74	GE2_RXD3	
75	GE2_RXD2	
76	GE2_RXD1	
77	GE2_RXD0	
78	GE2_RXDV	
79	GE2_RXCLK	
80	GE1_RXD3	
81	GE1_RXD2	
82	GE1_RXD1	
83	GE1_RXD0	
84	GE1_RXCLK	
85	GE1_RXDV	
86	GE_CLK_25M	
87	GE_GND	
88	GE_3.3V	
89	UPHY0_PADP	
90	UPHY0_PADM USB	



91	UPHY0_GND		
92	PCIE_1.2V		
93	PCIE_PERST_N		
94	PCIE_TXP		
95	PCIE_TXN		
96	PCIE_RXP		
97	PCIE_RXN		
98	APCK_RFCKOP		
99	APCK_RFCKON		
100	PCIE_CLK_A_IN		
101	PCIE_GND		
102	PCIE_3.3V		
103 JTAG_DINT			
These pin shared with JTAG and ETH LED, WPS LED, interface			
104	JTAG_RST_N		
104	JIAG_N31_14		
104	WDT_RST_N		
105	WDT_RST_N		
105 106	WDT_RST_N GPIO		
105 106 107	WDT_RST_N GPIO JTAG_TCK		
105 106 107 108	WDT_RST_N GPIO JTAG_TCK JTAG_TMS		
105 106 107 108 109	WDT_RST_N GPIO JTAG_TCK JTAG_TMS JTAG_TD0		
105 106 107 108 109 110	WDT_RST_N GPIO JTAG_TCK JTAG_TMS JTAG_TD0 JTAG_TD1		
105 106 107 108 109 110 111	WDT_RST_N GPIO JTAG_TCK JTAG_TMS JTAG_TD0 JTAG_TD1 JTAG_TRST		
105 106 107 108 109 110 111 112	WDT_RST_N GPIO JTAG_TCK JTAG_TMS JTAG_TD0 JTAG_TD1 JTAG_TRST WLED_N Wireless LED		
105 106 107 108 109 110 111 112	WDT_RST_N GPIO JTAG_TCK JTAG_TMS JTAG_TD0 JTAG_TD1 JTAG_TRST WLED_N Wireless LED ND_CS_N		
105 106 107 108 109 110 111 112 113	WDT_RST_N GPIO JTAG_TCK JTAG_TMS JTAG_TD0 JTAG_TD1 JTAG_TRST WLED_N Wireless LED ND_CS_N Nand/SD		
105 106 107 108 109 110 111 112 113	WDT_RST_N GPIO JTAG_TCK JTAG_TMS JTAG_TD0 JTAG_TD1 JTAG_TRST WLED_N Wireless LED ND_CS_N Nand/SD ND_RE_N		



8 SCHEMATIC DESIGN NOTES

This part contains the schematic and PCB design notes for the customer who use the Core moudle for their own production. You can see our reference design and the MT7620A Spec for more detail design information.

8.1 Power

There is only one external power 3.3VDC for the Core Moudle. Other powers as 1.8VDC,1.5VDC and 1.2VDC are all generated from the Core Moudle internally. Power consumption:

For the 3.3VDC, the main board should supply at least 1A current for the module, for security use ,the Margin should be 30% at least.

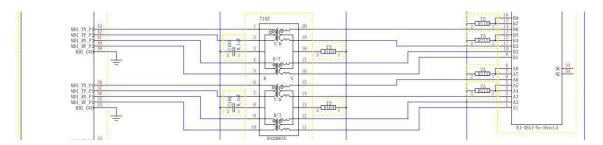
Power Ripple:

Small ripple is necessary for better performance, especially for the RF property. The 3.3VDC ripple should be \leq 50mV at idle state and \leq 100mV at full load.

8.2 ETHERNET PORT

There are 5 10/100M Ethernet port available form the Core moudle. For the MT7620A chip has already integrated the 10/100M Ethernet PHY, so the customer can only connect the ports to

the Transformer directly. These Port are changed to Current type. As seen in the below.



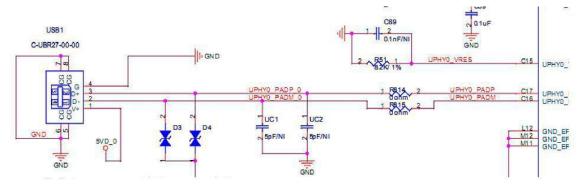
8.3 ETHERNET PORT

There are 2 RGMII(1000M) Ethernet port available form the Core moudle.Plz Follow the reference Design.



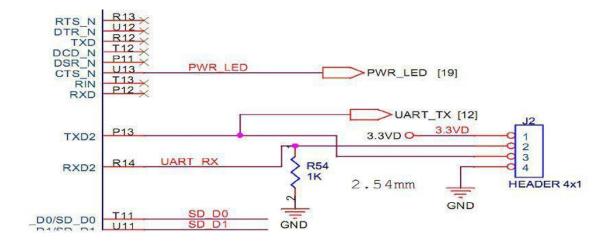
8.4 USB

USB 2.0 interface are available, customer can configure them to host or host/device by change the software configuration. Careful layou include equal length, appropriate space and 90ohm differential resistor for the differential USB signal is necessary. ESD protection can be reserved.



8.5 UART PORT

There are two UART port One is UART Lite, The other one is UART Full, Both can be used as the serial port for system debug or used as communication with Zigbee For attention, the external UART chip like RS232 is necessary when using the port. The connector on your main board can be usb, DB9, and any other kinds. Pull up to 3.3Von the RXD is necessary.





8.6 I2C

One I2C port can be use. External pull up to 3.3V is necessary.

8.7 UARTF PIN SHARE SCHEME

detailed Info Plz refer Datasheet.

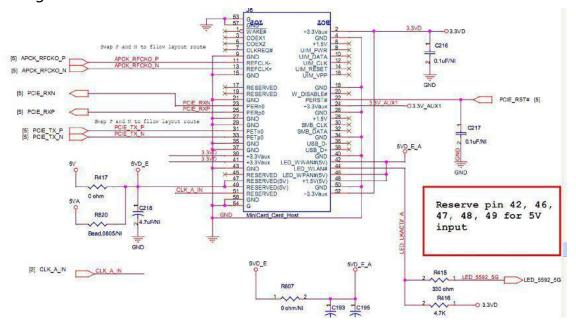
Controlled by the UARTF_SHARE_MODE register.

Pin Name	3'b000 UARTF	3'b001 PCM, UARTF	3'b010 PCM, I2S	3'b011 I2S UARTF	3'b100 PCM, GPIO	3'b101 GPIO, UARTF	3'b110 GPIO I2S	3'b111 GPIO
RIN	RIN	PCMDTX	PCMDTX	RXD	PCMDTX	GPIO#14	GPIO#14	GPIO#14
DSR_N	DSR_N	PCMDRX	PCMDRX	CTS_N	PCMDRX	GPIO#13	GPIO#13	GPIO#13
DCD_N	DCD_N	PCMCLK	PCMCLK	TXD	PCMCLK	GPIO#12	GPIO#12	GPIO#12
DTR_N	DTR_N	PCMFS	PCMFS	RTS_N	PCMFS	GPIO#11	GPIO#11	GPIO#11
RXD	RXD	RXD	12SSDI	12SSDI	GPIO#10	RXD	I2SSDI	GPIO#10
CTS_N	CTS_N	CTS_N	12SSDO	12SSDO	GPIO#9	CTS_N	12SSDO	GPIO#9
TXD	TXD	TXD	I2SWS	12SWS	GPIO#8	TXD	I2SWS	GPIO#8
RTS_N	RTS_N	RTS_N	12SCLK	12SCLK	GPIO#7	RTS_N	I2SCLK	GPIO#7

NOTE: This scheme applies only to the TFBGA package.

8.8 PCIE

One PCIE interface, Can be used as expand the PCIE wifi card(802.11a/802.11ac) and storage.



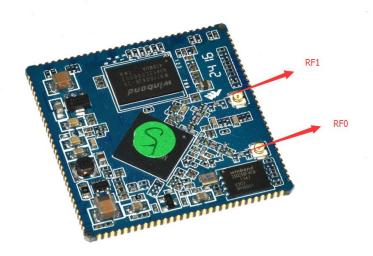


8.9 GPIO

The Core Module Supply One Standard GPIO(GPIO0), But almost 45 GPIO be used with UART Full,RGMII,I2C,ETH,at all. If these Pin is free, you can change it to GPIO mode, Plz Follow MT7620A Datasheet.

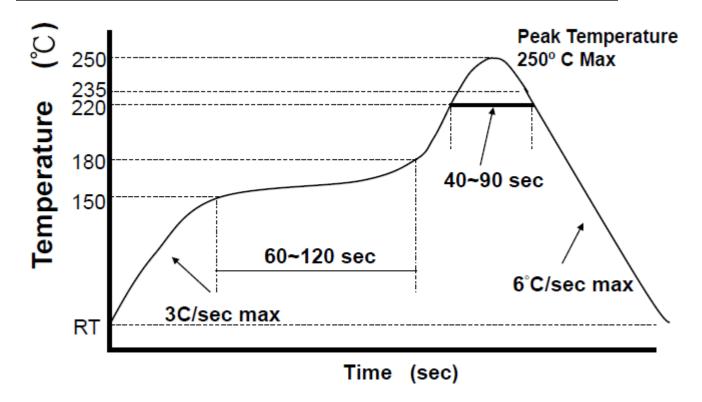
8.10 ANTENNA CONNECTER

The RF switch coaxial connector on the Core Moudle is I-PEX: 20279-001E-01.If the RF connected to the customer's main boad, the RF match circuit and suitable trace should be noted.





9 REFLOW PROFILE GUIDELINE



Notes:

- 1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
- 2. Reflow temperature is defined at the solder ball of package/or the lead of package.
- 3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
- 4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.



10 STRUCTURE

	Length	Width	Height
Size	40.0mm	40.0mm	4.25mm

11 OPERATING ENVIRONMENT

Storage Temperature	-20 °C ~ 70 °C
Storage Humidity	<90% (non-condensing)
Operating Temperature	-20℃ ~ 55℃
Relative humidity	5% ~ 90% (non-condensing)