

GAINSTRONG Oolite V5.1-QCA4531 Spec

Specification Version 1.0.4

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Rev.	Date	Contents of Revision Change	Remark
1.0.1	2016-8-30	Initial release	
1.0.2	2016-11-17	Adjust new template	
1.0.3	2017-11-07	Modifiy the specific shape and size of the module	
1.0.4	2017-12-16	Add the target power of wifi	



1 PRODUCT OVERVIEW

General Description

The OoliteV5.1 is a complete, small 802.11a/b/g/n Wi-Fi Solution optimized for low-cost, and highly integrated AP and consumer electronic devices, the module integrates all Wi-Fi functionality in a package friendly to low-cost PCB design, requiring only a 3.3V power supply.

The module based on the QCA4531 which integrates an 802.11n 2x2. MIMO MAC/BB/ radio with external PA and LNA. TX power up to 23dbm. RX sensitivity up to -75dbm, It supports 802.11 n operations up to 144 Mbps for 20 MHz and 300 Mbps for 40 MHz, compatible 802.11b/g/n.

The module support AP mode, client mode at the same time, and include mass service application software to reduce the research and design work of customer.

Applications Stage

- Smart home network equipment
- Wireless WIFI device, unmanned aerial vehicle
- Dual band Router, Industry Controller and so on.

Features

- ◆ PCI Express 1.1 Root Complex interface for minicpe device
- ◆ One USB 2.0 interface
- ◆ 1 WAN AND 4 LAN Ethernet PORTS
- ◆ One low-speed UART (115 Kbps) and multiple GPIO pins for general purpose I/O
- ◆ Built in 2.4GHz 300Mbps high power wifi transmitter with PA and LNA.
- ◆ 3.3V power supply
- ◆ 128Mbyte RAM and 16Mbyte ROM, max up to 32Mbyte ROM



ltem	type	real target		
	Frequency error	6.0ppm		
	power	CCK 11M 23dbm OFDM 54M 21dbm MCS7(HT20)21dbm MCS7(HT40)21dbm		
Antenna 0	evm	CCK 11M -27.5db OFDM 54M -25db MCS7(HT20)-28db MCS7(HT40)-27db		
	Reception Sensitivity	CCK 11M -89dbm OFDM 54M -75dbm MCS7(HT20)-70dbm MCS7(HT40)-68dbm		

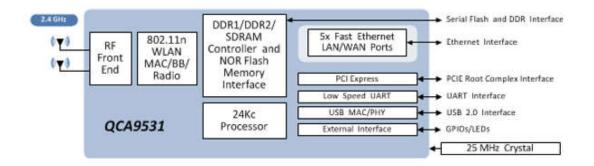
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Antenna 1	evm	CCK 11M -27db OFDM 54M -25db MCS7(HT20)-28db MCS7(HT40)-27db		
	Reception Sensitivity	CCK 11M -89dbm OFDM 54M -75dbm MCS7(HT20)-70dbm MCS7(HT40)-68dbm		



2 Hardware Overview

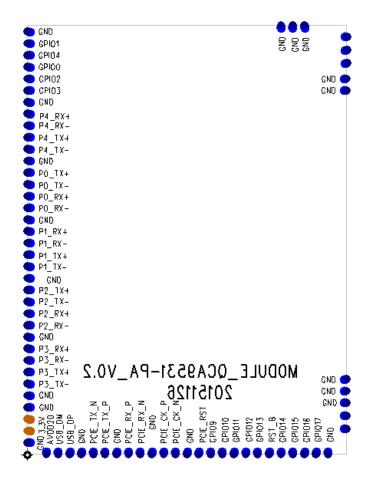
Block Diagram

The general Hardware architecture is shown below Figure:



Module Block Diagram

Pin Assignment





Pin Description

The OoliteV5.1 has 74 pins , including x1 PCI-E channel*1, USB2.0*1, JTAG*1, 1WAN AND 4 LAN Ethernet ports, and many GPIOs.

Pin NO.	Pin name	I/O	Description	Raemark
1	GND	G		
2	GPIO1		TDI	
3	GPIO4		LED_link4	
4	GPIO0	I/O	TCK	JTAG
5	GPIO2		TDO	
6	GPIO3		TMS	
7	GND	G		
8	P4_RX+	- 1	Falson of mont 4 massive main	
9	P4_RX-	I	Ethernet port 4 receive pair	D4
10	P4_TX+	0	Eth can at most 4 transmit nois	P4
11	P4_TX-	0	Ethernet port 4 transmit pair	
12	GND	G		
13	P0_TX+	0	Eth can et most 2 trongenit mair	
14	P0_TX-	0	Ethernet port 2 transmit pair	P0
15	P0_RX+	-	Ethornot port 2 resoive pair	PU
16	P0_RX-	_	Ethernet port 2 receive pair	
17	GND	G		
18	P1_RX+	1	Ethernet port 1 receive pair	
19	P1_RX-	_	Ethernet port 1 receive pair	P1
20	P1_TX+	0	Ethernet port 1 transmit pair	PI
21	P1_TX-)	Ethernet port i transmit pair	
22	GND	G		
23	P2_TX+	0	Ethernet port 2 transmit pair	
24	P2_TX-	0	Ethernet port 2 transmit pair	P2
25	P2_RX+	ı	Ethernet part 2 receive pair	PZ
26	P2_RX-	I	Ethernet port 2 receive pair	
27	GND	G		
28	P3_RX+	I	Ethernet port 3 receive pair	Р3



P3_RX- 30 P3_TX+ 31 P3_TX- 32 GND 33 GND 34 3.3V P 3.3V input 1000mA, recommended voltage 3.3V, Min2.97V, MAX 3.63V Min2.97V, Min2.97V, MAX 3.63V Min2.97V, MAX 3.63V Min2.97V, MAX 3.63V]	ĺ
31	29	P3_RX-			
31	30	P3_TX+	0	Ethernet port 3 transmit pair	
33 GND G Solution G Sol	31	P3_TX-			
33	32	GND	G		
Signature Sig	33	GND	י		
35 3.3V Min2.97V, MAX 3.63V 36 GND G 37 AVDD20 P 38 USB_DM I/O USB 2.0 D- signal 40 GND G 41 PCIE_TX_N 42 PCIE_TX_P 43 GND G 44 PCIE_RX_P 45 PCIE_RX_N 46 GND G 47 PCIE_CK_P O 48 PCIE_CK_N O 49 GND G 49 GND G 50 PCIE_RST I/O PCI Express reset, open drain, should be pulled up to Vdd33 through 1 KΩ resistor 51 GPIO9 I/O UART_SIN 52 GPIO10 I/O UART_SOUT 53 GPIO11 I/O UED_LINK_4 54 GPIO12 I/O WLAN_LED 55 GPIO13 I/O SYS_LED 56 RST_B I/O Otherwise the RESET_L input must be driven with 3.3 V logic.	34	3.3V	D	3.3V input 1000mA, recommended voltage 3.3V,	
37	35	3.3V	r	Min2.97V, MAX 3.63V	
38	36	GND	G		
39 USB_DP I/O USB 2.0 D+ signal 40 GND G 41 PCIE_TX_N 42 PCIE_TX_P 43 GND G 44 PCIE_RX_P 45 PCIE_RX_N 46 GND G 47 PCIE_CK_P O 48 PCIE_CK_N O 49 GND G 50 PCIE_RST I/O 51 GPIO9 52 GPIO10 53 GPIO11 54 GPIO12 55 GPIO13 56 RST_B 1/O USB 2.0 D+ signal USB2.0 Differential transmit PCIE_TX PCIE_TX PCIE_TX PCIE_TX PCIE_CLK PCIE_RX PCIE_RX PCIE_CLK PCIE_ST UART_SIN UART_SOUT UART_SOU	37	AVDD20	Р		
39	38	USB_DM	I/O	USB 2.0 D- signal	110000
41	39	USB_DP	I/O	USB 2.0 D+ signal	USB2.0
PCIE_TX PCIE_TX PCIE_TX	40	GND	G		
42 PCIE_TX_P 43 GND G 44 PCIE_RX_P 45 PCIE_RX_N 46 GND G 47 PCIE_CK_P O 48 PCIE_CK_N O 49 GND G 50 PCIE_RST 1/O PCI Express reset, open drain, should be pulled up to Vdd33 through 1 KΩ resistor 51 GPIO9 52 GPIO10 53 GPIO11 I/O LED_LINK_4 54 GPIO12 I/O WLAN_LED 55 GPIO13 I/O SYS_LED This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	41	PCIE_TX_N	_		_
A4	42	PCIE_TX_P	0	Differential transmit	PCIE_TX
PCIE_RX_N PCIE_RX 45	43	GND	G		
45 PCIE_RX_N 46 GND G 47 PCIE_CK_P O 48 PCIE_CK_N O 49 GND G 50 PCIE_RST I/O 51 GPIO9 52 GPIO10 53 GPIO11 I/O 54 GPIO12 I/O 55 GPIO13 I/O FOIE_RST I/O FOIE_CLK FOIE_CLK PCIE_CLK PCIE	44	PCIE_RX_P			
47 PCIE_CK_P O Differential reference clock (100 MHz) PCIE_CLK 48 PCIE_CK_N O G 49 GND G 50 PCIE_RST I/O PCI Express reset, open drain, should be pulled up to Vdd33 through 1 KΩ resistor 51 GPIO9 I/O UART_SIN UART 52 GPIO10 I/O LED_LINK_4 53 GPIO11 I/O WLAN_LED 55 GPIO13 I/O SYS_LED 56 RST_B I/O This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	45	PCIE_RX_N	I	Differential receive	PCIE_RX
Differential reference clock (100 MHz) PCIE_CLK	46	GND	G		
48 PCIE_CK_N O 49 GND G 50 PCIE_RST I/O PCI Express reset, open drain, should be pulled up to Vdd33 through 1 KΩ resistor 51 GPIO9 I/O UART_SIN 52 GPIO10 I/O LED_LINK_4 54 GPIO12 I/O WLAN_LED 55 GPIO13 I/O SYS_LED This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	47	PCIE_CK_P	0	716	
PCIE_RST I/O PCI Express reset, open drain, should be pulled up to Vdd33 through 1 KΩ resistor	48	PCIE_CK_N	0	Differential reference clock (100 MHz)	PCIE_CLK
FCIE_RST I/O up to Vdd33 through 1 KΩ resistor	49	GND	G		
52 GPIO10 I/O UART_SOUT 53 GPIO11 I/O LED_LINK_4 54 GPIO12 I/O WLAN_LED 55 GPIO13 I/O SYS_LED This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	50	PCIE_RST	I/O	·	
52 GPIO10 UART_SOUT 53 GPIO11 I/O LED_LINK_4 54 GPIO12 I/O WLAN_LED 55 GPIO13 I/O SYS_LED This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	51	GPIO9		UART_SIN	
54 GPIO12 I/O WLAN_LED 55 GPIO13 I/O SYS_LED This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	52	GPIO10	1/0	UART_SOUT	UART
55 GPIO13 I/O SYS_LED This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	53	GPIO11	I/O	LED_LINK_4	
This signal is internally pulled up to 3.3 V. It is recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	54	GPIO12	I/O	WLAN_LED	
recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with 3.3 V logic.	55	GPIO13	I/O	SYS_LED	
57 GPIO14 I/O LED_LINK_3	56	RST_B	I/O	recommended to leave this signal floating if resetting the chip externally is not required. Otherwise the RESET_L input must be driven with	
	57	GPIO14	I/O	LED_LINK_3	



58	GPIO15	I/O	LED_LINK_2			
59	GPIO16	I/O	LED_LINK_1			
60	GPIO17	I/O				
61	GND					
62	GND	G				
63	AT	0	nc			
64	GND					
65	GND					
66	GND	G				
67	GND	G				
68	GND			İ		
69	GND					
70	AT	0	nc			
71	GND					
72	GND	G				
73	GND	. u				
74	GND					



3 ELECTRICAL CHARACTERISTICS

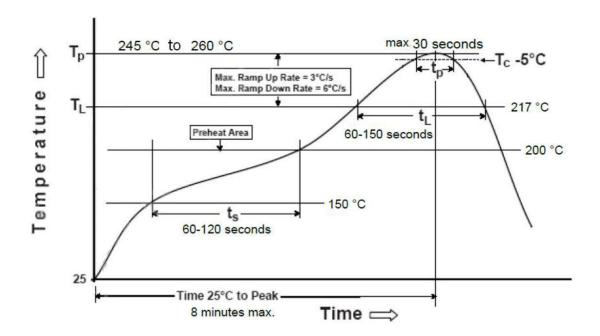
Absolute Maximum Ratin	g								
Parameter	Symbol	Min	Max	Units					
Power Supply Voltage									
3.3V	3.3	-0.3	3.6	٧					
GND	0	-0.3		V					
GPIO Voltage									
VIH	1.2	0.5	1.5	V					
VIL		-0.3	0.12	٧					
VOH	1.2	1.1	1.23	٧					
VOL		-0.3	0.12	٧					
Power Supply Current			•						
3.3V	1	0.95	1.2	Α					
GPIO Current	GPIO Current								
IIH			10	uA					
IOH			9	mA					
Environment									
Storage Temperature	Tstg	-40	80	°C					
Peak Reflow Soldering Temperature <10s	Tpeak		260	°C					
Humidity			95	%					



4 Manufacturing Process Recommendations

When the module is welded, please note that it's heating time and heating temperature, if you do not know how to set the corresponding parameters, please refer to the following figure, it helps to make the module get good welding performance, and not to appear unnecessary problems. Of course, you can adjust according to the actual situation.

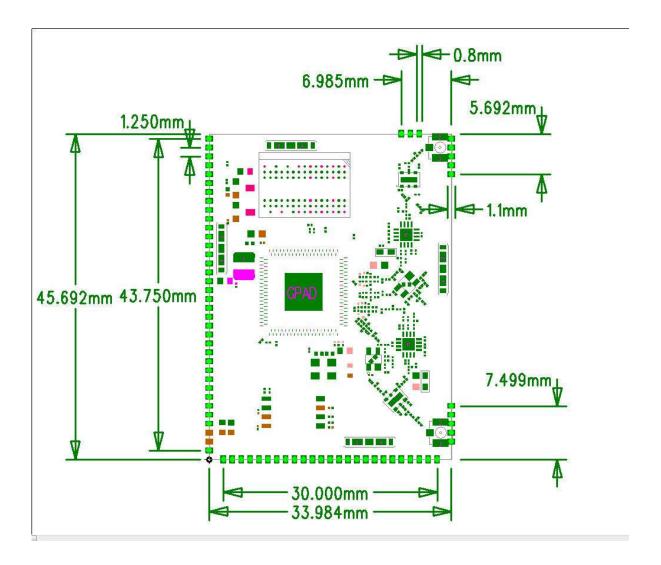
Manufacturing Process Recommendations





5 RECOMMEND LAYOUT

The following figure is the specific shape and size of the module, you can adjust your PCB package, in order to facilitate Lay out.



6 REFERENCE DESIGN SCHEMATIC

Please refer to the http://www.ooioe.com/oolitev5/openwrt