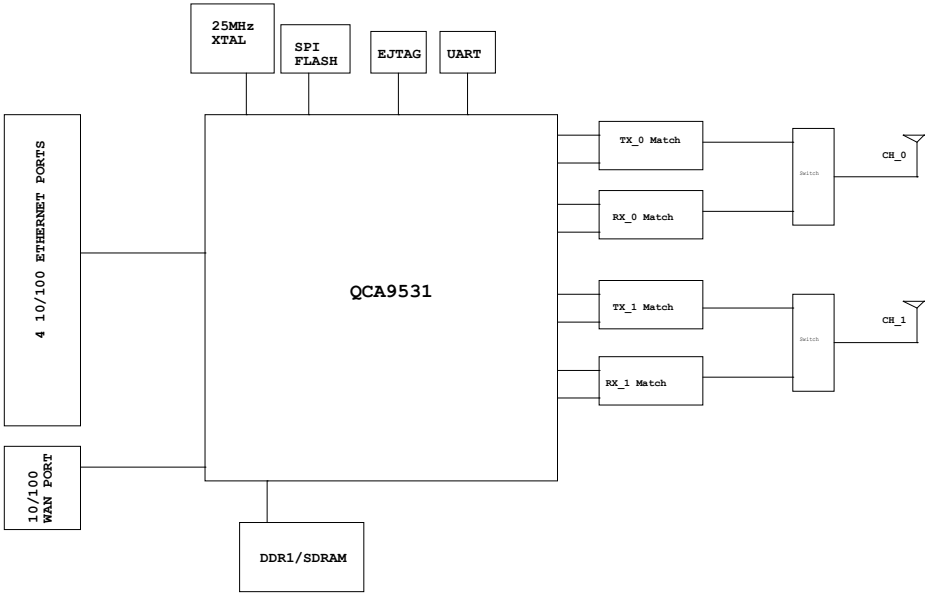


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DATE	REVISION NUMBER	INITIALS	DESCRIPTION
06 Dec 2012	245-02483-010	SC	INITIAL REVISION
14 Mar 2013	245-02483-020	RK	- Removed C138 - 1uF ; C11 - 0.1uF ;C9 - 10uF ;C130 - 1uF to improve 1.2V switching regulator noise - Replaced R39, R37 - 22E R39, R40 - 27E R170, R165 - 27E for better DDR operation with Winbond devices - Replaced C155 - 4700pF, Added C20 - 0.1uF ; C21 - 1uF to reduce noise in VDD12_SYNTH - Replaced R4 - 0 Ohms (0201) R122, R125 - 220 Ohm 3A ferrite bead C65, C68 - 22uF C9 (N1) C11 - 0.1uF Overall to reduce Clock Jitter R200 - 150E shunt cap for DDR Clock - Replaced C332 - 0.8pF to correct Pout imbalance between Chain-0 & Chain-1
18 Mar 2013	245-02483-020	RK	- Replaced C103, C104 - 1uF C162, C157 - 100pF No load - C4, C3, C38, C96, C100, C166, C169, C153 & C111 R2 - 600 Ohm @ 100 Mhz
26 Mar 2013	245-02483-030	RK	C142, C184 - No load C182, C133 - Cap size changed to 0402 Removed R124 C176, C178 - 1.2pF Added Pi filter L27, L28 - 2.2mH; C185, C189 - 1.2pF @ Rx Ch-0 & Ch-1 C42 - 1uF; Added C154 - 10uF for VDD_PU supply
28 Mar 2013	245-02483-030	RK	- Replaced C11, C147, C148, C150, C134 = 1uF C3 = 10uF R2 - 0 Ohms R4 = 70 Ohm 600mA ferrite bead C72 - 22uF loaded; C94 - No Load cap added for USB supply at the connector side
27 May 2013	245-02483-031	Nagendra	- Replaced 16MB DDR(U7) memory with 32MB DDR Notload R3,R206,C177,L22,C188,L23 Added shield L10,11,17,18 changed to 3nH and L19,20,21,24 Changed to 0 ohm.
7 June 2013	ECO-C431999	Nagendra	Template changed for Agile updation

CONTRACT NO.		QUALCOMM Atheros, INC. 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110 U.S.A.	
DRAWN BY Nagendra & Nagendra	DATE 7th June 2013	TITLE	
ENGINEER		SCHEMATIC	
PROJECT ENGINEER		CCA, AP143, QCA9531 Honeybee, Based 802.11 b/g/n Access point	
QUALITY ASSURANCE			
CONFIGURATION			
DESIGN ACTIVITY APPROVAL		SIZE D	DRAWING NO LD20-Y5935
DESIGN APPROVAL		SCALE NONE	RELEASE DATE 1 of 7

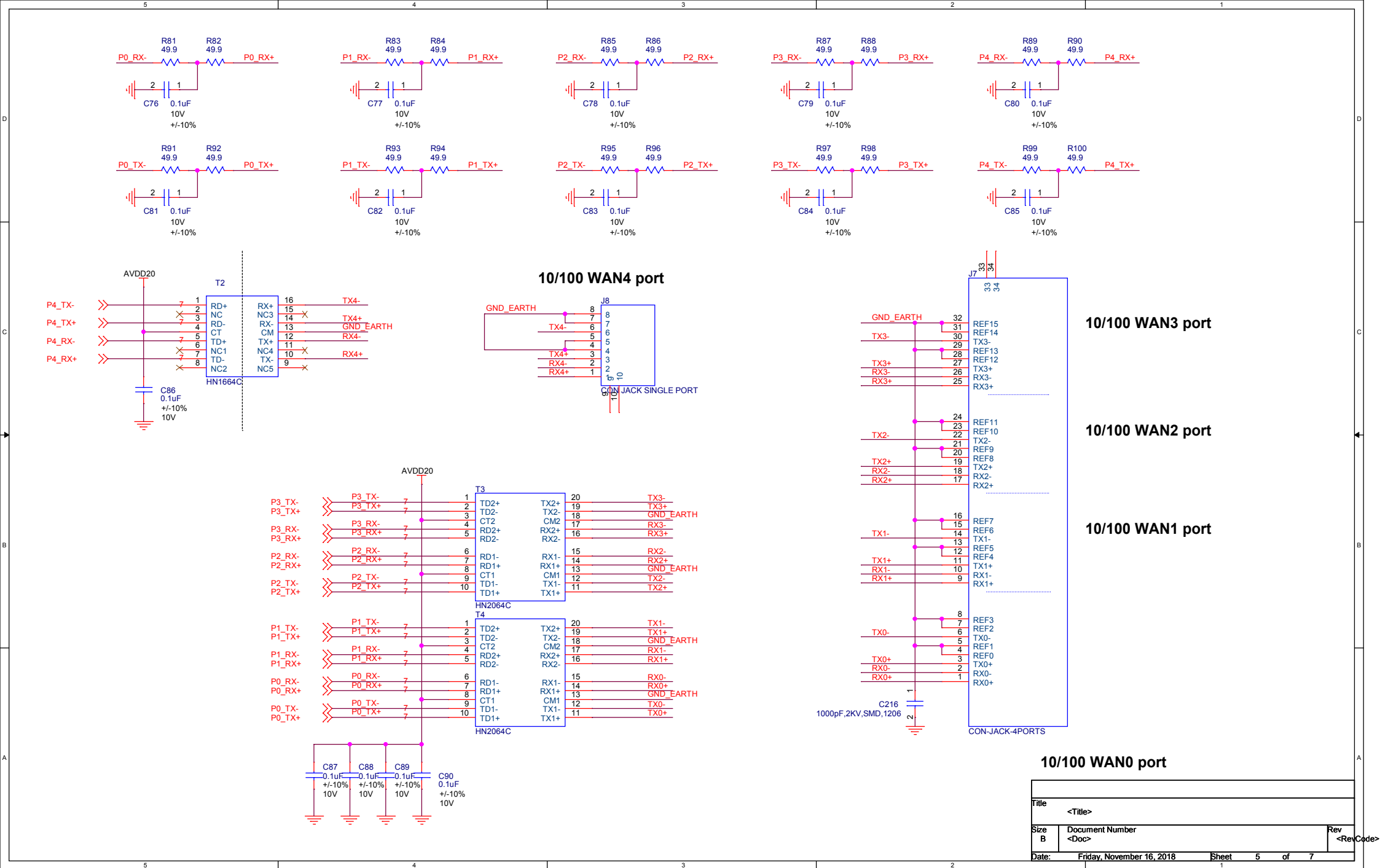


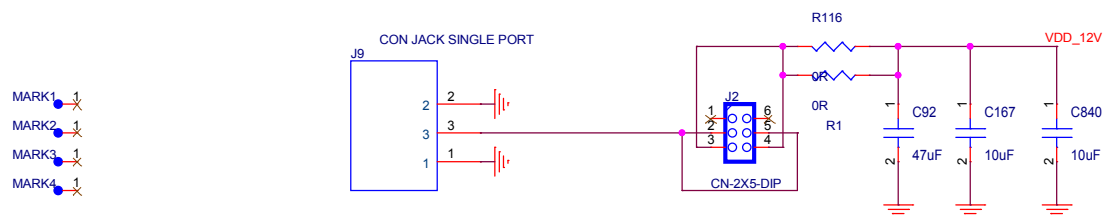
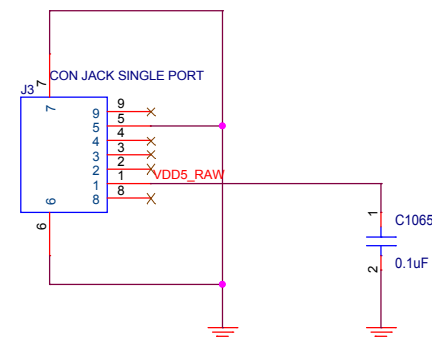
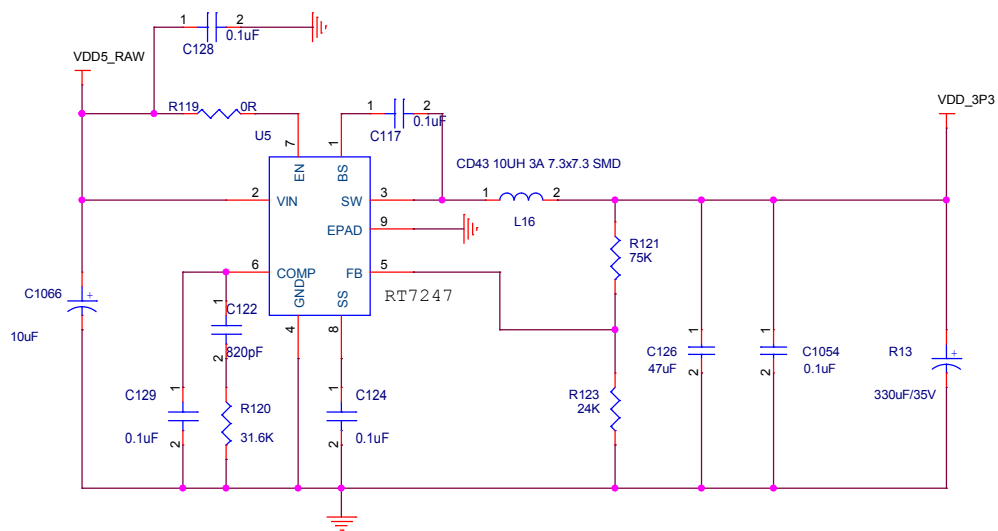
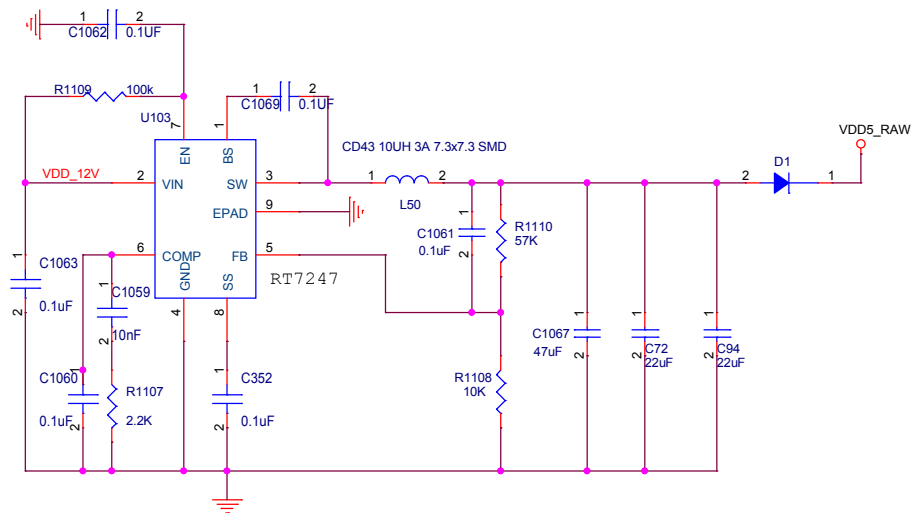
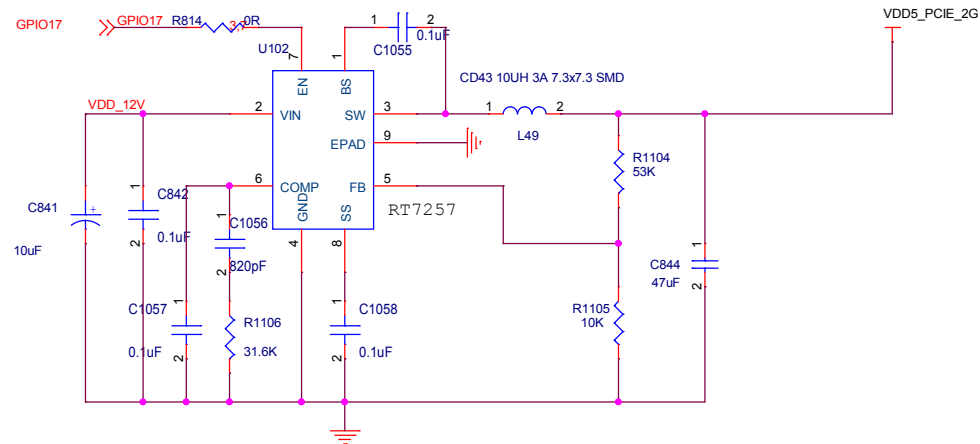
TITLE			
CCA, AP143, QCA9531 Honeybee, Based 802.11 b/g/n Access point			
QUALCOMM Atheros, INC. 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110 U.S.A	SIZE	DRAWING NO	REV
	D	LD26-YB35	A
SCALE NONE		SHEET	2 OF 7

The schematic diagram illustrates the electrical connections for a USB A Type Receptacle Up-Right Single Deck (Thru-Hole). The USB connector (J6) is connected to the USB controller (U1) and the USB port (U2). The connections are as follows:

- Ground (GND):** J6 pins 8, 5, 1, and 2 are connected to GND. J6 pins 3, 4, 6, and 7 are connected to GND1. J6 pin 9 is connected to GND2.
- USB_M:** J6 pin 1 is connected to USB_M. USB_M is connected to U1 pin 1 and U2 pin 1.
- USB_DP:** J6 pin 2 is connected to USB_DP. USB_DP is connected to U1 pin 2 and U2 pin 2.
- USB_DM:** J6 pin 3 is connected to USB_DM. USB_DM is connected to U1 pin 3 and U2 pin 3.
- Power (VDD5_RAW):** J6 pin 4 is connected to VDD5_RAW. VDD5_RAW is connected to U1 pin 4 and U2 pin 4.
- Resistors:** R38 (0R/1206) is connected between USB_M and VDD5_RAW. R30 (1R0/201) is connected between USB_M and USB_DM. R32 (0R/201) is connected between USB_DP and VDD5_RAW. R34 (1R0/201) is connected between USB_DP and USB_DM.
- Capacitors:** C121 (0.1uF/0402) is connected between VDD5_RAW and GND. C1064 (22uF/C0805) is connected between VDD5_RAW and GND. C75 (1uF/0402) is connected between USB_DP and GND. C74 (1uF/0402) is connected between USB_DM and GND.

QUALCOMM ATHEROS, INC. 1700 TECHNOLOGY DRIVE SAN JOSE, CA 95110 U.S.A	TITLE CCA, AP143, QCA9531 Honeybee, Based 802.11 b/g/n Access point	
	SIZE D	DRAWING NO LD20-Y5935
	SCALE NONE	REV A
		SHEET 3 OF 7





MARK1 1
MARK2 1
MARK3 1
MARK4 1

