GAINSTRONG

Oolite V3.0_SPEC_EN

Specification Version 1.0.0

Author：Bruce Lee

April 18, 2018

GainStrong Industry Co.,Ltd. http://www.gainstrong.cn
Tell:+86-755-81720165support@gainstrong.cn

Rev.	Date	Contents of Revision Change	Remark
1.0.0	2018-04-18	Initial release	

GainStrong Industry Co.,Ltd. http://www.gainstrong.cn
Tell:+86-755-81720165support@gainstrong.cn

INTRODUCTION

This Module use MT7688AN, it can support an EMMC for storage ,there also has a PCB ANTA on board and a IPX ANTA seat for alternative.What' s more,we lead out all function and I/O ports for expand.

The MT7688AN integrated a 1T1R 802.11n WiFi radio,a 580 MHZ MIPS 24KEc CPU,1port fast Ethernet PHY,USB2.0 host,PCIe,SD-XC,I2S/PCM and multi slow IOs.MT7688AN provide two operrtion modes-IoT gateway mode and IoT device mode.In IoT gateway mode,the PCI Express interface can connect to 802.11ac chipset for 11ac dule-band concurrent gateway.The high performance USB2.0 allows MT7688an to add 3G/LTE modem support or add a H.264 ISP for wireless IP camera.For the IoT device mode,MT7688AN supports eMMC,SD-XC and USB2.0. MT7688AN can support the WiFi high quality audio via 192Kbps/24bits I2S interface and

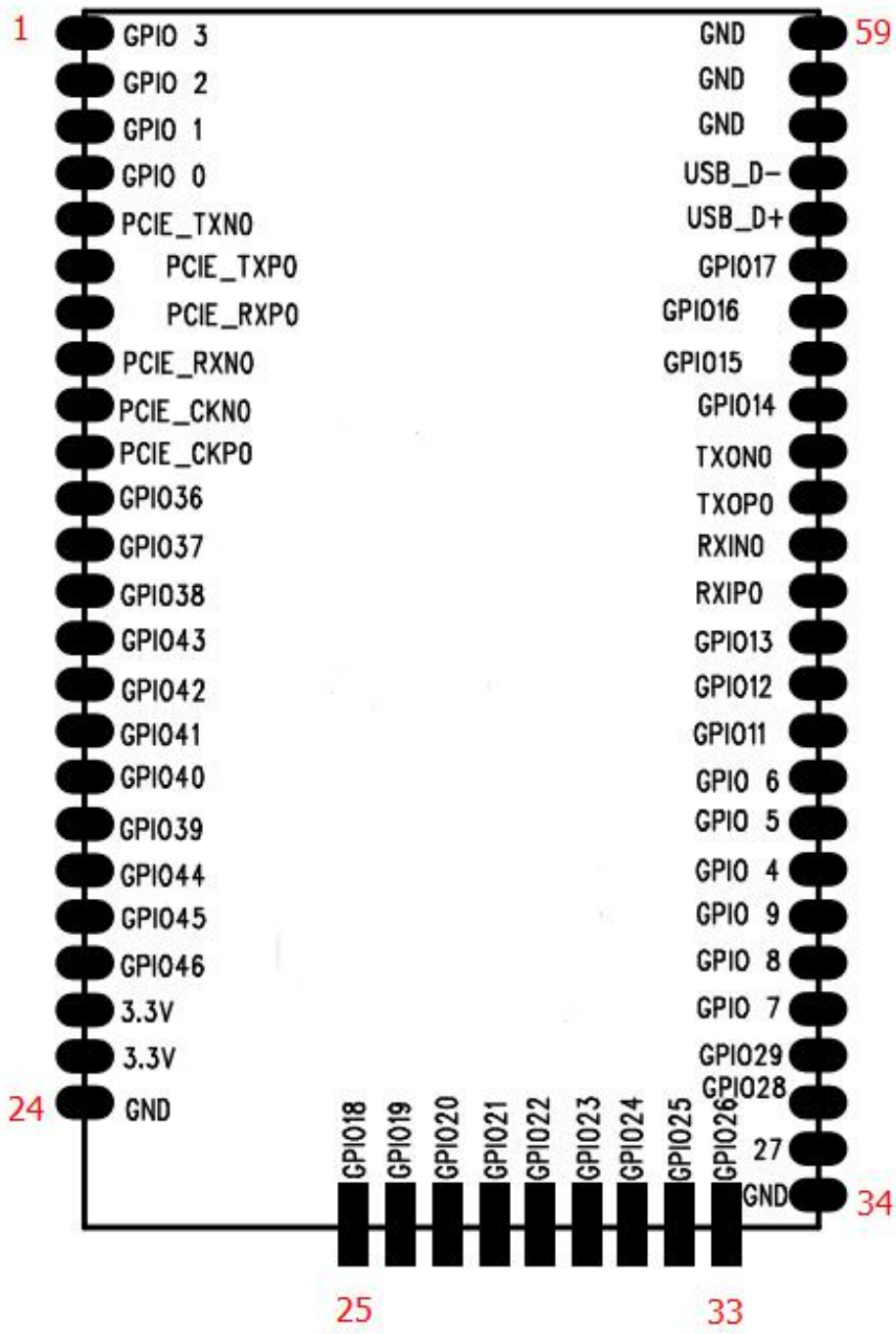
VoIP application through PCM. In IoT device mode,it further supports PWM,SPI slave,3rd UART and more GPIOs.For IoT gateway,it can connect to touch panel and BLE,Zigbee/Z-Wave and sub-1G RF for smart home control.

FEATURES

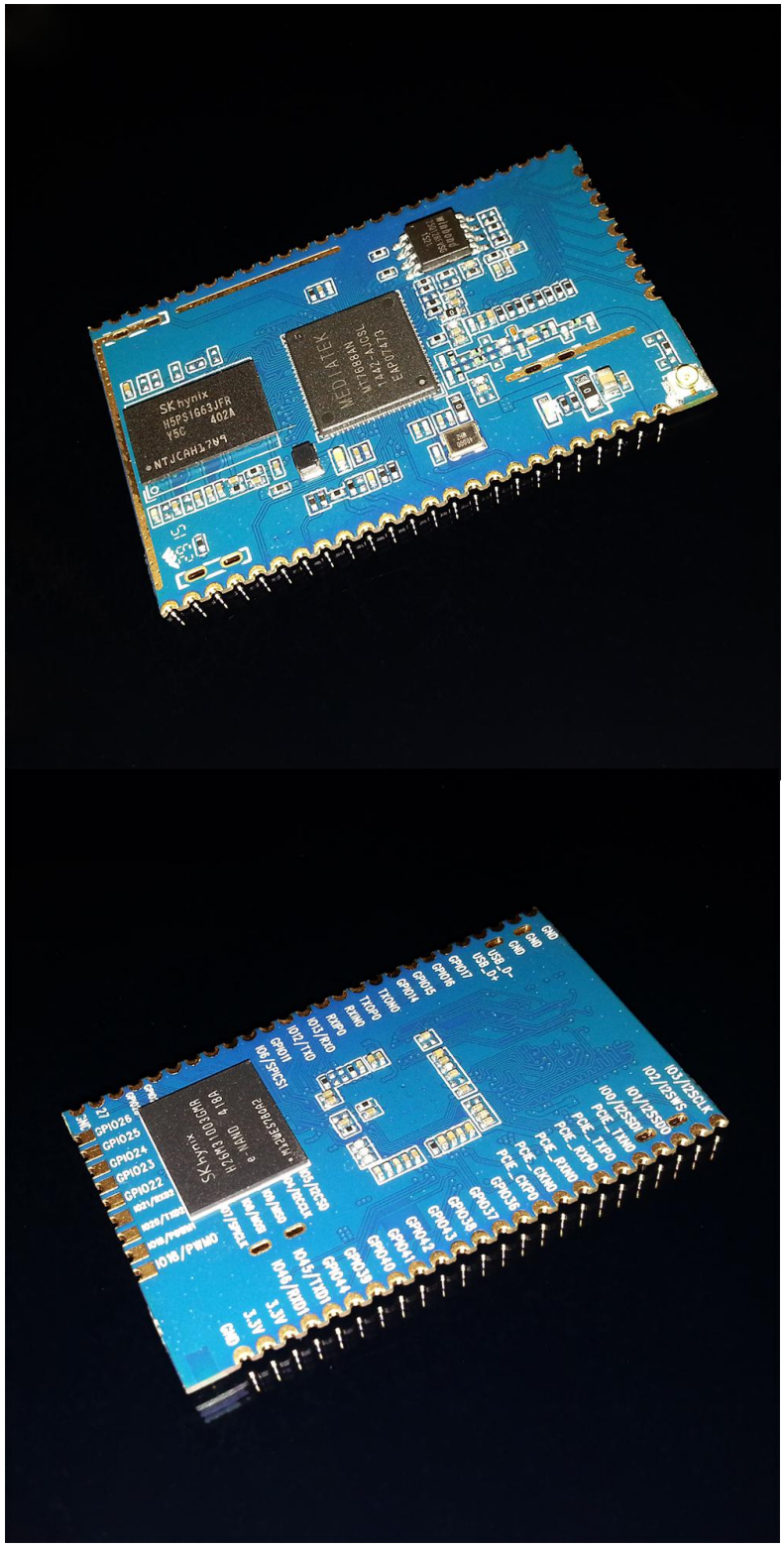
- **CPU** ：MT7688AN with 580 MHZ MIPS 24KEc ;
- **RAM** ：64MByte DDR2 RAM(32M/128M/256M options) ;
- **Flash** ：16Mbyte SPI NOR Flash ROM(4M/8M/32M/64M options) ;
- **EMMC** ：null(4G/8G/16G/32G/64G options) ;
- **Wireless speed** ：150Mbps ;
- **GPIO**：37 ;
- **USB**： 1*Usb 2.0 master interface, support USB hub extension ;
- **Ethernet:** 1*Ethnet port (IOT Mode)/5*Ethnet Port(Gateway Mode);
- **Antenna :**1*IPEX Antenna;
- **Power supply voltage**：3.3V ;
- **Product size** ： 31.5mm * 52.5mm*3.6mm(±0.1mm).

CPU	MT7688AN with 580 MHZ MIPS 24KEc
RAM	64MByte DDR2 RAM(32M/128M/256M options)
Flash	16Mbyte SPI NOR Flash ROM(4M/8M/32M/64M options)
EMMC	null(4G/8G/16G/32G/64G options)
Wireless speed	150Mbps
GPIO	37
USB	1*Usb 2.0 master interface, support USB hub extension ;
Ethernet	1*Ethnet port (IOT Mode)/5*Ethnet Port(Gateway Mode);
Antenna	1*IPEX Antenna
Power supply voltage	3.3V
Port	WAN +PCIE interface
Antenna	on board antenna /IPX external antenna.
Debug	serial debugging interface has lead out.
Product size	31.5mm * 52.5mm*3.6mm(±0.1mm)
High-speed UART for console support	

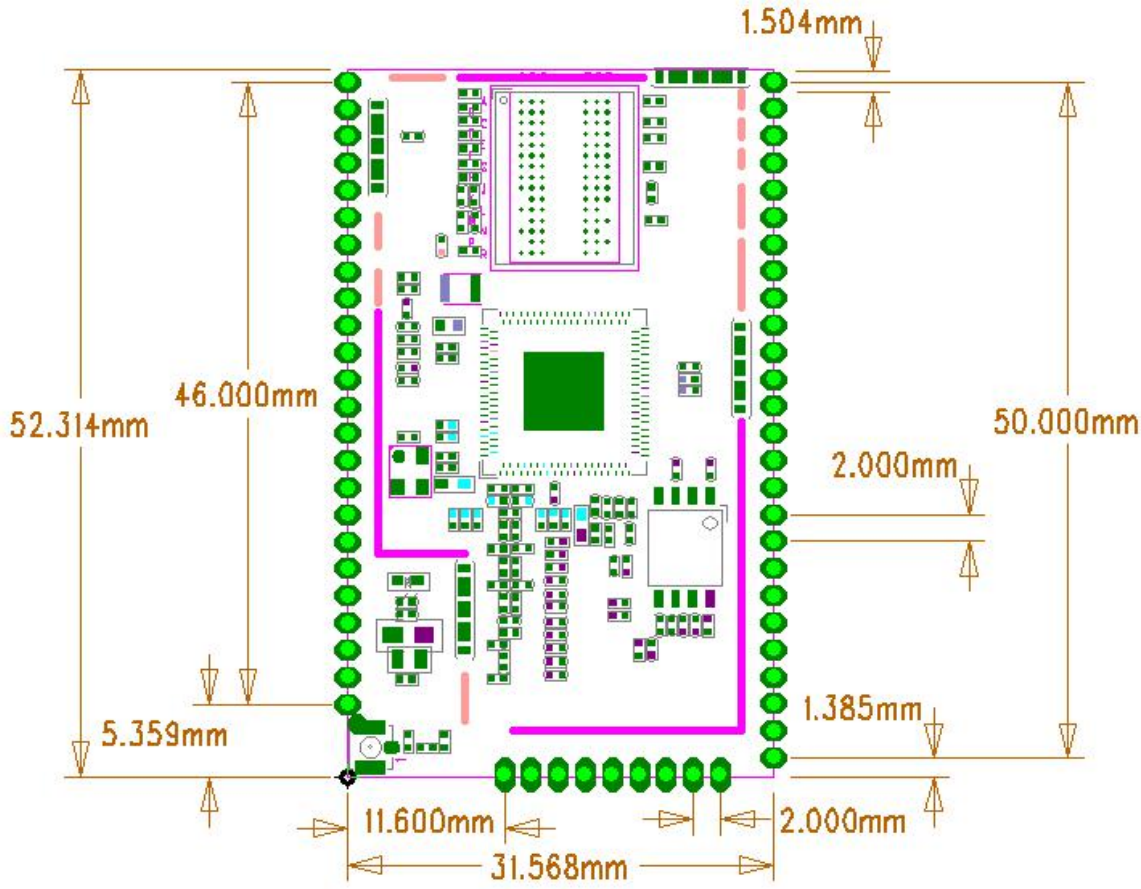
PINS DISTRIBUTE



PICTURES


SK hynix
H5PS1663JFR
Y5C 402A
MEDIATEK
GND
GND
USB_D-
USB_D+
GPIO7
GPIO6
GPIO5
GPIO4
TXD0
RXD0
RXFD
IO13/RXD
IO12/TXD
GPIO11
IO9/SPICS1
GPIO28
GPIO25
GPIO24
GPIO23
GPIO22
IO18/PWM0
IO46/TXD1
IO44/RXD1
GPIO44
GPIO43
GPIO42
GPIO41
GPIO40
GPIO39
GPIO38
GPIO37
GPIO36
PCIE_CKP0
PCIE_CKN0
PCIE_RXP0
PCIE_RXN0
PCIE_TXP0
PCIE_TXN0
IO1/I2SSDO
IO2/I2SWS
IO3/I2SCLK
3.3V
GND

PHYSICAL DEMENSIONS(REFERENCE FOR MAINBOARD DESIGN)



GainStrong Industry Co.,Ltd. http://www.gainstrong.cn
Tell:+86-755-81720165support@gainstrong.cn

PINS DESCRIPTION

Pin No.	Name	GPIO state(default)	Reuse(default)
P1	GPIO3	I/O	I2S_CLK
P2	GPIO2	O	I2S_WS
P3	GPIO1	I/O, pull low to GND	I2S_SDO
P4	GPIO0	O	I2S_SDI
P5	PCIE_TXN0	I/O	PCIE_TXN0
P6	PCIE_TXP0	I/O	PCIE_TXP0
P7	PCIE_RXP0	I/O	PCIE_RXP0
P8	PCIE_RXN0	I/O	PCIE_RXN0
P9	PCIE_CKN0	I/O	PCIE_CKN0
P10	PCIE_CKP0	I/O	PCIE_CKP0
P11	GPIO36	O, pull high to3.3V	PERST_N
P12	GPIO37	O,IPL	REFCLKO
P13	GPIO38	O, pull high to3.3V	WDT_RST_N
P14	GPIO43	I/O	P0_LED_AN
P15	GPIO42	I/O	P1_LED_AN
P16	GPIO41	I/O	P2_LED_AN
P17	GPIO40	I/O	P3_LED_AN
P18	GPIO39	I/O	P4_LED_AN
P19	GPIO44	O	WLAN_LED
P20	GPIO45	O, pull high to3.3V	UART_TXD1
P21	GPIO46	I	UART_RXD1
P22	3.3V	POWER	
P23	3.3V	POWER	
P24	GND	ground	
P25	GPIO18	A, pull high to3.3V	EMMC_D7
P26	GPIO19	A, pull high to3.3V	EMMC_D6

P27	GPIO20	A, pull high to3.3V	EMMC_D5
P28	GPIO21	A, pull high to3.3V	EMMC_D4
P29	GPIO22	A, pull high to3.3V	EMMC_WP
P30	GPIO23	A, pull low to GND	EMMC_CD
P31	GPIO24	A, pull low to GND	EMMC_D1
P32	GPIO25	A, pull high to3.3V	EMMC_D0
P33	GPIO26	A	EMMC_CLK
P34	GND		
P35	GPIO27	A	EMMC_CMD
P36	GPIO28	A, pull high to3.3V	EMMC_D3
P37	GPIO29	A, pull high to3.3V	EMMC_D2
P38	GPIO7	O,IPU	SPI_CLK
P39	GPIO8	I/O,IPD	SPI_MOSI
P40	GPIO9	I/O	SPI_MISO
P41	GPIO4	I/O,pull high to3.3V	I2C_SCL
P42	GPIO5	I/O,pull high to3.3V	I2C_SDA
P43	GPIO6	O, pull low to GND	I/O
P44	GPIO11	I/O,IPL	I/O
P45	GPIO12	O, pull low to GND	UART_TXD0
P46	GPIO13	I, pull low to GND	UART_RXD0
P47	RXIP0	A	RXIP0(WAN)
P48	RXIN0	A	RXIN0(WAN)
P49	TXOP0	A	TXOP0(WAN)
P50	TXON0	A	TXON0(WAN)
P51	GPIO14	A	I/O
P52	GPIO15	A	I/O
P53	GPIO16	A	I/O
P54	GPIO17	A	I/O
P55	USB_D+	I/O	USB_D+

P56	USB_D-	I/O	USB_D-
P57	GND		
P58	GND		
P59	GND		

NOTE：

I:Input

O:Ouput

I/O:Bi-directional

IPL:Internal pull low

A:Analog

3.1 Absolute Maximum Ratings

I/O supply voltage	3.63 V
Input, Output, or I/O Voltage	GND -0.3 V to Vcc +0.3 V

PIN SHARE SCHEME(GPIO REUSE)

2.3.2 UART1 pin share scheme

Controlled by the UART1_MODE register.

Pin Name	2'b00 UART-Lite #1	2'b01 GPIO	2'b10 PWM	2'b11 TRX_SW
UART1_RXD	UART1_RXD	GPIO#46	PWM_CH1	
UART1_TXD	UART1_TXD	GPIO#45	PWM_CH0	

2.3.3 MT7688AN EPHY LED pin share scheme

Controlled by the P#_LED_AN_MODE registers

Pin Name	Bootstrapping (DBG_JTAG_MODE=1)	Bootstrapping (DBG_JTAG_MODE=0)	
		P4_LED_AN_MODE =2'b00	P4_LED_AN_MODE =2'b01
EPHY_LED4_N_JTRST_N	JTAG_RST_N	EPHY_LED4_N	GPIO#39
		P3_LED_AN_MODE =2'b00	P3_LED_AN_MODE =2'b01
EPHY_LED3_N_JTCLK	JTAG_CLK	EPHY_LED3_N	GPIO#40
		P2_LED_AN_MODE =2'b00	P2_LED_AN_MODE =2'b01
EPHY_LED2_N_JTMS	JTAG_TMS	EPHY_LED2_N	GPIO#41
		P1_LED_AN_MODE =2'b00	P1_LED_AN_MODE =2'b01
EPHY_LED1_N_JTDI	JTAG_TDI	EPHY_LED1_N	GPIO#42
		P0_LED_AN_MODE =2'b00	P0_LED_AN_MODE =2'b01
EPHY_LED0_N_JTDO	JTAG_TDO	EPHY_LED0_N	GPIO#43

2.3.4 MT7688AN WLAN LED pin share scheme

Controlled by the WLED_AN_MODE registers

Pin Name	2'b00	2'b01
WLED_N	WLED_N	GPIO#44

2.3.7 PERST_N pin share scheme

Controlled by the PERST_ MODE register.

Pin Name	1'b0	1'b1
PERST_N	PERST_N	GPIO#36

2.3.8 WDT_RST_N pin share scheme

Controlled by the WDT _MODE register.

Pin Name	1'b0	1'b1
WDT_RST_N	WDT_RST_N	GPIO#37

2.3.9 REF_CLKO pin share scheme

Controlled by the REFCLK _MODE register.

Pin Name	1'b0	1'b1
REF_CLKO	REF_CLKO	GPIO#38

2.3.10 UART0 pin share scheme

Controlled by the UART0 _MODE register.

Pin Name	1'b0	1'b1
UART_TXD0	UART_TXD0	GPIO#12
UART_TXD0	UART_RXD0	GPIO#13

2.3.11 GPIO0 pin share scheme

Controlled by GPIO_MODE register.

Pin Name	2'b00	2'b01	2'b10	2'b11
GPIO0	GPIO#11	GPIO#11	REF_CLKO	PERST_N

2.3.12 SPI pin share scheme

Controlled by SPI_ MODE register.

Pin Name	1'b0	1'b1
SPI_CLK	SPI_CLK	GPO#7
SPI_MOSI	SPI_MOSI	GPO#8
SPI_MISO	SPI_MISO	GPIO#9
SPI_CS0	SPI_CS0	GPIO#10

2.3.13 SPI_CS1 pin share scheme

Controlled by SPI_CS1_MODE register.

Pin Name	2'b00	2'b01	2'b10
SPI_CS1	SPI_CS1	GPIO#6	REF_CLKO

2.3.14 I2C pin share scheme

Controlled by I2C_MODE register.

Pin Name	2'b00	2'b01
I2C_SCLK	I2C_SCLK	GPIO#4
I2C_SD	I2C_SD	GPIO#5

2.3.15 I2S pin share scheme

Controlled by I2S_MODE register.

Pin Name	2'b00	2'b01	2'b10
I2S_SDI	I2C_SCLK	GPIO#0	PCMDRX
I2S_SDO	I2C_SD	GPIO#1	PCMDTX
I2S_WS	I2C_SCLK	GPIO#2	PCMCLK
I2S_CLK	I2C_SD	GPIO#3	PCMFS

2.3.16 SD pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
Pin Name		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	SD_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	SD_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	SD_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	SD_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	SD_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	SD_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	SD_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	SD_D3	GPIO#29

2.3.17 eMMC pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
Pin Name		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	eMMC_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	eMMC_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	eMMC_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	eMMC_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	eMMC_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	eMMC_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	eMMC_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	eMMC_D3	GPIO#29

2.3.18 UART2 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and UART2_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_TP_P2	MDI_TP_P2	UART_TXD2	GPIO#20	PWM_CH2	eMMC_D5
MDI_TN_P2	MDI_TN_P2	UART_RXD2	GPIO#21	PWM_CH3	eMMC_D4

2.3.19 PWM_CH1 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM1_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_RN_P2	MDI_RN_P2	PWM_CH1	GPIO#19		eMMC_D6

2.3.20 PWM_CH0 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM0_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_RP_P2	MDI_RP_P2	PWM_CH0	GPIO#18		eMMC_D7

2.3.21 SPIS pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SPIS_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_TP_P1	MDI_TP_P1	SPIS_CS	GPIO#14		PWM_CH0
MDI_TN_P1	MDI_TN_P1	SPIS_CLK	GPIO#15		PWM_CH1
MDI_RP_P1	MDI_RP_P1	SPIS_MISO	GPIO#16		UART_TXD2
MDI_RN_P1	MDI_RN_P1	SPIS_MOSI	GPIO#17		UART_RXD2

2.3.22 Pin share function description

Pin Share Name	I/O	Pin Share Function description
PCMDTX	O	PCM Data Transmit DATA signal sent from the PCM host to the external codec.
PCMDRX	I	PCM Data Receive DATA signal sent from the external codec to the PCM host.
PCMCLK	I/O	PCM Clock The clock signal can be generated by the PCM host (Output direction), or provided by an external clock (input direction). The clock frequency should match the slot configuration of the PCM host. e.g. 4 slots, PCM clock out/in should be 256 kHz. 8 slots, PCM clock out/in should be 512 kHz. 16 slots, PCM clock out/in should be 1.024 MHz. 32 slots, PCM clock out/in should be 2.048 MHz. 64 slots, PCM clock out/in should be 4.096 MHz. 128 slots, PCM clock out/in should be 8.192 MHz.
PCMFS	I/O	PCM SYNC signal. In our design, the direction of this signal is independent of the direction of PCMCLK. Its direction and mode is configurable.

Pin Share Name	I/O	Pin Share Function description
PWM_CH0	O	Pulse Width Modulation Channle 0
PWM_CH1	O	Pulse Width Modulation Channle 1
PWM_CH2	O	Pulse Width Modulation Channle 2
PWM_CH3	O	Pulse Width Modulation Channle 3

2.4 Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7688AN only. It needs to be pull-low for 7688KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

STRUCTURE

	Length	Width	Height
Size	31.5mm	52.5mm	3.6mm

OPERATING ENVIRONMENT

Operating Temperature	-20℃ ~ 55℃
Operating Humidity	<60% non-condensing
Storage Temperature	0℃ ~ 40℃
Storage Humidity	Storage Humidity: <90% non-condensing in sealed bag