MT7628A with WM8523 HD Audio Wireless Module

OoliteV4.0 Module

Specification Version 1.0.2

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Revision	Date	Contents of Revision Change	Remark
1.0.1	2016-08-26	First release	
1.0.2	2016-08-27	Modify layout & fix MD	

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1 INTRODUCTION

The Oolite V4.0 module is mainly used for HD audio speaker and it is based on openwrt source code. (http://www.openwrt.org) , module main chip can be optional mt7628 or mt7688, and audio sample rate can be optional too.

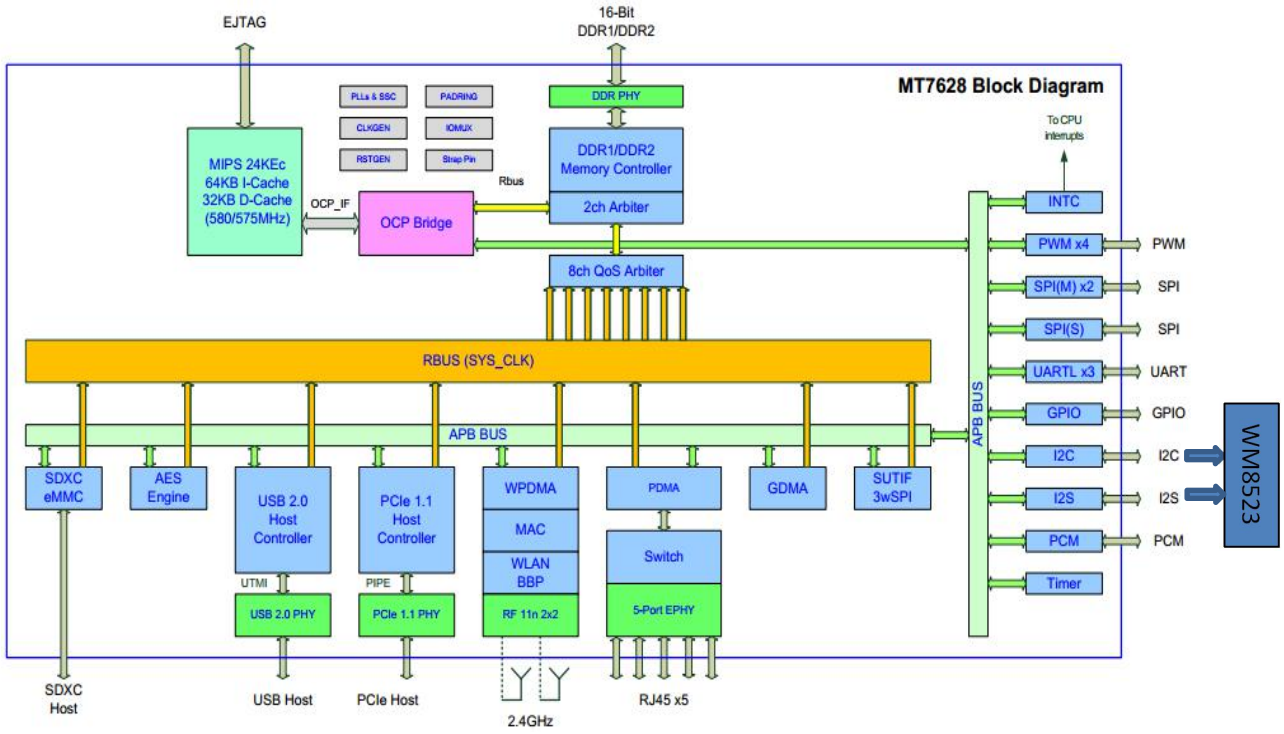
The MT7628AN includes a high performance 580/575 MHz MIPS 24KEc CPU core and high speed USB2.0/PCIe interfaces, which is designed to enable a multitude of high performance, cost-effective IEEE 802.11n applications with a MediaTek WiFi client card.There are several masters (MIPS 24KEc, USB, PCI Express, SDXC, FE) in the MT7628 SoC on a high performance,low latency Rbus. In addition, the MT7628 SoC supports lower speed peripherals such as UART Lite, GPIO, I2C and SPI via a low speed peripheral bus (Pbus). The DDR/DDR2 controller is the only bus slave on the Rbus. It includes an Advanced Memory Scheduler to arbitrate the requests from bus masters, enhancing the performance of memory access intensive tasks.

The WM8523 is a stereo DAC with integral charge pump and software control interface. This provides 2Vrms line driver outputs using a single 3.3V power supply rail.The device features ground-referenced outputs and the use of a DC servo to eliminate the need for line driving coupling capacitors and effectively eliminate power on pops and clicks.The device is controlled and configured either via the I2C/SPI compliant serial control interface or a hardware control interface.The device supports all common audio sampling rates between 8kHz and 192kHz using all common MCLK fs rates. Master and Slave modes are available and deemphasis is also supported.The WM8523 has a 3.3V tolerant digital interface, allowing logic up to 3.3V to be connected.The device is available in a 20-lead TSSOP or 24-lead QFN.

Features:

- CPU: MT7628AN with 580/575 MHz MIPS 24KEc (MT7688AN optional)
- RAM: 128MB DDR2 RAM (64MB optional)
- Flash: 16MB SPI NOR Flash ROM(8/16/32/64M option)
- Wireless speed: 300Mbps (MT7688AN Wireless speed: 150Mbps)
- GPIO:37(total), High-speed UART for console support
- USB: Usb 2.0 master interface, support USB hub extension
- Power supply voltage: 3.3V.
- Port: 1WAN+ 1PCIE interface
- Antenna:2× IPeX external antenna.
- Debug: serial debugging interface has lead out.
- With audio module (sampling rate of 32KHz,44.1KHz,48KHz,88.2KHz,96KHz and 192 KHz).
- double crystal oscillator for hifi audio output.

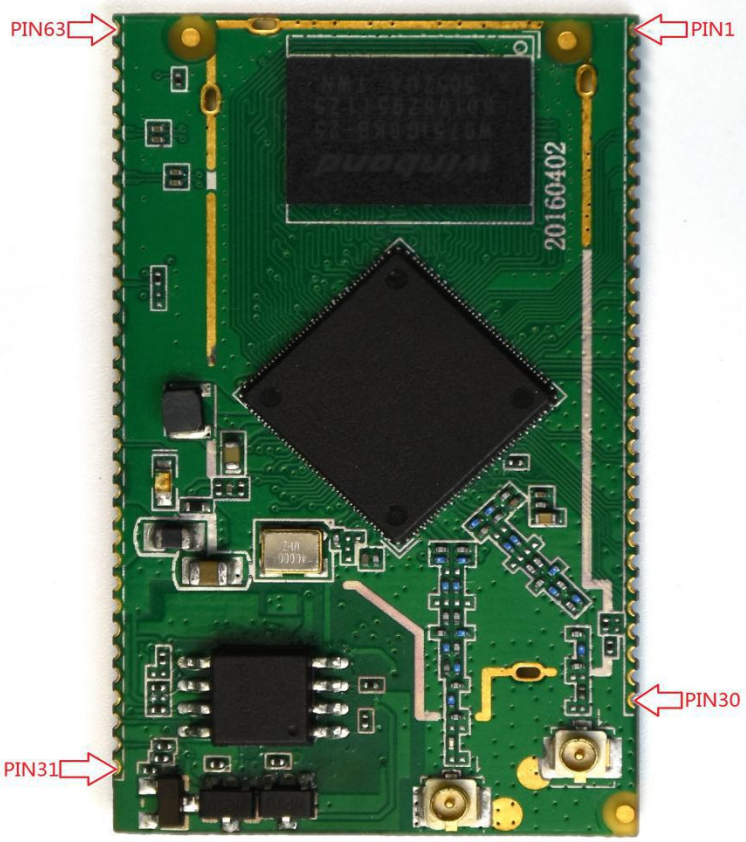
2 FUNCTIONAL BLOCK DIAGRAM



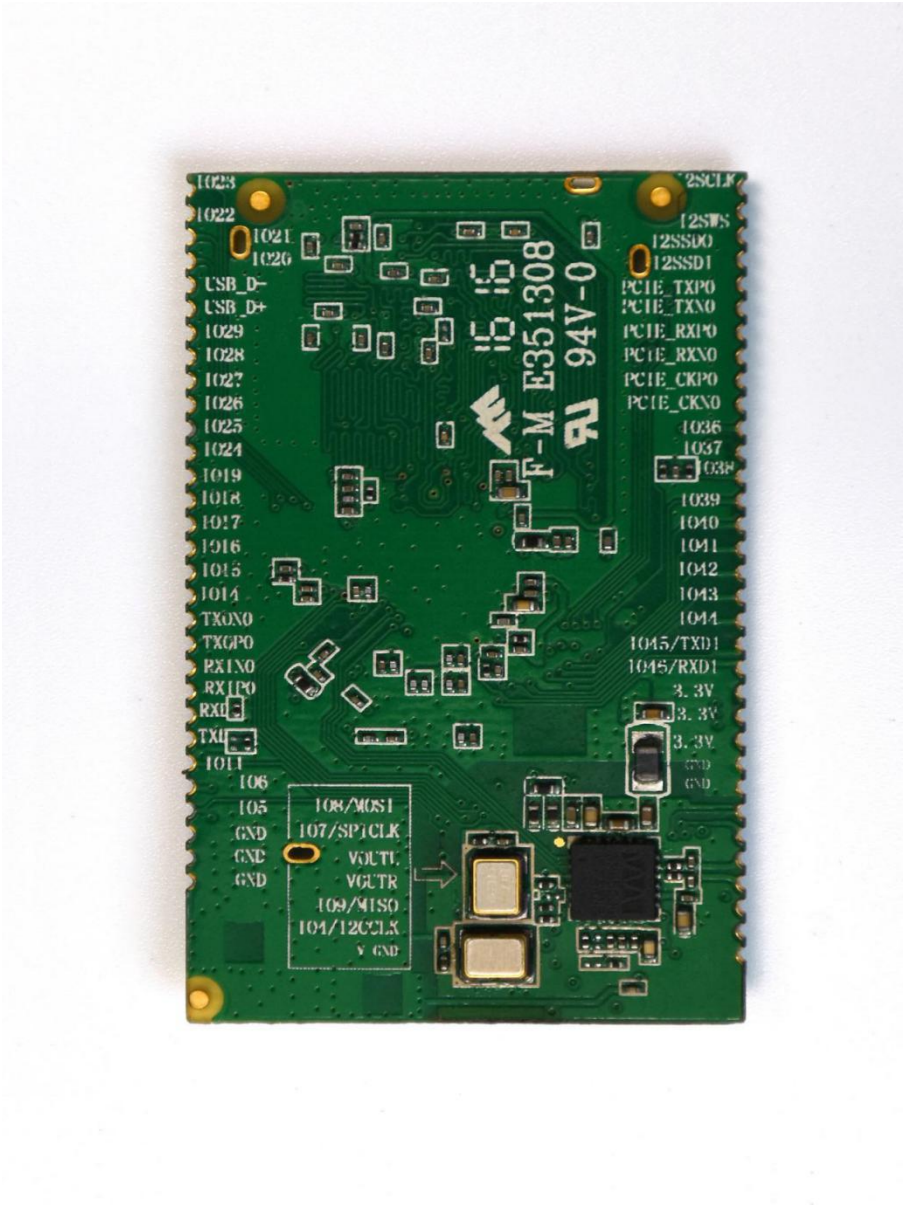
TBD

3 PICTURES

Top

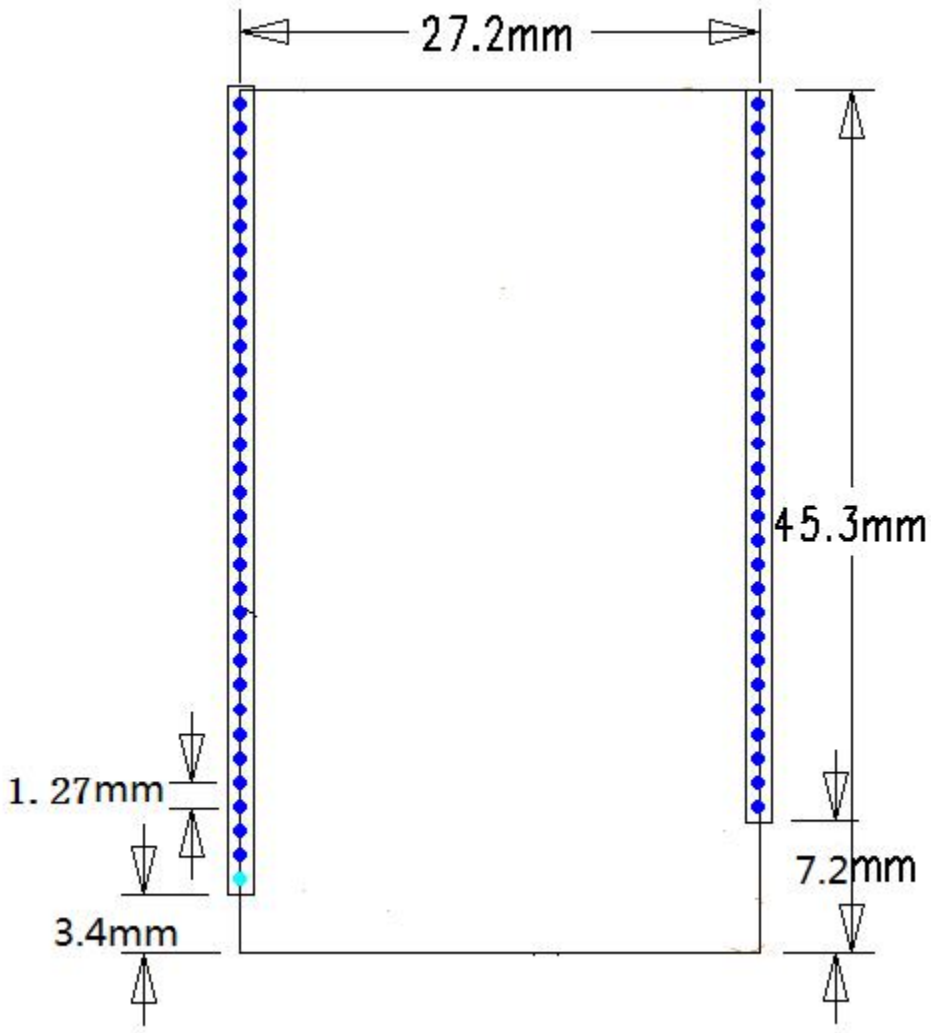


Bottom

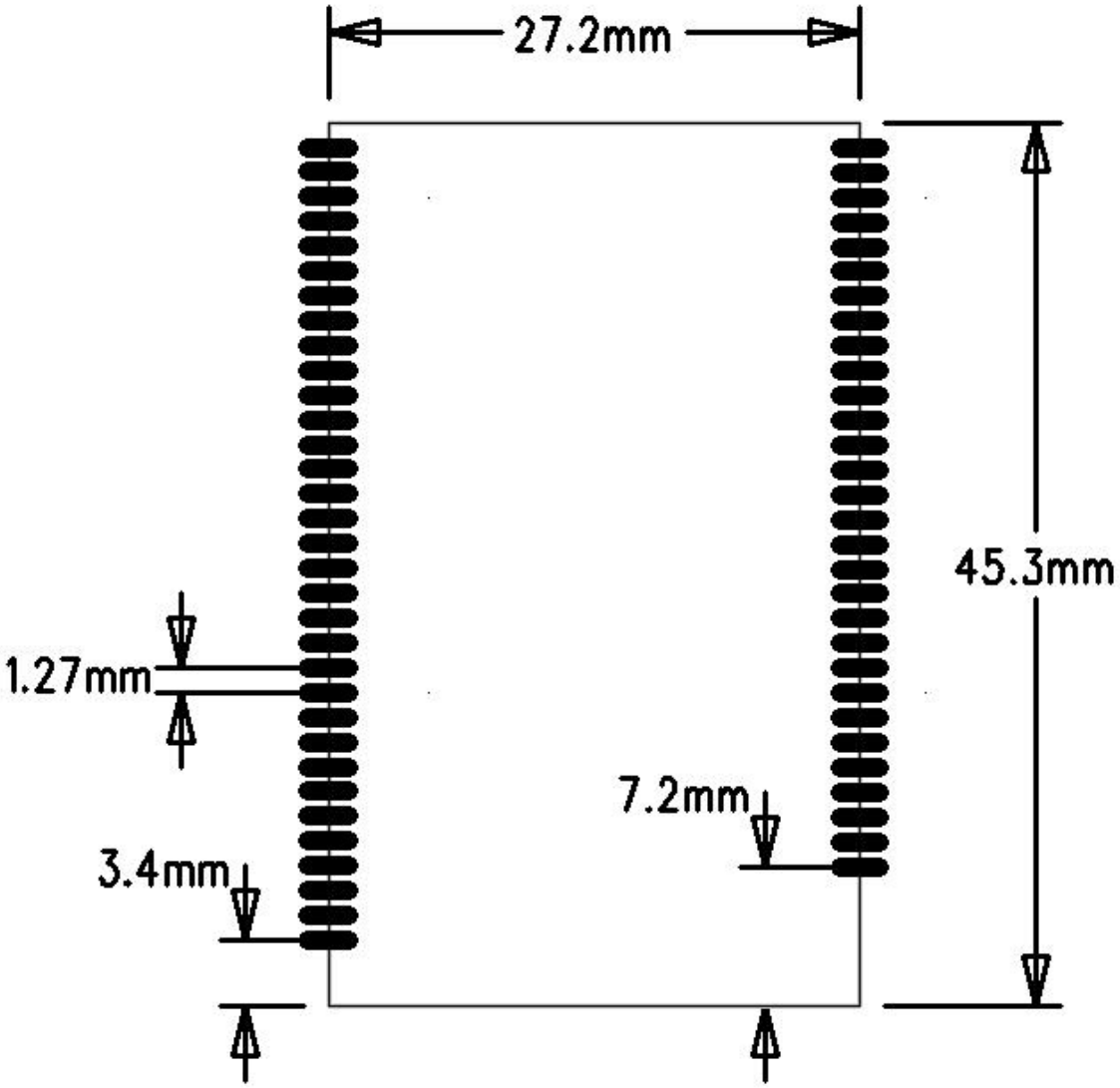

I023
I022
I021
I020
USB_D-
USB_D+
I029
I028
I027
I026
I025
I024
I019
I018
I017
I016
I015
I014
TXON0
TXGP0
RXIN0
RXIP0
RXD
TXD
I011
I06
I05
GND
GND
GND
I08/MOSI
I07/SPICLK
VOUTL
VOUTR
I09/MISO
I04/I2CCLK
GND
I2SCLK
I2SWS
I2SSDO
I2SSDI
PCIE_TXP0
PCIE_TXN0
PCIE_RXP0
PCIE_RXN0
PCIE_CKP0
PCIE_CKN0
I036
I037
I038
I039
I040
I041
I042
I043
I044
I045/TXD1
I045/RXD1
3.3V
3.3V
3.3V
GND
GND
E351308
94V-0

4 MECHANICAL

Dimensions (mm)	Length	Width	Height (without shield)
	45.3 (Tolerance:±0.2mm)	27.2 (Tolerance:±0.2mm)	1.0 (Tolerance:±0.2mm)



5 PACKAGE STRUCTURE FOR CONNECTING MODULE ON FLOOR PLATE



6 PINS DESCRIPTION

Pin No.	Name	GPIO state(default)	Reuse(default)
1	GPIO23	A, pull low to GND	EMMC_CD
2	GPIO22	A, pull high to3.3V	EMMC_WP
3	GPIO21	A, pull high to3.3V	EMMC_D4
4	GPIO20	A, pull high to3.3V	EMMC_D5
5	USB_D-	I/O	USB_D-
6	USB_D+	I/O	USB_D+
7	GPIO29	A, pull high to3.3V	EMMC_D2
8	GPIO28	A, pull high to3.3V	EMMC_D3
9	GPIO27	A	EMMC_CMD
10	GPIO26	A	EMMC_CLK
11	GPIO25	A, pull high to3.3V	EMMC_D0
12	GPIO24	A, pull low to GND	EMMC_D1
13	GPIO19	A, pull high to 3.3V	EMMC_D6
14	GPIO18	A, pull high to 3.3V	EMMC_D7
15	GPIO17	A	I/O
16	GPIO16	A	I/O
17	GPIO15	A	I/O
18	GPIO14	A	I/O
19	TXON0	A	TXON0(WAN)
20	TXOP0	A	TXOP0(WAN)
21	RXIN0	A	RXIN0(WAN)
22	RXIP0	A	RXIP0(WAN)
23	RXD	I, pull low to GND	UART_RXD0
24	TXD	O, pull low to GND	UART_TXD0

25	GPIO11	I/O,IPL	I/O
26	GPIO6	O, pull low to GND	I/O
27	GPIO5	I/O,pull high to3.3V	I2C_SDA
28	GND	Ground	
29	GND	Ground	
30	GND	Ground	
31	GND	Ground	
32	GPIO4/I2CCLK	I/O,pull high to3.3V	I2C_SCL
33	GPIO9/MISO	I/O	SPI_MISO
34	VOUTR	AUDIO	Reserved
35	VOUTL	AUDIO	Reserved
36	GPIO7/SPICLK	O,IPU	SPI_CLK
37	GPIO8/MOSI	I/O,IPD	SPI_MOSI
38	GND	Ground	
39	GND	Ground	
40	3.3V	POWER	
41	3.3V	POWER	
42	3.3V	POWER	
43	GPIO46/RXD1	I	UART_RXD1
44	GPIO45/TXD1	O, pull high to3.3V	UART_TXD1
45	GPIO44	O	WLAN_LED
46	GPIO43	I/O	P0_LED_AN/LINK 0
47	GPIO42	I/O	P1_LED_AN/LINK 1
48	GPIO41	I/O	P2_LED_AN/LINK 2

49	GPIO40	I/O	P3_LED_AN/LINK 3
50	GPIO39	I/O	P4_LED_AN/LINK 4
51	GPIO38	O, pull high to3.3V	WDT_RST_N
52	GPIO37	O,IPL	REFCLKO
53	GPIO36	O, pull high to3.3V	PERST_N
54	PCIE_CKN0	I/O	CKN0
55	PCIE_CKP0	I/O	CKP0
56	PCIE_RXN0	I/O	RXN0
57	PCIE_RXP0	I/O	RXP0
58	PCIE_TXN0	I/O	TXN0
59	PCIE_TXP0	I/O	TXP0
60	I2SSDI	O	GPIO0/D1
61	I2SSD0	I/O, pull low to GND	GPIO1/D0
62	I2SWS	O	GPIO2/WS
63	I2SCLK	I/O	GPIO3/CLK

NOTE：

I:Input

O:Ouput

I/O:Bi-directional

IPL:Internal pull low

A:Analog

Absolute Maximum Ratings

I/O supply voltage	3.3V
Input,Output,or I/O Voltage	GND-0.3 V to Vcc +0.3V

7 PIN SHARE SCHEME(GPIO REUSE)

UART1 Pin Share Scheme

Controlled by the UART1_MODE register.

Pin Name	2'b00 UART-Lite #1	2'b01 GPIO	2'b10 PWM	2'b11 TRX_SW
UART1_RXD	UART1_RXD	GPIO#46	PWM_CH1	
UART1_TXD	UART1_TXD	GPIO#45	PWM_CH0	

EPHY LED pin share scheme

Controlled by the P#_LED_AN_MODE registers

Pin Name	Bootstrapping (DBG_JTAG_MODE=1)	Bootstrapping (DBG_JTAG_MODE=0)	
		P4_LED_AN_MODE =2'b00	P4_LED_AN_MODE =2'b01
EPHY_LED4_N_JTRST_N	JTAG_RST_N	EPHY_LED4_N	GPIO#39
		P3_LED_AN_MODE =2'b00	P3_LED_AN_MODE =2'b01
EPHY_LED3_N_JTCLK	JTAG_CLK	EPHY_LED3_N	GPIO#40
		P2_LED_AN_MODE =2'b00	P2_LED_AN_MODE =2'b01
EPHY_LED2_N_JTMS	JTAG_TMS	EPHY_LED2_N	GPIO#41
		P1_LED_AN_MODE =2'b00	P1_LED_AN_MODE =2'b01
EPHY_LED1_N_JTDI	JTAG_TDI	EPHY_LED1_N	GPIO#42
		P0_LED_AN_MODE =2'b00	P0_LED_AN_MODE =2'b01
EPHY_LED0_N_JTDO	JTAG_TDO	EPHY_LED0_N	GPIO#43

WLAN LED pin share scheme

Controlled by the WLED_AN_MODE registers

Pin Name	2'b00	2'b01
WLED_N	WLED_N	GPIO#44

WLAN LED pin share scheme

Controlled by the WLED_KN_MODE registers

Pin Name	2'b00	2'b01
WLED_N	WLED_N	GPIO#35

PERST_N pin share scheme

Controlled by the PERST_ MODE register.

Pin Name	1'b0	1'b1
PERST_N	PERST_N	GPIO#36

WDT_RST_N pin share scheme

Controlled by the WDT _MODE register.

Pin Name	1'b0	1'b1
WDT_RST_N	WDT_RST_N	GPIO#38

REF_CLKO pin share scheme

Controlled by the REFCLK _MODE register.

Pin Name	1'b0	1'b1
REF_CLKO	REF_CLKO	GPIO#37

UART0 pin share scheme

Controlled by the UART0 _MODE register.

Pin Name	1'b0	1'b1
UART_TXD0	UART_TXD0	GPIO#12
UART_TXD0	UART_RXD0	GPIO#13

GPIO0 pin share scheme

Controlled by GPIO_MODE register.

Pin Name	2'b00	2'b01	2'b10	2'b11
GPIO0	GPIO#11	GPIO#11	REF_CLKO	PERST_N

SPI pin share scheme

Controlled by SPI_ MODE register.

Pin Name	1'b0	1'b1
SPI_CLK	SPI_CLK	GPO#7
SPI_MOSI	SPI_MOSI	GPO#8
SPI_MISO	SPI_MISO	GPIO#9
SPI_CS0	SPI_CS0	GPIO#10

SPI_CS1 pin share scheme

Controlled by SPI_CS1_MODE register.

Pin Name	2'b00	2'b01	2'b10
SPI_CS1	SPI_CS1	GPIO#6	REF_CLKO

I2C pin share scheme

Controlled by I2C_MODE register.

Pin Name	2'b00	2'b01
I2C_SCLK	I2C_SCLK	GPIO#4
I2C_SD	I2C_SD	GPIO#5

I2S pin share scheme

Controlled by I2S_MODE register.

Pin Name	2'b00	2'b01	2'b10
I2S_SDI	I2C_SCLK	GPIO#0	PCMDRX
I2S_SDO	I2C_SD	GPIO#1	PCMDTX
I2S_WS	I2C_SCLK	GPIO#2	PCMCLK
I2S_CLK	I2C_SD	GPIO#3	PCMFS

SD pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
Pin Name		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	SD_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	SD_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	SD_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	SD_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	SD_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	SD_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	SD_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	SD_D3	GPIO#29

eMMC pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
Pin Name		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	eMMC_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	eMMC_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	eMMC_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	eMMC_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	eMMC_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	eMMC_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	eMMC_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	eMMC_D3	GPIO#29

UART2 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and UART2_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_TP_P2	MDI_TP_P2	UART_TXD2	GPIO#20	PWM_CH2	eMMC_D5
MDI_TN_P2	MDI_TN_P2	UART_RXD2	GPIO#21	PWM_CH3	eMMC_D4

PWM_CH1 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM1_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_RN_P2	MDI_RN_P2	PWM_CH1	GPIO#19		eMMC_D6

PWM_CH0 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM0_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_RP_P2	MDI_RP_P2	PWM_CH0	GPIO#18		eMMC_D7

SPIS pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SPIS_MODE registers

	4'b0000	4'b1111			
Pin Name		2'b00	2'b01	2'b10	2'b11
MDI_TP_P1	MDI_TP_P1	SPIS_CS	GPIO#14		PWM_CH0
MDI_TN_P1	MDI_TN_P1	SPIS_CLK	GPIO#15		PWM_CH1
MDI_RP_P1	MDI_RP_P1	SPIS_MISO	GPIO#16		UART_TXD2
MDI_RN_P1	MDI_RN_P1	SPIS_MOSI	GPIO#17		UART_RXD2

Pin share function description

Pin Share Name	I/O	Pin Share Function description
PCMDTX	O	PCM Data Transmit DATA signal sent from the PCM host to the external codec.
PCMDRX	I	PCM Data Receive DATA signal sent from the external codec to the PCM host.
PCMCLK	I/O	PCM Clock The clock signal can be generated by the PCM host (Output direction), or provided by an external clock (input direction). The clock frequency should match the slot configuration of the PCM host. e.g. 4 slots, PCM clock out/in should be 256 kHz. 8 slots, PCM clock out/in should be 512 kHz. 16 slots, PCM clock out/in should be 1.024 MHz. 32 slots, PCM clock out/in should be 2.048 MHz. 64 slots, PCM clock out/in should be 4.096 MHz. 128 slots, PCM clock out/in should be 8.192 MHz.
PCMFS	I/O	PCM SYNC signal. In our design, the direction of this signal is independent of the direction of PCMCLK. Its direction and mode is configurable.

Pin Share Name	I/O	Pin Share Function description
PWM_CH0	O	Pulse Width Modulation Channle 0
PWM_CH1	O	Pulse Width Modulation Channle 1
PWM_CH2	O	Pulse Width Modulation Channle 2
PWM_CH3	O	Pulse Width Modulation Channle 3

Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7688AN only. It needs to be pull-low for 7688KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

8 MODULE OTHER CONTENT

RF HARDWARE PERFORMANCE

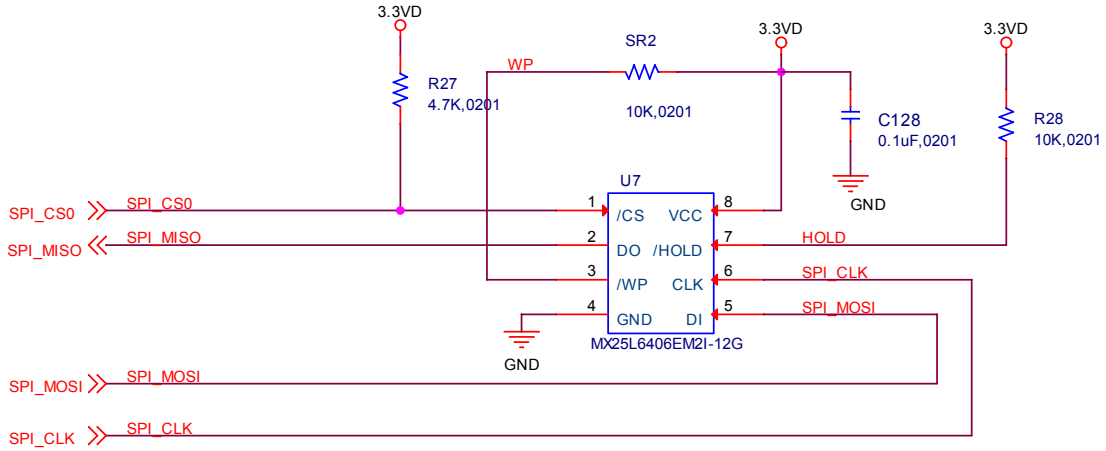
Item	type	real target
Antenna 0	Frequency error	-5.0ppm
	power	CCK 11M 18.0dbm OFDM 54M 16.0dbm MCS7(HT20) 16.0dbm MCS7(HT40) 15.0dbm
	EVM	CCK 11M -18.0db OFDM 54M -25.0db MCS7(HT20) -27.0db MCS7(HT40) -28db
	Reception Sensitivity	CCK 11M -85dbm OFDM 54M -63dbm MCS7(HT20) -61dbm MCS7(HT40) -59dbm

Item	type	real target
	Frequency error	-5.0ppm
	power	CCK 11M 18.0dbm OFDM 54M 16.0dbm MCS7(HT20) 16.0dbm MCS7(HT40) 15.0dbm
	EVM	CCK 11M 26.0db OFDM 54M -25.0db

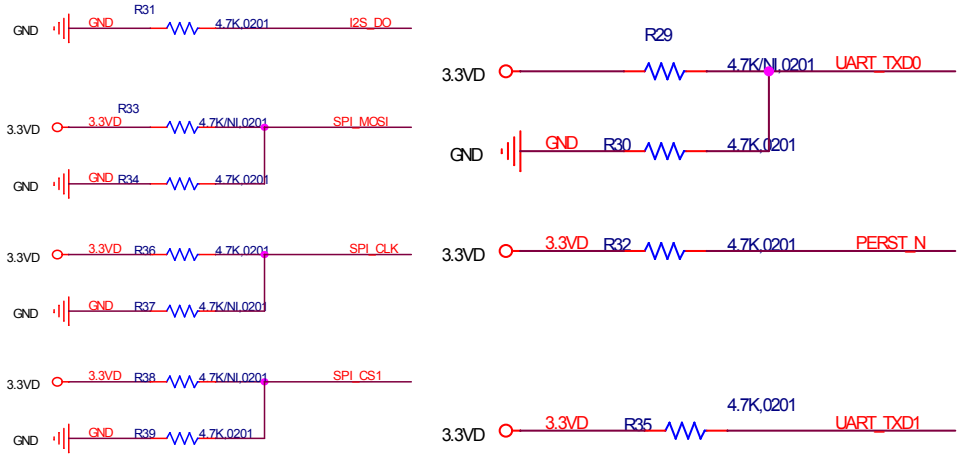
Antenna 1		MCS7(HT20) -27.0db MCS7(HT40) -28db
	Reception Sensitivity	CCK 11M -85dbm OFDM 54M -63dbm MCS7(HT20) -61dbm MCS7(HT40) -59dbm

9 ENCLOSURE

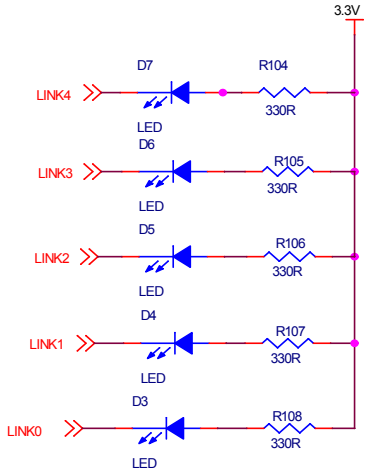
(1) SPI Flash Schematic



(2) Bootstrap CONFIG Schematic



(3) External mode of module



(4) Net port connection