MT7621A core module

OoliteV8.0_SPEC_EN

Version 0.1.9

Author: TRIGG

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GainStrong Industry Co.,Ltd. http://www.gainstrong.cn
Tell:+86-755-81720165 support@gainstrong.cn

Revision	Date	Contents of Revision Change	Remark
0.1.2	2016-07-05	First release	
0.1.3	2016-10-12	Update	
0.1.4	2017-01-06	Update	
0.1.5	2017-04-14	Add Pin Sketch Map	JamesBond
0.1.6	2017-06-23	Modify mechanical pictures	River
0.1.7	2017-06-27	Change picture	River
0.1.9	2018-11-16	Update Pins Map	JamesBond

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1 INTRODUTION

The OoliteV8.0 module use the MT7621A chipset. The MT7621A integrates a dual-core MIPS- 1004Kc (880MHz),HNAT/HQoS/ Samba/VPN accelerators,5-port GbE switch, RGMII, USB3.0, USB2.0, 3xPCIe, SD-XC. The powerful CPU with rich portfolio is suitable for 802.11ac, LTE cat4/5, edge, hotspot, VPN,AC (Access Control). It can also connect to touch-panel, ZigBee/Z-Wave for Internet Service Router and Home Security Gateway.

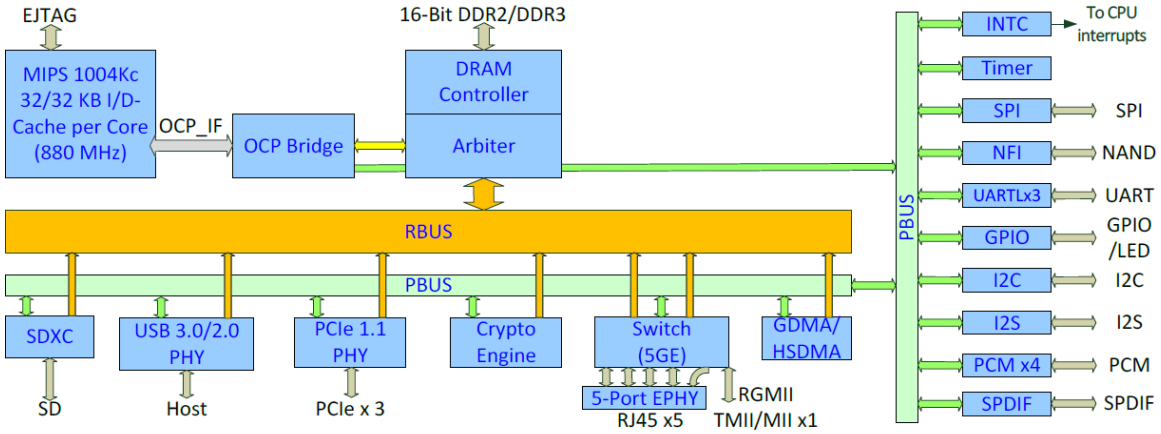
For the next generation router, MT7621A provides several dedicated hardware engines to accelerate the NAT, QoS, Samba and VPN traffic.These accelerators relief the CPU for other upper layer applications.

Features

- MT7621A Embedded MIPS1004Kc (880 MHz)
- RAM: 16-bit DDR 512Mbyte(64/128/256Mbyte optional)
- Flash: SPI Nor 32Mbyte Flash(8/16/64Mbyte optional)
- 5-port 10/100/1000Mbps SW/PHY
- 1x RGMII/MII interface
- SPI, NAND Flash, SDXC, eMMC(4 bits)
- 1x USB 3.0, 1x USB 2.0, 3x Mini-PCIe host
- I2C, SPI*2, UART lite*3, JTAG, MDC, MDIO, GPIO
- HW storage accelerator
- OPENWRT / LEDE / Linux 2.6 SDK
- VoIP support (I2S, PCM) , Audio interface (SPDIF-Tx, I2S, PCM)
- Size: 50.0mm x 50.0mm x 4.0mm
- Packaging: 140-Pins LCC

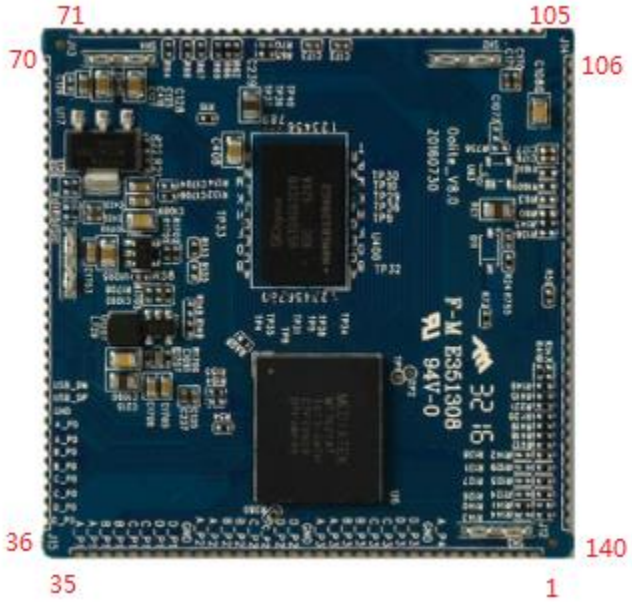
2 BLOCK DIAGRAM

Functional Block Diagram

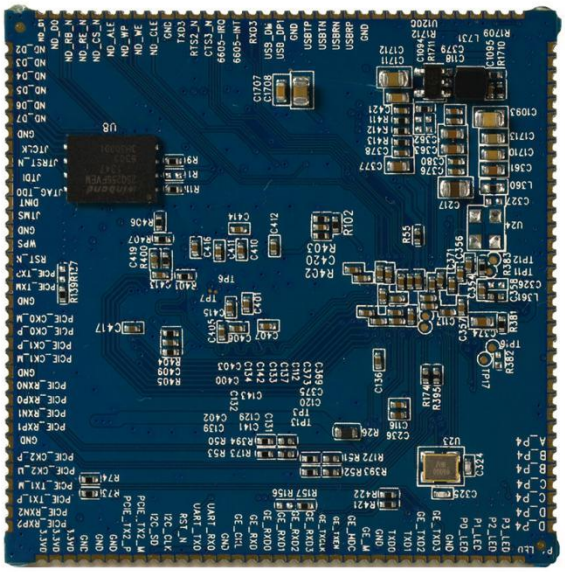


Features	MT7621A
CPU	MIPS1004Kc (880 MHz, Durl Core)
I-Cache, D-Cache	32 KB, 32 KB
L2 Cache	256KB
HNAT/HQoS	HQoS 16 queues HNAT 2 Gbps forwarding (IPv4, IPv6 routing, DS-Lite, 6RD, 6to4)
Memory	
DRAM Controller	16-bit
DDR2	800 Mbps (max 256 MByte)
DDR3	1200 Mbps (max 512 MByte)
NAND	Small page 512-Byte (max 512 Mbit) Large page 2k-Byte (max 8 Gbit)
SPI Flash	3B addr mode (max 128 Mbit) 4B addr mode (max 512 Mbit)
SD **eMMC**	SD-XC class 10 (max 128 GByte) 4-bit eMMC (max 8 GByte)
PCIe	3
USB	USB3 x 1+ USB2 x 1 or USB2 x 2
Ethernet	5-port GSW + RGMII(1)
I2S	1
PCM	1
I2C	1
SPDIF-Tx	1
UART Lite	3
JTAG	1
Package	LFBGA 11.7 mm x 13.6 mm

3 PICTURES



TOP



BOTTOM

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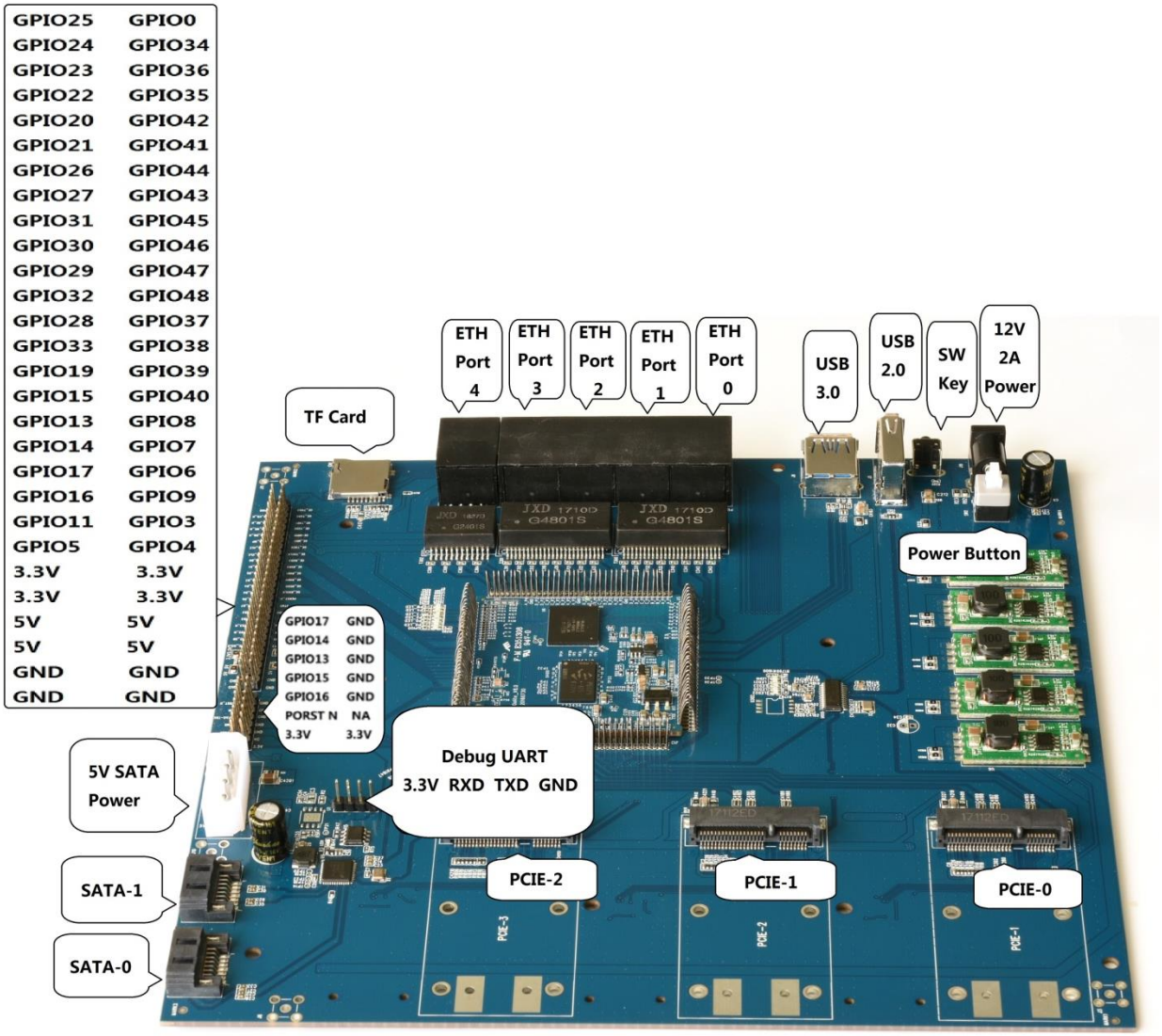

GPIO25 GPIO0
GPIO24 GPIO34
GPIO23 GPIO36
GPIO22 GPIO35
GPIO20 GPIO42
GPIO21 GPIO41
GPIO26 GPIO44
GPIO27 GPIO43
GPIO31 GPIO45
GPIO30 GPIO46
GPIO29 GPIO47
GPIO32 GPIO48
GPIO28 GPIO37
GPIO33 GPIO38
GPIO19 GPIO39
GPIO15 GPIO40
GPIO13 GPIO8
GPIO14 GPIO7
GPIO17 GPIO6
GPIO16 GPIO9
GPIO11 GPIO3
GPIO5 GPIO4
3.3V 3.3V
3.3V 3.3V
5V 5V
5V 5V
GND GND
GND GND
TF Card
ETH Port 4
ETH Port 3
ETH Port 2
ETH Port 1
ETH Port 0
USB 3.0
USB 2.0
SW Key
12V 2A Power
Power Button
GPIO17 GND
GPIO14 GND
GPIO13 GND
GPIO15 GND
GPIO16 GND
PORST N NA
3.3V 3.3V
Debug UART
3.3V RXD TXD GND
5V SATA Power
SATA-1
SATA-0
PCIE-2
PCIE-1
PCIE-0

4 PINS DESCRIPTION

Pin NO.	Function	Description
1	ESW_TXVN_D_P4	Gigabit Port4_D-
2	ESW_TXVP_D_P4	Gigabit Port4_D+
3	ESW_TXVN_C_P4	Gigabit Port4_C-
4	ESW_TXVP_C_P4	Gigabit Port4_C+
5	ESW_TXVN_B_P4	Gigabit Port4_B-
6	ESW_TXVP_B_P4	Gigabit Port4_B+
7	ESW_TXVN_A_P4	Gigabit Port4_A-
8	ESW_TXVP_A_P4	Gigabit Port4_A+
9	GND	Ground
10	ESW_TXVN_D_P3	Gigabit Port3_D-
11	ESW_TXVP_D_P3	Gigabit Port3_D+
12	ESW_TXVN_C_P3	Gigabit Port3_C-
13	ESW_TXVP_C_P3	Gigabit Port3_C+
14	ESW_TXVN_B_P3	Gigabit Port3_B-
15	ESW_TXVP_B_P3	Gigabit Port3_B+
16	ESW_TXVN_A_P3	Gigabit Port3_A-
17	ESW_TXVP_A_P3	Gigabit Port3_A+
18	GND	Ground
19	ESW_TXVN_D_P2	Gigabit Port2_D-
20	ESW_TXVP_D_P2	Gigabit Port2_D+
21	ESW_TXVN_C_P2	Gigabit Port2_C-
22	ESW_TXVP_C_P2	Gigabit Port2_C+
23	ESW_TXVN_B_P2	Gigabit Port2_B-
24	ESW_TXVP_B_P2	Gigabit Port2_B+
25	ESW_TXVN_A_P2	Gigabit Port2_A-
26	ESW_TXVP_A_P2	Gigabit Port2_A+
27	GND	Ground
28	ESW_TXVN_D_P1	Gigabit Port1_D-
29	ESW_TXVP_D_P1	Gigabit Port1_D+

30	ESW_TXVN_C_P1	Gigabit Port1_C-
31	ESW_TXVP_C_P1	Gigabit Port1_C+
32	ESW_TXVN_B_P1	Gigabit Port1_B-
33	ESW_TXVP_B_P1	Gigabit Por1_B+
34	ESW_TXVN_A_P1	Gigabit Port1_A-
35	ESW_TXVP_A_P1	Gigabit Por1_A+
36	ESW_TXVN_D_P0	Port #0 MDI Transceivers
37	ESW_TXVP_D_P0	Port #0 MDI Transceivers
38	ESW_TXVN_C_P0	Port #0 MDI Transceivers
39	ESW_TXVP_C_P0	Port #0 MDI Transceivers
40	ESW_TXVN_B_P0	Port #0 MDI Transceivers
41	ESW_TXVP_B_P0	Port #0 MDI Transceivers
42	ESW_TXVN_A_P0	Port #0 MDI Transceivers
43	ESW_TXVP_A_P0	Port #0 MDI Transceivers
44	GND	Ground
45	USB_DP	SB Port0 HS/FS/LS data pin Data+ (USB3.0)
46	USB_DM	USB Port0 HS/FS/LS data pin Data- (USB3.0)
47	GND	Ground
48	SSUSB_RXP	USB Port0 SS data pin RX+ (USB3.0)
49	SSUSB_RXN	USB Port0 SS data pin RX+-(USB3.0)
50	SSUSB_TXN	USB Port0 SS data pin TX- (USB3.0)
51	SSUSB_TXP	USB Port0 SS data pin TX+ (USB3.0)
52	GND	Ground
53	USB_DP_1P	USB Port1 data pin Data+ (USB2.0)
54	USB_DM_1P	USB Port1 data pin Data- (USB2.0)
55	RXD3	UART RX Data / GPIO#8
56	RXD2	UART RX Data / MT6605_INT / GPIO#12
57	CTS2_N	UART Clear To Send / MT6605_IRQ / GPIO#10
58	CTS3_N	UART Clear To Send / #GPIO#6
59	RTS2_N	UART Request To Send / GPIO#9
60	TXD3	UART TX Data / GPIO#7
61	GND	Ground
62	ND_CLE	NAND Flash Command Latch Enable / GPIO#43

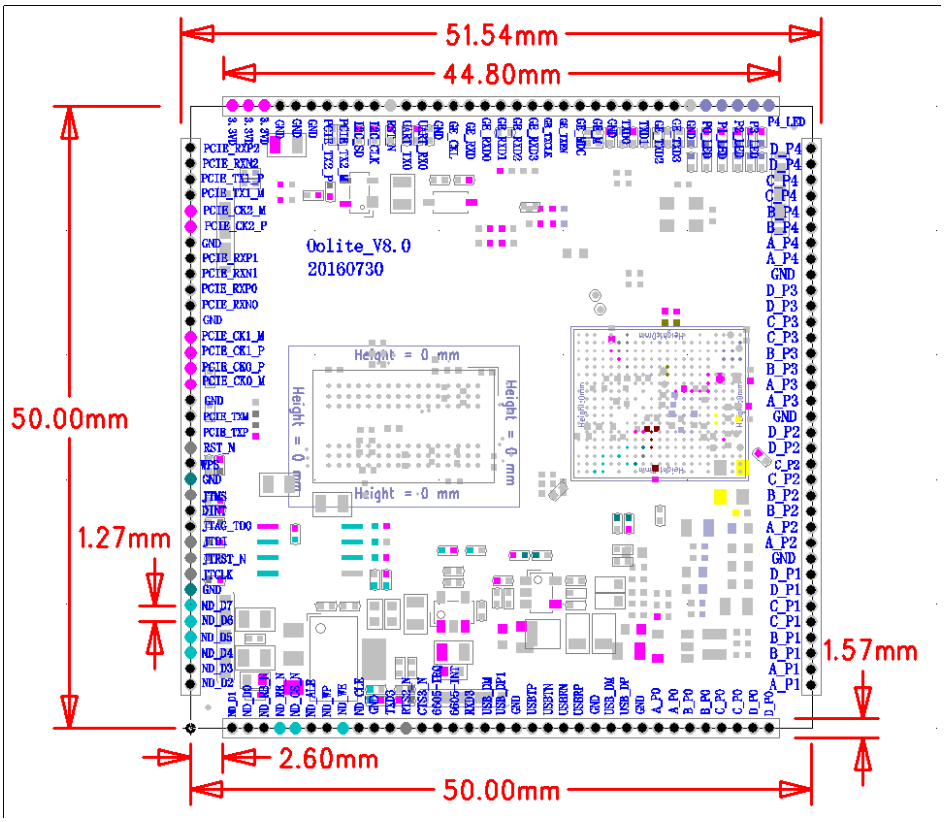
63	ND_WE_N	NAND Flash Write Enable / GPIO#35
64	ND_WP	NAND Flash Write Protect / GPIO#41
65	ND_ALE	NAND Flash ALE Latch Enable / GPIO#44
66	ND_CS_N	NAND Flash Chip Select / GPIO#34
67	ND_RE_N	NAND Flash Read Enable / GPIO#36
68	ND_RB_N	NAND Flash Ready/Busy / GPIO#42
69	ND_D0	NAND Flash Data0 / GPIO#45
70	ND_D1	NAND Flash Data1 / GPIO#46
71	ND_D2	NAND Flash Data2 / GPIO#47
72	ND_D3	NAND Flash Data3 / GPIO#48
73	ND_D4	NAND Flash Data4 / GPIO#37
74	ND_D5	NAND Flash Data5 / GPIO#38
75	ND_D6	NAND Flash Data6 / GPIO#39
76	ND_D7	NAND Flash Data7 / GPIO#40
77	TXD2	UART TX Data / GPIO11
78	JTCLK	JTAG Clock / GPIO#16
79	JTRST_N	JTAG Target Reset / GPIO#17
80	JTDI	JTAG Data Input / GPIO#14
81	JTDO	JTAG Data Output / GPIO#13
82	DINT	
83	JTMS	JTAG Mode Select / GPIO#15
84	RTS3_N	UART Request To Send / GPIO#5
85	WDT_RST_N	SW Reset / WDT_RST_N / WPS / GPIO#18
86	PERST_N	PCIE / GPIO#19
87	PCIE_TX0_P	PCIE0_TX+
88	PCIE_TX0_M	PCIE0_TX-
89	GND	Ground
90	PCIE_CK0_M	PCIE0_CLK-
91	PCIE_CK0_P	PCIE0_CLK+
92	PCIE_CK1_P	PCIE1_CLK+
93	PCIE_CK1_M	PCIE1_CLK-
94	GND	Ground
95	PCIE_RXN0	PCIE0_RX-

96	PCIE_RXP0	PCIE0_RX+
97	PCIE_RXN1	PCIE1_RX-
98	PCIE_RXP1	PCIE1_RX+
99	GND	Ground
100	PCIE_CK2_P	PCIE2_CLK+
101	PCIE_CK2_M	PCIE2_CLK-
102	PCIE_TX1_M	PCIE1_TX+
103	PCIE_TX1_P	PCIE1_TX-
104	PCIE_RXN2	PCIE2_RX-
105	PCIE_RXP2	PCIE2_RX+
106	3.3VD	POWER
107	3.3VD	POWER
108	3.3VD	POWER
109	GND	Ground
110	GND	Ground
111	GND	Ground
112	PCIE_TX2_P	PCIE2_TX+
113	PCIE_TX2_M	PCIE2_TX-
114	I2C_SD	I2C Data / GPIO#3
115	I2C_SCLK	I2C Clock / GPIO#4
116	D2DB_PORST_N	Power on reset
117	TXD1	UART TX Data / GPIO#2
118	RXD1	UART RX Data / GPIO#1
119	GND	Ground
120	GE_RXCLK	RGMII2 Rx Clock GPIO#33
121	GE_RXDV	RGMII2 Rx Data Valid / GPIO#32
122	GE_RXD0	RGMII2 Rx Data bit #0 / GPIO#28
123	GE_RXD1	RGMII2 Rx Data bit #1 / GPIO#29
124	GE_RXD2	RGMII2 Rx Data bit #2 / GPIO#30
125	GE_RXD3	RGMII2 Rx Data bit #3 / GPIO#31
126	GE_TXCLK	RGMII2 Tx Clock / GPIO#27
127	GE_TXEN	RGMII2 Tx Data Valid / GPIO#26
128	GE_MDC	PHY Management Clock. Note: While RGMII/MII connects to external PHY, this pin is MDC. Else, it should be NC.

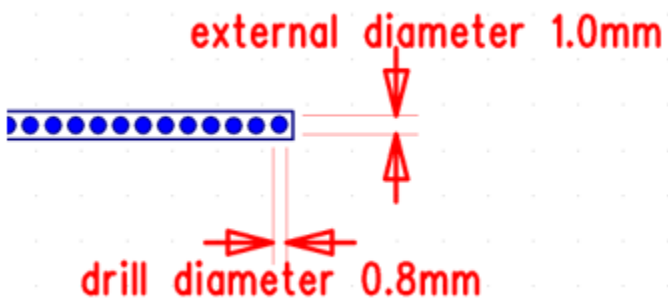
129	GE_MDIO	PHY Management Data. Note: While RGMII/MII connects to external PHY, this pin is MDIO. Else, it should be NC.
130	GND	Ground
131	GE_TXD0	RGMII2 Tx Data bit #0 / GPIO#22
132	GE_TXD1	RGMII2 Tx Data bit #1 / GPIO#23
133	GE_TXD2	RGMII2 Tx Data bit #2 / GPIO#24
134	GE_TXD3	RGMII2 Tx Data bit #0 / GPIO#25
135	GPIO0	GPIO#0
136	ESW_P0_LED_0	Port #0 PHY LED indicators
137	ESW_P1_LED_0	Port #1PHY LED indicators
138	ESW_P2_LED_0	Port #2 PHY LED indicators
139	ESW_P3_LED_0	Port #3 PHY LED indicators
140	ESW_P4_LED_0	Port #4 PHY LED indicators

5 MECHANICAL

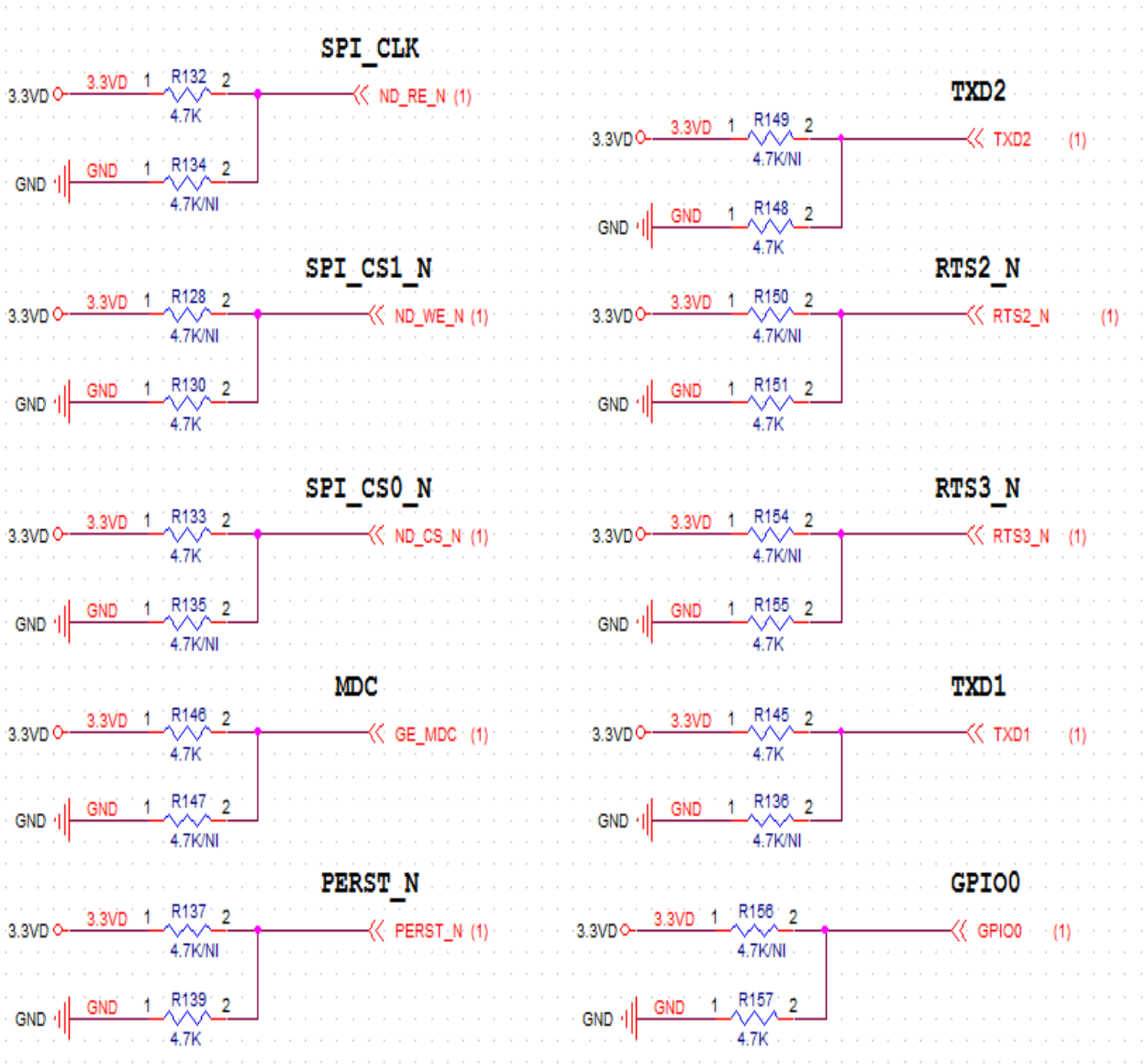
Dimensions (mm)	Length	Width	Height
	50.0 (Tolerance:±0.2mm)	50.0 (Tolerance:±0.2mm)	4.0 (Tolerance:±0.2mm)



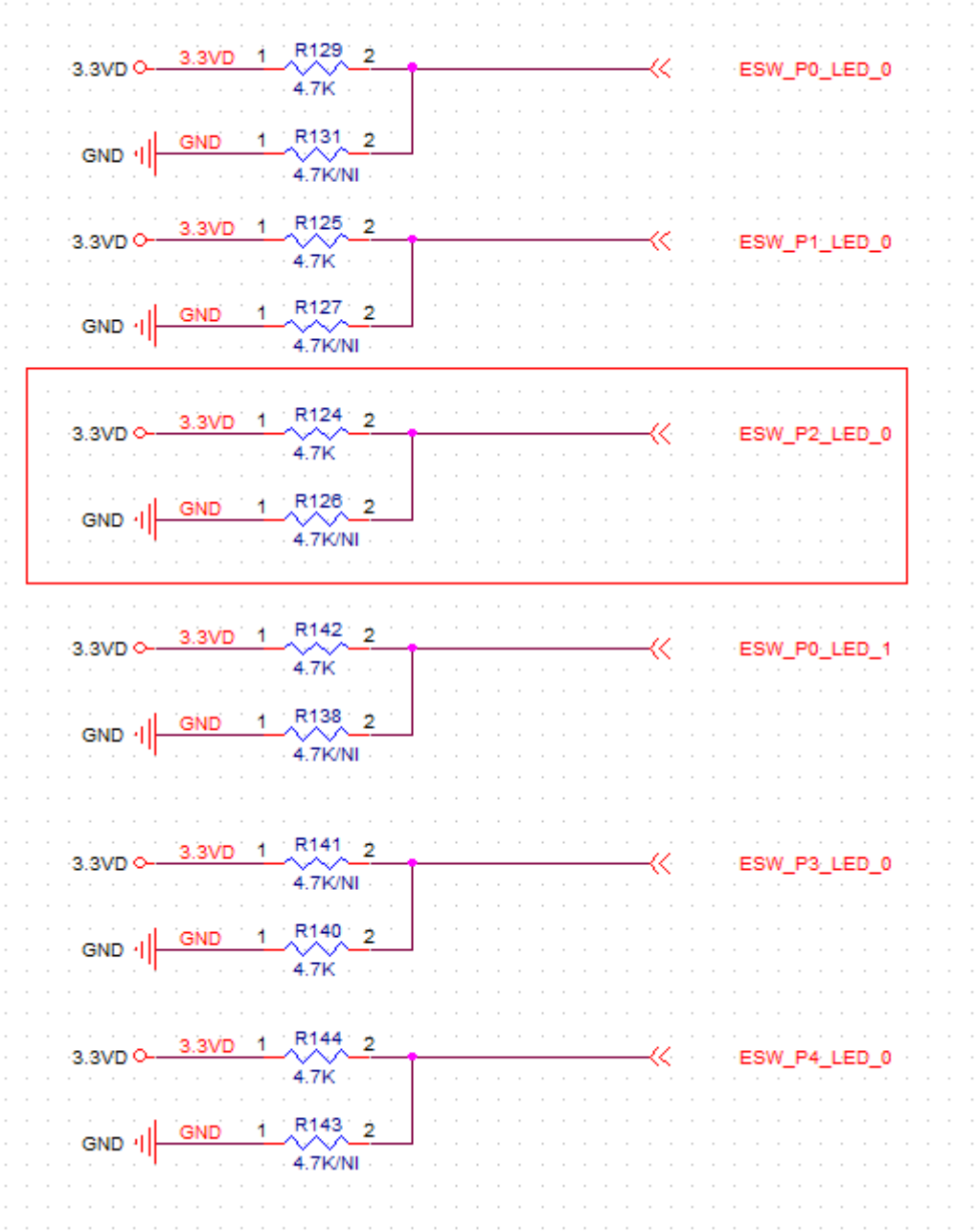
Pin describe:



6 BOOTSTRAP SETTING



LED:


3.3VD
3.3VD
1
R129
2
4.7K
ESW_P0_LED_0
GND
GND
1
R131
2
4.7K/NI
3.3VD
3.3VD
1
R125
2
4.7K
ESW_P1_LED_0
GND
GND
1
R127
2
4.7K/NI
3.3VD
3.3VD
1
R124
2
4.7K
ESW_P2_LED_0
GND
GND
1
R126
2
4.7K/NI
3.3VD
3.3VD
1
R142
2
4.7K
ESW_P0_LED_1
GND
GND
1
R138
2
4.7K/NI
3.3VD
3.3VD
1
R141
2
4.7K/NI
ESW_P3_LED_0
GND
GND
1
R140
2
4.7K
3.3VD
3.3VD
1
R144
2
4.7K
ESW_P4_LED_0
GND
GND
1
R143
2
4.7K/NI

7 REFLOW SOLDERING TEMPERATURE CURVE

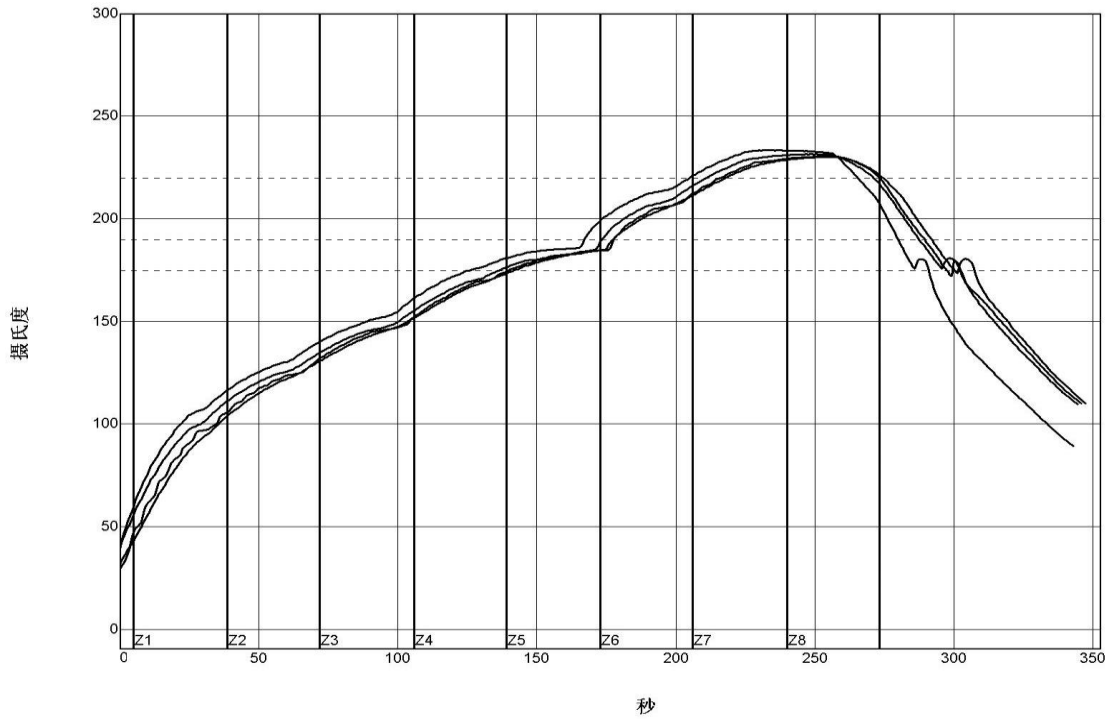
My First Product 周一 **2014年04月07日, 15:27:55**

炉子名称：**JTR-800** 制程界限名称：**System Default for Reflow**

温度设置 (摄氏度)

温区	1	2	3	4	5	6	7	8
上温区	125	135	155	185	195	225	240	230
下温区	125	135	155	185	195	225	240	230

传送带速度 (公分/分): 70.0



PWI= 94%	恒温时间175至190C		回流时间 /220C		最高温度	
<TC2>	35.53	-82%	55.58	-72%	230.28	-94%
<TC3>	37.66	-74%	58.66	-57%	230.56	-89%
<TC4>	41.52	-62%	60.63	-47%	233.62	-28%
<TC5>	37.07	-76%	60.44	-48%	231.67	-67%
温差	5.99		5.05		3.34	

制程界限:

锡膏: System Default for Reflow

统计数名称	最低界限	最高界限	单位
恒温时间175-190摄氏度	30	90	秒
回流以上时间 - 220摄氏度	50	90	秒
最高温度	230	240	度 摄氏度

描述:

KIC
San Diego, CA USA

温度曲线是由 KIC 科技所得
电话: +1-858-673-6050
传真: +1-858-673-0085

www.kicthermal.com
tech@kicmail.com

8 MODULE OPERATING ENVIRONMENT

Power Supply	3.3V ±5%
Operating Temperature	-20℃ ~ 55℃
Storage Temperature	-40℃ ~ 80℃
Operating Humidity	10%~90% non-condensing
Storage Humidity	5%~90% non-condensing