Oolite V3.1 Module SPEC

Specification Version 1.0.2

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Revision	Date	Contents of Revision Change	Remark
1.0.1	2016-9-27	First release	
1.0.2	2017-02-27	Update the document	James

1 INTRODUCTION

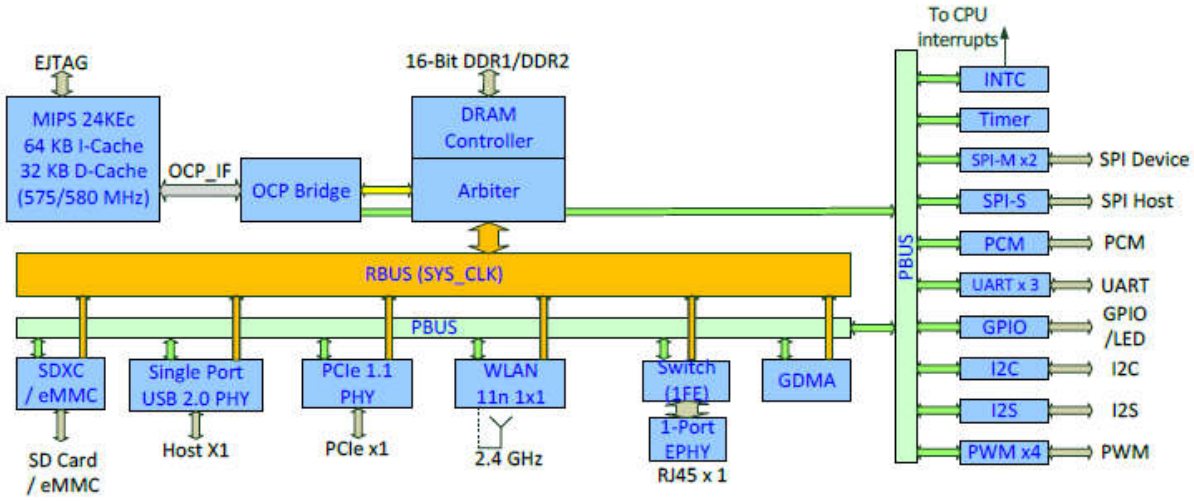
The Oolite V3.1 motherboard pick up Oolite V3.1 module .The Oolite V3.1 module use the MT7688AN chipset. The MT7688AN integrates a 1T1R 802.11n Wi-Fi radio, a 580MHz MIPS® 24KEc™ CPU, 1-port fast Ethernet PHY, USB2.0 host, PCIe, SD-XC, I2S/PCM and multiple slow IOs. The MT7688AN provides two operation modes – IoT gateway mode and IoT device mode. In IoT gateway mode, the PCI Express interface can connect to 802.11ac chipset for 11ac dual-band concurrent gateway. The high performance USB 2.0 allows the MT7688AN to add 3G/LTE modem support or add a H.264 ISP for wireless IP camera. For the IoT device mode, the MT7688AN supports eMMC, SD-XC and USB 2.0. The MT7688AN can support the WiFi high quality audio via 192Kbps/24bits I2S interface and VoIP application through PCM. In IoT device mode, it further supports PWM, SPI slave, 3rd UART and more GPIOs. For IoT gateway, it can connect to touch panel and BLE, Zigbee/Z-Wave and sub-1G RF for smart home control.

Features:

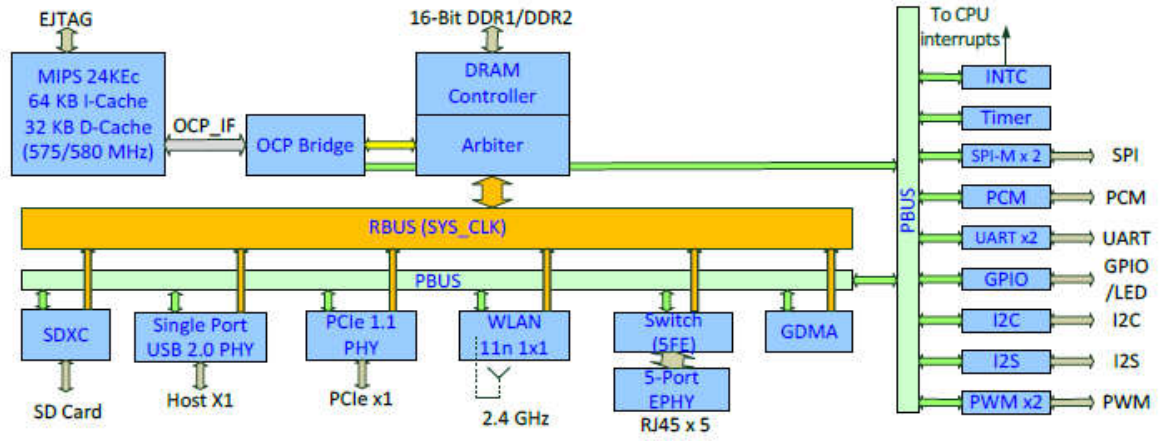
- CPU: MT7688AN with 580/575 MHz MIPS 24KEc
- RAM: 128M DDR2 RAM (256M optional)
- Flash: 3B addr mode 16M(8/16M option), 4B addr mode 64M(16/32/64M option)
- Wireless speed: 150Mbps
- GPIO: 41
- USB: 3 ×90 degrees of USB interface,1×Mini USB,
- Power supply voltage: 3.3V.
- 1×WAN+1×LAN
- 1×EMMC(optional)
- 20/40 MHz channel bandwidth
- Supports Legacy 802.11b/g ,HT 802.11n and 802.11vmodes
- Supports WEP64/128, TKIP, AES, WPA, WPA2, WAPI
- Green AP/STA
  - Intelligent Clock Scaling (exclusive)
  - DDRII: ODT off, Self-refresh mode
- iPA/iLNA and ePA/eLNA
- Embedded PMU

2 FUNCTIONAL BLOCK DIAGRAM

IoT Device Mode

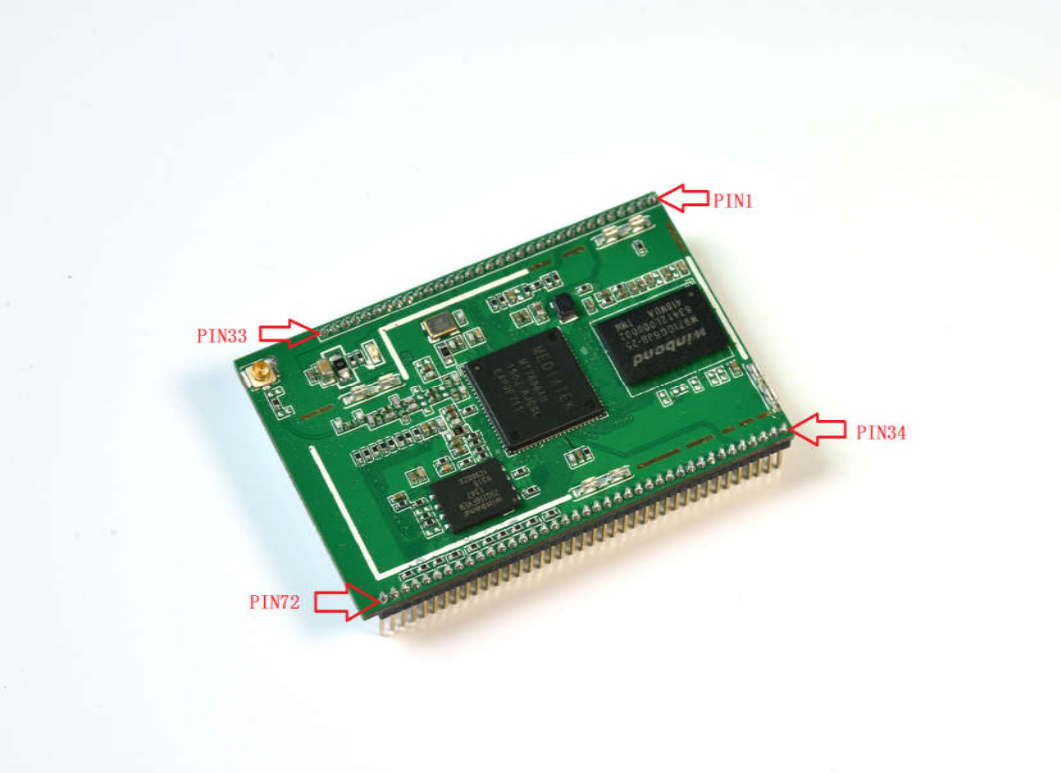


IoT Gateway Mode



3 PICTURES

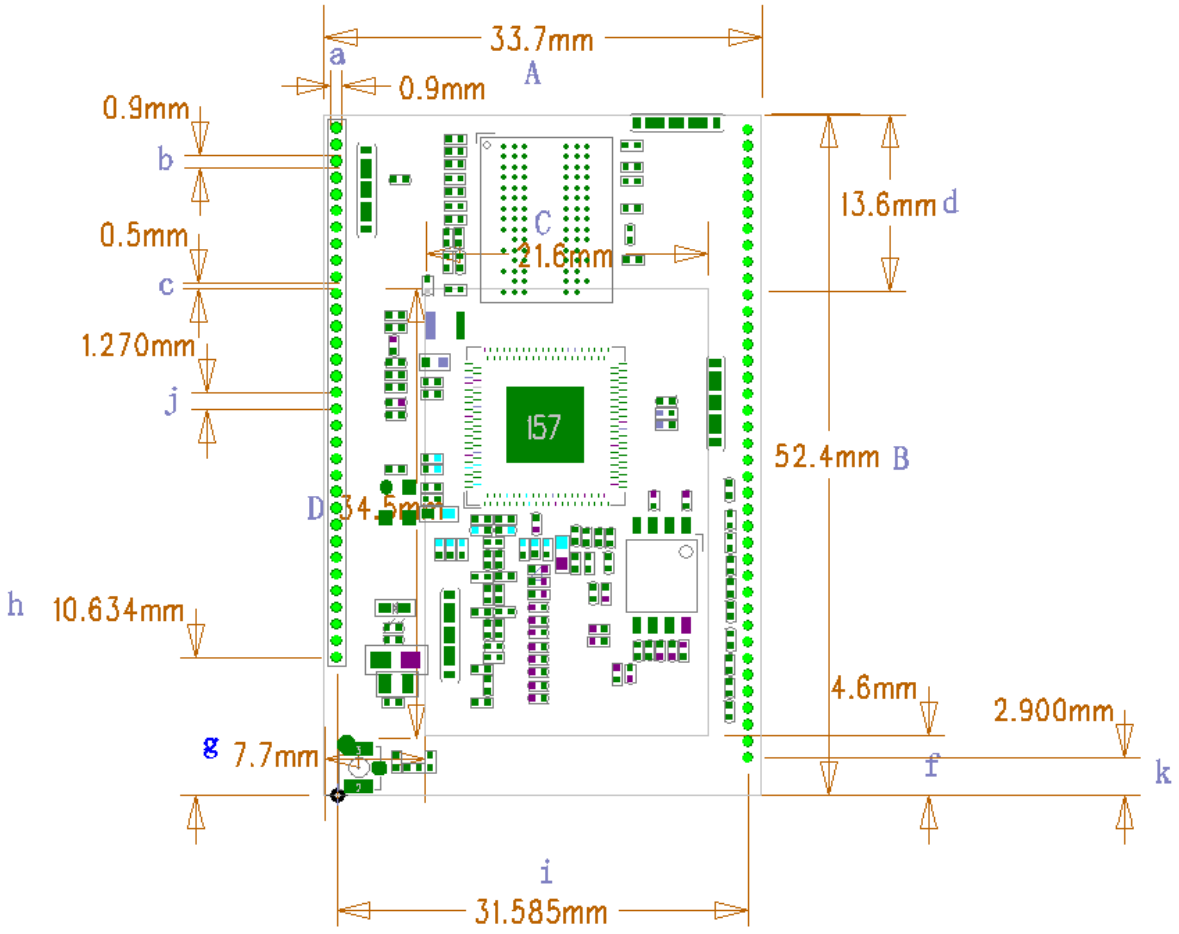
Module Top



Module Bottom

4 MECHANICAL AND STRUCTURE DIAGRAM

Dimensions (mm)	Length	Width	Height (without shield)
	52.4 (Tolerance:±0.2mm)	33.7 (Tolerance:±0.2mm)	9.0 (Tolerance:±0.2mm)



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5 PINS DESCRIPTION

Pin No.	Name	Description
1	GND	Ground
2	GND	Ground
3	GPIO3	I2S_CLK
4	GPIO2	I2S_WS
5	GPIO1	I2S_SDO
6	GPIO0	I2S_SDI
7	PCIE_TXN0	PCIe0 differential transmit TX -
8	PCIE_TXP0	PCIe0 differential transmit TX +
9	PCIE_RXP0	PCIe0 differential receiver RX +
10	PCIE_RXN0	PCIe0 differential receiver RX -
11	PCIE_CKN0	External reference clock output (negative)
12	PCIE_CKP0	External reference clock output (positive)
13	GPIO36	PERST_N
14	GPIO37	REF_CLKO
15	GPIO38	WDT_RST_N
16	GPIO43	EPHY_LED0_N_JTDO
17	GPIO42	EPHY_LED1_N_JTDI
18	GPIO41	EPHY_LED2_N_JTMS
19	GPIO40	EPHY_LED3_N_JTCLK
20	GPIO39	EPHY_LED4_N_JTRST_N
21	GPIO44	WLED_N
22	GPIO45	UART_TXD1
23	GPIO46	UART_RXD1

24	3.3VD	Power
25	3.3VD	Power
26	3.3VD	Power
27	3.3VD	Power
28	3.3VD	Power
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	GND	Ground
33	GND	Ground
34	GND	Ground
35	GND	Ground
36	GND	Ground
37	GND	Ground
38	USB_DM	USB Port0 data pin Data-
39	USB_DP	USB Port0 data pin Data+
40	GPIO17	MDI_RN_P1
41	GPIO16	MDI_RP_P1
42	GPIO15	MDI_TN_P1
43	GPIO14	MDI_TP_P1
44	TXON0	10/100 PHY Port #0 TXN
45	TXOP0	10/100 PHY Port #0 TXP
46	RXIN0	10/100 PHY Port #0 RXN
47	RXIP0	10/100 PHY Port #0 RXP
48	GPIO13	UART_RXD0
49	GPIO12	UART_TXD0

50	GPIO11	GPIO0
51	GPIO6	SPI_CS1
52	GPIO5	I2C_SD
53	GPIO4	2C_SCLK
54	GPIO9	SPI_MISO
55	GPIO8	SPI_MOSI
56	GPIO7	SPI_CLK
57	GPIO29	MDI_TN_P4
58	GPIO28	MDI_TP_P4
59	GPIO27	MDI_RN_P4
60	GPIO26	MDI_RP_P4
61	GPIO25	MDI_RN_P3
62	GPIO24	MDI_RP_P3
63	GPIO23	MDI_TN_P3
64	GPIO22	MDI_TP_P3
65	GPIO21	MDI_TN_P2
66	GPIO20	MDI_TP_P2
67	GPIO19	MDI_RN_P2
68	GPIO18	MDI_RP_P2
69	GND	Ground
70	GND	Ground
71	GND	Ground
72	GND	Ground

NOTE：

I/O supply voltage	3.3V
Input,Output,or I/O Voltage	GND-0.3 V to Vcc +0.3V

6 PIN SHARE SCHEME

UART1 pin share scheme

Controlled by the UART1_MODE register.

Pin Name	2'b00 UART-Lite #1	2'b01 GPIO	2'b10 PWM	2'b11 TRX_SW
UART1_RXD	UART1_RXD	GPIO#46	PWM_CH1	
UART1_TXD	UART1_TXD	GPIO#45	PWM_CH0	

MT7688AN EPHY LED pin share scheme

Controlled by the P#_LED_AN_MODE registers

Pin Name	Bootstrapping (DBG_JTAG_MODE=1)	Bootstrapping (DBG_JTAG_MODE=0)	
		P4_LED_AN_MODE =2'b00	P4_LED_AN_MODE =2'b01
EPHY_LED4_N_JTRST_N	JTAG_RST_N	EPHY_LED4_N	GPIO#39
		P3_LED_AN_MODE =2'b00	P3_LED_AN_MODE =2'b01
EPHY_LED3_N_JTCLK	JTAG_CLK	EPHY_LED3_N	GPIO#40
		P2_LED_AN_MODE =2'b00	P2_LED_AN_MODE =2'b01
EPHY_LED2_N_JTMS	JTAG_TMS	EPHY_LED2_N	GPIO#41
		P1_LED_AN_MODE =2'b00	P1_LED_AN_MODE =2'b01
EPHY_LED1_N_JTDI	JTAG_TDI	EPHY_LED1_N	GPIO#42
		P0_LED_AN_MODE =2'b00	P0_LED_AN_MODE =2'b01
EPHY_LED0_N_JTDO	JTAG_TDO	EPHY_LED0_N	GPIO#43

MT7688AN WLAN LED pin share scheme

Controlled by the WLED_AN_MODE registers

Pin Name	2'b00	2'b01
WLED_N	WLED_N	GPIO#44

PERST_N pin share scheme

Controlled by the PERST_ MODE register.

Pin Name	1'b0	1'b1
PERST_N	PERST_N	GPIO#36

WDT_RST_N pin share scheme

Controlled by the WDT _MODE register.

Pin Name	1'b0	1'b1
WDT_RST_N	WDT_RST_N	GPIO#37

REF_CLKO pin share scheme

Controlled by the REFCLK _MODE register.

Pin Name	1'b0	1'b1
REF_CLKO	REF_CLKO	GPIO#38

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UART0 pin share scheme

Controlled by the UART0 _MODE register.

Pin Name	1'b0	1'b1
UART_TXD0	UART_TXD0	GPIO#12
UART_TXD0	UART_RXD0	GPIO#13

GPIO0 pin share scheme

Controlled by GPIO_MODE register.

Pin Name	2'b00	2'b01	2'b10	2'b11
GPIO0	GPIO#11	GPIO#11	REF_CLKO	PERST_N

SPI pin share scheme

Controlled by SPI_ MODE register.

Pin Name	1'b0	1'b1
SPI_CLK	SPI_CLK	GPO#7
SPI_MOSI	SPI_MOSI	GPO#8
SPI_MISO	SPI_MISO	GPIO#9
SPI_CS0	SPI_CS0	GPIO#10

SPI_CS1 pin share scheme

Controlled by SPI_CS1_MODE register.

Pin Name	2'b00	2'b01	2'b10
SPI_CS1	SPI_CS1	GPIO#6	REF_CLKO

I2C pin share scheme

Controlled by I2C_MODE register.

Pin Name	2'b00	2'b01
I2C_SCLK	I2C_SCLK	GPIO#4
I2C_SD	I2C_SD	GPIO#5

I2S pin share scheme

Controlled by I2S_MODE register.

Pin Name	2'b00	2'b01	2'b10
I2S_SDI	I2C_SCLK	GPIO#0	PCMDRX
I2S_SDO	I2C_SD	GPIO#1	PCMDTX
I2S_WS	I2C_SCLK	GPIO#2	PCMCLK
I2S_CLK	I2C_SD	GPIO#3	PCMFS

SD pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

Pin Name	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	SD_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	SD_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	SD_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	SD_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	SD_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	SD_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	SD_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	SD_D3	GPIO#29

eMMC pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

Pin Name	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	eMMC_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	eMMC_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	eMMC_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	eMMC_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	eMMC_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	eMMC_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	eMMC_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	eMMC_D3	GPIO#29

UART2 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and UART2_MODE registers

Pin Name	4'b0000	4'b1111			
		2'b00	2'b01	2'b10	2'b11
MDI_TP_P2	MDI_TP_P2	UART_TXD2	GPIO#20	PWM_CH2	eMMC_D5
MDI_TN_P2	MDI_TN_P2	UART_RXD2	GPIO#21	PWM_CH3	eMMC_D4

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PWM_CH1 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM1_MODE registers

	4'b0000	4'b1111			
Pin Name		**2'b00**	**2'b01**	**2'b10**	**2'b11**
MDI_RN_P2	MDI_RN_P2	PWM_CH1	GPIO#19		eMMC_D6

PWM_CH0 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM0_MODE registers

	4'b0000	4'b1111			
Pin Name		**2'b00**	**2'b01**	**2'b10**	**2'b11**
MDI_RP_P2	MDI_RP_P2	PWM_CH0	GPIO#18		eMMC_D7

SPIS pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SPIS_MODE registers

	4'b0000	4'b1111			
Pin Name		**2'b00**	**2'b01**	**2'b10**	**2'b11**
MDI_TP_P1	MDI_TP_P1	SPIS_CS	GPIO#14		PWM_CH0
MDI_TN_P1	MDI_TN_P1	SPIS_CLK	GPIO#15		PWM_CH1
MDI_RP_P1	MDI_RP_P1	SPIS_MISO	GPIO#16		UART_TXD2
MDI_RN_P1	MDI_RN_P1	SPIS_MOSI	GPIO#17		UART_RXD2

Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7688AN only. It needs to be pull-low for 7688KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

7 OPERATING AND STORAGE CONDITIONS

Operating conditions

I/O supply voltage	3.3 V +/- 10%
DDR1 supply voltage	2.5 V +/- 5%
DDR2 supply voltage	1.8 V +/- 5%
Core supply voltage	1.2 V +/- 10%
Ambient Temperature Range	0 to 50 °C

storage condition

The calculated shelf life in a sealed bag is 12 months if stored between -20 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

8 INSTALLED MATTERS NEEDING ATTENTION (FOR WIFI MODULE)

a. In the opening of the steel mesh, the module of the pad hole in a ratio of 1:1 to expand 0.7mm and thickness of 0.12 mm.

b. Putting the module to the oven at 120 ℃ (±5℃) baking for 12 hours, and then on the basis of how much per hour can stick taking out the corresponding number of modules.

c. Bring gloves and electrostatic ring to get the module.

d. The furnace temperature on the basis of main board size .

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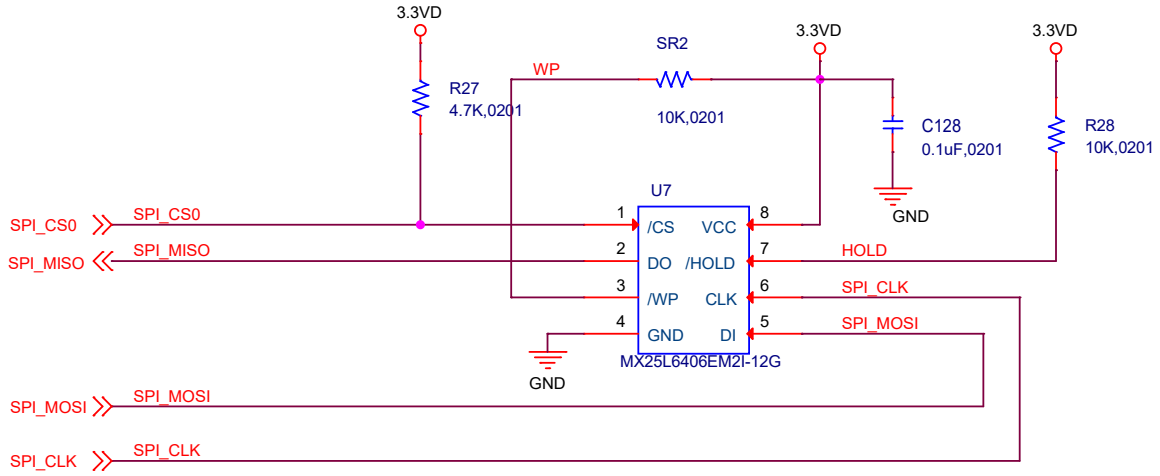
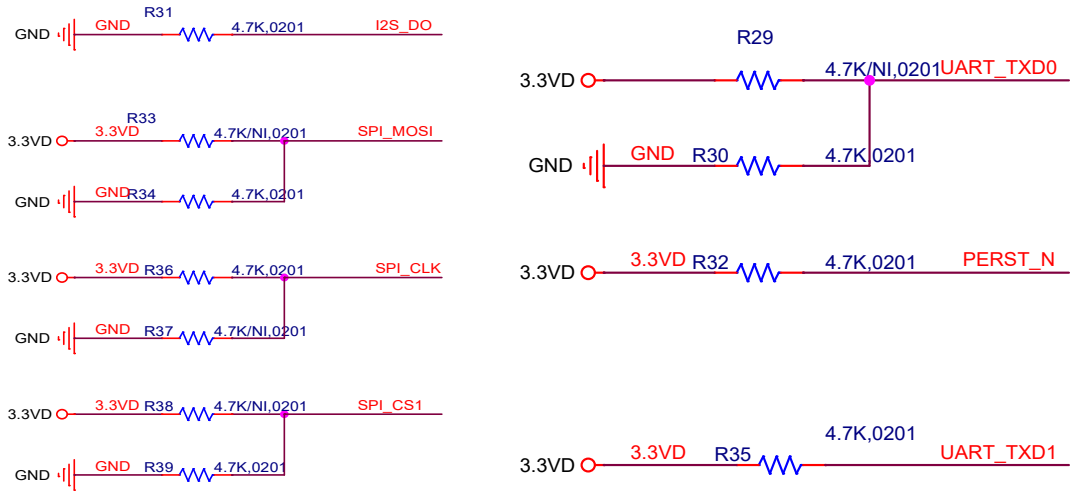
9 ENCLOSURE

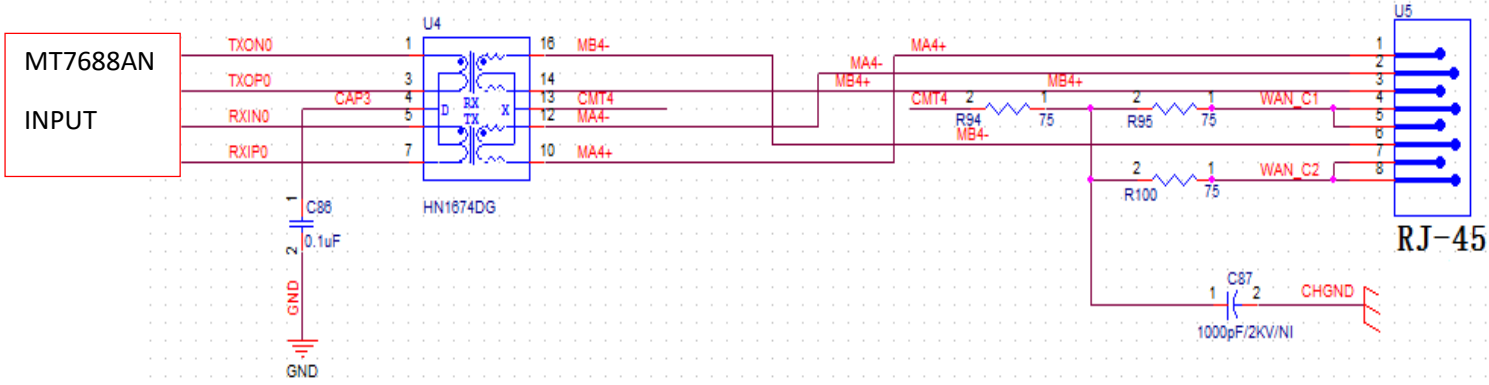
(1) SPI Flash Schematic



(2) Bootstrap CONFIG Schematic



(3) Net port connection



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