

GAINSTRONG

Oolite-IPQ6010_SPEC_EN

Version 1.0.1

Author : WSY

August 29, 2021

1. PRODUCT OVERVIEW

General Description

Oolite-IPQ6010 is a dual-band WiFi6 wireless routing module developed based on Qualcomm IPQ6000/6010/6018 quad-core ARM Cortex A53 platform; it complies with IEEE 802.11a/b/g/n/ac/ax wireless standards, and the wireless rate is up to 1800Mbps, can provide SGMII+*1 (extended optical port), 2.5G network port*1, Gigabit network port*5, PCIE3.0*1, USB3.0*1, USB2.0*1, UART, SPI, I2C Equivalent function interface and multiple GPIO general function pins.

The board-to-board high-speed connector installation method can be used to connect different types of interface board designs to expand WIFI6 wireless routing, network storage, advertising hotspots, 5G_CPE, DTU data transmission, serial port to WIFI, remote monitoring and other multi-functional product applications; This simplifies the wireless network product development and design process.

Gainstrong Technology can provide software development services and custom interface board design that meet customer requirements for this module according to customer applications.

Features

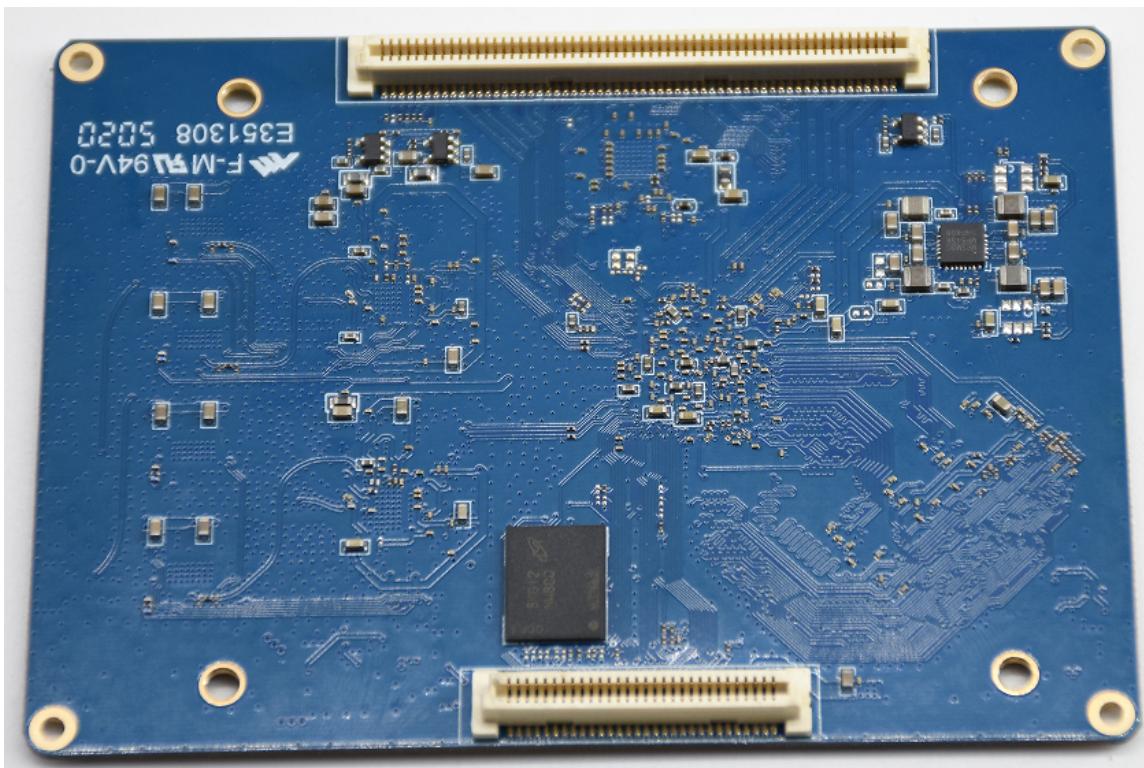
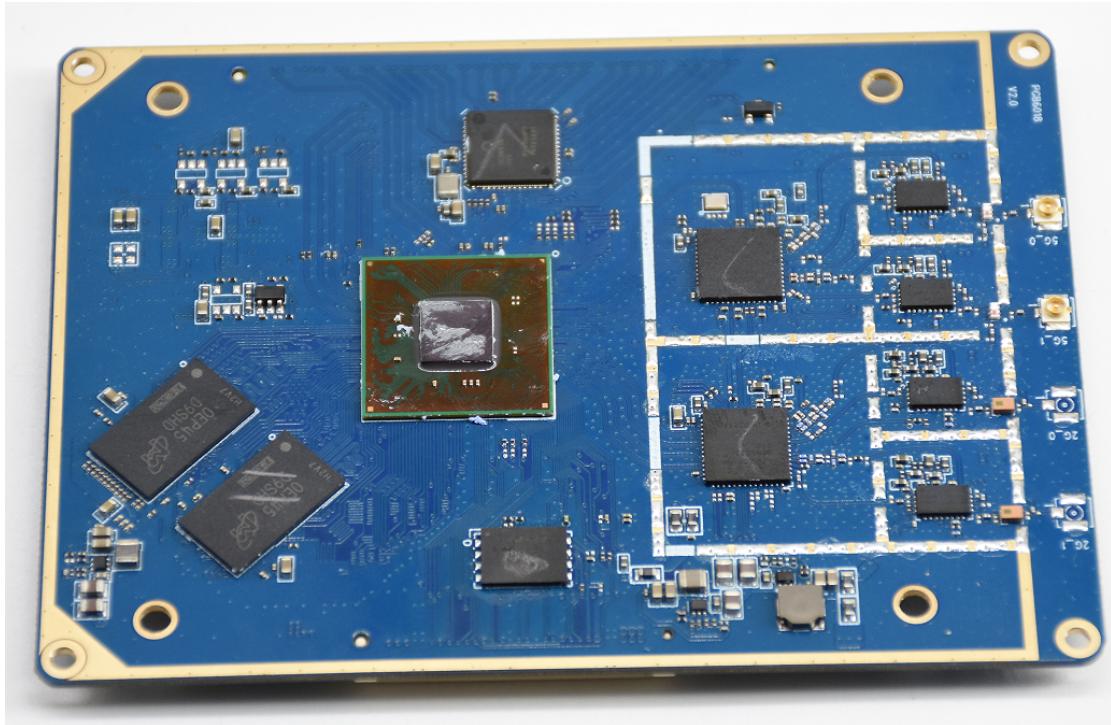
- Adopt OPENWRT deep customization system
- Support a variety of 3G/4G/5G wireless modules, basically plug and play
- Support 4G backup network, seamlessly switch to 4G network when the cable is disconnected, and can automatically detect the cable recovery
- Cloud remote background management, advertising push, remote upgrade and remote configuration
- Support USB storage device
- Local network PHP browsing, and remote synchronization of local storage content
- Support serial data serial port TCP/UDP transparent data transmission or AT command transmission
- Support VPN security tunnel function, including PPTP, L2TP
- Complete and robust router functions, support multiple ways to access the Internet: automatic allocation, designated IP, PPPoE
- Support IPTABLES firewall, various network protocols
- Support dynamic DDNS: support peanut shell, 88IP and dyndns domain name service providers
- Convenient and easy-to-use CONSOLE and SYSLOG system diagnosis and debugging functions
- Support serial port local TFTP, web software upgrade

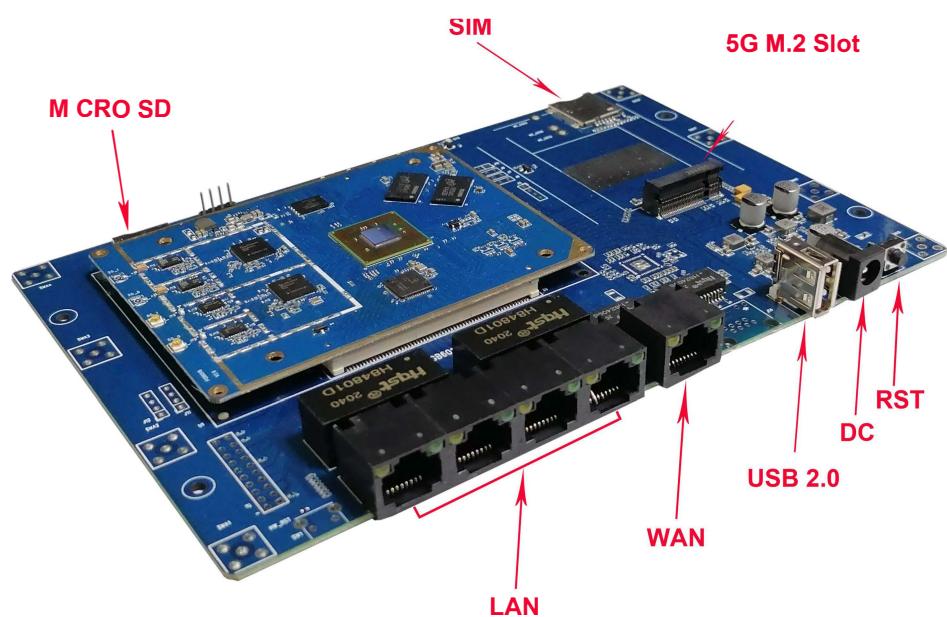
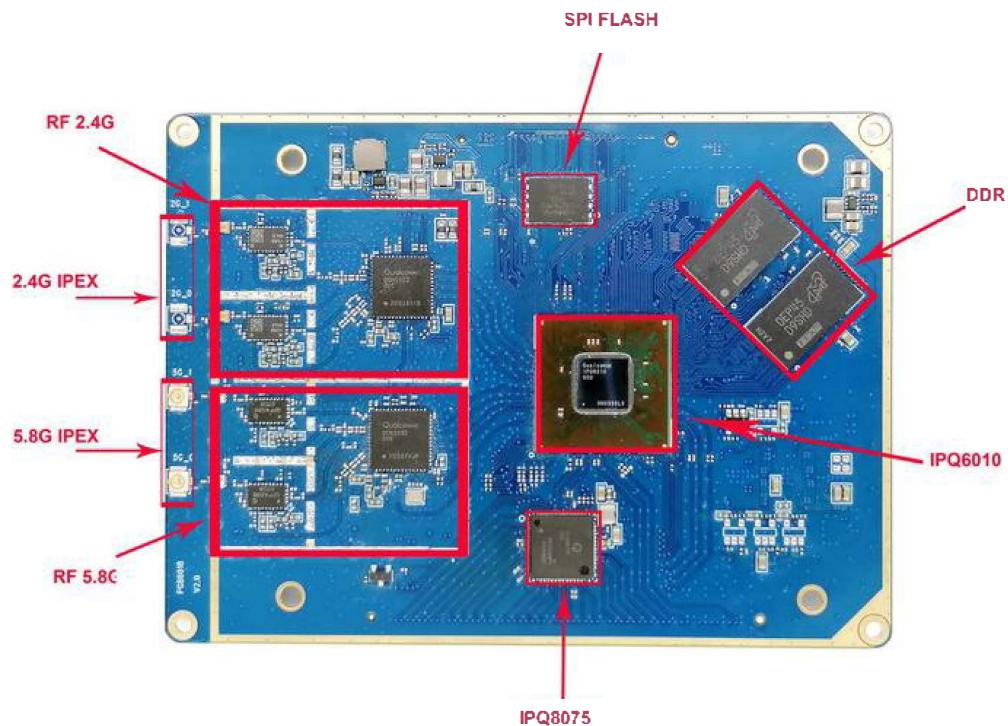
PS: The software function version is subject to the factory firmware; provides the hardware reference design of the expansion interface backplane;

2.Specifications

Model	IPQ6010
Chipset	CPU: IPQ6010 Quad core ARM Cortex A53 1.8GHz PHY: QCA8075
Memory	DDR3L 32bits 512MB*2
NAND Flash	256MB
NOR Flash	16MB
Wireless	QCA5152: 5 GHz: 2x2/80 MHz rate: 1200 Mbps POUT = +18dBm MCS11 HE80 -43dB EVM POUT = +26dBm @MCS0 QCA5122: 2.4 GHz: 2x2/40 MHz rate: 573.5 Mbps POUT = +19dBm MCS11 HE40 -43dB EVM POUT = +27dBm @MCS0
Expansion	1x PCIE3.0 1x USB 3.0 1x USB 2.0 1x SGMII 1x SD/eMMC
Interface	5x Gigabit Ethernet Port SPI UART I2C JTAG
POWER INPUT	DC3.3V @3A ; DC5V@3A; DC12V@0.5A
POWER COSUMPTION	TBD
SIZE	98*72*10mm

3.PICTURES





4.PIN DEFINITION

NO.	Describe	NO.	Describe	NO.	Describe	Function
1	GND	61	GND	121	2.4G_XPA_DC5V_IN	NC
2	P0_TRX0+	62	P0_1000M_LED	122	2.4G_XPA_DC5V_IN	NC
3	P0_TRX0-	63	P1_1000M_LED	123	2.4G_XPA_DC5V_IN	NC
4	P0_TRX1+	64	P2_1000M_LED	124	GND	
5	P0_TRX1-	65	P3_1000M_LED	125	GND	
6	P0_TRX2+	66	P4_1000M_LED	126	GPIO_0	
7	P0_TRX2-	67	ETH_LED_PWR_2.7V_OUT	127	GPIO16	
8	P0_TRX3+	68	GPIO_73	128	GPIO18	
9	P0_TRX3-	69	GPIO_68	129	GPIO2	
10	GND	70	GND	130	GPIO21	
11	P1_TRX0+	71	SPI_MISO_UART_RX_GPIO71	131	GPIO19	
12	P1_TRX0-	72	SPI莫斯 UART TX GPIO72	132	GPIO53	
13	P1_TRX1+	73	SPI_CS_UART_CTSN_GPIO70	133	GPIO43	
14	P1_TRX1-	74	SPI_CLK_UART_RTSN_GPIO69	134	GPIO42	
15	P1_TRX2+	75	GND	135	GPIO26	
16	P1_TRX2-	76	QTZ_INT_GPIO78	136	GND	
17	P1_TRX3+	77	QTZ_RESET_GPIO79	137	GPIO52	
18	P1_TRX3-	78	GPIO_49	138	GPIO33	
19	GND	79	GND	139	GPIO22	
20	P2_TRX0+	80	SD_LDO_EN	140	GPIO51	
21	P2_TRX0-	81	CP_SRSTN	141	GPIO29	
22	P2_TRX1+	82	CP_TMS	142	GPIO30	
23	P2_TRX1-	83	CP_TDI	143	GPIO31	
24	P2_TRX2+	84	CP_TRSTN	144	GPIO32	
25	P2_TRX2-	85	CP_TCK	145	GPIO36	
26	P2_TRX3+	86	CP_TDO	146	GND	
27	P2_TRX3-	87	GND	147	GND	
28	GND	88	SDC1_DATA_0	148	SOC-DC3V3_IN	
29	P3_TRX0+	89	SDC1_DATA_1	149	SOC-DC3V3_IN	
30	P3_TRX0-	90	SDC1_DATA_2	150	SOC-DC3V3_IN	
31	P3_TRX1+	91	SDC1_DATA_3	151	5G_XPA_DC5V_IN	
32	P3_TRX1-	92	SDC1_CLK	152	5G_XPA_DC5V_IN	
33	P3_TRX2+	93	SDC1_CMD	153	5G_XPA_DC5V_IN	

34	P3_TRX2-	94	SDC1_DET_GPIO62	154	GND
35	P3_TRX3+	95	SDC1_WP_GPIO63	155	GND
36	P3_TRX3-	96	GND	156	VDD_1V8_OUT
37	GND	97	PCIE_CLK_REQ_GPIO59	157	FLASH_1V8
38	P4_TRX0+	98	PCIE_PERET_N_GPIO60	158	FLASH_WP_HOLD
39	P4_TRX0-	99	GND	159	SPI0_CLK_GPIO38
40	P4_TRX1+	100	PCI_E_TX_P	160	SPI0_MOSI_GPIO41
41	P4_TRX1-	101	PCI_E_TX_N	161	SPI0_CS_IN_GPIO39
42	P4_TRX2+	102	GND	162	SPI0_MISO_GPIO40
43	P4_TRX2-	103	PCI_E_RX_P	163	GND
44	P4_TRX3+	104	PCI_E_RX_N	164	UART_TX_1V8_DEBUG
45	P4_TRX3-	105	GND	165	UART_RX_1V8_DEBUG
46	GND	106	PCIE_REFCLKP	166	GND
47	USXGMII0_TX_N	107	PCIE_REFCLKN	167	GPIO23
48	USXGMII0_TX_P	108	GND	168	CYPRESS_RESET_OUT
49	GND	109	CONN_USB0_DM	169	GPIO24
50	USXGMII0_RX_N	110	CONN_USB0_DP	170	WPS_GPIO9
51	USXGMII0_RX_P	111	GND	171	LED_SYS_OUTGPIO25
52	GND	112	CONN_USB0_SS_TXN	172	GPIO34
53	NAPA_RESET_GPIO77	113	CONN_USB0_SS_TXP	173	LED_USB_GPIO50
54	MDIO_GPIO65	114	GND	174	WIFI_LED_2.4G_GPIO37
55	MDC_GPIO64	115	CONN_USB0_SS_RXN	175	WIFI_LED_5G_GPIO35
56	NAPA_INTO_GPIO76	116	CONN_USB0_SS_RXP	176	GND
57	GND	117	GND	177	GND
58	CLK_50M_N_NAPA1	118	CONN_USB1_DM	178	SOC_DC12V_IN
59	CLK_50M_P_NAPA1	119	CONN_USB1_DP	179	SOC_DC12V_IN
60	GND	120	GND	180	SOC_DC12V_IN

The default GPIO definition of the Development board :

SYS_LED	GPIO 25
NET_LED	GPIO 24
USB_LED	GPIO50
2.5G_ETH_LED	GPIO34
2.4G_WIFI LED	GPIO37
5G_WIFI LED	GPIO35
RST_Button	GPIO9
5G M.2 SW	GPIO29