MT7688AN/MT7628AN Core Module

OoliteV3.2 Module

Specification Version V1.0.6

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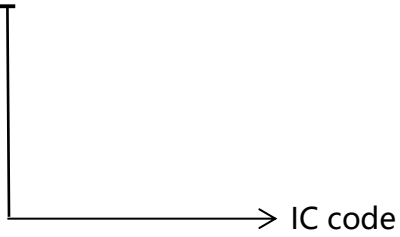
Revision	Date	Contents of Revision Change	Remark
1.0.1	2016-08-29	First release	
1.0.2	2016-09-27	Modify naming	
1.0.3	2016-09-28	Modify naming and content	
1.0.4	2016-10-5	Modify content	
1.0.5	2017-05-26	Fixed Size Marking Error	James
1.0.6	2023-02-16	Add the corresponding relationship between module pins and GPIO numbers, and add the GPIO and function correspondence table of MT76x8 chip	Joe

MODULE CODE

Oolite -V3.2S/D



IC code	IC
S	MT7688AN
D	MT7628AN

1 INTRODUCTION

The Oolite V3.2 module can use the MT7688AN chipset or MT7628AN chipset.

1.1 Oolite V3.2D

The Oolite V3.2D module use the MT7628AN chipset.The MT7628AN includes a high performance 580/575 MHz MIPS 24KEc CPU core and high speed USB2.0/PCIe interfaces, which is designed to enable a multitude of high performance, cost-effective IEEE 802.11n applications with a MediaTek WiFi client card.There are several masters (MIPS 24KEc, USB, PCI Express, SDXC, FE) in the MT7628 SoC on a high performance,low latency Rbus. In addition, the MT7628 SoC supports lower speed peripherals such as UART Lite, GPIO, I2C and SPI via a low speed peripheral bus (Pbus). The DDR/DDR2 controller is the only bus slave on the Rbus. It includes an Advanced Memory Scheduler to arbitrate the requests from bus masters, enhancing the performance of memory access intensive tasks.

Features:

- CPU: MT7628AN with 580/575 MHz MIPS 24KEc
- RAM: 128MB DDR2 RAM (64MB optional)
- Flash: 16MB SPI NOR Flash ROM(8/16/32/64M option)
- Wireless speed: 300Mbps
- GPIO:37(total), High-speed UART for console support
- USB: Usb 2.0 master interface, support USB hub extension
- Power supply voltage: 3.3V.
- Port: 1×WAN+ 4×LAN (IOT mode 1×port)
- 1×PCIE interface
- Antenna:2× IPeX external antenna.
- Debug: serial debugging interface has lead out.
- Supports 16 DMA channels and 32 bit address.
- 8 channel QoS Arbiter with Configurable Bandwidth and Duedate for each agent.
- Supports the Synchronous Inter-Integrated Circuits (I^2C) serial protocol.
- Supports up to 2 SPI master operations and Extends the addressable range from 24 bits to 32 bits for memory size larger than 128 Mb.

1.2 Oolite V3.2S

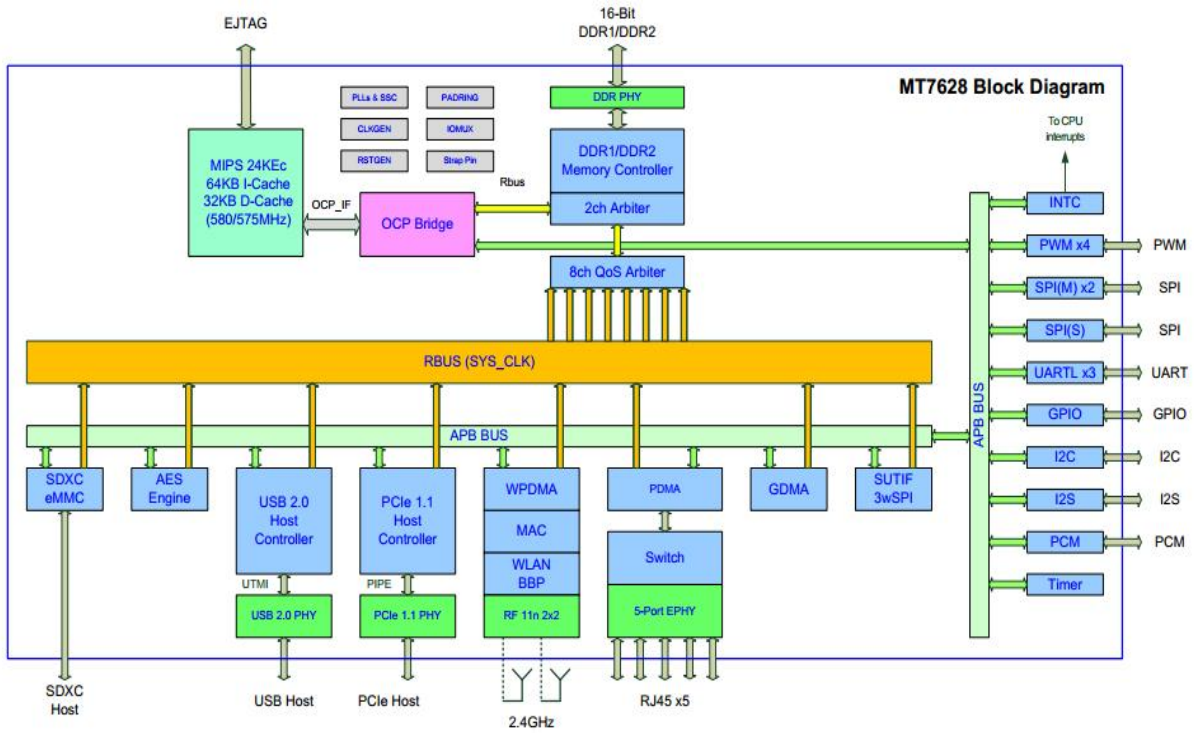
The Oolite V3.2S module use the MT7688AN chipset.The MT7688AN integrates a 1T1R 802.11n Wi-Fi radio, a 580MHz MIPS® 24KEc™ CPU, 1-port fast Ethernet PHY, USB2.0 host, PCIe, SD-XC, I2S/PCM and multiple slow IOs. The MT7688AN provides two operation modes – IoT gateway mode and IoT device mode. In IoT gateway mode, the PCI Express interface can connect to 802.11ac chipset for 11ac dual-band concurrent gateway. The high performance USB 2.0 allows the MT7688AN to add 3G/LTE modem support or add a H.264 ISP for wireless IP camera. For the IoT device mode, the MT7688AN supports eMMC, SD-XC and USB 2.0. The MT7688AN can support the WiFi high quality audio via 192Kbps/24bits I2S interface and VoIP application through PCM. In IoT device mode, it further supports PWM, SPI slave, 3rd UART and more GPIOs. For IoT gateway, it can connect to touch panel and BLE, Zigbee/Z-Wave and sub-1G RF for smart home control.

Features:

- CPU: MT7688AN with 580/575 MHz MIPS 24KEc
- RAM: 128MB DDR2 RAM (256MB optional)
- Flash: 16MB SPI NOR Flash ROM(8/16/32/64M option)
- Wireless speed: 150Mbps
- GPIO:41(total), High-speed UART for console support
- USB: Usb 2.0 master interface, support USB hub extension
- Power supply voltage: 3.3V.
- Port: 1×port (IOT Device Mode),1×WAN+ 4×LAN (IOT Gateway Mode),
- 1×PCIE interface
- Antenna:1× IPeX external antenna.
- 20/40 MHz channel bandwidth
- Supports Legacy 802.11b/g ,HT 802.11n and 802.11vmodes
- Supports WEP64/128, TKIP, AES, WPA, WPA2, WAPI
- Green AP/STA
  - Intelligent Clock Scaling (exclusive)
  - DDRII: ODT off, Self-refresh mode
- iPA/iLNA and ePA/eLNA
- Embedded PMU

2 FUNCTIONAL BLOCK DIAGRAM

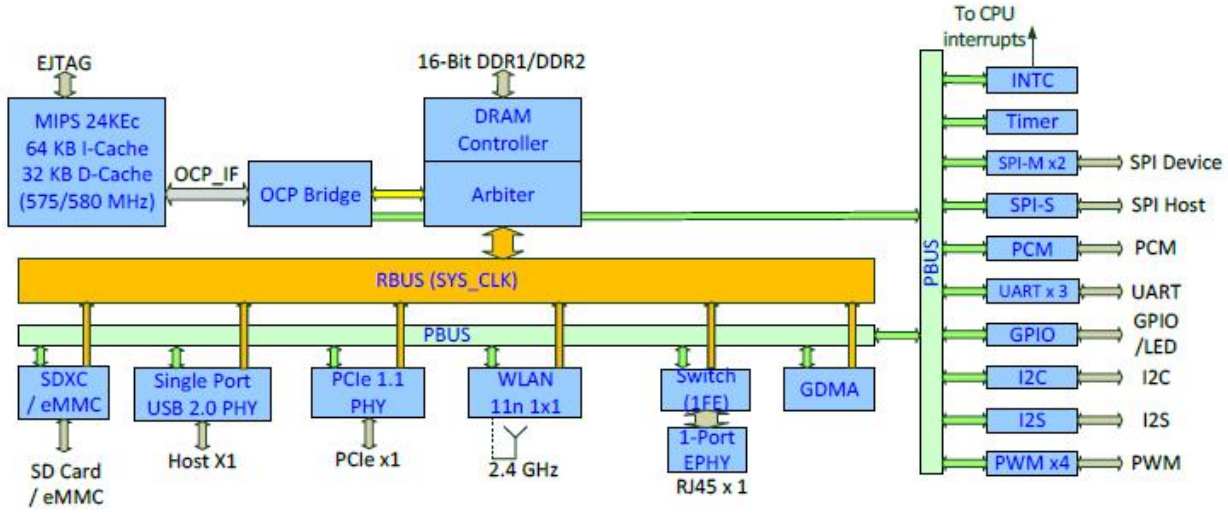
2.1 Oolite V3.2D



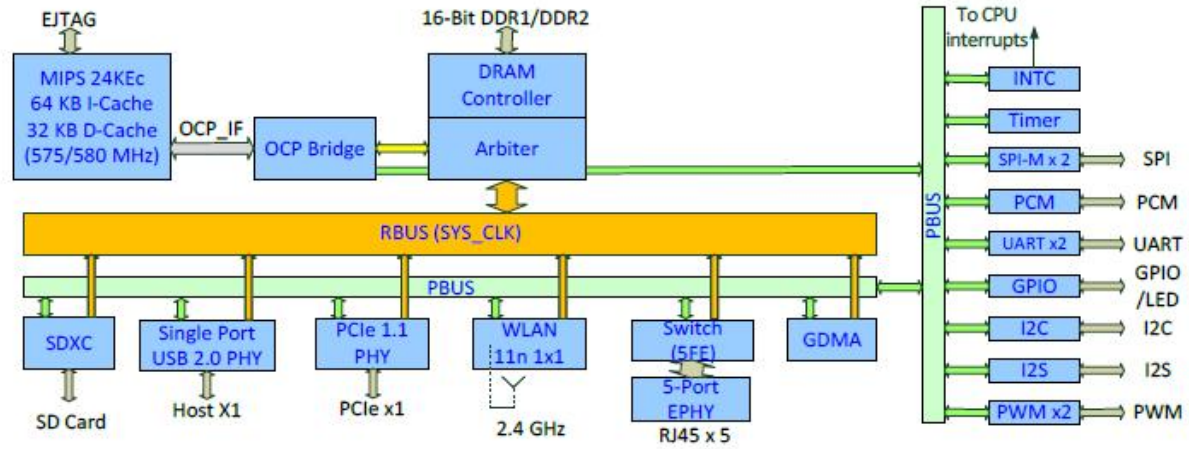
TBD

2.2 Oolite V3.2S

IoT Device Mode

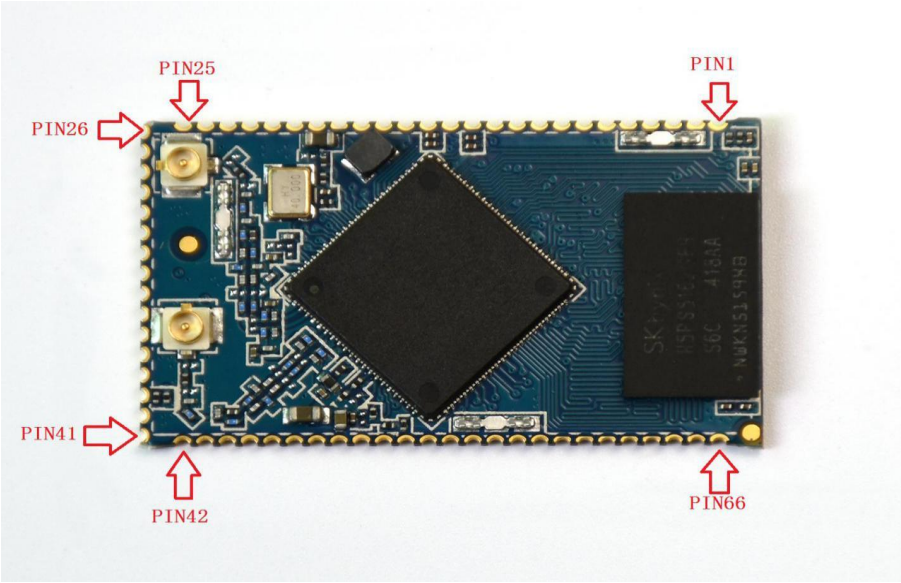


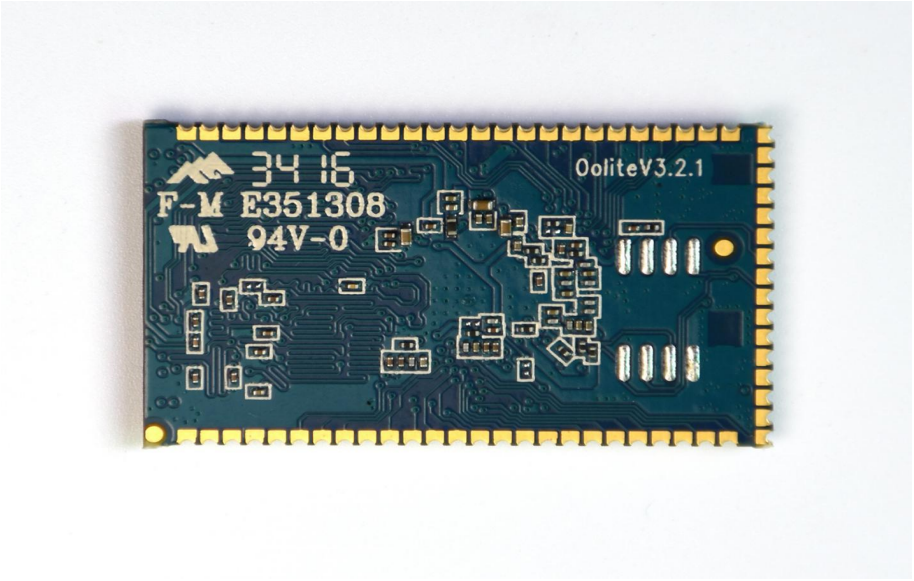
IoT Gateway Mode



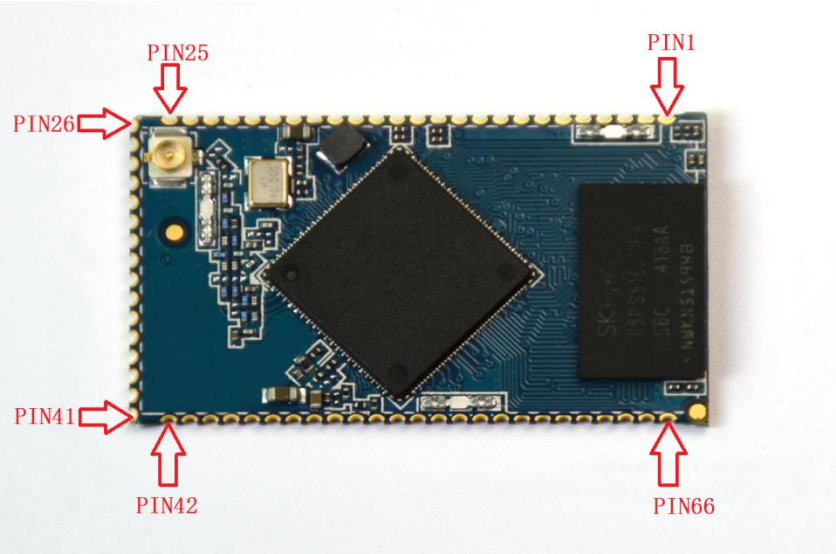
3 PICTURES

3.1 Oolite V3.2D





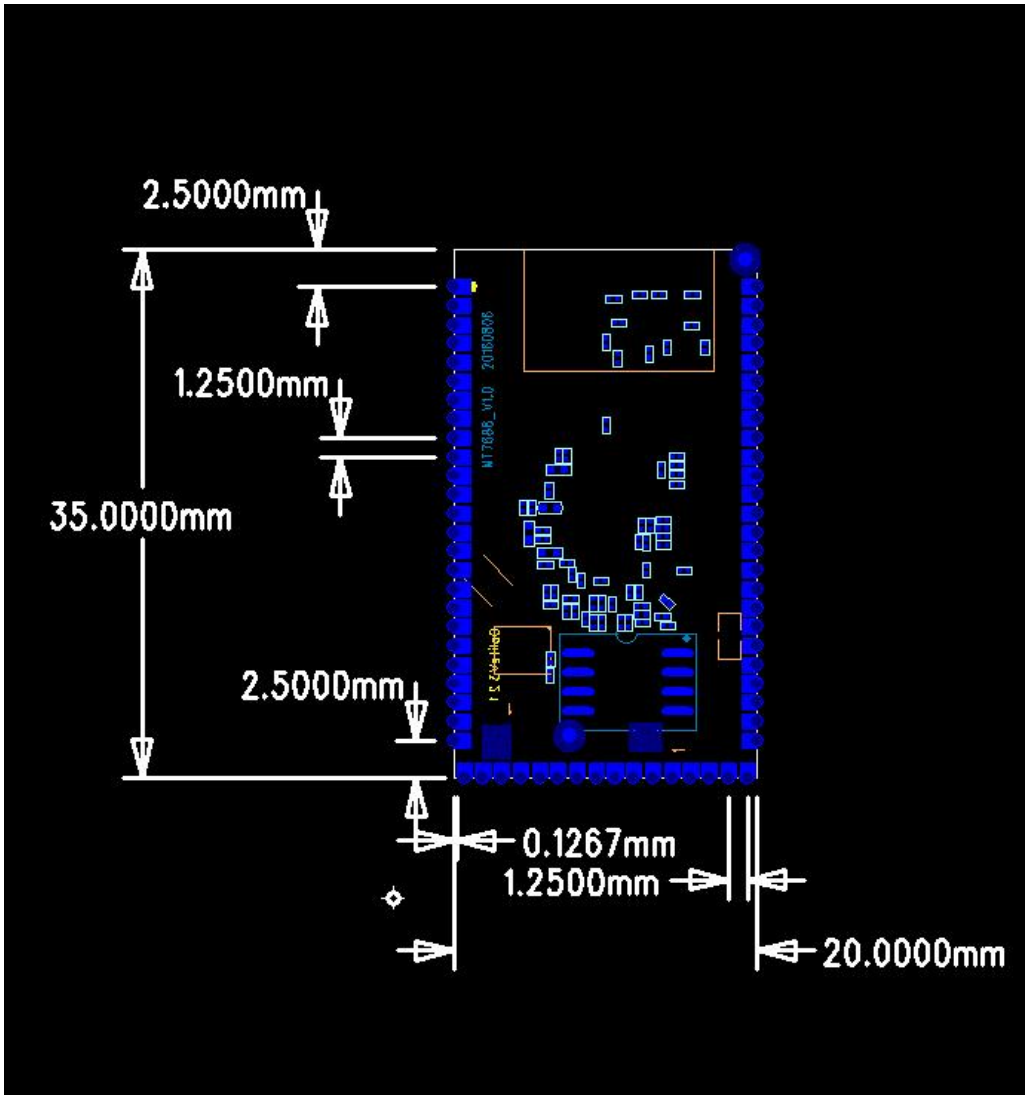
3.2 Oolite V3.2S



4 MECHANICAL

Oolite V3.2D and Oolite V3.2S are the same

Dimensions (mm)	Length	Width	Height (without shield)
	35.0 (Tolerance:±0.2mm)	20.0 (Tolerance:±0.2mm)	1.0 (Tolerance:±0.2mm)



Pin No.	GPIO No.	Name	Description
1		GND	Ground
2		GND	Ground
3		3.3V	Power
4		3.3V	Power
5		3.3V	Power
6		GND	Ground
7		PCIE_TXN0	PCIe0 differential transmit TX -
8		PCIE_TXP0	PCIe0 differential transmit TX +
9		N175406288/PCIE_RXP0	PCIe0 differential transmit RX +
10		N175406289/PCIE_RXN0	PCIe0 differential transmit RX-
11		PCIE_CKN0	External reference clock output (negative)
12		PCIE_CKP0	External reference clock output (positive)
13	36	PERST_N	PCIe device reset
14	37	REFCLK0_OUT	Reference Clock Ouptut
15	38	WPS_RST_PBC	Watchdog timeout reset
16		CPURST_N	Power on reset
17	39	LINK4	10/100 PHY Port #4 activity LED
18	40	LINK3	10/100 PHY Port #4 activity LED
19	41	LINK2	10/100 PHY Port #2 activity LED
20	42	LINK1	10/100 PHY Port #1 activity LED
21	43	LINK0	10/100 PHY Port #0 activity LED
22	44	WLED_N	WLAN Activity LED

23	45	UART_TXD1	UART1 Lite TXD
24	46	UART_RXD1	UART1 Lite RXD
25	0	I2S_DI	I2S data input
26	1	I2S_DO	I2S data output
27	2	I2S_WS	I2S word select
28	3	I2S_CLK	I2S clock
29	4	I2C_SCLK	I2C clock
30	5	I2C_SD	I2C Data
31	6	SPI_CS1	SPI chip select1
32	7	SPI_CLK	SPI clock
33	8	SPI_MISO	SPI Master input/Slave output
34	9	SPI_MOSI	SPI Master output/Slave output
35	10	SPI_CS0	SPI chip select0
36	11	GPIO0	General Purpose I/O
37		GND	Ground
38	12	UART_TXD0	UART0 Lite TXD
39	13	UART_RXD0	UART0 Lite RXD
40		GND	Ground
41		RXIP0	10/100 PHY Port #0 RXP
42		RXIN0	10/100 PHY Port #0 RXN
43		TXOP0	10/100 PHY Port #0 TXP
44		TXON0	10/100 PHY Port #0 TXN
45		GND	Ground
46	14	TXOP1	10/100 PHY Port #1 TXP
47	15	TXON1	10/100 PHY Port #1 TXN
48	16	RXIP1	10/100 PHY Port #1 RXP

49	17	RXIN1	10/100 PHY Port #1 RXN
50		GND	Ground
51	18	GPIO18	General Purpose I/O
52	19	GPIO19	General Purpose I/O
53	20	GPIO20	General Purpose I/O
54	21	GPIO21	General Purpose I/O
55	22	GPIO22	General Purpose I/O
56	23	GPIO23	General Purpose I/O
57	24	GPIO24	General Purpose I/O
58	25	GPIO25	General Purpose I/O
59	26	GPIO26	General Purpose I/O
60	27	GPIO27	General Purpose I/O
61	28	GPIO28	General Purpose I/O
62	28	GPIO29	General Purpose I/O
63		GND	Ground
64		USB_D+	USB Port0 data pin Data+
65		USB_D-	USB Port0 data pin Data+
66		GND	Ground

5 PINS DESCRIPTION

Oolite V3.2D and Oolite V3.2S are the same

NOTE：

I:Input

O:Ouput

I/O:Bi-directional

IPL:Internal pull low

A:Analog

Absolute Maximum Ratings

I/O supply voltage	3.3V
Input,Output,or I/O Voltage	GND-0.3 V to Vcc +0.3V

6 PIN SHARE SCHEME

Oolite V3.2D and Oolite V3.2S are the same

MT76x8 GPIO pin mapping (Please refer to chapter 4.8.3 of the chip manual)							
GPIO	PAD Name	Function 0	Function 1	Function 2	Function 3	strap	pmux_group
0	PAD_I2S_SDI	i2ssdi (I)	gpio (I/O)	pcmdrx (I)	antsel[5] (O)		i2s_gpio_psel[2:0]
1	PAD_I2S_SDO	i2ssdo (O)	gpio (I/O)	pcmdtx (O)	antsel[4] (O)	0	i2s_gpio_psel[2:0]
2	PAD_I2S_WS	i2sws(I/O)	gpio (I/O)	pcmclk (I/O)	antsel[3] (O)		i2s_gpio_psel[2:0]
3	PAD_I2S_CLK	i2sclk (I/O)	gpio (I/O)	pcmfs (I/O)	antsel[2] (O)		i2s_gpio_psel[2:0]
4	PAD_I2C_SCLK	i2c_sclk (I/O)	gpio (I/O)	sutif_txd (O)	ext_bgclk (I)		i2c_gpio_psel[2:0]
5	PAD_I2C_SD	i2c_sd (I/O)	gpio (I/O)	sutif_rxd (I)			i2c_gpio_psel[2:0]
6	PAD_SPI_CS1	spi_cs1 (O)	gpio (I/O)	co_clko (O)		1	spi_cs1_psel[2:0]
7	PAD_SPI_CLK	spi_clk (O)	gpio (I/O)			2	spi_gpio_psel[1:0]
8	PAD_SPI_MOSI	spi_mosi (I/O)	gpio (I/O)			3	spi_gpio_psel[1:0]
9	PAD_SPI_MISO	spi_miso (I/O)	gpio (I/O)				spi_gpio_psel[1:0]
10	PAD_SPI_CS0	spi_cs0 (O)	gpio (I/O)				spi_gpio_psel[1:0]
11	PAD_GPIO0	gpio (I/O)	gpio (I/O)	co_clko (O)	perst_n (O)	4	gpio_psel[2:0]
12	PAD_TXD0	txd0 (O)	gpio (I/O)			5	uart0_gpio_psel[2:0]
13	PAD_RXD0	rxd0 (I)	gpio (I/O)				uart0_gpio_psel[2:0]
14	PAD_MDI_TP_P1	spis_cs (I)	gpio (I/O)	w_utif[0] (I/O)	pwm_ch0 (O)		spis_gpio_psel[2:0]
15	PAD_MDI_TN_P1	spis_clk (I)	gpio (I/O)	w_utif[1] (I/O)	pwm_ch1 (O)		spis_gpio_psel[2:0]
16	PAD_MDI_RP_P1	spis_miso (O)	gpio (I/O)	w_utif[2] (I/O)	txd2 (O)		spis_gpio_psel[2:0]
17	PAD_MDI_RN_P1	spis_mosi (I)	gpio (I/O)	w_utif[3] (I/O)	rxd2 (I)		spis_gpio_psel[2:0]
18	PAD_MDI_RP_P2	pwm_ch0 (O)	gpio (I/O)	w_utif[4] (I/O)	sd_d7 (I/O)		pwm0_gpio_psel[2:0]
19	PAD_MDI_RN_P2	pwm_ch1 (O)	gpio (I/O)	w_utif[5] (I/O)	sd_d6 (I/O)		pwm1_gpio_psel[2:0]
20	PAD_MDI_TP_P2	txd2 (O)	gpio (I/O)	pwm_ch2 (O)	sd_d5 (I/O)		uart2_gpio_psel[2:0]

21	PAD_MDI_TN_P2	rxd2 (I)	gpio (I/O)	pwm_ch3 (O)	sd_d4 (I/O)		uart2_gpio_psel[2:0]
22	PAD_MDI_TP_P3	sd_wp (I)	gpio (I/O)	w_utif[10] (I/O)	w_dbgin (I)		sd_gpio_psel[2:0]
23	PAD_MDI_TN_P3	sd_cd (I)	gpio (I/O)	w_utif[11] (I/O)	w_dbgack (O)		sd_gpio_psel[2:0]
24	PAD_MDI_RP_P3	sd_d1 (I/O)	gpio (I/O)	w_utif[12] (I/O)	w_jtclk (I)		sd_gpio_psel[2:0]
25	PAD_MDI_RN_P3	sd_d0 (I/O)	gpio (I/O)	w_utif[13] (I/O)	w_jtdi (I)		sd_gpio_psel[2:0]
26	PAD_MDI_RP_P4	sd_clk (I/O)	gpio (I/O)	w_utif[14] (I/O)	w_jtdo (O)		sd_gpio_psel[2:0]
27	PAD_MDI_RN_P4	sd_cmd (I/O)	gpio (I/O)	w_utif[15] (I/O)	dbg_uart_txd (O)		sd_gpio_psel[2:0]
28	PAD_MDI_TP_P4	sd_d3 (I/O)	gpio (I/O)	w_utif[16] (I/O)	w_jtms (I)		sd_gpio_psel[2:0]
29	PAD_MDI_TN_P4	sd_d2 (I/O)	gpio (I/O)	w_utif[17] (I/O)	w_jtrst_n (I)		sd_gpio_psel[2:0]
30	PAD_EPHY_LED4_K	ephy_led4_k (O)	gpio (I/O)	w_utif_k[6] (I/O)	jtrstn_k (I)		p4_led_kn_psel[2:0]
31	PAD_EPHY_LED3_K	ephy_led3_k (O)	gpio (I/O)	w_utif_k[7] (I/O)	jtclk_k (I)		p3_led_kn_psel[2:0]
32	PAD_EPHY_LED2_K	ephy_led2_k (O)	gpio (I/O)	w_utif_k[8] (I/O)	jtms_k (I)		p2_led_kn_psel[2:0]
33	PAD_EPHY_LED1_K	ephy_led1_k (O)	gpio (I/O)	w_utif_k[9] (I/O)	jtdi_k (I)		p1_led_kn_psel[2:0]
34	PAD_EPHY_LED0_K	ephy_led0_k (O)	gpio (I/O)		jtdo_k (I/O)		p0_led_kn_psel[2:0]
35	PAD_WLED_K	wled_k (I/O)	gpio (I/O)				wled_kn_psel[2:0]
36	PAD_PERST_N	perst_n (O)	gpio (I/O)			6	prest_gpio_psel[1:0]
37	PAD_CO_CLKO	co_clko (O)	gpio (I/O)			7	rclk_gpio_psel[1:0]
38	PAD_WDT_RST_N	wdt (I/O)	gpio (I/O)				wdt_gpio_psel[1:0]
39	PAD_EPHY_LED4_N	ephy_led4_n (O)	gpio (I/O)	w_utif_n[6] (I/O)	jtrstn_n (I)		p4_led_gpio_psel[2:0]
40	PAD_EPHY_LED3_N	ephy_led3_n (O)	gpio (I/O)	w_utif_n[7] (I/O)	jtclk_n (I)		p3_led_gpio_psel[2:0]
41	PAD_EPHY_LED2_N	ephy_led2_n (O)	gpio (I/O)	w_utif_n[8] (I/O)	jtms_n (I)		p2_led_gpio_psel[2:0]
42	PAD_EPHY_LED1_N	ephy_led1_n (O)	gpio (I/O)	w_utif_n[9] (I/O)	jtdi_n (I)		p1_led_gpio_psel[2:0]
43	PAD_EPHY_LED0_N	ephy_led0_n (O)	gpio (I/O)		jtdo_n (I/O)		p0_led_gpio_psel[2:0]
44	PAD_WLED_N	wled_n (I/O)	gpio (I/O)				wled_gpio_psel[2:0]
45	PAD_TXD1	txd1 (O)	gpio (I/O)	pwm_ch0 (O)	antsel[1] (O)	8	uart1_gpio_psel[2:0]
46	PAD_RXD1	rxd1 (I)	gpio (I/O)	pwm_ch1 (O)	antsel[0] (O)		uart1_gpio_psel[2:0]

UART1 pin share scheme

Controlled by the UART1_MODE register.

Pin Name	2'b00 UART-Lite #1	2'b01 GPIO	2'b10 PWM	2'b11 TRX_SW
UART1_RXD	UART1_RXD	GPIO#46	PWM_CH1	
UART1_TXD	UART1_TXD	GPIO#45	PWM_CH0	

MT7688AN EPHY LED pin share scheme

Controlled by the P#_LED_AN_MODE registers

Pin Name	Bootstrapping (DBG_JTAG_MODE=1)	Bootstrapping (DBG_JTAG_MODE=0)	
		P4_LED_AN_MODE =2'b00	P4_LED_AN_MODE =2'b01
EPHY_LED4_N_JTRST_N	JTAG_RST_N	EPHY_LED4_N	GPIO#39
		P3_LED_AN_MODE =2'b00	P3_LED_AN_MODE =2'b01
EPHY_LED3_N_JTCLK	JTAG_CLK	EPHY_LED3_N	GPIO#40
		P2_LED_AN_MODE =2'b00	P2_LED_AN_MODE =2'b01
EPHY_LED2_N_JTMS	JTAG_TMS	EPHY_LED2_N	GPIO#41
		P1_LED_AN_MODE =2'b00	P1_LED_AN_MODE =2'b01
EPHY_LED1_N_JTDI	JTAG_TDI	EPHY_LED1_N	GPIO#42
		P0_LED_AN_MODE =2'b00	P0_LED_AN_MODE =2'b01
EPHY_LED0_N_JTDO	JTAG_TDO	EPHY_LED0_N	GPIO#43

MT7688AN WLAN LED pin share scheme

Controlled by the WLED_AN_MODE registers

Pin Name	2'b00	2'b01
WLED_N	WLED_N	GPIO#44

PERST_N pin share scheme

Controlled by the PERST_ MODE register.

Pin Name	1'b0	1'b1
PERST_N	PERST_N	GPIO#36

WDT_RST_N pin share scheme

Controlled by the WDT _MODE register.

Pin Name	1'b0	1'b1
WDT_RST_N	WDT_RST_N	GPIO#37

REF_CLKO pin share scheme

Controlled by the REFCLK _MODE register.

Pin Name	1'b0	1'b1
REF_CLKO	REF_CLKO	GPIO#38

UART0 pin share scheme

Controlled by the UART0 _MODE register.

Pin Name	1'b0	1'b1
UART_TXD0	UART_TXD0	GPIO#12
UART_TXD0	UART_RXD0	GPIO#13

GPIO0 pin share scheme

Controlled by GPIO_MODE register.

Pin Name	2'b00	2'b01	2'b10	2'b11
GPIO0	GPIO#11	GPIO#11	REF_CLKO	PERST_N

SPI pin share scheme

Controlled by SPI_ MODE register.

Pin Name	1'b0	1'b1
SPI_CLK	SPI_CLK	GPO#7
SPI_MOSI	SPI_MOSI	GPO#8
SPI_MISO	SPI_MISO	GPIO#9
SPI_CS0	SPI_CS0	GPIO#10

SPI_CS1 pin share scheme

Controlled by SPI_CS1_MODE register.

Pin Name	2'b00	2'b01	2'b10
SPI_CS1	SPI_CS1	GPIO#6	REF_CLKO

I2C pin share scheme

Controlled by I2C_MODE register.

Pin Name	2'b00	2'b01
I2C_SCLK	I2C_SCLK	GPIO#4
I2C_SD	I2C_SD	GPIO#5

I2S pin share scheme

Controlled by I2S_MODE register.

Pin Name	2'b00	2'b01	2'b10
I2S_SDI	I2C_SCLK	GPIO#0	PCMDRX
I2S_SDO	I2C_SD	GPIO#1	PCMDTX
I2S_WS	I2C_SCLK	GPIO#2	PCMCLK
I2S_CLK	I2C_SD	GPIO#3	PCMFS

SD pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

Pin Name	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	SD_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	SD_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	SD_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	SD_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	SD_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	SD_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	SD_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	SD_D3	GPIO#29

eMMC pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SD_MODE registers

Pin Name	EPHY_APGIO_AIO_EN[4:1] =4'b0000	EPHY_APGIO_AIO_EN[4:1] =4'b1111	
		SD_MODE =2'b00	SD_MODE =2'b01
MDI_TP_P3	MDI_TP_P3	eMMC_WP	GPIO#22
MDI_TN_P3	MDI_TN_P3	eMMC_CD	GPIO#23
MDI_RP_P3	MDI_RP_P3	eMMC_D1	GPIO#24
MDI_RN_P3	MDI_RN_P3	eMMC_D0	GPIO#25
MDI_RP_P4	MDI_RP_P4	eMMC_CLK	GPIO#26
MDI_TN_P4	MDI_TN_P4	eMMC_D2	GPIO#27
MDI_RN_P4	MDI_RN_P4	eMMC_CMD	GPIO#28
MDI_TP_P4	MDI_TP_P4	eMMC_D3	GPIO#29

UART2 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and UART2_MODE registers

Pin Name	4'b0000	4'b1111			
		2'b00	2'b01	2'b10	2'b11
MDI_TP_P2	MDI_TP_P2	UART_TXD2	GPIO#20	PWM_CH2	eMMC_D5
MDI_TN_P2	MDI_TN_P2	UART_RXD2	GPIO#21	PWM_CH3	eMMC_D4

PWM_CH1 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM1_MODE registers

	4'b0000	4'b1111			
Pin Name		**2'b00**	**2'b01**	**2'b10**	**2'b11**
MDI_RN_P2	MDI_RN_P2	PWM_CH1	GPIO#19		eMMC_D6

PWM_CH0 pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and PWM0_MODE registers

	4'b0000	4'b1111			
Pin Name		**2'b00**	**2'b01**	**2'b10**	**2'b11**
MDI_RP_P2	MDI_RP_P2	PWM_CH0	GPIO#18		eMMC_D7

SPIS pin share scheme

Controlled by the EPHY_APGIO_AIO_EN[4:1] and SPIS_MODE registers

	4'b0000	4'b1111			
Pin Name		**2'b00**	**2'b01**	**2'b10**	**2'b11**
MDI_TP_P1	MDI_TP_P1	SPIS_CS	GPIO#14		PWM_CH0
MDI_TN_P1	MDI_TN_P1	SPIS_CLK	GPIO#15		PWM_CH1
MDI_RP_P1	MDI_RP_P1	SPIS_MISO	GPIO#16		UART_TXD2
MDI_RN_P1	MDI_RN_P1	SPIS_MOSI	GPIO#17		UART_RXD2

Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7688AN only. It needs to be pull-low for 7688KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

7 MODULE OTHER CONTENT

7.1 RF hardware performance

7.1.1 Oolite V3.2D

Item	type	real target
Antenna 0	Frequency error	-5.0ppm
	power	CCK 11M 18.0dbm OFDM 54M 16.0dbm MCS7(HT20) 16.0dbm MCS7(HT40) 15.0dbm
	EVM	CCK 11M -18.0db OFDM 54M -25.0db MCS7(HT20) -27.0db MCS7(HT40) -28db
	Reception Sensitivity	CCK 11M -85dbm OFDM 54M -63dbm MCS7(HT20) -61dbm MCS7(HT40) -59dbm

Item	type	real target
	Frequency error	-5.0ppm
	power	CCK 11M 18.0dbm OFDM 54M 16.0dbm MCS7(HT20) 16.0dbm MCS7(HT40) 15.0dbm

Antenna 1	EVM	CCK 11M 26.0db OFDM 54M -25.0db MCS7(HT20) -27.0db MCS7(HT40) -28db
	Reception Sensitivity	CCK 11M -85dbm OFDM 54M -63dbm MCS7(HT20) -61dbm MCS7(HT40) -59dbm

7.1.2 Oolite V3.2S

Item	type	real target
Antenna 0	Frequency error	-5.0ppm
	power	CCK 11M 18.0dbm OFDM 54M 16.0dbm MCS7(HT20) 16.0dbm MCS7(HT40) 15.0dbm
	EVM	CCK 11M -18.0db OFDM 54M -25.0db MCS7(HT20) -27.0db MCS7(HT40) -28db
	Reception Sensitivity	CCK 11M -85dbm OFDM 54M -63dbm MCS7(HT20) -61dbm MCS7(HT40) -59dbm

7.2 Installed matters needing attention

a. In the opening of the steel mesh, the module of the pad hole in a ratio of 1:1 to expand 0.7mm and thickness of 0.12 mm.

b. Putting the module to the oven at 120 ℃ (±5℃) baking for 12 hours, and then on the basis of how much per hour can stick taking out the corresponding number of modules.

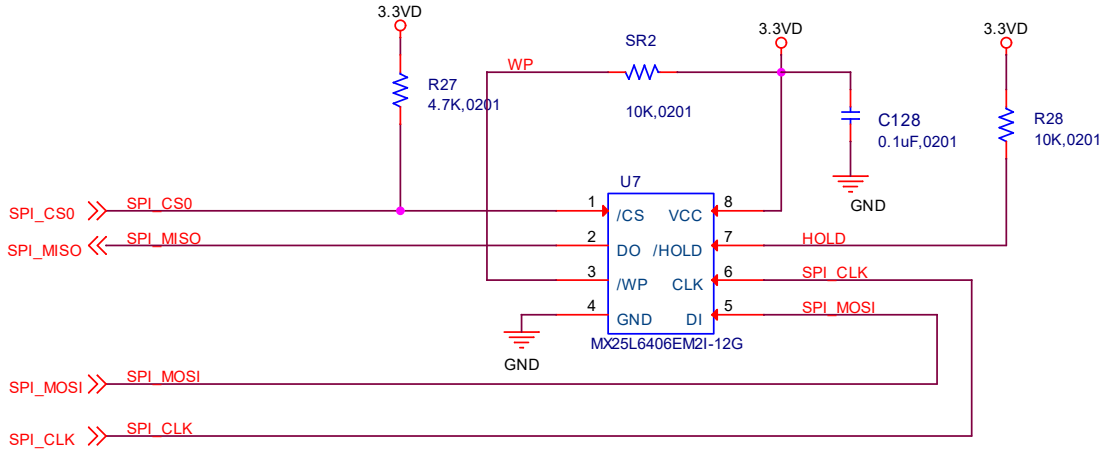
c. Bring gloves and electrostatic ring to get the module.

d. The furnace temperature on the basis of main board size .

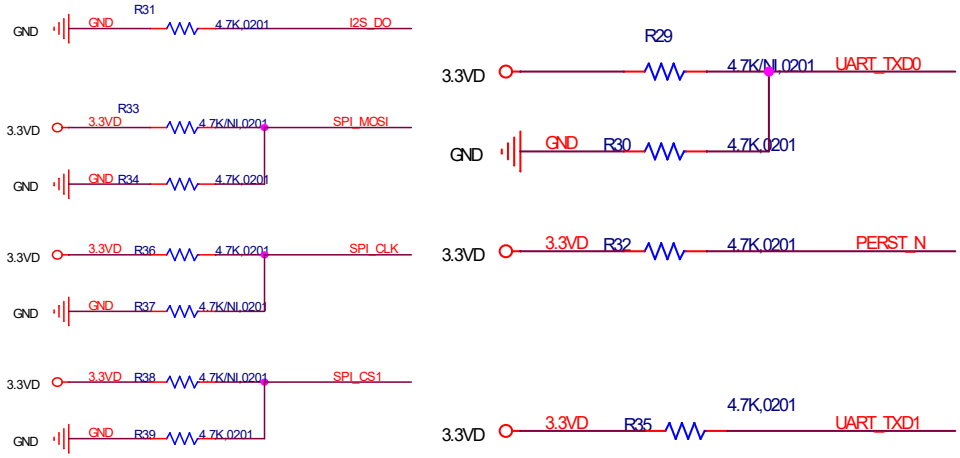
8 ENCLOSURE

Oolite V3.2D and Oolite V3.2S are the same

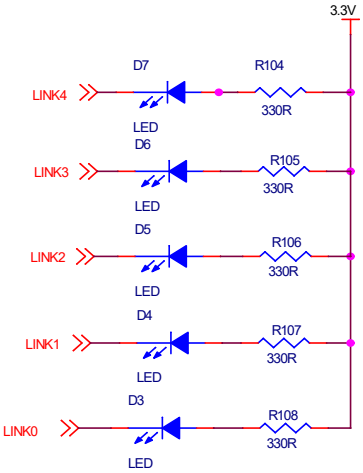
(1) SPI Flash Schematic



(2) Bootstrap CONFIG Schematic



(3) External mode of module



(4) Net port connection