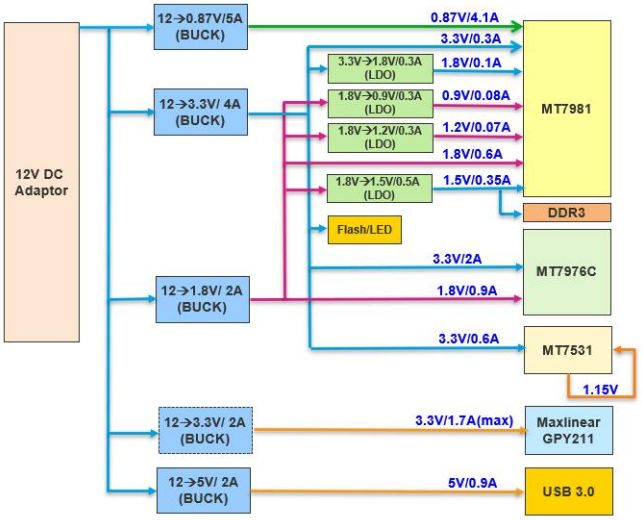
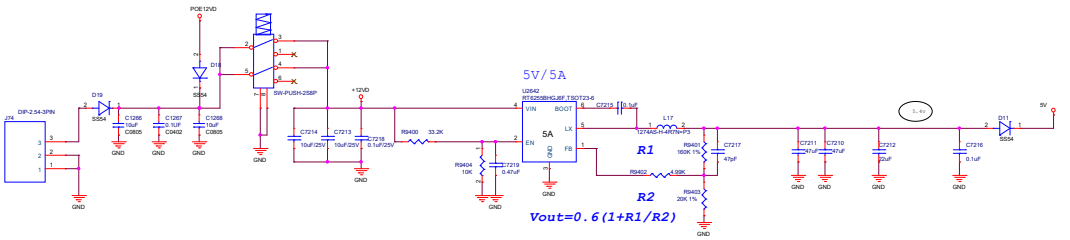
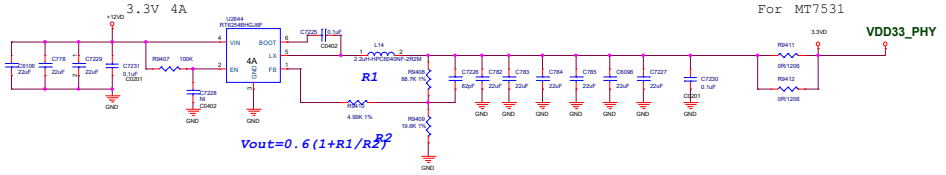
Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4
GPIO_WPS	B:GPIO0		I0:WA_AICE_TCKC	I0:WM_AICE_TCKC	
GPIO_RESET	B:GPIO1		B0:WA_AICE_TMSC	B0:WM_AICE_TMSC	
SYS_WATCHDOG	B:GPIO2	O:SYS_WATCHDOG			
PCIE_PERESET_N	B:GPIO3	O:PCIE_PERESET_N			
JTAG_JTDO	B:GPIO4	O:JTAG_JTDO	O:WM_JTAG_JTDO	I1:UART2_RXD	I0:PTA_EXT_ACT
JTAG_JTDI	B:GPIO5	I1:JTAG_JTDI	I1:WM_JTAG_JTDI	O:UART2_TXD	I0:PTA_EXT_PRI
JTAG_JTMS	B:GPIO6	B1:JTAG_JTMS	I1:WM_JTAG_JTMS	I1:UART2_CTS	O:PTA_EXT_WLAN_ACT
JTAG_JTCLK	B:GPIO7	I1:JTAG_JTCLK	I1:WM_JTAG_JTCLK	O:UART2_RTS	O:PWM2
JTAG_JTRST_N	B:GPIO8	I0:JTAG_JTRST_N	I0:WM_JTAG_JTRST_N	O:GBE_LED0	O:NET_WO0_UART_TXD
WO_JTAG_JTDO	B:GPIO9	O:WO0_JTAG_JTDO	I0:WM_AICE_TCKC		O:PCM_DTX
WO_JTAG_JTDI	B:GPIO10	I1:WO0_JTAG_JTDI	B0:WM_AICE_TMSC		I0:PCM_DRX
WO_JTAG_JTMS	B:GPIO11	B1:WO0_JTAG_JTMS			O:PCM_CLK
WO_JTAG_JTCLK	B:GPIO12	I1:WO0_JTAG_JTCLK			O:PCM_FS
WO_JTAG_JTRST_N	B:GPIO13	I0:WO0_JTAG_JTRST_N	O:PWM0	O:GBE_LED1	O:PCM_MCK
USB_VBUS	B:GPIO14	O:DRV_VBUS	O:PWM1	O:NET_WO0_UART_TXD	
PWM0	B:GPIO15	O:PWM0	O:EMMC_RSTB	O:PWM1	O:NET_WO0_UART_TXD
SPI0_CLK	B:GPIO16	O:SPI0_CLK	B1:EMMC_DAT0	O:SNFI_CLK	I1:UART1_RXD
SPI0_MOSI	B:GPIO17	B0:SPI0_MOSI	B1:EMMC_DAT1	B0:SNFI_MOSI	O:UART1_TXD
SPI0_MISO	B:GPIO18	B0:SPI0_MISO	B1:EMMC_DAT2	B0:SNFI_MISO	I1:UART1_CTS
SPI0_CS	B:GPIO19	O:SPI0_CS	B1:EMMC_DAT3	O:SNFI_CS	O:UART1_RTS
SPI0_HOLD	B:GPIO20	B0:SPI0_HOLD	B1:EMMC_DAT4	B0:SNFI_HOLD	O:WM_UART_TXD
SPI0_WP	B:GPIO21	B0:SPI0_WP	B1:EMMC_DAT5	B0:SNFI_WP	O:WA_UART_TXD
SPI1_CLK	B:GPIO22	O:SPI1_CLK	B1:EMMC_DAT6	I1:UART2_RXD	I0:PTA_EXT_ACT
SPI1_MOSI	B:GPIO23	O:SPI1_MOSI	B1:EMMC_DAT7	O:UART2_TXD	I0:PTA_EXT_PRI
SPI1_MISO	B:GPIO24	I0:SPI1_MISO	B1:EMMC_CMD	I1:UART2_CTS	O:PTA_EXT_WLAN_ACT
SPI1_CS	B:GPIO25	O:SPI1_CS	B1:EMMC_CLK	O:UART2_RTS	O:PCM_MCK
SPI2_CLK	B:GPIO26	O:SPI2_CLK	I1:UART1_RXD		
SPI2_MOSI	B:GPIO27	B0:SPI2_MOSI	O:UART1_TXD		
SPI2_MISO	B:GPIO28	B0:SPI2_MISO	I1:UART1_CTS	I0:WA_AICE_TCKC	
SPI2_CS	B:GPIO29	O:SPI2_CS	O:UART1_RTS	B0:WA_AICE_TMSC	
SPI2_HOLD	B:GPIO30	B0:SPI2_HOLD	O:WF2G_LED	O:WM_UART_TXD	B1:I2C_SCL
SPI2_WP	B:GPIO31	B0:SPI2_WP	O:WF5G_LED	O:WA_UART_TXD	B1:I2C_SDA
UART0_RXD	B:GPIO32	I1:UART0_RXD	B1:SGMII1_PHY_I2C_SCL	B1:U3_PHY_I2C_SCL	
UART0_TXD	B:GPIO33	O:UART0_TXD	B1:SGMII1_PHY_I2C_SDA	B1:U3_PHY_I2C_SDA	
WF2G_LED	B:GPIO34	O:WF2G_LED	B1:PCIE_CLK_REQ		
WF5G_LED	B:GPIO35	O:WF5G_LED	I1:PCIE_WAKE_N		
SMI_MDC	B:GPIO36	O:SMI_MDC	B1:I2C_SCL	I1:GBE_EXT_MDC	
SMI_MDIO	B:GPIO37	B0:SMI_MDIO	B1:I2C_SDA	B1:GBE_EXT_MDIO	
GBE_INT	B:GPIO38	I0:MT7531_INT			
GBE_RESET	B:GPIO39				
WF_DIG_RESETB	B:GPIO40	O:WF0_DIG_RESETB			
WF_CBA_RESETB	B:GPIO41	O:WF0_CBA_RESETB			
WF_XO_REQ	B:GPIO42	O:WF0_XO_REQ			
WF_TOP_CLK	B:GPIO43	O:WF0_TOP_CLK			
WF_TOP_DATA	B:GPIO44	B0:WF0_TOP_DATA			
WF_HB1	B:GPIO45	B0:WF_HB1	O:WF0_MODE_SEL_1		
WF_HB2	B:GPIO46	B0:WF_HB2	O:WF0_MODE_SEL_2		
WF_HB3	B:GPIO47	B0:WF_HB3	O:WF0_XTAL_SEL_0		
WF_HB4	B:GPIO48	B0:WF_HB4	O:WF0_XTAL_SEL_1		
WF_HB0	B:GPIO49	O:WF_O_HB0	O:WF0_MODE_SEL_0		
WF_HB0_B	B:GPIO50	O:WF_O_HB0_B			
WF_HB5	B:GPIO51	B0:WF_HB5	O:WF0_XTAL_SEL_2		
WF_HB6	B:GPIO52	B0:WF_HB6			
WF_HB7	B:GPIO53	B0:WF_HB7			
WF_HB8	B:GPIO54	B0:WF_HB8			
WF_HB9	B:GPIO55	B0:WF_HB9			
WF_HB10	B:GPIO56	B0:WF_HB10			

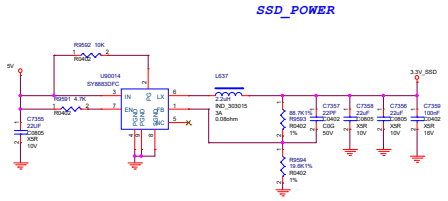
GAINSTRONG	Title: OOLITE7981V_DEV_1.0		
	Document Number: P05 Ethernet-GPIO_LED		
Size: A2	Design By: <Designer>	Review By: <Reviewer>	Rev: V1.0.2
Date: Tuesday, June 27, 2023		Sheet 1 of 12	

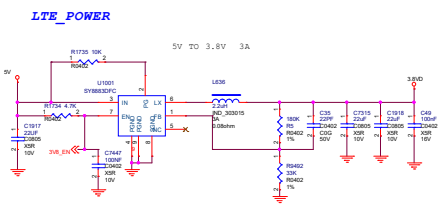


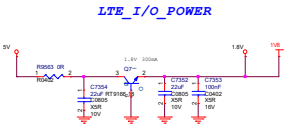
GAINSTRONG	Title: OOLITE7981V_DEV_1.0		
	Document Number: P05 Ethernet-GPIO_LED		
Size: A3	Design By: <Designer>	Review By: <Reviewer>	Rev: V1.0.2
Date: Tuesday, June 27, 2023	Sheet 2 of 12		











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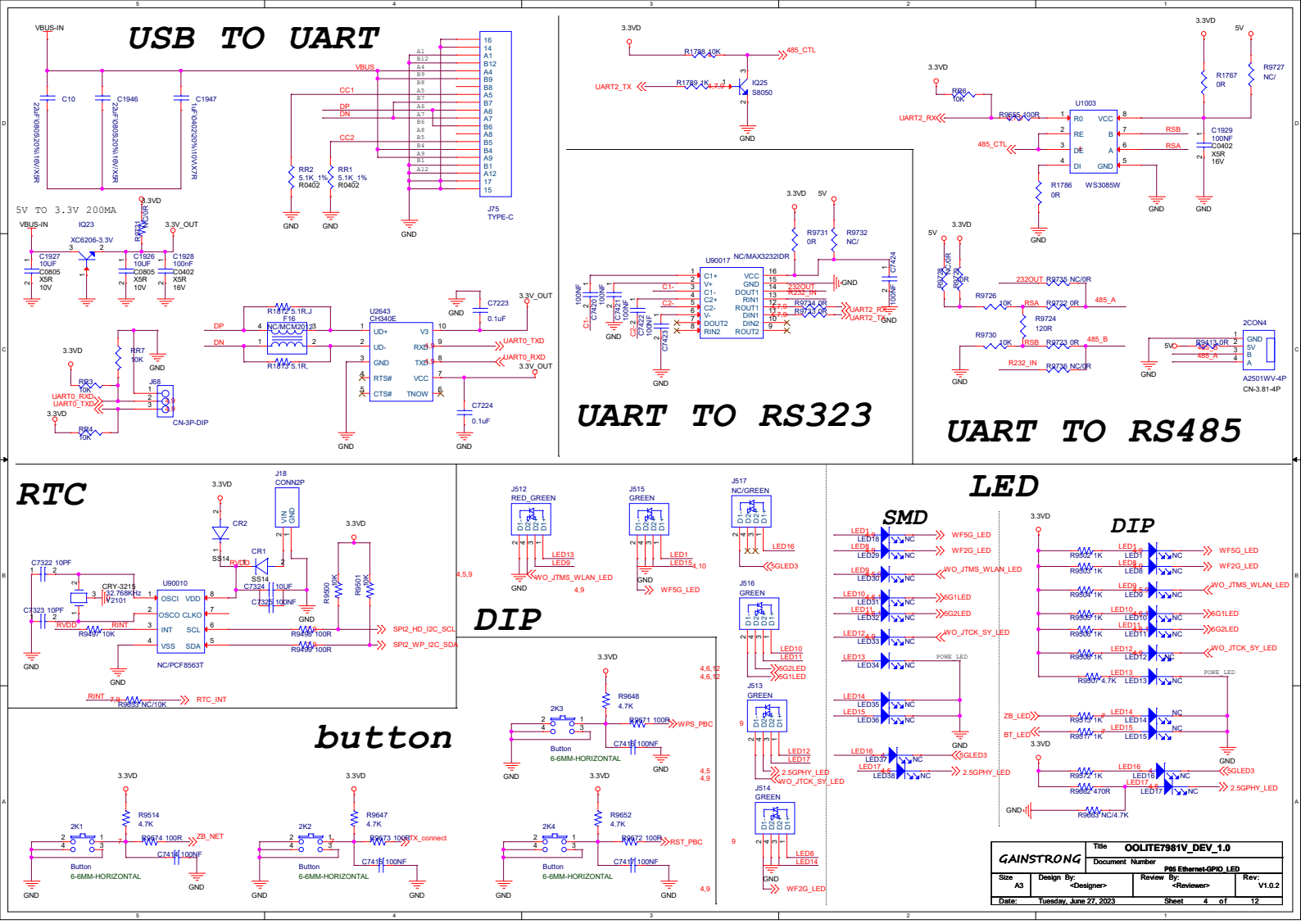
	Document Number: P05 Ethernet-GPIO_LED		
Size: A2	Design By: <Designer>	Review By: <Reviewer>	Rev: V1.0.2
Date: Tuesday, June 27, 2023	Sheet 3 of 12		



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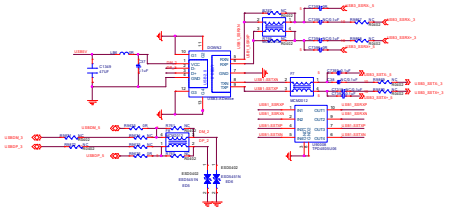
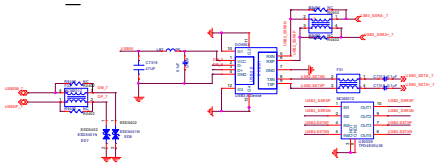
	Document Number: P0S Ethernet-GPIO_LED		
Size: A3	Design By: <Designer>	Review By: <Reviewer>	Rev: V1.0.2
Date: Tuesday, June 27, 2023	Sheet 4 of 12		

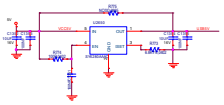
USB_CONNECTOR



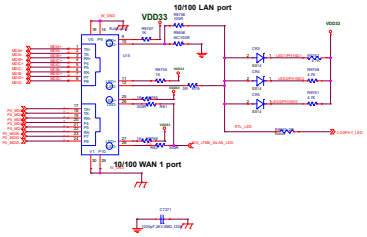
USB_CONNECTOR



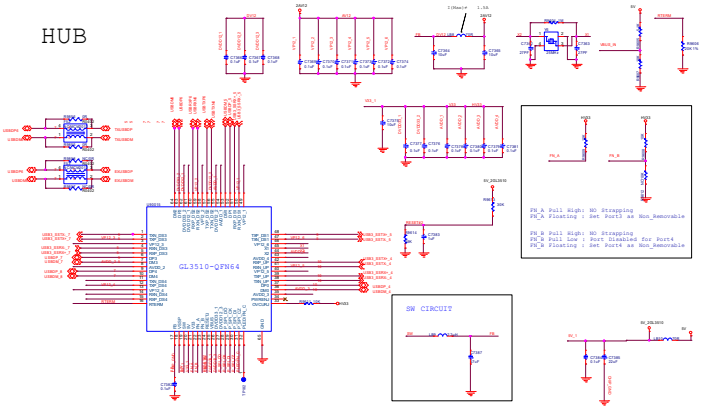
USB_POWER

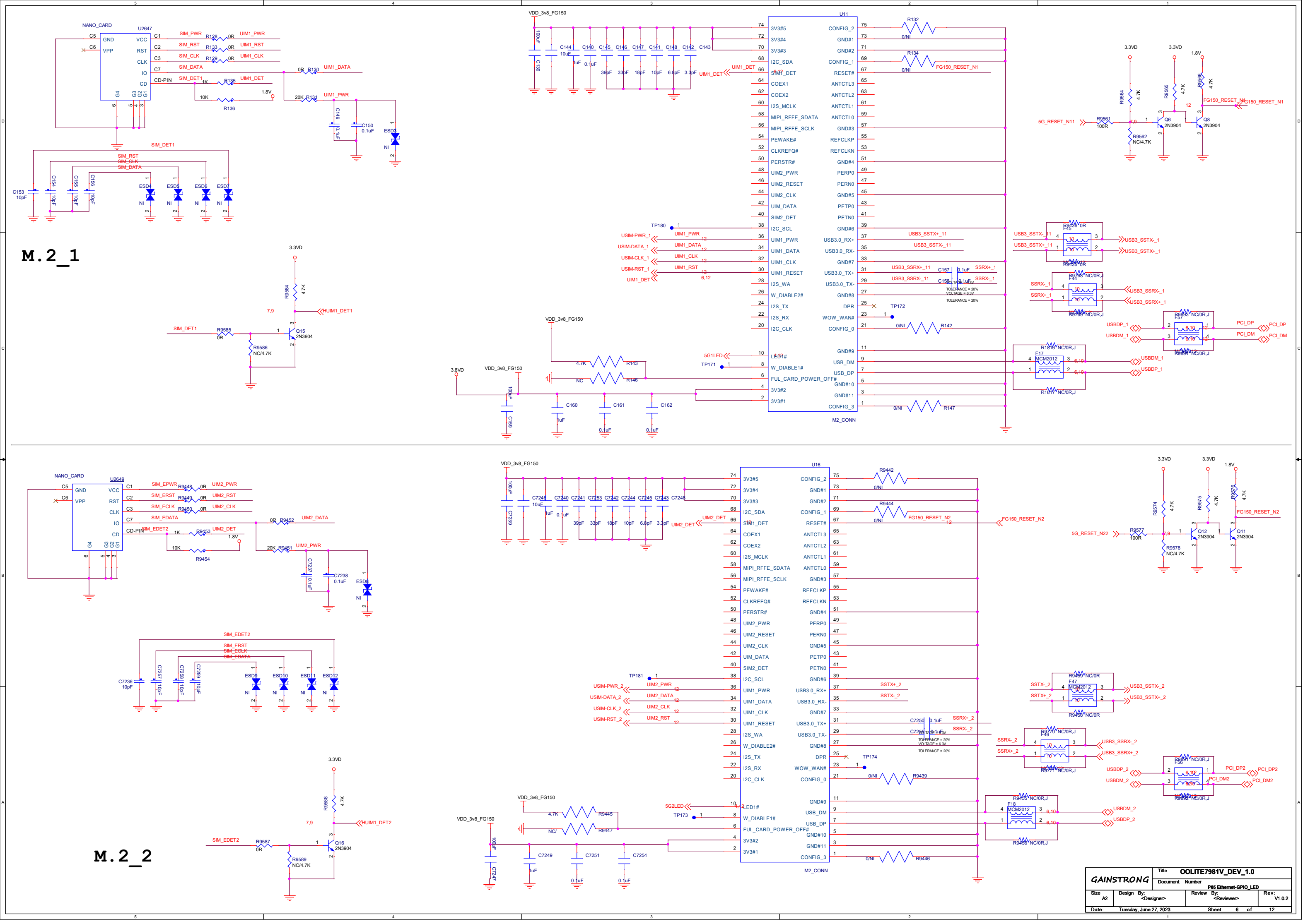


RJ45

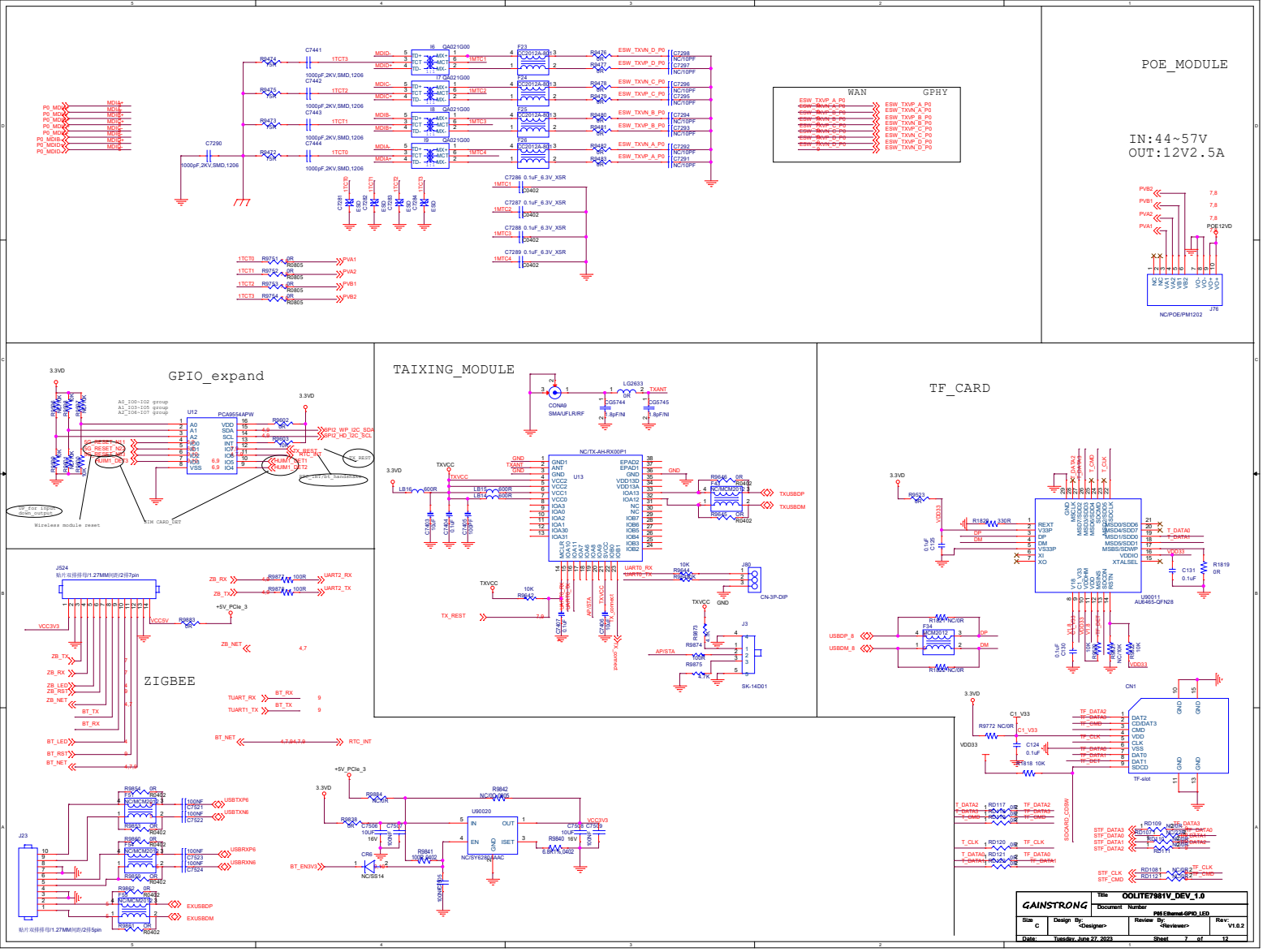


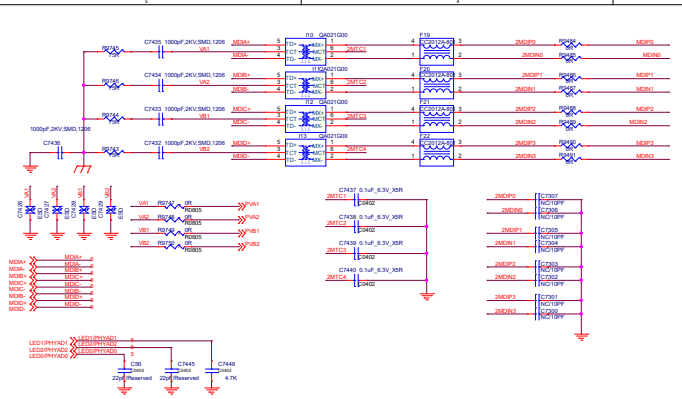
HUB

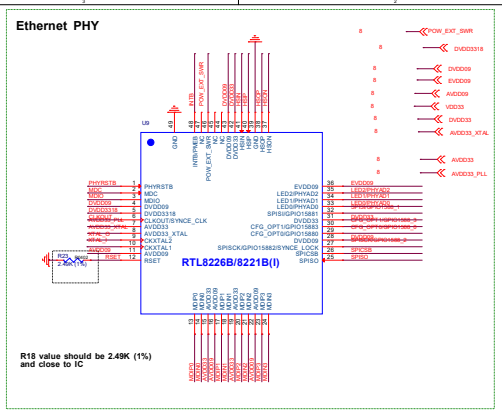


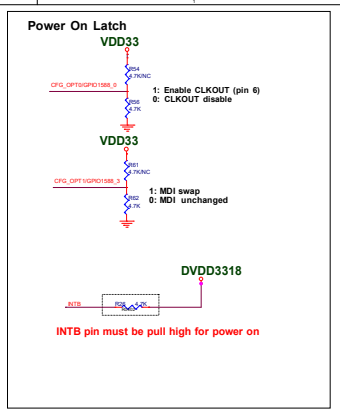


M.2_1
M.2_2
NANO_CARD
U2647
GND
VCC
VPP
RST
CLK
IO
CD
CD-PIN
SIM_PWR
SIM_RST
SIM_CLK
SIM_DATA
SIM_DET1
UIM1_PWR
UIM1_RST
UIM1_CLK
UIM1_DATA
UIM1_DET
SIM_RST
SIM_CLK
SIM_DATA
VDD_3v8_FG150
U11
3V3#5
3V3#4
3V3#3
I2C_SDA
SIM_DET
COEX1
COEX2
I2S_MCLK
MIPI_RFFE_SDATA
MIPI_RFFE_SCLK
PEWAKE#
CLKREFQ#
PERSTR#
UIM2_PWR
UIM2_RESET
UIM2_CLK
UIM_DATA
SIM2_DET
I2C_SCL
UIM1_PWR
UIM1_DATA
UIM1_CLK
UIM1_RESET
I2S_WA
W_DIABLE2#
I2S_TX
I2S_RX
I2C_CLK
LED1#
W_DIABLE1#
FUL_CARD_POWER_OFF#
3V3#2
3V3#1
CONFIG_2
CONFIG_1
RESET#
ANTCTL3
ANTCTL2
ANTCTL1
ANTCTL0
REFCLKP
REFCLKN
PERP0
PERN0
PETP0
PETN0
USB3.0_RX+
USB3.0_RX-
USB3.0_TX+
USB3.0_TX-
DPR
WOW_WAN#
CONFIG_0
USB_DM
USB_DP
CONFIG_3
M2_CONN
FG150_RESET_N1
USB3_SSTX+_11
USB3_SSTX-_11
USB3_SSRX+_11
USB3_SSRX-_11
USB3_SSTX-_1
USB3_SSTX+_1
USB3_SSRX-_1
USB3_SSRX+_1
USBDP_1
USBDM_1
PCI_DP
PCI_DM
MCM2012
5G_RESET_N11
2N3904
HUIM1_DET1
SIM_DET1
3.3VD
1.8V
U16
U2649
SIM_EPWR
SIM_ERST
SIM_ECLK
SIM_EDATA
SIM_EDET2
UIM2_PWR
UIM2_RST
UIM2_CLK
UIM2_DATA
UIM2_DET
FG150_RESET_N2
5G_RESET_N22
USB3_SSTX-_2
USB3_SSTX+_2
USB3_SSRX-_2
USB3_SSRX+_2
USBDM_2
USBDP_2
PCI_DP2
PCI_DM2
HUIM1_DET2
5G1LED
5G2LED
GAINSTRONG
Title OOLITE7981V_DEV_1.0
Document Number P05 Ethernet-GPIO_LED
Size A2
Design By: <Designer>
Review By: <Reviewer>
Rev: V1.0.2
Date: Tuesday, June 27, 2023
Sheet 6 of 12

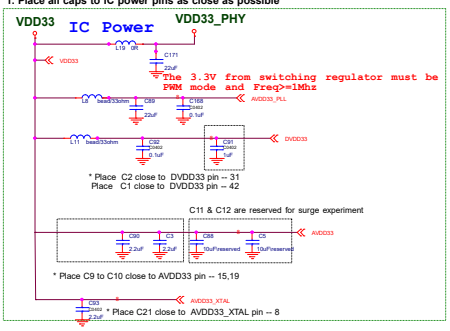

POE_MODULE
IN:44~57V
OUT:12V2.5A
WAN
GPHY
GPIO_expand
TAIXING_MODULE
TF_CARD
ZIGBEE
GAINSTRONG
GOLITE7981V_DEV_1.0
P85 Ethernet-GPIO_LED
Tuesday, June 27, 2023
V1.0.2

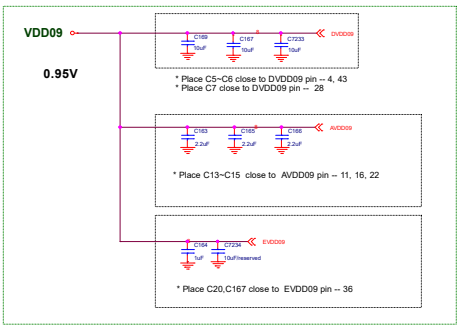


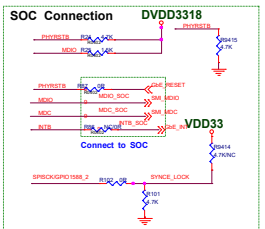




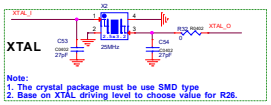
1. Place all caps to IC power pins as close as possible

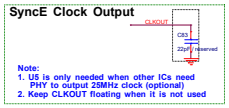


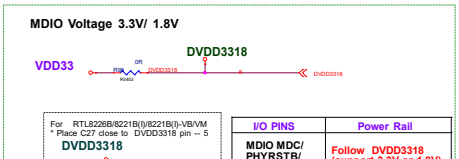


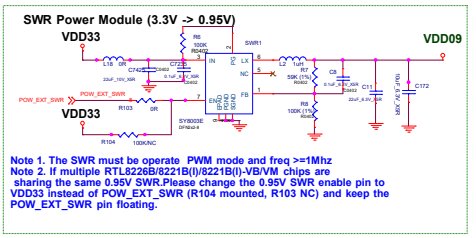


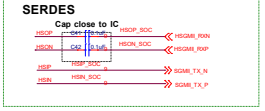
PHY Address=0x1
LED Polarity will be set based on latched PHYAD.
C36,C39 and C41 reserved for EMI (optional)

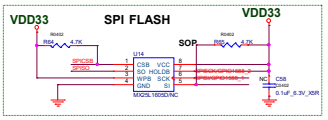


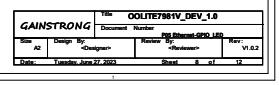




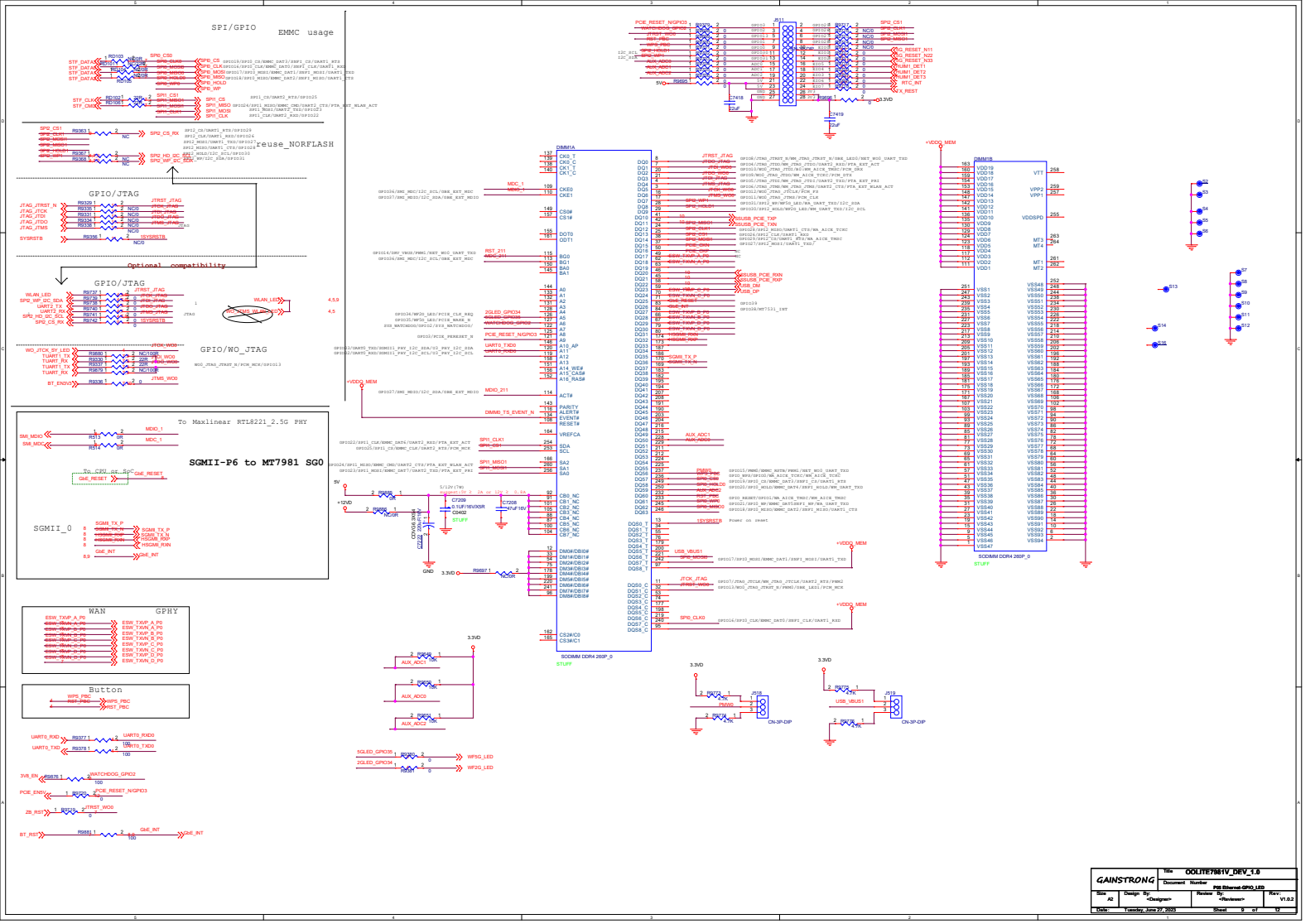


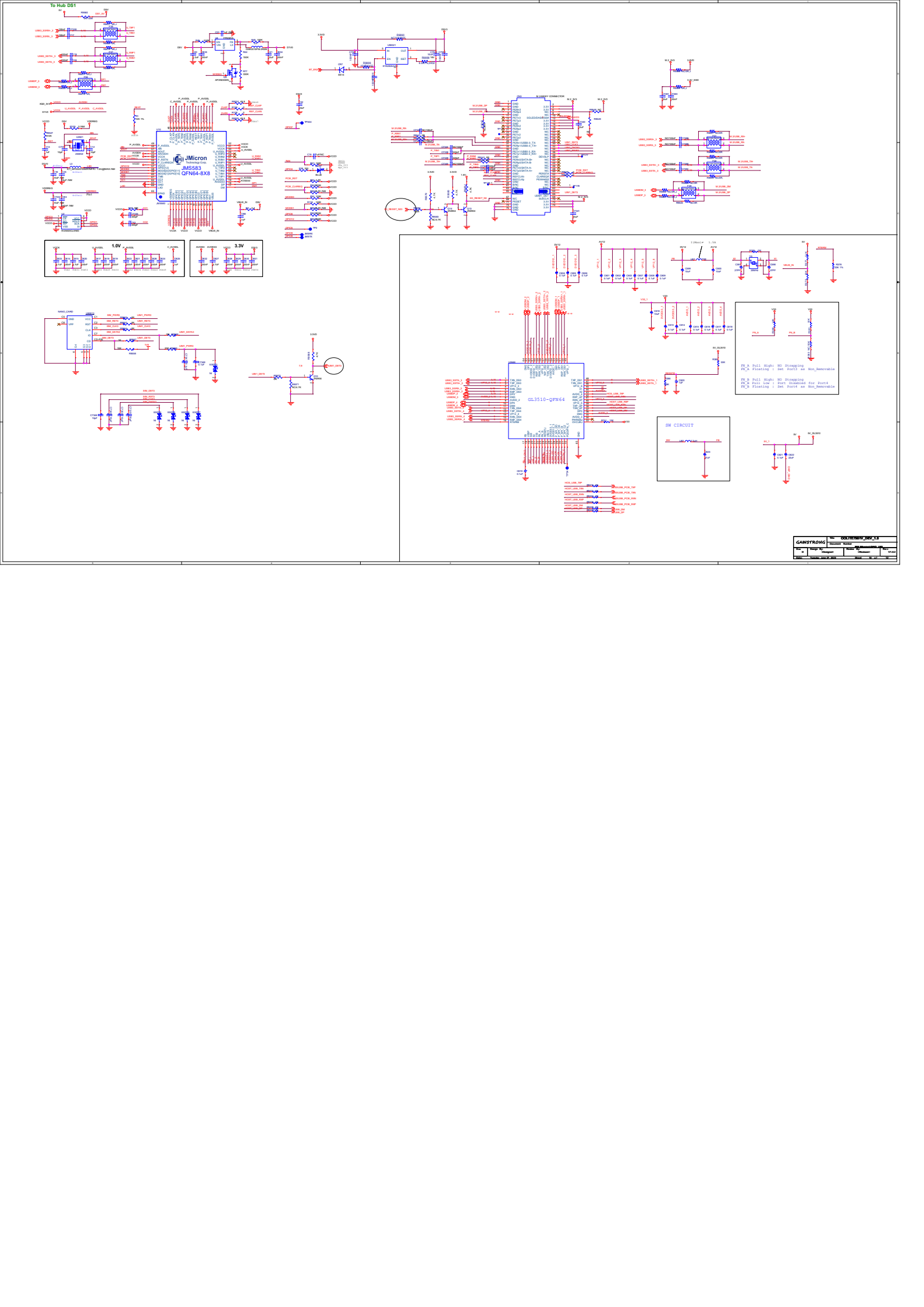




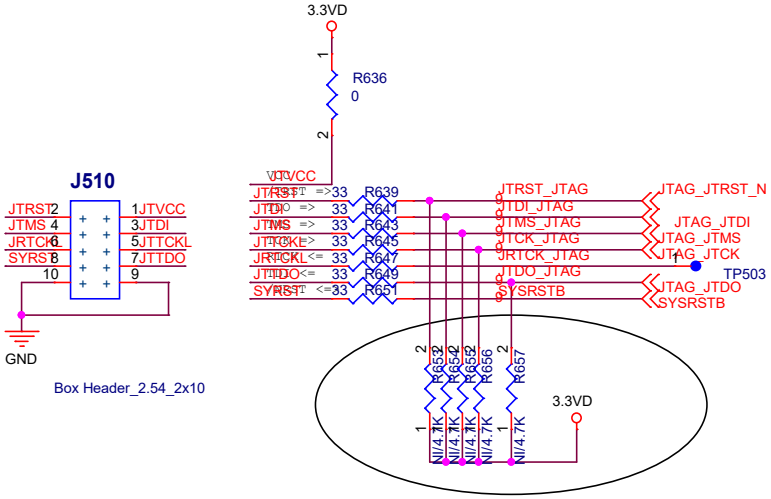


SyncE CLK will be high Z when CKLOUT is disabled.
Thus SyncE lock should be PD to prevent miss use of this CLK.

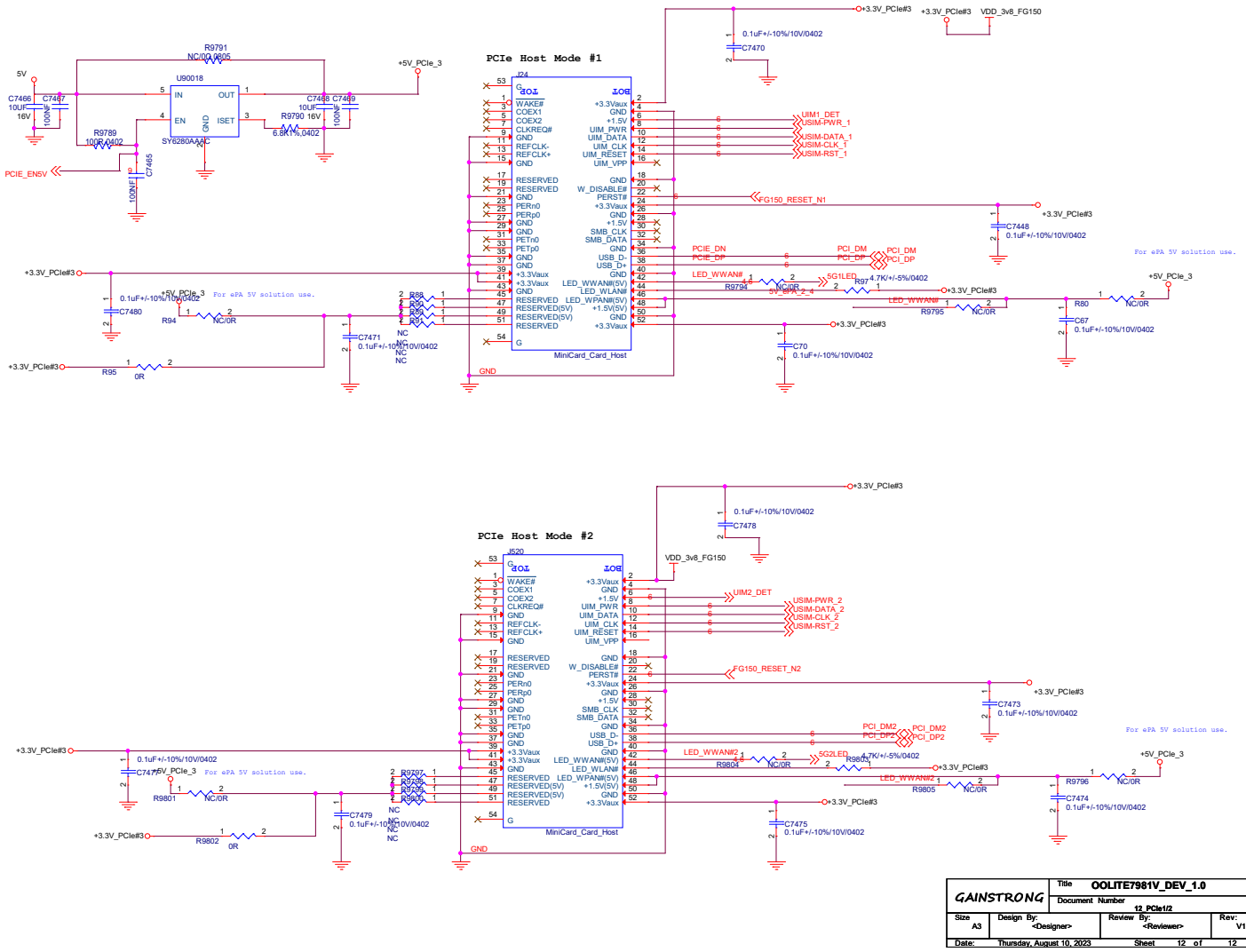

SPI/GPIO
EMMC usage
reuse_NORFLASH
GPIO/JTAG
Optional compatibility
GPIO/JTAG
GPIO/WO_JTAG
SGMII-P6 to MT7981 SG0
To Maxlinear RTL8221_2.5G PHY
To CPU or SoC
SGMII_0
WAN
GPHY
Button
DIMM1A
DIMM1B
SCOMM DDR4 260P_0
SCOMM DDR4 260P_0
STUFF
STUFF


To Hub DS1
JMicron
Technology Corp.
JMS583
QFN64-8X8
1.0V
3.3V
GL3510-QFN64
SW CIRCUIT
GAMSTRONG
GOLITE760V_DEV_1.0
Tuesday, June 27, 2023
V1.0.0

default- JTAG_CA53
sw config for WM0



GAINSTRONG	Title: OOLITE7981V_DEV_1.0		
	Document Number: P05 Ethernet-GPIO_LED		
Size: A	Design By: <Designer>	Review By: <Reviewer>	Rev: V1.0.2
Date: Tuesday, June 27, 2023		Sheet 11 of 12	


PCIe Host Mode #1
U90018
SY6280AAAC
MiniCard_Card_Host
+5V_PCIe_3
+3.3V_PCIe#3
VDD_3v8_FG150
PCIE_EN5V
UIM1_DET
USIM-PWR_1
USIM-DATA_1
USIM-CLK_1
USIM-RST_1
FG150_RESET_N1
PCIE_DN
PCIE_DP
PCI_DM
PCI_DP
LED_WWAN#
5G1LED
4.7K/+/-5%/0402
For ePA 5V solution use.
PCIe Host Mode #2
MiniCard_Card_Host
UIM2_DET
USIM-PWR_2
USIM-DATA_2
USIM-CLK_2
USIM-RST_2
FG150_RESET_N2
PCI_DM2
PCI_DP2
LED_WWAN#2
5G2LED
4.7K/+/-5%/0402
For ePA 5V solution use.
GAINSTRONG
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