

Design mealy sequence detector to detect a sequence ----1010---- using D filpflop and logic



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Pooja Joshi • 1.7k



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- A sequence detector is a sequential state machine. In a Mealy machine, output depends on the present state and the external input (x). Hence in the diagram, the output is written outside the states, along with inputs. The state diagram of a Mealy machine for a 1010 detector is:

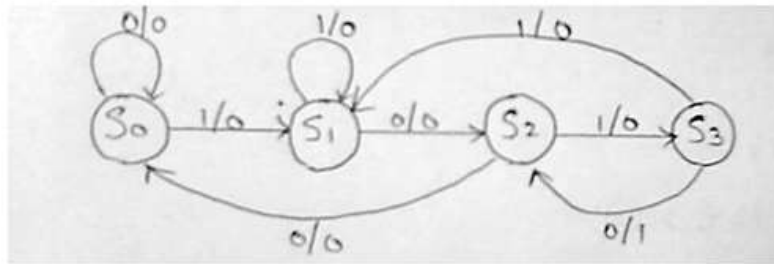


Fig14. State diagram for 1010 detector

- The state table for the above diagram:

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
S ₀	S ₀	S ₁	0	0
S ₁	S ₂	S ₁	0	0
S ₂	S ₀	S ₃	0	0
S ₃	S ₂	S ₁	1	1

Fig15. State table for above state diagram

- State assignments: Let $S_0 = 00$

$$S_1 = 01$$

$$S_2 = 10$$

$$S_3 = 11$$

The above state table becomes:

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
00	00	01	0	0
01	10	01	0	0
10	00	11	0	0
11	10	11	1	0

Fig16. State table with state assignments

- Four states will require two flip flops. Consider two D flip flops. Their excitation table is shown below.
- Excitation table:

Present State		Input	Next State		F/F Inputs		Output
A	B	X	A ⁺	B ⁺	D ₁	D ₂	Z
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	0
1	1	0	1	0	1	0	1
1	1	1	1	1	1	1	0

Fig17. Excitation table

- K-maps to determine inputs to D Flip flop:

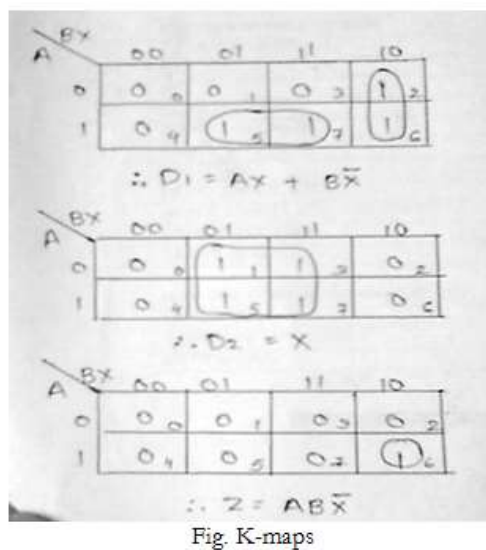
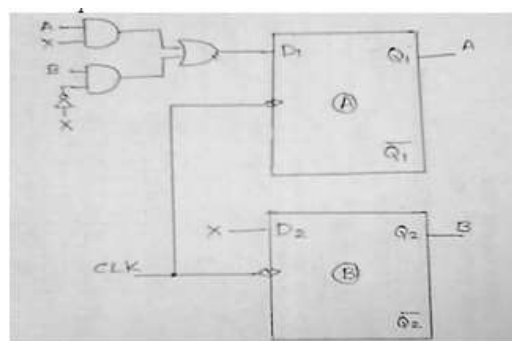


Fig. K-maps

- Circuit diagram for the sequence detector:



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if i design it using 5 states, is the method wrong in case of mealy FSM?

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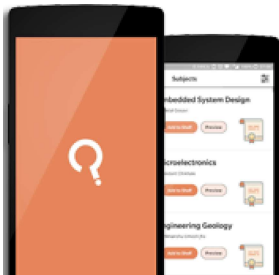
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