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EVD17I003

End Sem Project : 3 Bit Vedic Multiplier

Objective :

VLSI design & FPGA Implementation of "Design a Vedic Multiplier Architectures using HDL".

Theory :

Rapidly evolving technology has increased demand for real-time digital signal processing applications that are both fast and effective. Any application requires multiplication as one of the primary arithmetic operations. To improve their speed, a large number of multiplier designs have been produced. Vedic Multipliers have emerged as one of the quickest and low-power multipliers as a result of decades of study

The output and throughput of applications are determined by multipliers, which are main components of Arithmetic and logic units, Digital signal processing blocks, and Multiplier and accumulate units. The Vedic Multiplier has grown in popularity as a more efficient method of computation and analysis.

They've found a lot of use in image processing applications to save time and space. Image processing is the method of extracting useful information from images or enhancing a specific feature in them by performing operations on them such as image sharpening, pattern recognition, edge detection, and so on. As a result, it's critical in mapping, holography, x-ray imaging, and medical image processing.

Similarly, high-speed, low-area Vedic Multipliers are replacing widely used traditional multipliers in Digital Signal Processing. Their significance in the Semiconductor industry, which requires Digital Signal Processors for wireless communication, audio and video processing, industrial control, and portable electronics, could not have been greater.

Code :

Main Module

```
module vedic3bit(A,B,mul);
input [2:0]A,B;
output [5:0]mul;
wire [1:0]temp1,temp3;
wire [2:0]temp2;
wire [4:0]carry;
wire a,b;

//Stage 1(multiplication)
assign mul[0]=(A[0]&B[0]);

//Stage 2(multiplication)
assign temp1[0]=(A[0]&B[1]);
assign temp1[1]=(A[1]&B[0]);

//Stage 3(multiplication)
assign temp2[0]=(A[2]&B[0]);
assign temp2[1]=(A[0]&B[2]);
assign temp2[2]=(A[1]&B[1]);

//Stage 4(multiplication)
assign temp3[0]=(A[2]&B[1]);
assign temp3[1]=(A[1]&B[2]);

//Stage 5(multiplication)
assign a=(A[2]&B[2]);

//Addition of Stages(FINAL ADDITION STAGE)
halfadder P0(temp1[0],temp1[1],mul[1],carry[0]); //2bit add
fulladder P1(temp2[0],temp2[1],carry[0],b,carry[1]); // 3bit add
fulladder P2(temp2[2],b,carry[1],mul[2],carry[2]); //3bit add
fulladder P3(temp3[0],temp3[1],carry[2],mul[3],carry[3]); //3bit add
halfadder P4(a,carry[3],mul[4],carry[4]);  //2bit add
assign mul[5]=carry[4];//final sum bit calculation

endmodule
```

Half Adder Module

```
module halfadder(c,d,sum,carry);
input c,d;
output sum,carry;
xor x1(sum,c,d);
```

```
and a1(carry,c,d);
endmodule
```

Full Adder Module

```
module fulladder(a,b,c,sum,carry);
input a,b,c;
output sum,carry;
wire w1;
wire w2;
wire w3;
xor x1(w1,a,b);
xor x2(sum,w1,c);
and a1(w2,w1,c);
and a2(w3,a,b);
or o1(carry,w2,w3);
endmodule
```

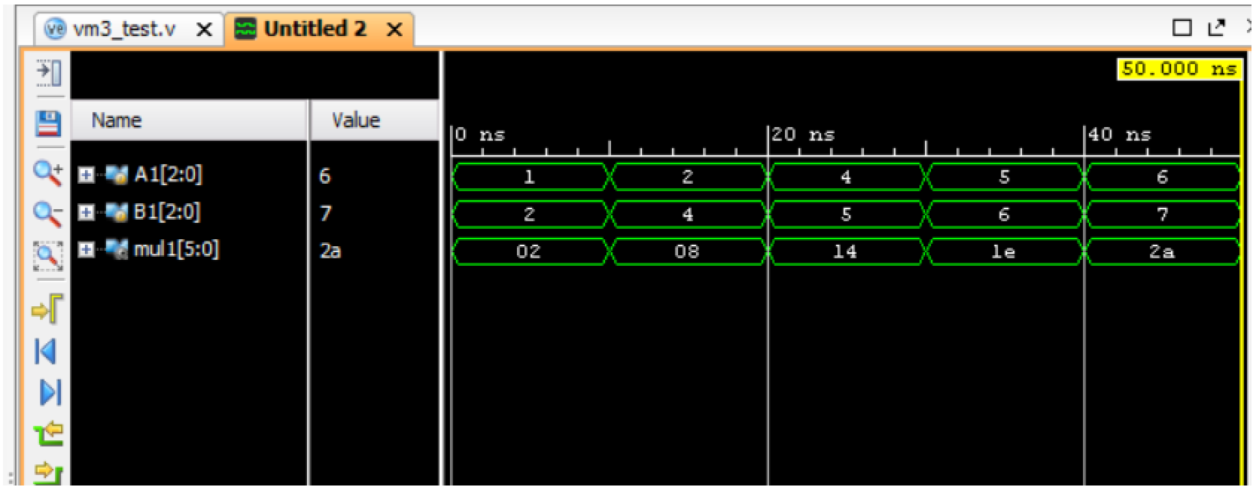
Test Bench

```
`include"ff.v"
`include"hf.v"
`timescale 10ns/1ns //timescale defined
module tb_vedic3bit();
reg [2:0]A1,B1; //ports declared
wire [5:0]mul1;

vedic3bit M(A1,B1,mul1);// module instantiation
initial
begin
$dumpfile("vedic3bit_test.vcd");
$dumpvars(0,tb_vedic3bit);
end

initial //various test inputs
begin
   A1=3'b001;
   B1=3'b010;

   #1 A1=3'b010;
      B1=3'b100;

   #1 A1=3'b100;
```

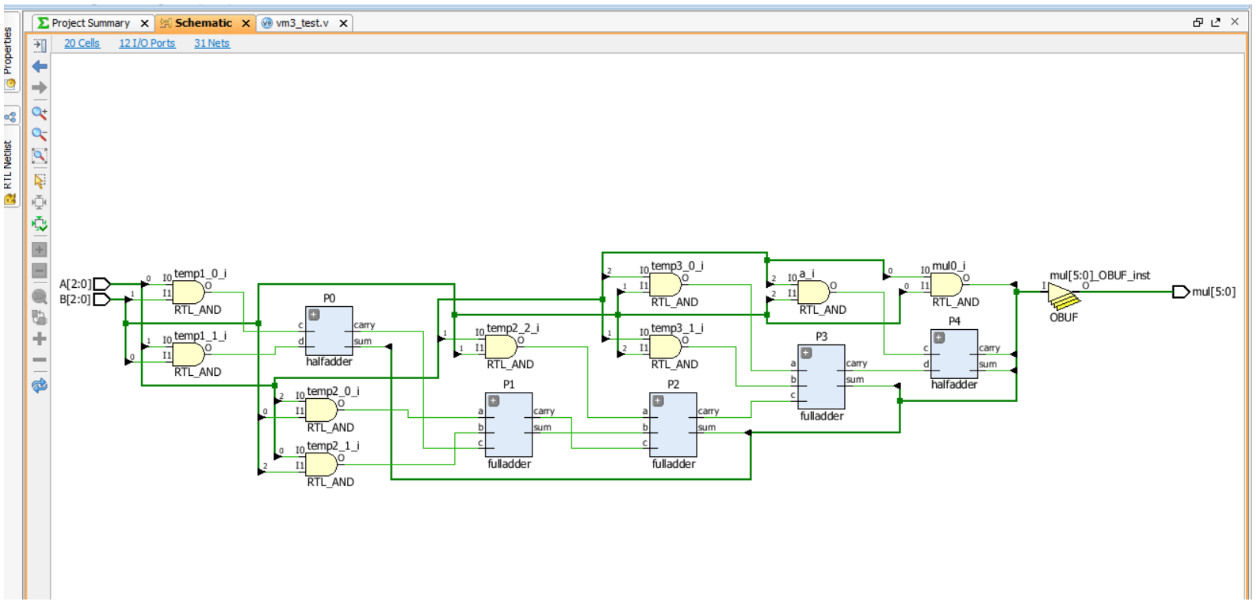
```
      B1=3'b101;

    #1 A1=3'b101;
       B1=3'b110;

    #1 A1=3'b110;
      B1=3'b111;
end

endmodule
```

Results :

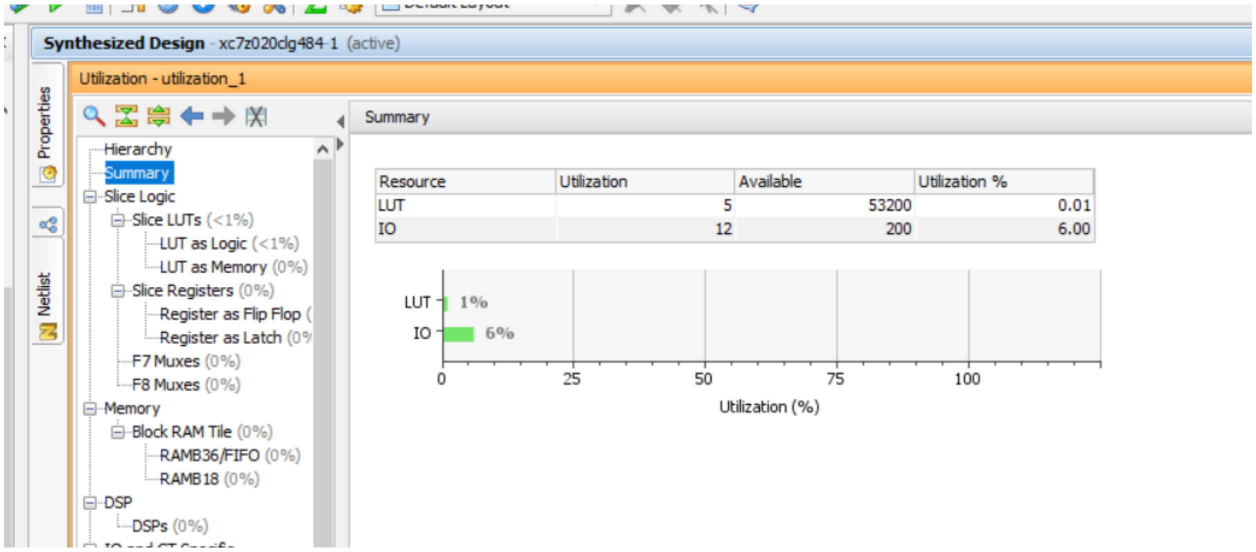
Simulation Output



Schematic



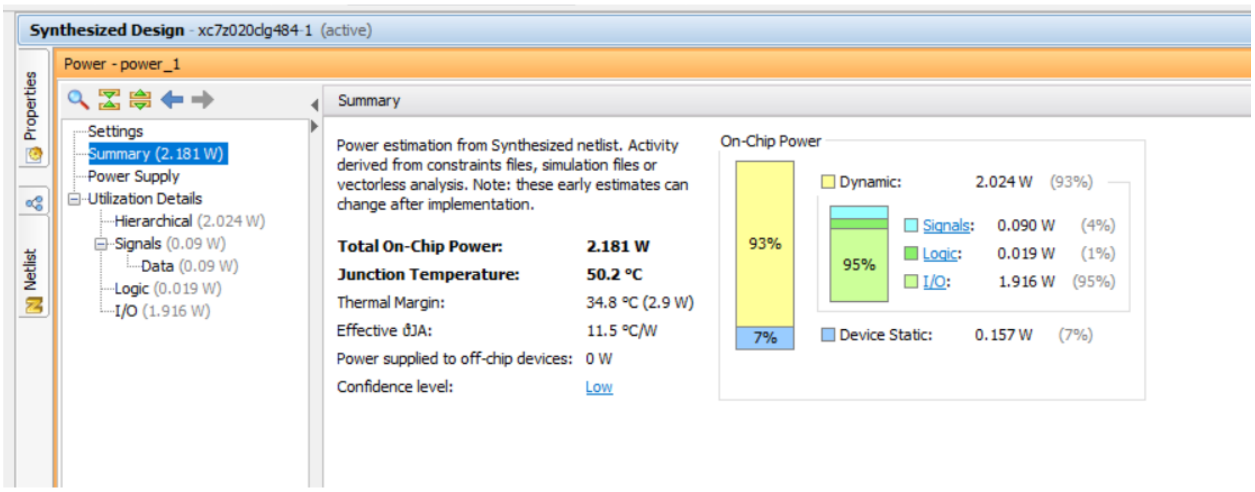
Utilization report



Summary

Resource	Utilization	Available	Utilization %
LUT	5	53200	0.01
IO	12	200	6.00

Power report



Synthesized Design - xc7z020clg484-1 (active)

Power - power_1

- Settings
- Summary (2.181 W)
- Power Supply
- Utilization Details
  - Hierarchical (2.024 W)
  - Signals (0.09 W)
    - Data (0.09 W)
  - Logic (0.019 W)
  - I/O (1.916 W)

Summary

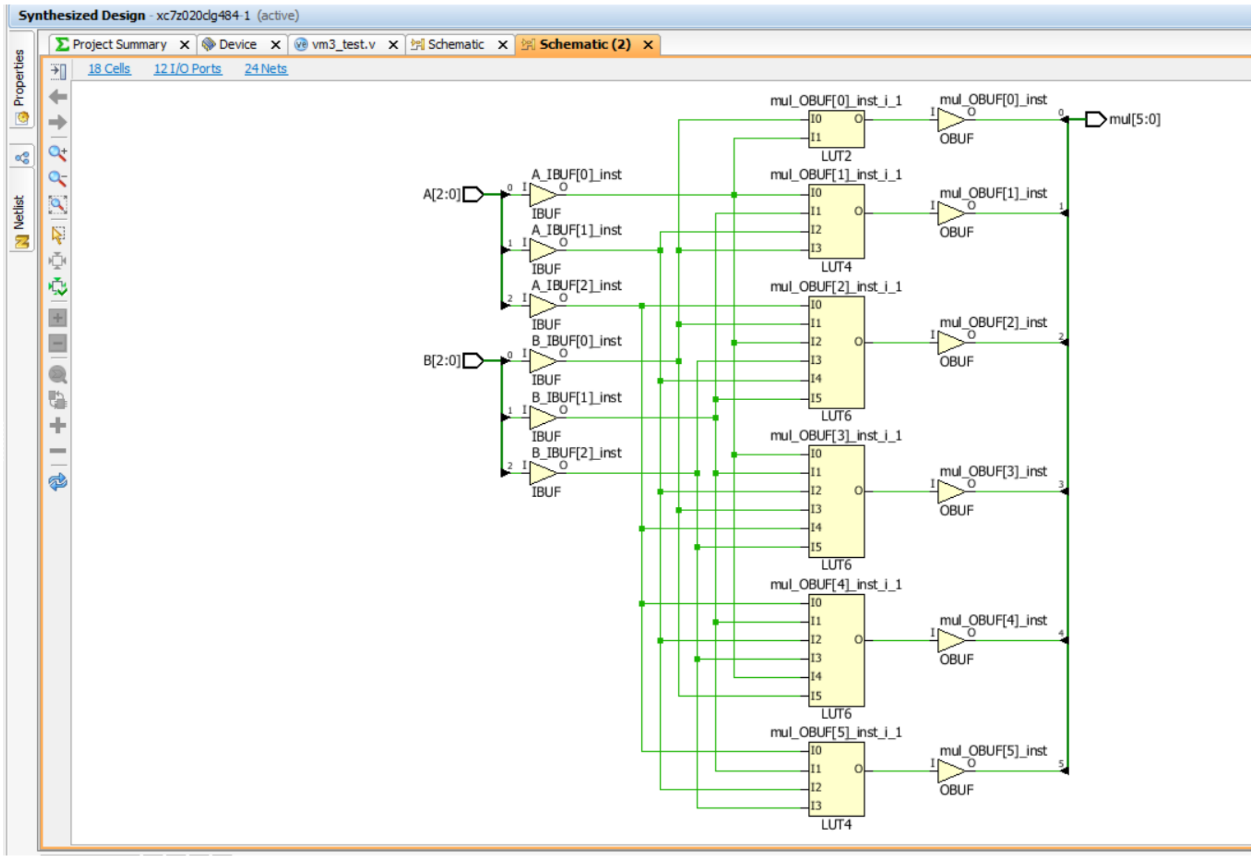
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

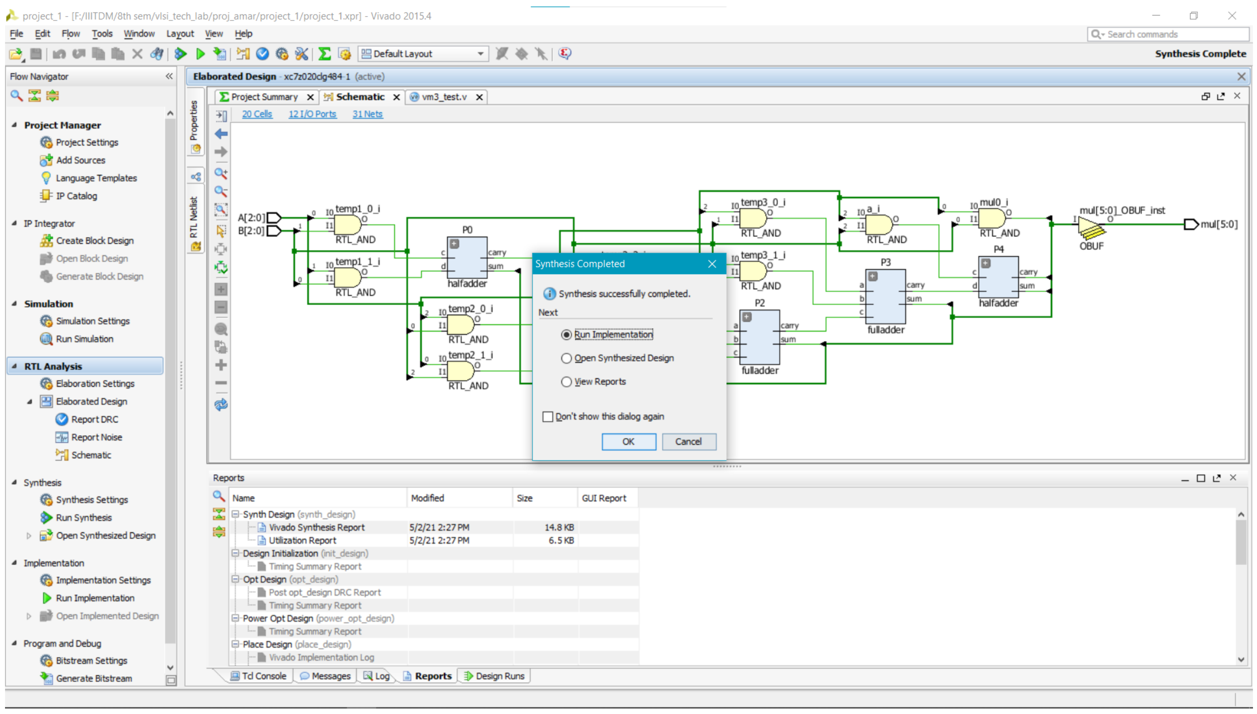
Total On-Chip Power:	**2.181 W**
Junction Temperature:	**50.2 °C**
Thermal Margin:	34.8 °C (2.9 W)
Effective θJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power

Dynamic:		2.024 W	(93%)
	Signals:	0.090 W	(4%)
	Logic:	0.019 W	(1%)
	I/O:	1.916 W	(95%)
Device Static:		0.157 W	(7%)

Synthesis Schematic





Synthesis Completed

Synthesis successfully completed.

Next

[✓ Run Implementation]
Open Synthesized Design
View Reports

Don't show this dialog again

OK Cancel

Reports

Name	Modified	Size	GUI Report
Synth Design (synth_design)			
Vivado Synthesis Report	5/2/21 2:27 PM	14.8 KB	
Utilization Report	5/2/21 2:27 PM	6.5 KB	
Design Initialization (init_design)			
Timing Summary Report			
Opt Design (opt_design)			
Post opt_design DRC Report			
Timing Summary Report			
Power Opt Design (power_opt_design)			
Timing Summary Report			
Place Design (place_design)			
Vivado Implementation Log			

Conclusion

3 bit Vedic Multiplier is implemented and outputs are attached