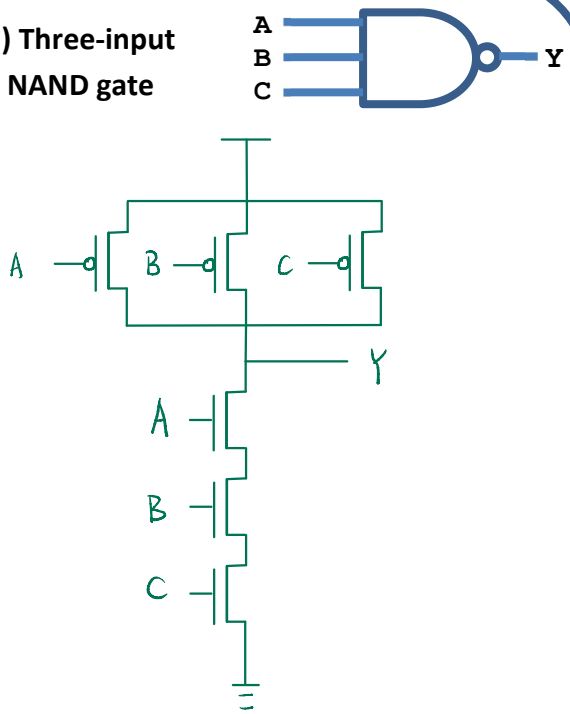
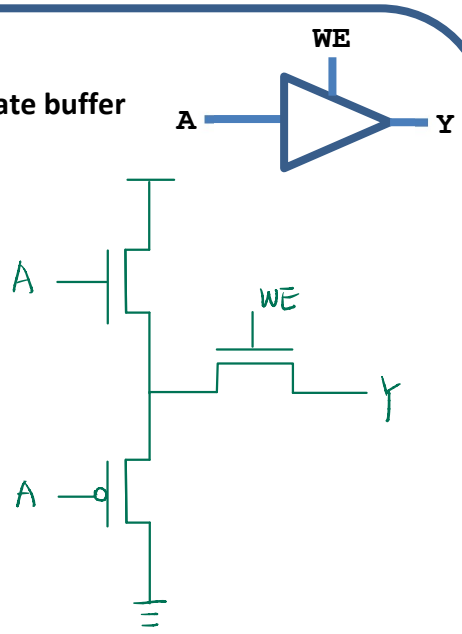
Part B: Transistors (16 marks)

For each of the gates and devices below, draw a transistor circuit that implements its behaviour in the spaces provided. In each case, full marks will only be given to circuits that a) use the fewest transistors possible and b) are drawn clearly and neatly (i.e. similar to the lecture slide diagrams).

a) Three-input NAND gate

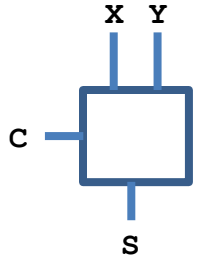


b) Tri-state buffer

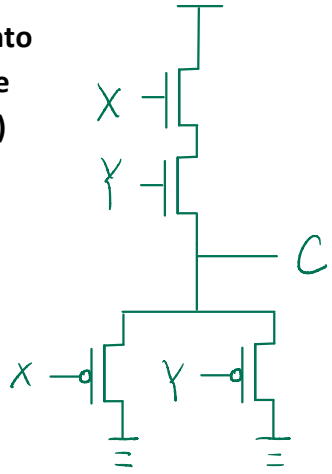


c) Half Adder

(separate this into two circuits, one for each output)



$C = X \cdot Y$



$S = X \cdot \bar{Y} + \bar{X} \cdot Y$