

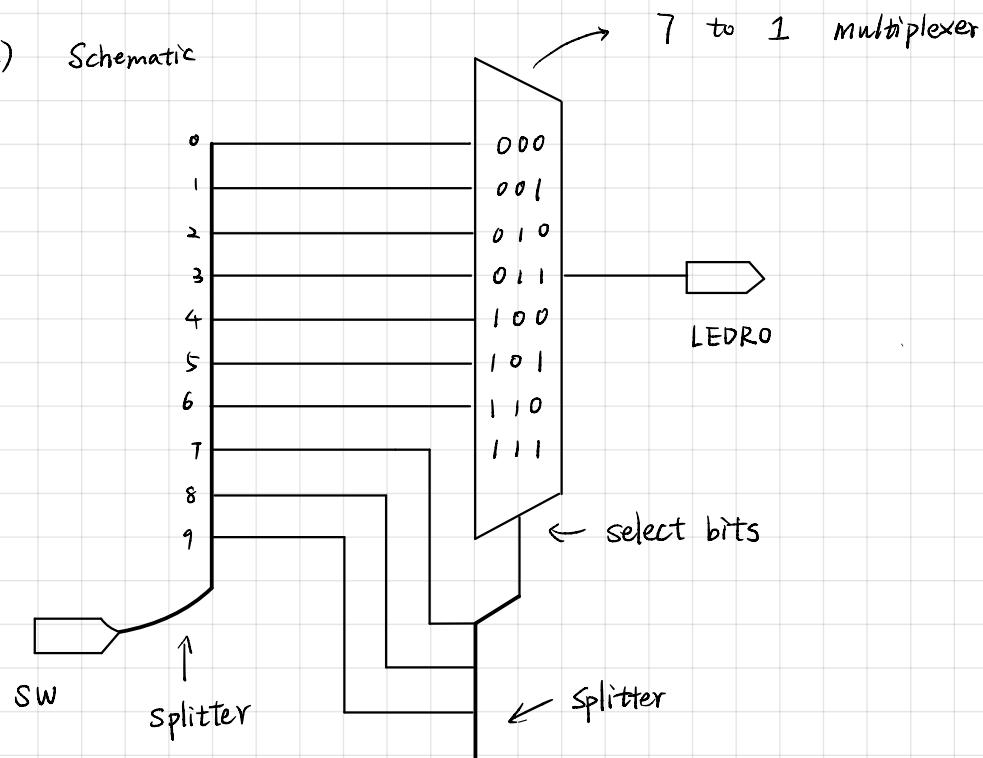
CSC 258 Lab 3

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Part I

1. (a) Schematic

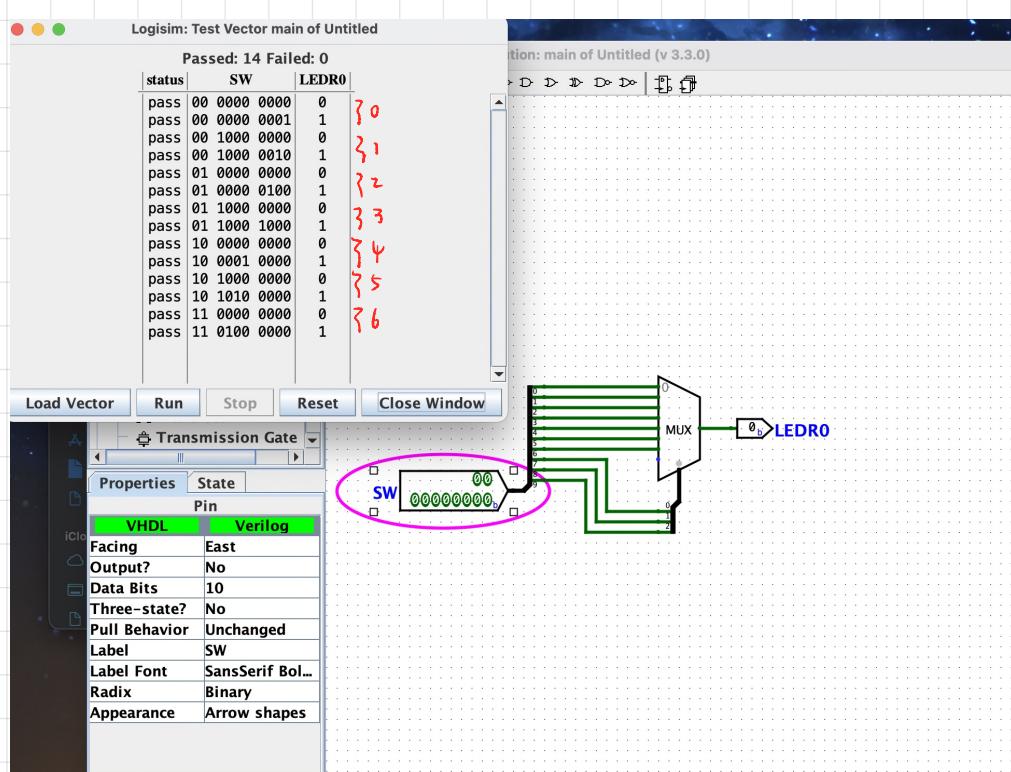


(b) 10 data bits in total

7 for multi-bit input

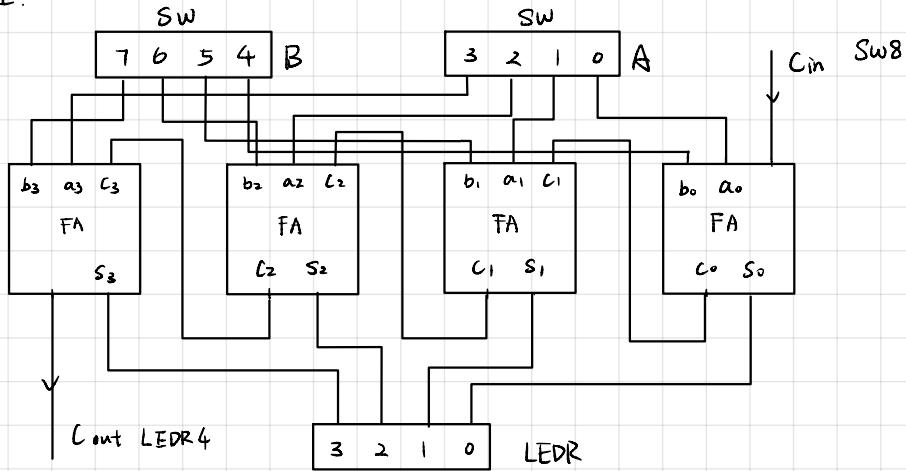
3 for select bits

2. 3.

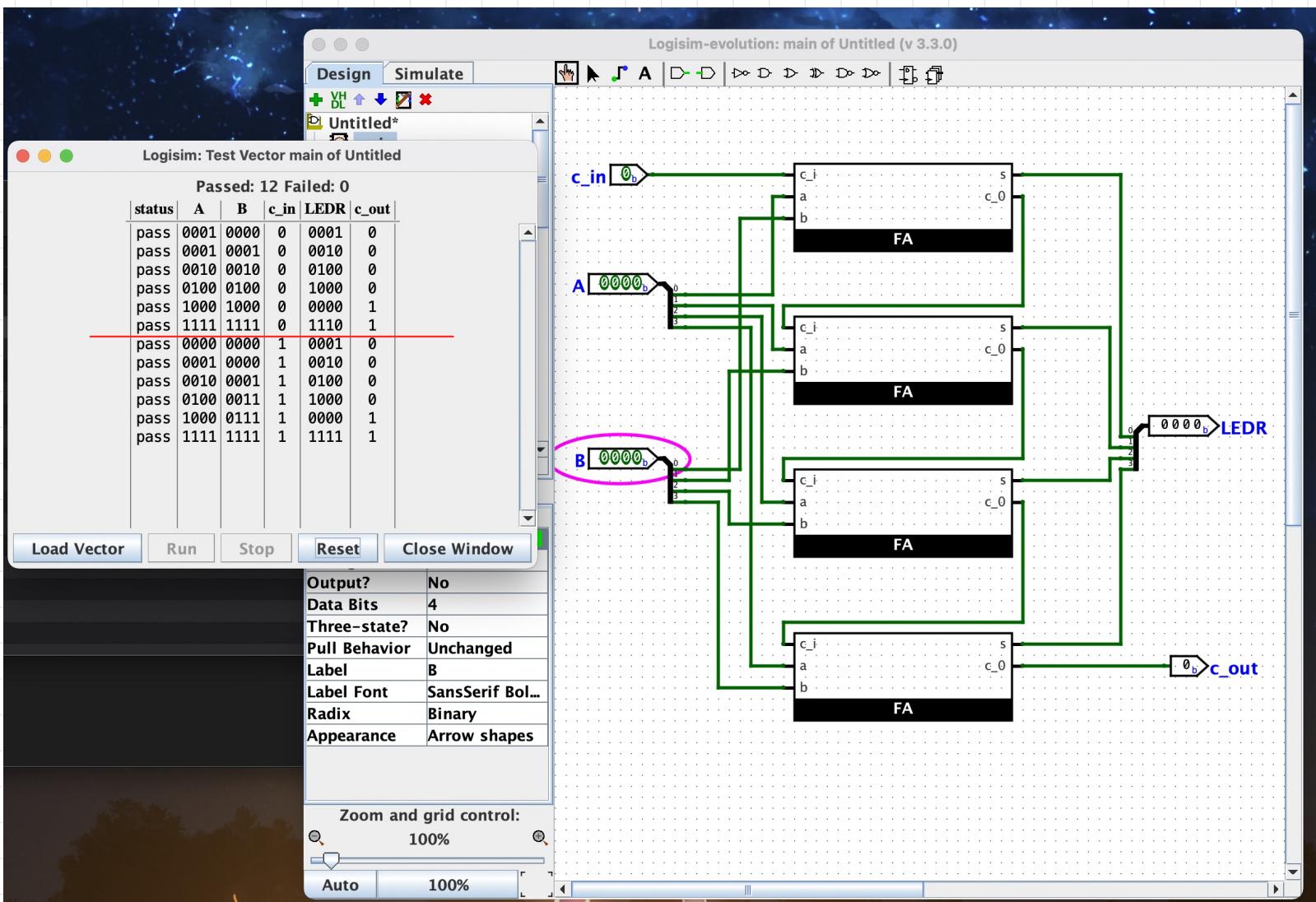


Part II

1

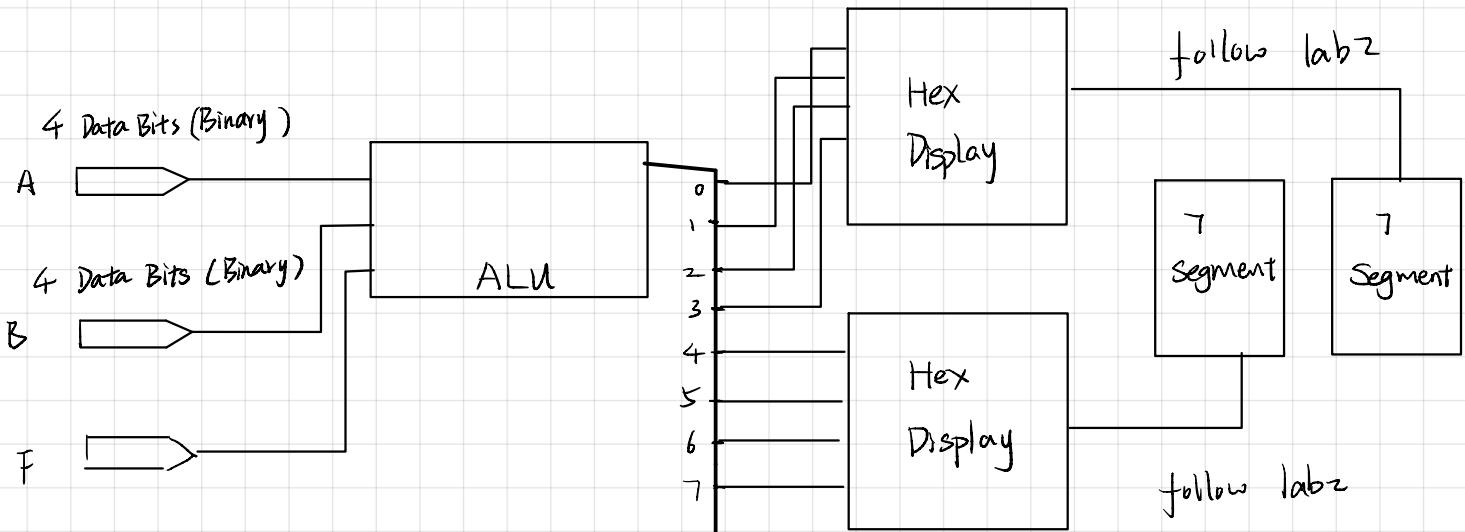


2. 3.

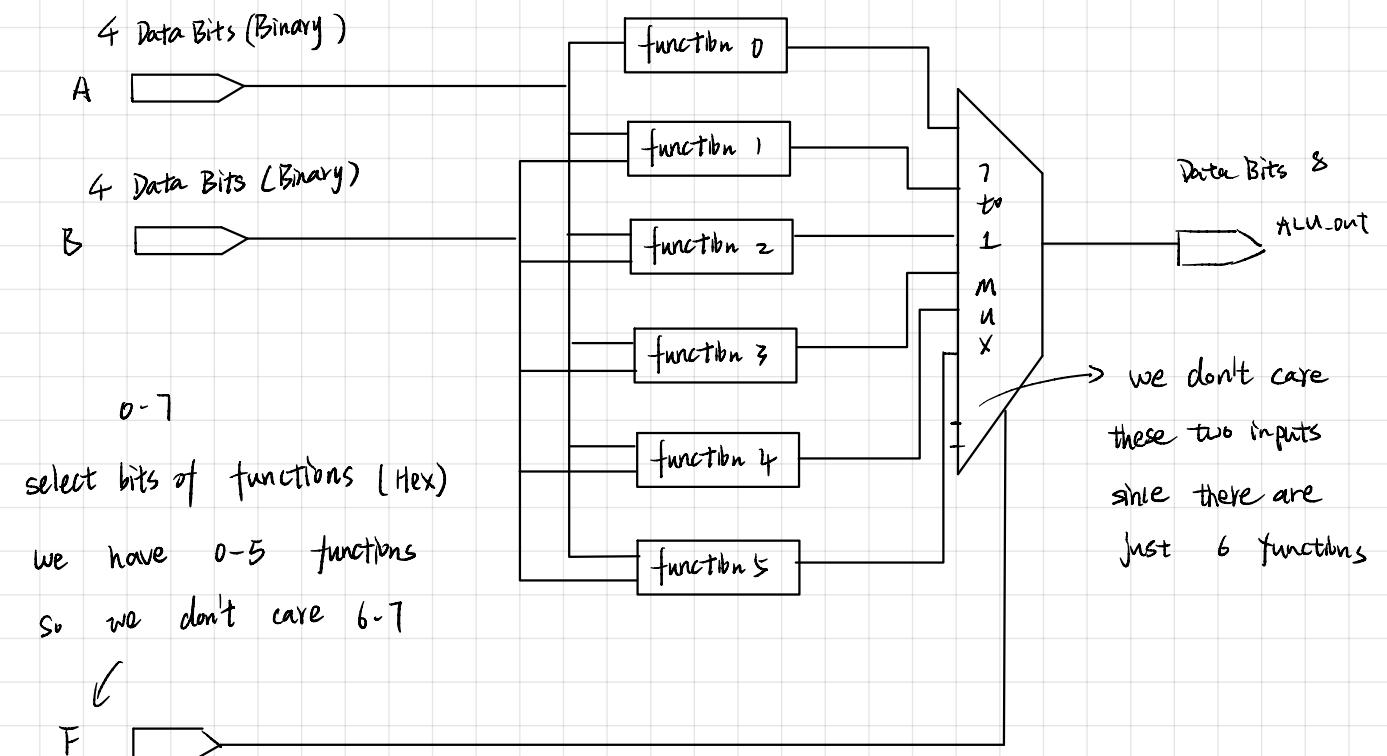


Part III

Main



ALU

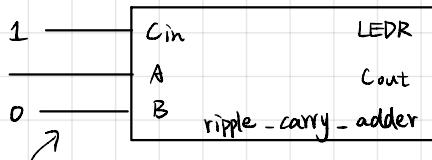


function 0

$A + 1$

use Part II

(4 Bits Binary) A



has no relationship with B

splitter

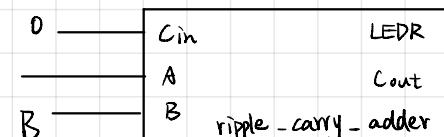
ALUout (8 bits Binary)

Bit Extender
1 to 4

function 1

$A + B$ use adder from Part II

(4 Bits Binary) A



(4 Bits Binary) B

splitter

ALUout (8 bits Binary)

Bit Extender
1 to 4

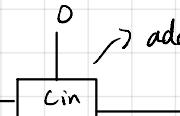
function 2

$A + B$ use adder

(4 Bits Binary) A

(4 Bits Binary) B

adder



ALUout (8 Bits Binary)

splitter

Bit Extender 1 to 4

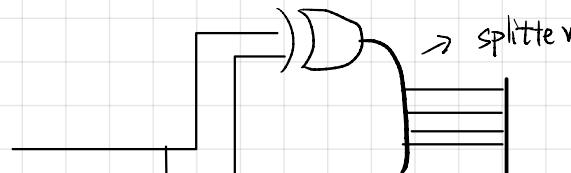
function 3

Bitwise A XOR B in the lower four and Bitwise A OR B in

the upper four

(4 Bits Binary) A

(4 Bits Binary) B



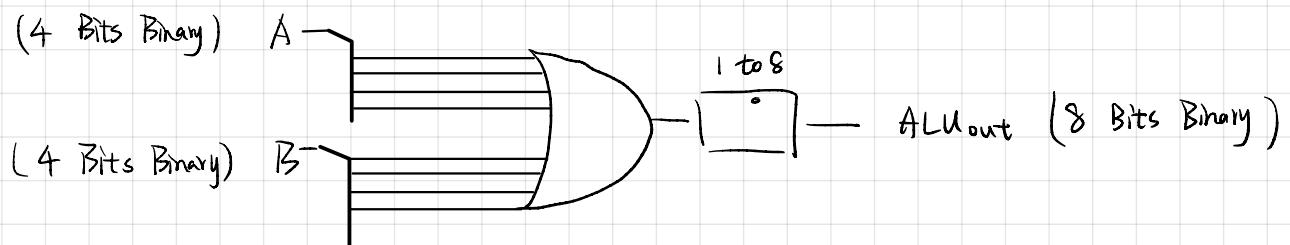
ALUout (8 Bits Binary)

splitter

splitter

function 4 any of 8 bits in A or B are high : output 1

all the bits are low : output 0



function 5

A left most four bits

B right most four bits

