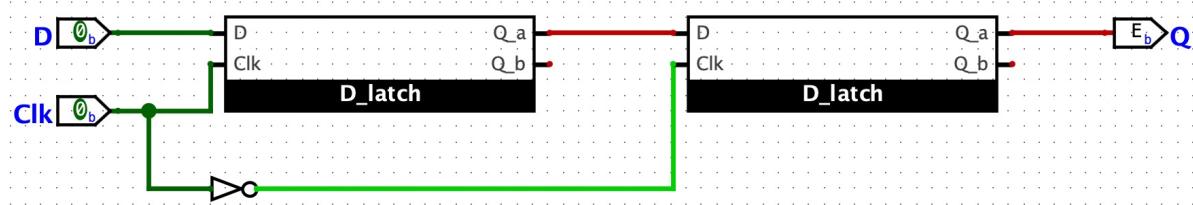
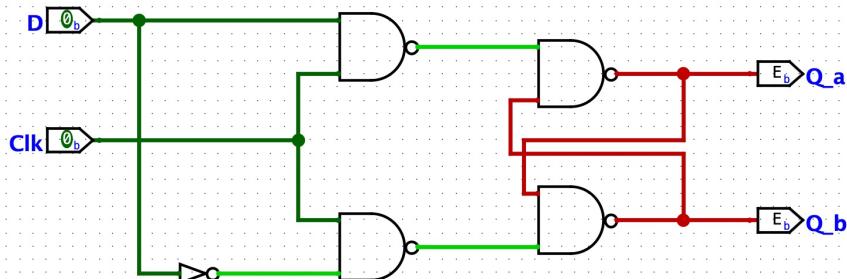


Part I

1.



3. D-Latch

When Clk is low at the beginning, no matter D is,
 Q_a and Q_b are unknown. That will make the result become error.

Master - slave - flip - flop

When Clk is low, there will be an error since the first
D-latch is not connected, there are no inputs for the second D-latch.

When Clk is high, the second D-latch is not connected
then there is not output, which makes an error.

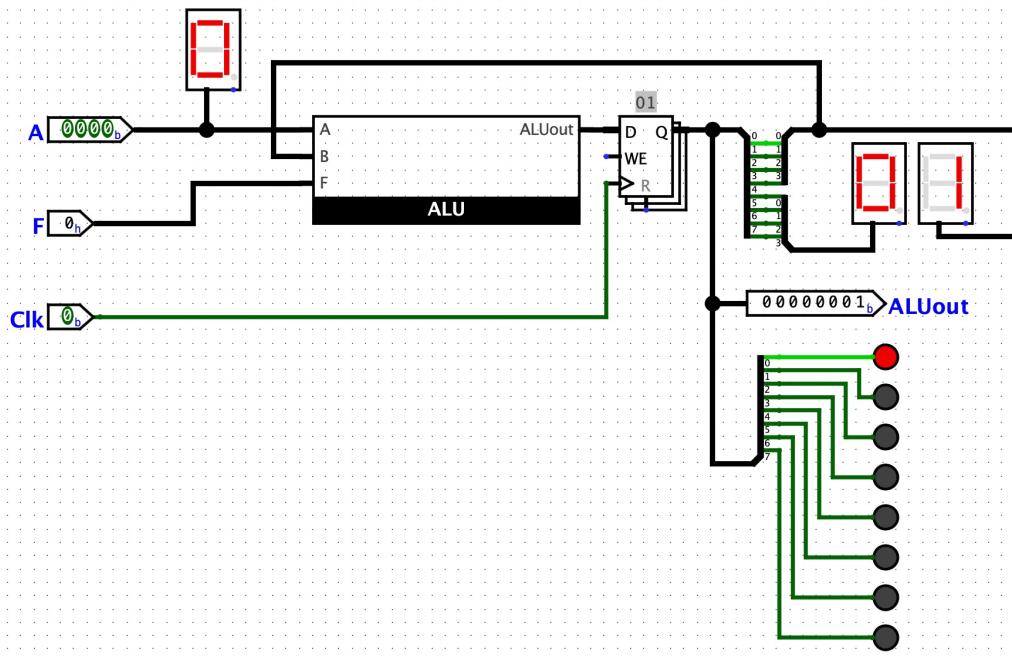
4. D-latch $(0,0)$ $(1,0)$ should not be the first (from 3)

Master-slave-flip-flop

$(0,0)$ $(0,1)$ $(1,0)$ $(0,1)$ should not be the first (from 3)

Part II

1.



2. (a) The Register is used to store a temporary value.

It stores B as input for the next "calculation".

If we didn't include register, the output from ALU will automatically become the input of B each time, which forms a "infinite loop".

(b) the largest n bits binary:

$$\underbrace{111 \dots 111}_{n \text{ bits}}$$

which equals to

$$\underbrace{100 \dots 000}_{n+1 \text{ bits}} - 1 = 2^n - 1 \text{ in decimal}$$

$$(2^n - 1)(2^n - 1) = 2^{2n} - 2^n - 2^n + 1 = 2^{2n} - 2 \cdot 2^n + 1$$

$$= 2^{2n} - 2^{n+1} + 1 = 2^{2n} - (2^{n+1} - 1)$$

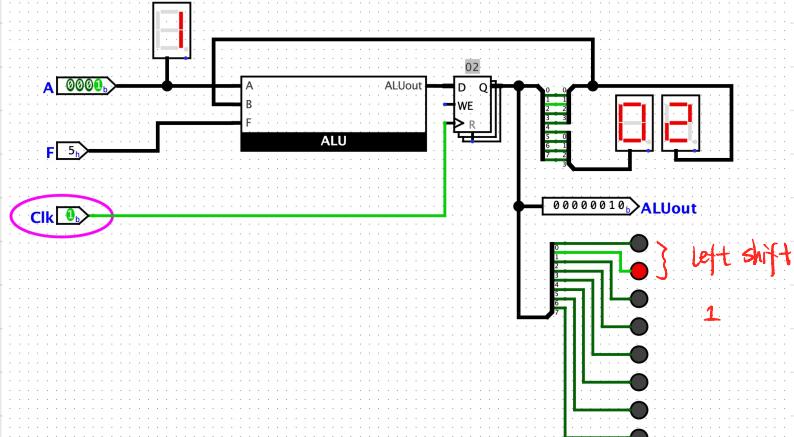
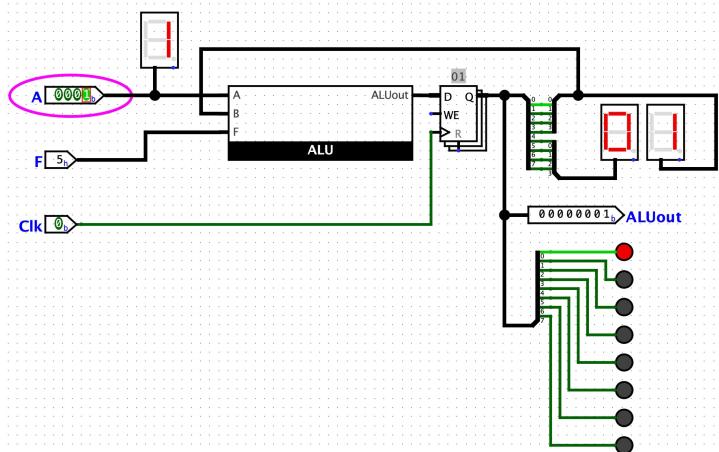
$$2^{n+1} - 1 \geq 1 \quad \text{when } n \geq 0$$

then $2^{2n} - (2^{n+1} - 1) \geq 2^{2n} - 1$ (2^{2n} has $2n+1$ bits)

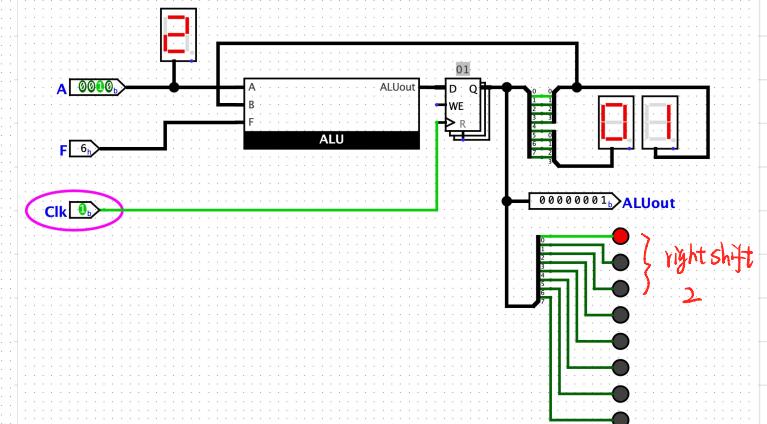
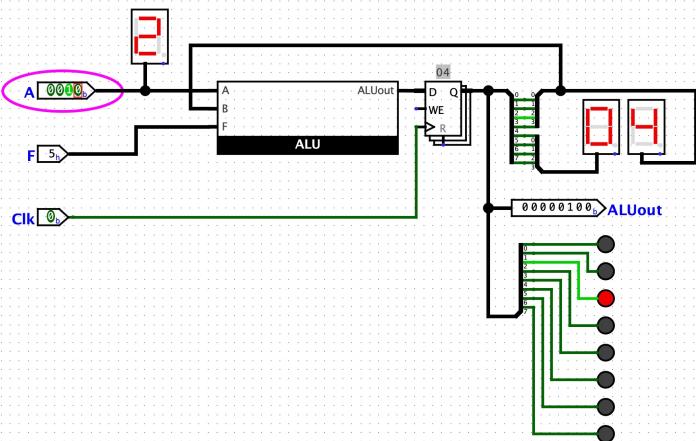
then n bits \times n bits has at least $2n$ bits

	F	A	ALUout		F	A	ALUout	
0	0000		0000 0001		1	0001	0000 0001	
0	0001		0000 0010		1	0010	0000 0011	
0	0010		0000 0011		1	0001	0000 0100	
0	0011		0000 0100		1	0011	0000 0111	
2	0001		0000 0001		3	0001	0001 0001	
2	0010		0000 0011		3	0001	0001 0000	
2	0001		0000 0100		3	1111	1111 1111	
2	0011		0000 0111		3	0101	1111 1010	
4	0000		0000 0000		5	0000	0000 0010	← ALU is 00000010
4	0001		0000 0001		5	0001	0000 0100	at first
4	0001		0000 0001		5	0010	0001 0000	
4	0010		0000 0001		5	0001	0010 0000	
ALU is 0000 1000 →		6	0000	0000 1000	7	0001	0000 0010	← ALU is 0000 0010
at first		6	0001	0000 0100	7	0001	0000 0010	at first
		6	0000	0000 0100	7	0010	0000 0100	
		6	0001	0000 0010	7	0001	0000 0100	

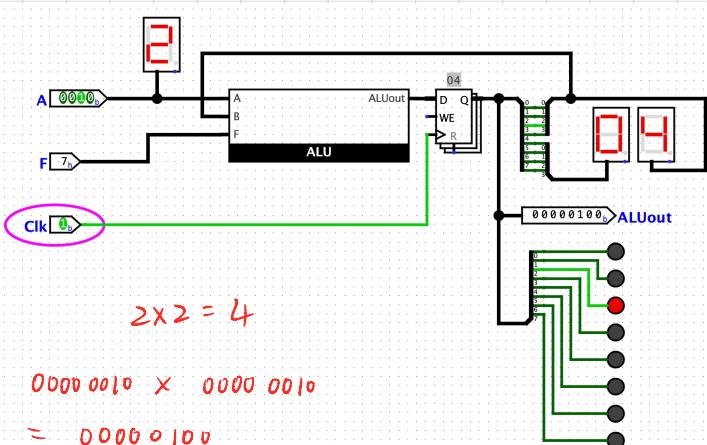
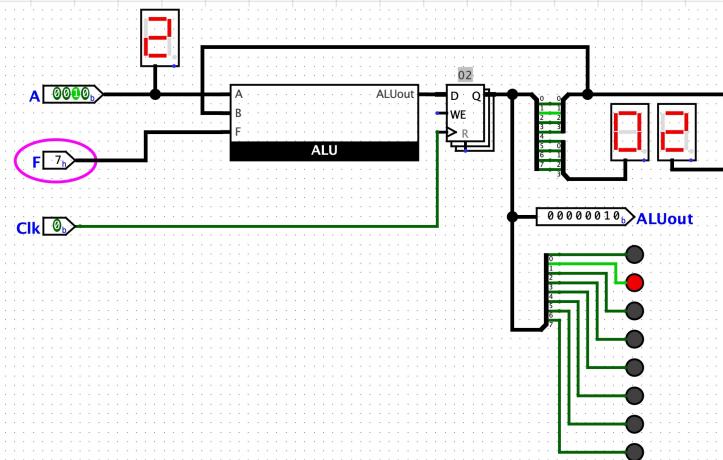
(b) Function 5 We set ALU 0000 0001 at first



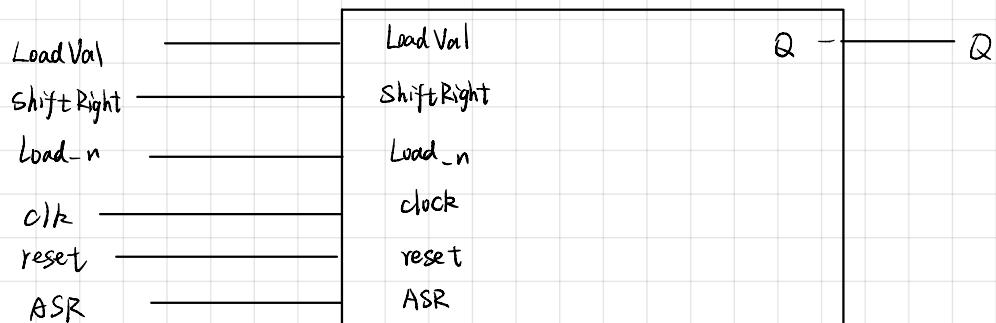
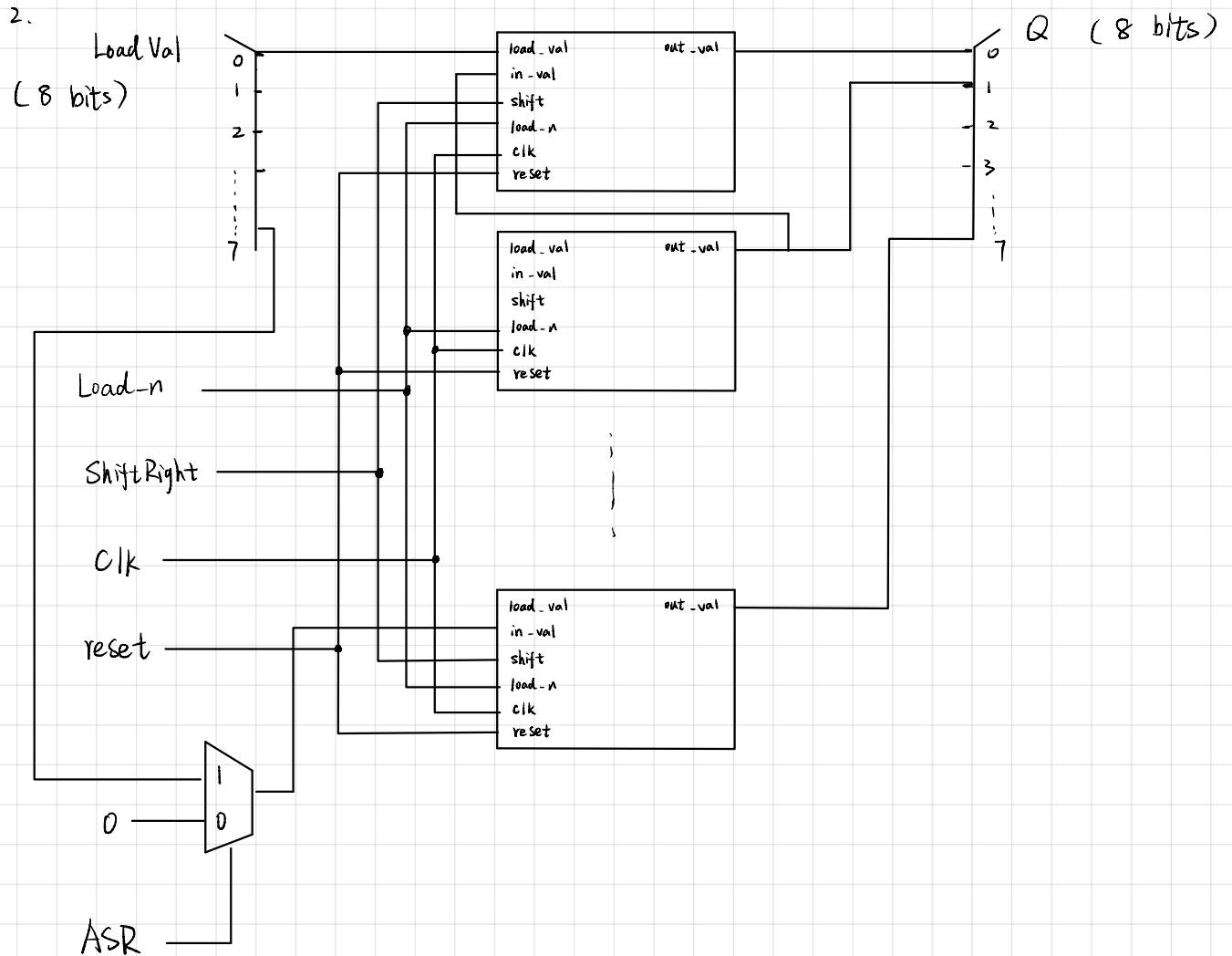
Function 6 we set ALU 0000 0100 at first



Function 7 we set ALU 0000 0010 at first

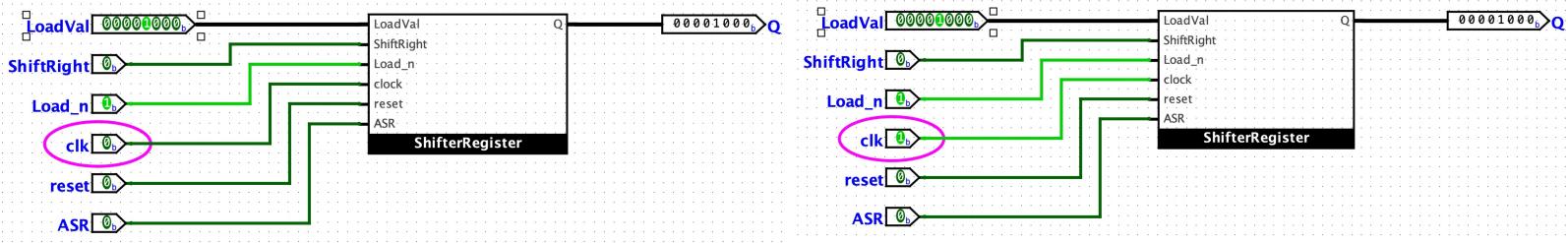


3. 1. If Shift Right = 0 , it makes the first mux of shifterBit output the original bit , If Load-n =1 it makes the the second mux output the original bit . the input just stays at the same position .

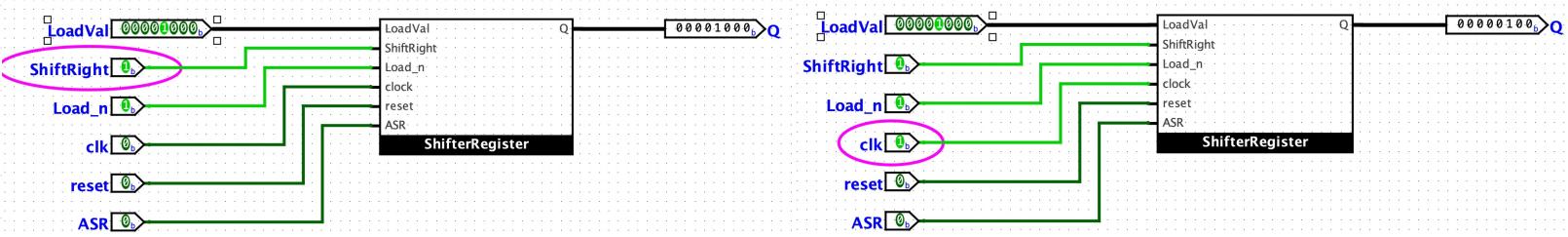


5.

When ShiftRight = 0 , the output bit doesn't change



when ShiftRight = 1 , ASR = 0 , it has logic right shift



When ShiftRight = 1 , ASR = 1 , it has arithmetic right shift

