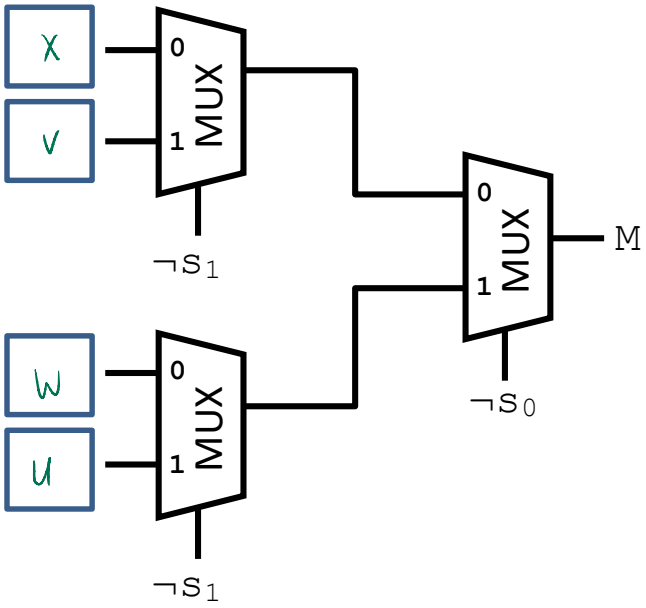
Part D: Logical Devices (8 marks)

1. Recall the 4-to-1 multiplexer schematic below that you produced for Lab 2 below. The table on the right is also the same as from Lab 2, but the select bit configuration is different. What would the inputs need to be to create the behaviour specified by the table on the right? Indicate your answer by filling in the spaces on the left side of the diagram. **(4 marks)**



S_1S_0	M
00	U
01	V
10	W
11	X

2. Consider the same 2-to-1 multiplexers shown above. In the space below, draw a circuit with inputs U, V, W & X and a single output M. This circuit implements M=U·V·W·X using only 2-to-1 multiplexers (no other gates). For full marks, use the fewest multiplexers possible. **(4 marks)**