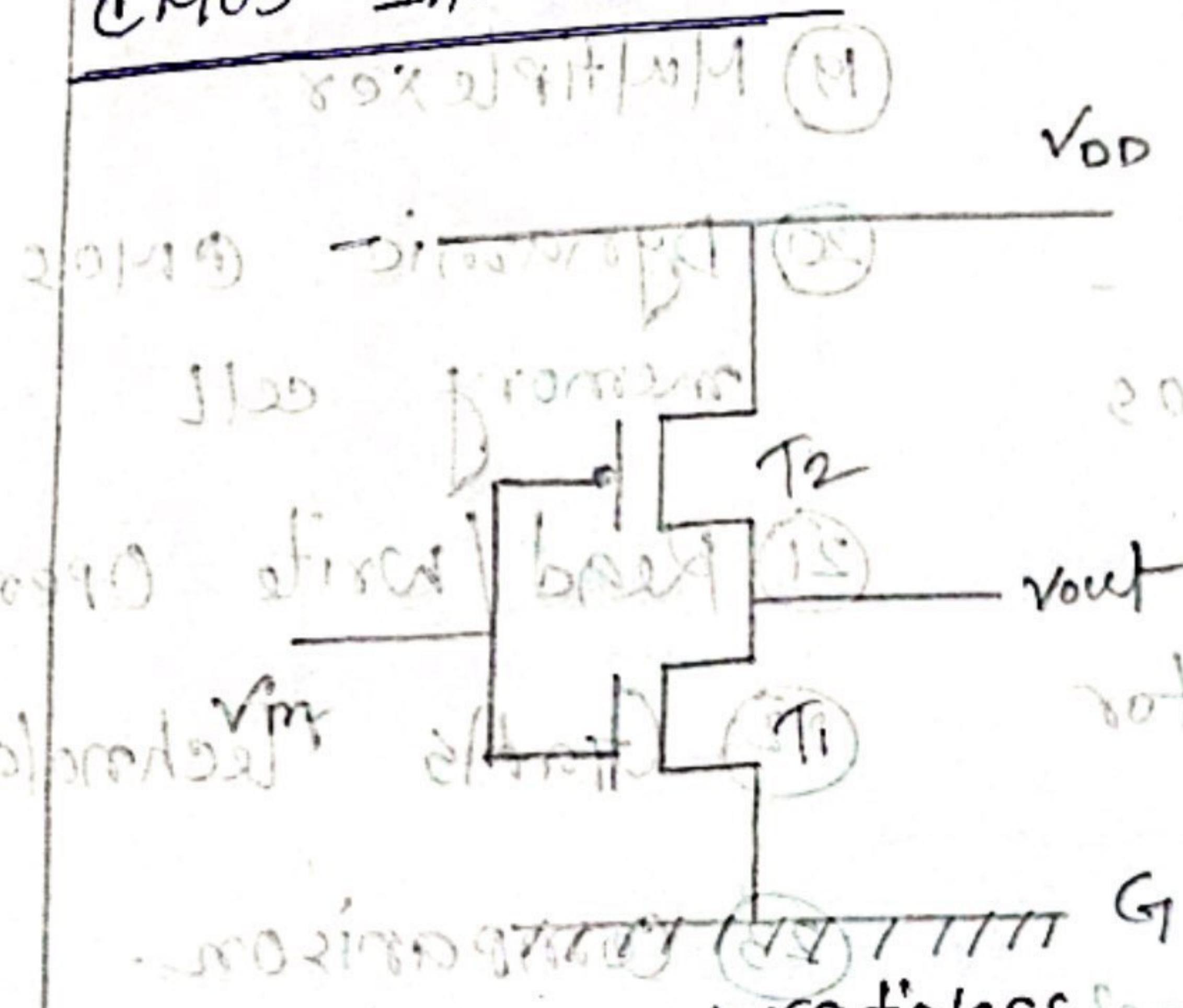


final Syllabus

- ① Intro to CMOS
- ② CMOS inverter and working principle
- ③ Disadvantage of CMOS inverter
- ④ NMOS Pass Transistor
- ⑤ CMOS pass gate
- ⑥ Ratioless NMOS inverter
- ⑦ Latch up in NMOS inverter
- ⑧ Design Rule
- ⑨ Stick diagram
- ⑩ Power dissipation
- ⑪ Scaling
- ⑫ Limitation of scaling
- ⑬ Sub system design
- ⑭ Multi input NAND/NOR
- ⑮ Pseudo NMOS logic
- ⑯ Dynamic CMOS logic
- ⑰ Clocked CMOS
- ⑱ Complex CMOS logic
- ⑲ Multiplexer
- ⑳ Dynamic CMOS memory cell
- ㉑ Read / write Operation
- ㉒ GaAs Technology
- ㉓ Comparison.

CMOS Inverter



$$V_{in} = \underline{\text{low}}$$

$\pi \rightarrow \text{off}$

$T_2 \rightarrow \infty$

$$V_{out} = V_{D0} = \text{high} = 5V \quad (\text{shorted } \text{with } \text{GND})$$

V_{in} = high

π → on

$T_2 \rightarrow$ off

$V_{out} = 0$ or $= \text{low}$ (shorted with ground)

Advantage:

$$-V_{out}^{\downarrow} \text{ low} = 0$$

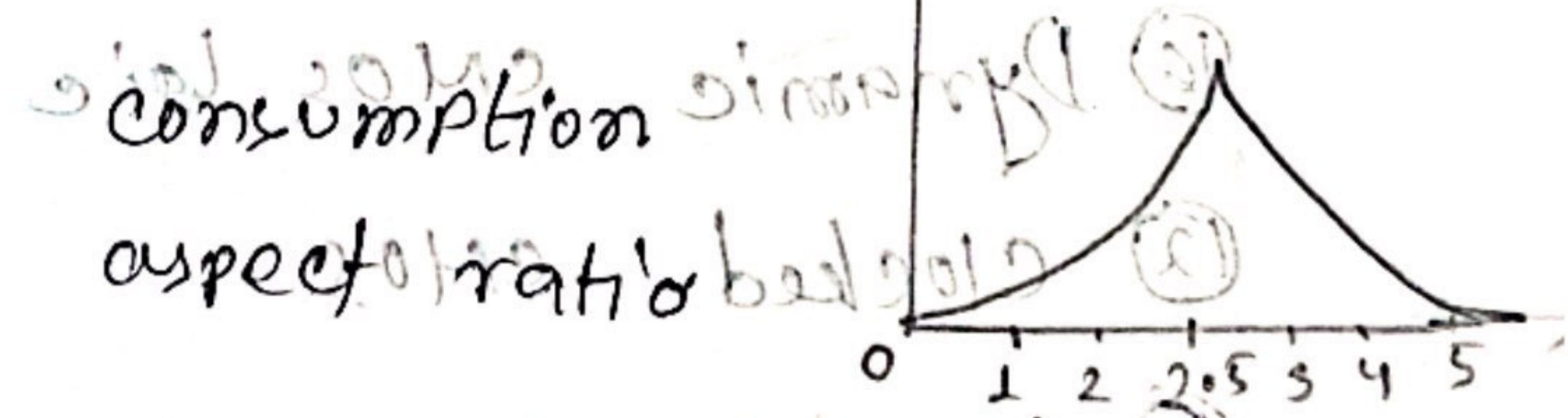
- No power loss

- No static power consumption

- No restriction of aspect ratio based on

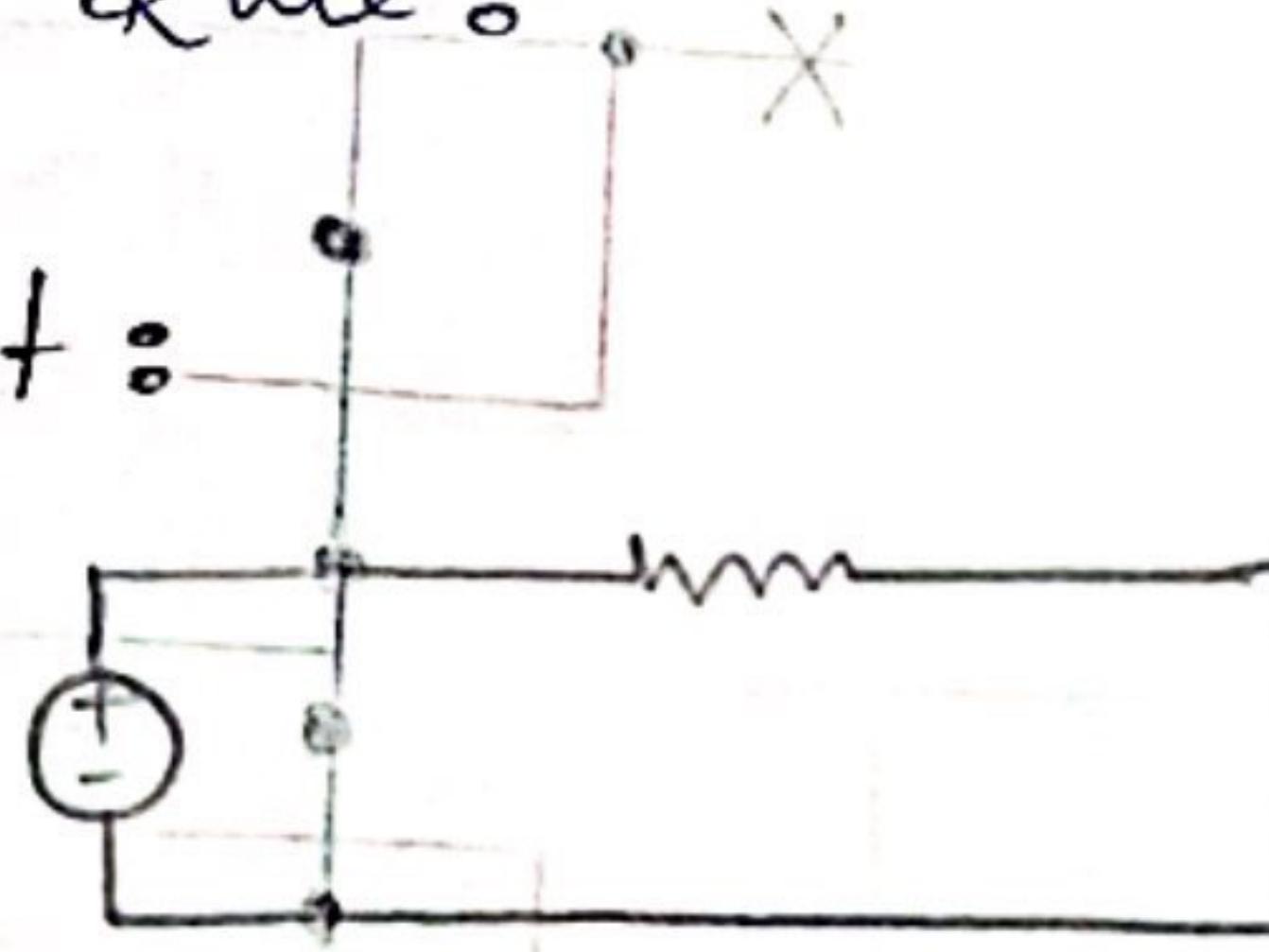
Disadvantage:

- Much slower than BJT



Design Rule:

1. Circuit:



2. Stick Diagram:

3. Layout draw:

4. Fabrication

Design Style:

Blue → Power line / Metal wire

Pink → Polysilicon → to n+ polyide gate

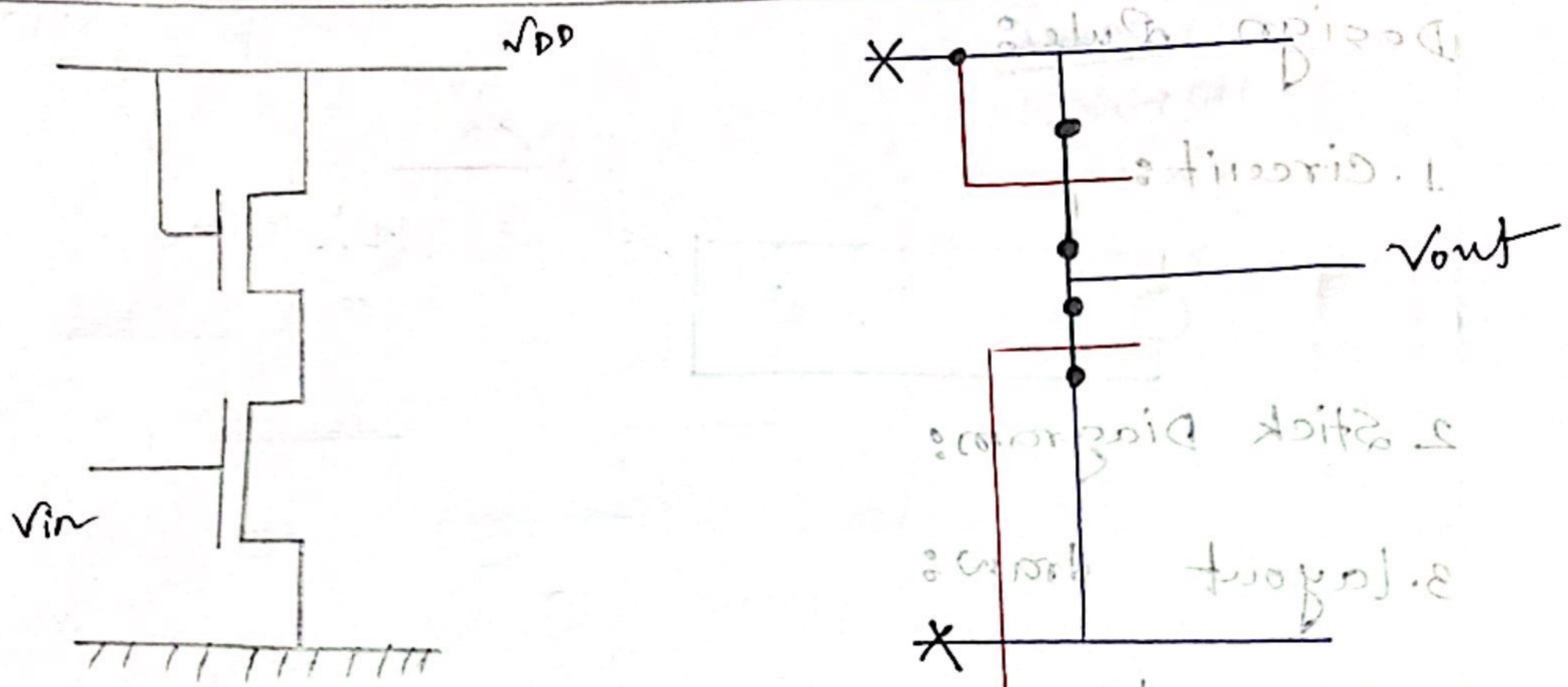
Green → diffusion layer (P/n)

brown → demarkation line
(Pencil)

Yellow → dotted → implant

Black cross → Power line

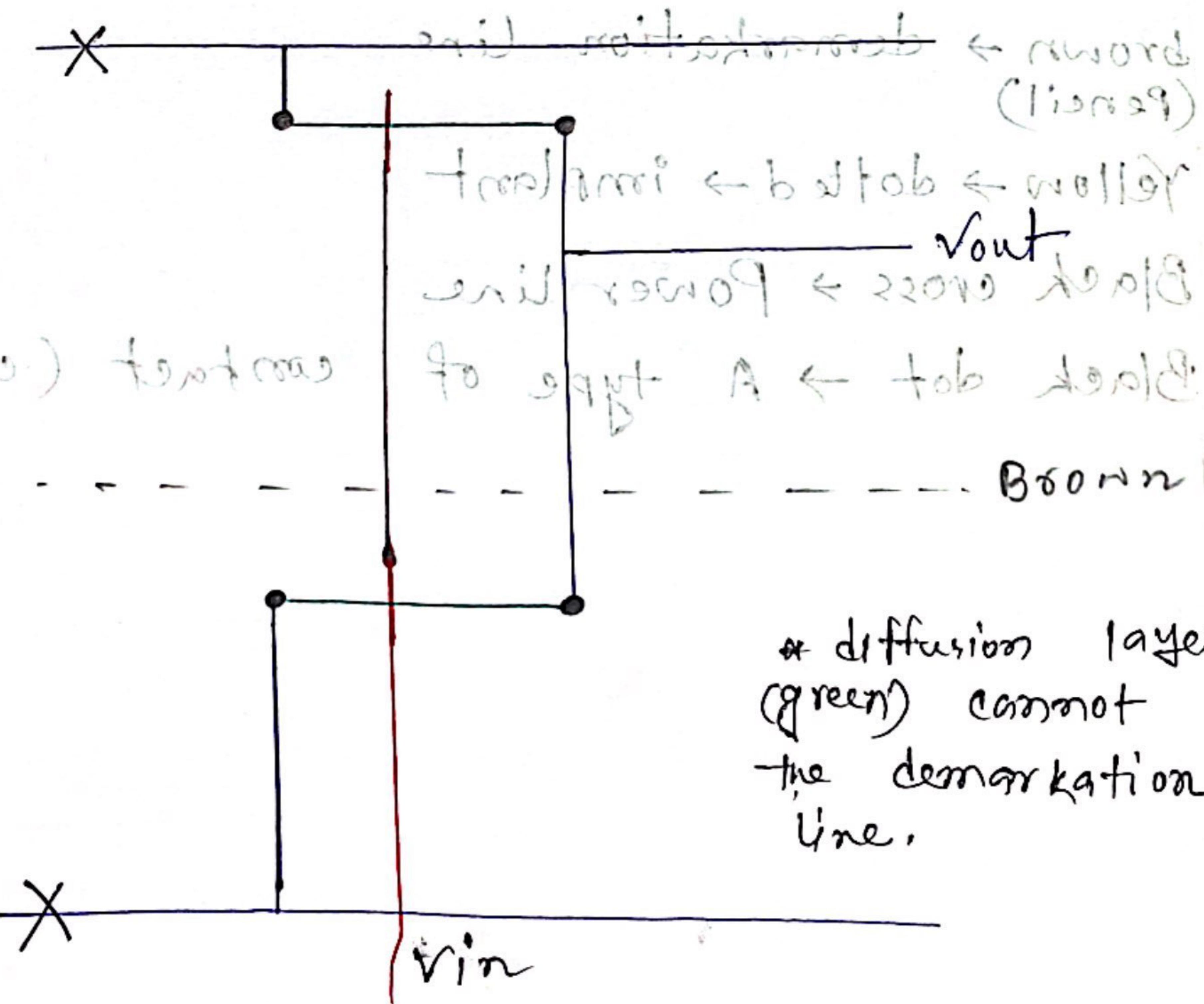
Black dot → A type of contact (connection)



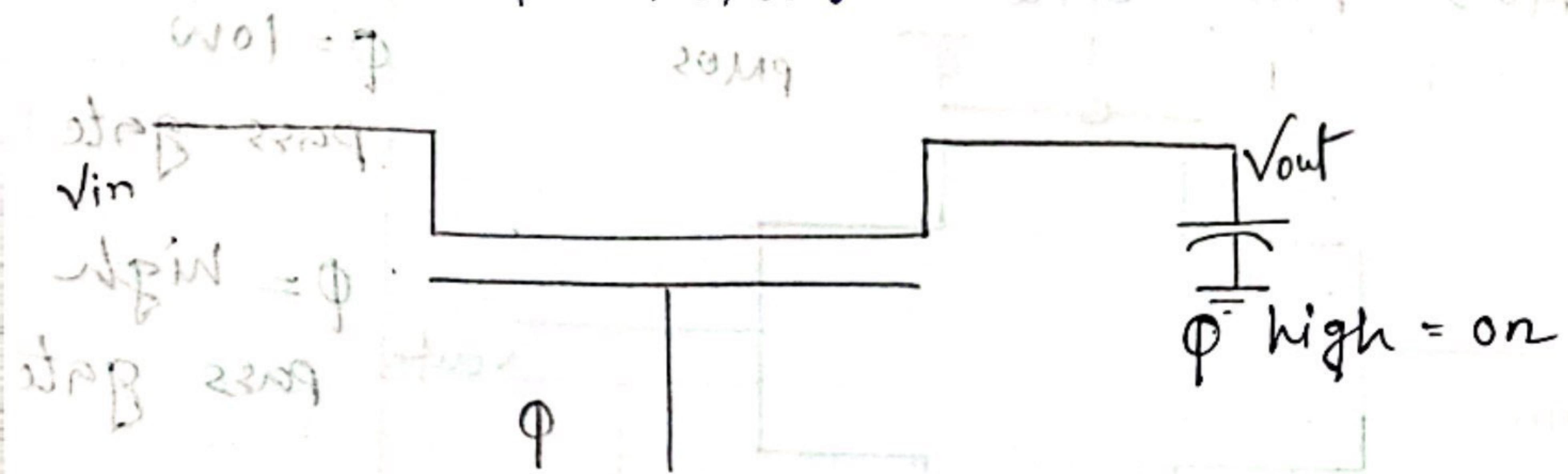
- yellow dot \rightarrow depletion
 \rightarrow yellow dot N^+ \rightarrow Enhancement

(NMOS) drain regions \leftarrow well

Stick diagram of CMOS Inverter

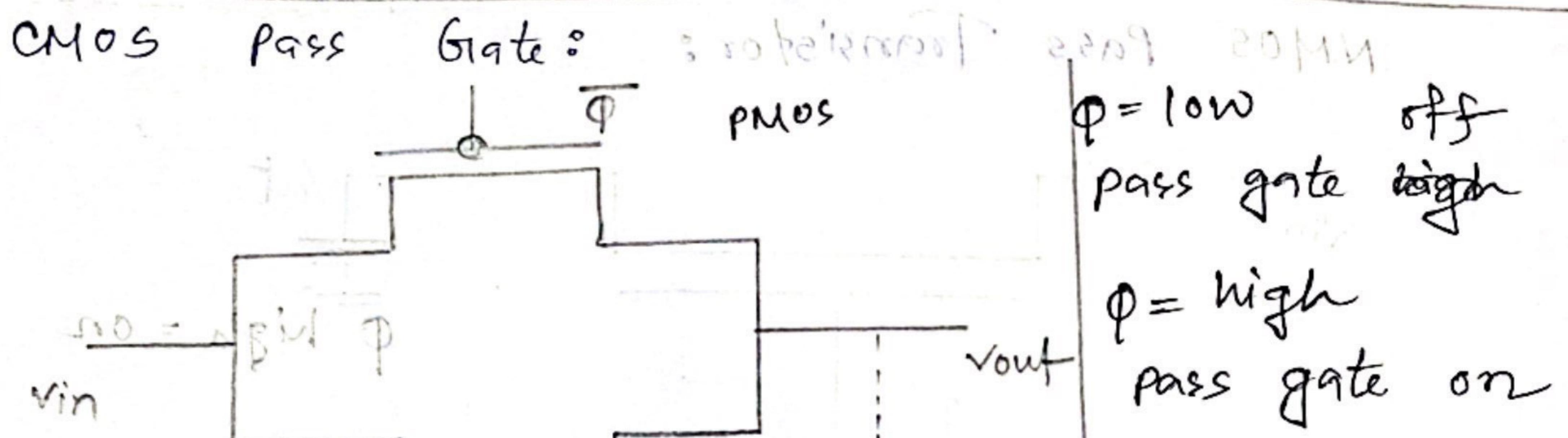


NMOS Pass Transistor:



* Output (V_{out}) will be degraded because NMOS cannot accurately pass high.

- ① V_{in} high, initial V_{out} high $\xrightarrow{\Phi \text{ high}}$ final V_{out} degraded high $\xrightarrow{\Phi \text{ high}}$
 - ② V_{in} low, initial V_{out} low $\xrightarrow{\Phi \text{ low}}$ final V_{out} low $\xrightarrow{\Phi \text{ low}}$
 - ③ V_{in} low, initial V_{out} high $\xrightarrow{\Phi \text{ high}}$ final V_{out} low $\xrightarrow{\Phi \text{ low}}$
 - ④ V_{in} high, initial V_{out} low $\xrightarrow{\Phi \text{ low}}$ final V_{out} degraded high $\xrightarrow{\Phi \text{ high}}$
- $\left. \begin{array}{l} \text{initial } w_0 \\ \text{final } w_f \\ \text{initial } w_0 = \\ \text{final } w_f = \\ \text{initial } w_0 = \\ \text{final } w_f = \\ \text{initial } w_0 = \\ \text{final } w_f = \end{array} \right\} \text{characteristic of NMOS pass transistor}$



Initial conditions: $v_{in} = 0$, $v_{out} = 0$

Final conditions: $v_{in} = 1$, $v_{out} = 0$

$\bar{\phi} = 0$, $\bar{\phi}_{PMOS} = 1$ and $\bar{\phi}_{NMOS} = 0$ (forward bias)

$\bar{\phi} = 1$, $\bar{\phi}_{PMOS} = 0$ and $\bar{\phi}_{NMOS} = 1$ (reverse bias)

① $v_{in} = \text{high}$, Initial $v_{out} = \text{high}$ and final $v_{out} = \text{high}$ (pure) no current flow

Initial conditions: $v_{in} = 1$, $v_{out} = 1$

② $v_{in} = \text{low}$, Initial $v_{out} = \text{low}$ and final $v_{out} = \text{low}$

Initial conditions: $v_{in} = 0$, $v_{out} = 0$

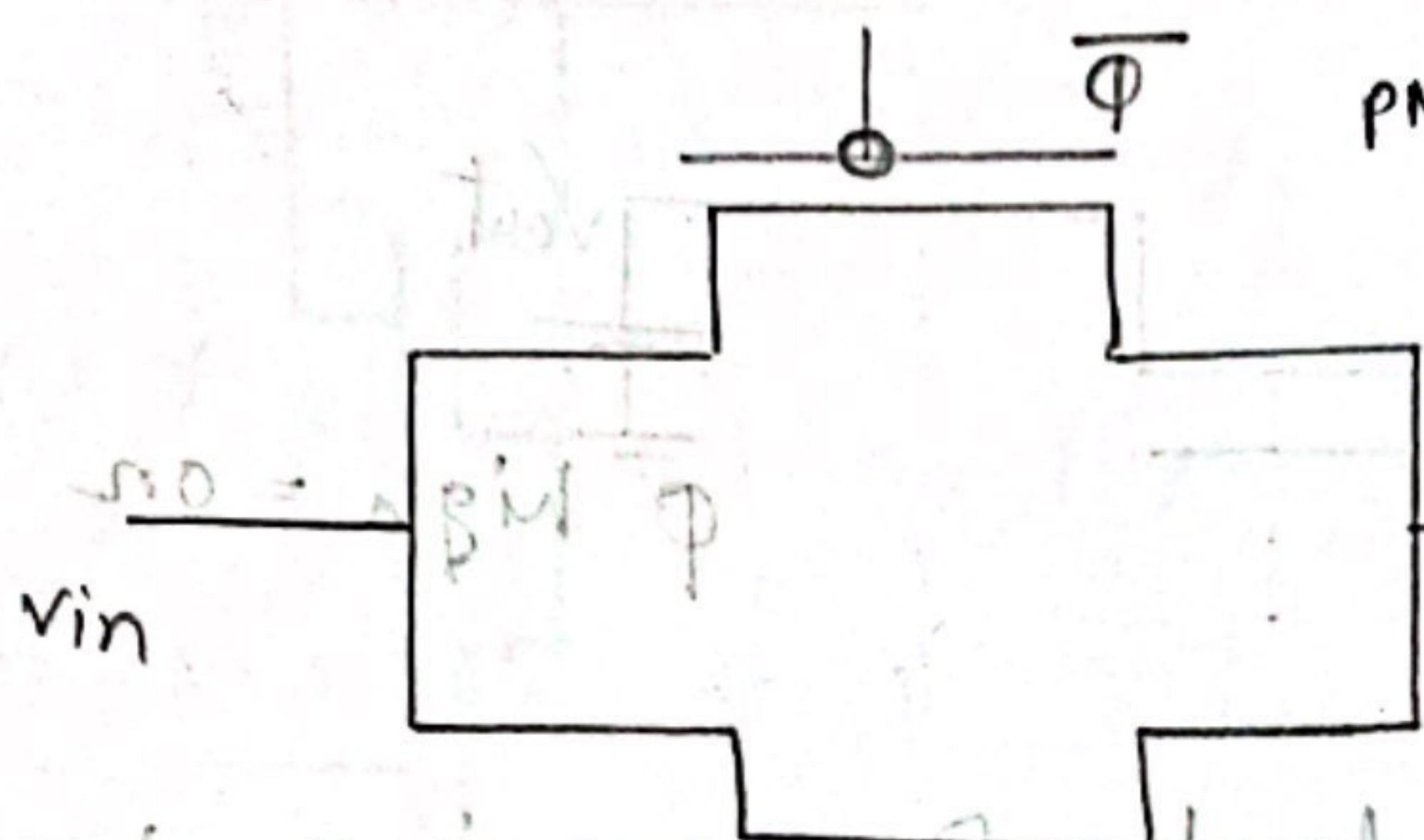
③ $v_{in} = \text{low}$, initial $v_{out} = \text{high}$ and final $v_{out} = \text{low}$ (pure)

Initial conditions: $v_{in} = 0$, $v_{out} = 1$

④ $v_{in} = \text{high}$, initial $v_{out} = \text{low}$ and final $v_{out} = \text{high}$ (pure)

Initial conditions: $v_{in} = 1$, $v_{out} = 0$

CMOS Pass Gate:



roheirenden 2019 - 2020

$\bar{\phi} = \text{low}$	off
$\bar{\phi} = \text{high}$	pass gate high
$\phi = \text{low}$	pass gate on
$\phi = \text{high}$	off

$$\begin{aligned} \bar{\phi} = 0, \bar{\phi}_{\text{PMOS}} = 1 & \Rightarrow \text{PMOS off} \\ \phi = 1, \bar{\phi}_{\text{NMOS}} = 0 & \Rightarrow \text{NMOS on} \end{aligned}$$

① $v_{in} = \text{high}$, initial $v_{out} = \text{high}$ (pure)
final $v_{out} = \text{high}$ (pure)

no current flow

② $v_{in} = \text{low}$, initial $v_{out} = \text{low}$
final $v_{out} = \text{low}$

③ $v_{in} = \text{low}$, initial $v_{out} = \text{high}$
final $v_{out} = \text{low}$ (pure)

④ $v_{in} = \text{high}$, initial $v_{out} = \text{low}$
final $v_{out} = \text{high}$ (pure)

2/05/23

Ratioed design

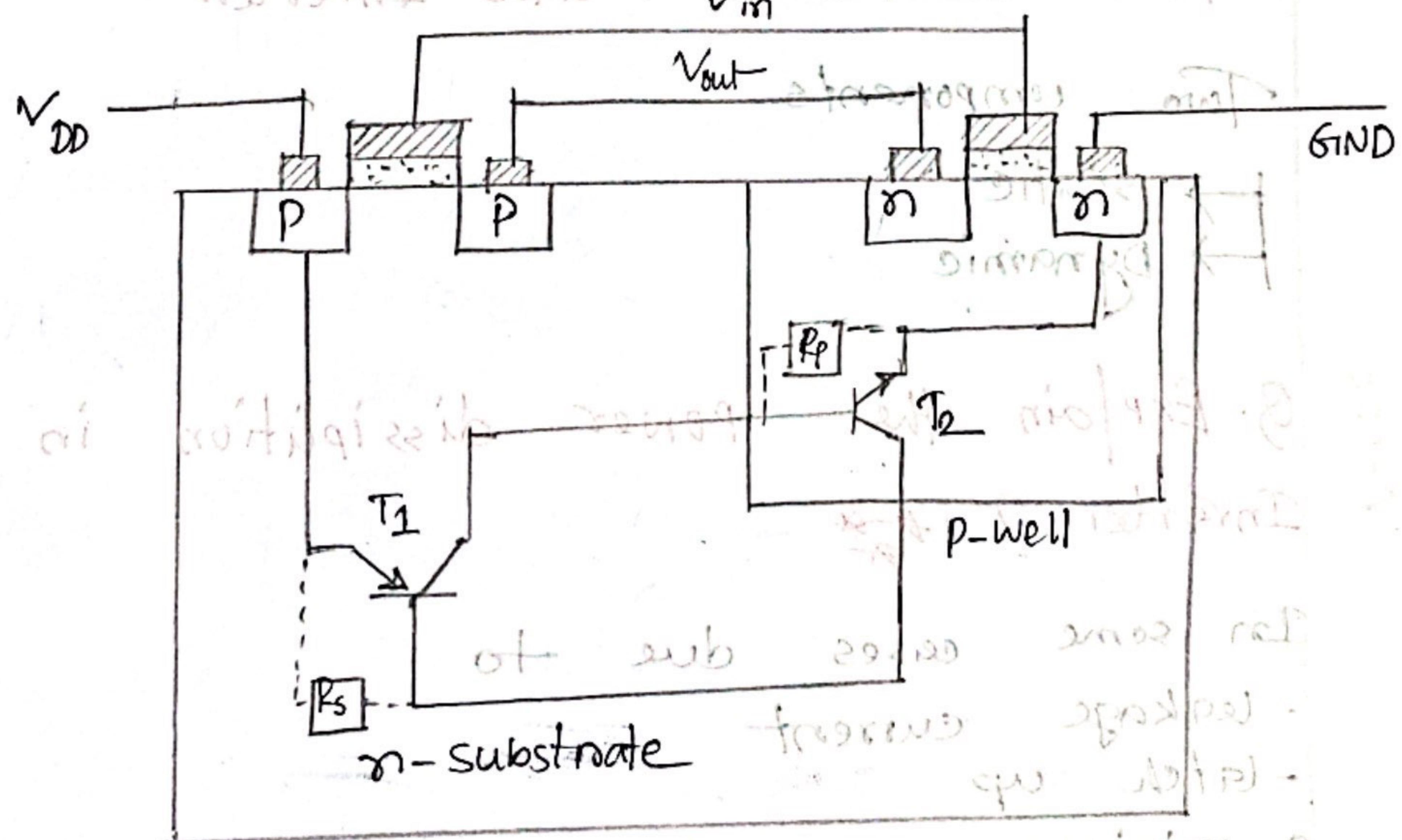
Ratioless design

Ratioed: (constant) load requirement

When V_{DD} and ground has direct connection and continuous power supply, it's ratioed design.

Ratioless: When load and driver are not connected at the same time.

Latch up in CMOS circuit (Pucknell)



- continuous power discharge due to leakage current → latch up current.

p-n-p
n-p-n

} Transistor for (Arrowhead) ~~bootstrapping~~

Q. What is barrier in p-N Junction?

How to stop latch up current?

- Increasing depletion region

- Increasing reverse bias

- Heavily doping n & p

(Hysteresis) theory COMS mi qu do toj ~~for~~

Power dissipation → CMOS Inverter

Two components

→ static

→ Dynamic

Q. Explain the power dissipation in CMOS Inverter ~~not q~~

In some cases due to

- leakage current

- latch up

A minimum amount of power consumption occurs in CMOS

Here comes static power dissipation

Another reason:

- Subthreshold phase

$$P_s = \sum_n^L \text{leakage current} \times \text{supply voltage}$$

Another reason:

- Subthreshold phase

$$P_s = \sum_n (\text{leakage current} \times \text{supply voltage})$$

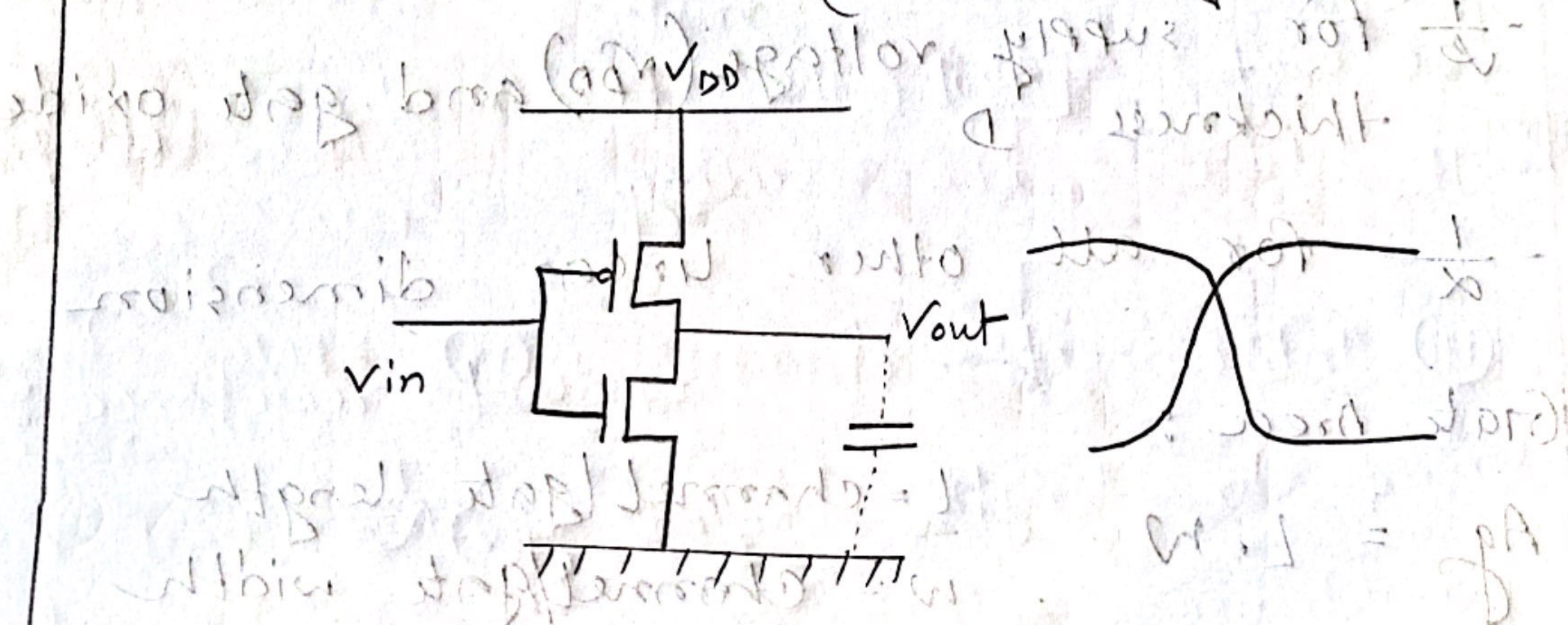
Dynamic power dissipation

from high to low/ low to high transition, it occurs.

Types: Two components:

→ Short circuit Power dissipation (for changing V_{in})

→ power dissipation during changing/discharge of the capacitor. (for changing V_{out})



$$\frac{1}{2} \times C \times \frac{V_{DD}}{2}$$

$$\frac{1}{2} \times C \times \frac{V_{DD}}{2}$$

$$\frac{1}{2} \times C \times \frac{V_{DD}}{2} = pA$$

$\frac{1}{2} \times C \times \frac{V_{DD}}{2} = pA$

Scaling:

Reducing feature size.

Scaling models:

1. Constant voltage scaling model

2. Constant electric field scaling model.

3. Combined voltage and dimension scaling model.

Two parameter:

- α (how much we're changing the size)

- $\beta \left(\frac{V_D}{\alpha} \frac{w}{L} \right)$

Scaling Rule:

- $\frac{1}{\sqrt{\alpha}}$ for supply voltage (V_{DD}) and gate oxide thickness D

- $\frac{1}{\alpha}$ for all other linear dimension

Gate Area:

$$A_g = L \cdot w$$

L = channel/gate length

w = channel/gate width

$$\frac{L \times \frac{1}{\alpha}}{\frac{L}{\alpha}} \quad \frac{w \times \frac{1}{\alpha}}{\frac{w}{\alpha}}$$

$$A_g = \frac{L \cdot w}{\alpha^2}$$

$$\text{Change in Scaling} = \frac{1}{\alpha^2}$$

Gate Capacitance per unit area: $C_A = \epsilon_0 \frac{V}{d}$

$$C_o = \frac{\epsilon_{ox}}{D}$$

Permeability of oxide layer.

$$\frac{\varepsilon_{ox}}{D} = \frac{\varepsilon_{ox}}{D} \times b^b \quad \text{or} \quad \text{Deposition}$$

C is scaled by β

Gate capacitance vs concentration (1)

$\text{Eg} = \text{Co} \times \text{Ag}$

Cg is scaled by $\frac{V}{\alpha r}$

Q. What do you mean by scaling?

8. Models of scaling?

g. Find out how Ag, C, Cg is scaled?

Limitation on Scaling :

① If voltage is scaled down the built in (V_0) potential becomes comparable to $V_{dd} \frac{\lambda^3}{\lambda^2} = \frac{\lambda^3}{\lambda} = \frac{V_0}{\lambda}$

(of P-n junction) $\rightarrow 0.2 V$ was ignored before as V_{dd} was high.

② Limitation of process technology from consideration of alignment accuracy & resolution of photolithography technology.
minimum size of a layer we can make if the feature size is so small that we can't control the PR hardness anymore. It limits the scaling.

③ Interconnect of conduct resistance:

conductor length scaled by $\frac{1}{\alpha}$

Resistance scaled by α .

It is decreased by $\frac{1}{\alpha}$

IR drop remains same.

⑭ Subthreshold current increase as $(V_{GS} - V_t)$ magnitude compared to $\frac{kT}{q}$ decrease

$$I_{sub} \propto e^{-\left(\frac{V_{GS} - V_t}{kT/q}\right)}$$

⑮ Decrease inter feature spacing and greater switching speed result in noise problem.

Because of mutual capacitance / mutual inductance induce cross talk. External noise such as rf signal, voltage spike also have more dominant effect.

⑯ Increased current density requires consideration of metal interconnects as they may get burned.

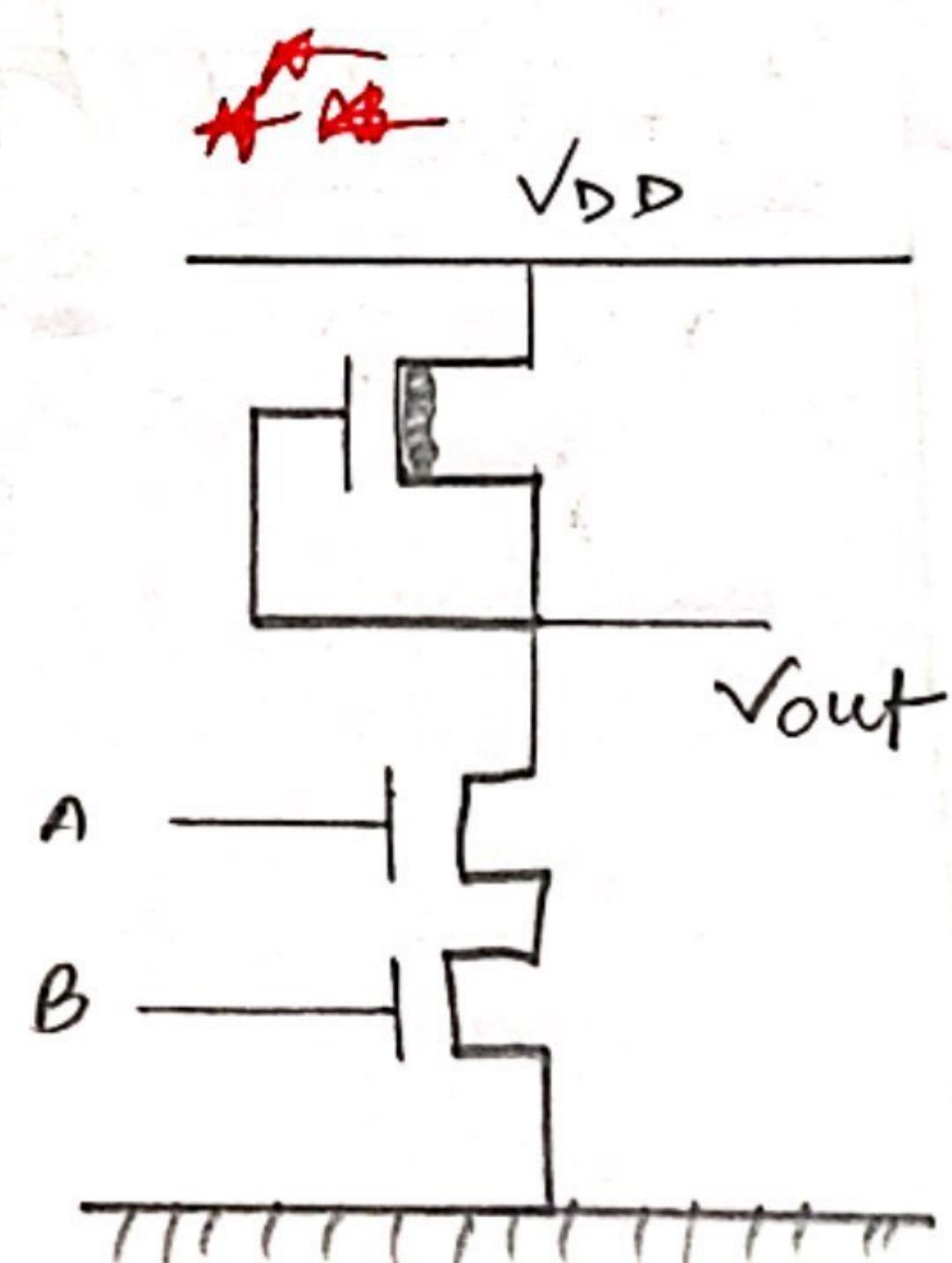
Sub System Design :

2 input NAND gate:

NMOS \rightarrow

load \rightarrow depletion type NMOS

Driver \rightarrow change



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

$$\left(\frac{V_{DD} - 2BV}{D + A} \right) \rightarrow$$

abutting point

so sure

CMOS \rightarrow

better noise reduction method

exists in these two prints

V_{DD}

Input voltage representation

Lowest state A → Nmos conduct

High state B → PMOS conduct

Efficiency V_{out} V_{DD}

Best in state A → Nmos conduct

Best in state B → PMOS conduct

Efficiency V_{out} V_{DD}

Best in state A → Nmos conduct

Best in state B → PMOS conduct

Efficiency V_{out} V_{DD}

Best in state A → Nmos conduct

Best in state B → PMOS conduct

Efficiency V_{out} V_{DD}

for designing CMOS:

→ Number of NMOS and PMOS are same

→ Input of NMOS and PMOS are same

→ NMOS and PMOS alternative manner

NMOS - Series
PMOS - Parallel

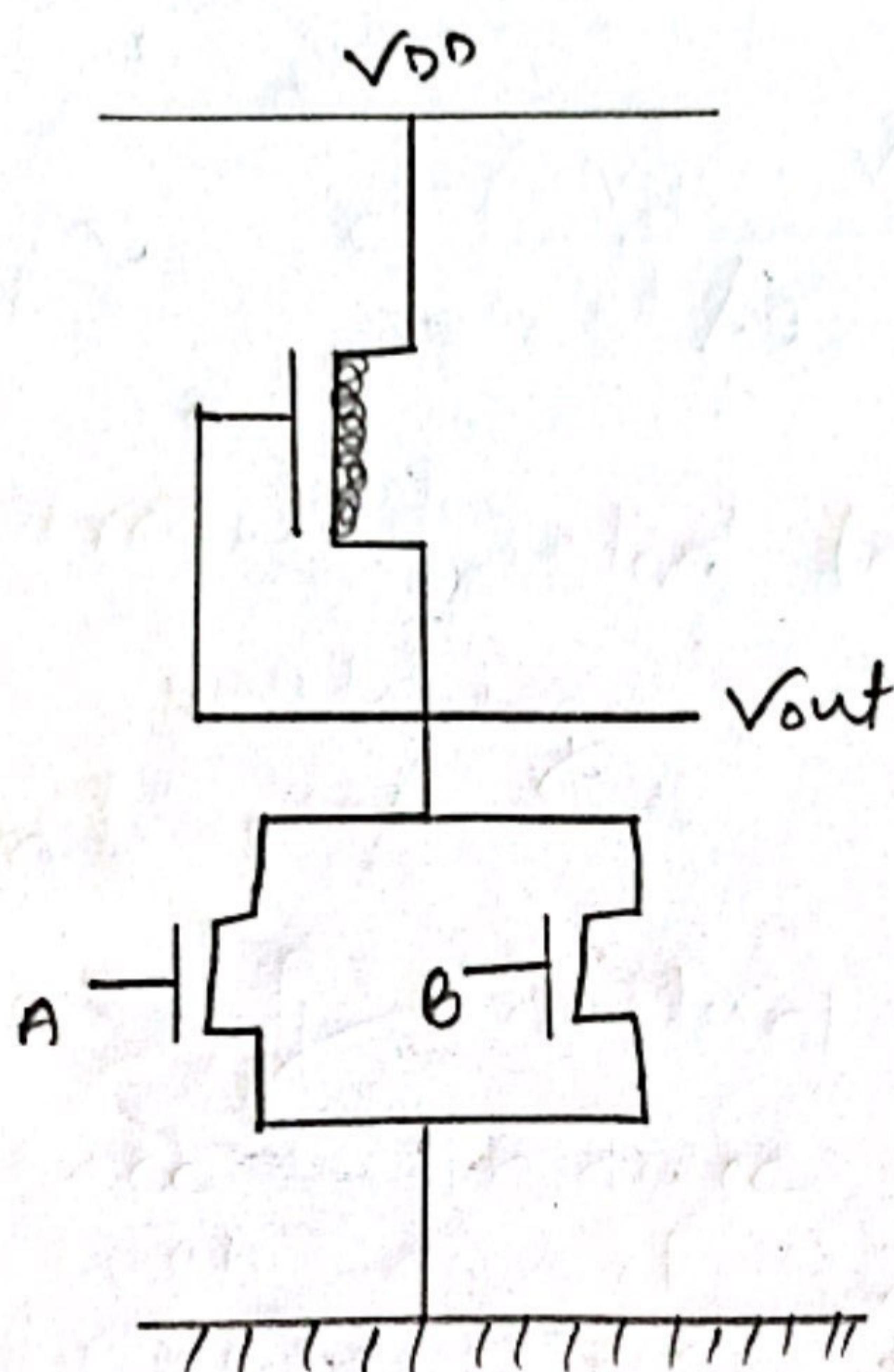
versa

→ PMOS \rightarrow load

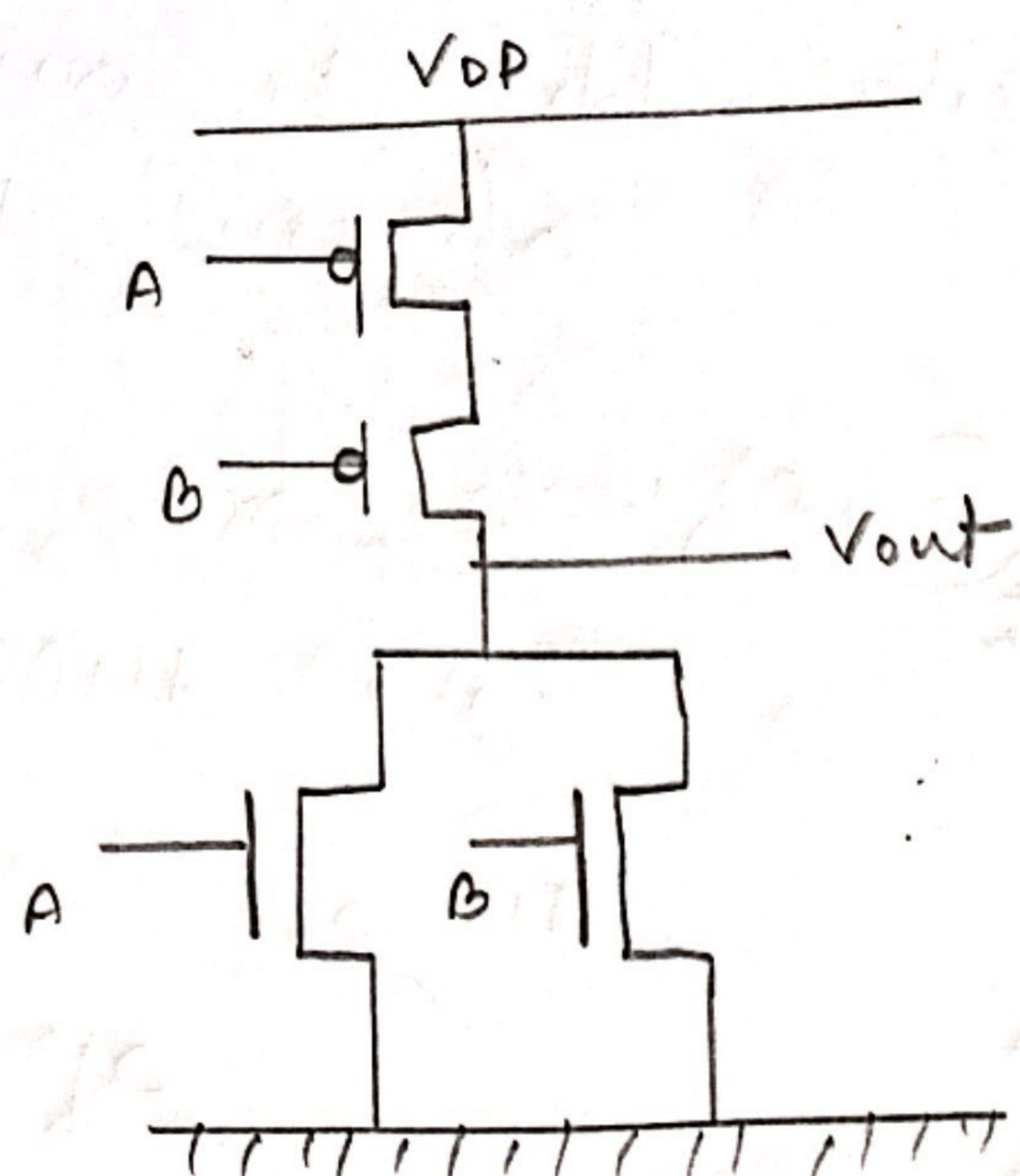
NMOS \rightarrow driver.

→ Output will be taken from intersection of PMOS and NMOS

2 input NOR Gate
NMOS \rightarrow

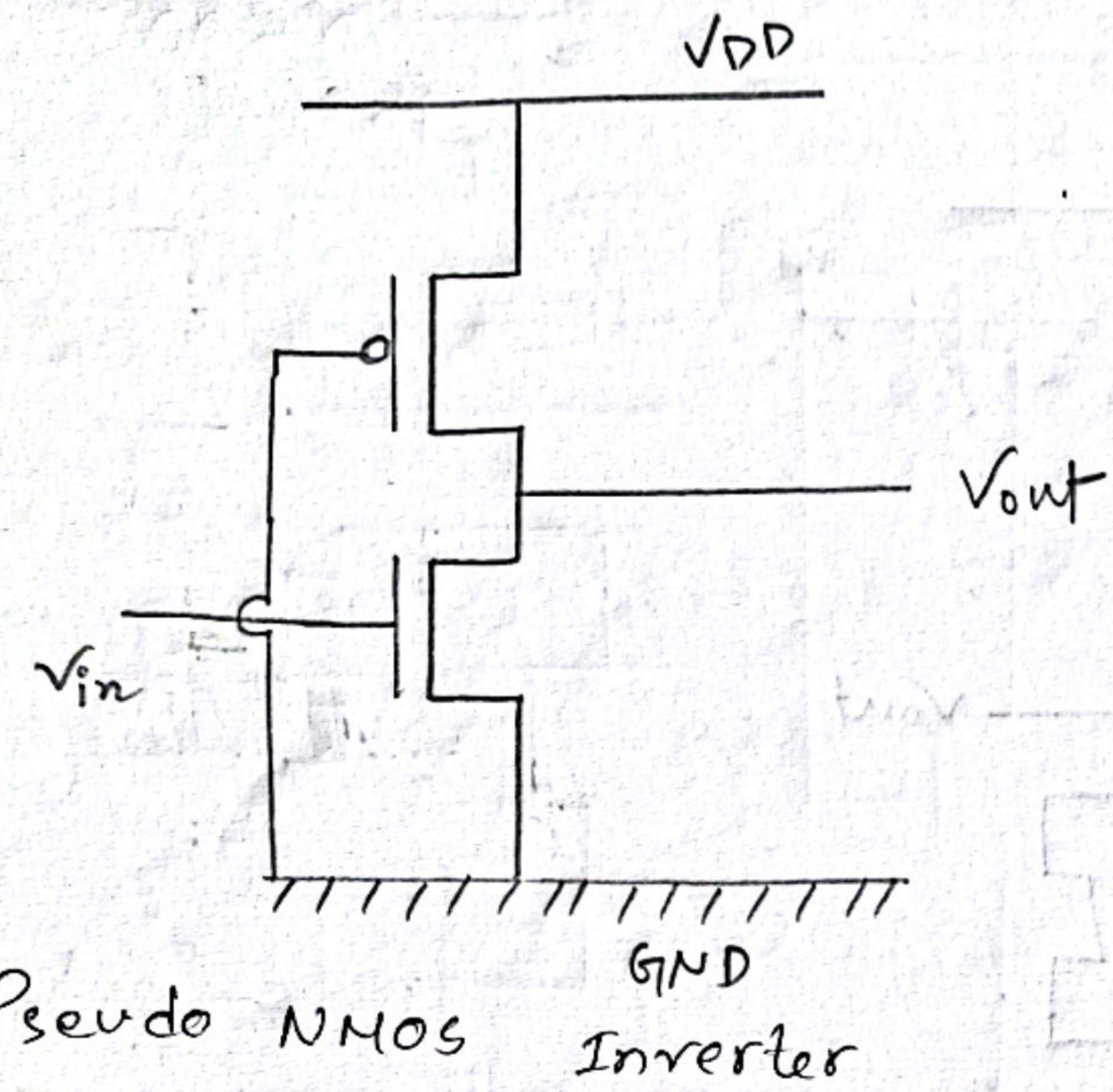


CMOS \rightarrow



15-05-23

Pseudo NMOS logic



$$\underline{V_{in} = \text{low}}$$

PMOS = on

NMOS = off

$V_{out} = \text{high}$

$$\underline{V_{in} = \text{high}}$$

PMOS = on

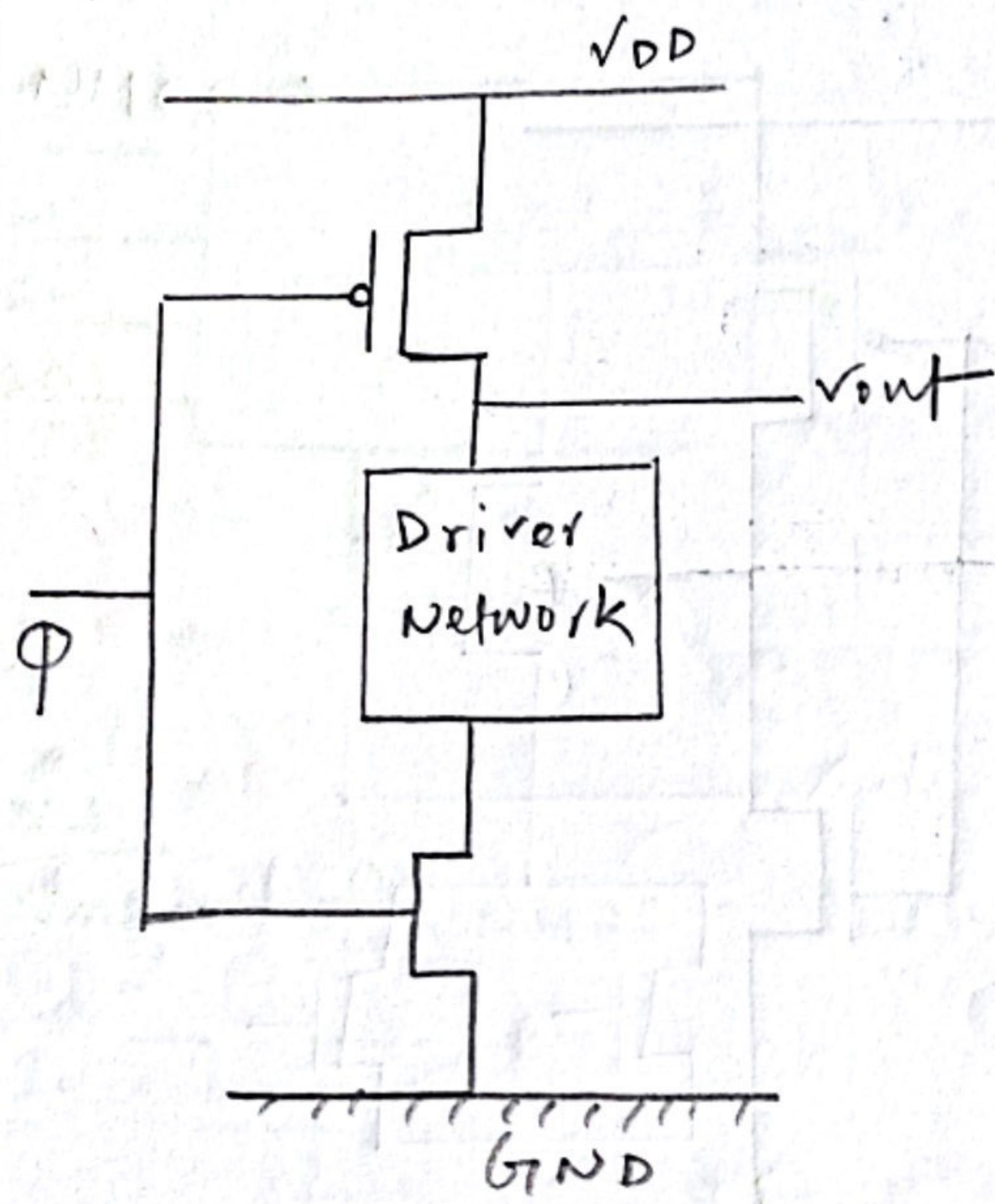
NMOS = on

$V_{out} = \text{low}$

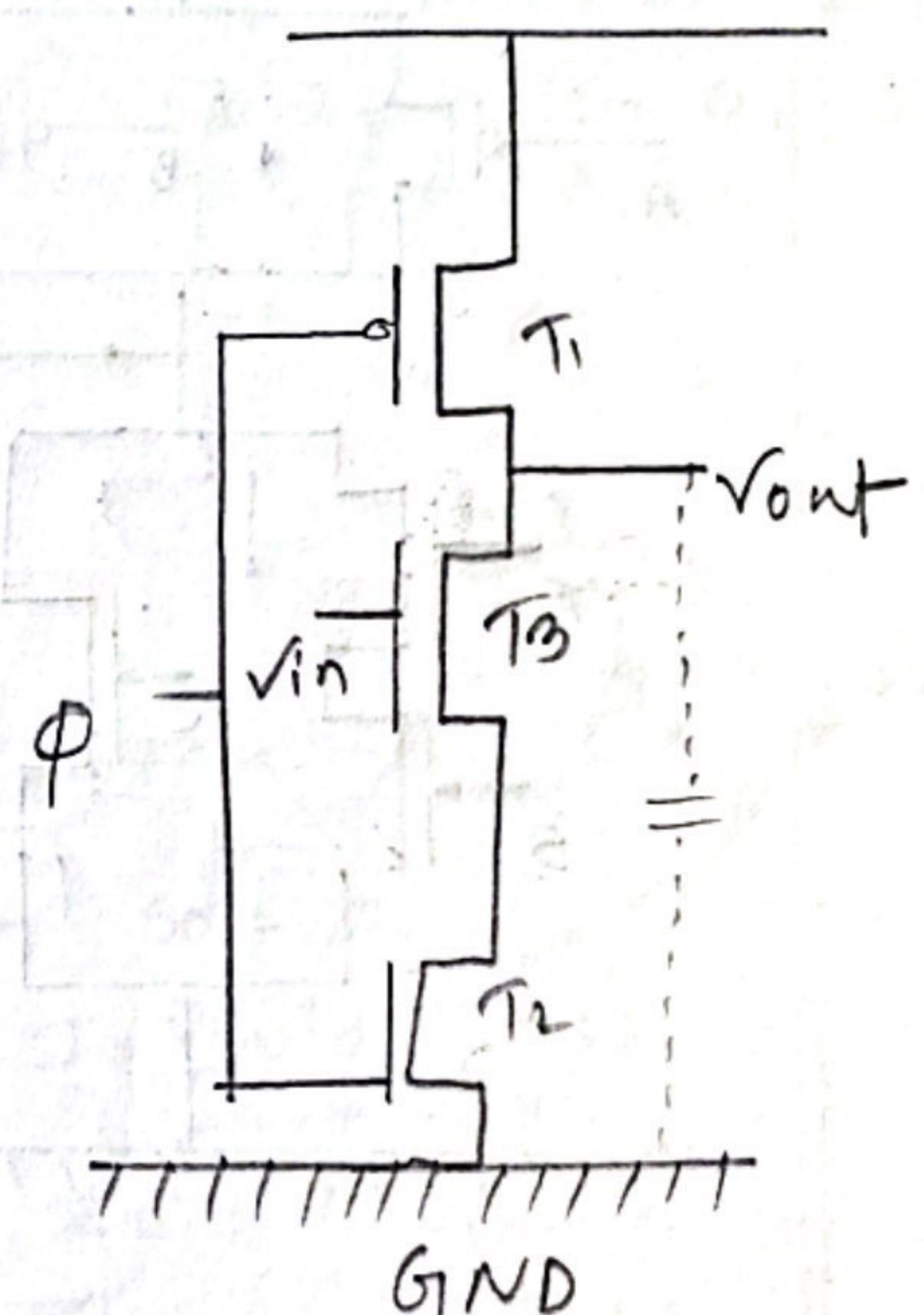
Pseudo NMOS Inverter

Q. Draw NAND or NOR using Pseudo NMOS Inverter.

Dynamic CMOS logic:



Dynamic CMOS Inverter:



Q. Draw an inverter using Dynamic CMOS logic?

- NAND

- NOR

) $\phi = \text{low}$ $\phi = \text{high}$
Precharge $T_1 = \text{on}$ $T_1 = \text{off}$
On State $T_2 = \text{off}$ $T_2 = \text{on}$
 $v_{out} = \text{high}$ Evaluation State

$v_{in} = \text{low}$

$T_3 = \text{off}$

$v_{out} = \text{high}$

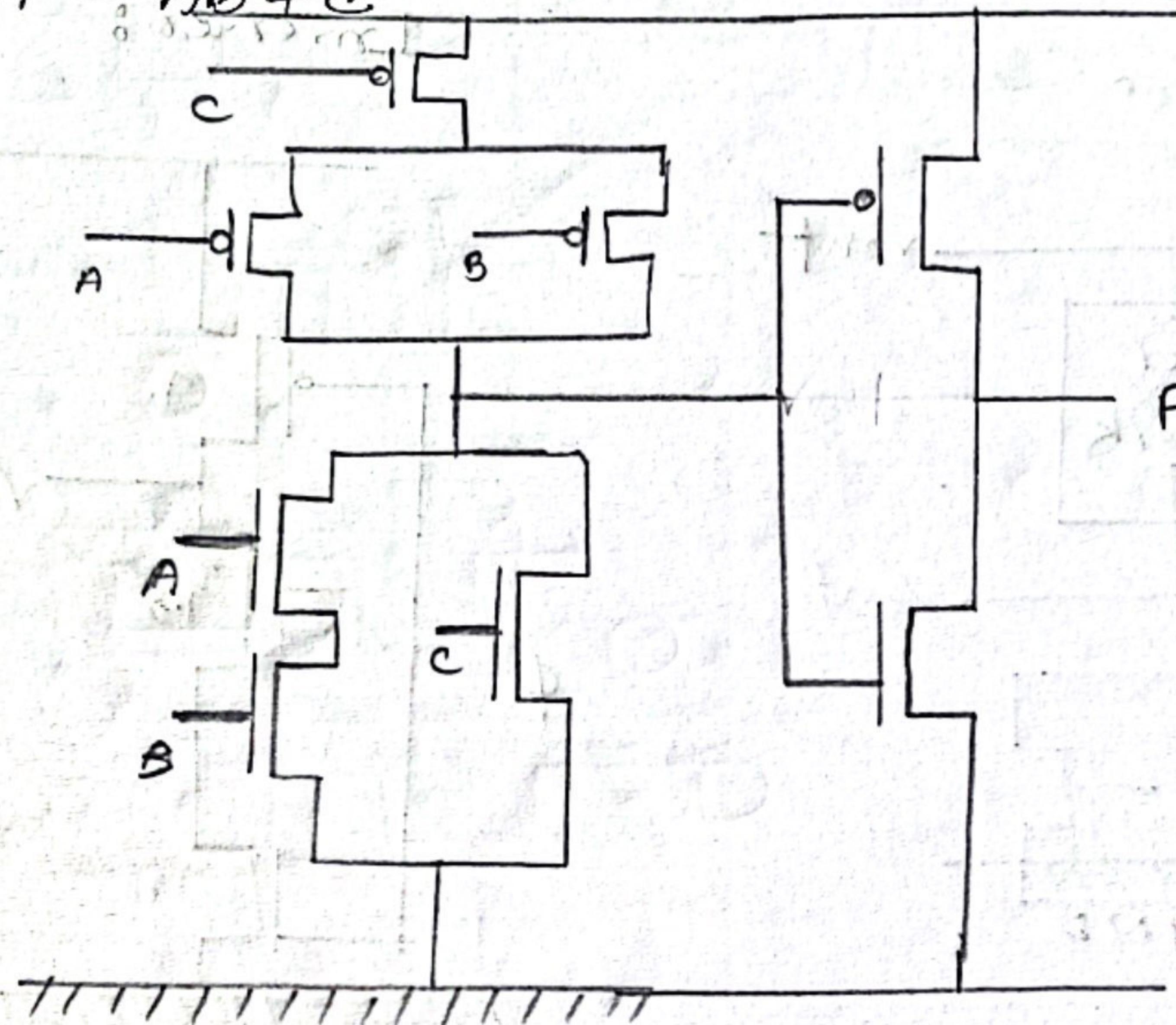
$v_{in} = \text{high}$

$T_3 = \text{on}$

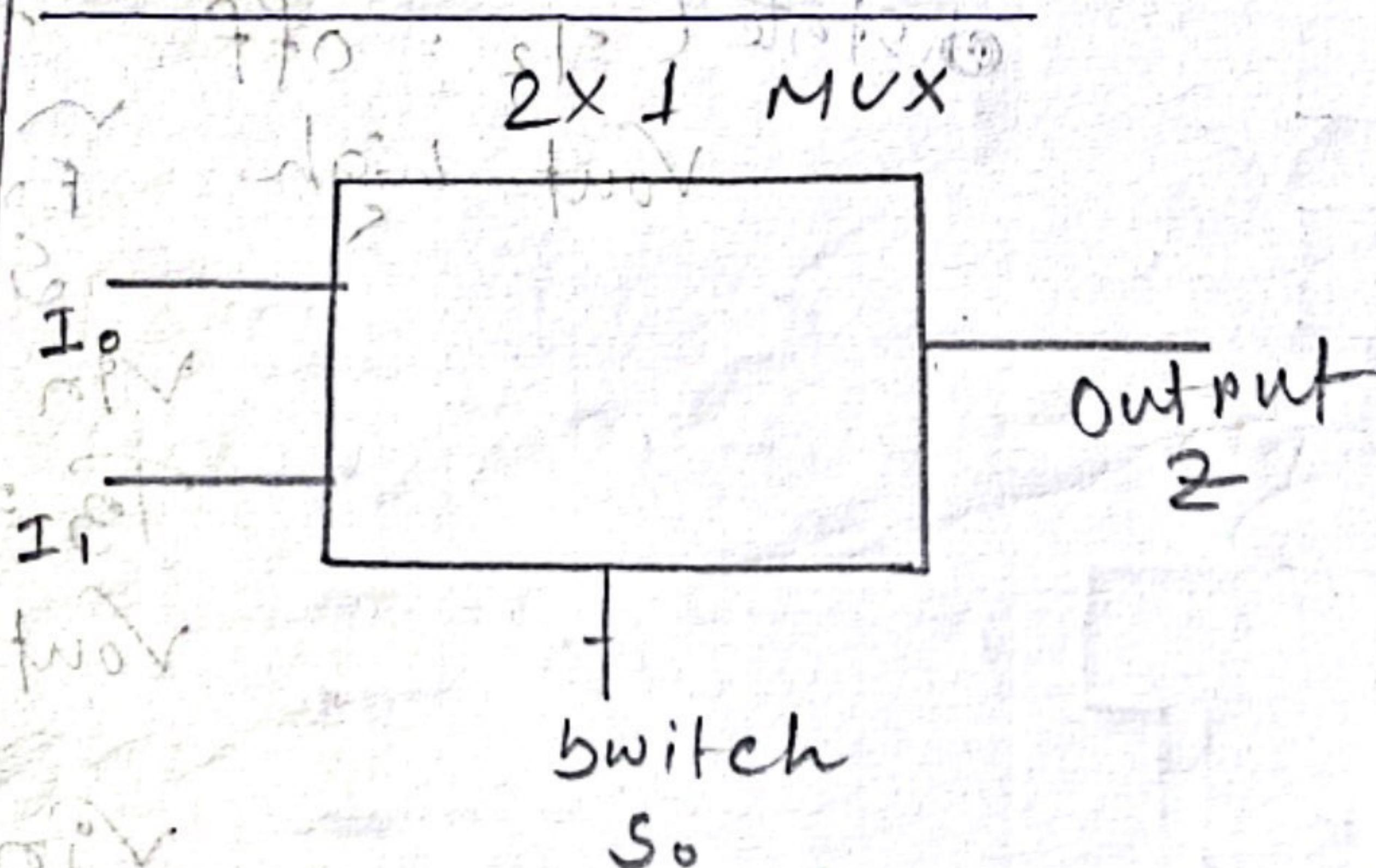
$v_{out} = \text{low}$

Complex CMOS Design (VVI for final)

$$F = AB + C$$



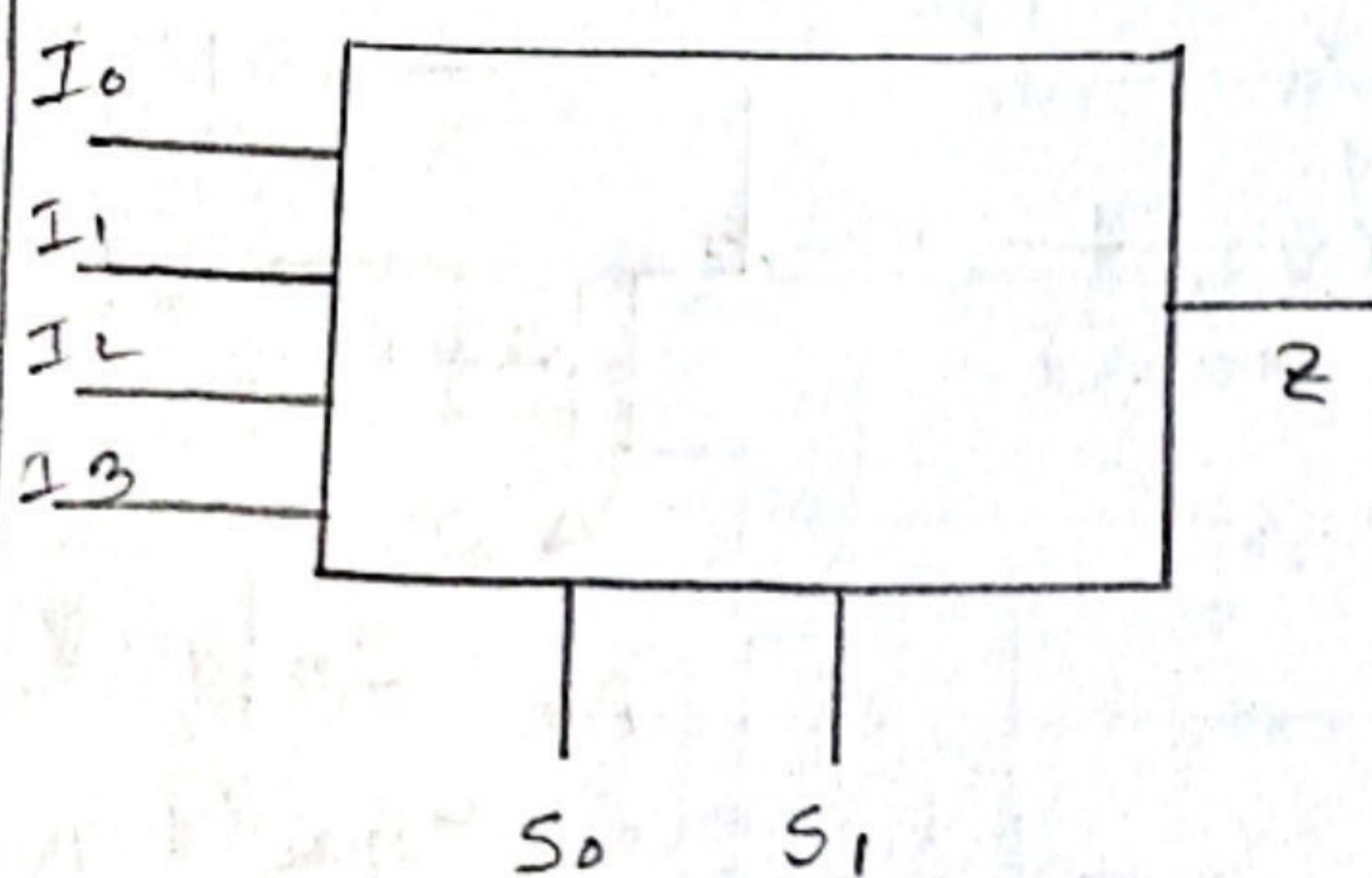
Multiplexer (MUX):



S	Z
0	I ₀
1	I ₁

$$Z = \bar{S}_0 I_0 + S_0 I_1$$

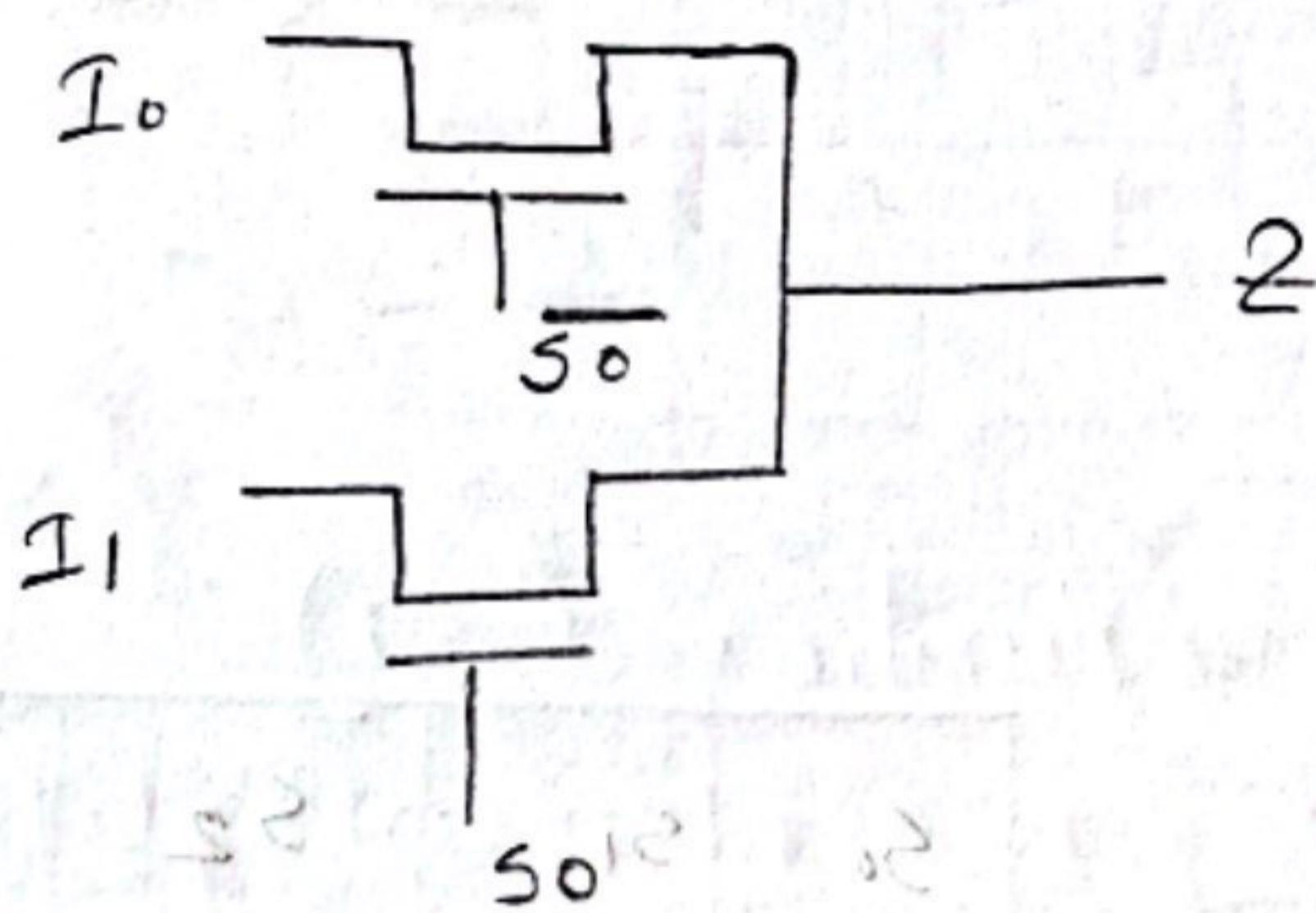
4x1 MUX



$$Z = \overline{S_0} \overline{S_1} I_0 + S_0 \overline{S_1} I_1 + \overline{S_0} S_1 I_2 + S_0 S_1 I_3$$

2x1

Number of NMOS = Input \times switch



When $S_0 = 0$

I_0 will pass

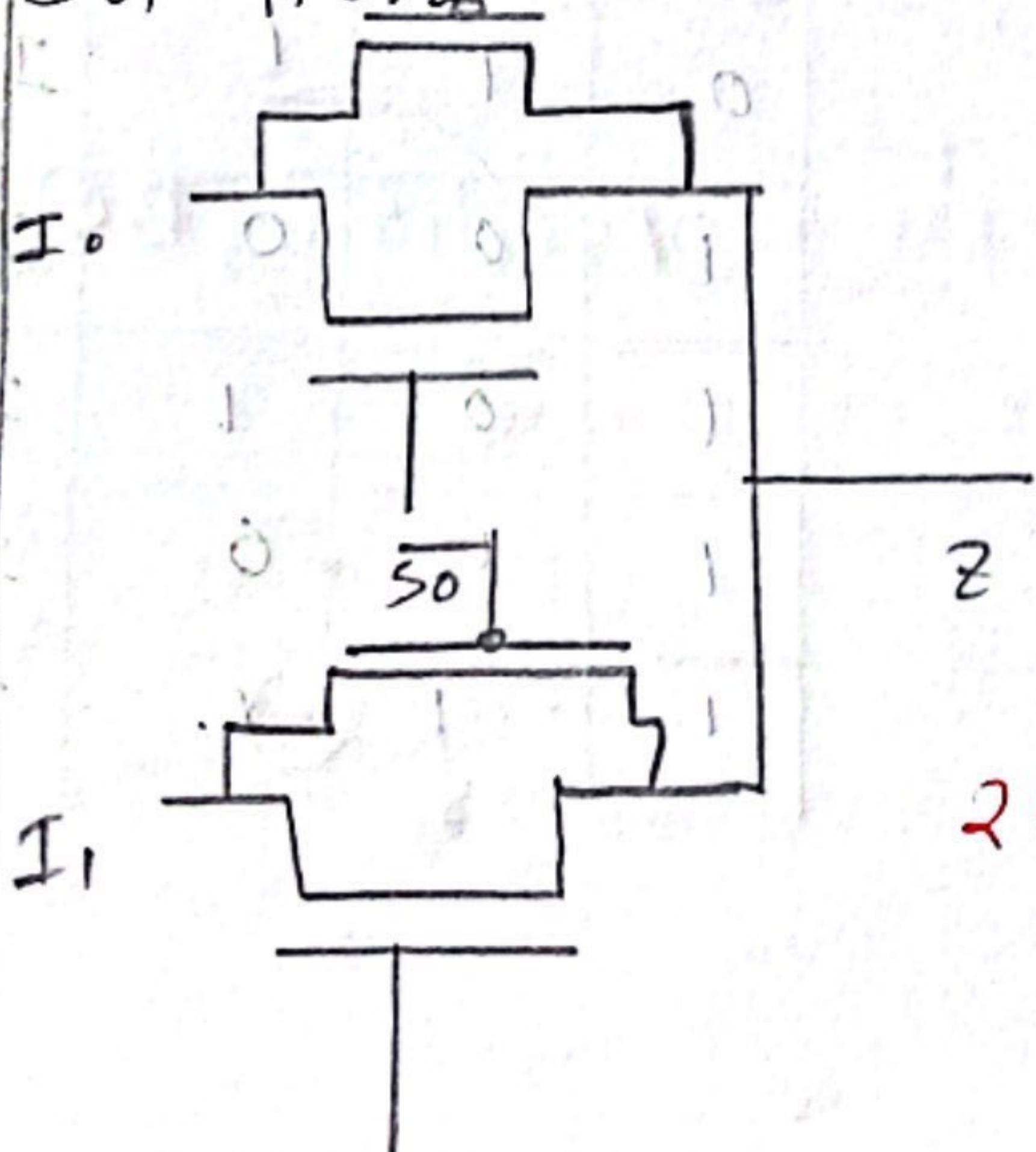
$S_0 = 1$

I_1 will pass

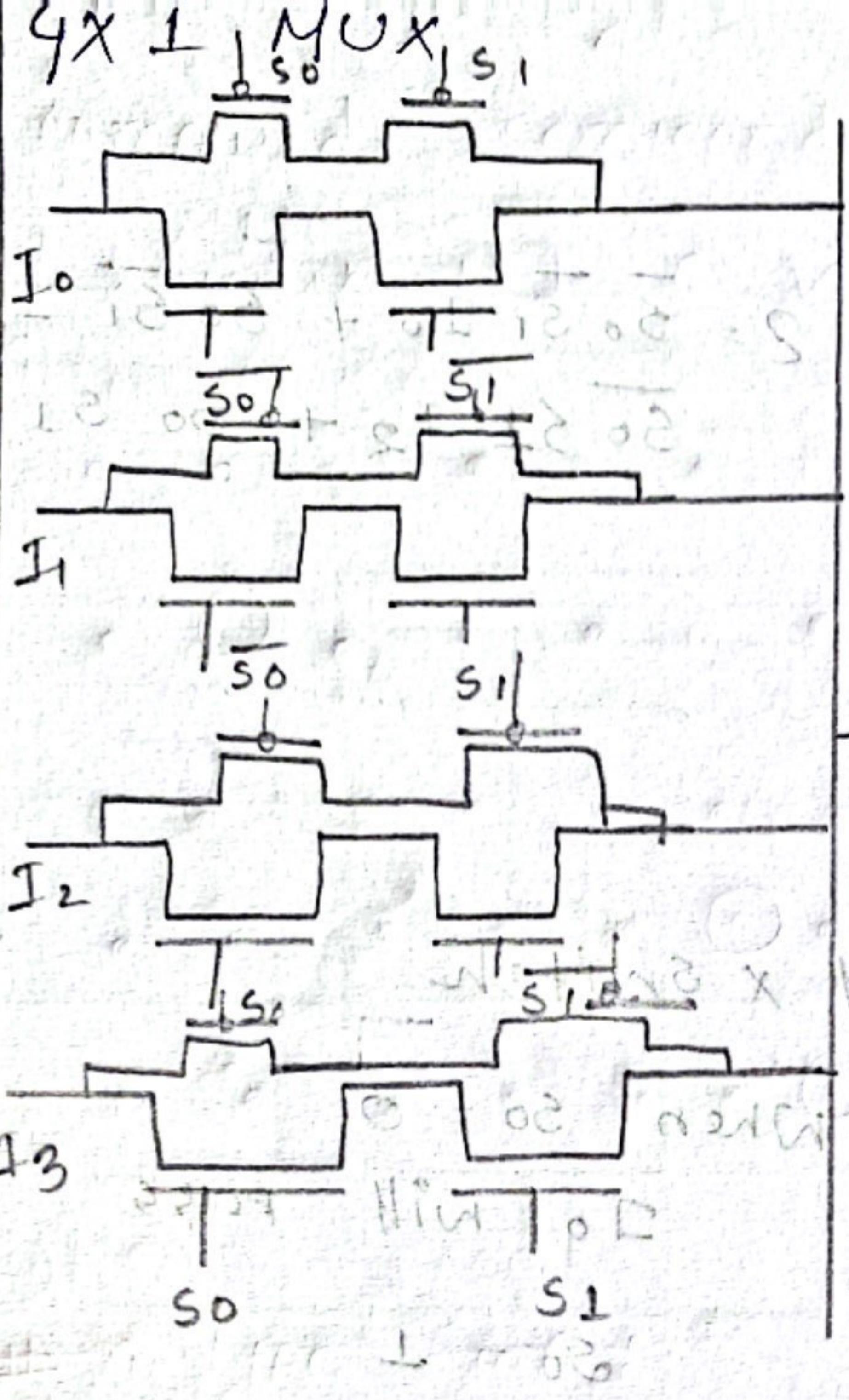
Disadvantage:

- Logic level low cannot pass I_0 (0 might, " " high " " " " " ")

Solution



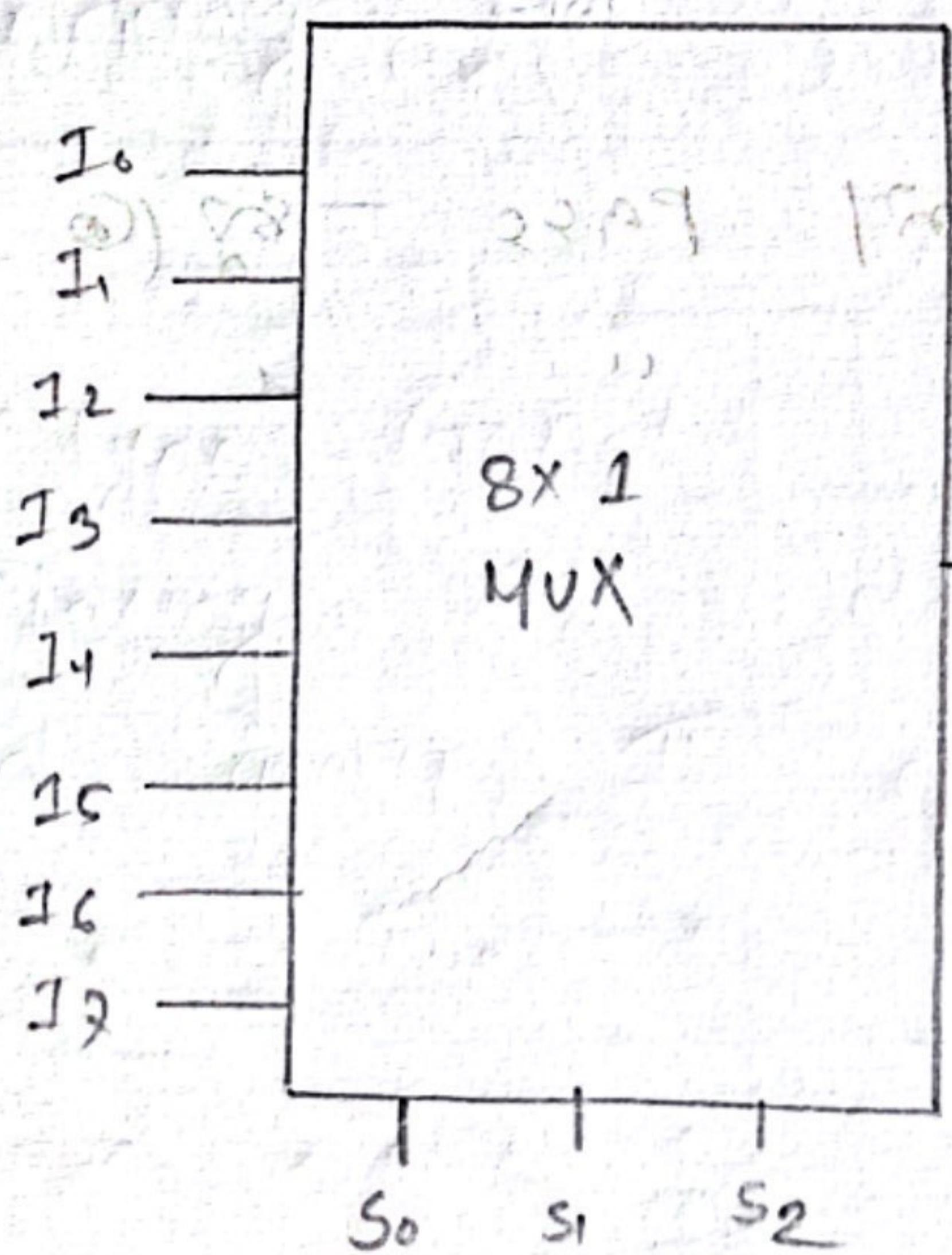
2x1 MUX using CMOS logic



Z

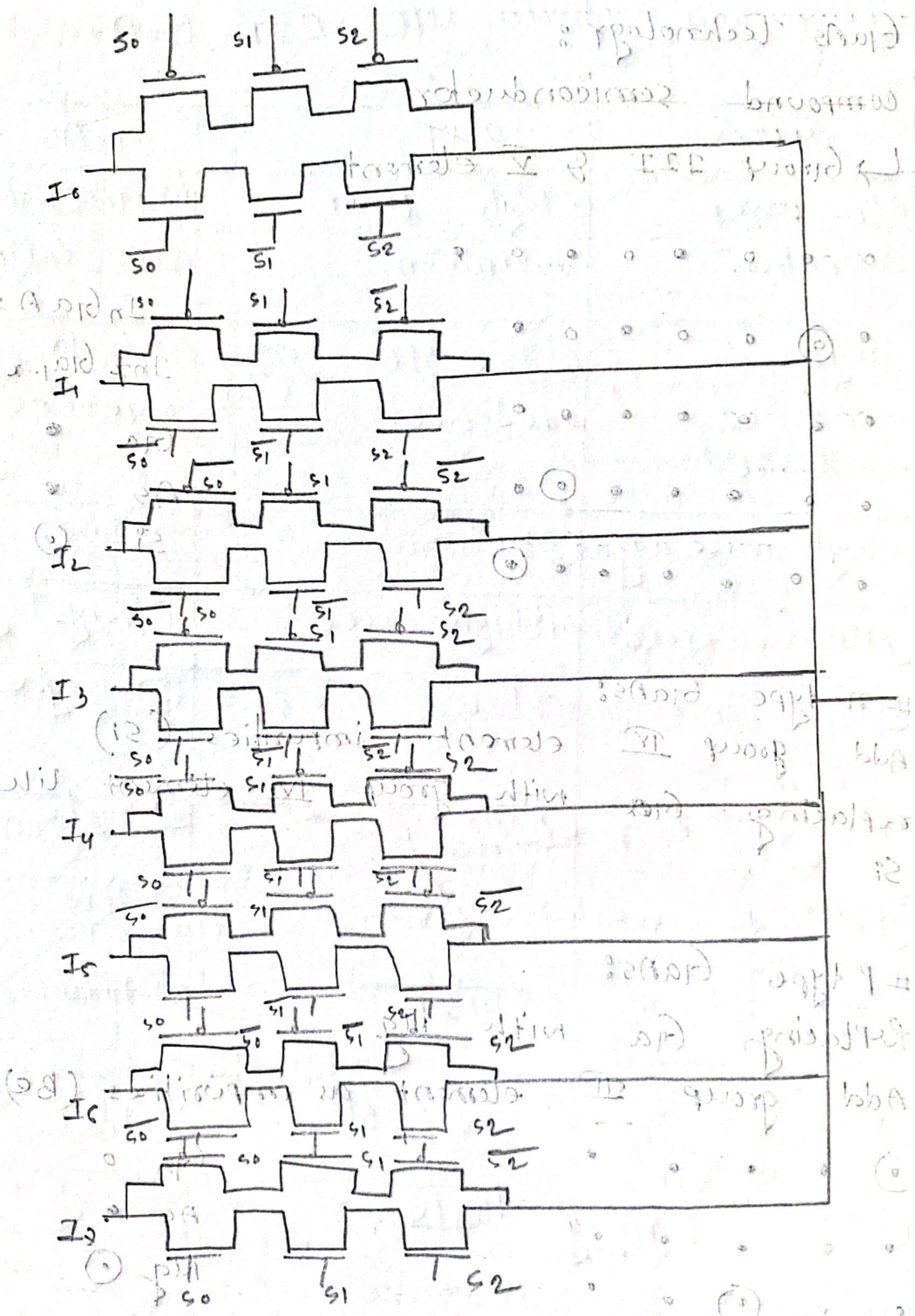
$W_{AB} = 2.0 \mu m$ for random

HW



8×1 MUX

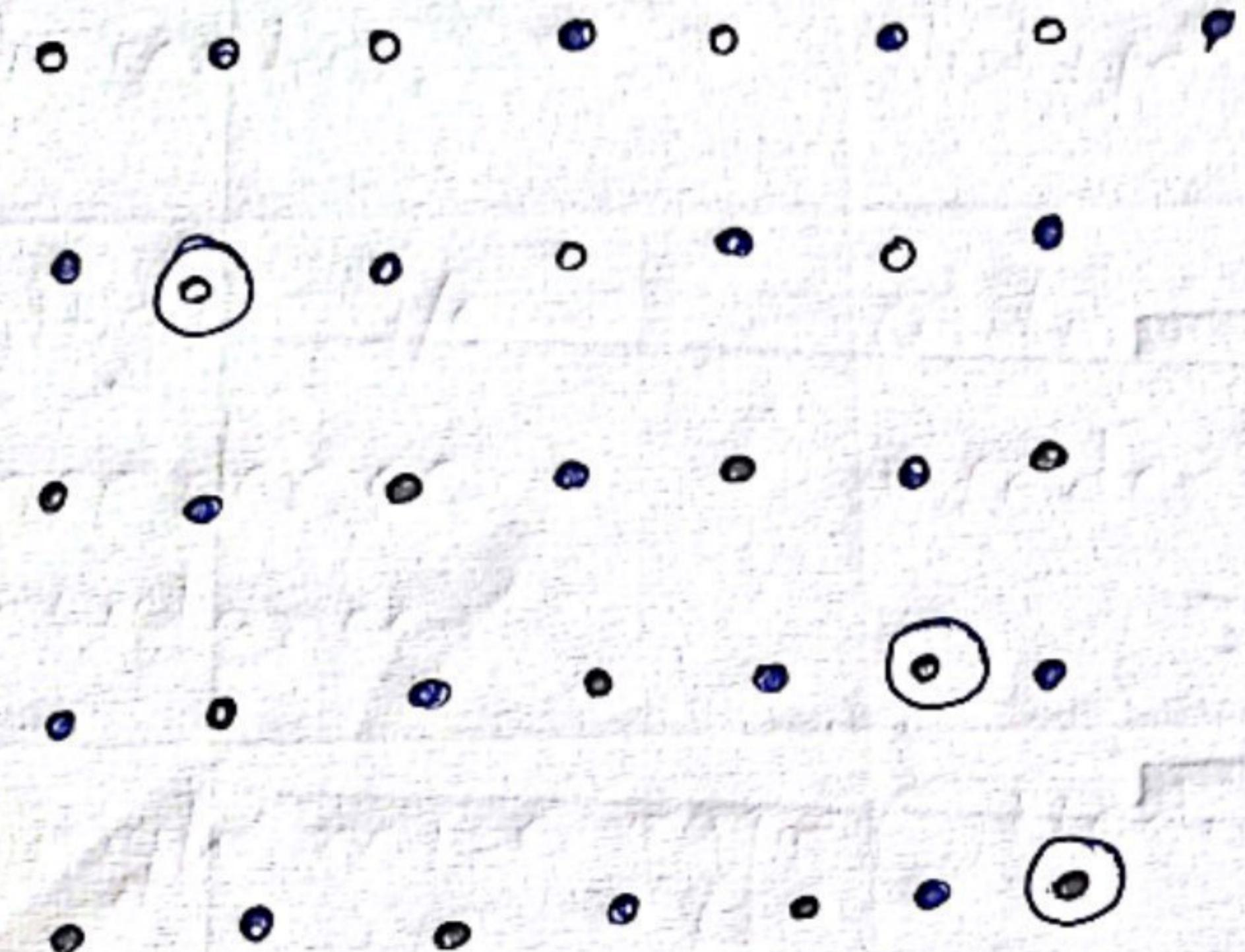
S_0	S_1	S_2	S_3
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7



GaAs Technology:

compound semiconductor

↳ Group III & V element



InGaAs

$In_x Ga_{1-x} As_y P_{1-y}$

Ga

As

Si

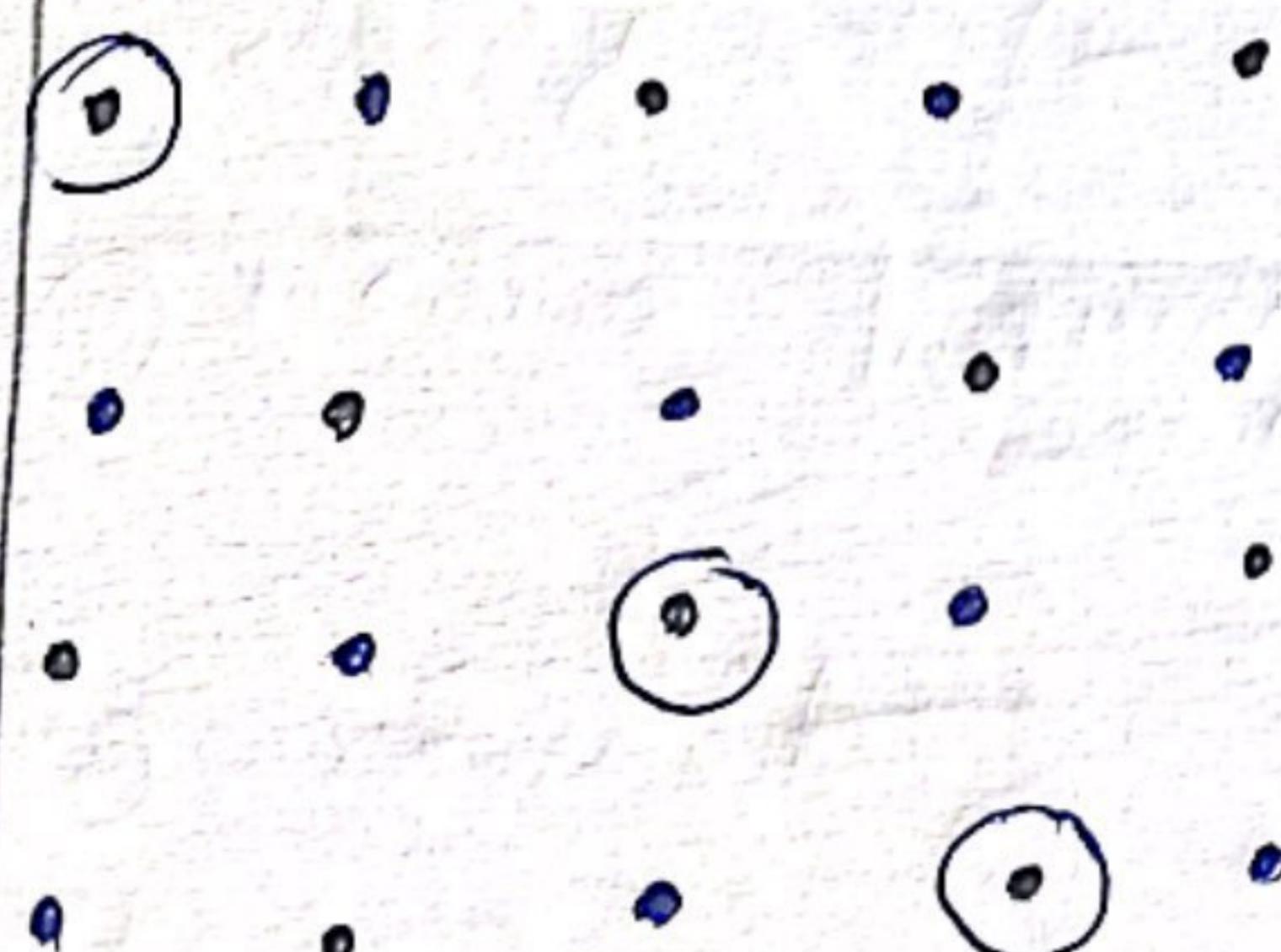
n-type GaAs:

Add group IV element impurities (Si)
replacing Ga with group IV element like
Si

P type GaAs:

Replacing Ga with Mg.

Add group II element as impurities (Be/Mg)



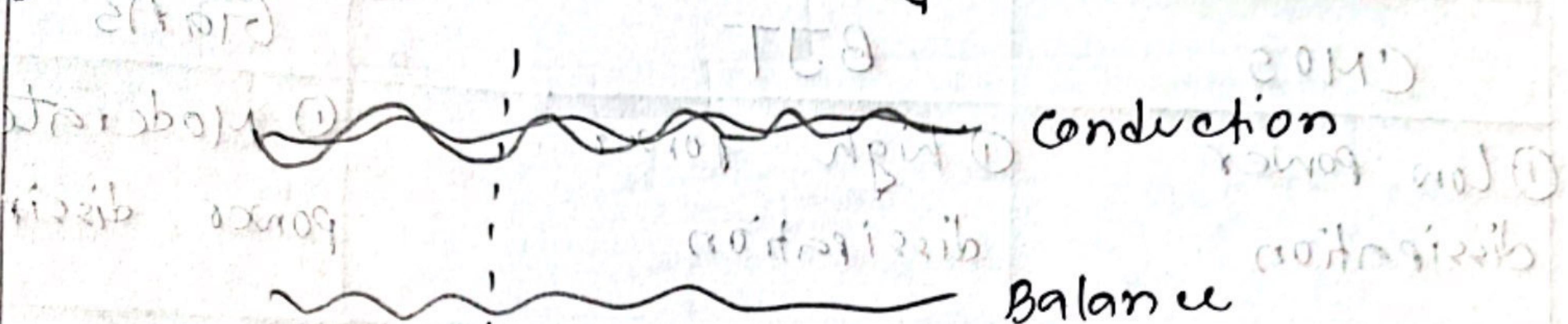
Ga

As

Mg

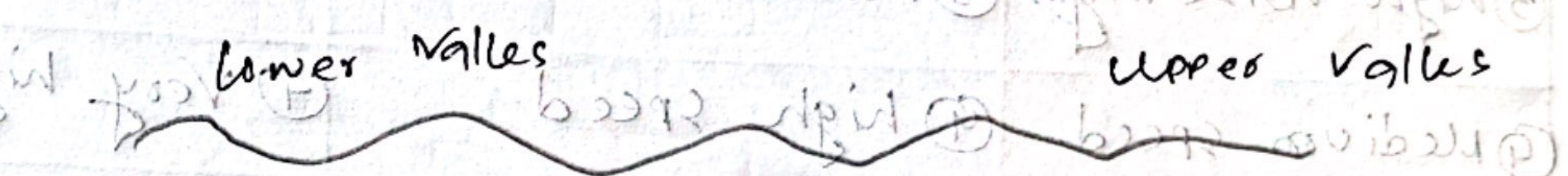
#Advantage: TCO + eOMD (bottom emission)
+ CVD

① GaAs is a direct bandgap semiconductor.



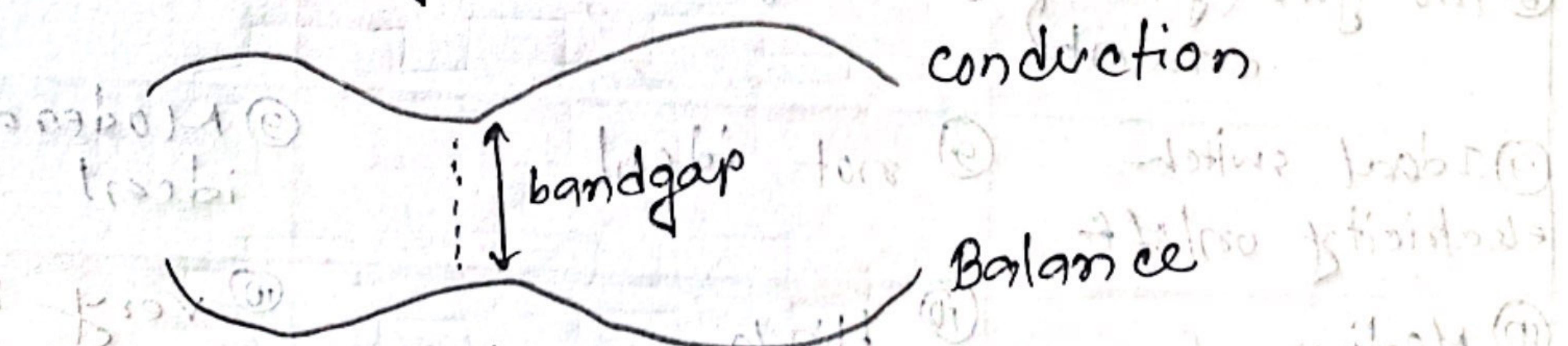
Radiation recombination is possible

② GaAs is a material's semiconductor. Upper
valley/lower Valleys



- lower resistance
- lower effective mass
- higher mobility
- more current / faster current

③ GaAs offers higher bandgap than silicon
semiconducting property.



- ④ lower percolation
- ⑤ allows easier electrical isolation of multiple devices
- ⑥ widen operating temperature range - 200°C to +200°C

comparison between CMOS, BJT, GaAs

CMOS	BJT	GaAs
① low power dissipation	① high power dissipation	① Moderate power dissipation
② High i/o impedance (resistance)	② low i/o impedance.	② high i/o impedance.
③ high noise margin	③ Medium	③ low
④ Medium speed	④ high speed	④ Very high speed
⑤ High Tracking density	⑤ low	⑤ high
⑥ High delay sensitivity had	⑥ low	⑥ high
⑦ Output drive low.	⑦ high	⑦ low.
⑧ low gm (gate current)	⑧ high	⑧ low
⑨ Ideal switch electricity on/off	⑨ not ideal	⑨ moderately ideal
⑩ Medium frequency	⑩ High	⑩ very high
⑪ Indirect bandgap	⑪ Indirect	⑪ Direct