CSE 4207 CT 4 Assignment
Roll No: 1903118

Assignment Problem: Combinational (ALU Op) + FSM Circuit using Verilog + Synthesis using 130nm Skywater PDK with OpenLane toolchain
Category: C
Word Size = 5 Bits
ALU Operations = XOR & ROR

Solution:
https://drive.google.com/file/d/1T-JGRSbyM76HUGAIoZIkAshH8jjWYLEv/view?usp=sharing
Video:
https://drive.google.com/file/d/1AYszy3tefUZkbTqrNzXDf1Pht8vkVW_b/view?usp=sharing

Have you uploaded the video?	YES
Check List 1: Have you explained the design using testbenches to prove that your circuit is working correctly and giving correct results?	YES
Check List 2: Have you shown full synthesis results showing all the required info including RTL Synthesis, RTL Floorplan, RTL Power Analysis, GDS and Heatmap (for details, see assignment template doc)?	YES
NB: Failing to upload video will cause heavy point penalty (5-6 Marks)	
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

HDL Code:

Check List: Have you added all the modules written in verilog including ALU, ALU_OP1, ALU_OP2, CONTROLLER, TOP, TOP_TESTBENCH, ALU_TESTBENCH, CONTROLLER_TESTBENCH?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

`top.v`

```
module top(
    input wire clk, reset, start,
    output wire [4:0] R,
    output wire ZF);

wire [4:0] fsm_A, fsm_B;
wire op;
```

```
FSM fsm(
            .clk(clk),
            .reset(reset),
            .start(start),
            .A(fsm_A),
            .B(fsm_B),
            .op(op));

ALU alu(
            .A(fsm_A),
            .B(fsm_B),
            .op(op),
            .R(R),
            .ZF(ZF));

endmodule
```

FSM.v

```
module FSM(
          input wire clk, reset, start,
          output reg [4:0] A,B,
          output reg op);


          reg [4:0] pstate, nstate;
                parameter [4:0] START = 5'b00000,
                    ONE = 5'b00001,
                    TWO = 5'b00010,
                    THREE = 5'b00011,
                    FINISH = 5'b00100;



               always @(*) begin : NSOL
                    begin : NSL
                         case(pstate)

                              START : nstate = start ? ONE :
START;

                              ONE  : nstate = TWO;

                              TWO : nstate = THREE;

                              THREE : nstate = FINISH;
```

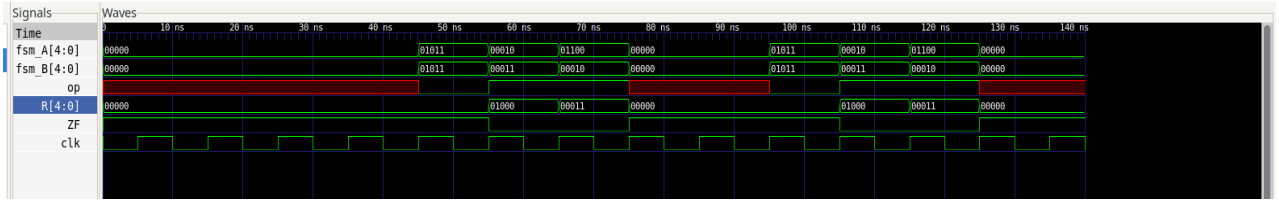
```
                    FINISH : nstate = START;

                    default : nstate = 5'bx;

            endcase
    end

        begin : OL
       case(pstate)

                     START : begin
                     A = 5'b00000;
                     B = 5'b00000;
                    op = 1'bx;
                       end

                ONE : begin
                    A = 5'b01011;
                    B = 5'b01011;
                    op = 1'b0;
                       end

                     TWO : begin
                    A = 5'b00010;
                    B = 5'b00011;
                    op = 1'b1;
                       end

                THREE  : begin
                    A = 5'b01100;
                    B = 5'b00010;
                    op = 1'b1;
                       end

                FINISH  : begin
                    A = 5'b00000;
                             B = 5'b00000;
                             op = 1'bx;

                       end


                default : begin
                             A = 5'bx;
                    B = 5'bx;
                             op = 1'bx;
                          end
```

```
                        endcase
                    end
                end

            always @(posedge clk or negedge reset) begin :
PSR
                    begin
                        if(~reset) begin
                          pstate <= START;
                        end

                       else begin
                          pstate <= nstate;
                    end
                end
            end

endmodule
```

RTL Timing Diagram:

Check List: Have you added all the timing diagrams of ALU_TESTBENCH, CONTROLLER_TESTBENCH, TOP_TESTBENCH?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

`Top_tb.v -> gtkwave`



RTL Synthesis (130nm Skywater PDK with OpenLane toolchain):

Check List: Have you added *RTL synthesis summary*, *RTL synthesized design figure* and *Standard cell usage in synthesized design*?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

RTL synthesis summary

top.v -> stat.rpt

Metrics	Count
Number of wires:	18
Number of wire bits:	22
Number of public wires:	11
Number of public wire bits:	15
Number of ports:	5
Number of port bits:	9
Number of memories:	0
Number of memory bits:	0
Number of processes:	0
Number of cells:	19

Breakdown of stat.rpt

=== top ===

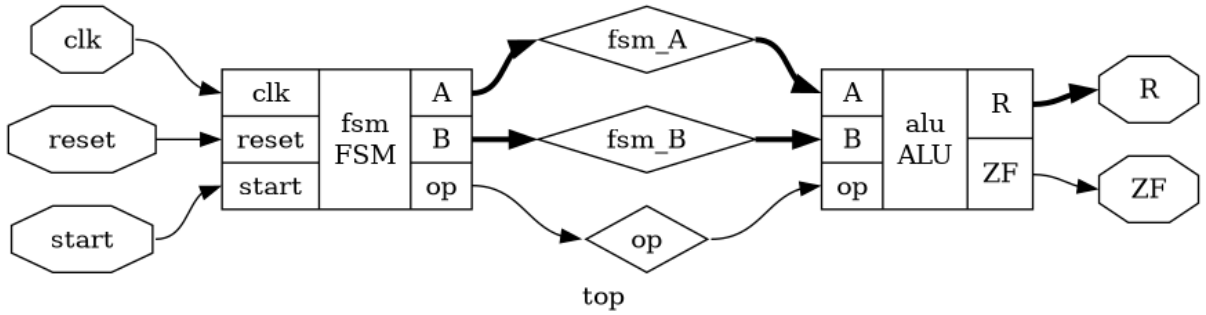
Number of wires:	8
Number of wire bits:	20
Number of public wires:	8
Number of public wire bits:	20
Number of ports:	5
Number of port bits:	9
Number of memories:	0
Number of memory bits:	0
Number of processes:	0
Number of cells:	2
ALU	1
FSM	1

```
=== FSM ===

   Number of wires:                 43
   Number of wire bits:            103
   Number of public wires:           8
   Number of public wire bits:      24
   Number of ports:                  6
   Number of port bits:             14
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 26
     $adff                           1
     $eq                            15
     $logic_not                      3
     $mux                            1
     $not                            2
     $pmux                           4

=== ALU_XOR ===

   Number of wires:                  4
   Number of wire bits:             20
   Number of public wires:           3
   Number of public wire bits:      15
   Number of ports:                  3
   Number of port bits:             15
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                  1
     $xor                            1

=== ALU_ROR ===

   Number of wires:                 10
   Number of wire bits:             34
   Number of public wires:           3
   Number of public wire bits:      15
   Number of ports:                  3
   Number of port bits:             15
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
```

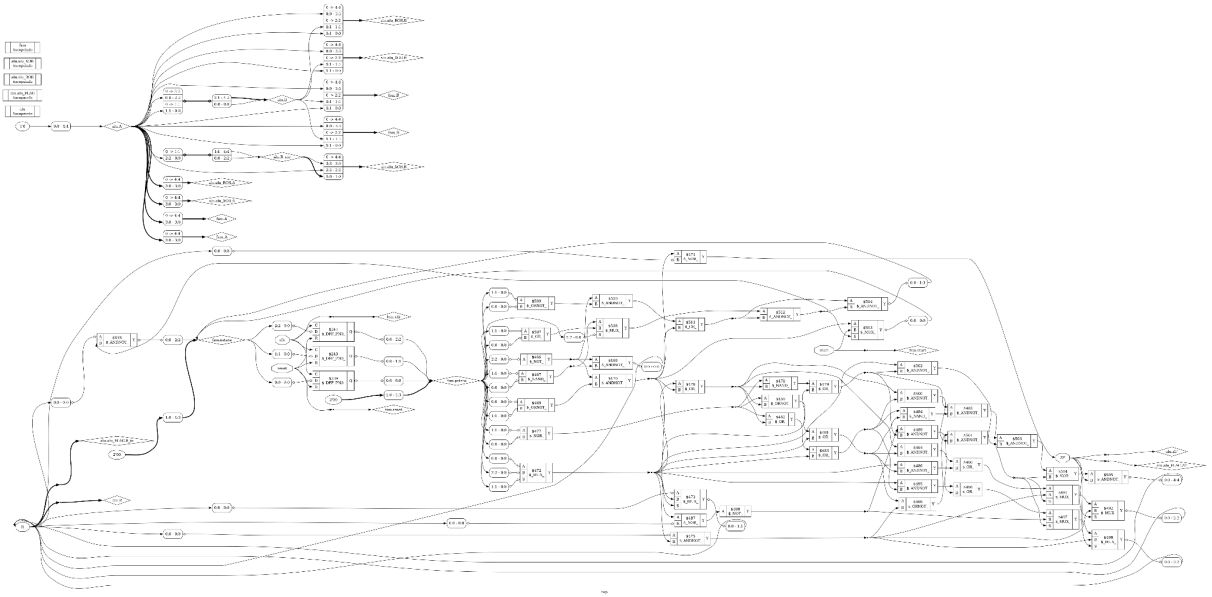
```
   Number of cells:                 5
     $eq                            4
     $pmux                          1

=== ALU_FLAG ===

   Number of wires:                 4
   Number of wire bits:             8
   Number of public wires:          2
   Number of public wire bits:      6
   Number of ports:                 2
   Number of port bits:             6
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 2
     $logic_not                     1
     $mux                           1

=== ALU ===

   Number of wires:                16
   Number of wire bits:            64
   Number of public wires:          8
   Number of public wire bits:     32
   Number of ports:                 5
   Number of port bits:            17
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 5
     $mux                           2
     ALU_FLAG                       1
     ALU_ROR                        1
     ALU_XOR                        1
```

RTL synthesized design figure

hierarchy.dot



primitive_techmap.dot



Standard cell usage in the synthesized design

sky130_fd_sc_hd__and3_2	3
sky130_fd_sc_hd__buf_2	3
sky130_fd_sc_hd__conb_1	2
sky130_fd_sc_hd__dfrtp_2	3
sky130_fd_sc_hd__inv_12	1
sky130_fd_sc_hd__nand2_2	1
sky130_fd_sc_hd__nand2_4	1
sky130_fd_sc_hd__nor2_2	2
sky130_fd_sc_hd__o21a_4	1
sky130_fd_sc_hd__o221a_4	1
sky130_fd_sc_hd__xnor2_2	1

RTL Floorplan (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added RTL Floorplan info?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 50.0 50.0 (µm).
[INFO] Floorplanned on a core area of 5.52 10.88 44.16 38.08 (µm).
Writing metric design__die__bbox: 0.0 0.0 50.0 50.0
Writing metric design__core__bbox: 5.52 10.88 44.16 38.08
Setting global connections for newly added cells…
[INFO] Setting global connections...
Updating metrics…

Cell type report:	Count	Area (µm)
Buffer	3	15.01
Inverter	1	16.27
Sequential cell	3	**78.83**
Multi-Input combinational cell	12	**111.36**
Total	19	**221.46**

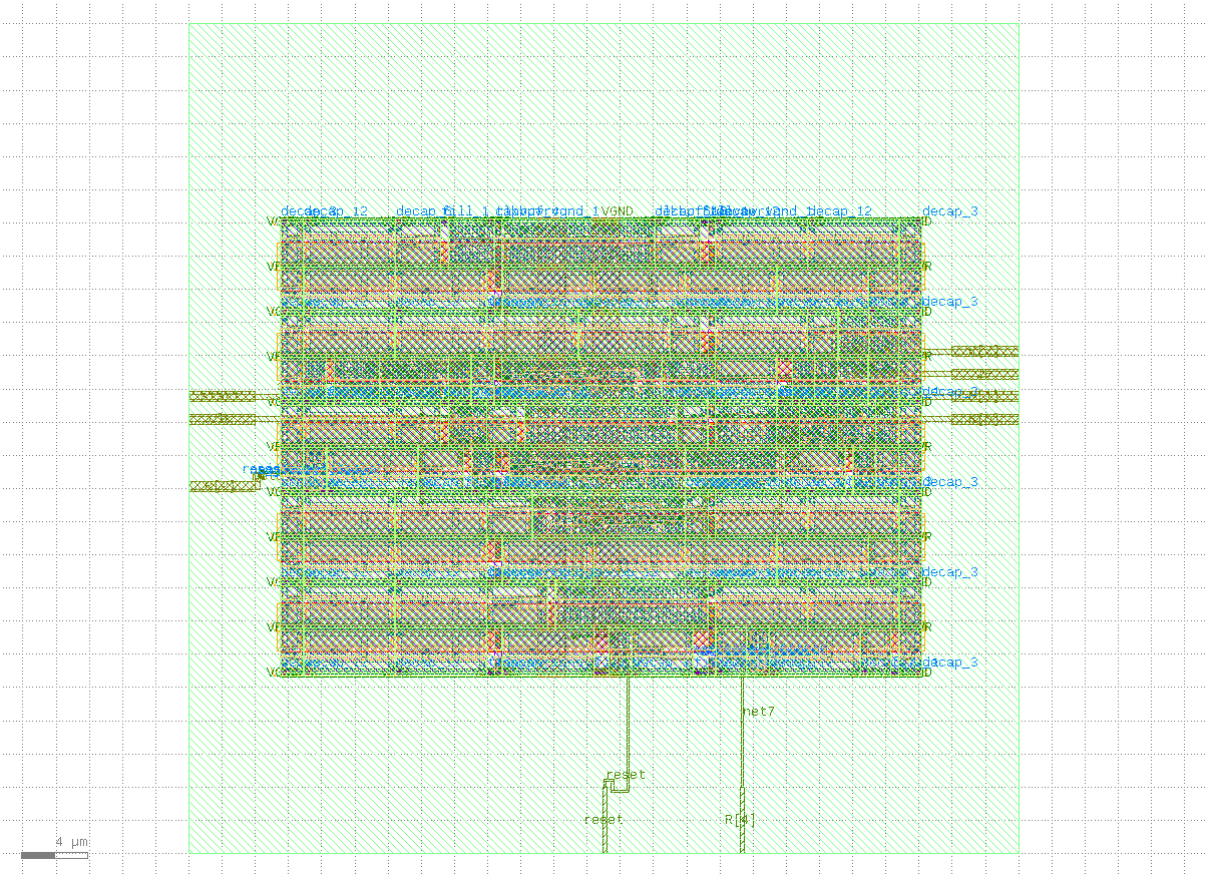
RTL Power Analysis (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added RTL Power Analysis info?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	

```
========================================================================
 report_power
========================================================================
======================= nom_tt_025C_1v80 Corner ===================================

Group                  Internal    Switching      Leakage        Total
                          Power        Power        Power        Power (Watts)
----------------------------------------------------------------------------
Sequential           8.137030e-06 4.154676e-06 3.476829e-11 1.229174e-05  20.5%
Combinational        8.621550e-06 1.325401e-05 7.568256e-11 2.187564e-05  36.5%
Clock                2.200619e-05 3.840083e-06 1.711718e-10 2.584644e-05  43.1%
Macro                0.000000e+00 0.000000e+00 0.000000e+00 0.000000e+00   0.0%
Pad                  0.000000e+00 0.000000e+00 0.000000e+00 0.000000e+00   0.0%
----------------------------------------------------------------------------
Total                3.876477e-05 2.124877e-05 2.816227e-10 6.001382e-05 100.0%
                            64.6%        35.4%         0.0%
```

GDS Layout (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added the GDS Layout figure?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)	



Heatmap (130nm Skywater PDK with OpenLane toolchain)

Check List: Have you added the heatmap?	YES
NB: Failing to add any required info will cause point penalty (1-2 Marks)