PROJECT REPORT of CSE-2204: Digital Techniques LAB

Group 6: 1903117, 1903118, 1903119, 1903120

Assigned Project: T-2

1. Design a MOD - 60 Counter by using any kinds of Flip – Flops.

2. Develop a 2 inputs NAND Gate using MOS Technology.

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Project No. 01

Name of Project: MOD - 60 Counter by using JK Flip – Flops

Objective: We have to design a synchronous counter using JK Flip-Flops

Introduction:

A special type of sequential circuit used to count the pulse is known as a counter, or a collection of flip flops where the clock signal is applied is known as counters.

Two types of counters can be made using flip-flops:

a) **Asynchronous Counter:** Asynchronous counters are those counters which do not operate on simultaneous clocking. The Asynchronous counter is also known as the ripple counter.
b) **Synchronous Counter:** A synchronous counter, in contrast to an asynchronous counter, is one whose output bits change state simultaneously, with no ripple.

Apparatus:

1. Integrated Circuits Used:

IC Model	IC Name	Pin Count	Manufacturer	Quantity (Pieces)
1. IC 74HC107N	JK Flip-Flop	14	Philips	3
2. IC SN74HC00N	NAND Gate	14	National Semiconductors	1
3. IC SN74HC08N	AND Gate	14	National Semiconductors	2
4. IC NE555	555 Timer	8	ST Microelectronics	1

2. 3-Volt Red & Green LEDs Manufacturer: NTE Semiconductors Quantity: 9

3. 1 Mega Ohm Rotary POT Manufacturer: W.L Electrical Quantity: 1

4. 1 Micro Farad Capacitor Manufacturer: Jameco ValuePro Quantity: 1

5. Resistors (330 Ohm, 1K Ohm, 100K Ohm)

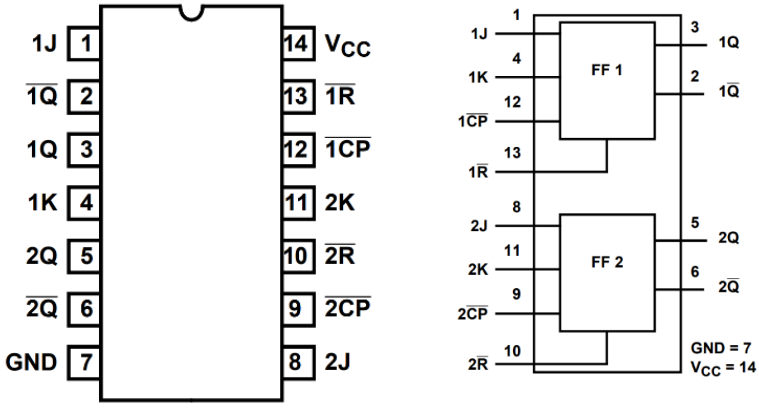
6. Generic Tap Switches Quantity: 2

7. Connecting Wires

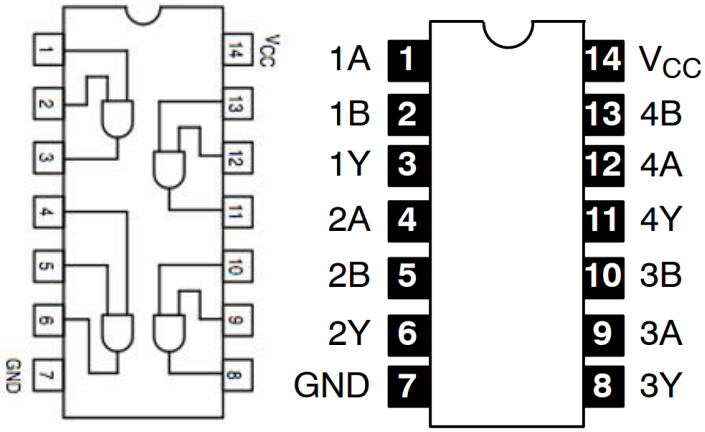
8. Bread Board Quantity: 2

Integrated Circuit Pinout Diagram:

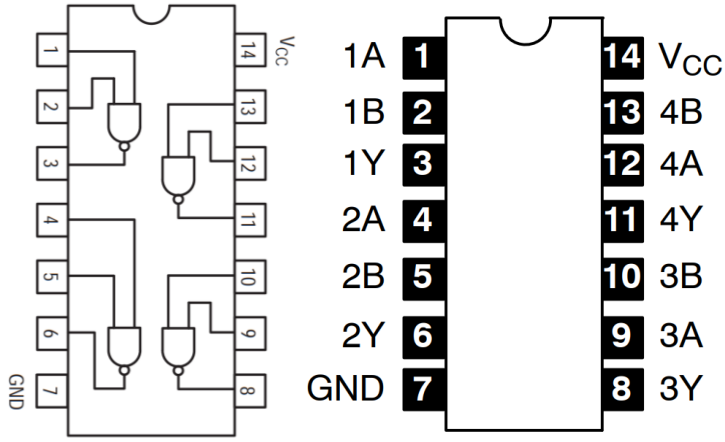
1. IC 74HC107N



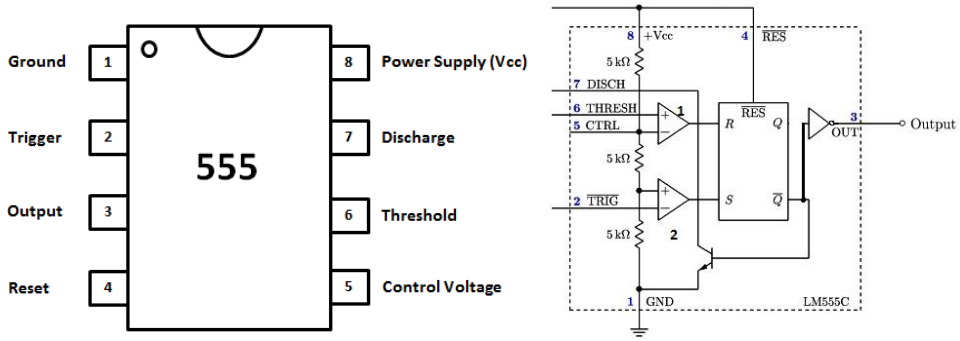
2. IC SN74HC00N



3. IC SN74HC08N



4. IC NE555


Ground
1
Trigger
2
Output
3
Reset
4
555
8
Power Supply (Vcc)
7
Discharge
6
Threshold
5
Control Voltage
+Vcc
RES
5 kΩ
DISCH
THRESH
CTRL
TRIG
GND
LM555C
R
Q
S
OUT
Output

Circuit Diagram:

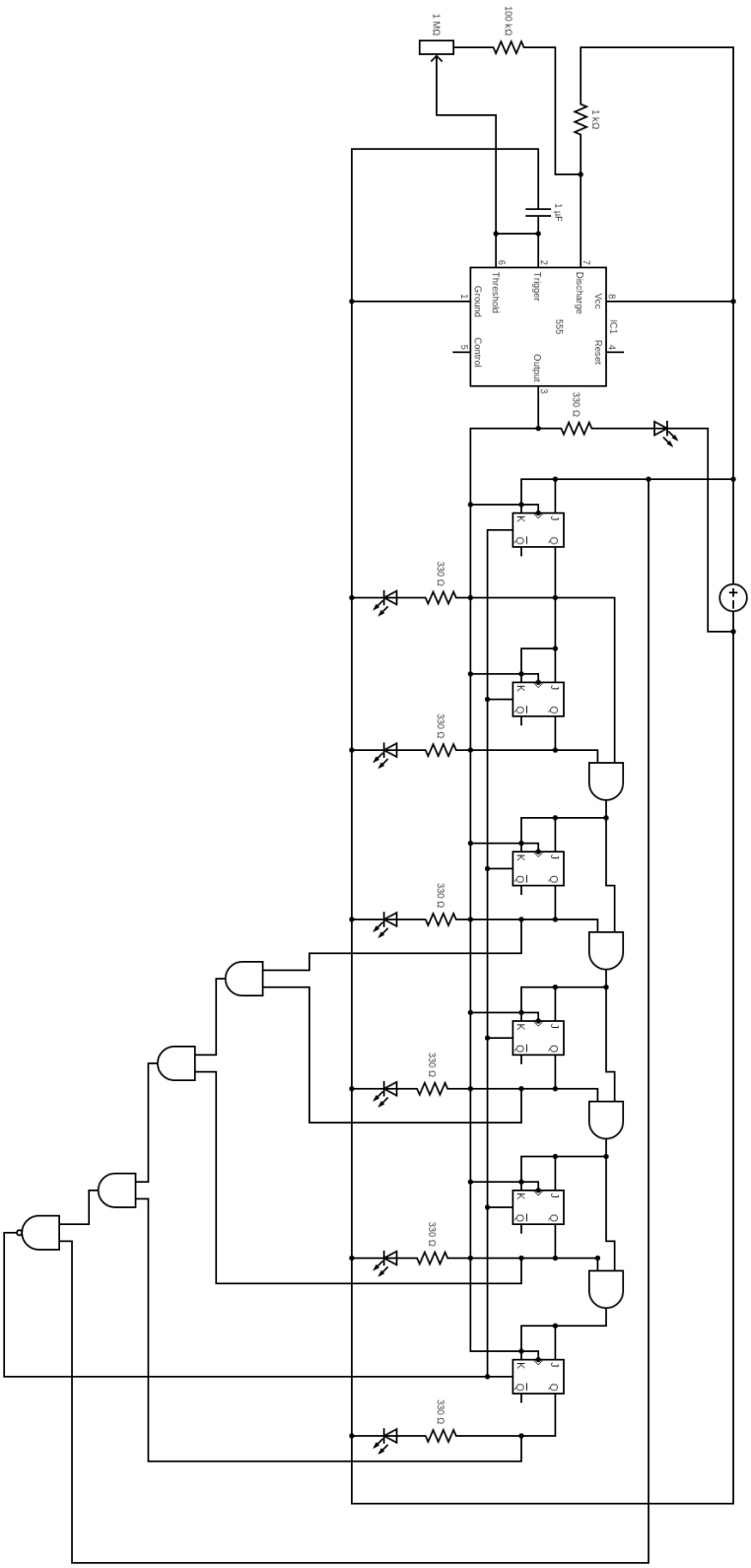


Figure 1: Circuit Connection (Drawn using circuitdesign.org)

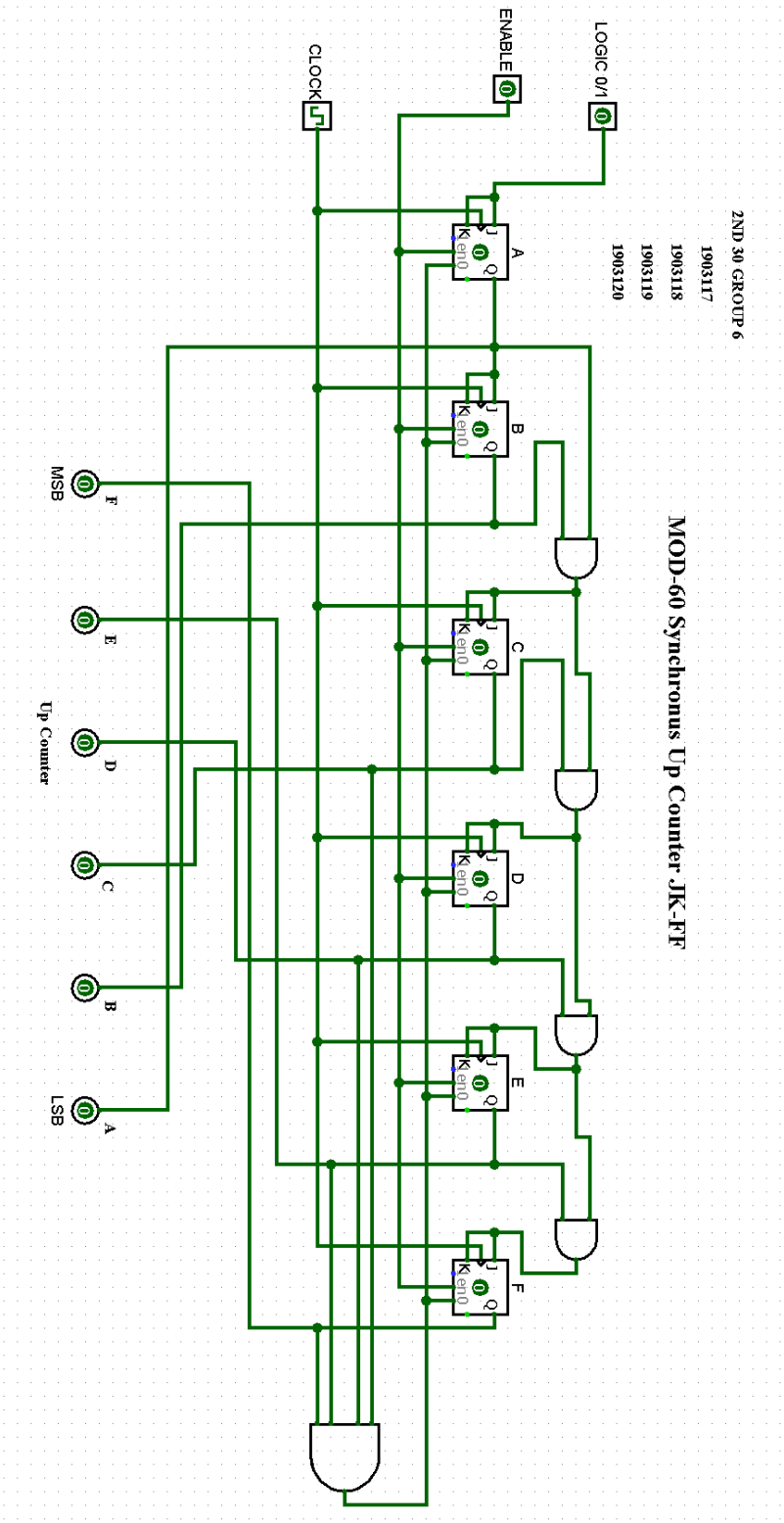


Figure 2: Logisim Circuit Design

Procedure:

Counter Section:

1. Pin 1,4 of all IC 74HC107N was sorted
2. Pin 8,11 of all IC 74HC107N was sorted
3. Pin 9,12 of all IC 74HC107N was sorted
4. Pin 10,13 of all IC 74HC107N was sorted
5. Pin 14 of all IC 74HC107N was connected to $+V_{cc}$
6. Pin 7 of all IC 74HC107N was connected to Ground
7. Pin 1,4 first IC 74HC107N was connected to $+V_{cc}$
8. Output A was taken from pin 3 of first IC 74HC107N
9. Output B was taken from pin 5 of first IC 74HC107N
10. Output C was taken from pin 3 of second IC 74HC107N
11. Output D was taken from pin 5 of second IC 74HC107N
12. Output E was taken from pin 3 of third IC 74HC107N
13. Output F was taken from pin 5 of third IC 74HC107N
14. Outputs F, E, D, C were passed to IC SN74HC08N
15. Output of IC SN74HC08N was passed to SN74HC00N
16. Output of IC SN74HC00N was passed to pin 13 of IC74HC107N for Clear/Reset.
17. Output from Pin 3 of IC NE555 was connected to pin 12 of first IC74HC107N for NGT Clock Pulse

IC NE555 Clock Pulse Section:

1. Pin 1 was connected to Ground
2. Pin 8 was given $+V_{cc}$
3. Pin 2, 6 was sorted
4. Pin 2 was connected through 1 Micro Farad Capacitor to Ground
5. Pin 7 was connected through 1 Kilo Ohm Resistor to $+V_{cc}$
6. Pin 6 was connected to 1 Mega Ohm POT through 100 Kilo Ohm Resistor to Pin 7
7. Pin 3 was used for output

Result:

The expected result was found it counted from 0-59 in binary number base where very left LED connected to first IC 74HC107N was LSB and the most right one connected to third IC 74HC107N was MSB.

Discussion:

Synchronous Counter was chosen over Asynchronous Counter because asynchronous or ripple counter has propagation delay and wasn't ideal type of design.

We couldn't use 9V battery to power the IC 74HC107N because the activation voltage of that IC is max 7V so, we used 3.3V DC battery.

Another anomaly was seen because of the IC SN74HC00N, it was creating some issues like false outputs due to problems in voltage filtering so we couldn't directly reset through NAND gate instead we used IC SN74HC08N first then manipulated the output through SN74HC00N and resetted it.

Project No. 02

Name of Project: 2 inputs NAND Gate using MOS Technology

Objective: We have to design a 2 inputs NAND Gate using Pull Up and Pull Down

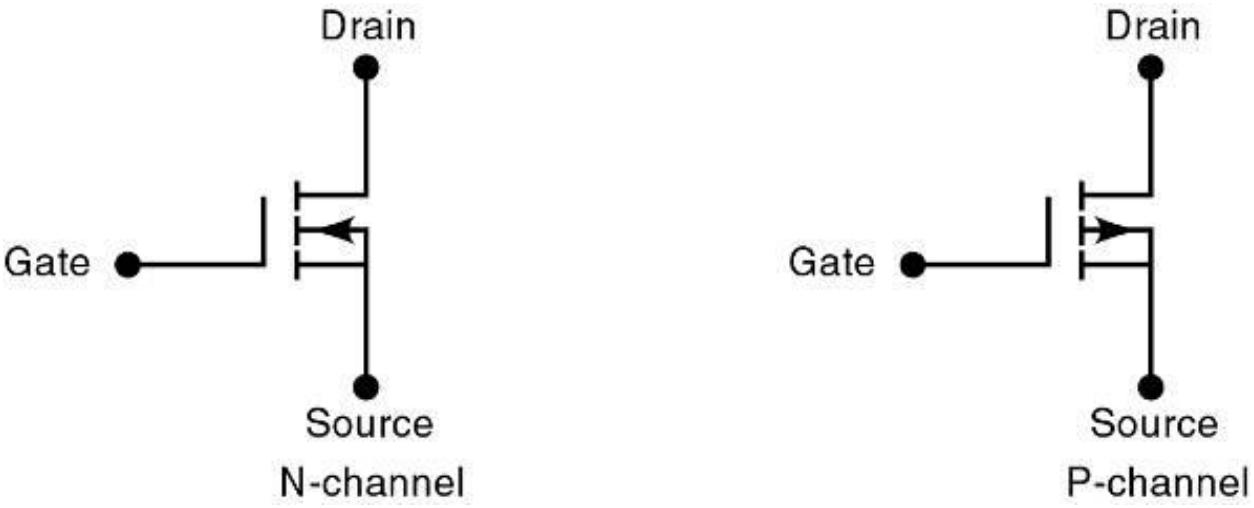
Introduction:

The NAND gate or "Not AND" gate is the combination of two basic logic gates, the AND gate and the NOT gate connected in series. The NAND gate and NOR gate can be called the universal gates since the combination of these gates can be used to accomplish any of the basic operations.

The type of transistor available is the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). These transistors are formed as a 'sandwich' consisting of a semiconductor layer, usually a slice, or wafer, from a single crystal of silicon; a layer of silicon dioxide (the oxide) and a layer of metal**.**

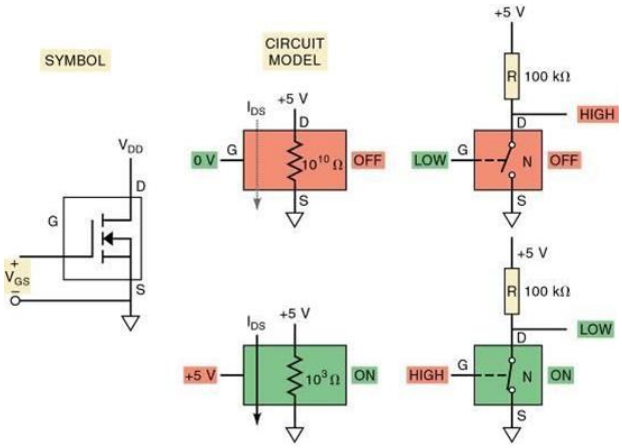
Complementary MOSFET (CMOS) technology is widely used today to form circuits in numerous and varied applications. Today's computers, CPUs and cell phones make use of CMOS due to several key advantages. CMOS offers low power dissipation, relatively high speed, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed).

Two Types of MOS are there:



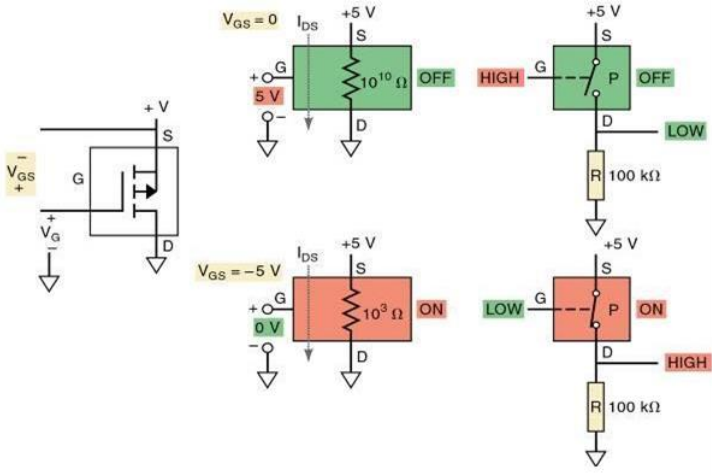
a) N-MOS: A N-channel MOSFET is the basic element in a family of devices known as N-MOS. Drain is always biased positive relative to the source.

- Gate-to-source voltage VGS is the input voltage.
- Where, $V_{GS} = V_G - V_S$
- ON/OFF Condition of N-MOS:
- When $V_{GS} > 0$ then N – MOS is ON
- When $V_{GS} \leq 0$ then N – MOS is OFF



b) P-MOS: The P-channel MOSFET—P-MOS—operates in the same manner as the N-channel, except that it uses voltages of opposite polarity. The drain is connected to the lower side of the circuit so it is biased with a more negative voltage relative to the source.

- Gate-to-source voltage V_{GS} is the input voltage.
- Where, $V_{GS} = V_G - V_S$
- ON/OFF Condition of P-MOS:
- When $V_{GS} < 0$ then P – MOS is ON
- When $V_{GS} \geq 0$ then P – MOS is OFF



Summary of N-MOS and P-MOS

Characteristics	N – MOS	P - MOS
Turning ON Condition	If Gate Input = 1 (HIGH)	If Gate Input = 0 (LOW)
Turning OFF Condition	If Gate Input = 0 (LOW)	If Gate Input = 1 (HIGH)
INPUT & OUTPUT	1. If Input = 0, then Output = 1 2. If Input = 1, then Output = 0	1. If Input = 0, then Output = 1 2. If Input = 1, then Output = 0
Application	Used in Pull down Network	Used in Pull up Network

Implementing NAND gate

Adding parallel P-channel & series N-channel MOSFETs to the basic INVERTER.

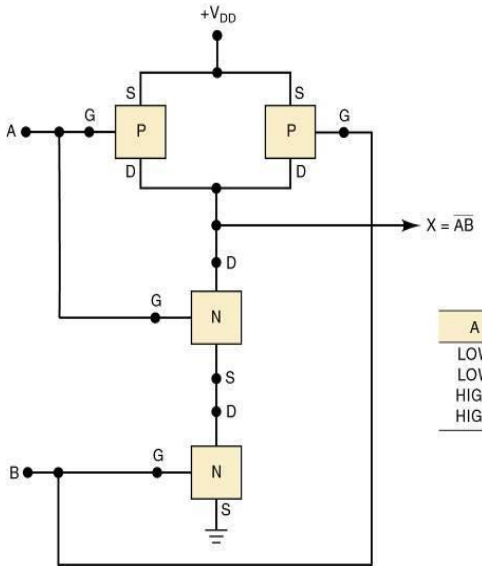
For NAND gate, $f=\overline{(A.B)}$

Pulldown $\bar{f} = A.B$

Pullup $p = f = \overline{A.B}$

$= \bar{A}+\bar{B}$

(De Morgan's Laws)



A	B	X
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

Apparatus:

1. Integrated Circuits Used:

IC Model	Pin Count	Quantity (Pieces)
1. IC P55F06N	3	2
2. IC IRFZ44N	3	2

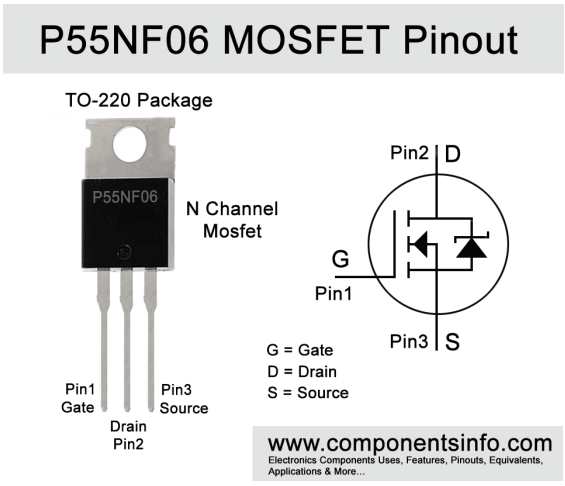
2. 3-Volt Red & Green LEDs Manufacturer: NTE Semiconductors Quantity: 1

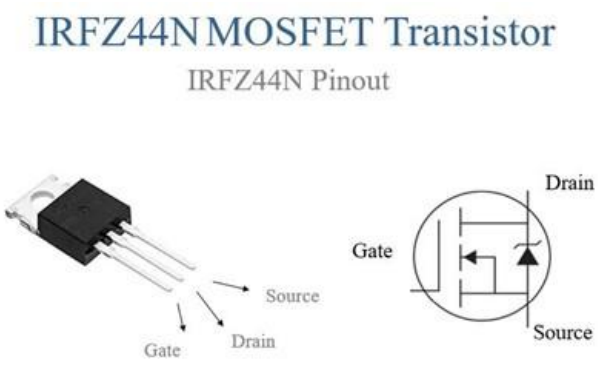
5. Resistors (330 Ohm)

7. Connecting Wires

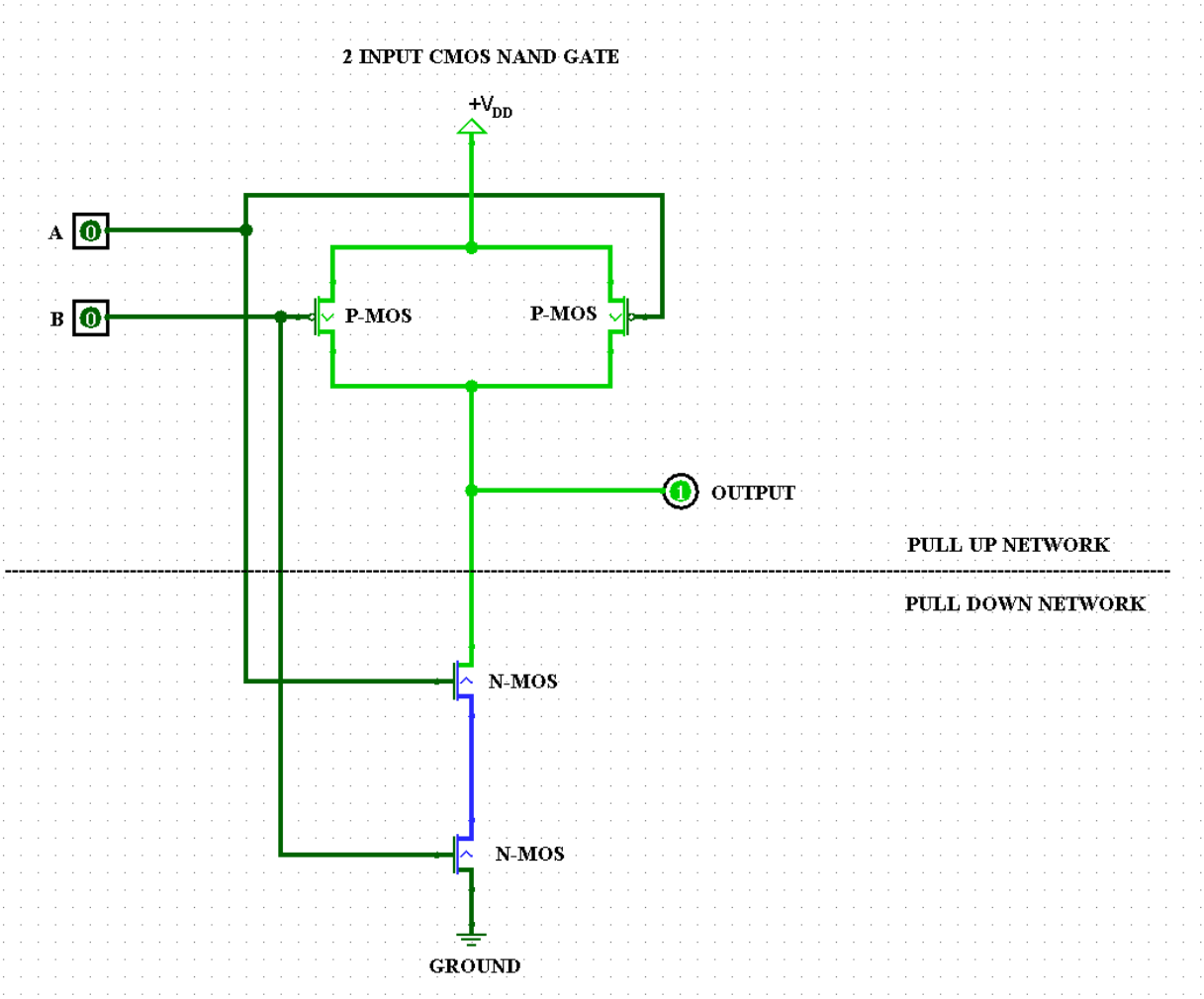
8. Bread Board Quantity: 1

Integrated Circuit Pinout Diagram:





Circuit Diagram:



Procedure:

1. Pin 3 of first IC P55F06N and second IC P55F06N was sorted and given $+V_{cc}$
2. Pin 2 of first IC P55F06N and second IC P55F06N was sorted
3. From Sorted Pin 2 of of first IC P55F06N and second IC P55F06N Output was taken
4. From Sorted Pin 2 of first IC P55F06N and second IC P55F06N we passed it to first IRFZ44N pin 2
5. From Pin 3 of first IRFZ44N we passed it to second IRFZ44N Pin 2
6. Pin 3 of second IRFZ44N was connected to Ground
7. Both Pin 1 of first IRFZ44N and P55F06N was sorted and taken as A input

8. Both Pin 1 of second IRFZ44N and P55F06N was sorted and taken as B input

Result:

The expected result was found as it gave output of a NAND Gate and matched the truth table.

Discussion:

The input current of the both MOSFETs were kept below 0.25mA because that was mentioned in the manufacturer's specs sheet.