

Avnet Engineering Services

Title:

01 - Avnet Lead Sheet_B.SchDoc

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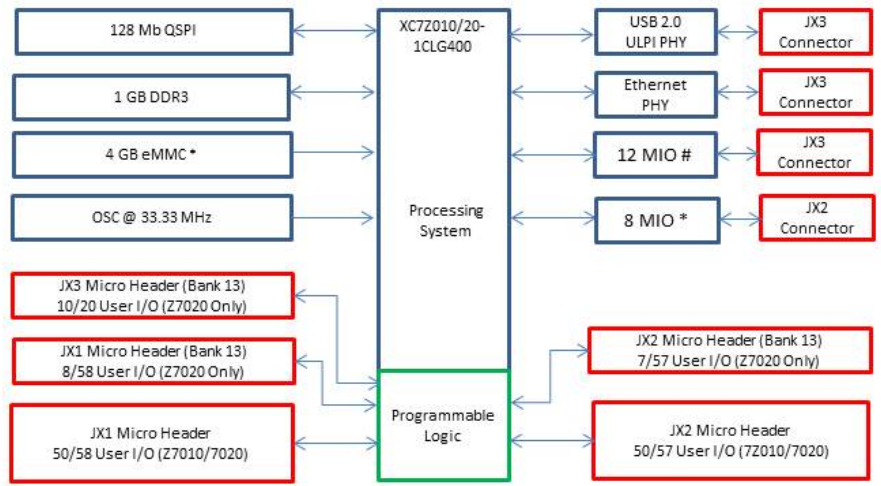
B

PicoZed

C

Date: 11/17/2014

Sheet 1 of 12



MIO47 and ETHERNET RESET Shared
* eMMC and MIO Interface Shared on JX2

Zynq PS DDR - Bank 502

U1G
Zynq 1010/1020 SOC CI 6400

BANK 502

PS_DDR_DQ0_502	DDR3 DQ0
PS_DDR_DQ1_502	DDR3 DQ1
PS_DDR_DQ2_502	DDR3 DQ2
PS_DDR_DQ3_502	DDR3 DQ3
PS_DDR_DQ4_502	DDR3 DQ4
PS_DDR_DQ5_502	DDR3 DQ5
PS_DDR_DQ6_502	DDR3 DQ6
PS_DDR_DQ7_502	DDR3 DQ7
PS_DDR_DQ8_502	DDR3 DQ8
PS_DDR_DQ9_502	DDR3 DQ9
PS_DDR_DQ10_502	DDR3 DQ10
PS_DDR_DQ11_502	DDR3 DQ11
PS_DDR_DQ12_502	DDR3 DQ12
PS_DDR_DQ13_502	DDR3 DQ13
PS_DDR_DQ14_502	DDR3 DQ14
PS_DDR_DQ15_502	DDR3 DQ15
PS_DDR_DQ16_502	DDR3 DQ16
PS_DDR_DQ17_502	DDR3 DQ17
PS_DDR_DQ18_502	DDR3 DQ18
PS_DDR_DQ19_502	DDR3 DQ19
PS_DDR_DQ20_502	DDR3 DQ20
PS_DDR_DQ21_502	DDR3 DQ21
PS_DDR_DQ22_502	DDR3 DQ22
PS_DDR_DQ23_502	DDR3 DQ23
PS_DDR_DQ24_502	DDR3 DQ24
PS_DDR_DQ25_502	DDR3 DQ25
PS_DDR_DQ26_502	DDR3 DQ26
PS_DDR_DQ27_502	DDR3 DQ27
PS_DDR_DQ28_502	DDR3 DQ28
PS_DDR_DQ29_502	DDR3 DQ29
PS_DDR_DQ30_502	DDR3 DQ30
PS_DDR_DQ31_502	DDR3 DQ31

PS_DDR_A0_502	DDR3 A0 3
PS_DDR_A1_502	DDR3 A1 3
PS_DDR_A2_502	DDR3 A2 3
PS_DDR_A3_502	DDR3 A3 3
PS_DDR_A4_502	DDR3 A4 3
PS_DDR_A5_502	DDR3 A5 3
PS_DDR_A6_502	DDR3 A6 3
PS_DDR_A7_502	DDR3 A7 3
PS_DDR_A8_502	DDR3 A8 3
PS_DDR_A9_502	DDR3 A9 3
PS_DDR_A10_502	DDR3 A10 3
PS_DDR_A11_502	DDR3 A11 3
PS_DDR_A12_502	DDR3 A12 3
PS_DDR_A13_502	DDR3 A13 3
PS_DDR_A14_502	DDR3 A14 3

PS_DDR_DQS_P0_502	DDR3 DQS0 3 P
PS_DDR_DQS_N0_502	DDR3 DQS0 3 N
PS_DDR_DQS_P1_502	DDR3 DQS1 3 P
PS_DDR_DQS_N1_502	DDR3 DQS1 3 N
PS_DDR_DQS_P2_502	DDR3 DQS2 3 P
PS_DDR_DQS_N2_502	DDR3 DQS2 3 N
PS_DDR_DQS_P3_502	DDR3 DQS3 3 P
PS_DDR_DQS_N3_502	DDR3 DQS3 3 N
PS_DDR_CK0_P_502	DDR3 CK0 3 P
PS_DDR_CK0_N_502	DDR3 CK0 3 N

PS_DDR_BA0_502	DDR3 BA0 3
PS_DDR_BA1_502	DDR3 BA1 3
PS_DDR_BA2_502	DDR3 BA2 3
PS_DDR_DM0_502	DDR3 DM0 3
PS_DDR_DM1_502	DDR3 DM1 3
PS_DDR_DM2_502	DDR3 DM2 3
PS_DDR_DM3_502	DDR3 DM3 3

PS_DDR_CS0_502	DDR3 CS# 3
PS_DDR_WE0_502	DDR3 WE# 3
PS_DDR_CAS0_502	DDR3 CAS# 3
PS_DDR_RAS0_502	DDR3 RAS# 3
PS_DDR_ODT_502	DDR3 ODT 3
PS_DDR_RSTB_502	DDR3 RESET# 3
PS_DDR_VPP_502	DDR3 VPP 3
PS_DDR_VRN_502	DDR3 VRN 3

DDR_D_BI_0 DDR3 DQ[7..0]
DDR_D_BI_1 DDR3 DQ[15..8]
DDR_D_BI_2 DDR3 DQ[23..16]
DDR_D_BI_3 DDR3 DQ[31..24]

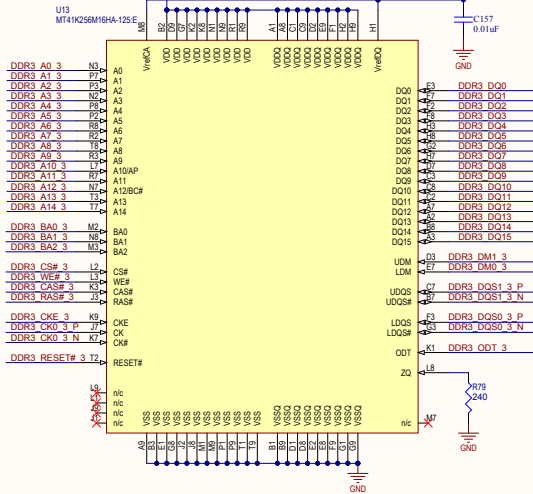
DDR_D

DDR_AC

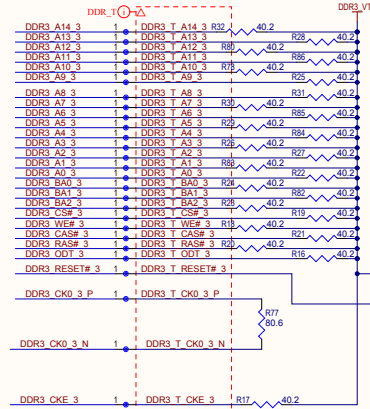
DDR_DM

Layout Note:
DDR3 trace lengths must include
Zynq package flight times.
See UG933 and Layout
Guidelines.

Layout Note:
DDR3 target trace impedances
are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms



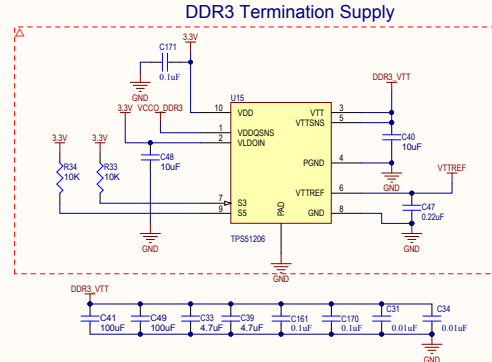
Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.



Default: Pins 1 - 2, 4.75K-ohm resistor.

NOTE:
RESET# requires a Pull
Down resistor through FPGA
Configuration. See
UG933p62 and Answer
Record 55616.

DDR3



Zynq PS MIO - Bank 500

U11E
Zynq 7010/7020 SOC CLG400

BANK 500

PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500

PS_POR_B_500
PS_CLK_500

PG_MODULE
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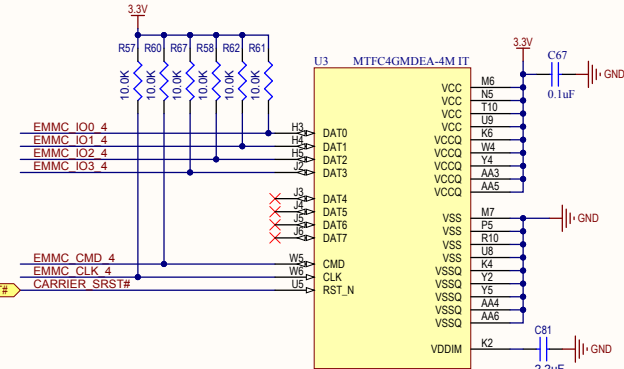
PG_MODULE

PG_MODULE

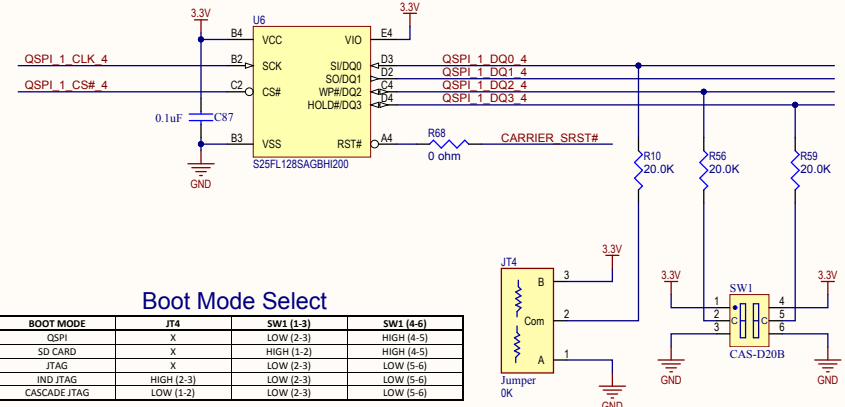
PG_MODULE

PG_MODULE

Embedded eMMC: 2GB, 4GB, 8GB



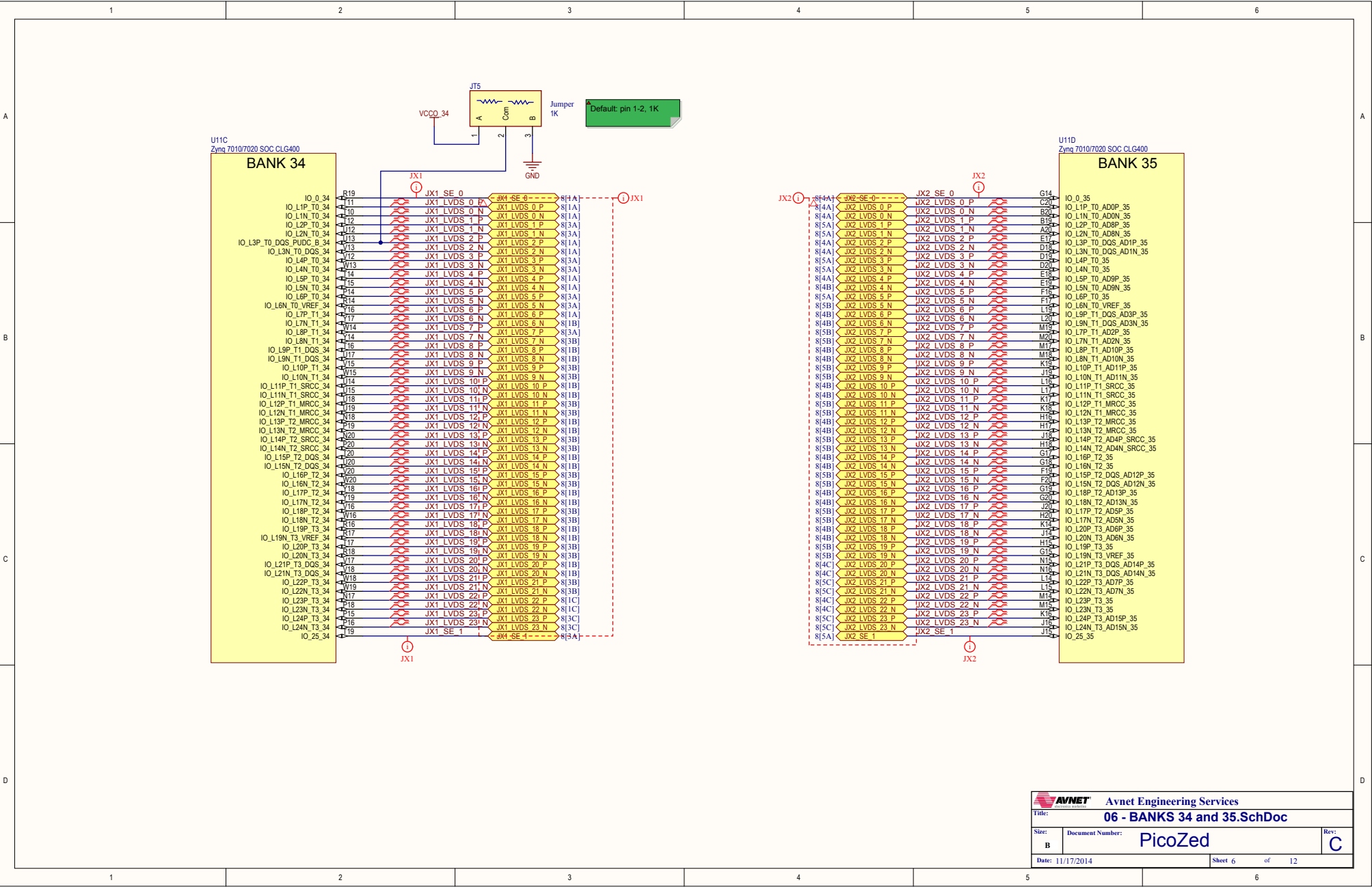
QSPI



Boot Mode Select

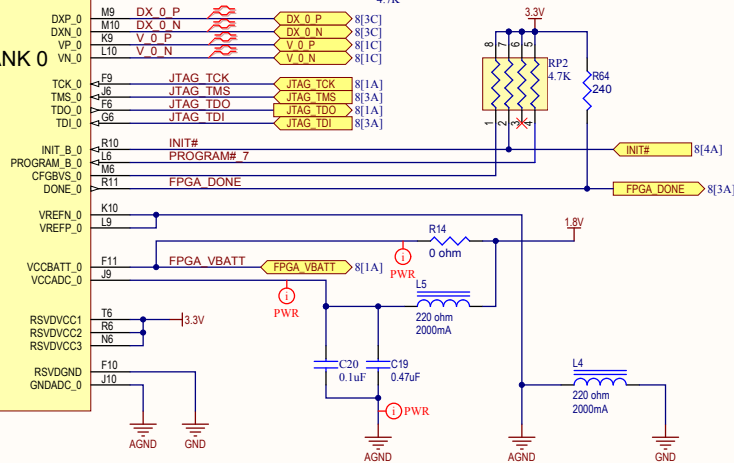
CASCADE JTAG - DEFAULT MODE





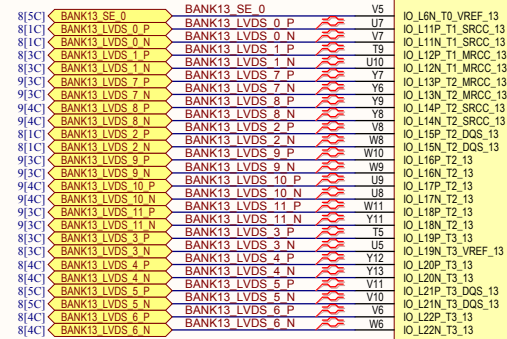
U11A
Zynq 7010/7020 SOC CLG400

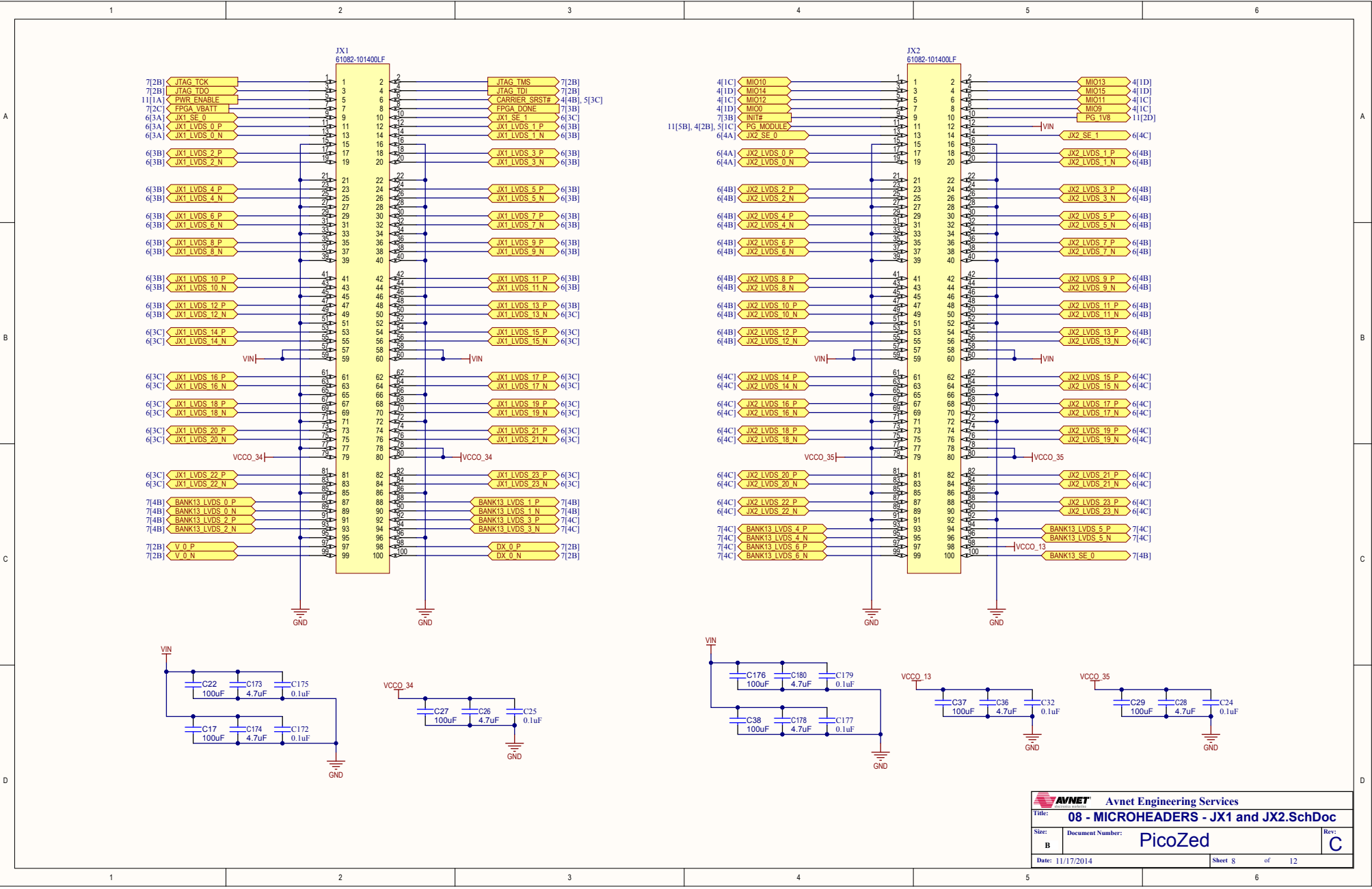
BANK 0

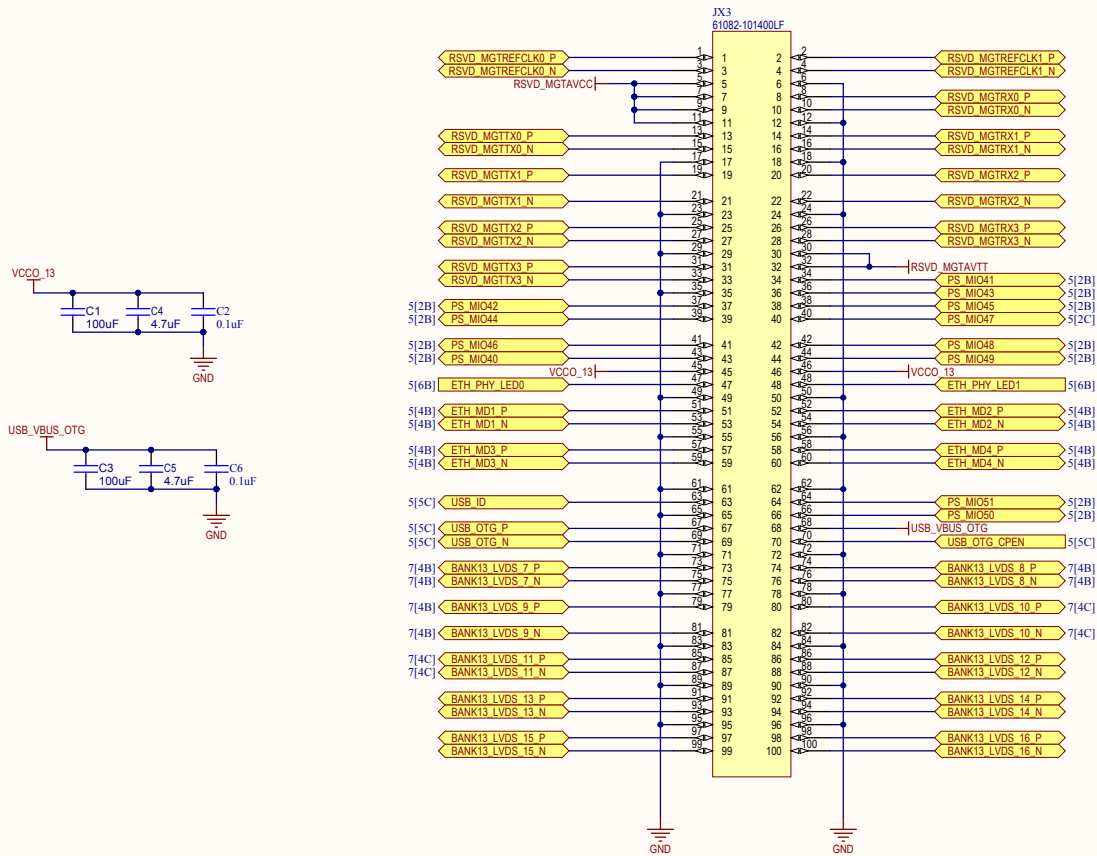


U11B
Zynq 7010/7020 SOC CLG400

BANK 13 (Z7020 Only)







All RSVD_MGT* signals are RESERVED for devices with MGTs.

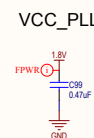
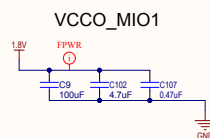
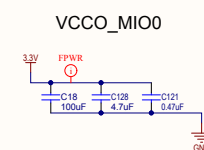
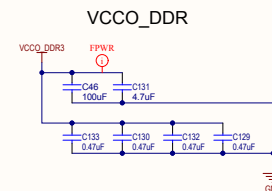
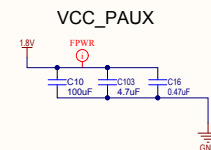
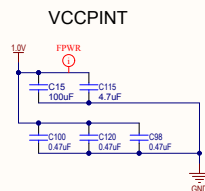
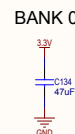
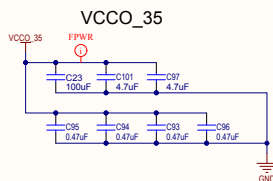
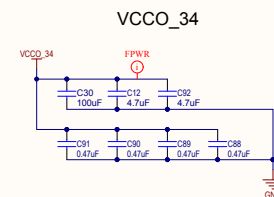
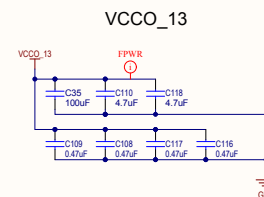
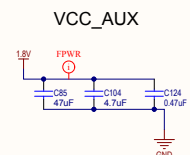
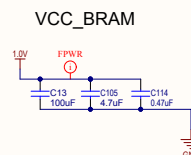
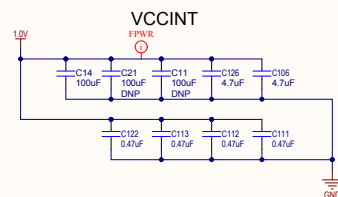
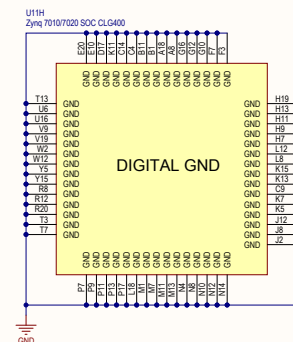
ZYNQ MIO POTENTIAL MAPPING OPTIONS:

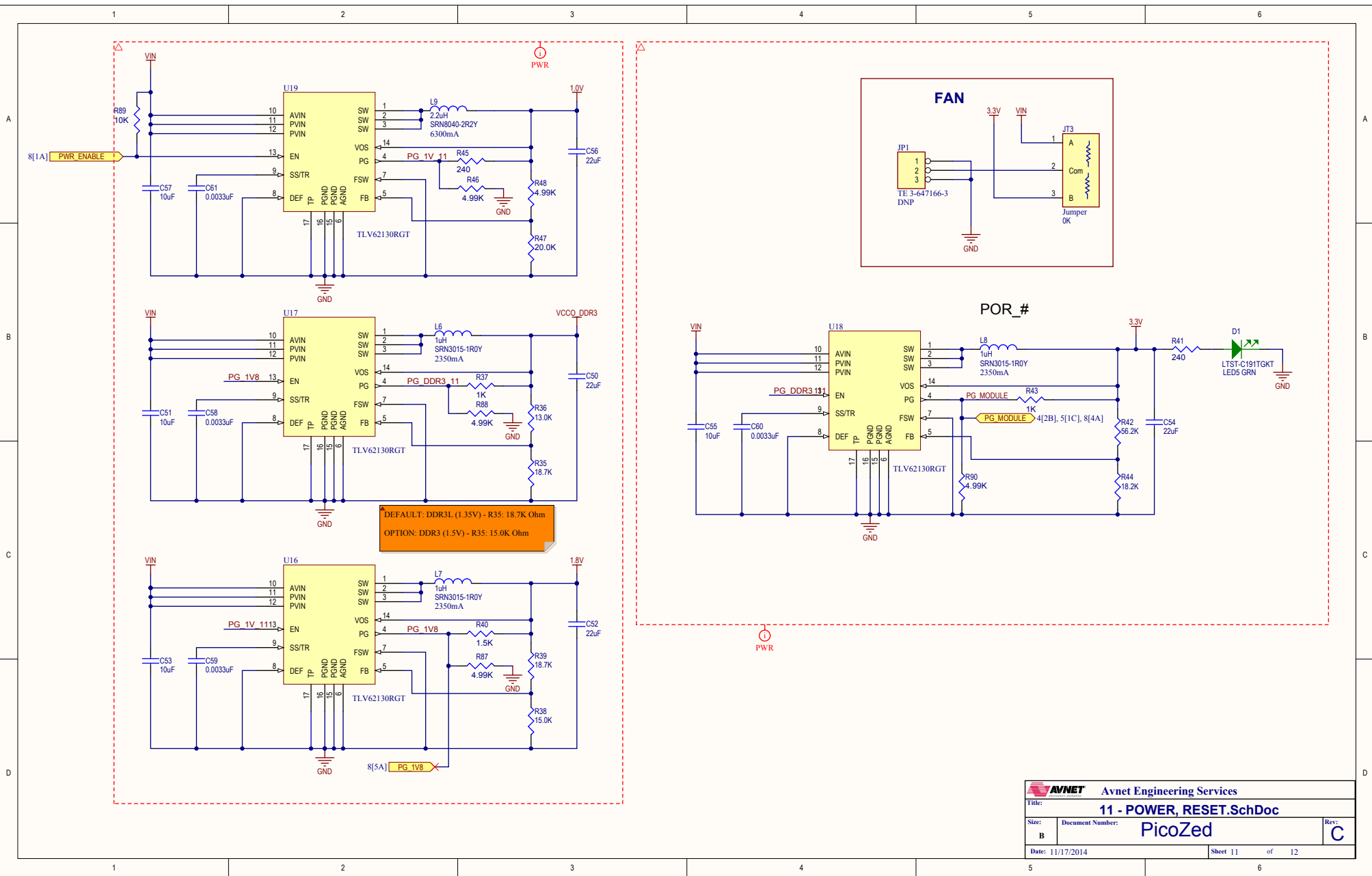
SDIO INTERFACE
PS_MIO40 - SD_CLK through a 40.2-ohm RES
PS_MIO41 - SD_CMD
PS_MIO42 - SD_D0
PS_MIO43 - SD_D1
PS_MIO44 - SD_D2
PS_MIO45 - SD_D3
PS_MIO46 - SD_CD

UART INTERFACE
PS_MIO48 - UART_RXD (Tie to the TXD pin of a UART)
PS_MIO49 - UART_TXD (Tie to the RXD pin of a UART)

USB INTERFACE
PS_MIO40 - DATA
PS_MIO41 - DIR
PS_MIO42 - STP
PS_MIO43 - NXT
PS_MIO44 - DATA
PS_MIO45 - DATA
PS_MIO46 - DATA
PS_MIO47 - DATA
PS_MIO48 - CK
PS_MIO49 - DATA
PS_MIO50 - DATA

BANK13_LVDS_12_P/N thru BANK13_LVDS_16_P/N is reserved for larger density BANK13





Revision Notes:

- PicoZed Revision B1:
- 1) Multiplexed JX2 MIO signals with EMMC
 - 2) Removed Push Button Footprint
 - 3) Incorporated ETHERNET RESET circuit
 - 4) Added bulk cap to AVDD18
 - 5) Added GND Testpoints

- PicoZed Revision B2:
- 1) Updated BOOT MODE table

- PicoZed Revision C:
- 1) Updated Block Diagram
 - 2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
 - 3) Added RC time constant to ETHERNET RESET
 - 4) DDR3L / DDR3 Option Added
 - 5) Modified resistor divider value on PG_1V8
 - 6) Changed DDR3 Termination Regulator VLDOIN from 1.8V to 3.3V

Mechanicals:

