Zynq PicoZed	
Avnet Engineering Services	
www.picozed.org	
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PicoZed - Rev C

11/17/2014

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AVNET Avnet Engineering Services		
Title: 01 - Avnet Lead Sheet_B.SchDoc		
Size: B	Document Number: PicoZed	Rev: C
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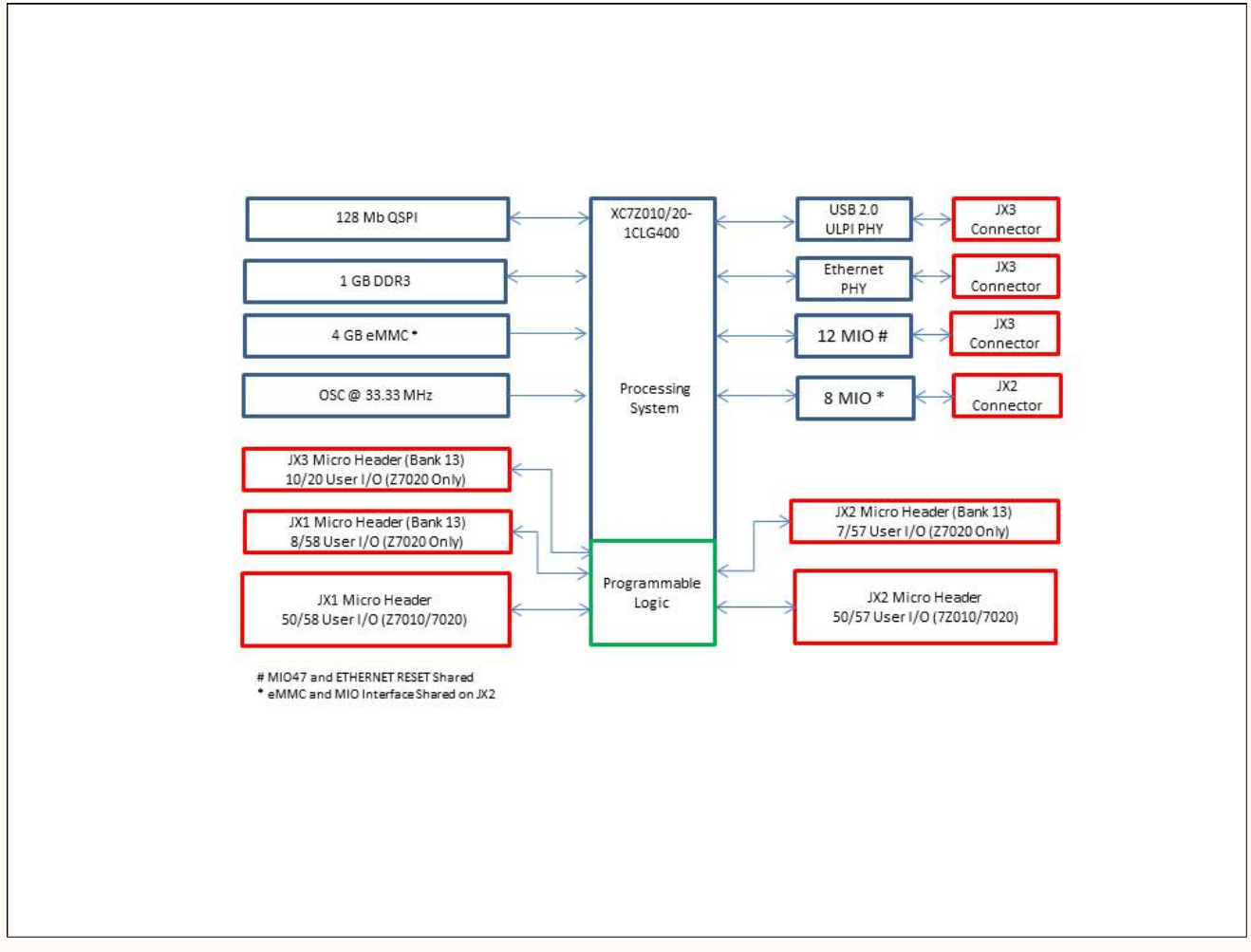

Avnet Engineering Services		
Title: 02 - Block Diagram.SchDoc		
Size: B	Document Number: PicoZed	Rev: C
Date: 11/17/2014	Sheet 2 of 12	

Zynq PS DDR - Bank 502

DDR3

DDR3 Termination Supply

Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.

Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms

Default: Pins 1 - 2, 4.75K-ohm resistor.

NOTE:
RESET# requires a Pull Down resistor through FPGA Configuration. See UG953p62 and Answer Record 55616.

Avnet Engineering Services	
Title:	03 - DDR3.SchDoc
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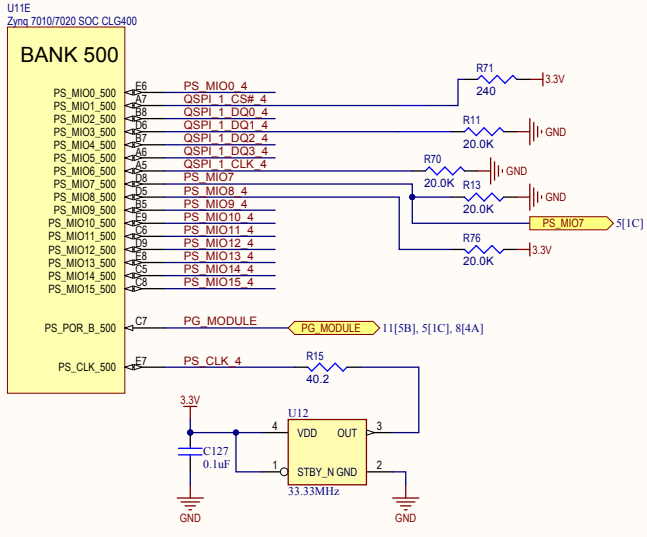
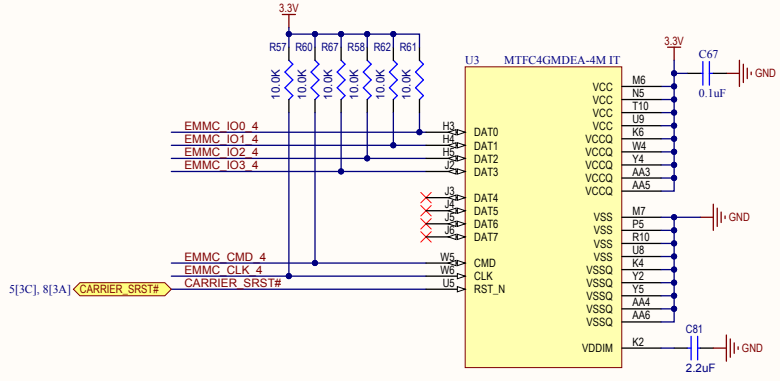
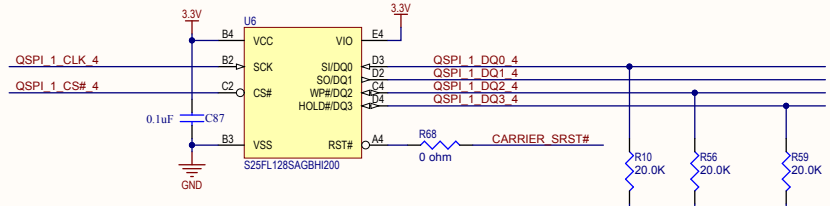
Zynq PS MIO - Bank 500



Embedded eMMC: 2GB, 4GB, 8GB

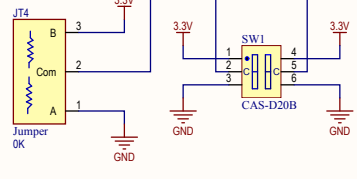


QSPI

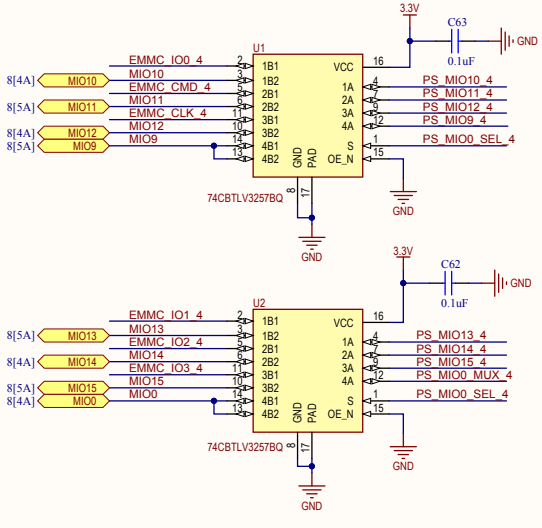


Boot Mode Select

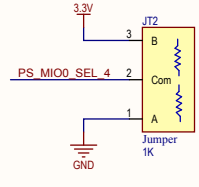
BOOT MODE	JT4	SW1 (1-3)	SW1 (4-6)
QSPI	X	LOW (2-3)	HIGH (4-5)
SD CARD	X	HIGH (1-2)	HIGH (4-5)
JTAG	X	LOW (2-3)	LOW (5-6)
IND JTAG	HIGH (2-3)	LOW (2-3)	LOW (5-6)
CASCADE JTAG	LOW (1-2)	LOW (2-3)	LOW (5-6)



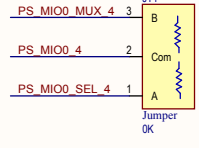
CASCADE JTAG - DEFAULT MODE



MUX SEL: Default - eMMC



PMOD / MUX SEL: Default - MUX SEL



AVNET Avnet Engineering Services			
Title: 04 - QSPI FLASH, eMMC.SchDoc			
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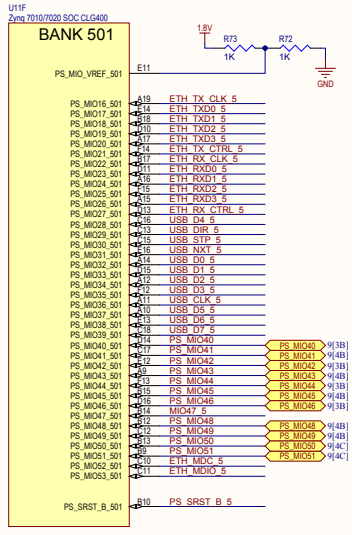
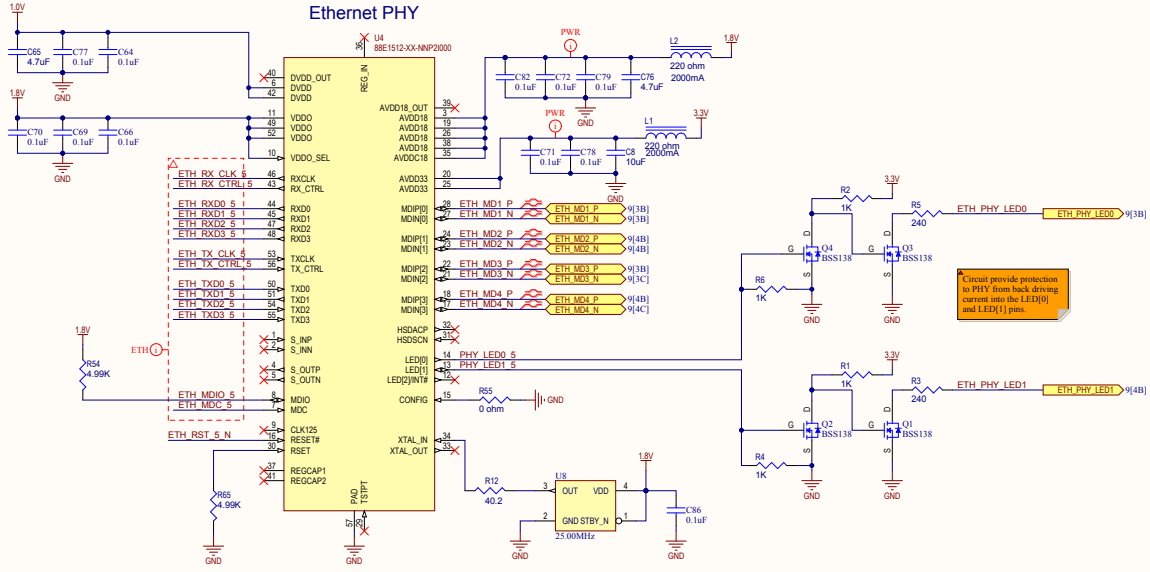
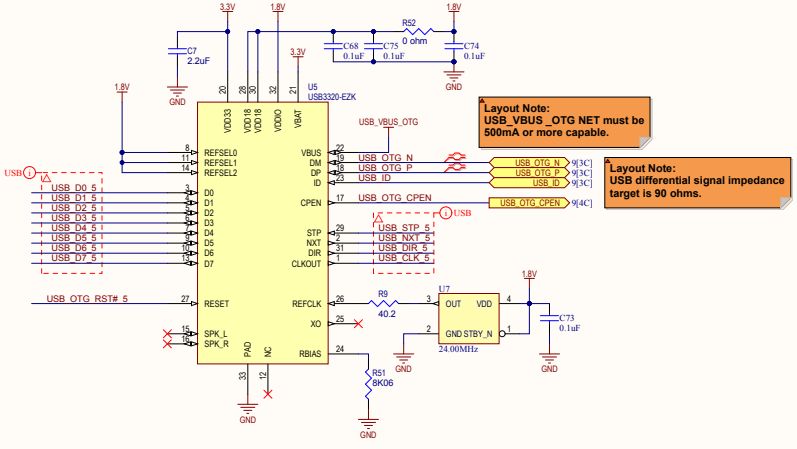
Zynq PS MIO - Bank 501

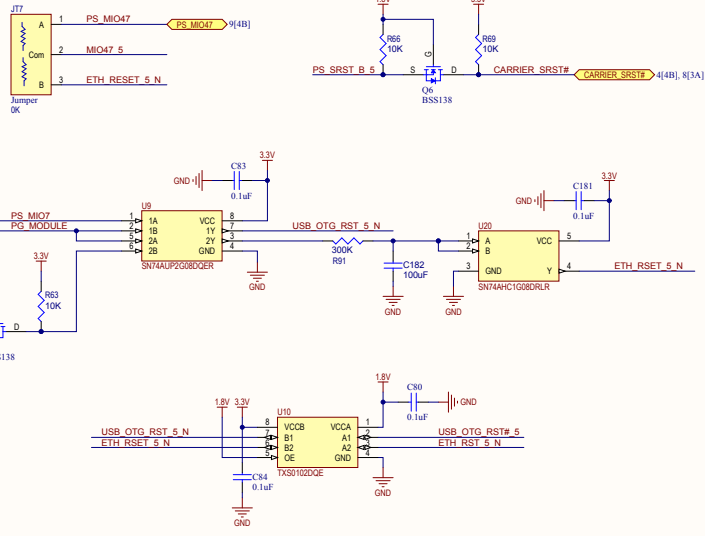


Ethernet PHY



USB 2.0 OTG





Avnet Engineering Services			
Title: 05 - ETHERNET, USB.SchDoc			
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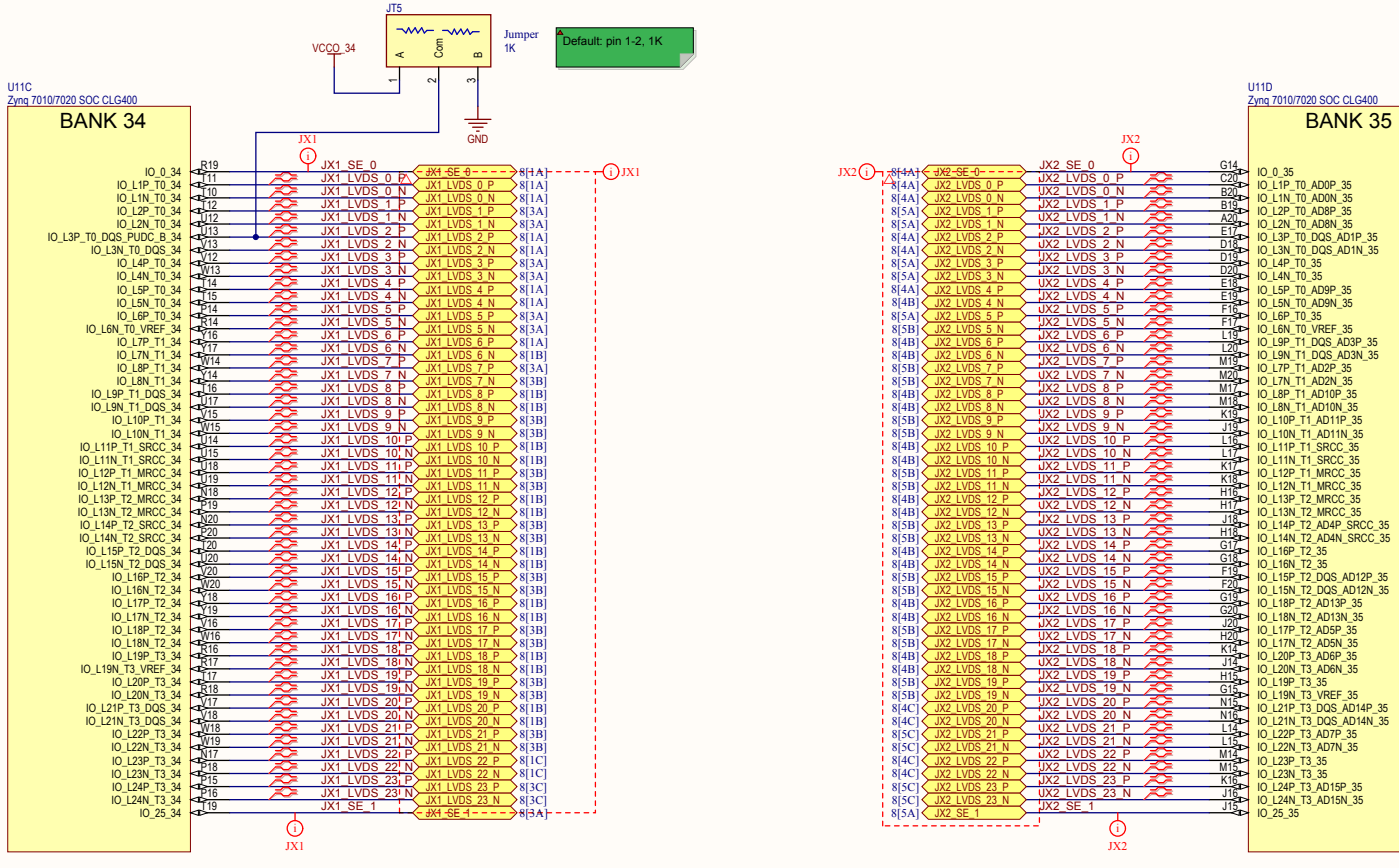

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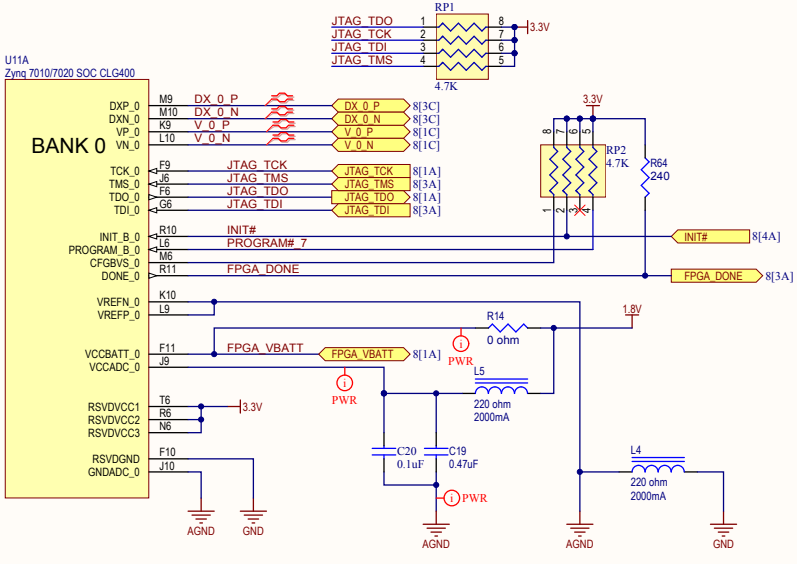

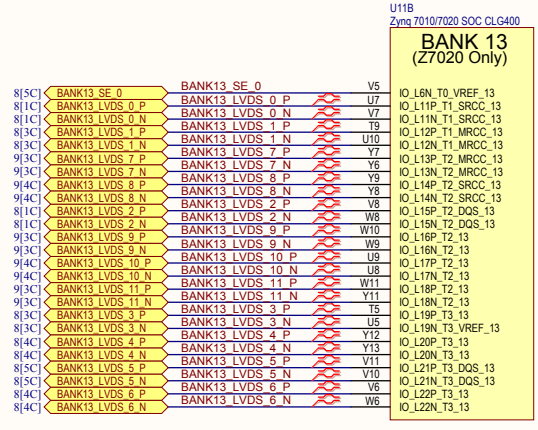

Avnet Engineering Services	
Title:	07 - BANK 0, BANK13, JTAG.SchDoc
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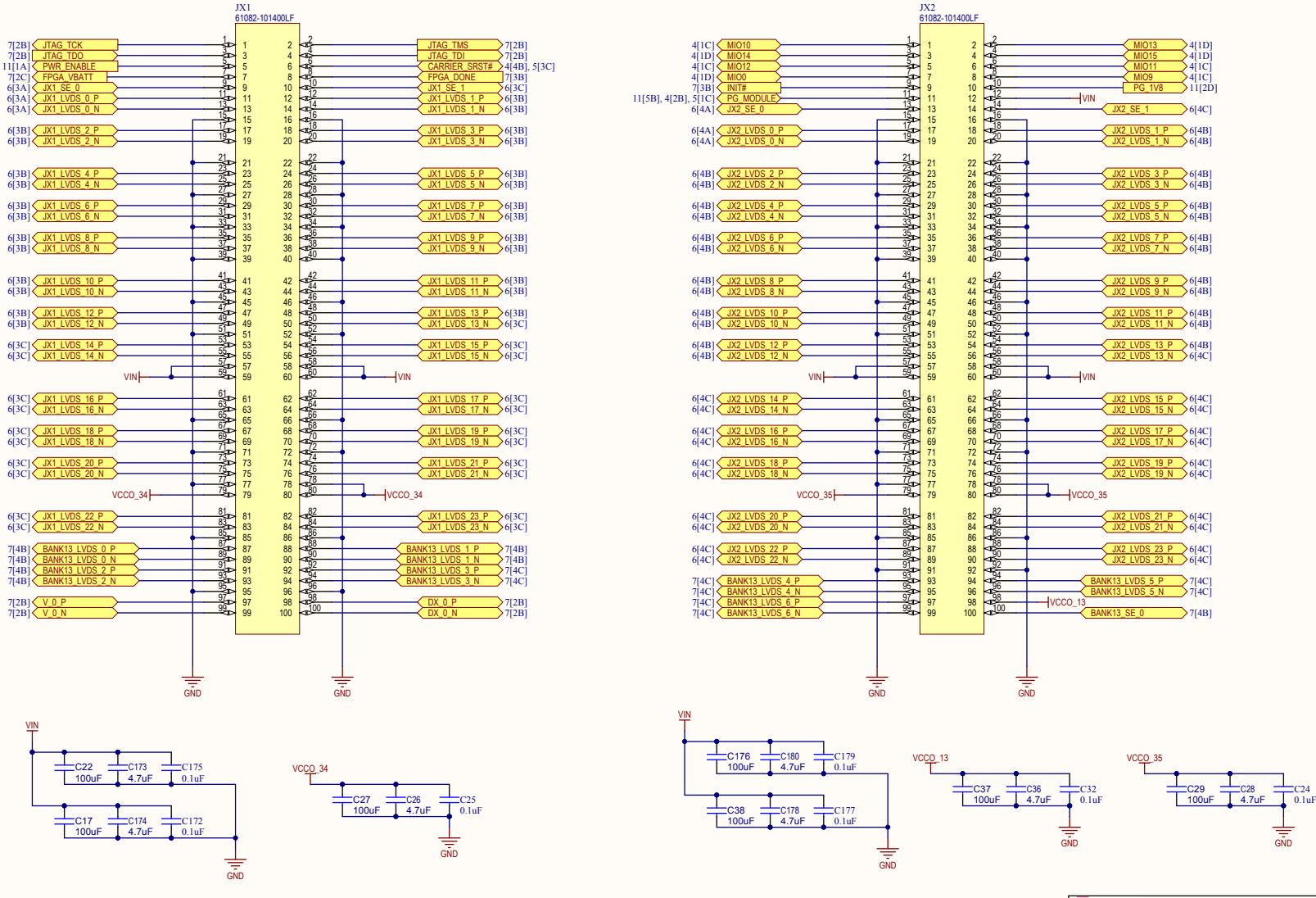

Avnet Engineering Services		
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Size: B	Document Number: PicoZed	Rev: C
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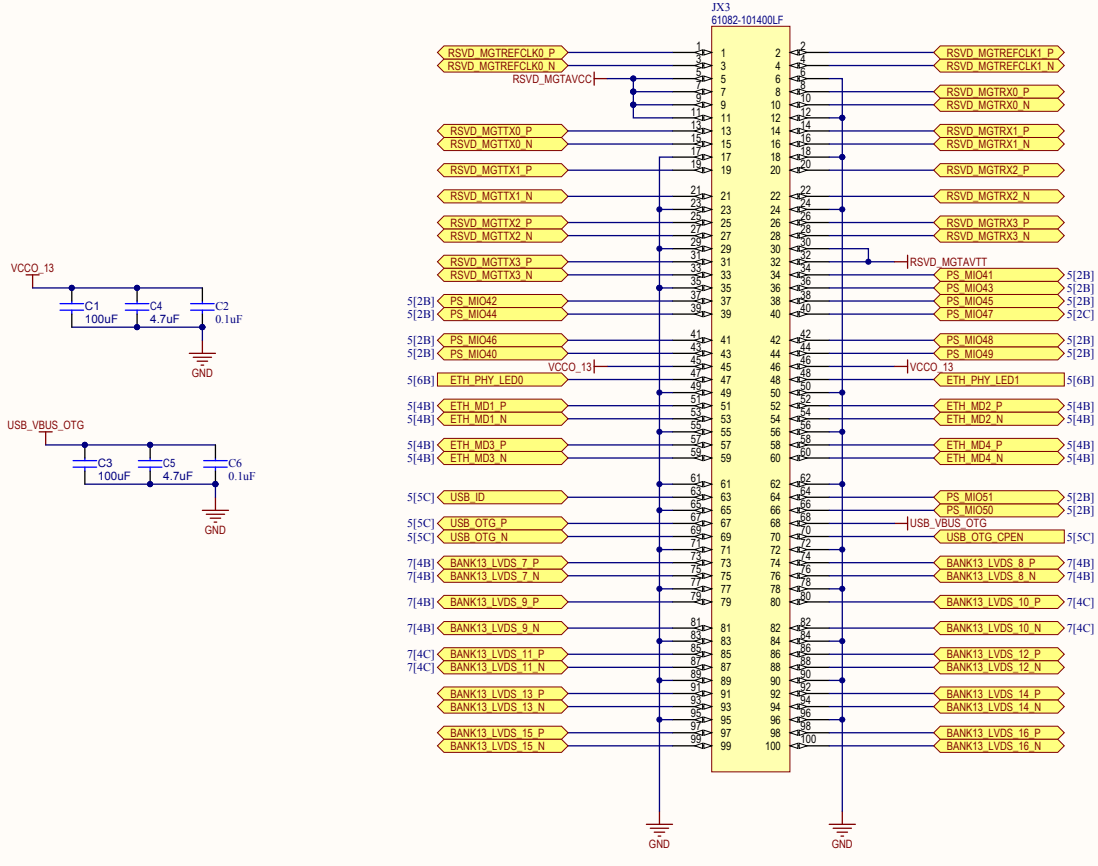

All RSVD_MGT* signals are RESERVED for devices with MGTs.

ZYNQ MIO POTENTIAL MAPPING OPTIONS:

SDIO INTERFACE
PS_MIO40 - SD_CLK through a 40.2-ohm RES
PS_MIO41 - SD_CMD
PS_MIO42 - SD_D0
PS_MIO43 - SD_D1
PS_MIO44 - SD_D2
PS_MIO45 - SD_D3
PS_MIO46 - SD_CD

UART INTERFACE
PS_MIO48 - UART_RXD (Tie to the TXD pin of a UART)
PS_MIO49 - UART_TXD (Tie to the RXD pin of a UART)

USB INTERFACE
PS_MIO40 - DATA
PS_MIO41 - DIR
PS_MIO42 - STP
PS_MIO43 - NXT
PS_MIO44 - DATA
PS_MIO45 - DATA
PS_MIO46 - DATA
PS_MIO47 - DATA
PS_MIO48 - CK
PS_MIO49 - DATA
PS_MIO50 - DATA

BANK13_LVDS_12_P/N thru BANK13_LVDS_16_P/N is reserved for larger density BANK13

Avnet Engineering Services		
Title: 09 - MICROHEADER - JX3.SchDoc		
Size: B	Document Number: PicoZed	Rev: C
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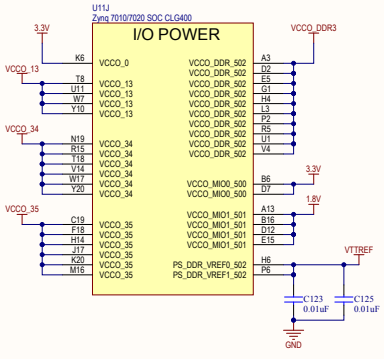

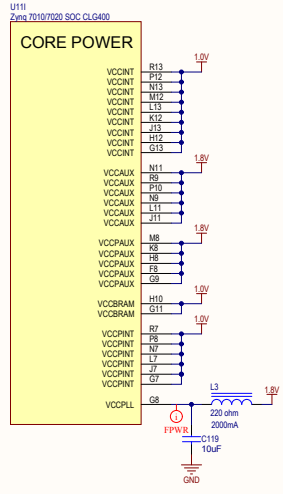

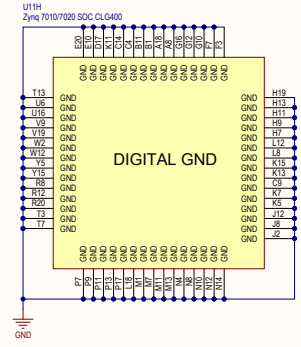

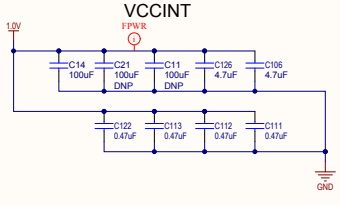

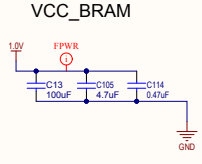

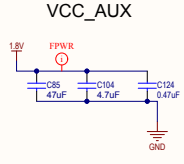

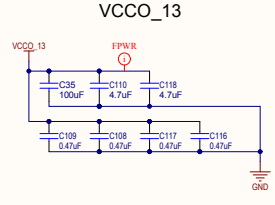

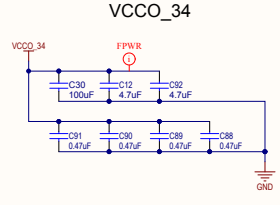

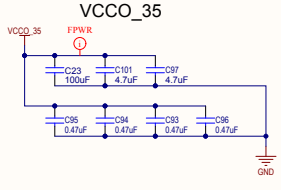

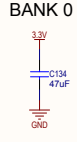

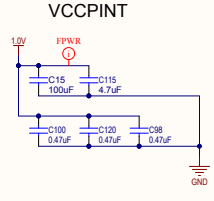

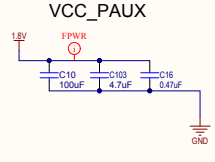

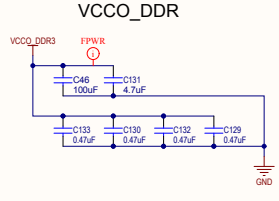

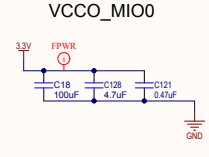

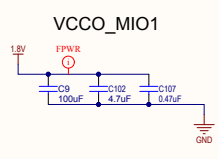

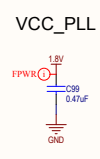

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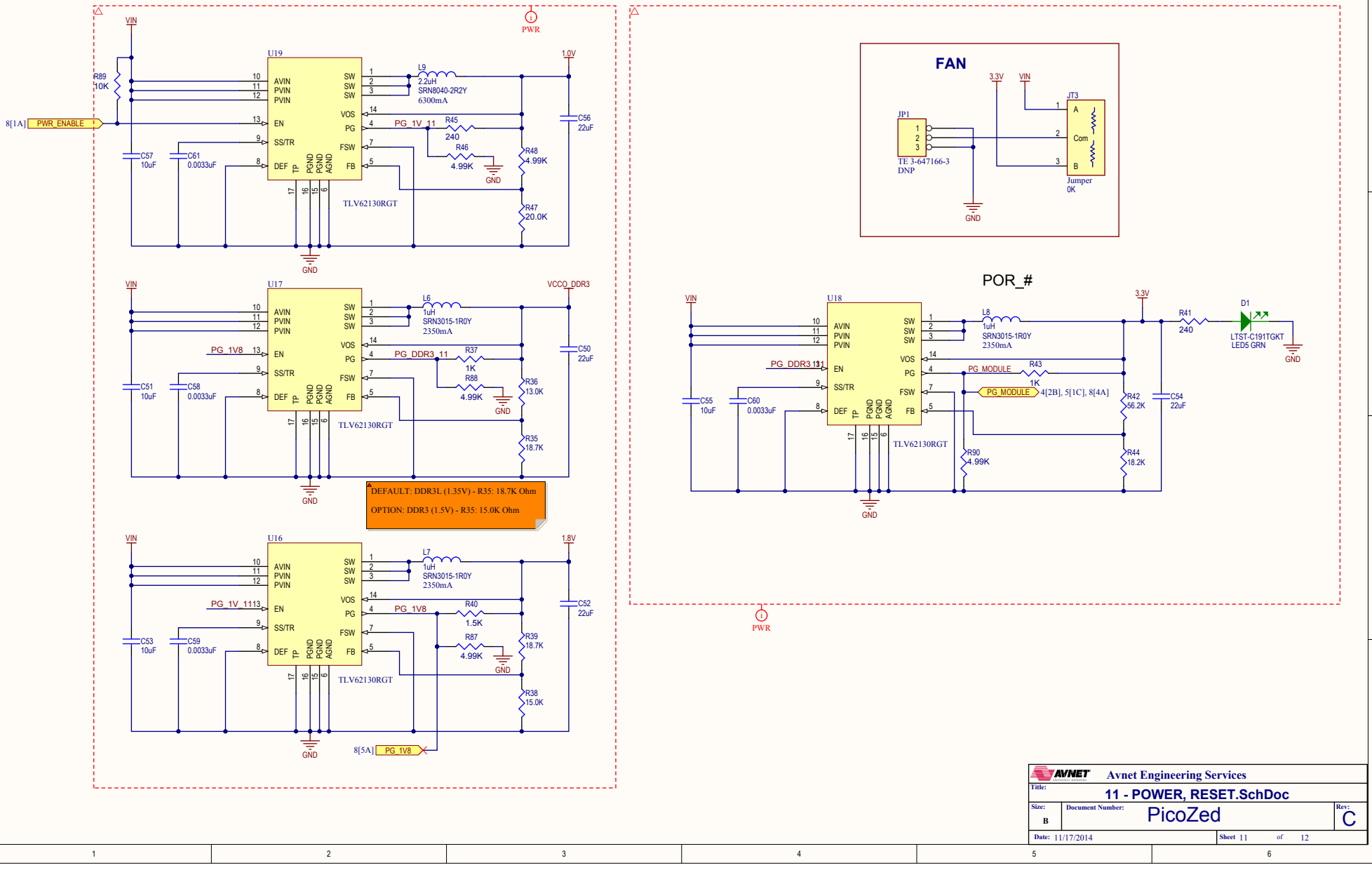

Avnet Engineering Services	
Title:	11 - POWER, RESET.SchDoc
Size: B	Document Number: PicoZed — Rev: C
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Revision Notes:

PicoZed Revision B1:
1) Multiplexed JX2 MIO signals with EMMC
2) Removed Push Button Footprint
3) Incorporated ETHERNET RESET circuit
4) Added bulk cap to AVDD18
5) Added GND Testpoints

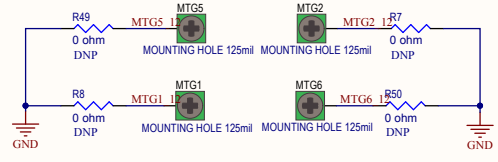
PicoZed Revision B2:
1) Updated BOOT MODE table

PicoZed Revision C:
1) Updated Block Diagram
2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
3) Added RC time constant to ETHERNET RESET
4) DDR3L / DDR3 Option Added
5) Modified resistor divider value on PG_1V8
6) Changed DDR3 Termination Regulator VLDOIN from 1.8V to 3.3V

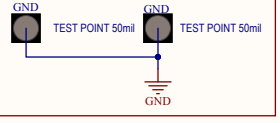
Mechanicals:

PCB
Z7PZ-Z70x0-PCB-C

PCB Mounting Holes



GND Test Points



Fansink Mounting Holes

Avnet Engineering Services		
Title: 12 - Back Page.SchDoc		
Size: B	Document Number: PicoZed	Rev: C
Date: 11/17/2014	Sheet 12 of 12	