Zynq PicoZed	
Avnet Engineering Services	
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PicoZed - Rev B

9/15/2014

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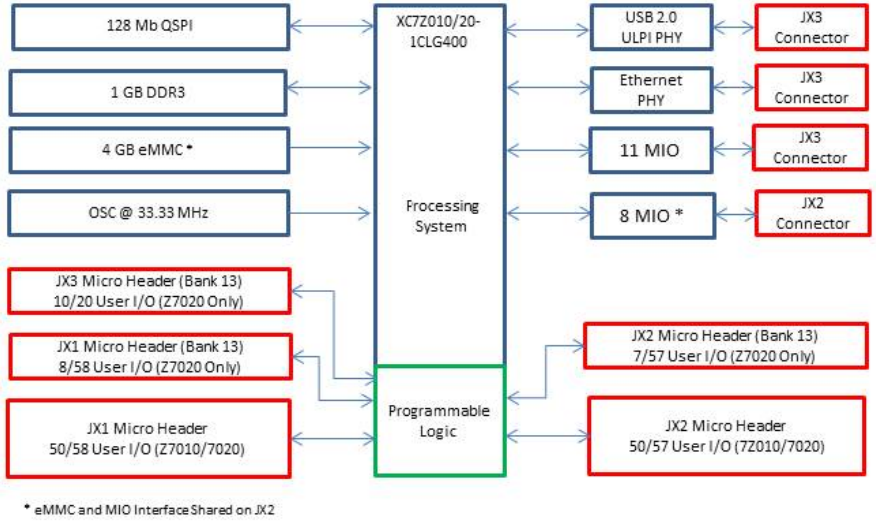
AVNET Avnet Engineering Services		
Title: 01 - Avnet Lead Sheet_B.SchDoc		
Size: B	Document Number: PicoZed	Rev: B
Date: 9/15/2014	Sheet 1 of 12	



AVNET Avnet Engineering Services		
Title: 02 - Block Diagram.SchDoc		
Size: B	Document Number: PicoZed	Rev: B
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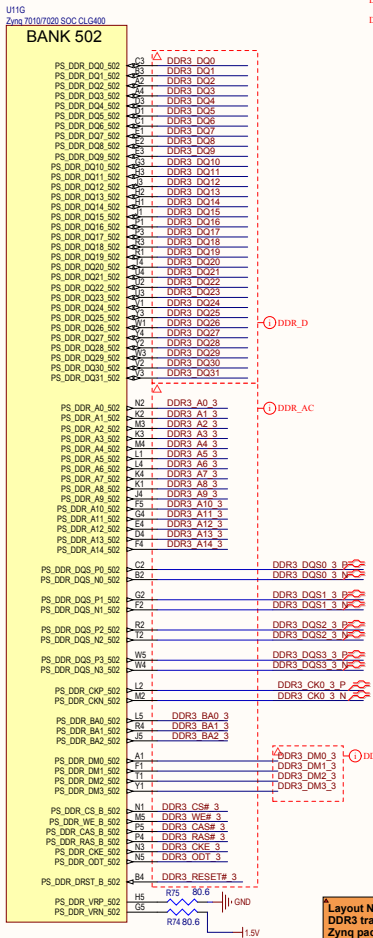
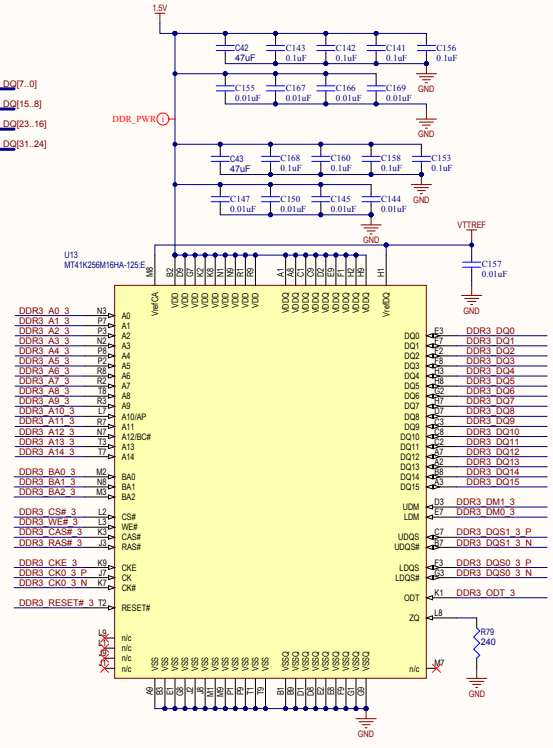
Zynq PS DDR - Bank 502



DDR_D_BL0 DDR3_DQ[7..0]
DDR_D_BL1 DDR3_DQ[15..8]
DDR_D_BL2 DDR3_DQ[23..16]
DDR_D_BL3 DDR3_DQ[31..24]

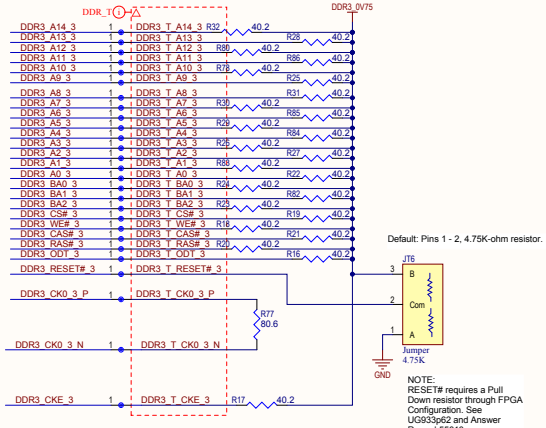
DDR3



Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.

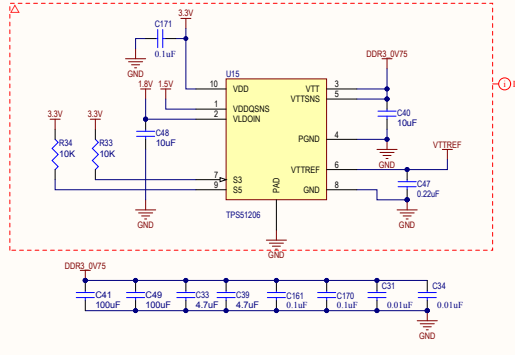
Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms



Default: Pins 1 - 2, 4.75K-ohm resistor.

NOTE:
RESET# requires a Pull Down resistor through FPGA Configuration. See UG953p62 and Answer Record 55616.

DDR3 Termination Supply



AVNET Avnet Engineering Services		
Title: 03 - DDR3.SchDoc		
Size: C	Document Number: PicoZed	Rev: B
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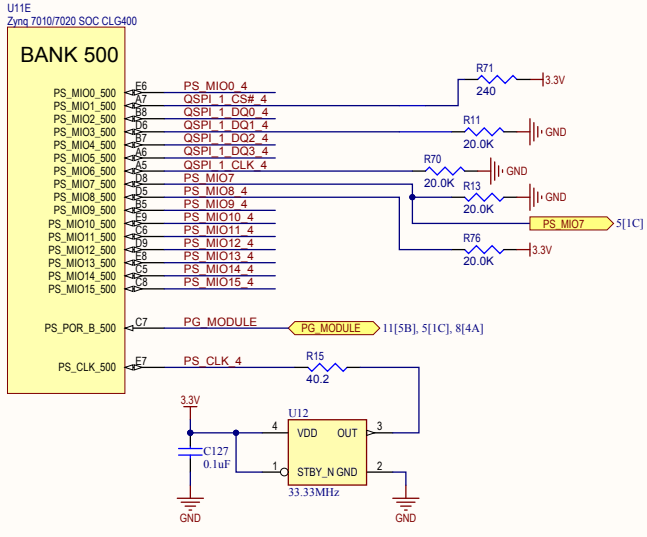
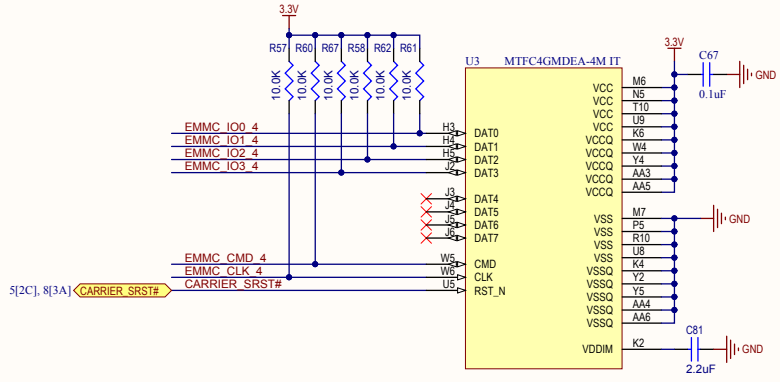
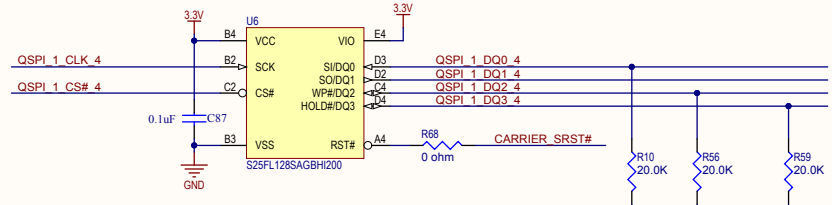
Zynq PS MIO - Bank 500



Embedded eMMC: 2GB, 4GB, 8GB

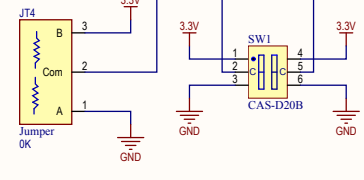


QSPI

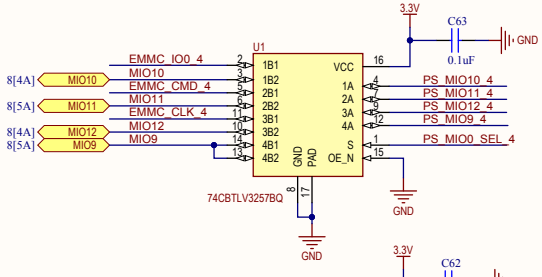


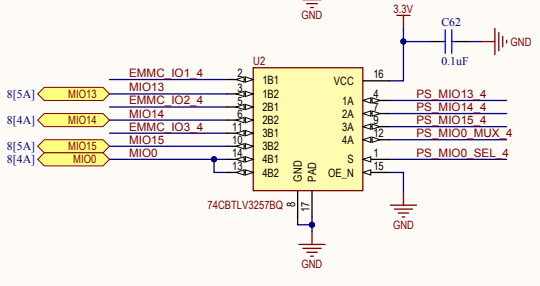
Boot Mode Select

BOOT MODE	JT4	SW1 (1-3)	SW1 (4-6)
QSPI	X	LOW (2-3)	HIGH (4-5)
SD CARD	X	HIGH (1-2)	HIGH (4-5)
JTAG	X	LOW (2-3)	LOW (5-6)
IND JTAG	HIGH (2-3)	LOW (2-3)	LOW (5-6)
CASCADE JTAG	LOW (1-2)	LOW (2-3)	LOW (5-6)

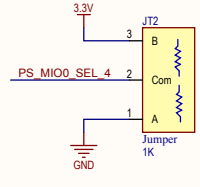


CASCADE JTAG - DEFAULT MODE

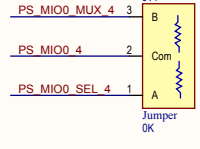




MUX SEL: Default - eMMC



PMOD / MUX SEL: Default - MUX SEL



Avnet Engineering Services			
Title: 04 - QSPI FLASH, eMMC.SchDoc			
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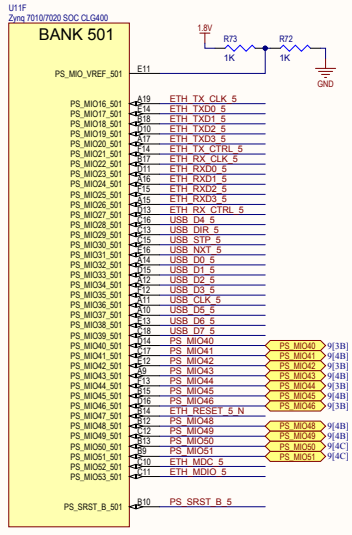
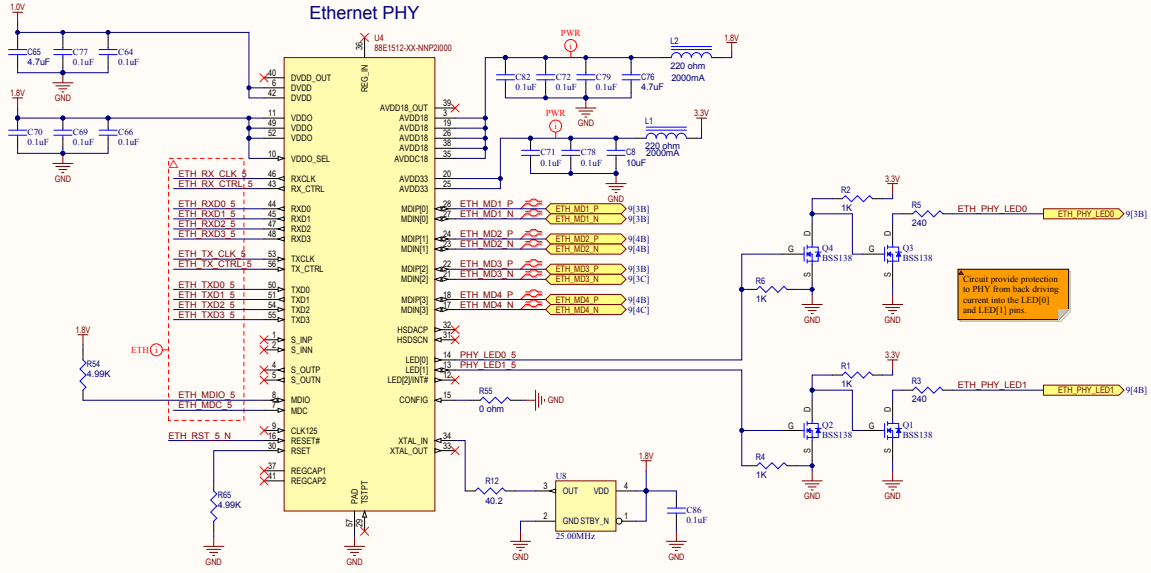
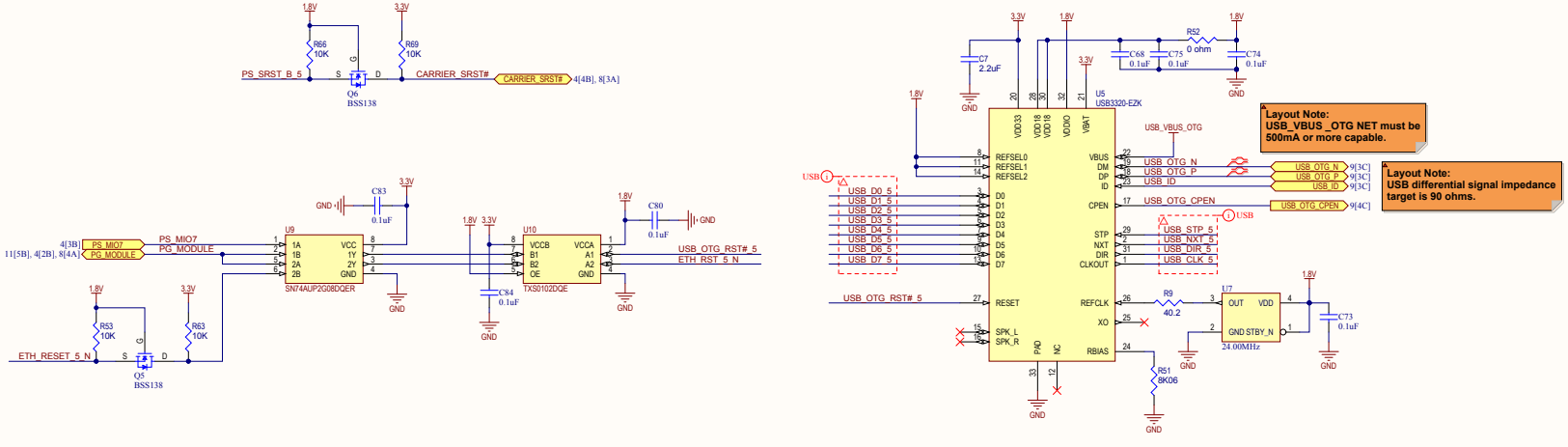
Zynq PS MIO - Bank 501



Ethernet PHY



USB 2.0 OTG



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Size: C	Document Number: PicoZed	Rev: B	
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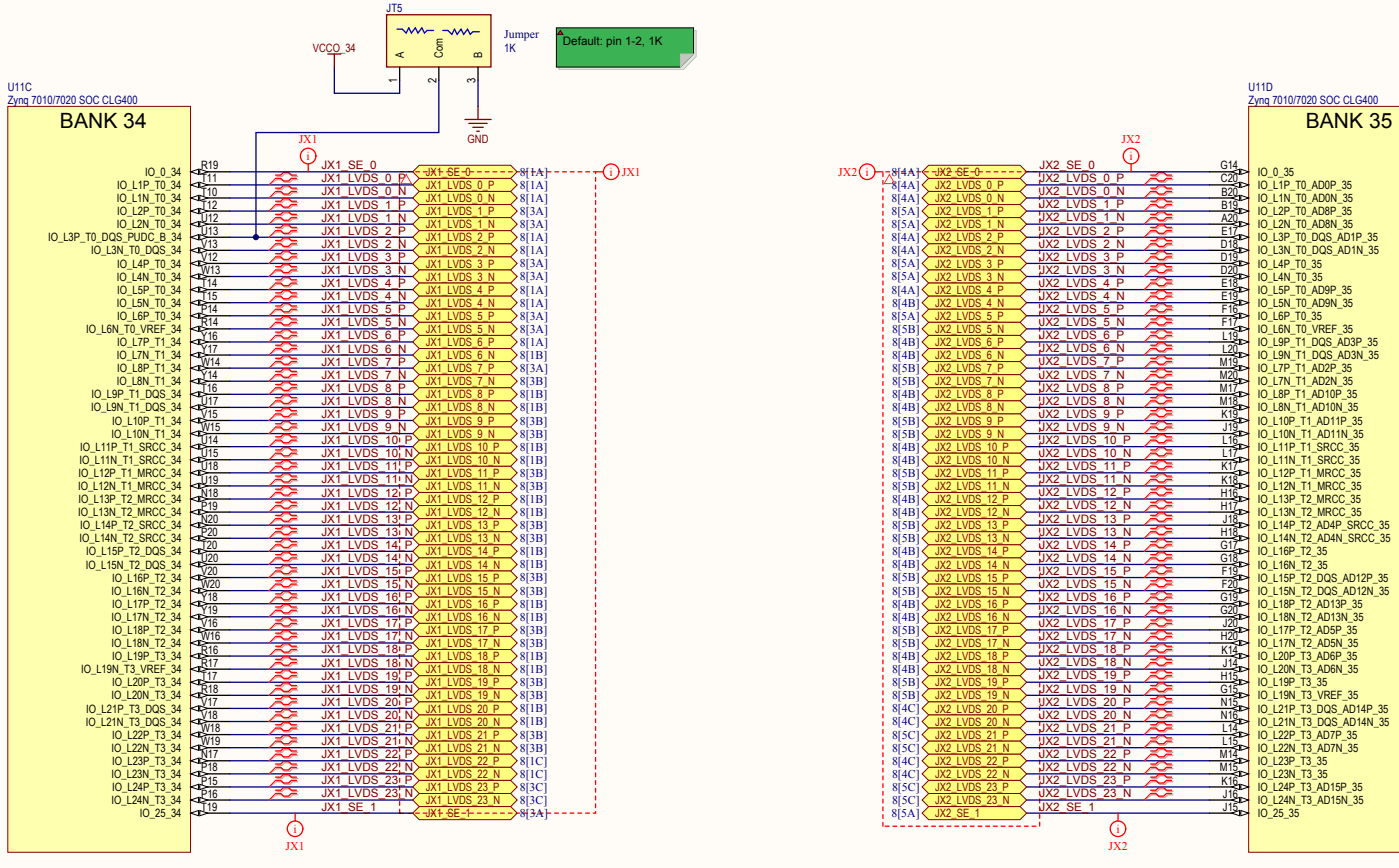

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Size: B	Document Number: PicoZed — Rev: B
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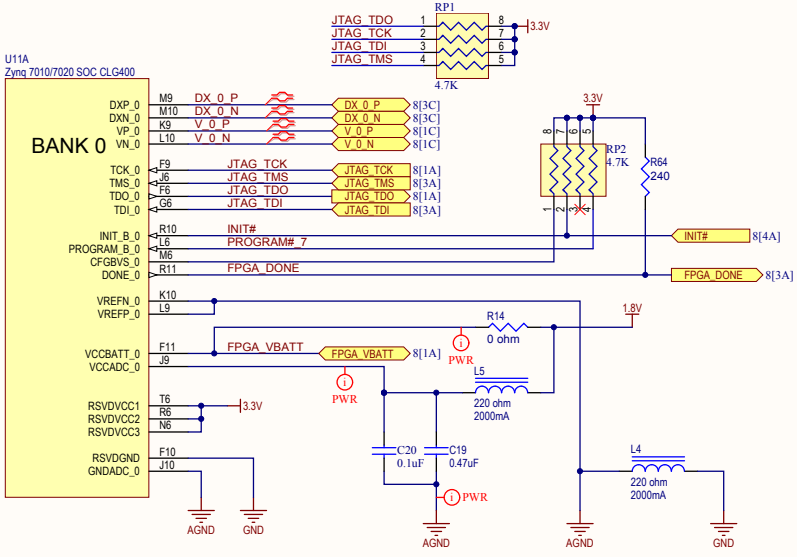

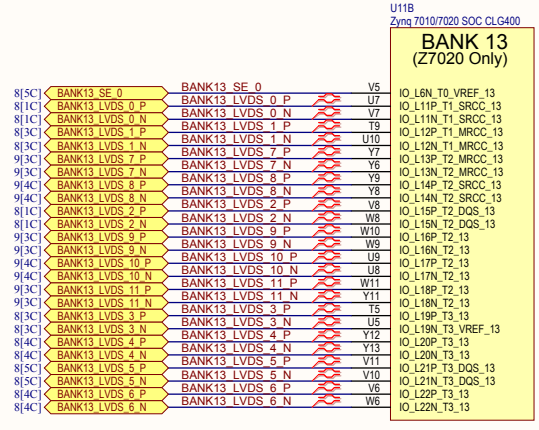

Avnet Engineering Services	
Title:	07 - BANK 0, BANK13, JTAG.SchDoc
Size: B	Document Number: PicoZed
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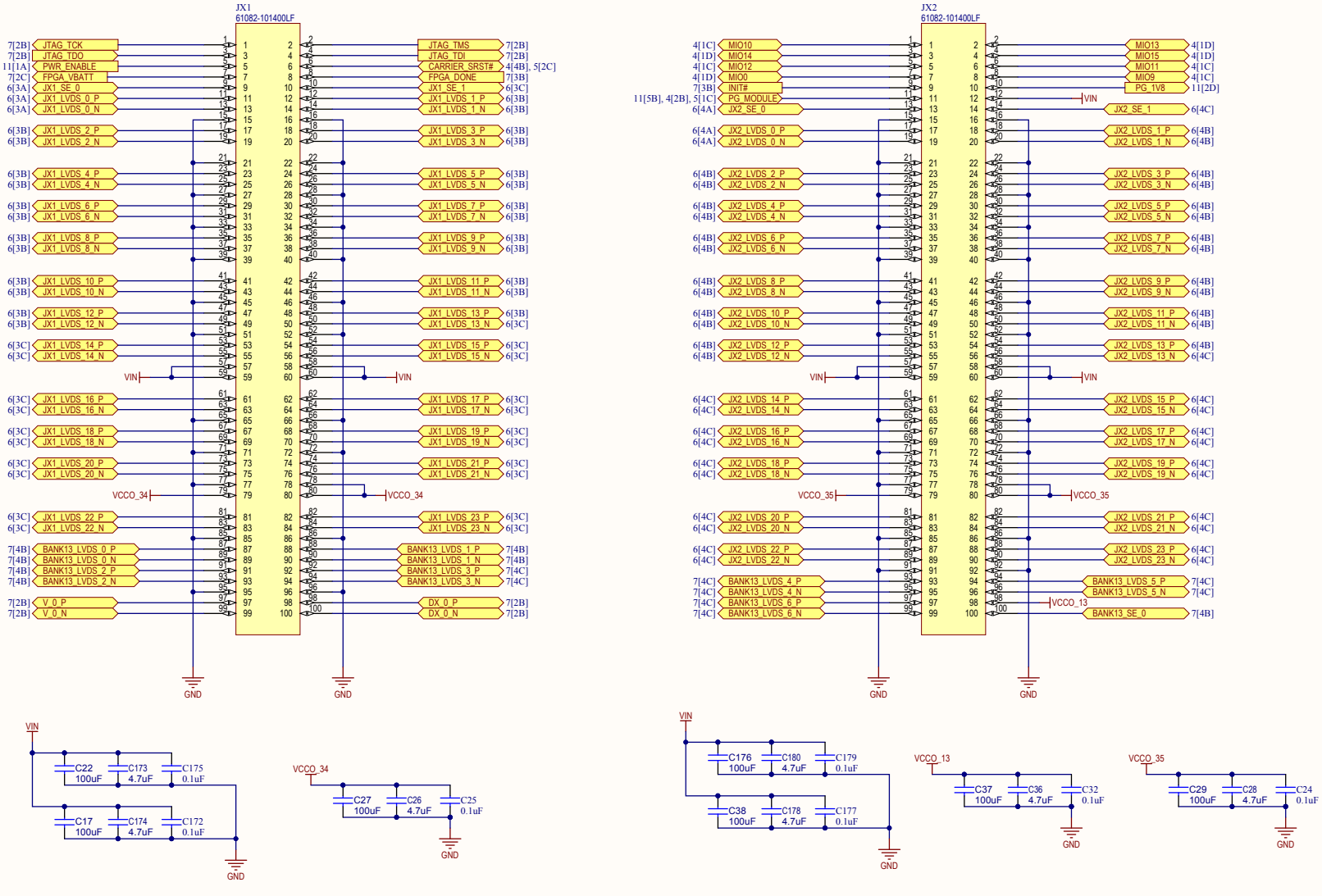

Avnet Engineering Services		
Title: 08 - MICROHEADERS - JX1 and JX2.SchDoc		
Size: B	Document Number: PicoZed	Rev: B
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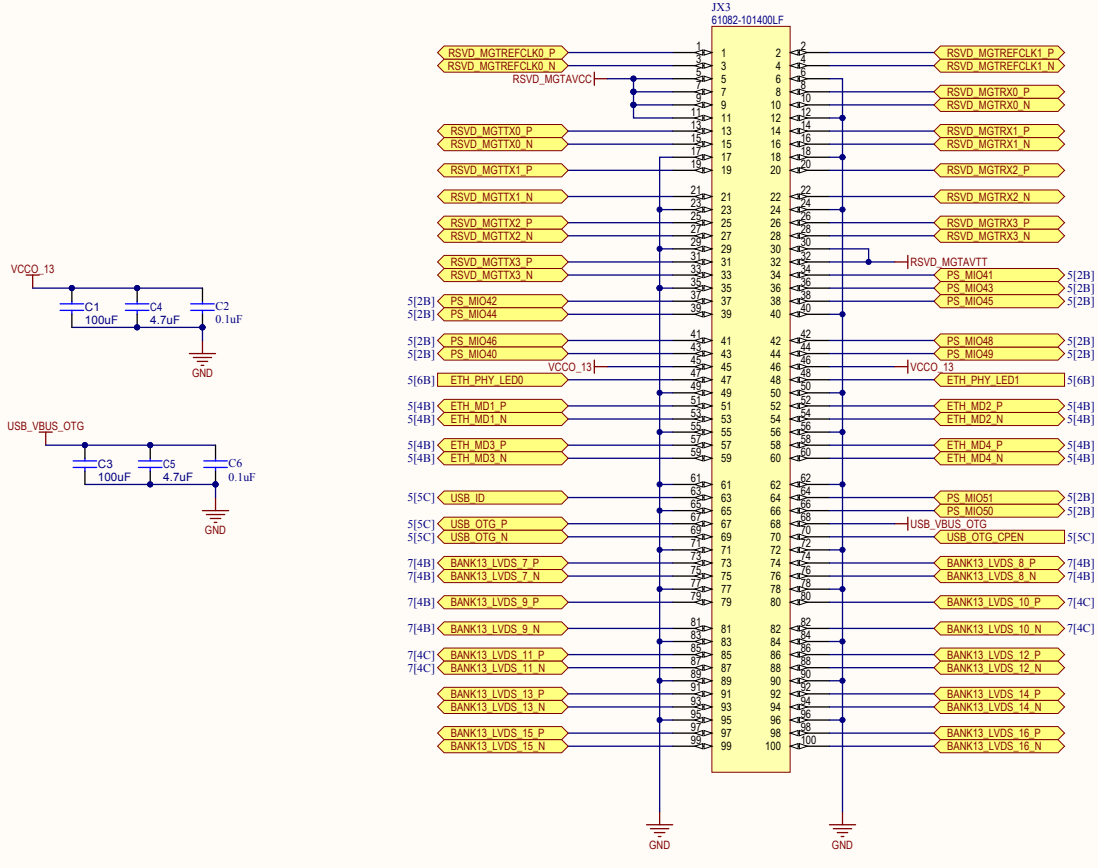

All RSVD_MGT* signals are RESERVED for devices with MGTs.

ZYNQ MIO POTENTIAL MAPPING OPTIONS:

SDIO INTERFACE
PS_MIO40 - SD_CLK through a 40.2-ohm RES
PS_MIO41 - SD_CMD
PS_MIO42 - SD_D0
PS_MIO43 - SD_D1
PS_MIO44 - SD_D2
PS_MIO45 - SD_D3
PS_MIO46 - SD_CD

UART INTERFACE
PS_MIO48 - UART_RXD (Tie to the TXD pin of a UART)
PS_MIO49 - UART TXD (Tie to the RXD pin of a UART)

BANK13_LVDS_12_P/N thru BANK13_LVDS_16_P/N is reserved for larger density BANK13

Avnet Engineering Services		
Title: 09 - MICROHEADER - JX3.SchDoc		
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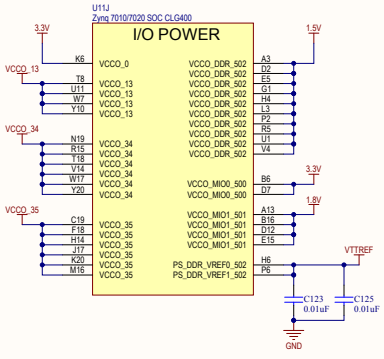

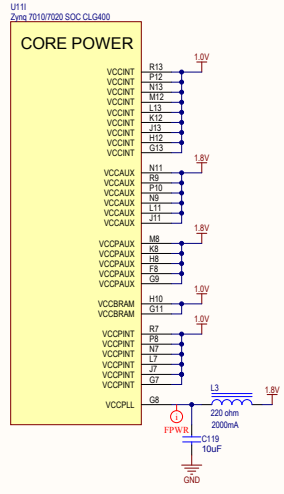

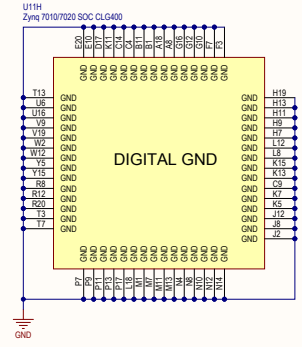

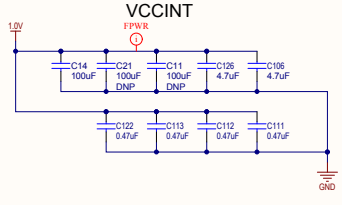

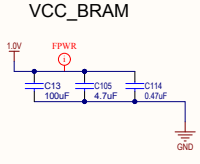

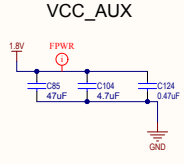

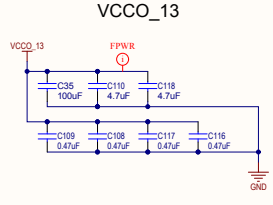

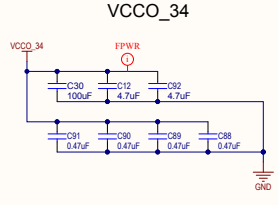

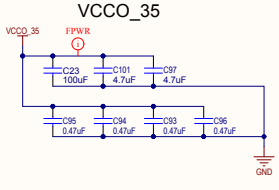

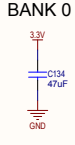

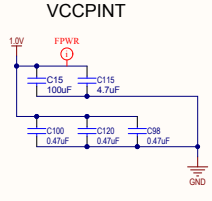

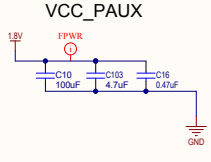

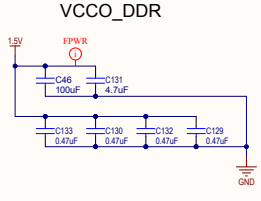

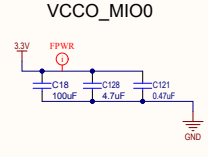

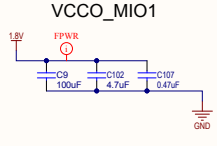

AVNET Avnet Engineering Services		
Title: 10 - DEVICE POWER.SchDoc		
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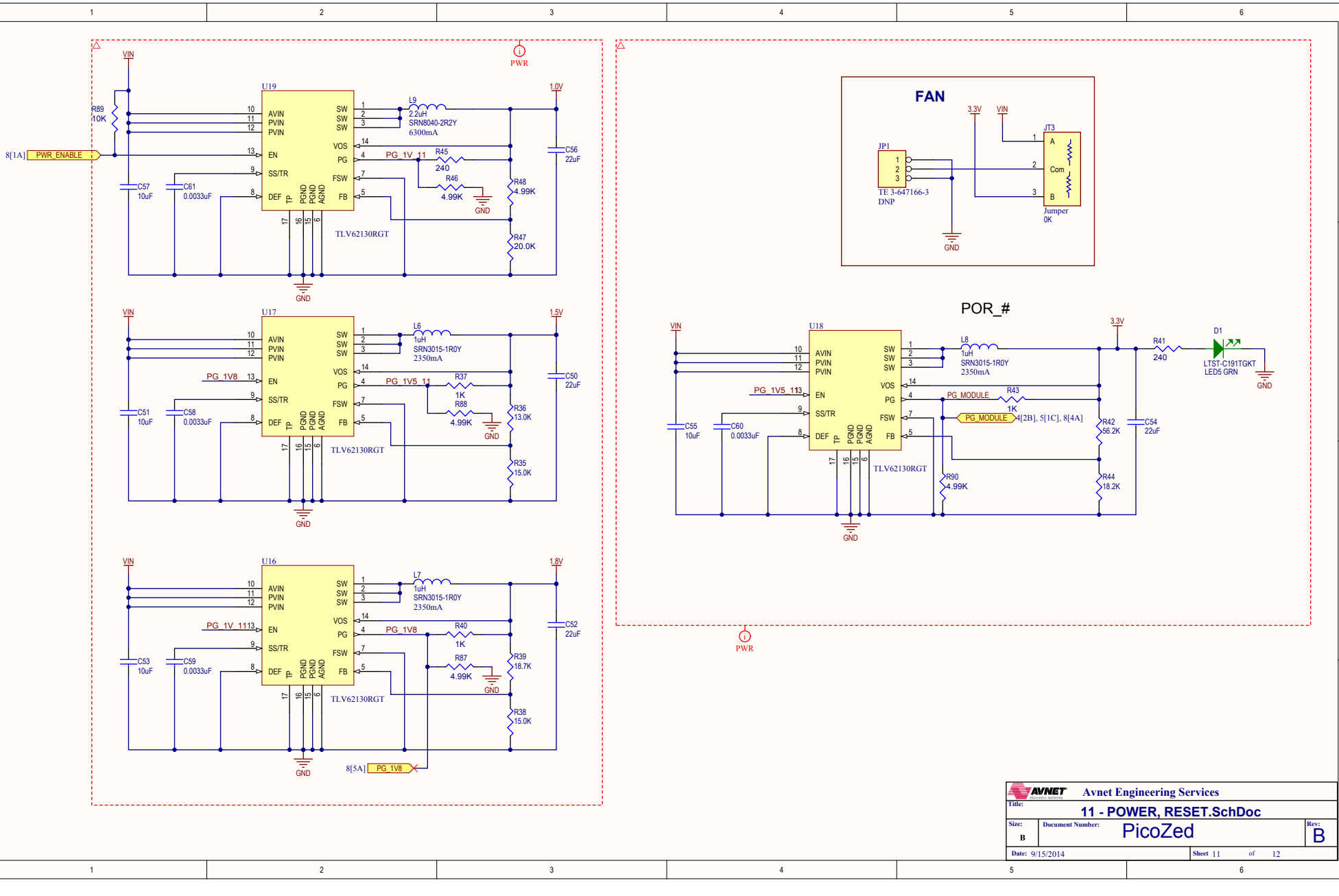

Avnet Engineering Services	
Title:	11 - POWER, RESET.SchDoc
Size: B	Document Number: PicoZed — Rev: B
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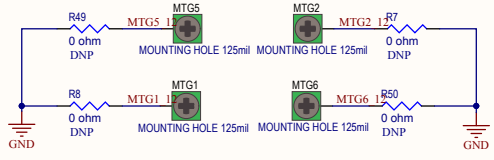
Revision Notes:

02 Sep 2014
1) Multiplexed JX2 MIO signals with EMMC
2) Removed Push Button Footprint
3) Incorporated ETHERNET RESET circuit
4) Added bulk cap to AVDD18
5) Added GND Testpoints

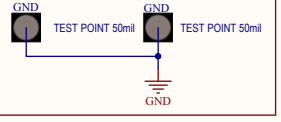
15 Sep 2014
1) Updated BOOT MODE table

Mechanicals:

PCB Mounting Holes



GND Test Points



Fansink Mounting Holes

Avnet Engineering Services		
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