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1 Formeln

- CLIAF (Neftci 2011):

$$C\frac{\mathrm{d}}{\mathrm{d}x}V_m = I(t) - \beta + I_{fb}e^{\frac{\kappa}{U_T}(V_m - V_{th})}$$

2 Abkürzungen

AER - Address Event Representation
CLIAF - Constant Leaky Integrate And Fire neuron
DNC - Digital Network Chip
FPGA - Field Programmable Gate Array
HH - Hodgkin Huxley neuron model
HICANN - High Input Count Analog Neural Network
IAF - Integrate-and-fire neuron model
LTD - Long Term Depression
LTP - Long Term Potention
LTU - Linear Threshold Unit
STDP - Spike Timing Dependent Plasticity
sWTA - Soft Winner-Take-All Network

3 Definitionen

- AER: Communication Protocoll which describes spikes from sources
- overconstrained: equations outnumber the unknowns

4 Notizen zu wichtigen Arbeiten

4.1 Neftci 2010: A Device Mismatch Compensation Method for VLSI Neural Networks

- transistor properties mismatch as major VLSI problem
- mismatch compensation algorithm through connectivity
- no layout disadvantage (no extra HW memory)
- exploits Address-Event Representation
- metaplasticity as homeostatic mechanism for homogeneous population response
- change connectivity profile (# or %) to normalize response strength
- test: sWTA as possible general purpose structure
- synaptic scaling method to normalize response of VLSI sWTA with HW respresentation and constraints (e.g. spiking output)
- synaptic circuits with linear filter (1st order) to summarize different sources
- 1 synapse emulates synapses with same time constant and weight → modulates coupling strength between populations
- test of theory with sWTA and an compensation matrix → up to 40% less variability and same mean in transfer function

- fig 1: bumps getting homogeneous after compensation (reduced mismatch)
- increased discrimination performance: generally better win rate of stronger input population

4.2 Neftci 2011: A Systematic Method for Configuring VLSI Networks of Spiking Neurons

- subthreshold transistor → small signal → prone to noise and mismatch
- automatic bidirectional parameter mapping technique (high-level NN simulation ←→ VLSI)
- algorithm is general and usable if LTU behaviour approximated in circuit (IAF for example)
- approx possible if a regime exists in which neurons have threshold-activation linear function
- algorithm: standart parameter translation + determining bias voltage
- LTU ←→ CLIAF model ←→ CLIAF VLSI
-

4.3 Neftci 2013: Synthesizing cognition in neuromorphic electronic systems

4.4 Sheik 2011: Systematic configuration and automatic tuning of neuromorphic Systems

4.5 Gao 2012: Dynamical System Guided Mapping of Quantitative Neuronal Models Onto Neuromorphic Hardware

4.6 Grassia 2011: Tunable neuromimetic integrated system for emulating cortical neuron models

4.7 Brüderle Dissertation 2009: Neuroscientific Modeling with a Mixed-Signal VLSI Hardware System

4.8 Brüderle 2011: A Comprehensive Workflow for General-Purpose Neural Modeling with Highly Configurable Neuromorphic Hardware Systems

4.9 Schwartz Dissertation 2011: Reproducing Biologically Realistic Regimes on a Highly-Accelerated Neuromorphic Hardware System

5 Mögliche wichtige Arbeiten

- determining unknown parameters and state variables of physical systems by measurements of a limited number of observables (parameter estimation methods)
- Brillinger 2008
- Keat, Reinagel, Reid, Meister 2001
- Paninski, Pillow, Simoncelli 2004
- Okatan, Wilson, Brown 2005
- Huys, Ahrens, Paninski 2006
- Abarbanel, Creveling, Farsian, Kostuk 2009

6 Notizen

- iterative Parametersuche kann durch Heuristik verbessert werden
(Russel, Orchard, Etienne-Cummings 2007)
- IAF sind strombasiert
- Das erste IAF Modell ist das Axon-Hillock Modell von Mead
- Das A-H-Modell nutzt einen konstanten Strom als leak statt Konduktanz
- LTUs sind simple Modelle, die keine Spikezeitinformation und nichtlineare Elemente beinhalten

7 Kleine nützliche Wortsammlung

- parameter estimation/extraction/translation/mapping